

裕太微电子
MotorComm

Motorcomm YT8614

Datasheet

INTEGRATED QUAD 10/100/1000M ETHERNET
COMBO TRANSCEIVER

VERSION DRAFT_11
DATE 2020-12-23

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Revision History

Revision	Release Date	Summary
DRAFT	2019/09/11	Initial
Draft 01	2019/09/12	Update
Draft 02	2019/10/18	Modify Pin arrangement
Draft 03	2020/02/06	1. Modify Errors. 2. Add register description.
Draft 04	2020/03/20	Add mechanical information.
Draft 05	2020/04/27	1. Modify pin assignment. 2. Add AC characteristics.
Draft 06	2020/08/04	1. Modify pin34 description. 2. Add Power Consumption and Thermal Resistance.
Draft 07	2020/08/21	1. Modify Maximum Power Consumption. 2. Modify Thermal Resistance.
Draft 08	2020/08/28	1. Update DC characteristics, Thermal Resistance and SGMII Receiver Characteristics. 2. Add QSGMII AC Characteristics.
Draft 09	2020/08/31	1. Update DC & AC characteristics. 2. Update Maximum Power Consumption.
Draft 10	2020/12/16	1. Update register description. 2. Update DC & AC characteristics.
Draft 11	2020/12/23	Update Oscillator/External Clock Requirement.

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1. General Description

The YT8614 integrates quad independent 10/100/1000M Ethernet transceivers and four SerDes interface into a single IC, and performs all the physical layer (PHY) functions for 1000BASE-T, 100BASE-TX, and 10BASE-T Ethernet on category 5 UTP cable except 1000BASE-T half-duplex. 10BASE-T functionality can also be achieved on standard category 3 or 4 cable.

This device also supports four dual media ports and can support up to four 100BASE-FX, 1000BASE-X.

This device includes PCS, PMA, and PMD sub-layers. They perform encoding/decoding, clock/data recovery, digital adaptive equalization, echo cancellers, crosstalk elimination, and line driver, as well as other required supporting circuit functions. The YT8614 also integrates an internal hybrid that allows the use of inexpensive 1:1 transformer modules.

Each of the four independent transceivers features an comprehensive QSGMII for reduced PCB trace. All transceivers can communicate with the MAC simultaneously through the same QSGMII.

1.1. TARGET APPLICATIONS

- High Port Density Switch
- QSGMII MAC
- Copper/Fiber Dual Media

1.2. System Application

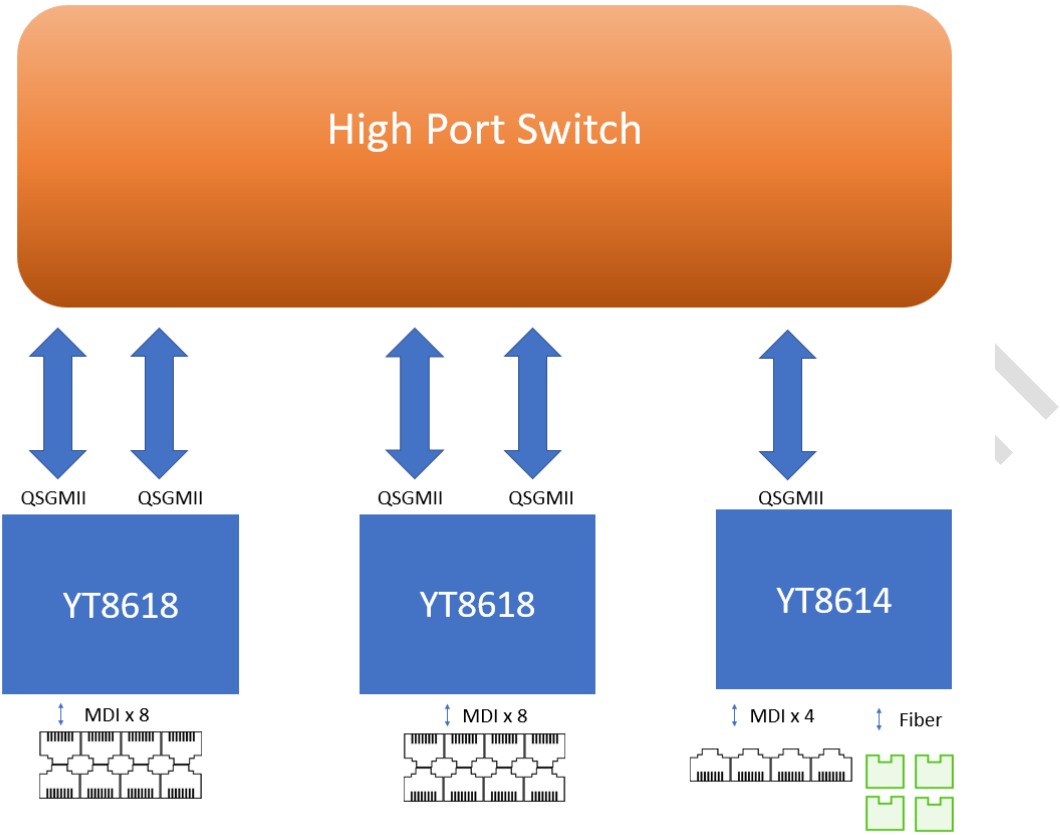


Figure 1. System Application

2. Features

- Integrated Quad 10/100/1000M Ethernet Transceiver with four SerDes interface
- Support QSGMII (Quad Serial Gigabit Media Independent Interface) in 10/100/1000M mode
- Support SGMII mode direct link to one designated Copper Giga PHY with speed adaption
- Physical interface supports 1000BASE-X
- Physical interface supports 100Base-FX
- Support LRE100-4, disabled by default
 - Cable reach up to 400 meter @100Mbps
- Supports IEEE 802.3az-2010 (Energy Efficient Ethernet)
 - EEE Buffering
 - Incorporates EEE buffering for seamless support of legacy MACs
- Supports crossover detection and auto correction
- Supports auto-detection and auto-correction of wiring pair swaps, pair skew, and pair polarity
- Supports Cable diagnostic
- Supports Link Down Power Saving (Sleep Mode)
- Supports one interrupt output to external CPU for notification
- Supports fast link failure indication
- Supports unidirection in 1000BASE-X/100Base-FX
- Supports 120m for CAT.5E cable in 1000BASE-T
- Supports Serial LED interface.
- Supports SyncE clock output Mux
 - Recover clock from either SerDes
 - Recover clock from either Copper PHY
 - From internal 25Mhz Clock
- SerDes Test pattern
 - PRBS-7/10
 - IDLE /K28.5 /D5.6
 - Customized define by user
 - SerDes BIST
- Packet Generator and Checker
- Low power consumption
- Easy layout, good EMI/EMS, and good thermal performance
- Supports 25MHz crystal or 3.3V OSC input

Motorcomm YT8614 Datasheet

- 3.3V and 1.2V power supply
- LQFP-176 E-PAD package

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3. PiN Assignment

3.1. YT8614 LQFP-176

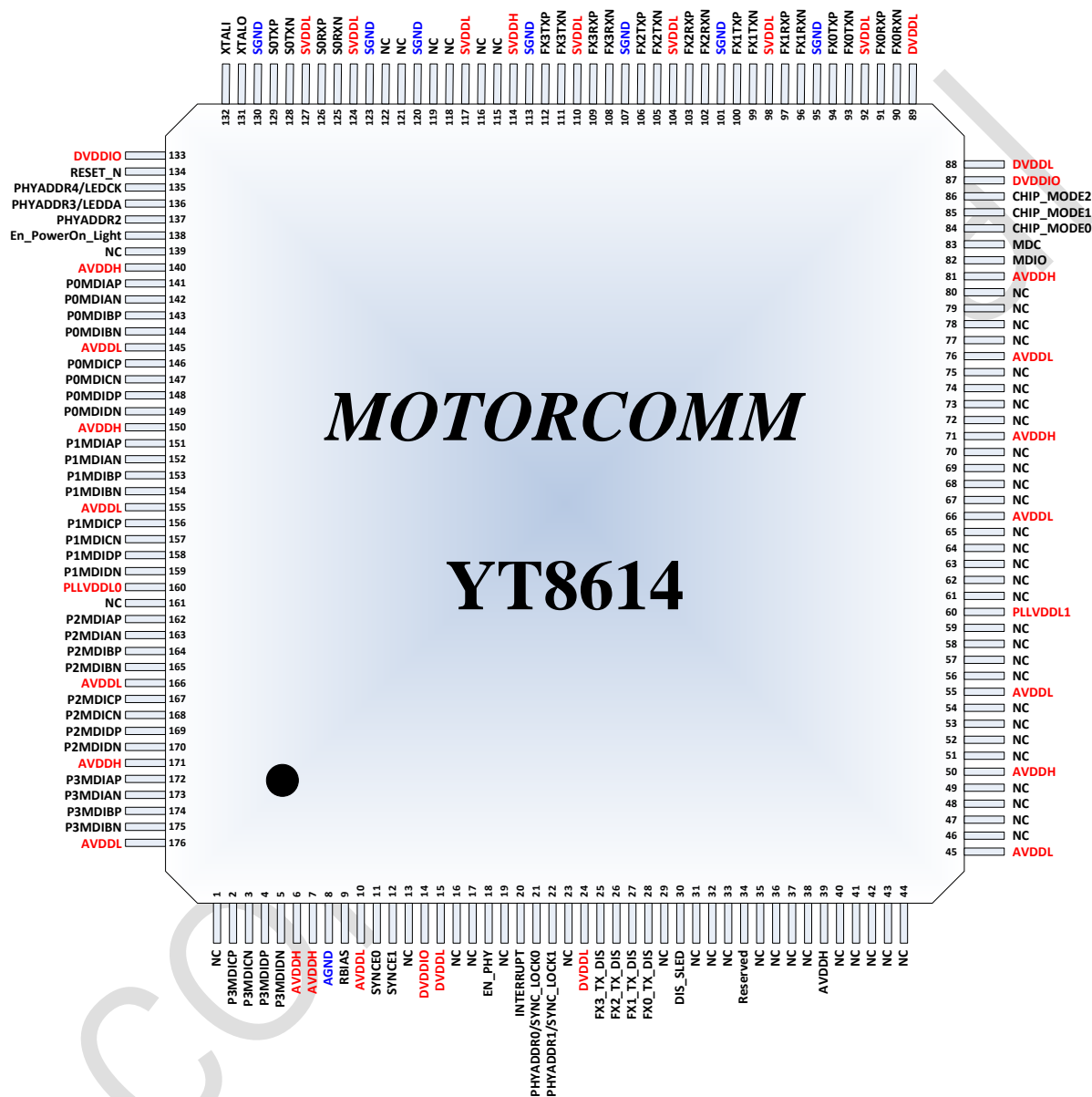


Figure 2. System Application

3.2. Pin Descriptions

- I: Input Pin
- AI: Analog Input Pin
- O: Output Pin
- AO: Analog Output Pin
- IO: Bidirectional Input/Output Pin
- AIO: Analog Bidirectional Input/Output Pin
- LI: Latched Input During Power UP
- P: Digital Power Pin
- AP: Analog Power Pin
- G: Digital Ground Pin
- AG: Analog Ground Pin
- PD: Internal Pull-Down
- PU: Internal Pull-UP
- SP: SerDes Power Pin
- SG: SerDes Ground Pin
- OD: Open Drain
- XT: Crystal Related

3.2.1. ALL pins

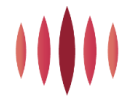
Table 1. All Pins Assignment

NO.	Name	TYPE
1	NC	-
2	P3MDICP	AIO
3	P3MDICN	AIO
4	P3MDIDP	AIO
5	P3MDIDN	AIO
6	AVDDH	AP
7	AVDDH	AP
8	AGND	AG
9	RBIAS	AO
10	AVDDL	AP
11	SYNCE0	AO
12	SYNCE1	AO
13	NC	-
14	DVDDIO	P
15	DVDDL	P
16	NC	-
17	NC	-
18	EN_PHY	LI/PU
19	NC	-
20	INTERRUPT	O/OD
21	PHYADDR0/SYNC_L OCK0	LI/O/PD
22	PHYADDR1/SYNC_L OCK1	LI/O/PD
23	NC	-
24	DVDDL	P
25	FX3_TX_DIS	O/PU
26	FX2_TX_DIS	O/PU
27	FX1_TX_DIS	O/PU
28	FX0_TX_DIS	O/PU
29	NC	-
30	DIS_SLED	LI/PU
31	NC	-
32	NC	-
33	NC	-
34	Reserved	PD

NO.	Name	TYPE
35	NC	-
36	NC	-
37	NC	-
38	NC	-
39	AVDDH	AP
40	NC	-
41	NC	-
42	NC	-
43	NC	-
44	NC	-
45	AVDDL	AP
46	NC	-
47	NC	-
48	NC	-
49	NC	-
50	AVDDH	AP
51	NC	-
52	NC	-
53	NC	-
54	NC	-
55	AVDDL	AP
56	NC	-
57	NC	-
58	NC	-
59	NC	-
60	PLLVDL1	AP
61	NC	-
62	NC	-
63	NC	-
64	NC	-
65	NC	-
66	AVDDL	AP
67	NC	-
68	NC	-

NO.	Name	TYPE
69	NC	-
70	NC	-
71	AVDDH	AP
72	NC	-
73	NC	-
74	NC	-
75	NC	-
76	AVDDL	AP
77	NC	-
78	NC	-
79	NC	-
80	NC	-
81	AVDDH	AP
82	MDIO	IO/PU
83	MDC	I/PD
84	CHIP_MODE0	LI/PU
85	CHIP_MODE1	LI/PU
86	CHIP_MODE2	LI/PU
87	DVDDIO	P
88	DVDDL	P
89	DVDDL	P
90	FX0RXN	AI
91	FX0RXP	AI
92	SVDDL	SP
93	FX0TXN	AO
94	FX0TXP	AO
95	SGND	SG
96	FX1RXN	AI
97	FX1RXP	AI
98	SVDDL	SP
99	FX1TXN	AO
100	FX1TXP	AO
101	SGND	SG
102	FX2RXN	AI
103	FX2RXP	AI
104	SVDDL	SP

NO.	Name	TYPE
107	SGND	SG
108	FX3RXN	AI
109	FX3RXP	AI
110	SVDDL	SP
111	FX3TXN	AO
112	FX3TXP	AO
113	SGND	SG
114	SVDDH	SP
115	NC	-
116	NC	-
117	SVDDL	SP
118	NC	-
119	NC	-
120	SGND	SP
121	NC	-
122	NC	-
123	SGND	SG
124	SVDDL	SP
125	S0RXN	AO
126	S0RXP	AO
127	SVDDL	SP
128	S0TXN	AI
129	S0TXP	AI
130	SGND	SG
131	XTALO	XT
132	XTALI	XT
133	DVDDIO	P
134	RESET_N	I/PU
135	PHYADDR4/LEDCK	LI/O/PD
136	PHYADDR3/LEDDA	LI/O/PD
137	PHYADDR2	LI/PD
138	En_PowerOn_Light	LI/PU
139	NC	-
140	AVDDH	AP
141	P0MDIAP	IO
142	P0MDIAN	AIO



Motorcomm YT8614 Datasheet

105	FX2TXN	AO
106	FX2TXP	AO
NO.	Name	TYPE
145	AVDDL	AP
146	P0MDICP	AIO
147	P0MDICN	AIO
148	P0MDIDP	AIO
149	P0MDIDN	AIO
150	AVDDH	AP
151	P1MDIAP	AIO
152	P1MDIAN	AIO
153	P1MDIBP	AIO
154	P1MDIBN	AIO
155	AVDDL	AP
156	P1MDICP	AIO
157	P1MDICN	AIO
158	P1MDIDP	AIO
159	P1MDIDN	AIO
160	PLLVDL0	AP
161	NC	-

143	P0MDIBP	AIO
144	P0MDIBN	AIO
NO.	Name	TYPE
162	P2MDIAP	AIO
163	P2MDIAN	AIO
164	P2MDIBP	AIO
165	P2MDIBN	AIO
166	AVDDL	AP
167	P2MDICP	AIO
168	P2MDICN	AIO
169	P2MDIDP	AIO
170	P2MDIDN	AIO
171	AVDDH	AP
172	P3MDIAP	AIO
173	P3MDIAN	AIO
174	P3MDIBP	AIO
175	P3MDIBN	AIO
176	AVDDL	AP
EPAD	GND EPAD	EPAD

3.2.2. Media Dependent Interface Pins

Table 2. Media Dependent Interface Pins

Pin Name	Pin No.	Type	Description
P0MDIAP	141	AIO	Port 0 Media Dependent Interface A~D. For 1000BASE-T operation, differential data from the media is transmitted and received on all four pairs. For 100BASE-TX and 10BASE-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P0MDIAN	142	AIO	
P0MDIBP	143	AIO	
P0MDIBN	144	AIO	
P0MDICP	146	AIO	
P0MDICN	147	AIO	
P0MDIDP	148	AIO	
P0MDIDN	149	AIO	
P1MDIAP	151	AIO	Port 1 Media Dependent Interface A~D. For 1000BASE-T operation, differential data from the media is transmitted and received on all four pairs. For 100BASE-TX and 10BASE-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P1MDIAN	152	AIO	
P1MDIBP	153	AIO	
P1MDIBN	154	AIO	
P1MDICP	156	AIO	
P1MDICN	157	AIO	
P1MDIDP	158	AIO	
P1MDIDN	159	AIO	
P2MDIAP	162	AIO	Port 2 Media Dependent Interface A~D. For 1000BASE-T operation, differential data from the media is transmitted and received on all four pairs. For 100BASE-TX and 10BASE-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P2MDIAN	163	AIO	
P2MDIBP	164	AIO	
P2MDIBN	165	AIO	
P2MDICP	167	AIO	
P2MDICN	168	AIO	
P2MDIDP	169	AIO	
P2MDIDN	170	AIO	
P3MDIAP	172	AIO	Port 3 Media Dependent Interface A~D. For 1000BASE-T operation, differential data from the media is transmitted and received on all four pairs. For 100BASE-TX and 10BASE-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100ohm termination resistor.
P3MDIAN	173	AIO	
P3MDIBP	174	AIO	
P3MDIBN	175	AIO	
P3MDICP	2	AIO	
P3MDICN	3	AIO	
P3MDIDP	4	AIO	
P3MDIDN	5	AIO	

3.2.3. QSGMII Interface Pins

Table 3. QSGMII Interface Pins

Pin Name	Pin No.	Type	Description
S0RXP	126	AO	In the chip modes which QSGMII exists, these two pins are used for QSGMII Differential Output. 5GHz serial interfaces to transfer data to an External device that supports the QSGMII interface. Differential pairs have an internal 100ohm termination resistor. In other chip modes, these two pins are not used.
S0RXN	125	AO	
S0TXP	129	AI	In the chip modes which QSGMII exists, these two pins are used for QSGMII Differential Input. 5GHz serial interfaces to receive data from an External device that supports the QSGMII interface. Differential pairs have an internal 100ohm termination resistor. In other chip modes, these two pins are not used.
S0TXN	128	AI	

3.2.4. Serial LED Pins

Table 4. Serial LED Pins

Pin Name	Pin No.	Type	Description
DIS_SLED	30	LI/PU	Input Upon Reset, 1: Disable Serial LED function. 0: Enable Serial LED function.
PHYADDR4/ LEDCK	135	LI/O/PD	Output after reset if Serial LED is enabled by DIS_SLED = 0. Used for Serial LED Clock.
PHYADDR3/ LEDDA	136	LI/O/PD	Output after reset if Serial LED is enabled by DIS_SLED = 0. Used for Serial LED Data.

3.2.5. SYNCE Interface

Table 5. SYNCE Interface

Pin Name	Pin No.	Type	Description
SYNCE0	11	AO	SyncE0 clock output
SYNCE1	12	AO	SyncE1 clock output
PHYADDR0/ SYNC_LOCK0	21	LI/O/PD	Sync 0 lock indicator
PHYADDR1/ SYNC_LOCK1	22	LI/O/PD	Sync 1 lock indicator

3.2.6. Configuration Pins

Table 6. Configuration Pins

Pin Name	Pin No.	Type	Description
PHYADDR0/ SYNC_LOCK0	21	LI/O/PD	PHYADDR0, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. <i>Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.</i>
PHYADDR1/ SYNC_LOCK1	22	LI/O/PD	PHYADDR1, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. <i>Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.</i>
PHYADDR2	137	LI/PD	PHYADDR2, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. <i>Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.</i>
PHYADDR3/ LEDDA	136	LI/O/PD	PHYADDR3, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. <i>Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.</i>
PHYADDR4/ LEDCK	135	LI/O/PD	PHYADDR4, PHY Address Select. These pins are the 5-bit IEEE-specified PHY address. The states of these five pins are latched during power-up or reset. <i>Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.</i>
EN_PHY	18	LI/PU	Enable PHY Power 1: Power up all ports. 0: Power down all ports and set the MII register 0.11 power down as 1. <i>Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.</i>
CHIP_MODE2	86	LI/PU	CHIP MODE [2:0] refer to: 3'b000, 4x 1000base-X + Copper x4 3'b001, Reserved 3'b010, Qsgmii x1 + Copper x4 mode, 3'b011, Qsgmii x1 + Fiber x4 mode; 3'b100, Qsgmii x1 + Combo x4 mode; 3'b101, Qsgmii x1 + Combo x4 mode;
CHIP_MODE1	85	LI/PU	
CHIP_MODE0	84	LI/PU	

			3'b110, Qsgmii x1 + Sgmii(MAC) x4 mode; 3'b111, Sgmii(PHY) x4 + Copper x4 mode.
En_PowerOn_ Light	138	LI/PU	En_PowerOn_Light. 1: Enable Serial LED Power On Light. 0: Disable Serial LED Power On Light. <i>Note: This pin must be kept floating, and pulled high or low via an external 4.7k ohm resistor upon power on or reset.</i>

3.2.7. Miscellaneous Pins

Table 7. Miscellaneous Pins

Pin Name	Pin No.	Type	Description
MDC	83	I/PD	MII Management Interface Clock Input. The clock reference for the MII management interface. The maximum frequency support is 12.5MHz.
MDIO	82	IO/PU	MII Management Interface Data Input/Output. MDIO transfer management data in and out of the device synchronous to the rising edge of MDC.
INTERRUPT	20	O/OD	Interrupt output when Interrupt even occurs, active low. Always open drain, must pull-up to DVDDIO via a 4.7K resistor.
RESET_N	134	I/PU	Hardware Reset (Active Low Reset Signal). To complete the reset function, this pin must be asserted for at least 10ms. It must be pulled high for normal operation.
RBIAS	9	AO	Bias Resistor. An external 2.49 k Ω ±1% resistor must be connected between the RBIAS pin and GND
XTALI	132	XT	25MHz Crystal Clock Input. 25MHz±50ppm tolerance crystal reference or oscillator input. When using a crystal, connect a loading capacitor from each pad to ground. When either using an oscillator or driving an external 25MHz clock from another device, XTALO should be kept floating. The maximum XTALI input voltage is 3.3V.
XTALO	131	XT	25Mhz Crystal Clock Output. 25MHz±50ppm tolerance crystal output. Refer to XTALI.
Reserved	34	PD	Internal pull down. Recommended to be floating or connected to GND directly.
NC	1, 13, 16, 17, 19, 23,	-	NC pins and keep floating.

	29, 31, 32, 33, 35, 36, 37, 38, 40, 41, 42, 43, 44, 46, 47, 48, 49, 51, 52, 53, 54, 56, 57, 58, 59, 61, 62, 63, 64, 65, 67, 68, 69, 70, 72, 73, 74, 75, 77, 78, 79, 80, 115, 116, 118, 119, 121, 122, 139, 161		
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3.2.8. Power and GND Pins

Table 8. Power and GND Pins

Pin Name	Pin No.	Type	Description
AVDDH	6, 7, 39, 50, 71, 81, 140, 150, 171	AP	Analog High Voltage Power
AVDDL	10, 45, 55, 66, 76, 145, 155, 166, 176	AP	Analog Low Voltage Power
PLLVDDL0	160	AP	PLL Power This pin should be filtered with a low resistance series ferrite bead and 1000pF + 2.2μF shunt capacitors to ground
PLLVDDL1	60	AP	PLL Power This pin should be filtered with a low resistance series ferrite bead and 1000pF + 2.2μF shunt capacitors to ground
SVDDH	114	SP	QSGMII SerDes High Voltage Power
SVDDL	92, 98, 104, 110, 117, 124, 127	SP	QSGMII SerDes Low Voltage Power
DVDDIO	14, 87, 133	P	Digital I/O Power
DVDDL	15, 24, 88, 89	P	Digital Low Voltage Power

AGND	8	AG	Analog Ground
SGND	95, 101, 107, 113, 120, 123, 130	SG	SerDes Ground
GND	EPAD	G	Digital/Analog Ground

3.2.9. 1000BASE-X/100BASE-FX Interface Pins

Table 9. 1000BASE-X/100BASE-FX Interface Pins

Pin Name	Pin No.	Type	Description
FX0RXP	91	AI	Port 0 1000BASE-X Receiver Pair (1.25GHz Differential Signal Input).
FX0RXN	90		Port 0 100BASE-FX Receiver Pair (125MHz Differential Signal Input).
FX0TXP	94	AO	Port 0 1000BASE-X Transmit Pair (1.25GHz Differential Signal Output).
FX0TXN	93		Port 0 100BASE-FX Transmit Pair (125MHz Differential Signal Output).
FX1RXP	97	AI	Port 1 1000BASE-X Receiver Pair (1.25GHz Differential Signal Input).
FX1RXN	96		Port 1 100BASE-FX Receiver Pair (125MHz Differential Signal Input).
FX1TXP	100	AO	Port 1 1000BASE-X Transmit Pair (1.25GHz Differential Signal Output).
FX1TXN	99		Port 1 100BASE-FX Transmit Pair (125MHz Differential Signal Output).
FX2RXP	103	AI	Port 2 1000BASE-X Receiver Pair (1.25GHz Differential Signal Input).
FX2RXN	102		Port 2 100BASE-FX Receiver Pair (125MHz Differential Signal Input).
FX2TXP	106	AO	Port 2 1000BASE-X Transmit Pair (1.25GHz Differential Signal Output).
FX2TXN	105		Port 2 100BASE-FX Transmit Pair (125MHz Differential Signal Output).
FX3RXP	109	AI	Port 3 1000BASE-X Receiver Pair (1.25GHz Differential Signal Input).
FX3RXN	108		Port 3 100BASE-FX Receiver Pair (125MHz Differential Signal Input).
FX3TXP	112	AO	Port 3 1000BASE-X Transmit Pair (1.25GHz Differential Signal Output).
FX3TXN	111		Port 3 100BASE-FX Transmit Pair (125MHz Differential Signal Output).

FX0_TX_DIS	28	O/PU	Port 0 100BASE-FX/1000BASE-X Transmit Optical module Power Control
FX1_TX_DIS	27	O/PU	Port 1 100BASE-FX/1000BASE-X Transmit Optical module Power Control
FX2_TX_DIS	26	O/PU	Port 2 100BASE-FX/1000BASE-X Transmit Optical module Power Control
FX3_TX_DIS	25	O/PU	Port 3 100BASE-FX/1000BASE-X Transmit Optical module Power Control

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4. Function Description

4.1. Mode selction

4.1.1. QSGMII x 1 + Combo x 4

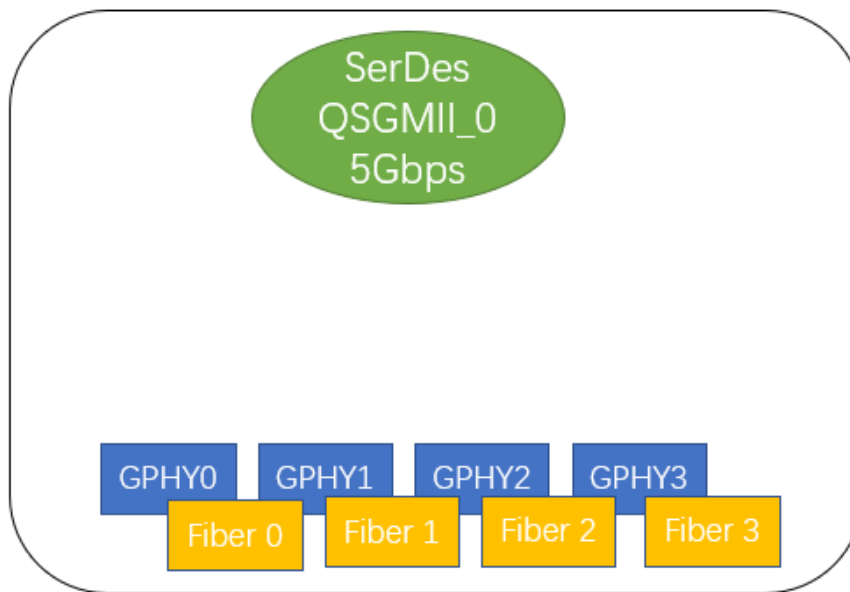


Figure 3. QSGMII x 1 + Combo x 4

4.1.2. QSGMII x 1 + Copper x 4

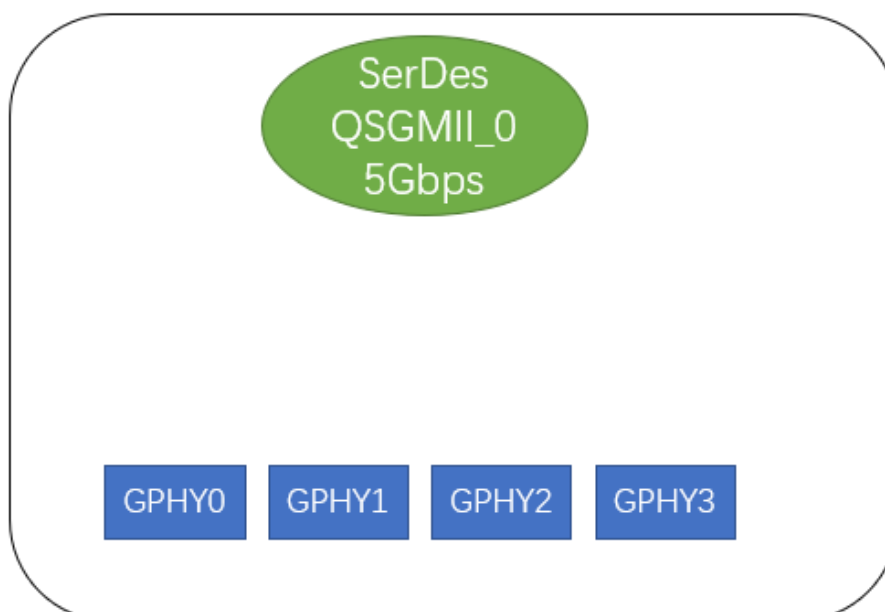


Figure 4. QSGMII x 1 + Copper x 4

4.1.3. QSGMII x 1 + Fiber x 4

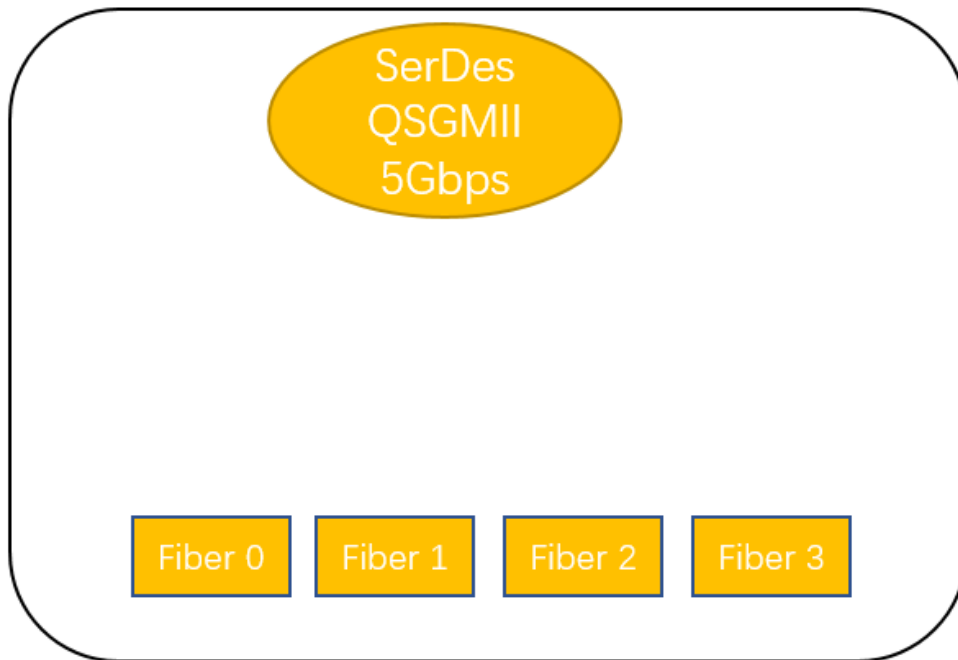


Figure 5. QSGMII x 1 + Fiber x 4

4.1.4. QSGMII x 1 + SGMII x 4

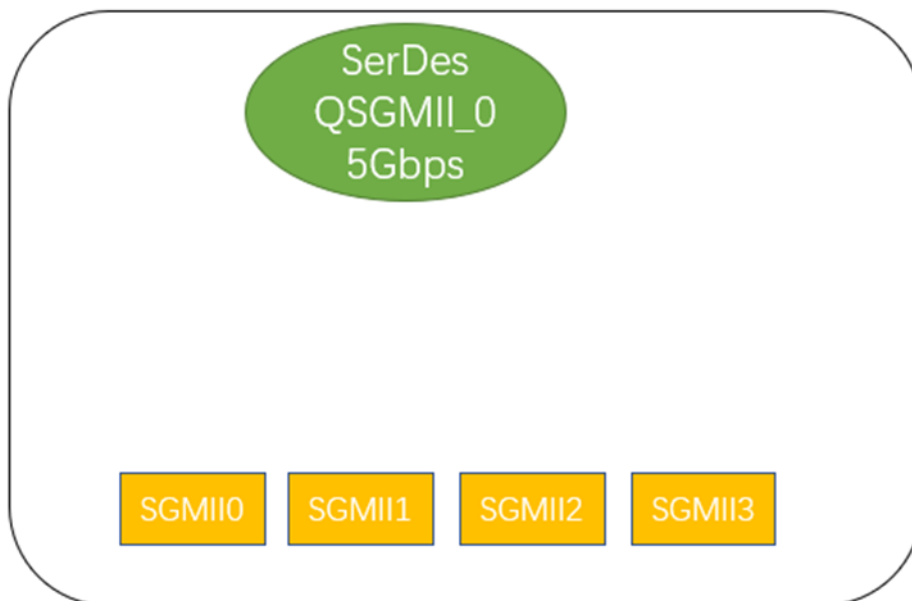


Figure 6. QSGMII x 1 + SGMII x 4

4.1.5. SGMII x 4 + Copper x 4

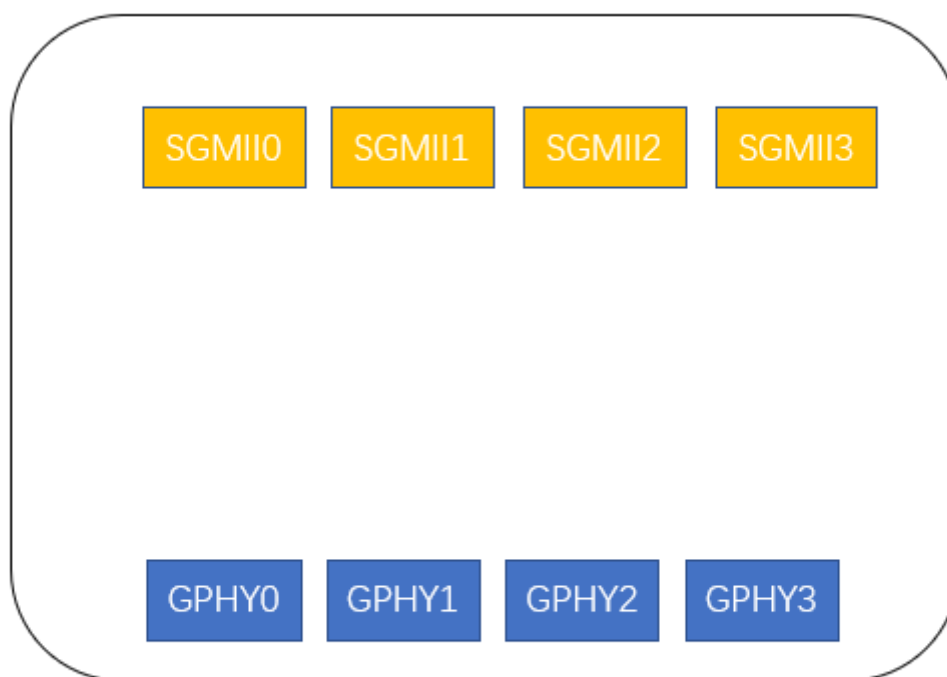


Figure 7. SGMII x 4 + Copper x 4

4.1.6. Copper x 4 + Fiber x 4

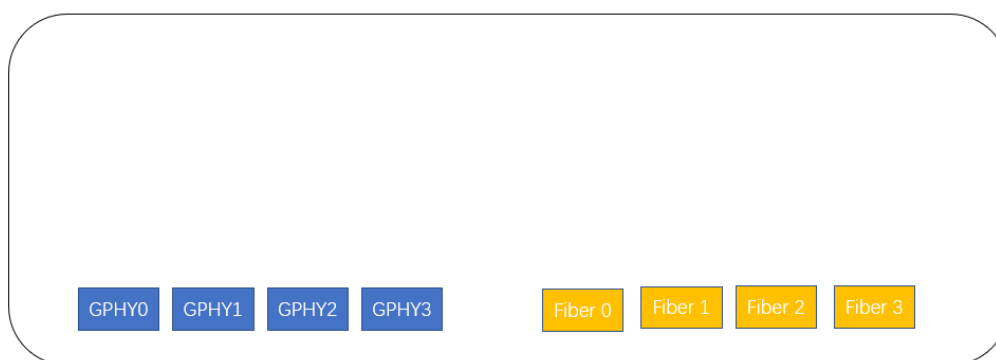


Figure 8. Copper x 4 + Fiber x 4

4.2. Transmit Functions

4.2.1. Transmit Encoder Modes

4.2.1.1. 1000BASE-T

In 1000BASE-T mode, the YT8614 scrambles transmit data bytes from the MAC interfaces to 9-bit symbols and encodes them into 4D five-level PAM signals over the four pairs of CAT.5E cable.

4.2.1.2. 100BASE-TX

In 100BASE-TX mode, 4-bit data from the MII is 4B/5B serialized, scrambled, and encoded to a three-level MLT3 sequence transmitted by the PMA.

4.2.1.3. 10BASE-Te

In 10BASE-Te mode, the YT8614 transmits and receives Manchester-encoded data.

4.3. Receive Functions

4.3.1. Receive Decoder Modes

4.3.1.1. 1000BASE-T

In 1000BASE-T mode, the PMA recovers the 4D PAM signals after accounting for the cabling conditions such as skew among the four pairs, the pair swap order, and the polarity of the pairs. The resulting code group is decoded into 8-bit data values. Data stream delimiters are translated appropriately and data is output to the MAC interfaces.

4.3.1.2. 100BASE-TX

In 100BASE-TX mode, the receive data stream is recovered and descrambled to align to the symbol boundaries. The aligned data is then parallelized and 5B/4B decoded to 4-bit data. This output runs to the MII receive data pins after data stream delimiters have been translated.

4.3.1.3. 10BASE-Te

In 10BASE-Te mode, the recovered 10 BASE-Te signal is decoded from Manchester then aligned.

4.4. LRE100-4

YT8614 supports a Motorcomm proprietary feature called LRE100-4, the long reach Ethernet application up to 400m at 100Mbps data rate by 4-pairs in the CAT.5E UTP cable.

4.5. Management Interface

The Status and Control registers of the device are accessible through the MDIO and MDC serial interface. The functional and electrical properties of this management interface comply with IEEE 802.3, Section 22 and also support MDC clock rates up to 12.5 MHz.

4.6. Auto-Negotiation

The YT8614 negotiates its operation mode using the auto negotiation mechanism according to IEEE 802.3 clause 28 over the copper media. Auto negotiation supports choosing the mode of operation automatically by comparing its own abilities and received abilities from link partner. The advertised abilities include:

- a) Speed: 10/100/1000Mbps
- b) Duplex mode: full duplex and/or half duplex

Auto negotiation is initialized when the following scenarios happen:

- c) Power-up/Hardware/Software reset
- d) Auto negotiation restart
- e) Transition from power-down to power up
- f) Link down

Auto negotiation is enabled for YT8614 by default, and can be disabled by software control.

4.7. LDS (Link discovery signaling)

YT8614 supports long range Ethernet (LRE), which uses link discovery signaling (LDS) instead of auto negotiation since the extended cable reach attenuates the auto negotiation link pulses. LDS is an extended reach signaling scheme and protocol, which is used to

- g) Master/Slave assignment
- h) Estimate cable length
- i) Confirm pair number and pair connectivity ordering
- j) Choose highest common operation mode

IEEE-compliant PHYs will ignore LDS signal since its frequency is less than 2MHz according to IEEE802.3 clause 14. If the link partner is an IEEE legacy ethernet PHY, YT8614 can detect the standard NLP, FLP, or MLT-3 IDLE signal, and then transits LDS mode into Clause 28 auto negotiation mode.

Forcing pair number and speed mode is also supported. The same forcing must be done at both ends of the link. By default the LDS is disabled, and should be enabled before using this feature.

4.8. Polarity detection and auto correction

YT8614 can detect and correct two types of cable errors: swapping of pairs within the UTP cable (swapping between pair 0 and pair 1, and(or) swapping between pair 2 and pair 3) and swapping of wires within a pair.

4.9. Energy Efficient Ethernet (EEE)

EEE is IEEE 802.3az, an extension of the IEEE 802.3 standard. EEE defines support for the PHY to operate in Low Power Idle (LPI) mode which, when enabled, supports QUIET times during low link utilization allowing both link partners to disable portions of each PHY's circuitry and save power.

YT8614 also helps legacy MAC without EEE ability to work as a complete EEE power saving system.

4.10. Synchronous Ethernet (Sync-E)

YT8614 provides Synchronous Ethernet (Sync-E) support, and two Sync-E clock can output from SYNCE0 (pin 11) or SYNCE1 (pin 12). The Sync-E clock sources can be configured to recovery from UTP0~4, QSGMII0, or Fiber0~3 respectively. When SYNCE0 or SYNCE1 lock, the SYNC_LOCK0 (pin 21) or SYNC_LOCK1 (pin 22) will pull high.

The recovery clock for Sync-E can be either a 125MHz or 25MHz clock.

When the PHY is in SLAVE mode, the CLKOUT will output the recovered clock from the MDI. If the device is in MASTER mode, the CLKOUT will output the clock based on the local free run PLL.

4.11. Link Down Power Saving (Sleep Mode)

YT8614 supports link down power saving, also called sleep mode. When UTP port link down and no signals over UTP cable for 40 seconds, YT8614 will enter sleep mode.

For most of time in sleep mode, YT8614 will disable almost all the circuits except crystal clock and comparators for channel 0/1 of 10BASE-Te. Access by MDC/MDIO interface is available.

At a time interval in sleep mode, YT8614 will wake to transmit signals over TRXP1/TRXN1. The time interval is a random value around 2.7s.

Once detect signals over UTP cable, YT8614 will exit sleep mode.

4.12. Interrupt

YT8614 provides an active low interrupt output pin (INT_N) based on change of the PHY status. Every interrupt condition is represented by the read-only general interrupt status register (section 6.2.18. Interrupt Status Register (UTP MII register 0x13)).

The interrupts can be individually enable or disable by setting or clearing bits in the interrupt enable register (section 6.2.17. Interrupt Mask Register (UTP MII register 0x12)).

Note 1: The interrupt of the YT8614 is a level-triggered mechanism.

Note 2: The interrupt output pin (INT_N) is open drain mode, and must pull-up to DVDDIO via a 4.7K resistor.

5. Operational Description

5.1. Reset

YT8614 have a hardware reset pin(RESET_N) which is low active. RESET_N should be active for at least 10ms to make sure all internal logic is reset to a known state. Hardware reset should be applied after power up. RESET_N is also used for power on strapping. During RESET_N is active, YT8614 latches input value on strapping. Strapping is used as configuration information which provides flexibility in application without mdio access.

YT8614 also provides three software reset control registers. Two of them are used to reset all UTP internal logic except some mdio configuration registers, by setting bit 15 of UTP mii register (address 0x0) or LDS mii register (address 0x0). And the third is used to reset all SerDes internal logic except CDR and some mdio configuration registers, by setting bit15 of SerDes mii register(address 0x0) to 1. These three bits are self-clear after reset process is done. For detailed information about what register will be reset by software reset, please refer to register table.

Table 10. Reset Timing Characteristics

Symbol	Description	Min	Typ	Max	Units
T1	The duration from all powers steady to reset signal release to high	10	-	-	ms
T2	The duration of reset signal remain low timing	10	-	-	ms

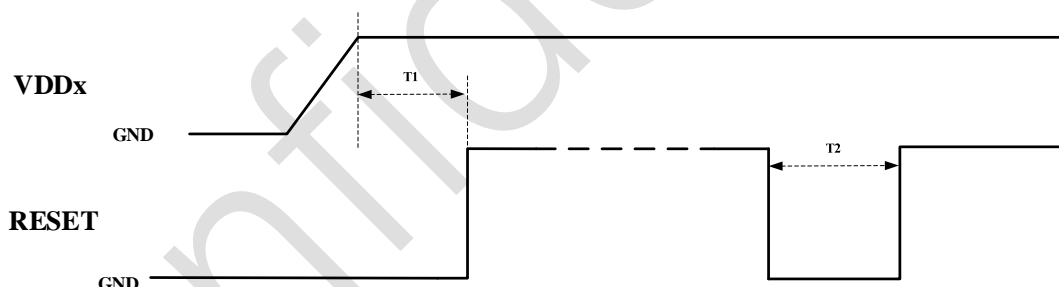


Figure 9. Reset Timing Diagram

5.2. PHY Address

For YT8614, Strapping PHYAD[4:0] is used to generate phy address port 0. The other port's phy address is the sum of the PHYAD[4:0] and port number. For example, if PHYAD[4:0] = 8, the phy address of port 3 is 11 (the sum of 8 and 3)

5.3. Loopback Mode

There are three loopback modes in YT8614.

5.3.1. Digital Loopback

Digital loopback provides the ability to loop transmitted data back to the receiver using digital circuitry in YT8614.

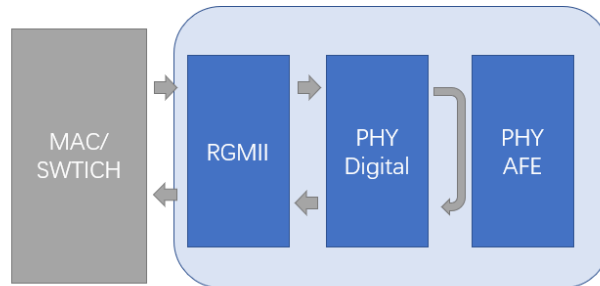


Figure 10. Digital Loopback

5.3.2. External loopback

External cable loopback loops Tx to Rx through a complete digital and analog path and an external cable, thus testing all the digital data paths and all the analog circuits. Figure shows a block diagram of external cable loopback.

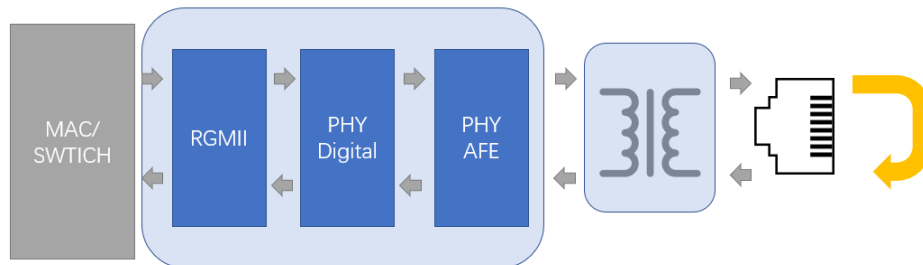
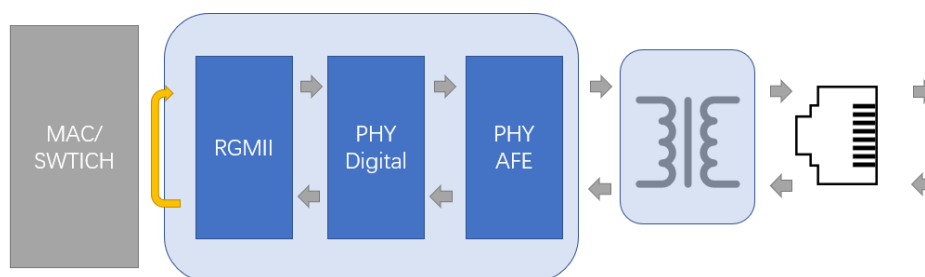


Figure 11. External Loopback

5.3.3. Remote PHY loopback

The Remote loopback connects the MDI receive path to the MDI transmit path, near the RGMII interface, thus the remote link partner can detect the connectivity in the resulting loop. Figure below, shows the path of the remote loopback.

**Figure 12. Remote PHY Loopback**

5.4. LED

The YT8614 supports serial LED mode. In the serial LED mode, the data is clocked through a shift register and the shifted symbols are output to the 36 LED pins.

Each MDI port has three indicator symbols and each fiber port has three indicator symbols. Each symbol may have different indicator.

You can find more information from *YT8614 application note*.

5.5. Power Supplies

YT8614 requires external power supply 3.3 V and 1.2V. Please refer to *section 8. Power Requirements* for more information.

6. Register Overview

6.1.1. SMI Mux (EXT 0xA000)

Table 11. SMI Mux (EXT 0xA000)

Bit	Symbol	Access	Default	Description
15:13	Reserved	RO	0x0	Reserved
12:8	MDIO_PHYAD	RO	0x0	the PHYAD field in current MDIO command
7:5	Reserved	RO	0x0	Reserved
4	en_brdst_phy	RW	0x0	When bit1 smi_sds_phy is 0, this bit controls to broadcast write to all PHYs. 0: disable. 1: enable broadcast write.
3	en_brdst_q	RW	0x0	When bit1 smi_sds_phy is 1, this bit controls to broadcast write to all QSGMII channels. 0: disable. 1: enable broadcast write;.
2	en_brdst_sf	RW	0x0	When bit1 smi_sds_phy is 1, this bit controls to broadcast write to all SGMIIs. 0: disable. 1: enable broadcast write.
1	Smi_sds_phy	RW	0x0	To control access whether phy register or sds register. 0: to access phy. 1: to access sds.
0	smi_sf	RW	0x0	When smi_sds_phy is 1, this bit controls to access whether sds 2/3/4/5 (SGMII) register or sds 0/1 (QSGMII) register. 0: to access QSGMII register. 1: to access SGMII register;

6.1.2. SLED cfg0 (EXT 0xA001)

Table . SLED cfg0 (0xA001)

Bit	Symbol	Access	Default	Description
15	led_manu_en	RW	0x0	to control serial LEDs status manually. 1: enable; 0: disable, SLED are controled by internal status then.
14:12	led_manu_st	RW	0x0	SLEDs' manu status, corresponding to each port's 3 SLEDs.
11	led_act_low	RW	0x1	control SLED's polarity. 1: active low; 0: active high.

10:8	led_bit_mask	RW	0x7	The thress mask bit for the three LED pins of each port: 1'b1: enable the pin output; 1'b0: disable pin output.
7:0	led_en_ctrl	RW	0xFF	Control to enable the eight ports' SLED: 1'b1: enable serial led output for this port; 1'b0: disable serial led output for this port.

6.1.3. PHY_ID (0xA002)

Table 12. PHY_ID (0xA002)

Bit	Symbol	Access	Default	Description
15:0	phy_id	RO	0x3210	None

6.1.4. Chip_Version (0xA003)

Table 13. Chip_Version (0xA003)

Bit	Symbol	Access	Default	Description
15:0	chip_version	RO	0x400	None

6.1.5. SLED cfg (0xA004)

Table 14. SLED cfg (0xA004)

Bit	Symbol	Access	Default	Description
15:10	Reserved	RO	0x0	Always 0.
9	led_lsb	RW	0x1	control the SLED order; 1: LED00 first and LED35 last; 0: LED35 first and LED00 last.
8	led_seri_dis	RW	0x0	1: to disable the SLED function; 0: normal mode. See ext.A007.4 for detail.
7	led_clk_en	RW	0x1	1: enable SLED clock to output to SLED_CK pin; 0: disable SLED clock output and drive 0 on SLED_CK pin.
6	led_data_en	RW	0x1	1: enable SLED data to output to SLED_DA pin; 0: disable SLED data output and drive 0 on SLED_DA pin.
5:4	led_mode	RW	0x3	Control each port's LED indicator symbol number and the information it indicates. 2'b00, each port has one LED indicator symbols, { 1st led }, to indicates: MDI: [link/act] FIBER: [link/act] 2'b01, each port has 2 LED indicator symbols, { 1st led, 2nd led }, to indicate: MDI: [speed1000/act] [speed100(10)/act] FIBER: [speed1000/act] [speed100/act]

				2'b10, each port has 3 LED indicator symbols, { 1st led, 2nd led, 3rd led }, to indicate: MDI: [speed1000/act] [speed100/act] [speed10/act] FIBER: [speed1000/act] [speed100/act] [Disable] 2'b11, each port has 3 LED indicator symbols, { 1st led, 2nd led, 3rd led }, to indicate: MDI: [link/act] [speed1000] [speed100] FIBER: [link/act] [speed1000] [speed100] Refer to ext.A060 led_idx_sel for more.
3:2	led_burst_cycle	RW	0x2	Serial led burst cycle. SLED status will be updated when the timer is done. 2'b00: 8ms 2'b01: 16ms 2'b10: 32ms 2'b11: 64ms
1:0	led_clk_cycle	RW	0x1	Serial led clock cycle: 2'b00: 80ns 2'b01: 160ns 2'b10: 240ns 2'b11: 320ns

6.1.6. mode_chg_reset (0xA005)

Table 15. mode_chg_reset (0xA005)

Bit	Symbol	Access	Default	Description
15	mode_chg_reset	RW SC	0x0	This bit will asserts when ext.a007.12 en_phy or ext.a007.3:0 changes. When this bit asserts, whole chip will be reset. This bit is self-cleared.
14	en_manu_porten	RW	0x0	1: enable to control *_port_en in EXT 0xA00F manually; 0: *_port_en in EXT 0xA00F is controlled by chip_mode.
13	en_manu_ck_sel	RW	0x0	1: enable to control SerDes ck_sel in EXT 0xA018 bit[15:14] manually; 0: SerDes ck_sel in EXT 0xA018 bit[15:14] is controlled by chip_mode.
12	iddq_mode_reg	RW	0x0	1: control to enter IDDQ mode.
11	int_polarity	RW	0x0	1: INT_N is active LOW; 0: INT_N is active HIGH.
10	Bypass_mdio_watchdog	RW	0x0	bypass mdio watch dog
9:8	Reserved	RO	0x0	Reserved
7	En_mdc_la	RW	0x1	enable mdc latch for read data

6	En_phyaddr0	RW	0x0	enable phyaddr0
5	En_bdcst_addr	RW	0x0	enable broadcast address
4:0	Bdcst_addr	RW	0x0	broadcast address

6.1.7. chip_mode (0xA007)

Table 16. chip_mode (0xA007)

Bit	Symbol	Access	Default	Description
15:13	package_id	RO	0x7	the package_id. 011b and 111b means 128pin; 010b and 110b means 144pin; else means 176pin.
12	en_phy	RW POS	0x1	1: enable all the coppers port and serdes ports; 0: disable all the copper ports and serdes ports.
11:6	reserved	RO	0x0	always 0.
5	en_pwron_light	RW POS	0x1	make SLEDs or direct LEDs light for 200ms after hardware reset or power on reset.
4	dis_sled	RW POS	0x1	1: to disable SLED PINs SCL/SDA; 0: to enable SLED PINs SCL/SDA. To disable SLED, ext.A004.8 shall be set to 1 first, then set this register to 1. SLEDs may behave abnormally if set this register to 1 before set ext.A004.8 to 1.
3:0	chip_mode	RW POS	0x4	<p>4'b0000 Reserved for feature usage 4'b0001 Reserved for feature usage 4'b0010, Qsgmii x1 and Sgmii x1 + Copper x5 mode; 4'b0011, Sgmii x2 + Copper x2 mode 4'b0100, Qsgmii x2 + Copper x8 mode; same as 8218 4'b0101, Qsgmii x2 + Copper x8 mode; 4'b0110, SGMII x1 + Combo x1 (Combo port consist of Port3 and the other 5G Serdes works in fiber mode); 4'b0111, Qsgmii x1 + Copper x3 and Combo x1 (Combo port consist of Port3 and the other 5G Serdes works in fiber mode);</p> <p>4'b1000, Fiber x4 + Copper x4 4'b1001, Reserved. 4'b1010, Qsgmii x1 + Copper x4 mode, 4'b1011 Qsgmii x1 + Fiber x4 mode; (4 fiber ports' speed are programed via extended register A009h bit3:0 respectively when 100FX auto sensing is closed); 4'b1100, Qsgmii x1 + Combo x4 mode; (4</p>

				<p>fiber ports' speed are programed via extended register A009h bit3:0 respectively when 100FX auto sensing is closed);</p> <p>4'b1101 Qsgmii x1 + Combo x4 mode;</p> <p>4'b1110, Qsgmii x1 + Sgmii(MAC) x4 mode;</p> <p>4'b1111, Sgmii(PHY) x4 + Copper x4 mode.</p> <p>For 128pin and 144pin, Chip_mode[3] is tied to 0;</p> <p>For 176pin, chip_mode[3] is 1 by default, and can be programed to 0.</p>
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6.1.8. SYNCE0 cfg (0xA006)

Table 17. SYNCE0 cfg (0xA006)

Bit	Symbol	Access	Default	Description
15	sync_clk_en_0	RW	0x0	1=enable to output the sync_clk0 to the PAD SYNC0.
14	bp_sync_lock_gating_0	RW	0x0	<p>When sync_clk0 is not locked, this bit controls whether to output the sync_clk0 or crystal clock to the PAD SYNC0 or not.</p> <p>1: to output;</p> <p>0: to not output.</p>
13	sel_synce_125m_0	RW	0x0	<p>bit13 and bit10 controls the sync_clk0's frequency and source: {sel_synce_125m_0, sel_clk_25m_xtl_0},</p> <p>2'b00: output 25MHz syncE clock;</p> <p>2'b01: output 31.25MHz syncE clock;</p> <p>2'b10: output 125MHz syncE clock;</p> <p>2'b11: output 25MHz reference clock.</p>
12:11	reserved	RO	0x0	always 0.
10	sel_clk_25m_xtl_0	RW	0x0	refer to bit13 sel_synce_125m_0 for detail.
9	reserved	RW	0x0	<p>bit9:0, select the source of the sync_clk0 from the recovered RX clocks. The recovered RX clocks include that from 4 port copper PHY, 4 port Fiber/SGMII 1.25G serdes PHY and one 5G serdes PHY.</p> <p>MSB has the higher priority, for example, bit9:0=0x030 means to output the phy 6's RX recovered clock.</p> <p>sds0, means the 5G serdes QSGMII0.</p> <p>phy7, means the fiber/SGMII port 3.</p> <p>phy6, means the fiber/SGMII port 2.</p> <p>phy5, means the fiber/SGMII port 1.</p>
8	sel_rclk_sds0_0	RW	0x0	
7	sel_rclk_phy7_0	RW	0x0	
6	sel_rclk_phy6_0	RW	0x0	
5	sel_rclk_phy5_0	RW	0x0	
4	sel_rclk_phy4_0	RW	0x0	
3	sel_rclk_phy3_0	RW	0x0	
2	sel_rclk_phy2_0	RW	0x0	
1	sel_rclk_phy1_0	RW	0x0	
0	sel_rclk_phy0_0	RW	0x0	

				phy4, means the fiber/SGMII port 0. phy3, means the copper port 3. phy2, means the copper port 2. phy1, means the copper port 1. phy0, means the copper port 0.
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6.1.9. SYNCE1 cfg (0xA00E)

Table 18. SYNCE1 cfg (0xA00E)

Bit	Symbol	Access	Default	Description
15	sync_clk_en_1	RW	0x0	1=enable to output the sync_clk1 to the PAD SYNC1.
14	bp_sync_lock_gating_1	RW	0x0	When sync_clk1 is not locked, this bit controls whether to output the sync_clk1 or crystal clock to the PAD SYNC1 or not. 1: to output; 0: to not output.
13	sel_synce_125m_1	RW	0x0	bit13 and bit10 controls the sync_clk1's frequency and source: {sel_synce_125m_1, sel_clk_25m_xtl_1}, 2'b00: output 25MHz syncE clock; 2'b01: output 31.25MHz syncE clock; 2'b10: output 125MHz syncE clock; 2'b11: output 25MHz reference clock.
12:11	reserved	RO	0x0	always 0.
10	sel_clk_25m_xtl_1	RW	0x0	refer to bit13 sel_synce_125m_1 for detail.
9	reserved	RW	0x0	bit9:0, select the source of the sync_clk0 from the recovered RX clocks. The recovered RX clocks include that from 4 port copper PHY, 4 port Fiber/SGMII 1.25G serdes PHY and one 5G serdes PHY. MSB has the higher priority, for example, bit9:0=0x030 means to output the phy 6's RX recovered clock. sds0, means the 5G serdes QSGMII0. phy7, means the fiber/SGMII port 3. phy6, means the fiber/SGMII port 2. phy5, means the fiber/SGMII port 1. phy4, means the fiber/SGMII port 0. phy3, means the copper port 3. phy2, means the copper port 2. phy1, means the copper port 1. phy0, means the copper port 0.
8	sel_rclk_sds0_1	RW	0x0	
7	sel_rclk_phy7_1	RW	0x0	
6	sel_rclk_phy6_1	RW	0x0	
5	sel_rclk_phy5_1	RW	0x0	
4	sel_rclk_phy4_1	RW	0x0	
3	sel_rclk_phy3_1	RW	0x0	
2	sel_rclk_phy2_1	RW	0x0	
1	sel_rclk_phy1_1	RW	0x0	
0	sel_rclk_phy0_1	RW	0x0	

6.1.10. pkg_cfg0 (0xA0a0)

Port Index : 0 - 7

Port Offset : 0x100

Table 19. pkg_cfg0 (0xA0a0)

Bit	Symbol	Access	Default	Description
15	u0_pkg_chk_en	RW	0x0	1: to enable RX/TX package checker. For RX checker, if ext.A0B7.15=0, RX checker checks the downstream media's GMII RX data or in UTP2Fiber mode, the UTP's GMII RX data, else it checks upstream media's GMII RX data or in UTP2Fiber mode, the Fiber's GMII RX data; For TX checker, if ext.A0B7.10=1, TX checker checks the pkg_gen's TX data; else if ext.A0B7.14=0, TX checker checks the downstream media's GMII TX data or in UTP2Fiber mode, the UTP's GMII TX data, else, it checks upstream media's GMII TX data or in UTP2Fiber mode, the Fiber's GMII TX data;
14	u0_pkg_en_gate	RW	0x1	1: to enable gate all the clocks to package self-test module when bit15 pkg_chk_en is 0, bit13 bp_pkg_gen is 1 and bit12 pkg_gen_en is 0;
13	u0_bp_pkg_gen	RW	0x1	1: normal function; 0: test function, the TX data is sourced from pkg_gen;
12	u0_pkg_gen_en	RW SC	0x0	1: to enable pkg_gen generating MII packages. But, the data will only be sent to transceiver when Bit13 bp_pkg_gen is 1'b0.
11:8	u0_pkg_prm_lth	RW	0x8	The preamble length of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.
7:4	u0_pkg_ipg_lth	RW	0xc	The IPG of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.
3	u0_Xmit_mac_force_gen	RW	0x0	1: To enable pkg_gen to send out the generated data even when the link is not established.
2	u0_pkg_corrupt_crc	RW	0x0	1: to make pkg_gen to send out CRC error packages.
1:0	u0_pkg_payload	RW	0x0	Control the payload of the generated packages.

6.1.11. pkg_cfg1 (0xA0a1)

Port Index : 0 - 7

Port Offset : 0x100

Table 20. pkg_cfg1 (0xA0a1)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_length	RW	0x40	To set the length of the generated packages.

6.1.12. pkg_cfg2 (0xA0a2)

Port Index : 0 – 7

Port Offset : 0x100

Table 21. pkg_cfg2 (0xA0a2)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_burst_size	RW	0x0	To set the number of packages in a burst of package generation.

6.1.13. pkg_rx_valid0 (0xA0a3)

Port Index : 0 – 7

Port Offset : 0x100

Table 22. pkg_rx_valid0 (0xA0a3)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_valid_high	RO RC	0x0	Pkg_ib_valid[31:16], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte.

6.1.14. pkg_rx_valid1 (0xA0a4)

Port Index : 0 – 7

Port Offset : 0x100

Table 23. pkg_rx_valid1 (0xA0a4)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_valid_low	RO RC	0x0	Pkg_ib_valid[15:0], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte.

6.1.15. pkg_rx_os0 (0xA0a5)

Port Index : 0 – 7

Port Offset : 0x100

Table 24. pkg_rx_os0 (0xA0a5)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_os_good_high	RO RC	0x0	Pkg_ib_os_good[31:0], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

6.1.16. pkg_rx_os1 (0xA0a6)

Port Index : 0 – 7

Port Offset : 0x100

Table 25. pkg_rx_os1 (0xA0a6)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_os_good_low	RO RC	0x0	Pkg_ib_os_good[15:0], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

6.1.17. pkg_rx_us0 (0xA0a7)

Port Index : 0 – 7

Port Offset : 0x100

Table 26. pkg_rx_us0 (0xA0a7)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_us_good_high	RO RC	0x0	Pkg_ib_us_good[31:0], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are <64Byte.

6.1.18. pkg_rx_us1 (0xA0a8)

Port Index : 0 – 7

Port Offset : 0x100

Table 27. pkg_rx_us1 (0xA0a8)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_us_good_low	RO RC	0x0	Pkg_ib_us_good[15:0], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

6.1.19. pkg_rx_err (0xA0a9)

Port Index : 0 – 7

Port Offset : 0x100

Table 28. pkg_rx_err (0xA0a9)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_err	RO RC	0x0	pkg_ib_err is the number of RX packages from wire whose CRC are wrong and length are >=64Byte, <=1518Byte.

6.1.20. pkg_rx_os_bad (0xA0aa)

Port Index : 0 – 7

Port Offset : 0x100

Table 29. pkg_rx_os_bad (0xA0aa)

Bit	Symbol	Access	Default	Description
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15:0	u0_pkg_ib_os_bad	RO RC	0x0	pkg_ib_os_bad is the number of RX packages from wire whose CRC are wrong and length are >=1518Byte.
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6.1.21. pkg_rx_fragment (0xA0ab)

Port Index : 0 – 7

Port Offset : 0x100

Table 30. pkg_rx_fragment (0xA0ab)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_frag	RO RC	0x0	pkg_ib_frag is the number of RX packages from wire whose length are <64Byte.

6.1.22. pkg_rx_nosfd (0xA0ac)

Port Index : 0 – 7

Port Offset : 0x100

Table 31. pkg_rx_nosfd (0xA0ac)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ib_nosfd	RO RC	0x0	pkg_ib_nosfd is the number of RX packages from wire whose SFD is missed.

6.1.23. pkg_tx_valid0 (0xA0ad)

Port Index : 0 – 7

Port Offset : 0x100

Table 32. pkg_tx_valid0 (0xA0ad)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_valid_high	RO RC	0x0	Pkg_ob_valid[31:16], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length are >=64Byte and <=1518Byte.

6.1.24. pkg_tx_valid1 (0xA0ae)

Port Index : 0 – 7

Port Offset : 0x100

Table 33. pkg_tx_valid1 (0xA0ae)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_valid_low	RO RC	0x0	Pkg_ob_valid[15:0], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length are >=64Byte and <=1518Byte.

6.1.25. pkg_tx_os0 (0xA0af)

Port Index : 0 – 7

Port Offset : 0x100

Table 34. pkg_tx_os0 (0xA0af)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_os_good_high	RO RC	0x0	Pkg_ob_os_good[31:0], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

6.1.26. pkg_tx_os1 (0xA0b0)

Port Index : 0 – 7

Port Offset : 0x100

Table 35. pkg_tx_os1 (0xA0b0)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_os_good_low	RO RC	0x0	Pkg_ob_os_good[15:0], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

6.1.27. pkg_tx_us0 (0xA0b1)

Port Index : 0 – 7

Port Offset : 0x100

Table 36. pkg_tx_us0 (0xA0b1)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_us_good_high	RO RC	0x0	Pkg_ob_us_good[31:0], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length are <64Byte.

6.1.28. pkg_tx_us1 (0xA0b2)

Port Index : 0 – 7

Port Offset : 0x100

Table 37. pkg_tx_us1 (0xA0b2)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_us_good_low	RO RC	0x0	Pkg_ob_us_good[15:0], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

6.1.29. pkg_tx_err (0xA0b3)

Port Index : 0 – 7

Port Offset : 0x100

Table 38. pkg_tx_err (0xA0b3)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_err	RO RC	0x0	pkg_ob_err is the number of TX packages from MII whose CRC are wrong and length are >=64Byte, <=1518Byte.

6.1.30. pkg_tx_os_bad (0xA0b4)

Port Index : 0 – 7

Port Offset : 0x100

Table 39. pkg_tx_os_bad (0xA0b4)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_os_bad	RO RC	0x0	pkg_ob_os_bad is the number of TX packages from MII whose CRC are wrong and length are >=1518Byte.

6.1.31. pkg_tx_fragment (0xA0b5)

Port Index : 0 – 7

Port Offset : 0x100

Table 40. pkg_tx_fragment (0xA0b5)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_frag	RO RC	0x0	pkg_ob_frag is the number of TX packages from MII whose length are <64Byte.

6.1.32. pkg_tx_nosfd (0xA0b6)

Port Index : 0 – 7

Port Offset : 0x100

Table 41. pkg_tx_nosfd (0xA0b6)

Bit	Symbol	Access	Default	Description
15:0	u0_pkg_ob_nosfd	RO RC	0x0	pkg_ob_nosfd is the number of TX packages from MII whose SFD is missed.

6.1.33. pkg_cfg3 (0xA0b7)

Port Index : 0 – 7

Port Offset : 0x100

Table 42. pkg_cfg3 (0xA0b7)

Bit	Symbol	Access	Default	Description
15	u0_pkgchk_rxsrc_sel	RW	0x0	control RX checker's data source. =0, RX checker checks the downstream media's GMII RX data or in UTP2Fiber mode, the UTP's GMII RX data, =1, it checks upstream media's GMII RX data or in UTP2Fiber mode, the Fiber's GMII RX data
14	u0_pkgchk_txsrc_sel	RW	0x0	When ext.A0b7.10 is 0, it controls TX checker's data source. =0, TX checker checks the downstream media's GMII TX data or in UTP2Fiber mode, the UTP's GMII TX data; =1, it checks upstream media's GMII TX data or

				in UTP2Fiber mode, the Fiber's GMII TX data. It is not valid when ext.A0b7.10 is 1.
13	u0_pkgen_txdir_sel	RW	0x0	0=to downstream or to UTP in utp2fib; 1=to upstream or to fiber in utp2fib
12	u0_en_pkgen_da_sa	RW	0x0	1: set the DA/SA of the packet generated by pkg_gen to a programmed value; For DA, if EXT 0xA0B7 bit[11] is 1, the DA is set to broadcast address FF-FF-FF-FF-FF-FF; else, the DA is set to fix value, the highest 5 Bytes are 00-00-00-00-00, and the lowest 1 Byte is programmed by EXT 0xA0B9 bit[15:8]. For SA, the highest 5 Bytes are 00-00-00-00-00, and the lowest 1 Byte is programmed by EXT 0xA0B9 bit[7:0]. 0: the DA/SA is not programmed value
11	u0_pkg_brdest	RW	0x0	Valid when EXT 0xA0B7 bit12 is 1. 1: set the DA to broadcast address FF-FF-FF-FF-FF-FF 0: set the DA to a fixed programmed value.
10	u0_pkgchk_txsrc_pkgen	RW	0x0	1'b1: the package checker on TX side will check the tx data generated by pkg_gen; 1'b0: the package checker on TX side will check the tx data of UTP GMII/MII.
9	u0_pkg_en_az	RW	0x0	1: enable to generate and send out LPI pattern during IPG;
8:0	u0_pkg_in_az_t	RW	0x1ff	control the time dewll in LPI;

6.1.34. pkg_az_cfg (0xA0b8)

Port Index : 0 – 7

Port Offset : 0x100

Table 43. pkg_az_cfg (0xA0b8)

Bit	Symbol	Access	Default	Description
15:8	u0_pkgen_pre_az_t	RW	0x20	control the time after last package done and before sending LPI pattern;
7:0	u0_pkgen_aft_az_t	RW	0x19	control the time after sending LPI pattern and before the next burst package;

6.1.35. pkg_da_sa_cfg (0xA0b9)

Port Index : 0 – 7

Port Offset : 0x100

Table 44. pkg_da_sa_cfg (0xA0b9)

Bit	Symbol	Access	Default	Description
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15:8	u0_pkgen_da	RW	0x0	Lowest 8 bits of DA, others is zero. Refer to EXT 0xA0B7 bit[12] for detail.
7:0	u0_pkgen_sa	RW	0x0	Lowest 8 bits of SA, others is zero. Refer to EXT 0xA0B7 bit[12] for detail.

6.1.36. manu_hw_reset (0xA0c0)

Table 45. manu_hw_reset (0xA0c0)

Bit	Symbol	Access	Default	Description
15	manu_hw_reset	RW	0x0	1: to reset whole chip including all register space except itself.
14:0	reserved	RO	0x0	Reserved.

6.2. UTP MII Register

The YT8614 transceiver is designed to be fully compliant with the MII clause of the IEEE 802.3u Ethernet specification.

The MII management interface registers are written and read serially, using the MDIO and MDC pins.

A clock of up to 12.5 MHz must drive the MDC pin of the YT8614. Data transferred to and from the MDIO pin is synchronized with the MDC clock. The following sections describe what each MII read or write instruction contains.

6.2.1. Basic control register (0x00)

Table 46. Basic control register (0x00)

Bit	Symbol	Access	Default	Description
15	Reset	RW SC	0x0	PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically. 0: Normal operation 1: PHY reset
14	Loopback	RW SWC	0x0	Internal loopback control 1'b0: disable loopback 1'b1: enable loopback
13	Speed_Selection(LSB)	RW	0x0	LSB of speed_selection[1:0]. Link speed can be selected via either the Auto-Negotiation process, or manual speed selection speed_selection[1:0]. Speed_selection[1:0] is valid when Auto-Negotiation is disabled by clearing bit 0.12 to zero. Bit6 bit13 1 1 = Reserved 1 0 = 1000Mb/s

				0 1 = 100Mb/s 0 0 = 10Mb/s
12	Autoneg_En	RW	0x1	1: to enable auto-negotiation; 0: auto-negotiation is disabled.
11	Power_down	RW SWC	0x0	1 = Power down 0 = Normal operation When the port is switched from power down to normal operation, software reset and Auto-Negotiation are performed even bit[15] RESET and bit[9] RESTART_AUTO_NEGOTIATION are not set by the user.
10	Isolate	RW SWC	0x0	Isolate phy from RGMII/SGMII/FIBER. 1'b0: Normal mode 1'b1: Isolate mode
9	Re_Autoneg	RW SC SWS	0x0	Auto-Negotiation automatically restarts after hardware or software reset regardless of bit[9] RESTART. 1 = Restart Auto-Negotiation Process 0 = Normal operation
8	Duplex_Mode	RW	0x1	The duplex mode can be selected via either the Auto-Negotiation process or manual duplex selection. Manual duplex selection is allowed when Auto-Negotiation is disabled by setting bit[12] AUTO_NEGOTIATION to 0. 1 = Full Duplex 0 = Half Duplex
7	Collision_Test	RW SWC	0x0	Setting this bit to 1 makes the COL signal asserted whenever the TX_EN signal is asserted. 1 = Enable COL signal test 0 = Disable COL signal test
6	Speed_Selection(MSB)	RW	0x1	See bit13.
5:0	Reserved	RO	0x0	Reserved. Write as 0, ignore on read

6.2.2. Basic status register (0x01)

Table 47. Basic status register (0x01)

Bit	Symbol	Access	Default	Description
15	100Base-T4	RO	0x0	PHY doesn't support 100BASE-T4
14	100Base-X_Fd	RO	0x1	PHY supports 100BASE-X_FD
13	100Base-X_Hd	RO	0x1	PHY supports 100BASE-X_HD
12	10Mbps_Fd	RO	0x1	PHY supports 10Mbps_Fd
11	10Mbps_Hd	RO	0x1	PHY supports 10Mbps_Hd

10	100Base-T2_Fd	RO	0x0	PHY doesn't support 100Base-T2_Fd
9	100Base-T2_Hd	RO	0x0	PHY doesn't support 100Base-T2_Hd
8	Extended_Status	RO	0x1	Whether support EXTended status register in 0Fh 0: Not supported 1: Supported
7	Unidirect_Ability	RO	0x0	1'b0: PHY able to transmit from MII only when the PHY has determined that a valid link has been established 1'b1: PHY able to transmit from MII regardless of whether the PHY has determined that a valid link has been established
6	Mf_Preamble_Suppression	RO	0x1	1'b0: PHY will not accept management frames with preamble suppressed 1'b1: PHY will accept management frames with preamble suppressed
5	Autoneg_Complete	RO SWC	0x0	1'b0: Auto-negotiation process not completed 1'b1: Auto-negotiation process completed
4	Remote_Fault	RO RC SWC LH	0x0	1'b0: no remote fault condition detected 1'b1: remote fault condition detected
3	Autoneg_Ability	RO	0x1	1'b0: PHY not able to perform Auto-negotiation 1'b1: PHY able to perform Auto-negotiation
2	Link_Status	RO SWC LL	0x0	Link status 1'b0: Link is down 1'b1: Link is up
1	Jabber_Detect	RO RC SWC LH	0x0	10Baset jabber detected. It would assert if TX activity lasts longer than 42ms. 1'b0: no jabber condition detected 1'b1: Jabber condition detected.
0	Extended_Capability	RO	0x1	To indicate whether support EXTended registers, to access from address register 1Eh and data register 1Fh 1'b0: Not supported 1'b1: Supported

6.2.3. PHY identification register1 (0x02)

Table 48. PHY identification register1 (0x02)

Bit	Symbol	Access	Default	Description
15:0	Phy_Id	RO	0x4F51	Bits 3 to 18 of the Organizationally Unique Identifier

6.2.4. PHY identification register2 (0x03)

Table 49. PHY identification register2 (0x03)

Bit	Symbol	Access	Default	Description
15:10	Phy_Id	RO	0x3A	Bits 19 to 24 of the Organizationally Unique Identifier
9:4	Type_No	RO	0x9	For YT8614.
3:0	Revision_No	RO	0x9	4 bits manufacturer's revision number.

6.2.5. Auto-Negotiation advertisement (0x04)

Table 50. Auto-Negotiation advertisement (0x04)

Bit	Symbol	Access	Default	Description
15	NEXT_Page	RW	0x0	<p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down <p>If 1000BASE-T is advertised, the required next pages are automatically transmitted. This bit must be set to 0 if no additional next page is needed.</p> <p>1 = Advertise 0 = Not advertised</p>
14	Ack	RO	0x0	Always 0.
13	Remote_Fault	RW	0x0	<p>1 = Set Remote Fault bit 0 = Do not set Remote Fault bit</p>
12	Extended_NEXT_Page	RW	0x1	<p>Extended nEXT page enable control bit</p> <p>1 = Local device supports transmission of extended next pages 0 = Local device does not support transmission of extended next pages.</p>
11	Asymmetric_Pause	RW	0x1	<p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> • Software reset is asserted by writing register 0x0 bit[15]

				<ul style="list-style-type: none"> • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Asymmetric Pause 0 = No asymmetric Pause
10	Pause	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: <ul style="list-style-type: none"> • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = MAC PAUSE implemented 0 = MAC PAUSE not implemented
9	100BASE-T4	RO	0x0	1 = Able to perform 100BASE-T4 0 = Not able to perform 100BASE-T4 Always 0
8	100BASE-TX_Full_Duplex	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: <ul style="list-style-type: none"> • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised
7	100BASE-TX_Half_Duplex	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: <ul style="list-style-type: none"> • Software reset is asserted by writing register

				0x0 bit[15] <ul style="list-style-type: none"> • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised
6	10BASE-Te_Full_Duplex	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: <ul style="list-style-type: none"> • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised
5	10BASE-Te_Half_Duplex	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: <ul style="list-style-type: none"> • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised
4:0	Selector_Field	RW	0x1	Selector Field mode. 00001 = IEEE 802.3

6.2.6. Auto-Negotiation link partner ability (0x05)

Table 51. Auto-Negotiation link partner ability (0x05)

Bit	Symbol	Access	Default	Description
15	1000Base-X_Fd	RO SWC	0x0	Received Code Word Bit 15 1 = Link partner is capable of next page 0 = Link partner is not capable of next page
14	ACK	RO SWC	0x0	Acknowledge. Received Code Word Bit 14 1 = Link partner has received link code word

				0 = Link partner has not received link code word
13	REMOTE_FAULT	RO SWC	0x0	Remote Fault. Received Code Word Bit 13 1 = Link partner has detected remote fault 0 = Link partner has not detected remote fault
12	RESERVED	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 12
11	ASYMMETRIC_PAUSE	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 11 1 = Link partner requests asymmetric pause 0 = Link partner does not request asymmetric pause
10	PAUSE	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 10 1 = Link partner supports pause operation 0 = Link partner does not support pause operation
9	100BASE-T4	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 9 1 = Link partner supports 100BASE-T4 0 = Link partner does not support 100BASE-T4
8	100BASE-TX_FULL_DUPLEX	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 8 1 = Link partner supports 100BASE-TX full-duplex 0 = Link partner does not support 100BASE-TX full-duplex
7	100BASE-TX_HALF_DUPLEX	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 7 1 = Link partner supports 100BASE-TX half-duplex 0 = Link partner does not support 100BASE-TX half-duplex
6	10BASE-Te_FULL_DUPLEX	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 6 1 = Link partner supports 10BASE-Te full-duplex 0 = Link partner does not support 10BASE-Te full-duplex
5	10BASE-Te_HALF_DUPLEX	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 5 1 = Link partner supports 10BASE-Te half-duplex

				0 = Link partner does not support 10BASE-T half-duplex
4:0	SELECTOR_FIELD	RO SWC	0x0	Selector Field Received Code Word Bit 4:0

6.2.7. Auto-Negotiation expansion register (0x06)

Table 52. Auto-Negotiation expansion register (0x06)

Bit	Symbol	Access	Default	Description
15:5	Reserved	RO	0x0	Reserved
4	Parallel Detection fault	RO RC SWC LH	0x0	1 = Fault is detected 0 = No fault is detected
3	Link partner nEXT page able	RO SWC LH	0x0	1 = Link partner supports NEXT page 0 = Link partner does not support next page
2	Local NEXT Page able	RO	0x1	1 = Local Device supports NEXT Page 0 = Local Device does not Next Page
1	Page received	RO RC LH	0x0	1 = A new page is received 0 = No new page is received
0	Link Partner Auto negotiation able	RO	0x0	1 = Link partner supports auto-negotiation 0 = Link partner does not support auto-negotiation

6.2.8. Auto-Negotiation NEXT Page register (0x07)

Table 53. Auto-Negotiation NEXT Page register (0x07)

Bit	Symbol	Access	Default	Description
15	NEXT Page	RW	0x0	Transmit Code Word Bit 15 1 = The page is not the last page 0 = The page is the last page
14	Reserved	RO	0x0	Transmit Code Word Bit 14
13	Message page mode	RW	0x1	Transmit Code Word Bit 13 1 = Message Page 0 = Unformatted Page
12	Ack2	RW	0x0	Transmit Code Word Bit 12 1 = Comply with message 0 = Cannot comply with message
11	Toggle	RO	0x0	Transmit Code Word Bit 11 1 = This bit in the previously exchanged Code Word is logic 0 0 = The Toggle bit in the previously exchanged Code Word is logic 1
10:0	Message/Unformatte	RW	0x1	Transmit Code Word Bits [10:0]. These bits are encoded as Message Code Field when bit[13] is set to 1, or as Unformatted Code Field when bit[13] is set to 0.

6.2.9. Auto-Negotiation link partner Received NEXT Page register (0x08)

Table 54. Auto-Negotiation link partner Received NEXT Page register (0x08)

Bit	Symbol	Access	Default	Description
15	NEXT Page	RO	0x0	Received Code Word Bit 15 1 = This page is not the last page 0 = This page is the last page
14	Reserved	RO	0x0	Received Code Word Bit 14
13	Message page mode	RO	0x0	Received Code Word Bit 13 1 = Message Page 0 = Unformatted Page
12	Ack2	RO	0x0	Received Code Word Bit 12 1 = Comply with message 0 = Cannot comply with message
11	Toggle	RO	0x0	Received Code Word Bit 11 1 = This bit in the previously exchanged Code Word is logic 0 0 = The Toggle bit in the previously exchanged Code Word is logic 1
10:0	Message/Unformatte	RO	0x0	Received Code Word Bit 10:0 These bits are encoded as Message Code Field when bit[13] is set to 1, or as Unformatted Code Field when bit[13] is set to 0.

6.2.10. MASTER-SLAVE control register (0x09)

Table 55. MASTER-SLAVE control register (0x09)

Bit	Symbol	Access	Default	Description
15:13	Test mode	RW	0x0	The TX_TCLK signals from the RX_CLK pin is for jitter testing in test modes 2 and 3. When exiting the test mode, hardware reset or software reset through writing register 0x0 bit[15] must be performed to ensure normal operation. 000 = Normal Mode 001 = Test Mode 1 - Transmit Waveform Test 010 = Test Mode 2 - Transmit Jitter Test (MASTER mode) 011 = Test Mode 3 - Transmit Jitter Test (SLAVE mode) 100 = Test Mode 4 - Transmit Distortion Test 110, 111 = Reserved normal operation.
12	Master/Slave Manual configuration Enable	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not

				take effect until any of the following occurs: <ul style="list-style-type: none"> • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Manual MASTER/SLAVE configuration 0 = Automatic MASTER/SLAVE configuration.
11	Master/Slave configuration	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: <ul style="list-style-type: none"> • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down This bit is ignored if bit[12] is 0. 1 = Manual configuration as MASTER 0 = Manual configuration as SLAVE.
10	Port Type	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: <ul style="list-style-type: none"> • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down This bit is ignored if bit[12] is 1. 1 = Prefer multi-port device (MASTER) 0 = Prefer single port device (SLAVE)
9	1000BASE-T Full	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: <ul style="list-style-type: none"> • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9]

				<ul style="list-style-type: none"> The port is switched from power down to normal operation by writing register 0x0 bit[11] Link goes down 1 = Advertise 0 = Not advertised
8	1000BASE-T Half-	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: <ul style="list-style-type: none"> Software reset is asserted by writing register 0x0 bit[15] Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] The port is switched from power down to normal operation by writing register 0x0 bit[11] Link goes down 1 = Advertise 0 = Not advertised (default)
7:0	Reserved	RW	0x0	Write as 0, ignore on read.

6.2.11. MASTER-SLAVE status register (0x0A)

Table 56. MASTER-SLAVE status register (0x0A)

Bit	Symbol	Access	Default	Description
15	Master/Slave_cfg_error	RO RC SWC LH	0x0	This register bit will clear on read, rising of MII 0.12 and rising of AN complete. 1 = Master/Slave configuration fault detected 0 = No fault detected
14	Master/Slave	RO	0x0	This bit is not valid unless register 0x1 bit5 is 1. 1 = Local PHY configuration resolved to Master 0 = Local PHY configuration resolved to Slave
13	Local Receiver Status	RO	0x0	1 = Local Receiver OK 0 = Local Receiver not OK
12	Remote Receiver	RO	0x0	1 = Remote Receiver OK 0 = Remote Receiver not OK
11	Link Partner	RO	0x0	This bit is not valid unless register 0x1 bit5 is 1. 1 = Link Partner supports 1000BASE-T half duplex 0 = Link Partner does not support 1000BASE-T half duplex
10	Link Partner	RO	0x0	This bit is not valid unless register 0x1 bit5 is 1. 1 = Link Partner supports 1000Base-T full duplex 0 = Link Partner does not support 1000Base-T full duplex

9:8	Reserved	RO	0x0	Reserved
7:0	Idle Error Count	RO RC	0x0	MSB of Idle Error Counter. The register indicates the idle error count since the last read operation performed to this register. The counter pegs at 11111111 and does not roll over.

6.2.12. MMD access control register (0x0D)

Table 57. MMD access control register (0x0D)

Bit	Symbol	Access	Default	Description
15:14	Function	RW	0x0	00 = Address 01 = Data, no post increment 10 = Data, post increment on reads and writes 11 = Data, post increment on writes only
13:5	Reserved	RO	0x0	Reserved
4:0	DEVAD	RW	0x0	MMD register device address. 00001 = MMD1 00011 = MMD3 00111 = MMD7

6.2.13. MMD access data register (0x0E)

Table 58. MMD access data register (0x0E)

Bit	Symbol	Access	Default	Description
15:0	Address data	RW	0x0	If register 0xD bits [15:14] are 00, this register is used as MMD DEVAD address register. Otherwise, this register is used as MMD DEVAD data register as indicated by its address register.

6.2.14. Extended status register (0x0F)

Table 59. Extended status register (0x0F)

Bit	Symbol	Access	Default	Description
15	1000BASE-X Full Duplex	RO	0x0	1 = PHY supports 1000BASE-X Full Duplex 0 = PHY does not supports 1000BASE-X Full Duplex Always 0.
14	1000BASE-X Half Duplex	RO	0x0	1 = PHY supports 1000BASE-X Half Duplex. 0 = PHY does not support 1000BASE-X Half Duplex. Always 0
13	1000BASE-T Full Duplex	RO	0x1	1 = PHY supports 1000BASE-T Full Duplex 0 = PHY does not supports 1000BASE-T Full

				Duplex Always 1
12	1000BASE-T Half Duplex	RO	0x0	1 = PHY supports 1000BASE-T Half Duplex 0 = PHY does not support 1000BASE-T Half Duplex Always 0.
11:0	Reserved	RO	0x0	Always 0

6.2.15. PHY specific function control register (0x10)

Table 60. PHY specific function control register (0x10)

Bit	Symbol	Access	Default	Description
15:7	Reserved	RO	0x0	Reserved
6:5	Cross_md	RW	0x3	Changes made to these bits disrupt normal operation, thus a software reset is mandatory after the change. And the configuration does not take effect until software reset. 00 = Manual MDI configuration 01 = Manual MDIX configuration 10 = Reserved 11 = Enable automatic crossover for all modes
4	Int_polar_sel	RW	0x0	Reserved
3	Crs_on_tx	RW	0x0	This bit is effective in 10BASE-Te half-duplex mode and 100BASE-TX mode: 1 = Assert CRS on transmitting or receiving 0 = Never assert CRS on transmitting, only assert it on receiving.
2	En_sqe_test	RW	0x0	1 = SQE test enabled, 0 = SQE test disabled Note: SQE Test is automatically disabled in full-duplex mode regardless the setting in this bit.
1	En_pol_inv	RW	0x1	If polarity reversal is disabled, the polarity is forced to be normal in 10BASE-Te. 1 = Polarity Reversal Enabled 0 = Polarity Reversal Disabled
0	Dis_jab	RW	0x0	Jabber takes effect only in 10BASE-Te half-duplex mode. 1 = Disable jabber function 0 = Enable jabber function

6.2.16. PHY specific status register (0x11)

Table 61. PHY specific status register (0x11)

Bit	Symbol	Access	Default	Description
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15:14	Speed_mode	RO	0x0	<p>These status bits are valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.</p> <p>11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps</p>
13	Duplex	RO	0x0	<p>This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.</p> <p>1 = Full-duplex 0 = Half-duplex</p>
12	Page Received real-time	RO	0x0	<p>1 = Page received 0 = Page not received</p>
11	Speed and Duplex Resolved	RO	0x0	<p>When Auto-Negotiation is disabled, this bit is set to 1 for force speed mode.</p> <p>1 = Resolved 0 = Not resolved</p>
10	Link status real-time	RO	0x0	<p>1 = Link up 0 = Link down</p>
9:7	Reserved	RO	0x0	Reserved
6	MDI Crossover Status	RO	0x0	<p>This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. The bit value depends on register 0x10 “PHY specific function control register” bits6~bit5 configurations. Register 0x10 configurations take effect after software reset.</p> <p>1 = MDIX 0 = MDI</p>
5	Wirespeed downgrade	RO	0x0	<p>1 = Downgrade 0 = No Downgrade</p>
4	Reserved	RO	0x0	Reserved
3	Transmit Pause	RO	0x0	<p>This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed.</p> <p>This bit indicates MAC pause resolution. This bit is for information purposes only and is not used by the device. When in force mode, this bit is set to be 0.</p> <p>1 = Transmit pause enabled 0 = Transmit pause disabled</p>

2	Receive Pause	RO	0x0	This status bit is valid only when bit[11] is 1. Bit[11] is set when Auto-Negotiation is completed. This bit indicates MAC pause resolution. This bit is for information purposes only and is not used by the device. When in force mode, this bit is set to be 0. 1 = Receive pause enabled 0 = Receive pause disabled
1	Polarity Real Time	RO	0x0	1 = Reverted polarity 0 = Normal polarity
0	Jabber Real Time	RO	0x0	1 = Jabber 0 = No jabber

6.2.17. Interrupt Mask Register (0x12)

Table 62. Interrupt Mask Register (0x12)

Bit	Symbol	Access	Default	Description
15	Auto-Negotiation Error INT mask	RW	0x0	1 = Interrupt enable 0 = Interrupt disable
14	Speed Changed INT mask	RW	0x0	same as bit 15
13	Duplex changed INT mask	RW	0x0	same as bit 15
12	Page Received INT mask	RW	0x0	same as bit 15
11	Link Failed INT mask	RW	0x0	same as bit 15
10	Link Succeed INT mask	RW	0x0	same as bit 15
9:6	reserved	RW	0x0	No used.
5	Wirespeed downgraded INT mask	RW	0x0	same as bit 15
4:2	Reserved	RW	0x0	No used.
1	Polarity changed INT mask	RW	0x0	same as bit 15
0	Jabber Happened INT mask	RW	0x0	same as bit 15

6.2.18. Interrupt Status Register (0x13)

Table 63. Interrupt Status Register (0x13)

Bit	Symbol	Access	Default	Description
15	Auto-Negotiation Error INT	RO	0x0	Error can take place when any of the following happens: <ul style="list-style-type: none"> • MASTER/SLAVE does not resolve correctly • Parallel detect fault • No common HCD • Link does not come up after negotiation is complete • Selector Field is not equal • flp_receive_idle=true while Autoneg

				Arbitration FSM is in NEXT PAGE WAIT state 1 = Auto-Negotiation Error takes place 0 = No Auto-Negotiation Error takes place
14	Speed Changed INT	RO	0x0	1 = Speed changed 0 = Speed not changed
13	Duplex changed INT	RO	0x0	1 = duplex changed 0 = duplex not changed
12	Page Received INT	RO	0x0	1 = Page received 0 = Page not received
11	Link Failed INT	RO	0x0	1 = Phy link down takes place 0 = No link down takes place
10	Link Succeed INT	RO	0x0	1 = Phy link up takes place 0 = No link up takes place
9:6	Reserved	RO	0x0	reserved
5	Wirespeed downgraded INT	RO	0x0	1 = speed downgraded. 0 = Speed didn't downgrade.
4:2	Reserved	RO	0x0	reserved
1	Polarity changed INT	RO	0x0	1 = PHY reverred MDI polarity 0 = PHY didn't revert MDI polarity
0	Jabber Happened INT	RO	0x0	1 = 10BaseT TX jabber happened 0 = 10BaseT TX jabber didn't happen Please refer to mii.1.1 Jabber_Detect.

6.2.19. Speed Auto Downgrade Control Register (0x14)

Table 64. Speed Auto Downgrade Control Register (0x14)

Bit	Symbol	Access	Default	Description
15:12	Reserved	RO	0x0	Reserved
11	En_mdio_latch	RW	0x1	1 = To latch MII/MMD register's read out value during MDIO read 0 = Do not latch MII/MMD register's read out value during MDIO read
10	Start_autoneg	RW SC	0x0	Set it to cause PHY to restart auto-negotiation.
9	Reverse_autoneg	RW	0x0	1 = reverse the autoneg direction, 10Mb/s has 1st priority, then 100Mb/s and at last 1000Mb/s. 0 = normal autoneg direction
8	Dis_giga	RW	0x0	1 = disable advertise Giga ability in autoneg; 0 = don't disable, so PHY advertises Giga ability based on MII register 0x9.
7:6	Reserved	RO	0x0	Reserved
5	En_speed_downgrade	RW POS	0x1	When this bit is set to 1, the PHY enables smart-speed function. Writing this bit requires a software reset to update. This bit will be set to

				1'b0 in UTP_TO_FIBER_FORCE and UTP_TO_FIBER_AUTO mode; else set to 1'b1, only take effect after software reset
4:2	Autoneg retry limit pre-downgrade	RW	0x3	If these bits are set to 3, the PHY attempts five times (set value 3 + additional 2) before downgrading. The number of attempts can be changed by these bits. only take effect after software reset
1	Bp_autosspd_timer	RW	0x0	1 = the wirespeed downgrade FSM will bypass the timer used for link stability check; only take effect after software reset 0 = not bypass the timer, then links that established but hold for less than 2.5s would still be taken as failure, autoneg retry counter will increase by 1.
0	Reserved	RO	0x0	Reserved

6.2.20. Rx Error Counter Register (0x15)

Table 65. Rx Error Counter Register (0x15)

Bit	Symbol	Access	Default	Description
15:0	Rx_err_counter	RO	0x0	This counter increase by 1 at the 1st rising of RX_ER when RX_DV is 1. The counter will hold at maximum 16'hFFFF and not roll over.

6.2.21. Debug Register's Address Offset Register (0x1E)

Table 66. Debug Register's Address Offset Register (0x1E)

Bit	Symbol	Access	Default	Description
15:8	Reserved	RO	0x0	Reserved
7:0	Debug Register Address Offset	RW	0x0	It's the address offset of the debug register that will be Write or Read

6.2.22. Debug Register's Data Register (0x1F)

Table 67. Debug Register's Data Register (0x1F)

Bit	Symbol	Access	Default	Description
15:0	Debug Register Datas	RW	0x0	It's the data to be written to the debug register indicated by the address offset in register 0x1E, or the data read out from that debug register.

6.3. LDS MII Register

6.3.1. LRE control (0x00)

Table 68. LRE control (0x00)

Bit	Symbol	Access	Default	Description
15	Reset	RW SC	0x0	PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically.; 1'b0: Normal operation; 1'b1: PHY reset
14	Loopback	RW	0x0	Loopback control; 1'b0: disable loopback; 1'b1: enable loopback
13	Restart_LDS	RW SC	0x0	1'b1: restart LDS process
12	LDS_Enable	RW	0x0	1'b1: LDS enabled; 1'b0: LDS disabled
11	Power_down	RW	0x0	1 = Power down; 0 = Normal operation; When the port is switched from power down to; normal operation, software reset and Auto-; Negotiation are performed even bit[15] RESET and bit[9] RESTART_AUTO_NEGOTIATION are not set by the user.
10	Isolate	RW	0x0	Isolate phy from MII/GMII/RGMII: PHY will not respond to RGMII TXD/TX_CTL, and present high impedance on RXD/RX_CTL.; 1'b0: Normal mode; 1'b1: Isolate mode
9:6	Speed_selection	RW	0x0	4'b0000: 10Mbps; 4'b1000: 100Mbps; Others: reserved
5:4	Pair_selection	RW	0x0	2'b00: 1 pair connection; 2'b01: 2 pair connections; 2'b10: 4 pair connections; 2'b11: reserved
3	M/S_selection	RW	0x0	1'b1: manually force local device to master, when reg0.12 = 0; 1'b0: manually force local device to slave, when reg0.12 = 0
2	Force auto negotiation	RW	0x0	1'b1: manually force local device to auto negotiation state, when reg0.12 = 0
1:0	Reserved	RO	0x0	Reserved. Write as 0, ignore on read

6.3.2. LRE status (0x01)

Table 69. LRE status (0x01)

Bit	Symbol	Access	Default	Description
15:14	Reserved	RO	0x0	Ignore on read

13	100Mbps_1-pair capable	RO	0x0	1'b1: 100Mbps 1-pair capable; 1'b0: Not 100Mbps 1-pair capable
12	100Mbps_4-pair capable	RO	0x1	1'b1: 100Mbps 4-pair capable; 1'b0: Not 100Mbps 4-pair capable
11	100Mbps_2-pair capable	RO	0x0	1'b1: 100Mbps 2-pair capable; 1'b0: Not 100Mbps 2-pair capable
10	10Mbps_2-pair capable	RO	0x0	1'b1: 10Mbps 2-pair capable; 1'b0: Not 10Mbps 2-pair capable
9	10Mbps_1-pair capable	RO	0x0	1'b1: 10Mbps 1-pair capable; 1'b0: Not 10Mbps 1-pair capable
8	Extended_Status	RO	0x1	Whether support EXTended status register in 0Fh; 0: Not supported; 1: Supported
7	Reserved	RO	0x1	None
6	Mf_Preamble_Suppression	RO	0x1	1'b0: PHY will not accept management frames with preamble suppressed; 1'b1: PHY will accept management frames with preamble suppressed
5	LDS_Complete	RO	0x0	1'b1: LDS auto-negotiation complete; 1'b0: LDS auto-negotiation not complete
4	Support_IEEE_802.3_PHY	RO	0x1	1'b1: Support IEEE 802.3 PHY operation; 1'b0: Not Support IEEE 802.3 PHY operation
3	LDS_Ability	RO	0x1	1'b1: LDS auto-negotiation capable; 1'b0: Not LDS auto-negotiation capable
2	Link_Status	RO	0x0	Link status; 1'b0: Link is down; 1'b1: Link is up
1	Jabber_Detect	RO LH	0x0	10Baset jabber detected; 1'b0: no jabber condition detected; 1'b1: Jabber condition detected
0	Extended_Capability	RO LH	0x1	To indicate whether support EXTended registers, to access from address register 1Eh and data register 1Fh; 1'b0: Not supported; 1'b1: Supported

6.3.3. PHY ID (0x02)

Table 70. PHY ID (0x02)

Bit	Symbol	Access	Default	Description
15:0	PHY_ID	RO	0x4f51	None

6.3.4. PHY ID (0x03)

Table 71. PHY ID (0x03)

Bit	Symbol	Access	Default	Description
15:0	PHY_ID	RO	0xe889	None

6.3.5. LDS auto-negotiation advertised ability (0x04)

Table 72. LDS auto-negotiation advertised ability (0x04)

Bit	Symbol	Access	Default	Description
15	Asymmetric_pause	RW	0x0	1'b1: Advertise asymmetric pause; 1'b0: Advertise no asymmetric pause
14	Pause_capable	RW	0x0	1'b1: Advertise pause capable; 1'b0: Advertise no pause capable
13:6	Reserved	RO	0x0	reserved
5	100Mbps_1-pair capable	RW	0x0	1'b1: 100Mbps 1-pair capable; 1'b0: Not 100Mbps 1-pair capable
4	100Mbps_4-pair capable	RW	0x1	1'b1: 100Mbps 4-pair capable; 1'b0: Not 100Mbps 4-pair capable
3	100Mbps_2-pair capable	RW	0x0	1'b1: 100Mbps 2-pair capable; 1'b0: Not 100Mbps 2-pair capable
2	10Mbps_2-pair capable	RW	0x0	1'b1: 10Mbps 2-pair capable; 1'b0: Not 10Mbps 2-pair capable
1	10Mbps_1-pair capable	RW	0x0	1'b1: 10Mbps 1-pair capable; 1'b0: Not 10Mbps 1-pair capable
0	Auto negotiation capable	RW	0x1	1'b1: Auto negotiation capable; 1'b0: Auto negotiation capable

6.3.6. LDS auto-negotiation advertised control (0x05)

Table 73. LDS auto-negotiation advertised control (0x05)

Bit	Symbol	Access	Default	Description
15:13	Test_Mode	RW	0x0	Test Mode control
12:10	Reserved	RO	0x0	Reserved
9	Port_type_preference	RW	0x0	1'b1: multiport device (Mater); 1'b0: single-port device (Salve)
8	Ability_field_update	RW SC	0x0	1'b1: Contents of register 06h are updated; 1'b0: No updates
7:0	Local_field_number	RW	0x0	Local field number of NEXT Page message

6.3.7. LDS ability nEXT page transmit (0x06)

Table 74. LDS ability nEXT page transmit (0x06)

Bit	Symbol	Access	Default	Description
15:0	NEXT_page_message	RW	0x0	LDS nEXT page message

6.3.8. LDS link partner ability (0x07)

Table 75. LDS link partner ability (0x07)

Bit	Symbol	Access	Default	Description
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15	Asymmetric_pause	RO	0x0	1'b1: link partner supports asymmetric pause; 1'b0: link partner doesn't support asymmetric pause
14	Pause_capable	RO	0x0	1'b1: link partner supports pause capable; 1'b0: link partner doesn't support pause capable
13:6	Reserved	RO	0x0	None
5	100Mbps_1-pair_capable	RO	0x0	1'b1: link partner 100Mbps 1-pair capable; 1'b0: link partner not 100Mbps 1-pair capable
4	100Mbps_4-pair_capable	RO	0x0	1'b1: link partner 100Mbps 4-pair capable; 1'b0: link partner not 100Mbps 4-pair capable
3	100Mbps_2-pair_capable	RO	0x0	1'b1: link partner 100Mbps 2-pair capable; 1'b0: link partner not 100Mbps 2-pair capable
2	10Mbps_2-pair_capable	RO	0x0	1'b1: link partner 10Mbps 2-pair capable; 1'b0: link partner not 10Mbps 2-pair capable
1	10Mbps_1-pair_capable	RO	0x0	1'b1: link partner 10Mbps 1-pair capable; 1'b0: link partner not 10Mbps 1-pair capable
0	Reserved	RO	0x0	None

6.3.9. LDS link partner nEXT page message (0x08)

Table 76. LDS link partner nEXT page message (0x08)

Bit	Symbol	Access	Default	Description
15:0	Link_partner_nEXT_page_message	RO	0x0	LDS link partner nEXT page message

6.3.10. LDS link partner nEXT page message control (0x09)

Table 77. LDS link partner nEXT page message control (0x09)

Bit	Symbol	Access	Default	Description
15	NEXT_page_read_flag	RW SC	0x0	1'b1: nEXT page has been read
14:9	Reserved	RO	0x0	None
8	Remote_acknowledge	RO RC	0x0	1'b1: acknowledge from link partner;
7:0	Remote_field_number	RO	0xff	Remote field number of nEXT page message

6.3.11. LDS expansion (0x0A)

Table 78. LDS expansion (0x0A)

Bit	Symbol	Access	Default	Description
15	Downgrade_ability	RO	0x0	1'b1: LDS speed downgrade
14	Master/Slave	RO	0x0	1 = Local PHY configuration resolved to Master; 0 = Local PHY configuration resolved to Slave
13:12	Connections_pairs	RO	0x0	Number of pairs; 2'b00: 1 pair; 2'b01: 2 pairs; 2'b10: 4 pairs; 2'b11: reserved
11:0	Estimated_cable_length	RO	0x0	None

6.3.12. LDS Results (0x0B)

Table 79. LDS Results (0x0B)

Bit	Symbol	Access	Default	Description
15:6	Reserved	RO	0x0	None
5	4-pair_100M	RO	0x0	1'b1: local PHY configuration resolved to 4-pair 100M
4	Auto_negotiation	RO	0x0	1'b1: local PHY configuration resolved to AN
3	1-pair_100M	RO	0x0	1'b1: local PHY configuration resolved to 1-pair 100M
2	1-pair_10M	RO	0x0	1'b1: local PHY configuration resolved to 1-pair 10M
1	2-pair_100M	RO	0x0	1'b1: local PHY configuration resolved to IEEE 100M
0	2-pair_10M	RO	0x0	1'b1: local PHY configuration resolved to IEEE 10M

6.3.13. LDS Extended status (0x0F)

Table 80. LDS Extended status (0x0F)

Bit	Symbol	Access	Default	Description
15:10	Reserved	RO	0x0	Reserved
9	Local_receiver status	RO	0x0	1'b1: local receiver ok; 1'b0: local receiver not ok
8	Remote_receiver status	RO	0x0	1'b1: remote receiver ok; 1'b0: remote receiver not ok
7:0	Idle_error_count	RO	0x0	Number of idle errors since last read

6.4. UTP MMD Register

6.4.1. PCS control 1 register (MMD3, 0x00)

Table 81. PCS control 1 register (MMD3, 0x00)

Bit	Symbol	Access	Default	Description
15	Pcs_rst	RW SC	0x0	Setting this bit will set all PCS registers to their default states. This action also initiate a reset in MMD1 and MMD7.
14:11	Reserved	RO	0x0	Reserved
10	Clock_stoppable	RW SWC	0x0	Not used.
9:0	Reserved	RO	0x0	Reserved

6.4.2. PCS status 1 register (MMD3, 0x01)

Table 82. PCS status 1 register (MMD3, 0x01)

Bit	Symbol	Access	Default	Description
15:12	Reserved	RO	0x0	Reserved
11	Tx_lpi_rxd	RO LH	0x0	When read as 1, it indicates that the transmit PCS has received low power idle signaling one or more times since the register was last read. Lach High.
10	Rx_lpi_rxd	RO LH	0x0	When read as 1, it indicates that the receive PCS has received low power idle signaling one or more times since the register was last read. Lach High.
9	Tx_lpi_indic	RO	0x0	When read as 1, it indicates that the transmit PCS is currently receiving low power idle signals.
8	Rx_lpi_indic	RO	0x0	When read as 1, it indicates that the receive PCS is currently receiving low power idle signals.
7:3	Reserved	RO	0x0	Reserved
2	Pcsrx_lnk_status	RO LL	0x0	PCS status, latch low.
1:0	Reserved	RO	0x0	Reserved

6.4.3. EEE control and capability register (MMD3, 0x14)

Table 83. EEE control and capability register (MMD3, 0x14)

Bit	Symbol	Access	Default	Description
15:3	Reserved	RO	0x0	Reserved
2	1000BASE-T EEE	RO	0x1	Always 1. EEE is supported for 1000BASE-T
1	100BASE-TX EEE	RO	0x1	Always 1. EEE is supported for 100BASE-TX
0	Reserved	RO	0x0	Reserved

6.4.4. EEE wake error counter (MMD3, 0x16)

Table 84. EEE wake error counter (MMD3, 0x16)

Bit	Symbol	Access	Default	Description
15:0	Lpi_wake_err_cnt	RO RC SWC	0x0	Count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type.

6.4.5. Local Device EEE Ability (MMD7, 0x3C)

Table 85. Local Device EEE Ability (MMD7, 0x3C)

Bit	Symbol	Access	Default	Description
15:3	Reserved	RO	0x0	Reserved
2	EEE_1000BT	RW POS	0x0	PHY's 1000BT EEE ability.

1	EEE_100BT	RW POS	0x0	PHY's 100BT EEE ability.
0	Reserved	RO	0x0	Reserved

6.4.6. Link Partner EEE Ability (MMD7, 0x3D)

Table 86. Link Partner EEE Ability (MMD7, 0x3D)

Bit	Symbol	Access	Default	Description
15:3	Reserved	RO	0x0	Reserved
2	LP_ge_eee_ability	RO	0x0	Link partner's 1000BT EEE ability.
1	LP_ge_eee_ability	RO	0x0	Link partner's 100BT EEE ability.
0	Reserved	RO	0x0	Reserved

6.4.7. Autoneg Result of EEE (MMD7, 0x8000)

Table 87. Autoneg Result of EEE (MMD7, 0x8000)

Bit	Symbol	Access	Default	Description
15:3	Reserved	RO	0x0	Reserved
2	En_ge_eee	RO	0x0	The autoneg result of whether 1000BT EEE is supported by both sides.
1	En_fe_eee	RO	0x0	The autoneg result of whether 100BT EEE is supported by both sides.
0	Phy_lpbk	RW	0x0	Not used.

6.5. UTP EXT Register

6.5.1. 10BT Debug, LPBKs Register (0x0A)

Table 88. 10BT Debug, LPBKs Register (0x0A)

Bit	Symbol	Access	Default	Description
15:12	Reserved	RO	0x0	Reserved
11	En_mskbt10_inan	RW	0x1	1 = enable the function of dividing Manchester code from MLT-3 code.
10	En_10bt_idl	RW	0x0	1 = In 10BT mode , if there's no data or NLP to transmit, shut off DAC; otherwise turn on the DAC; For FPGA due to mdio control, this bit is set to 1'b0
9	Bt10_squlch_ctrl	RW	0x1	1 = while receiving pulse_p/n toggle, bt10 carrier sense will be set even though link is no up;
8:6	phy_reg	RW	0x0	Reserved
5	rem_phy_lpbk	RW	0x0	control to set UTP to remote phy loopback mode or not.

4	Ext_lpbk	RW	0x0	External loopback.
3	Lpbk_ctrl_10bt	RW SWC	0x1	Control the loopback depth in 10BT when MII register 0x0 bit14 loopback is set.
2:0	Test_mode_10bt	RW SWC	0x0	Test_mode[2:0] is for 10BT test mode select:

6.5.2. Sleep Control1 (0x27)

Table 89. Sleep Control1 (0x27)

Bit	Symbol	Access	Default	Description
15	En_sleep_sw	RW	0x1	1 = enable sleep mode: PHY will enter sleep mode and close AFE after unplug cable for a timer;
14	Pllon_in_slp	RO	0x0	1 = keep PLL on in sleep mode;
13	Slp_pulse_sw	RW	0x1	when PHY enter sleep,
12	En_upd_afe_sbs	RW	0x0	When AFE control is changed, no matter it's triggered by sleep control logic or normal work mode change,
11:6	Reserved	RO	0x0	Reserved
5	Sleeping	RO	0x0	1 = PHY is slept;
4	Gate_25m	RO	0x0	Not used.
3:0	Slp_state	RO	0x0	FSM state of internal sleep control logic.

6.5.3. debug mon1 (0x5A)

Table 90. debug mon1 (0x5A)

Bit	Symbol	Access	Default	Description
15	Hold_snap_shot	RO	0x0	Valid when EXT 58h bit14 en_snap_shot is set.
14:0	Mse0	RO	0x0	Valid when EXT 58h bit14 en_snap_shot is set, or EXT 59h bit15 prob_auto is set. Corresponding to these two setting, it is the:

6.5.4. debug mon2 (0x5B)

Table 91. debug mon2 (0x5B)

Bit	Symbol	Access	Default	Description
15	Hold_snap_shot_az	RO	0x0	Valid when EXT 58h bit15 en_snap_shot_az is set.
14:0	Mse1	RO	0x0	Valid when EXT 58h bit14 en_snap_shot is set, or EXT 59h bit15 prob_auto is set. Corresponding to these two setting, it is the:

6.5.5. debug mon3 (0x5C)

Table 92. debug mon3 (0x5C)

Bit	Symbol	Access	Default	Description
15	Reserved	RO	0x0	Reserved
14:0	Mse2	RO	0x0	Valid when EXT 58h bit14 en_snap_shot is set, or EXT 59h bit15 prob_auto is set. Corresponding to these two setting, it is the:

6.5.6. debug mon4 (0x5D)

Table 93. debug mon4 (0x5D)

Bit	Symbol	Access	Default	Description
15	Reserved	RO	0x0	Reserved
14:0	Mse3	RO	0x0	Valid when EXT 58h bit14 en_snap_shot is set, or EXT 59h bit15 prob_auto is set. Corresponding to these two setting, it is the:

6.6. SDS(1.25G/5G) MII Register

6.6.1. Basic control register (0x00)

Table 94. Basic control register (0x00)

Bit	Symbol	Access	Default	Description
15	Reset	RW SC	0x0	PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically.
14	Loopback	RW	0x0	Internal loopback control
13	Speed_Selection(LSB)	RW	0x0	LSB of speed_selection[1:0]. Link speed can be selected via either the Auto-Negotiation process, or manual speed selection speed_selection[1:0]. Speed_selection[1:0] is valid when Auto-Negotiation is disabled by clearing bit 0.12 to zero.
12	Autoneg_En	RW	0x1	1: to enable auto-negotiation;
11	Power_down	RW	0x0	1 = Power down
10	Isolate	RW	0x0	Isolate phy from RGMII/SGMII/FIBER.
9	Re_Autoneg	RW SC	0x0	Auto-Negotiation automatically restarts after hardware or software reset regardless of bit[9] RESTART.
8	Duplex_Mode	RW	0x1	The duplex mode can be selected via either the Auto-Negotiation process or manual duplex

				selection. Manual duplex selection is allowed when Auto-Negotiation is disabled by setting bit[12] AUTO_NEGOTIATION to 0.
7	Collision_Test	RW	0x0	Setting this bit to 1 makes the COL signal asserted whenever the TX_EN signal is asserted.
6	Speed_Selection(MSB)	RW	0x1	See bit13.
5	en_unidirection	RW	0x0	When bit 0.12 is one or bit 0.8 is zero, this bit is ignored. When bit 0.12 is zero and bit 0.8 is one: 1 = Enable transmit from media independent interface regardless of whether the PHY has determined that a valid link has been established 0 = Enable transmit from media independent interface only when the PHY
4:0	Reserved	RO	0x0	Reserved. Write as 0, ignore on read

6.6.2. Basic status register (0x01)

Table 95. Basic status register (0x01)

Bit	Symbol	Access	Default	Description
15	100Base-T4	RO	0x0	PHY doesn't support 100BASE-T4
14	100Base-X_Fd	RO	0x1	PHY supports 100BASE-X_FD
13	100Base-X_Hd	RO	0x0	PHY supports 100BASE-X_HD
12	10Mbps_Fd	RO	0x0	PHY supports 10Mbps_Fd
11	10Mbps_Hd	RO	0x0	PHY supports 10Mbps_Hd
10	100Base-T2_Fd	RO	0x0	PHY doesn't support 100Base-T2_Fd
9	100Base-T2_Hd	RO	0x0	PHY doesn't support 100Base-T2_Hd
8	Extended_Status	RO	0x1	Whether support EXTended status register in 0Fh
7	Unidirect_Ability	RO	0x1	1'b0: PHY able to transmit from MII only when the PHY has determined that a valid link has been established
6	Mf_Preamble_Suppression	RO	0x1	1'b0: PHY will not accept management frames with preamble suppressed
5	Autoneg_Complete	RO	0x0	1'b0: Auto-negotiation process not completed
4	Remote_Fault	RO RC SWC LH	0x0	1'b0: no remote fault condition detected
3	Autoneg_Ability	RO	0x1	1'b0: PHY not able to perform Auto-negotiation

2	Link_Status	RO SWC LL	0x0	Link status
1	Jabber_Detect	RO	0x0	always 0
0	Extended_Capability	RO	0x1	To indicate whether support EXTended registers, to access from address register 1Eh and data register 1Fh

6.6.3. Sds identification register1 (0x02)

Table 96. Sds identification register1 (0x02)

Bit	Symbol	Access	Default	Description
15:0	Phy_Id	RO	0x4f51	Bits 3 to 18 of the Organizationally Unique Identifier

6.6.4. Sds identification register2 (0x03)

Table 97. Sds identification register2 (0x03)

Bit	Symbol	Access	Default	Description
15:10	Phy_Id	RO	0x3a	Bits 19 to 24 of the Organizationally Unique Identifier
9:4	Type_No	RO	0x8	6 bits manufacturer's type number
3:0	Revision_No	RO	0x9	4 bits manufacturer's revision number

6.6.5. Auto-Negotiation advertisement (0x04)

Table 98. Auto-Negotiation advertisement (0x04)

Bit	Symbol	Access	Default	Description
15	NEXT_Page	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:
14	Ack	RO	0x0	Always 0
13:12	Remote_Fault	RO	0x0	Always 0
11:9	Reserved	RO	0x0	Reserved
8	Asymmetric_Pause	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:
7	Pause	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:
6	Half_duplex	RW	0x0	Half duplex ability
5	Full_duplex	RW	0x1	Full duplex ability
4:0	Reserved	RO	0x0	Reserved

6.6.6. Auto-Negotiation link partner ability (0x05)

Table 99. Auto-Negotiation link partner ability (0x05)

Bit	Symbol	Access	Default	Description
15	NEXT Page	RO SWC	0x0	NEXT page. Received Code Word Bit 15
14	ACK	RO SWC	0x0	Acknowledge. Received Code Word Bit 14
13:12	REMOTE_FAULT	RO SWC	0x0	Remote Fault. Received Code Word Bit 13:12
11:9	RESERVED	RO	0x0	Reserved. Received Code Word Bit 11:9
8:7	PAUSE	RO SWC	0x0	Pause. Received Code Word Bit 8:7
6	HALF_DUPLEX	RO SWC	0x0	Half duplex. Received Code Word Bit 6
5	FULL_DUPLEX	RO SWC	0x0	Full duplex. Received Code Word Bit 5
4:0	RESERVED	RO	0x0	Reserved. Received Code Word Bit 4:0

6.6.7. Auto-Negotiation expansion register (0x06)

Table 100. Auto-Negotiation expansion register (0x06)

Bit	Symbol	Access	Default	Description
15:3	Reserved	RO	0x0	Reserved
2	Local NEXT Page able	RO	0x0	1 = Local Device supports NEXT Page
1	Page received	RO RC LH	0x0	1 = A new page is received
0	Reserved	RO	0x0	Reserved

6.6.8. Auto-Negotiation NEXT Page register (0x07)

Table 101. Auto-Negotiation NEXT Page register (0x07)

Bit	Symbol	Access	Default	Description
15:0	NEXT Page	RO	0x0	always be 0

6.6.9. Auto-Negotiation link partner Received NEXT Page register (0x08)

Table 102. Auto-Negotiation link partner Received NEXT Page register (0x08)

Bit	Symbol	Access	Default	Description
15:0	Link Partner NEXT Page	RO	0x0	always be 0

6.6.10. Extended status register (0x0F)

Table 103. Extended status register (0x0F)

Bit	Symbol	Access	Default	Description
15	1000BASE-X Full Duplex	RO	0x1	1 = PHY supports 1000BASE-X Full Duplex
14	1000BASE-X Half Duplex	RO	0x0	1 = PHY supports 1000BASE-X Half Duplex.
13	1000BASE-T Full Duplex	RO	0x0	1 = PHY supports 1000BASE-T Full Duplex
12	1000BASE-T Half Duplex	RO	0x0	1 = PHY supports 1000BASE-T Half Duplex
11:0	Reserved	RO	0x0	Always 0

6.6.11. Sds specific status register (0x11)**Table 104. Sds specific status register (0x11)**

Bit	Symbol	Access	Default	Description
15:14	Speed_mode	RO	0x0	These status bits are valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.
13	Duplex	RO	0x0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.
12:11	Pause	RO	0x0	Pause to mac
10	Link status real-time	RO	0x0	1 = Link up
9	Rx_lpi_active	RO	0x0	rx lpi is active
8	Duplex_error	RO	0x0	realtime duplex error
7	En_flowctrl_rx	RO	0x0	realtime en_flowctrl_rx
6	En_flowctrl_tx	RO	0x0	realtime en_flowctrl_tx
5:4	Ser_mode_cfg	RO	0x0	realtime serdes working mode. 00: SG_MAC; 01: SG_PHY; 10: FIB_1000; 11: FIB_100.
3:1	Xmit	RO	0x0	realtime transmit statemachine. 001: Xmit Idle; 010: Xmit Config; 100: Xmit Data.
0	Syncstatus	RO	0x0	realtime syncstatus

6.6.12. 100fx cfg (0x14)**Table 105. 100fx cfg (0x14)**

Bit	Symbol	Access	Default	Description
15	Force_sg_status	RW	0x0	Force sds linkup
14	Duplex_to_mac_100fx	RW	0x1	duplex setting to mac in 100fx mode
13:12	Pause_to_mac_100fx	RO	0x3	Pause setting to mac in 100fx mode
11:0	Reserved	RO	0x0	Reserved

6.6.13. receive err counter mon (0x15)**Table 106. receive err counter mon (0x15)**

Bit	Symbol	Access	Default	Description
15:0	error_counter_rx	RO	0x0	receive error counter

6.6.14. lint fail counter mon (0x16)**Table 107. lint fail counter mon (0x16)**

Bit	Symbol	Access	Default	Description
15:8	Reserved	RO	0x0	Reserved
7:0	Link_fail_cnt	RO	0x0	link fail counter

6.7. SDS(5G) EXT Register

6.7.1. sds analog digital interface cfg (0x02)

Table 108. sds analog digital interface cfg (0x02)

Bit	Symbol	Access	Default	Description
15	Sw_reset	RW	0x0	SerDes software reset, high active; ext.0.13 control it to be self clear or not, by default it's not self clear.
14	Tx_clk_sel	RW	0x0	select tx clock phase from analog, 1: inverted; 0: non-inverted.
13	Rx_clk_sel	RW	0x1	select rx clock phase from analog, 1: inverted; 0: non-inverted.
12	Rx_clk_cdr_sel	RW	0x1	select CDR's rx clock phase from analog, 1: inverted; 0: non-inverted.
11	Rot_clk_sel	RW	0x0	select rx clock phase used to latch rotator setting, 1: inverted; 0: non-inverted.
10	Loopback	RW	0x0	sds internal loopback, for QSGMII, all 4 channels' TX are loopbacked to RX.
9	Reserved	RO	0x0	always 0.
8	pcs_sw_reset	RW	0x0	SerDes PCS software reset, high active; ; ext.0.12 control it to be self clear or not, by default it's not self clear.
7	Tx_data_mlsb_sel	RW	0x0	1: swap msb and lsb for tx data to analog
6	Rx_data_mlsb_sel	RW	0x1	1: swap msb and lsb of rx data from analog. For FPGA, this is 1'b0 due to PMD difference between FPGA and chip
5	Tx_data_pol_sel	RW	0x0	1: 1 map to 0 and 0 map to 1 for tx data to analog
4	Rx_data_pol_sel	RW	0x0	1: 1 map to 0 and 0 map to 1 for rx data from analog
3	Cdr_data_mlsb_sel	RW	0x0	1: swap msb and lsb of rx data for cdr from analog
2	ana_cdrin_clk_sel	RW	0x0	0: Q0 digital cdr code received by positive edge; 1: Q0 digital cdr code received by negative edge;
1	ana_cfg_inv	RW	0x0	0: Q0 analog CDR runs with negative edge; 1: Q0 analog CDR runs with positive edge;
0	Reserved	RO	0x0	Reserved

6.7.2. sds prbs cfg1 (0x05)

Table 109. sds prbs cfg1 (0x05)

Bit	Symbol	Access	Default	Description
15	En_prbs	RW	0x0	enable TX PRBS or self-defined pattern, the pattern type is determined by bit7:5 test_mode.
14	En_bert	RW	0x0	enable Bit Error Rate Test;
13	Prbs_invert	RW	0x0	TX error injection function, it has highest polarity than prbs_err_once and prbs_err_cont. 1: to send polarity inverted PRBS or self-defined pattern;
12	Prbs_err_cont	RW	0x0	TX error injection function, it has the lowest polarity.1: to inject error on TX pattern continuously and periodic, the period is controlled by prbs_err_rate.
11:10	Prbs_err_rate	RW	0x0	It's valid only when prbs_err_cont is 1. 2'b00: inject one error every 1024 cycles; 2'b01: inject one error every 2048 cycles; 2'b10: inject one error every 4096 cycles; 2'b11: inject one error every 8192 cycles;
9	Prbs_err_once	RW	0x0	TX error injection function.At the rising of this bit, to send polarity inverted PRBS or self-defined pattern for one cycle;
8	Test_mode_prbs31	RW	0x0	1: PRBS31, bit7:5 test_mode[2:0] has no effect.0: not PRBS31, bit7:5 test_mode[2:0] take effect then.
7:5	Test_mode	RW	0x0	Control the TX pattern in test mode: 3'h0, PRBS7; 3'h1, PRBS10; 3'h2, Fix pattern, the fix pattern is controlled by Ext.6;3'h3, 010101...; 3'h4, 00110011...; 3'h5, 00000_11111_00000_11111...; 3'h6, 0000_0000_00_1111_1111_11...; 3'h7, Increase pattern, 0->1023->0->1023...
4	Duration_check_en	RW	0x0	enable fixed number of bits check defined in sds EXT BA/BB
3:0	Reserved	RO	0x0	Reserved

6.7.3. sds prbs cfg2 (0x06)

Table 110. sds prbs cfg2 (0x06)

Bit	Symbol	Access	Default	Description
15:0	Fix_pattern_15_0	RW	0x0	fix pattern transmited in test_mode 2

6.7.4. sds prbs cfg2 (0x07)**Table 111. sds prbs cfg2 (0x07)**

Bit	Symbol	Access	Default	Description
15:4	Reserved	RO	0x0	Reserved
3:0	Fix_pattern_19_16	RW	0x0	fix pattern transmited in test_mode 2

6.7.5. sds prbs mon1 (0x08)**Table 112. sds prbs mon1 (0x08)**

Bit	Symbol	Access	Default	Description
15:9	Fix_pattern	RO	0x0	Reserved
8	Err	RO	0x0	Err flag after PRBS has synchronized
7:2	Reserved	RO	0x0	Reserved
1	bisync_latch_low	RO LL	0x0	PRBS test synchronization status, once the sync is lost, this bit will latch low, until it's been read out.
0	Bitsync	RO	0x0	real time PRBS test synchronization status

6.7.6. sds prbs mon2 (0x09)**Table 113. sds prbs mon2 (0x09)**

Bit	Symbol	Access	Default	Description
15:0	Err_cnt_15_0	RO	0x0	real time lowest 16 bits received error bit counter

6.7.7. sds prbs mon3 (0x0A)**Table 114. sds prbs mon3 (0x0A)**

Bit	Symbol	Access	Default	Description
15:0	Err_cnt_31_16	RO	0x0	real time highest 16 bits received error bit counter

6.7.8. sds prbs mon4 (0x0B)**Table 115. sds prbs mon4 (0x0B)**

Bit	Symbol	Access	Default	Description
15:0	Good_cnt_15_0	RO	0x0	real time lowest 16 bits received good bit counter

6.7.9. sds prbs mon5 (0x0C)**Table 116. sds prbs mon5 (0x0C)**

Bit	Symbol	Access	Default	Description
15:0	Good_cnt_31_16	RO	0x0	real time highest 16 bits received good bit

				counter
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6.7.10. analog cfg2 (0xA1)

Table 117. analog cfg2 (0xA1)

Bit	Symbol	Access	Default	Description
15:12	Tx_driver_stg2	RW	0xA	TX driver stage2 amplitude control bit<3:2>: 00 +0mA 01: +2.5mA 10:+2.5mA 11+5mA bit<1:0>: 00 +0mA 01: +0.625mA 10: +1.25mA 11:+2.5mA
11	Tx_driver_stg1	RW	0x1	TX driver stage1 amplitude control
10:8	Reserved	RO	0x0	Reserved
7:6	vb_tx_term	RW	0x2	tx output common mode voltage when tx power down 00: 0.7V 01:0.8V 10:0.9V 11:1V
5	tx_vamp_post	RW	0x0	TX driver post stage1 amplitude control.
4	Reserved	RO	0x0	always 0.
3:1	tx_driver_post	RW	0x7	TX driver stage2 de-emphasize control bit<2>: 0 +0mA, 1: +2.5mA bit<1:0>: 00: +0mA 01: +0.625mA 10: +1.25mA 11:+2.5mA
0	Tx_pd	RW	0x0	power down analog tx

6.8. SDS(1.25G) EXT Register

6.8.1. sds prbs cfg1 (0x05)

Table 118. sds prbs cfg1 (0x05)

Bit	Symbol	Access	Default	Description
15	En_prbs	RW	0x0	enable TX PRBS or self-defined pattern, the pattern type is determined by bit7:5 test_mode.
14	En_bert	RW	0x0	enable Bit Error Rate Test;
13	Prbs_invert	RW	0x0	TX error injection function, it has highest polarity than prbs_err_once and prbs_err_cont. 1: to send polarity inverted PRBS or self- defined pattern;

12	Prbs_err_cont	RW	0x0	TX error injection function, it has the lowest polarity.1: to inject error on TX pattern continuously and periodic, the period is controlled by prbs_err_rate.
11:10	Prbs_err_rate	RW	0x0	It's valid only when prbs_err_cont is 1. 2'b00: inject one error every 1024 cycles; 2'b01: inject one error every 2048 cycles; 2'b10: inject one error every 4096 cycles; 2'b11: inject one error every 8192 cycles;
9	Prbs_err_once	RW	0x0	TX error injection function.At the rising of this bit, to send polarity inverted PRBS or self-defined pattern for one cycle;
8	Test_mode_prbs31	RW	0x0	1: PRBS31, bit7:5 test_mode[2:0] has no effect.0: not PRBS31, bit7:5 test_mode[2:0] take effect then.
7:5	Test_mode	RW	0x0	Control the TX pattern in test mode: 0x0, PRBS7; 0x1, PRBS10; 0x2, Fix pattern, the fix pattern is controlled by Ext.6;0x3, 010101...; 0x4, 00110011...; 0x5, 00000_11111_00000_11111...; 0x6, 0000_0000_00_1111_1111_11...; 0x7, Increase pattern, 0->1023->0->1023...
4	Duration_check_en	RW	0x0	enable fixed number of bits check define in sds EXT BA/BB
3:0	Reserved	RO	0x0	Reserved

6.8.2. sds prbs cfg2 (0x06)

Table 119. sds prbs cfg2 (0x06)

Bit	Symbol	Access	Default	Description
15:10	Reserved	RO	0x0	Reserved
9:0	Fix_pattern_9_0	RW	0x0	fix pattern transmited in test_mode 2

6.8.3. sds prbs mon1 (0x08)

Table 120. sds prbs mon1 (0x08)

Bit	Symbol	Access	Default	Description
15:9	Reserved	RO	0x0	Reserved
8	Err	RO	0x0	Err flag after PRBS has synchronized
7:2	Reserved	RO	0x0	Reserved
1	Bitsync_latch	RO LL	0x0	PRBS test synchronization status, once the sync is lost, this bit will latch low, until it's been read out.
0	Bitsync	RO	0x0	real time synchronization status

6.8.4. sds prbs mon2 (0x09)**Table 121. sds prbs mon2 (0x09)**

Bit	Symbol	Access	Default	Description
15:0	Err_cnt_15_0	RO	0x0	real time lowest 16 bits received error bit counter

6.8.5. sds prbs mon3 (0x0A)**Table 122. sds prbs mon3 (0x0A)**

Bit	Symbol	Access	Default	Description
15:0	Err_cnt_31_16	RO	0x0	real time highest 16 bits received error bit counter

6.8.6. sds prbs mon4 (0x0B)**Table 123. sds prbs mon4 (0x0B)**

Bit	Symbol	Access	Default	Description
15:0	Good_cnt_15_0	RO	0x0	real time lowest 16 bits received good bit counter

6.8.7. sds prbs mon5 (0x0C)**Table 124. sds prbs mon5 (0x0C)**

Bit	Symbol	Access	Default	Description
15:0	Good_cnt_31_16	RO	0x0	real time highest 16 bits received good bit counter

6.8.8. analog cfg2 (0xA1)**Table 125. analog cfg2 (0xA1)**

Bit	Symbol	Access	Default	Description
15:12	Tx_driver_stg2	RW	0xA	Amplitude control of TX driver, 4'b0000: min; 4'b1111: max
11	Tx_driver_stg1	RW	0x1	TX driver stage1 amplitude control
10:8	Tx_ckdiv10_con	RW	0x0	tx divide by 10 clock delay control
7:6	vb_tx_term	RW	0x0	not used
5	tx_vamp_post	RW	0x0	not used
4	tx_post_en	RW	0x0	Enable or disable TX de-emphasis. 1'b0: disable; 1'b1: enable
3:1	tx_driver_post	RO	0x7	Amplitude control of TX de-emphasis. 3'b000: min; 3'b111: max
0	Tx_pd	RW	0x0	power down analog tx

7. Electrical Characteristics

7.1. DC Characteristics

Table 126. DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
DVDDIO, AVDDH, SVDDH	3.3V Supply Voltage	3.135	3.30	3.465	V
DVDDL, AVDDL, SVDDL, PLLVDDL	1.2V Supply Voltage	1.14	1.20	1.26	V
Voh	High Level Output Voltage	2.4	-	-	V
Vol	Low Level Output Voltage	-	-	0.4	V
Vih	High Level Input Voltage	DVDDIO-0.7	-	-	V
Vil	Low Level Input Voltage	-	-	GND+0.7	V

7.2. AC Characteristics

7.2.1. QSGMII Differential Transmitter Characteristics

Table 127. QSGMII Differential Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit Interval	-	200	-	ps
T_X1	Eye Mask	-	-	0.15	UI
T_X2	Eye Mask	-	-	0.4	UI
T_Y1	Eye Mask	200	-	-	mV
T_Y2	Eye Mask	-	-	450	mV
T _{TX-JITTER}	Output Jitter	-	-	0.30	UI
T _{TX-RISE}	Output Rise Time	30	-	-	ps
T _{TX-FALL}	Output Fall Time	30	-	-	ps
R _{TX}	Differential Resistance	80	100	120	ohm
C _{TX}	AC Coupling Capacitor	75	100	200	nF

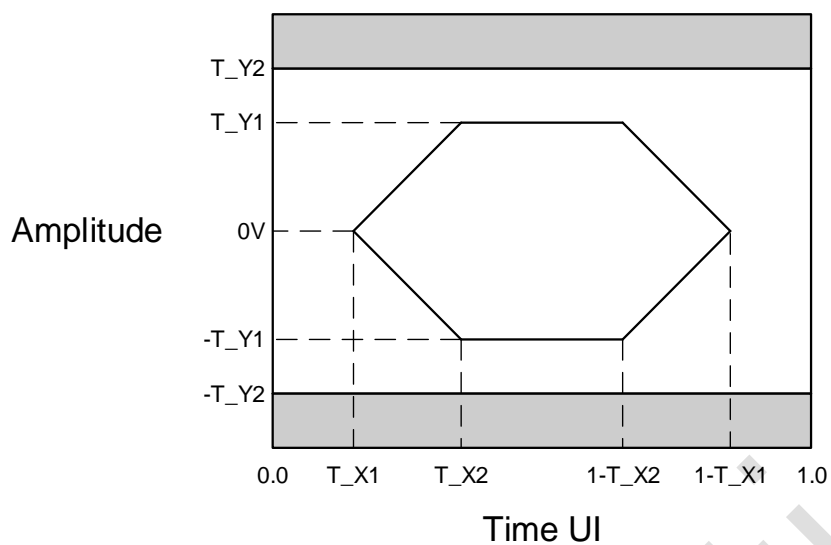


Figure 13. QSGMII Differential Transmitter Eye Diagram

7.2.2. QSGMII Differential Receiver Characteristics

Table 128. QSGMII Differential Receiver Characteristics

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit Interval	-	200	-	ps
R_X1	Eye Mask	-	-	0.3	UI
R_Y1	Eye Mask	50	-	-	mV
R_Y2	Eye Mask	-	-	450	mV
T _{RX-JITTER}	Input Jitter Tolerance	-	-	0.60	UI
R _{RX}	Differential Resistance	80	100	120	ohm

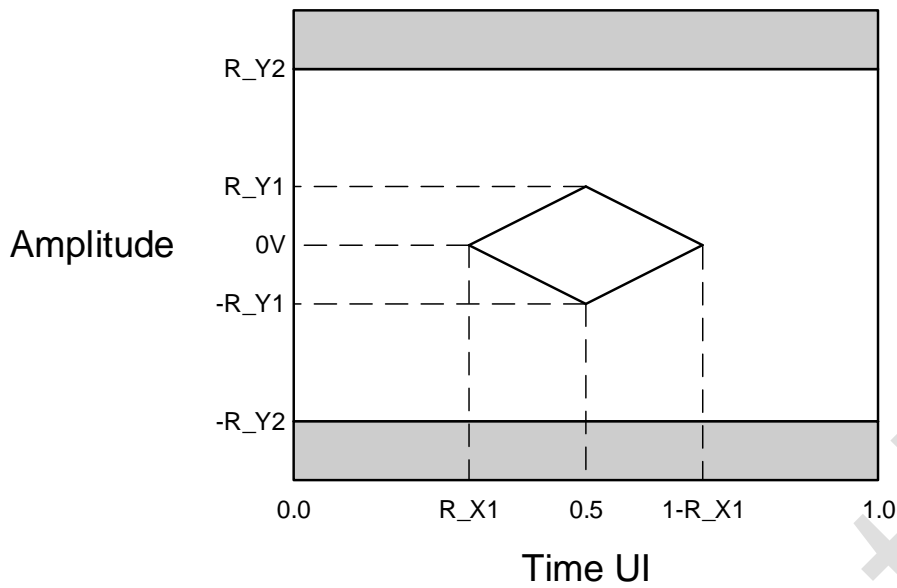


Figure 14. QSGMII Differential Receiver Eye Diagram

7.2.3. SGMII Differential Transmitter Characteristics

Table 129. SGMII Differential Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	799.94	800	800.06	ps	800ps \pm 75ppm
T_X1	Eye Mask	-	-	0.1875	UI	-
T_X2	Eye Mask	-	-	0.4	UI	-
T_Y1	Eye Mask	125	-	-	mV	-
T_Y2	Eye Mask	-	-	500	mV	-
V _{TX-DIFFp-p}	Output Differential Voltage	400	700	900	mV	-
T _{TX-EYE}	Minimum TX Eye Width	0.625	-	-	UI	-
T _{TX-JITTER}	Output Jitter	-	-	0.375	UI	T _{TX-JITTER-MAX} = 1 - T _{TX-EYE-MIN} = 0.375UI
R _{TX}	Differential Resistance	80	100	120	ohm	-
C _{TX}	AC Coupling Capacitor	75	100	200	nF	-
L _{TX}	Transmit Length in PCB	-	-	10	inch	-

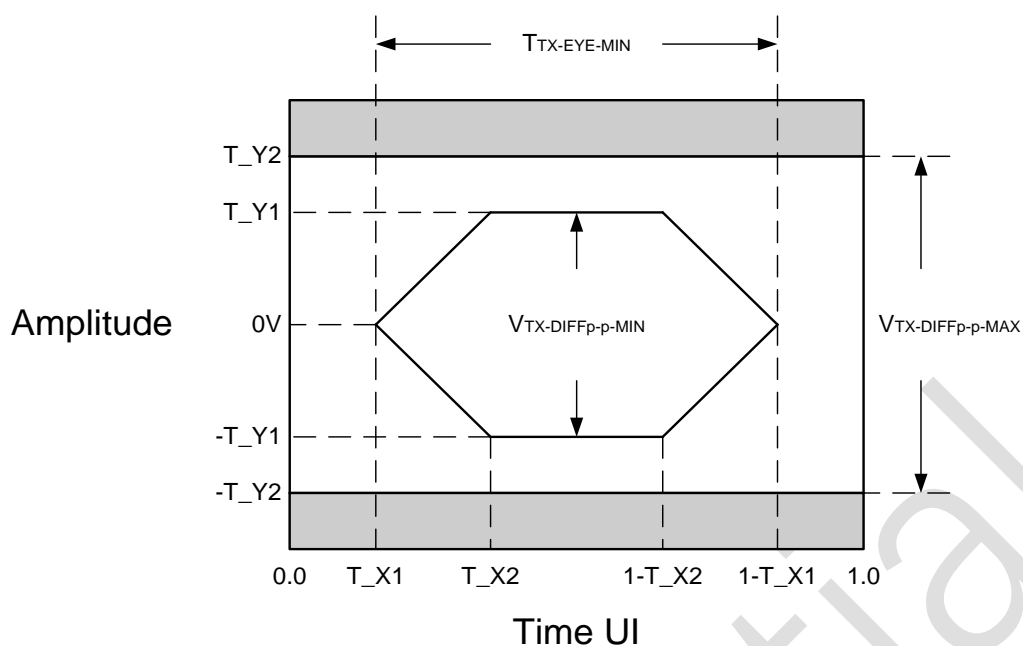


Figure 15. SGMII Differential Transmitter Eye Diagram

7.2.4. SGMII Differential Receiver Characteristics

Table 130. SGMII Differential Receiver Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	799.94	800	800.06	ps	$800\text{ps} \pm 75\text{ppm}$
R_X1	Eye Mask	-	-	0.3125	UI	-
R_Y1	Eye Mask	50	-	-	mV	-
R_Y2	Eye Mask	-	-	1000	mV	-
V _{RX-DIFFp-p}	Input Differential Voltage	100	-	2000	mV	-
T _{RX-EYE}	Minimum RX Eye Width	0.375	-	-	UI	-
T _{RX-JITTER}	Input Jitter Tolerance	-	-	0.625	UI	$T_{\text{RX-JITTER-MAX}} = 1 - T_{\text{RX-EYE-MIN}} = 0.625\text{UI}$
R _{RX}	Differential Resistance	80	100	120	ohm	-

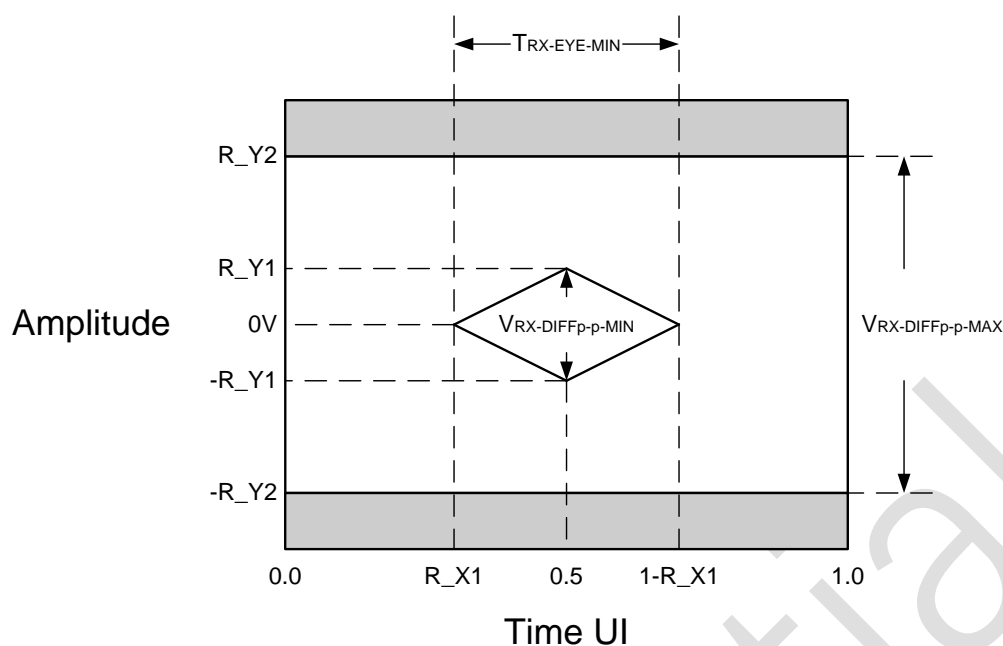


Figure 16. SGMII Differential Receiver Eye Diagram

7.2.5. SMI (MDC/MDIO) Interface Characteristics

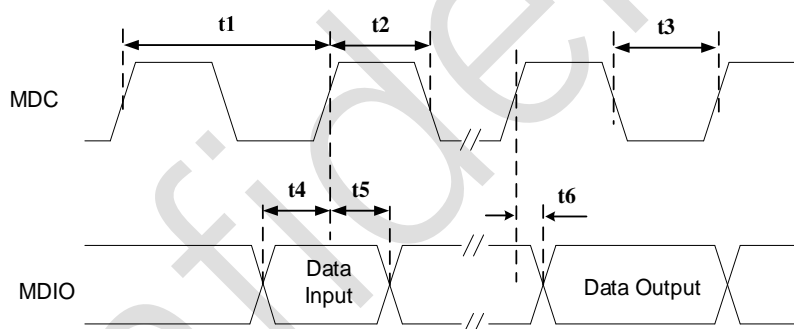


Figure 17. SMI (MDC/MDIO) Timing

Table 131. SMI (MDC/MDIO) Interface Characteristics

Symbol	Description	Min	Typ	Max	Units
t1	MDC Clock Period	80	-	-	ns
t2	MDC High Time	32	-	-	ns
t3	MDC Low Time	32	-	-	ns
t4	MDIO to MDC Rising Setup Time (Data Input)	10	-	-	ns
t5	MDIO to MDC Rising Hold Time (Data Input)	10	-	-	ns
t6	MDIO Valid from MDC rising edge (Data Output)	0	-	20	ns

7.2.6. Reset Characteristics

Table 132. Reset Timing Characteristics

Symbol	Description	Min	Typ	Max	Units
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T1	The duration from all powers steady to reset signal release to high	10	-	-	ms
T2	The duration of reset signal remain low timing	10	-	-	ms

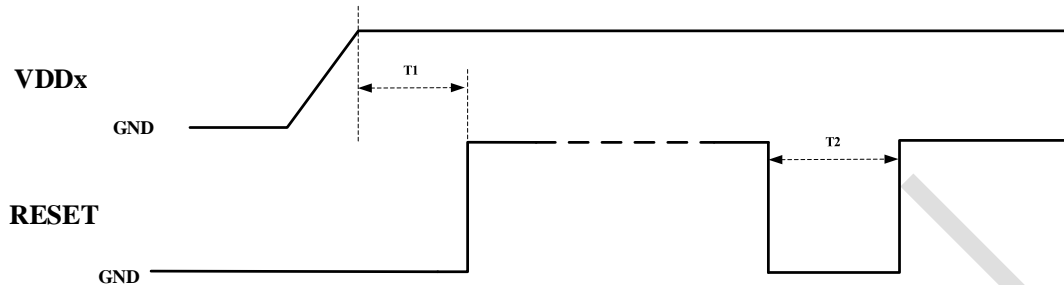


Figure 18. Reset Timing Diagram

7.3. Crystal Requirement

Table 133. Crystal Requirement

Symbol	Description	Min	Typ	Max	Unit
Fref	Parallel Resonant Crystal Reference Frequency	-	25	-	MHz
Fref Tolerance	Parallel Resonant Crystal Reference Frequency Tolerance	-50	-	50	ppm
Fref Duty Cycle	Reference Clock Input Duty Cycle	40	-	60	%
ESR	Equivalent Series Resistance	-	-	50	ohm
DL	Drive Level	-	-	0.5	mW
Vih	Crystal output high level	1.5	-	-	V
Vil	Crystal output low level	-	-	0.4	V

7.4. Oscillator/External Clock Requirement

Table 134. Oscillator/External Clock Requirement

Parameter	Min	Typ	Max	Unit
Frequency		25		MHz
Frequency tolerance	-50		50	PPM
Duty Cycle	40	-	60	%
Peak to Peak Jitter			50	ps
Vih	1.6		AVDD33+0.3	V
Vil			0.4	V
Rise Time (10%~90%)			10	ns
Fall Time (10%~90%)			10	ns
25kHz~25MHz RMS Jitter			1	ps
Broadband RMS Jitter			3	ps

8. Power Requirements

8.1. Absolute Maximum Ratings

Table 135. Absolute Maximum Ratings

Symbol	Description	Mini	Max	Unit
AVDDH	3.3 V power supply	-0.3	3.63	V
DVDDIO	3.3 V power supply	-0.3	3.63	V
AVDDL	1.2 V power supply	-0.2	1.32	V
DVDDL	1.2 V power supply	-0.2	1.32	V
PLLVDL	1.2 V power supply	-0.2	1.32	V
Junction Temperature		–	125	°C

8.2. Recommended Operating Conditions

Table 136. Recommended Operating Conditions

Description	Pins	Min	Typ	Max	Unit
Supply Voltage	DVDDIO	3.14	3.30	3.47	V
	AVDDH	3.14	3.30	3.47	V
	AVDDL	1.14	1.20	1.26	V
	DVDDL	1.14	1.20	1.26	V
	PLLVDL	1.14	1.20	1.26	V
Ambient Operation Temperature Ta Commercial		0	-	70	°C
Ambient Operation Temperature Ta Industry		-40	-	85	°C

8.3. Power Sequence

8.4. Power Consumption

8.4.1. QSGMII x 1 + Combo x 4

Table 137. QSGMII x 1 + Combo x 4 Power Consumption

Condition	AVDDH (mA)	DVDDH (mA)	SVDDH (mA)	AVDDL (mA)	DVDDL (mA)	SVDDL (mA)	Power Consumption (mW)
Reset	45.3	0.2	2.1	2.1	7.3	9.6	179.88
Power Down	46.4	0.2	2.1	2.8	7	11.5	186.27

Copper Link Up @1000Mbps	296.6	39	29.7	178.2	390.2	60.2	1959.81
Copper Traffic @1000Mbps	296.2	39	29.7	178.2	421.3	60.5	1996.17
Fiber Link Up @1000Mbps	47.8	0.3	35.7	3.5	47.5	154	522.54
Fiber Traffic @1000Mbps	47.8	0.3	35.7	3.5	46.5	154	521.34

Note: Test by TT IC with VDDH = 3.3V and VDDL = 1.2V.

8.4.2. QSGMII x 1 + Copper x 4

Table 138. QSGMII x 1 + Copper x 4 Power Consumption

Condition	AVDDH (mA)	DVDDH (mA)	SVDDH (mA)	AVDDL (mA)	DVDDL (mA)	SVDDL (mA)	Power Consumption (mW)
Reset	45.3	0.1	2.1	2.1	7.3	9.6	179.55
Power Down	46.4	0.1	2.1	2.8	7.1	11.5	186.06
Link Up @1000Mbps	296.5	39.1	29.7	178.1	391.5	60.4	1961.49
Traffic @1000Mbps	296.2	39	29.8	178.2	423	60.5	1998.54

Note: Test by TT IC with VDDH = 3.3V and VDDL = 1.2V.

8.4.3. QSGMII x 1 + Fiber x 4

Table 139. QSGMII x 1 + Fiber x 4 Power Consumption

Condition	AVDDH (mA)	DVDDH (mA)	SVDDH (mA)	AVDDL (mA)	DVDDL (mA)	SVDDL (mA)	Power Consumption (mW)
Power Down	46.4	0.3	2.1	2.8	7.1	11.5	186.72
Link Up @1000Mbps	46.5	0.3	35.7	2.8	49.4	153.9	519.57
Traffic @1000Mbps	46.4	0.3	35.7	2.8	48.3	154	518.04

Note: Test by TT IC with VDDH = 3.3V and VDDL = 1.2V.

8.4.4. QSGMII x 1 + SGMII x 4

Table 140. QSGMII x 1 + SGMII x 4 Power Consumption

Condition	AVDDH (mA)	DVDDH (mA)	SVDDH (mA)	AVDDL (mA)	DVDDL (mA)	SVDDL (mA)	Power Consumption (mW)
Power Down	46.4	0.3	2.1	2.8	7.1	11.5	186.72
Link Up @1000Mbps	46.5	0.3	35.7	2.8	51.7	154	522.45

Traffic @1000Mbps	46.4	0.3	35.7	2.8	49.7	154	519.72
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Note: Test by TT IC with VDDH = 3.3V and VDDL = 1.2V.

8.4.5. SGMII x 4 + Copper x 4

Table 141. SGMII x 4 + Copper x 4 Power Consumption

Condition	AVDDH (mA)	DVDDH (mA)	SVDDH (mA)	AVDDL (mA)	DVDDL (mA)	SVDDL (mA)	Power Consumption (mW)
Reset	45.4	0.2	2.1	2.1	7.4	9.6	180.33
Power Down	46.4	0.2	2.1	2.8	7.1	12.6	187.71
Link Up @1000Mbps	296.8	6.1	8.5	178.2	397.3	108.1	1847.94
Traffic @1000Mbps	295.8	6.1	8.5	178.4	455.1	108	1914.12

Note: Test by TT IC with VDDH = 3.3V and VDDL = 1.2V.

8.4.6. Copper x 4 + Fiber x 4

Table 142. Copper x 4 + Fiber x 4 Power Consumption

Condition	AVDDH (mA)	DVDDH (mA)	SVDDH (mA)	AVDDL (mA)	DVDDL (mA)	SVDDL (mA)	Power Consumption (mW)
Reset	45.4	0.2	2.1	2.1	7.4	9.6	180.33
Power Down	46.4	0.2	2.1	2.8	7.1	12.6	187.71
Link Up @1000Mbps	296.6	6.1	8.5	178.2	397.7	108.1	1847.76
Traffic @1000Mbps	295.8	6.1	8.5	178.4	455.2	108	1914.24

Note: Test by TT IC with VDDH = 3.3V and VDDL = 1.2V.

8.5. Maximum Power Consumption

Table 143. Maximum Power Consumption

Condition	AVDDH (mA)	DVDDH (mA)	SVDDH (mA)	AVDDL (mA)	DVDDL (mA)	SVDDL (mA)	Power Consumption (mW)
Reset	48	0.1	2.2	2.2	7.7	10.2	190.11
Power Down	49.2	35.9	2.2	3	7.5	12.2	315.33
Link Up @1000Mbps	314.3	41.4	31.5	188.8	415	64	2079.12
Traffic @1000Mbps	314	41.3	31.6	188.9	448.4	64.1	2118.45

Note: Test by FF corner IC in QSGMII x 1 + Copper x 4 mode with VDDH = 3.3V and VDDL = 1.2V at high temperature 85°C.

8.6. Power Noise

The max noise of 3.3V should be under 50mV, and that of 1.2V should be under 30mV.

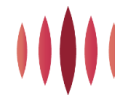
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9. Thermal Characteristics

9.1. Thermal Resistance

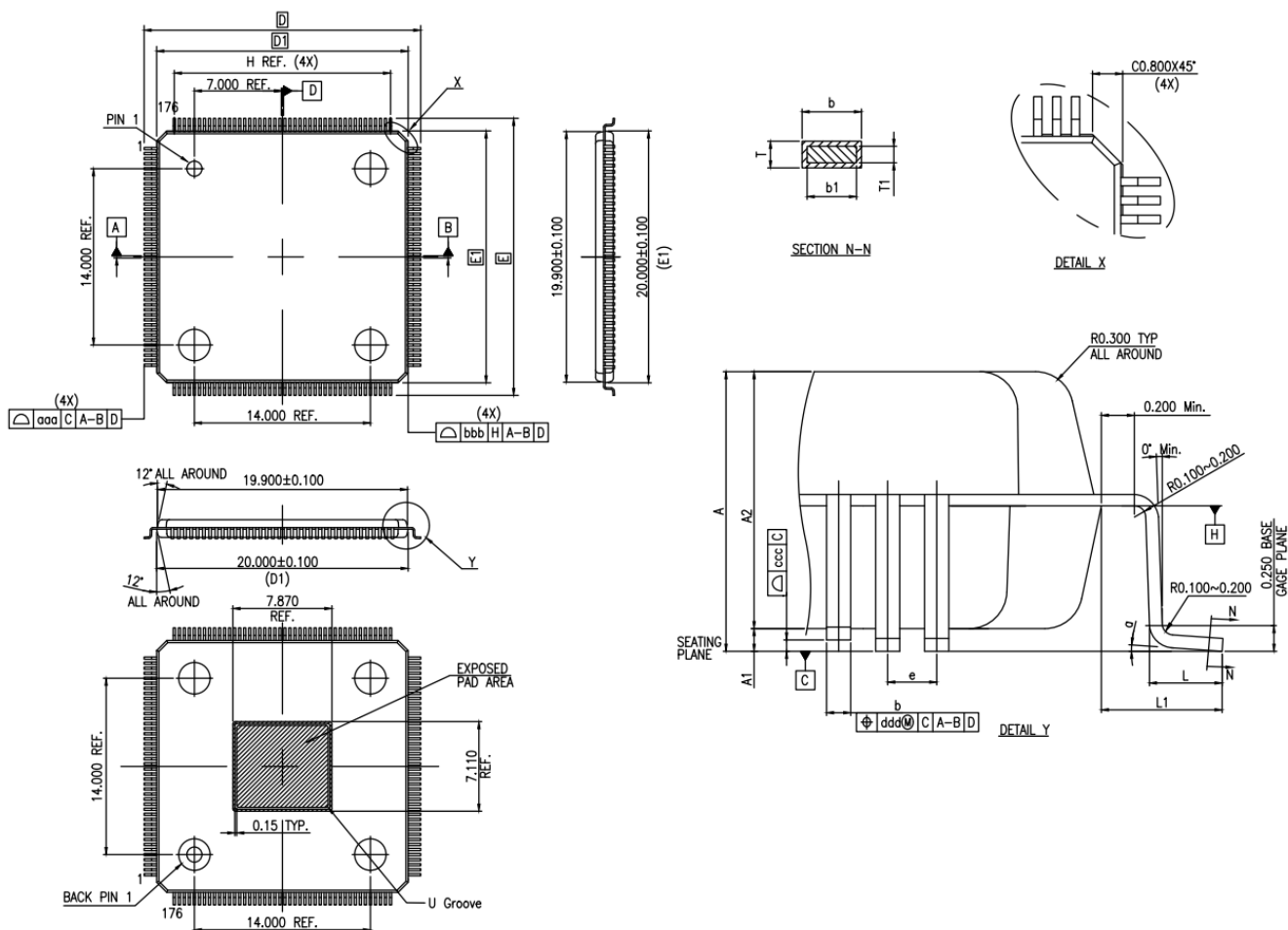
Table 144. Thermal Resistance

Symbol	Parameter	Condition	Typ	Units
θ_{JA}	Thermal resistance - junction to ambient $\theta_{JA} = (T_J - T_A) / P$ P = Total power dissipation	JEDEC 3.0 in. x 4.5 in. 4-layer PCB with no air flow $T_A = 25^\circ\text{C}$	21.2	$^\circ\text{C/W}$
		JEDEC 3.0 in. x 4.5 in. 4-layer PCB with no air flow $T_A = 85^\circ\text{C}$	19.22	$^\circ\text{C/W}$
θ_{JC}	Thermal resistance - junction to case $\theta_{JC} = (T_J - T_C) / P_{top}$ P_{top} = Power dissipation from the top of the package	JEDEC with no air flow	13.49	$^\circ\text{C/W}$
θ_{JB}	Thermal resistance - junction to board $\theta_{JB} = (T_J - T_B) / P_{bottom}$ P_{bottom} = Power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow	10.63	$^\circ\text{C/W}$



10. Package Information

10.1. LQFP-176 E-PAD



10.2. Mechanical Dimensions

DIMENSION LIST (FOOTPRINT: 2.00)

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 1.600	OVERALL HEIGHT
2	A1	$0.100^{+0.027}_{-0.050}$	STANDOFF
3	A2	1.400 ± 0.050	PKG THICKNESS
4	D	22.000 ± 0.200	LEAD TIP TO TIP
5	D1	20.000 ± 0.100	PKG LENGTH
6	E	22.000 ± 0.200	LEAD TIP TO TIP
7	E1	20.000 ± 0.100	PKG WIDTH
8	L	0.600 ± 0.150	FOOT LENGTH
9	L1	1.000 REF.	LEAD LENGTH
10	T	$0.150^{+0.050}_{-0.060}$	LEAD THICKNESS
11	T1	0.127 ± 0.030	LEAD BASE METAL THICKNESS
12	a	$0^{\circ} \sim 7^{\circ}$	FOOT ANGLE
13	b	0.180 ± 0.050	LEAD WIDTH
14	b1	0.160 ± 0.030	LEAD BASE METAL WIDTH
15	e	0.400 BASE	LEAD PITCH
16	H (REF.)	(17.200)	CUM. LEAD PITCH
17	aaa	0.200	PROFILE OF LEAD TIPS
18	bbb	0.200	PROFILE OF MOLD SURFACE
19	ccc	0.080	FOOT COPLANARITY
20	ddd	0.080	FOOT POSITION

NOTES :

S/N	DESCRIPTION		SPECIFICATION
1	GENERAL TOLERANCE.	DISTANCE	± 0.100
		ANGLE	$\pm 2.5^{\circ}$
2	MATTE FINISH ON PACKAGE BODY SURFACE EXCEPT EJECTION AND PIN 1 MARKING.		Ra0.8~2.0um
3	ALL MOLDED BODY SHARP CORNER RADII UNLESS OTHERWISE SPECIFIED.		MAX. R0.200
4	PACKAGE/LEADFRAME MISALIGNMENT (X, Y):		MAX. 0.127
5	TOP/BTM PACKAGE MISALIGNMENT (X, Y):		MAX. 0.127
6	DRAWING DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OR CUTTING BURR.		
7	COMPLIANT TO JEDEC STANDARD: MS-026		

11. Ordering Information

Motorcomm offers an RoHS package that is compliant with RoHS.

Part Number	Grade	Package	Pack	Status	Operation Temp
YT8614 C XXXX	Consumer	LQFP-176 E-PAD	TBD		0 ~70°C
YT8614 H XXXX	Industrial	LQFP-176 E-PAD	TBD		-40 ~ 85°C

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