SENSYLINK Microelectronics

(CT80)

System Thermal Monitor with Digital Interface

CT80 is a system level solution chip to sense local temperature and monitor 7-channels external analog and/or digital temperature sensor, fan speed with I^2C, SMBus Digital Interface.

It is ideally used in System Level Thermal Monitoring, such as Server and Telecom Equipment System etc.

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Description

The CT80 is a system level thermal monitor solution chip, with digital interface.

It includes local temperature sensor, 7-channel analog input, 2 channel programmable fan speed monitor, 3 channel digital input for logic monitor and 3 channel logic output.

Analog input can be used for voltage monitor, like connecting analog output temperature sensor (like CT7035) or monitor power supply voltage. Digital input can sense digital temperature sensor (like CT75) ALERT/THERM logic output.

The chip supports both speed of standard mode (100 kHz) and fast mode (400 kHz) for digital communication.

Available Package: TSSOP-24

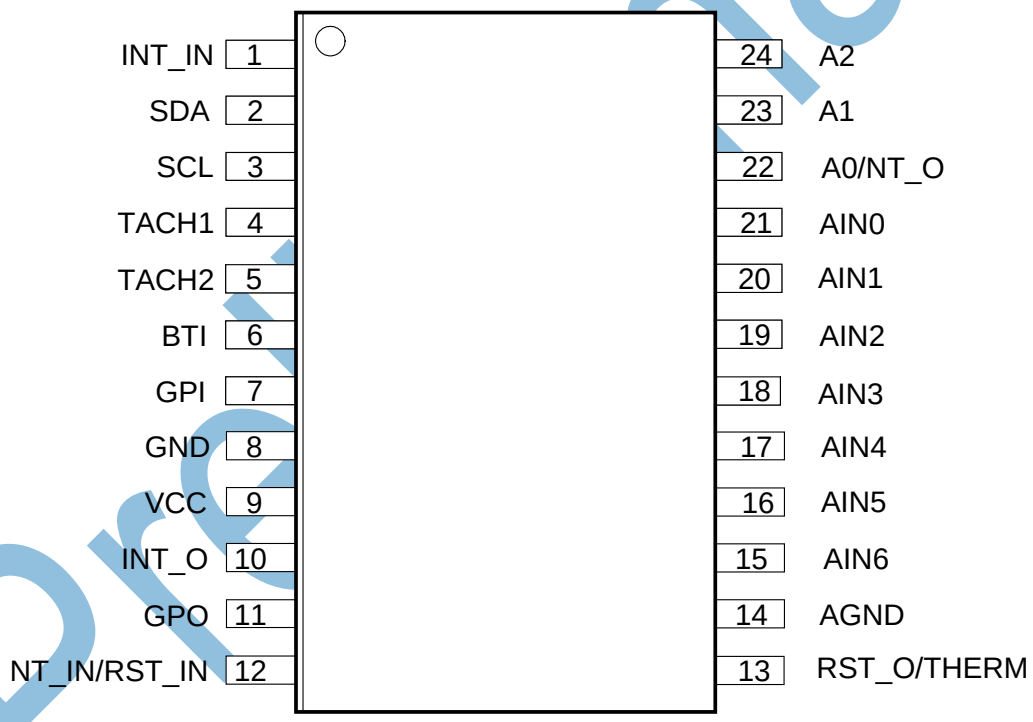
Features

- Operation Voltage: 2.7V to 5.5V
- Average Quiescent Current: 350uA (Typ.)
- Standby Current: 50uA (Typ.)
- Local Temperature Sensor with ±1°C Accuracy, 0.0625°C resolution
- 7-CH Analog Input for Voltage Monitor
- 2-CH Fan Speed Monitor
- 3-CH Logic Input for interrupt Monitor
- 2-CH Logic Output for interrupt Alarm
- 8 different slave address by setup A0/A1/A2 pin
- Alarm output for over/under limit temperature
- SMBus and I²C Digital interface up to 400kHz
- Temperature Range: -40°C to 125°C

Applications

- Server
- Telecom Equipment

PIN Configurations (Top View)



TSSOP-24 (Package Code, MT)

Typical Application

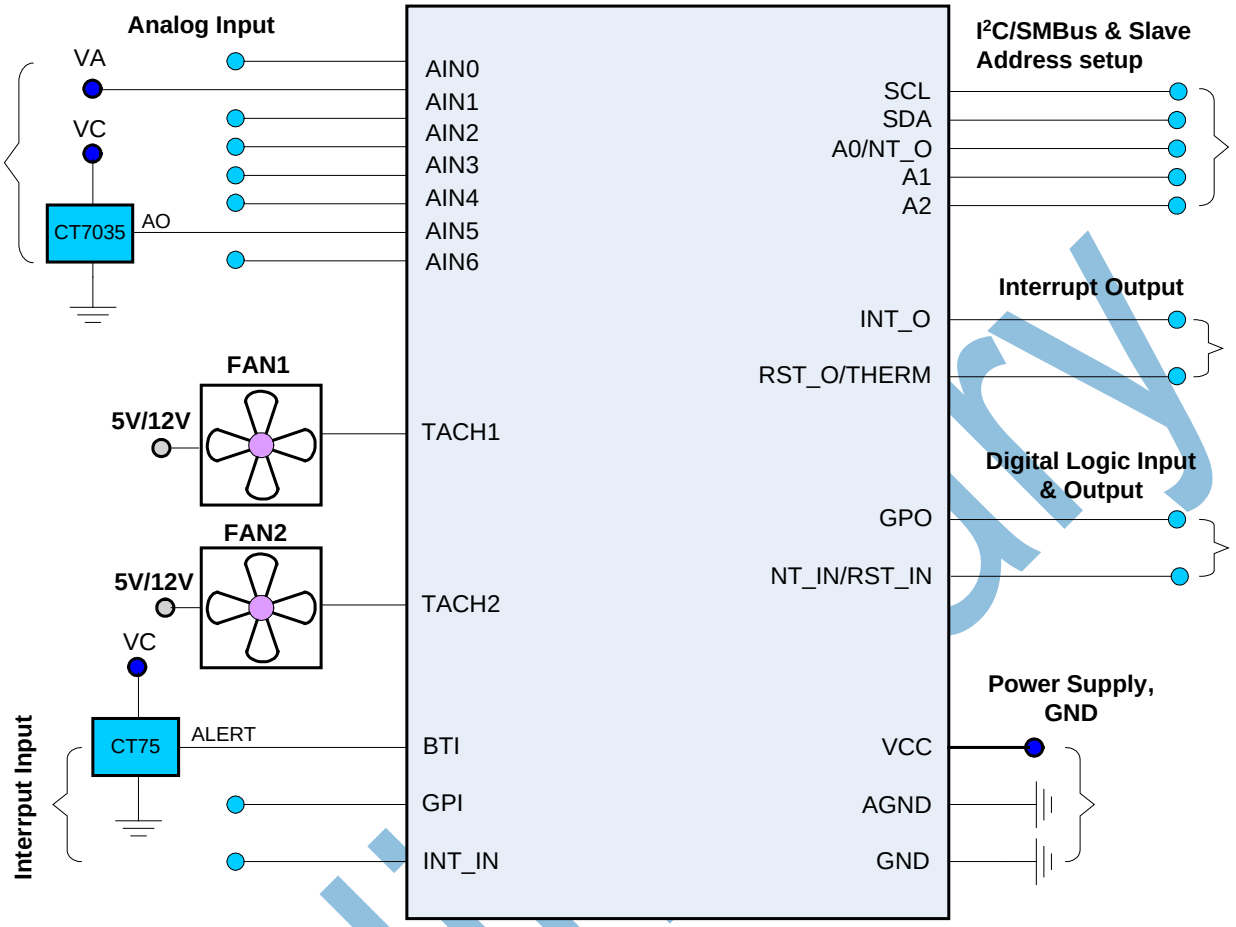


Figure 1. Typical Application of CT80

Pin Description

PIN No.	PIN Name	Description
1	INT_IN	Interrupt input pin with active low, it propagates to INT_O pin of the chip.
2	SDA	Digital interface data input or output pin, need a pull-up resistor to VCC.
3	SCL	Digital interface clock input pin, need a pull-up resistor to VCC.
4	TACH1	Fan1 tachometer input for speed measurement.
5	TACH2	Fan2 tachometer input for speed measurement.
6	BTI	Board temperature interrupt input with active low, this pin can be connected to ALERT output of CT75. This pin has an internal pull-up resistor of 10k ohm.
7	GPI	General purpose digital input pin with active high.
8	GND	Ground pin.
9	VCC	Power supply input pin, using 0.1uF low ESR ceramic capacitor to ground
10	INT_O	Interrupt output pin with active low, it gets active once BTI, INT_IN or GPI pin interrupt happens. This pin does not need an external pull-up resistor.
11	GPO	General purpose digital output pin with active low, open drain. This pin needs an external pull-up resistor of 4.7k to 10k.

12	NT_IN/RST_IN	Digital input with active low, apply logic low on this pin will enable NAND combinatory logic tree function test; also it will reset the chip and all registers will reset as default data. this pin needs a pull-up resistor of 4.7k to 10k to VCC.
13	RST_O/THERM	Interrupt output pin with active low, open drain. This pin needs a pull-up resistor of 4.7k to 10k. It can be used to reset the host chip. This pin will be active once interrupt alarm happens caused by over/under limit temperature.
14	AGND	Analog ground pin
15	AIN6	Analog input channel 6, 0 to 2.56V range with 2.5mV resolution.
16	AIN5	Analog input channel 5, 0 to 2.56V range with 2.5mV resolution.
17	AIN4	Analog input channel 4, 0 to 2.56V range with 2.5mV resolution.
18	AIN3	Analog input channel 3, 0 to 2.56V range with 2.5mV resolution.
19	AIN2	Analog input channel 2, 0 to 2.56V range with 2.5mV resolution.
20	AIN1	Analog input channel 1, 0 to 2.56V range with 2.5mV resolution.
21	AIN0	Analog input channel 0, 0 to 2.56V range with 2.5mV resolution.
22	A0/NT_O	Slave Address setup bit0. Also this bit can be used as logic output during NAND combinatory logic tree function test.
23	A1	Slave Address setup bit1
24	A2	Slave Address setup bit2

Function Block

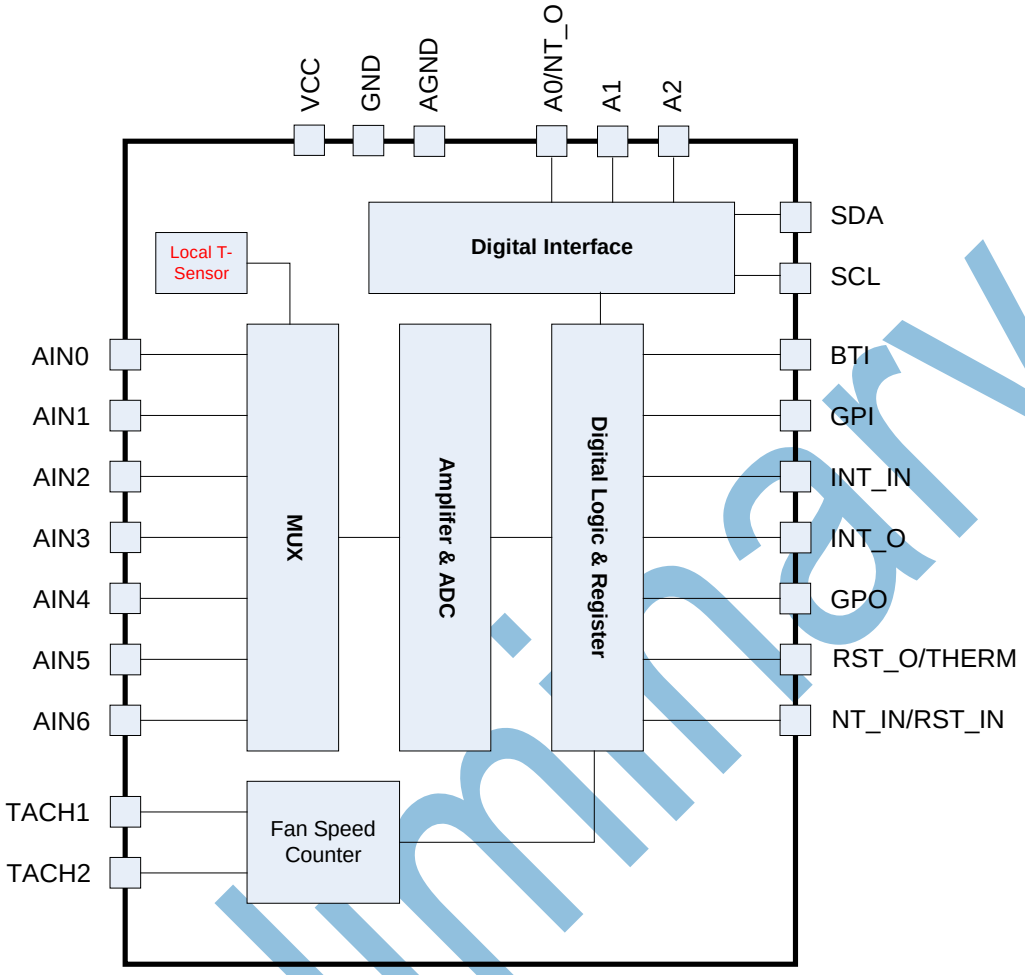
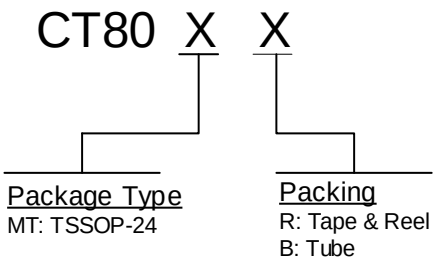


Figure 2. CT80 function block

Ordering Information



Order PN	Accuracy	Green[1]	Package	Marking ID[1]	Packing	MPQ	Operation Temperature
CT80MTR	±1 °C	Halogen free	TSSOP-24	80 YWWAXX	Tape & Reel	4,000	-40°C~+125°C

1. Based on ROHS Y2012 spec, Halogen free covers lead free. So most package types Sensylink offers only states halogen free, instead of lead free.

2. Marking ID includes 2 rows of characters. In general, the 1st row of characters are part number, and the 2nd row of characters are date code plus production information.

1) *Generally, date code is represented by 3 numbers. The number stands for year and work week information. e.g. 501stands for the first work week of year 2015;621 stands for the 21st work week of year 2016.*
2) *Right after the date code information, the next 2-3 numbers or letters are specified to stands for supplier or production location information.*
3) *For very small outline package, there's 4 digits to stands for product information and date code, first 2 digits represent product code, and the other 2 digits stands for work week*

Absolute Maximum Ratings (Note 2)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC} to GND	-0.3 to 5.5	V
Analog Input (AIN0-AIN6)	V_{AIN0} ...V_{AIN6} to GND	-0.3 to VCC+0.3	V
SDA, SCL, A0, A1, A2 Voltage	V_{SDA}/V_{SCL}/V_{A0}/V_{A1}/V_{A2}/to GND	-0.3 to 5.5	V
TACH1/2 Voltage	$V_{TACH1/2}$ to GND	-0.3 to 5.5	V
Interrupt Input/output (BTI, GPI, INT_IN, INT_O, RST_O/THERM)	$V_{INTI/O}$ to GND	-0.3 to 5.5	V
Logic Input/output (GPO, RST_IN)	$V_{IN/OUT}$ to GND	-0.3 to 5.5	V
Input Current at any pin	$I_{IN/OUT}$ to GND	±5.0	mA
Operation Junction temperature	T_J	-50 to 150	ºC
Storage temperature Range	T_{STG}	-65 to 150	ºC
Lead Temperature (Soldering, 10 Seconds)	T_{LEAD}	260	ºC
ESD Machine Mode	ESD_{MM}	±200	V
ESD Human Body Mode	ESD_{HBM}	±2000	V
ESD Charge Device Mode	ESD_{CDM}	±500	V

Note 2

1. *St Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at the "Absolute Maximum Ratings" conditions or any other conditions beyond those indicated under "Recommended Operating Conditions" is not recommended. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.*

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2.7 ~ 5.5	V
Ambient Operation Temperature Range	T_A	-40 ~ +125	°C

Electrical Characteristics (Note 3)

Test Condition: V_{CC} = 3.3V, T_A = -30 to 125°C, unless otherwise specified, all limits are 100% test at T_A=25°C.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		2.7		5.5	V
Average Operating Current	I_{AOC}	V_{IN} = 3.3V, 1.0 Con/s		350		uA
		V_{IN} = 5.0V,1.0 Con/s		400		uA
Shutdown Current	$I_{SHUTDOWN}$	Shutdown mode, I2C inactive		30		uA
Local Temperature Sensor						
Temperature Sensor Accuracy	T_{RAC}	T_A = 20 to 85°C	-1.0		1.0	°C
		T_A = -40 to 125°C	-3.0		3.0	°C
Resolution		12 bit		0.0625		°C
Total Conversion time (NOTE3)	t_{CON}			600		ms
Analog Input						
Input Range	V_{IN}		0		2.560	V
Resolution		10 bit ADC, full scale 2.56V		2.50		mV
ADC bit				10		bit
Input Resistance	R_{IN}			2		kohm
Input Leakage	$I_{LEAKAGE}$	Set ON or OFF		±0.005		uA
FAN RPM to Digital Converter						
RPM Error			-10%		+10%	
Internal clock	f_{CLK}			22.5		kHz
Fan scale counter		8-bit			255	
Fan nominal speed	FAN_{SPEED}	Divisor = 1, fan counter = 153		8800		RPM
		Divisor = 2, fan counter = 153		4400		RPM
		Divisor = 3, fan counter = 153		2200		RPM
		Divisor = 4, fan counter = 153		1100		RPM
Digital Input ()						
Logic Input High Voltage	V_{IH}	Except BTI pin	0.7*VCC		VCC	V
Logic Input Low Voltage	V_{IL}	Except BTI pin	0		0.3*VCC	V
Logic Input Capacitance	C_{IL}			5.0		pF
Logic Input Current	I_{INL}	Except BTI pin	-1.0		1.0	uA
		BTI pin, VIN = VCC	-10			uA
		BTI pin, VIN = 0			2000	uA
Digital Output with push-pull (A0/NT_O, INT_O pin)						
Logic Output High Voltage	V_{OH}	Source current 5.0mA, VCC 2.7 to 5.5	2.4			V
Logic Output Low Voltage	V_{OL}	Sink current 5.0mA, VCC 2.7 to 5.5			0.4	V
Digital Output with open-drain (GPO, RST_O/THERM, SDA pin)						
Output Voltage (Logic low)	V_{OL}	sink current 5mA	0		0.2	V
Output Leakage (logic high)	I_{ODL}	Vout = Vcc	-1.0		1.0	uA
Pulse width	t_{PW}	RST_O/TERM, GPI pin		22		ms
Digital Communication Interface (I2C, SMBus)						
SCL frequency	f_{CLK}	SCL pin (Note 3)	10		400	kHz
Timeout of detecting clock or data low period time	t_{TOUT}			30		ms
Clock low period time	t_{LOW}		4.7			us
Clock high period time	t_{HIGH}		4.0		50	us
Bus free time	t_{BUF}	Between Stop and Start condition	4.7			us
Hold time after Start condition	$t_{HD:STA}$		4.0			us
Repeated Start condition setup time	$t_{SU:STA}$		4.7			us
Stop condition setup time	$t_{SU:STO}$		4.0			us

Data Hold time	$t_{HD:DAT}$		300			ns
Data Setup time	$t_{SU:DAT}$		250			ns
Clock/Data fall time	t_F				300	ns
Clock/Data rise time	t_{SR}				1000	ns

Note 3:

1. *All devices are 100% production tested at TA = +25°C; all specifications over the automotive temperature range is guaranteed by design, not production tested.*
2. *Total conversion time, includes local temperature, 7 channels analog input and 2 channel fan tachometer conversion.*
3. *The minimal clock frequency, 10kHz which is compatible to SMBus specification. There is no limitation for I2C protocol; the minimal frequency is limited by time-out feature with 35ms in typical, we recommend the minimal frequency of clock is 1000Hz.*

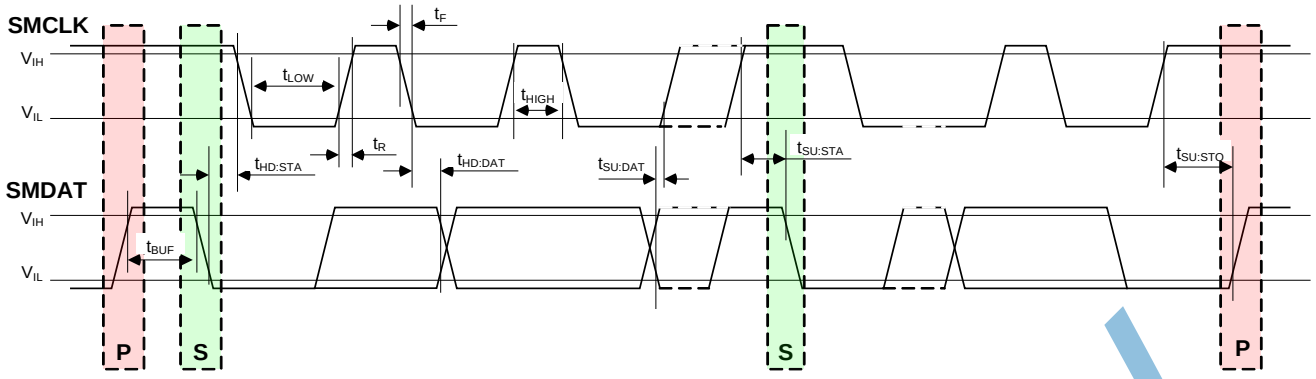


Figure 3. SMBusTimingDiagram

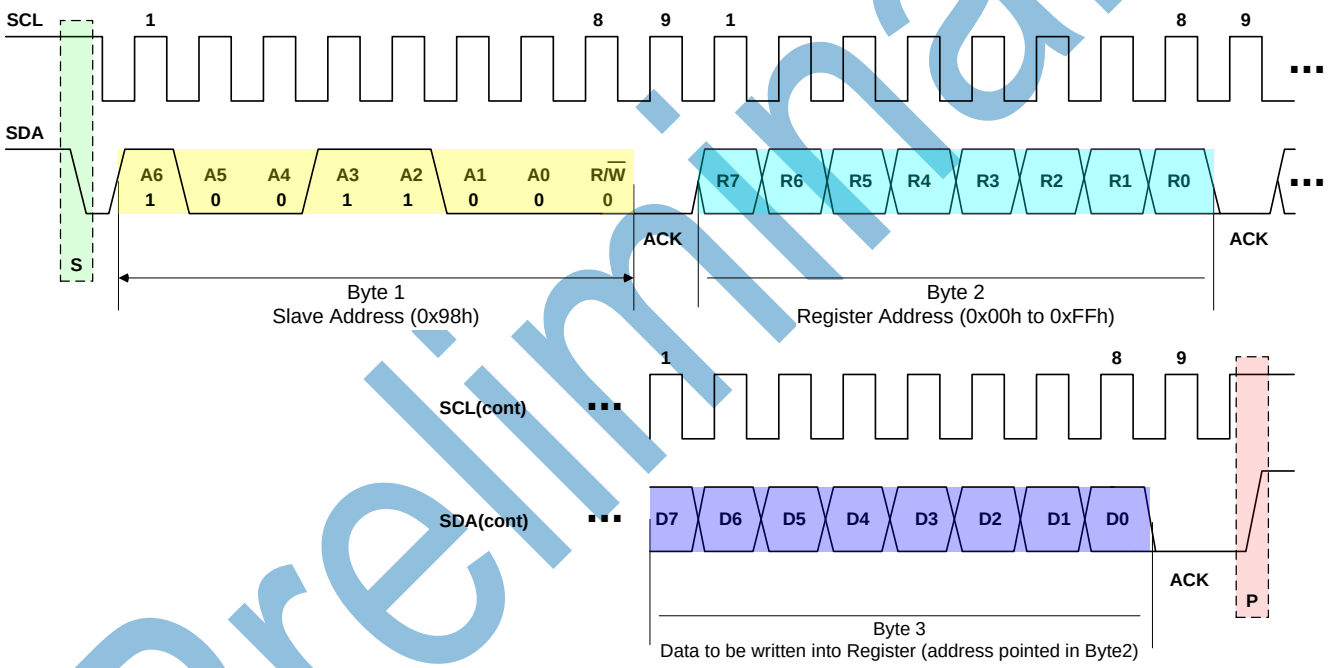


Figure 4. SMBus Write Timing Diagram

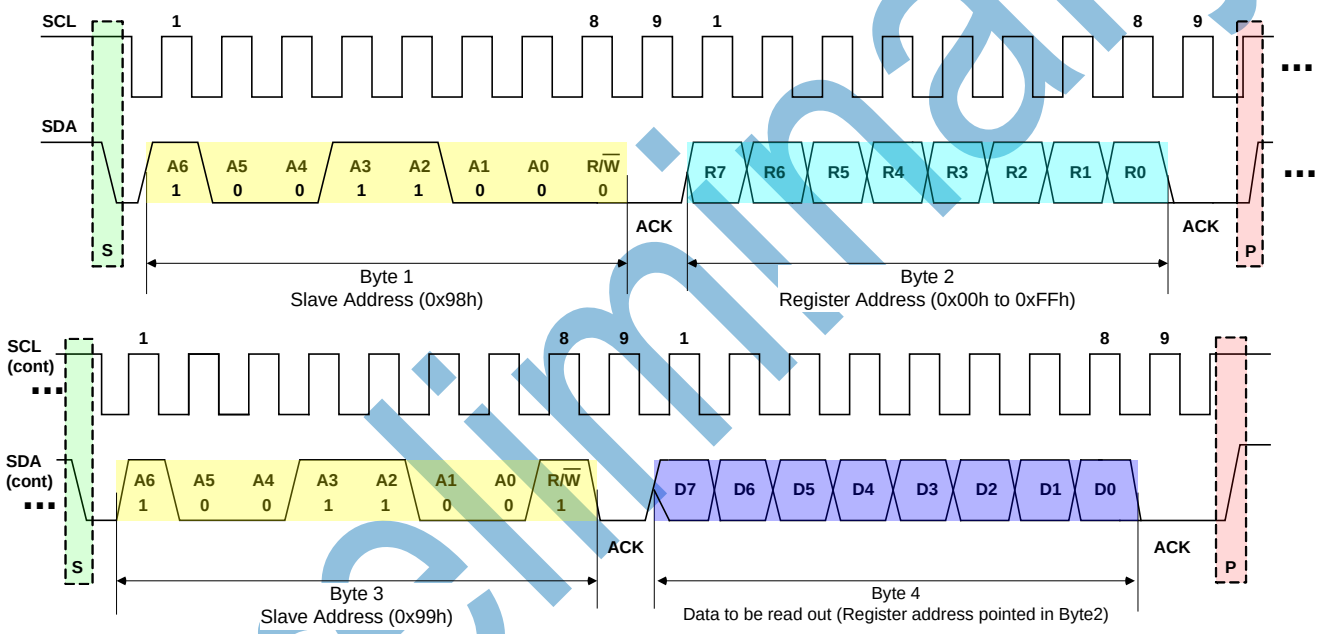


Figure 5. SMBus Read Timing Diagram

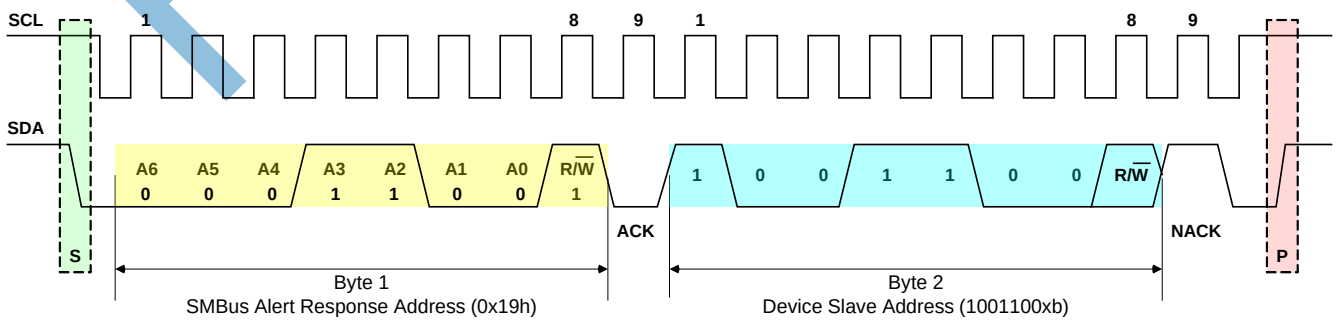


Figure 6. SMBus ALERT Response Diagram

1 Function Descriptions

The chip integrates 7 channel analog input, 2 channel fan speed monitor, a local temperature sensor, multi interrupt input and output and SMBus/I^{2}C digital interface with programmable slave address. Besides temperature sensing directly by local temperature sensor, it can continuously monitor power supply voltage, analog output temperature sensor (like CT7035), interrupt alarm input caused by digital temperature sensor over/under threshold temperature (like CT75). Also it can output interrupt alarm once any of above monitor event happens. It is a thermal monitor solution chip in system level.

1.1 Start Monitoring Procedure

To start the chip monitoring functions (local temperature, analog inputs, and fan speeds), user just write '1' to Start bit (bit 0) and '0' to INT_Clear bit (bit 3) of the Configuration Register (Reg Add 0x00). The chip then performs continuous monitoring of all temperature, analog inputs, and fan speeds. The sequence of items that are monitored of each cycle corresponds to locations in the registers respectively (Reg Add: 0x20 to 0x29):

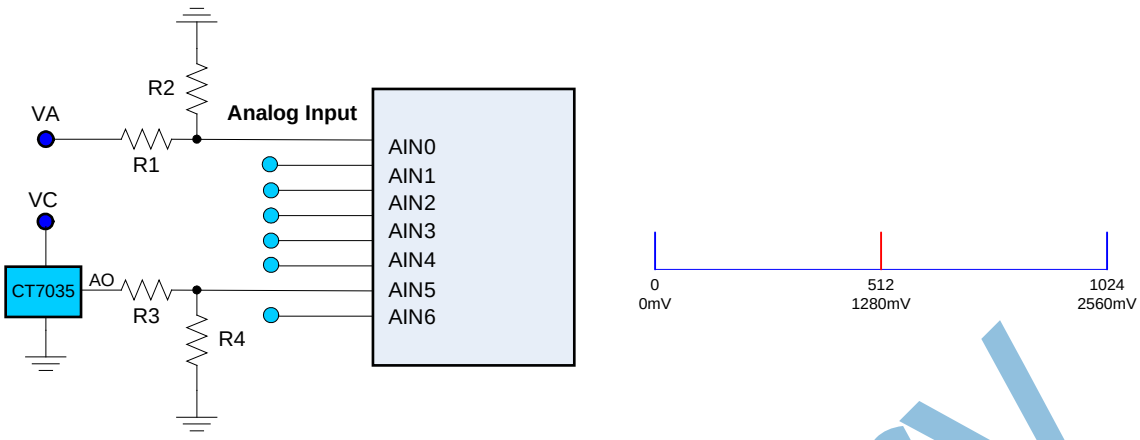
1) AIN0, Register Add, 0x20, 10-bit;
2) AIN1, Register Add, 0x21, 10-bit;
3) AIN2, Register Add, 0x22, 10-bit;
4) AIN3, Register Add, 0x23, 10-bit;
5) AIN4, Register Add, 0x24, 10-bit;
6) AIN5, Register Add, 0x25, 10-bit;
7) AIN6, Register Add, 0x26, 10-bit;
8) Local Temperature, Register Add, 0x27, 8, 9 or 12-bit;
9) FAN1 tachometer, Register Add, 0x28, 8-bit counter;
10) FAN2 tachometer, Register Add, 0x29, 8-bit counter;

The monitoring results are stored in the registers at listed above addresses. These conversion results can be read at any time and correspond to the result of the last conversion. A typical sequence of events after the chip power-on is as follows:

1. Setup proper alarm limitation
2. Setup proper interrupt
3. Start the chip monitoring

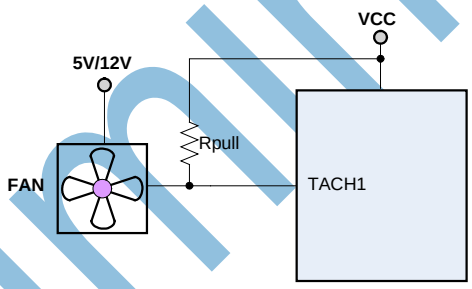
1.2 7 Channel Analog Inputs (AIN0-AIN6)

The chip continuously monitors external analog input, which could be different power supply voltage, analog output temperature sensor, like CT7035 using A-D converter with 10-bit. The voltage input range is 0 to 2.56V with 2.5mV resolution. Analog inputs can monitor external power supply voltage even voltage exceeds 0V to 2.56V, like 2.8V, 3.3V, 5V or negative voltage, -5V or -12V, just using a simile voltage divider formed by 2 resistors (R1, R2). To make sure the voltage forced at AIN0 to AIN6 pin is within the range of 0V to 2.56V. Likewise, if connecting external analog output temperature sensor, it is better to use voltage divider (R3, R4) to make sure the voltage forced AIN0-6 pin is within 0-2.56V under the full temperature, like -40^{o}C to 125^{o}C.



1.3 2 Channel Fan Speed Monitor (TACH1, TACH2)

The chip has 2 channel inputs (TACH1, TACH2) to connect fan tachometer output for monitoring fan speed. In general, tachometer signal is open drain output structure; connecting to TACH1/2 pin directly is ok if pull-up resistor connects to VCC of the chip. However if connecting to 12V or other higher voltage exceeds VCC range, 5.5V, using resistive divider (eg. R5 = 20k, R6 = 10k) or zener diode (Z1, 5.0V) to clamp the voltage is necessary. If fan has strong pull-up resistor, serial resistor (R7) is necessary to add shown as below figure.



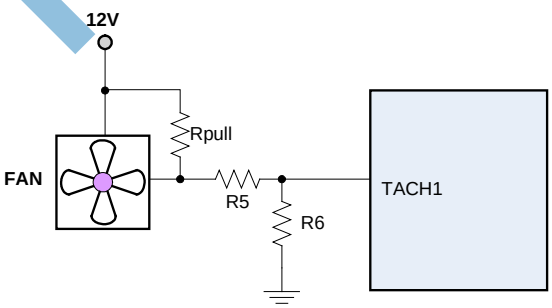
The chip builds in 22.5 kHz oscillator to sampling one period fan tachometer signal and converter into digital count. The count is 8-bit with Max. 255. The default divisor is set as 2, (selectable 1, 2, 4, or 8) which will generate 153 in decimal in count (Reg Add: 0x28 or 0x29) for 4400 RPM fan speed with 2 pulses per revolution. RPM can be calculated by below formulation.

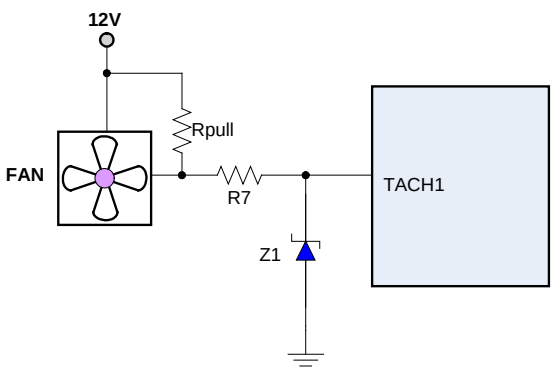
$$RPM = \frac{1.35 \times 10^6}{\text{Count} \times \text{Divisor}}$$

RPM, means fan speed, revolution per minutes;

Count, register data in decimal;

Divisor, setup by register at Reg Add 0x05. set as '1', means 1 pulse per revolution, or pole number inside the fan.





Fan Speed Limit Value

In general fans will not over speed if run from the correct voltage, so the failure condition of interest is under speed due to electrical or mechanical failure. For this reason only low-speed limits are programmed into the limit registers for the fans. The bigger the count number, the lower the fan speed based on above formulation. It should be noted that, since fan period rather than speed is being measured, a fan failure interrupt will occur when the measurement exceeds the limit value, setup in register, Reg Add 0x3C, 0x3D.

1.4 Local Temperature Sensor

The local temperature measurement data is in the local temperature register (read only attribution, Reg Add, 0x27h). Local temperature data is stored in 8, 9 or 12-bit twos binary complement format. For 9 or 12 bit format, the temperature data is composed by 2 bytes, MSB plus LSB, which can be get in same time using I^2C 2 bytes reading. The 1st byte is eight most significant bits [MSB] plus least significant bits [LSB]. For 8-bit format, the data range is from 0x00 to 0xFF, which means the expressed temperature range is from -128°C to 127°C with 1°C LSB. For 9-bit format, the data range is from 0x000 to 0x1FF, which means the expressed temperature range is from -128°C to 127.5°C with 0.5°C LSB. For 12-bit format, the data range is from 0x000 to 0x7FF, which means the expressed temperature range is from -128°C to 127.9375°C with 0.0625°C LSB. And the detail data format is shown as below tables.

Table 1. Temperature Data formed by 1-byte or 2-byte reading

Data Format	1-byte reading		2-byte reading	
	MSB	LSB	MSB	LSB
8-bit	Reg Add 0x27h	N/A	Reg Add 0x27h	N/A
9-bit	Reg Add 0x27h	Reg Add 0x06, bit7	Reg Add 0x27h, 1st byte	Reg Add 0x27h, 2nd byte
12-bit	Reg Add 0x27h	Reg Add 0x06, bit7-bit4	Reg Add 0x27h, 1st byte	Reg Add 0x27h, 2nd byte

Table 2. Temperature Data in 8-bit Digital Format

Measured Temperature (°C)	8-bit Digital Output (HEX)	8-bit Digital Output (BIN) (MSB)	8-bit Digital Output (BIN) (LSB)
+127	0x7F	0 1 1 1 ,1 1 1 1	0 0 0 0 ,0 0 0 0
+125	0x7D	0 1 1 1, 1 1 0 1	0 0 0 0 ,0 0 0 0
+25	0x19	0 0 0 1, 1 0 0 1	0 0 0 0 ,0 0 0 0
+1	0x01	0 0 0 0, 0 0 0 1	0 0 0 0 ,0 0 0 0
0	0x00	0 0 0 0, 0 0 0 0	0 0 0 0 ,0 0 0 0
-1	0xFF	1 1 1 1, 1 1 1 1	0 0 0 0 ,0 0 0 0
-25	0xE7	1 1 1 0, 0 1 1 1	0 0 0 0 ,0 0 0 0
-40	0xD8	1 1 0 1, 1 0 0 0	0 0 0 0 ,0 0 0 0

Table 3. Temperature Data in 9-bit Digital Format (2-bytes)

Measured Temperature (°C)	9-bit Digital Output (HEX)	9-bit Digital Output (BIN) (MSB)	9-bit Digital Output (BIN) (LSB)
+127.5	0x7F8	0 1 1 1 ,1 1 1 1	1 0 0 0 ,0 0 0 0
+125	0x7D0	0 1 1 1, 1 1 0 1	0 0 0 0 ,0 0 0 0
+25	0x190	0 0 0 1, 1 0 0 1	0 0 0 0 ,0 0 0 0
+0.5	0x008	0 0 0 0, 0 0 0 0	1 0 0 0 ,0 0 0 0
0.0	0x000	0 0 0 0, 0 0 0 0	0 0 0 0 ,0 0 0 0
-0.5	0xFF8	1 1 1 1, 1 1 1 1	1 0 0 0 ,0 0 0 0
-25	0xE70	1 1 1 0, 0 1 1 1	0 0 0 0 ,0 0 0 0
-40	0xD80	1 1 0 1, 1 0 0 0	0 0 0 0 ,0 0 0 0

Table 4 Temperature Data in 12-bit Digital Format (2-bytes)

Measured Temperature (°C)	12-bit Digital Output (HEX)	12-bit Digital Output (BIN) (MSB)	12-bit Digital Output (BIN) (LSB)
+127.9375	0x7FF	0 1 1 1 ,1 1 1 1	1 1 1 1 ,0 0 0 0
+125	0x7D0	0 1 1 1, 1 1 0 1	0 0 0 0 ,0 0 0 0
+25	0x190	0 0 0 1, 1 0 0 1	0 0 0 0 ,0 0 0 0
+0.0625	0x001	0 0 0 0, 0 0 0 0	0 0 0 1 ,0 0 0 0
0.0	0x000	0 0 0 0, 0 0 0 0	0 0 0 0 ,0 0 0 0
-0.0625	0xFFF	1 1 1 1, 1 1 1 1	1 1 1 1 ,0 0 0 0
-25	0xE70	1 1 1 0, 0 1 1 1	0 0 0 0 ,0 0 0 0
-40	0xD80	1 1 0 1, 1 0 0 0	0 0 0 0 ,0 0 0 0

Temperature Limit & Interrupt

When measuremed temperature is equal or higher than setup in temperature limit register, Thermal Alarm interrupt happens. There are four register limits for the temperature reading that affect the INT_O and THERM outputs of the CT80. These are the high temperature limit (HTL, Reg Add, 0x38), high temperature hysteresis (HT_HYS, Reg Add, 0x39), thermal temperature limit (THERM_LIMIT, Reg Add, 0x3A) and thermal temperature hysteresis (THERM_HYST, Reg Add 0x3B). There are three kinds of interrupt modes for selection: Continuous Interrupt, One-Time Interrupt and Comparator Interrupt. The THERM output of the chip can be programmed as One-Time Interrupt mode or Comparator mode. INT_O can be programmed as Continuous Interrupt mode or One-Time Interrupt mode. These modes and trigger/release conditions are explained in the following sections:

1). Continuous Interrupt Mode,

Setting bit6 of Interrupt Setup Register (Reg Add 0x04) as '0' (default) will setup the chip as continuous interrupt mode. In this mode, INT_O pin will be active and keep this situation once trigger events happen until release events happen. The trigger condition is the measurement temperature each time exceeds setup in HTL register (Reg Add, 0x38). The release condition of this interrupt is reading Interrupt Status Register (Reg Add, 0x01) or clearing INT_Clear bit of Configuration Register (bit3, Reg Add, 0x00). In this mode, the chip could be trigged again in next time temperature measurement if trigger condition happens, and it will be reset again after release condition happens until the temperature falls below setup in HT_HYS register (Reg Add, 0x39), meantime the interrupt will be reset automatically.

2). One-time Interrupt Mode

Setting bit6 of Interrupt Setup Register (Reg Add 0x04) as '1' will setup the chip as one-time interrupt mode. In this mode, INT_O pin will be active and keep this situation once trigger events happen until release events happen. The trigger condition is the measurement temperature 1st time exceeds setup in HTL register (Reg Add, 0x38). The release condition of this interrupt is reading Interrupt Status Register (Reg Add, 0x01) or clearing INT_Clear bit of Configuration Register (bit3, Reg Add, 0x00). In this mode, the chip will be trigged only one time if trigger condition happens, and it will be reset after release condition happens until the temperature falls below setup in HT_HYS register (Reg Add, 0x39).

Setting bit7 of Interrupt Setup Register (Reg Add 0x04) as '1' will setup the chip as one-time interrupt mode. In this mode, THERM pin will be active and keep this situation once trigger events happen until release events happen. The trigger condition is the measurement temperature 1st time exceeds setup in THERM_LIMIT (Reg Add, 0x3A). The release condition of this interrupt is reading Interrupt Status Register (Reg Add, 0x01) or clearing INT_Clear bit of Configuration Register (bit3, Reg Add, 0x00). In this mode, the chip will be trigged only one time if trigger condition happens, and it will be reset after release condition happens until the temperature

falls below setup in THERM_HYST (Reg Add 0x3B).

3). Comparator mode

Setting bit2 of THERM/Temp Config Register (Reg Add 0x06) as '0' (default) will setup the chip as comparator interrupt mode. In this mode, THERM pin will be active (kept low) and keep this situation once trigger events happen until release events happen. The trigger condition is the measurement temperature exceeds setup in THERM_LIMIT (Reg Add, 0x3A). The release condition of this interrupt is the measurement temperature falls below setup in THERM_HYST (Reg Add, 0x3B). THERM pin will get high once release condition happens.

Table 5 Interrupt Mode Selection

Interrupt Output PIN	Interrupt Mode	
INT_O (PIN10)	Continuous Interrupt mode Set bit6 of Interrupt Setup Register, (Reg Add 0x04) as '0'. default is 0.	One-Time Interrupt mode Set bit6 of Interrupt Setup Register, (Reg Add 0x04) as '1'
THERM (PIN13)	Comparator mode Set bit7 of Interrupt Setup Register, (Reg Add 0x04) as '0'. default is 0.	One-Time Interrupt mode Set bit7 of Interrupt Setup Register, (Reg Add 0x04) as '1'

1.5 Interrupt Input

Also the chip can monitor 3 external interrupt inputs.

1) INT_IN (pin1), this pin is an active low interrupt input that provides a way to connect an INT from other devices through the chip to the host/processor. If this pin is pulled low, then bit 7 of Interrupt Status Register 1 (Reg Add, 0x01) gets '1', indicating this interrupt detection. Setting bit 1 of the Configuration Register (Reg Add 0x00) as '1' also allows the INT_O pin to go low when INT_IN goes low. To disable this feature, set bit 7 of Interrupt Mask Register 1 (address 03h) as '1' to high.

2) BTI (pin6), Board Temperature Interrupt, this pin is an active low interrupt input recommended to come from the over/under temperature alert (ALERT) output of CT75 temperature sensors. The CT75 alert output activates when its temperature exceeds the programmed threshold. If the temperature of any CT75 exceeds its programmed limit, BTI pin is driven low. This action generates an interrupt at bit 1 of Interrupt Status Register 2 (Reg Add, 0x02) that notifies the host of a possible over temperature condition. To disable this feature, set bit 1 of Interrupt Mask Register 2 (Reg Add, 0x04) to '1'. This pin also provides an internal, 10 kohm pull-up resistor.

3) GPI (pin7), this pin is an active high interrupt input from the device or circuit that detects and latches the external signal. This action could be accomplished mechanically, optically, or electrically; circuitry external to the chip is expected to latch the event. Read this interrupt using bit 4 of Interrupt Status Register 2 (Reg Add, 0x02), and disable it using bit 4 of Interrupt Mask Register 2 (Reg Add, 0x04). The design of the chip allows this input to go high even with no power applied, and no clamping or other interference with the line occurs. This line can also be pulled low by the chip for at least 10ms to reset a typical circuit. Accomplish this reset by setting bit 5 of the Configuration Register (Reg Add, 0x00) to '1'; this bit is self-clearing.

1.6 Interrupt Output

The chip has 2 interrupt outputs which could come from the below sources.

1) INT_O (pin10), this pin gets active once INT_IN, BTI, or GPI pin has active interrupt input. INT_O is enabled when bit 1 of the Configuration Register (Reg Add 0x00) is set '1'. Bits 2 and 3 of the Configuration Register (Reg Add 0x00) are also used to set the polarity and state of the INT_O interrupt line.
2) THERM (pin13), bit 6 (THERM Pin Enable) of the Fan Divisor Setup Register (Reg Add, 0x05), has to be set '1' and bit 7 (RST_O Enable) has to be set '0' in order to enable the THERM alarm function on the this pin. This pin has two modes of operation: One-Time Interrupt and Comparator. One-Time Interrupt mode is selected by taking bit 2 of the THERM Configuration/Temperature Resolution Register (Reg Add, 0x06) '1'. If bit 2 is set '0', then Comparator mode is selected. Unlike the THERM pin, the THERM bit in Interrupt Status Register 2 (Reg Add, 0x02, bit 5) functions in Continuous Interrupt and One-Time Interrupt modes. The THERM bit can be masked to the INT_O pin by setting bit 5 in Interrupt Mask Register 2 (Reg Add, 0x04) '0'.

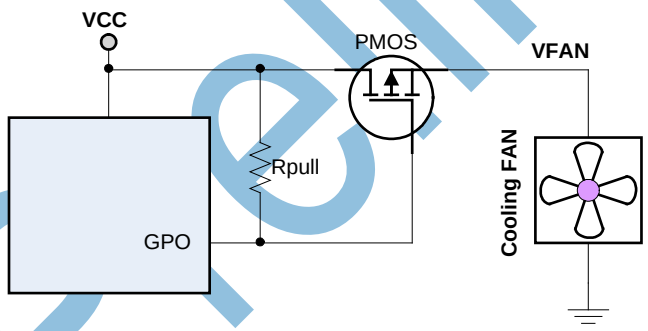
1.7 Interrupt Clear

User can get the interrupt contents and resets the Interrupt Status Registers (Reg Add, 0x01 and 0x02) and the INT_O pin by reading this register. The INT_O pin can also be cleared by the INT_Clear bit (Reg Add, 0x00, bit 3) without affecting the contents of the Interrupt Status Registers. When this bit is '1', the chip stops monitoring loop, and the monitoring action resumes when this bit is '0'.

1.8 General Digital Logic Input & Output

The chip has 1 general digital logic output pin and 1 logic input pin as below.

1) GPO (pin11), this pin is a general digital logic output pin with active low and open drain structure. It needs an external pull up resistor to VCC. Output logic status of this pin can be set by setting bit 6 (GPO bit) of the configuration register (Reg Add, 0x00). This pin can be used in software power control by activating an external power control MOSFET shown as below.



Bit 6	GPO pin
0	High
1	Low

2) NT_IN/RST_IN (pin12), this pin can be used as reset signal input to reset all registers as default data of the chip just forcing this pin as low with 100us time at least. Generally this pin is used for ATE.

1.9 Register Map

All registers are shown as below table.

Table 6. Register Map

Register Address	Register Name	Attribution	Default Data	BIT							
				7	6	5	4	3	2	1	0
0x00	Configuration	R/W	0x08	INIT	GPO_EN	GPI_Set	RESET	INT_C	INT_P	INT_EN	START
0x01	Interrupt Status 1	R/O	0x00	INT_IN	AIN6	AIN5	AIN4	AIN3	AIN2	AIN1	AIN0
0x02	Interrupt Status 2	R/O	0x00	Reserved	Reserved	THERM_S	GPI_S	TACH2_S	TACH1_S	BTI_S	ALT_S
0x03	Interrupt Setup 1	R/W	0x00	INT_IN_EN	AIN6_EN	AIN5_EN	AIN4_EN	AIN3_EN	AIN2_EN	AIN1_EN	AIN0_EN
0x04	Interrupt Setup 2	R/W	0x00	THERM_MS	ALT_MS	THERM_EN	GPI_EN	TACH2_EN	TACH1_EN	BTI_EN	ALT_EN
0x05	Fan/THERM Setup	R/W	0x14	RST_O	THERM_O	TACH2_Divisor[1:0]		TACH1_Divisor[1:0]		TACH2_MS	TACH1_MS
0x06	THERM/Temp Config	R/W	0x01	T3	T2	T1	T0	TEMP_RS	THERM_PIN_MS	THERM_PIN_POL	THERM_PIN_S
0x07	Conv_Rate 1	R/W	0x00	CR	Reserved						
0x08	Channel Select	R/W	0x00	TEMP_S	AIN6_S	AIN5_S	AIN4_S	AIN3_S	AIN2_S	AIN1_S	AIN0_S
0x09	CR/Input Config	R/W	0x00	CR1	CR0	AIN45_P	AIN45	AIN23_P	AIN23	AIN01_P	AIN01
0x20	AIN0 Voltage	R/O	0x0000	AIN0[9:0]							
0x21	AIN1 Voltage	R/O	0x0000	AIN1[9:0]							
0x22	AIN2 Voltage	R/O	0x0000	AIN2[9:0]							
0x23	AIN3 Voltage	R/O	0x0000	AIN3[9:0]							
0x24	AIN4 Voltage	R/O	0x0000	AIN4[9:0]							
0x25	AIN5 Voltage	R/O	0x0000	AIN5[9:0]							
0x26	AIN6 Voltage	R/O	0x0000	AIN6[9:0]							
0x27	TEMP_Data	R/O	0x00	T11	T10	T9	T8	T7	T6	T5	T4
0x28	FAN1_Tach	R/O	0x00	FAN1_TACH[7:0]							
0x29	FAN2_Tach	R/O	0x00	FAN1_TACH[7:0]							
0x2A	AIN0_High_Limit	R/W	0x00	AIN0_HL[7:0]							
0x2B	AIN0_Low_Limit	R/W	0x00	AIN0_LL[7:0]							
0x2C	AIN1_High_Limit	R/W	0x00	AIN1_HL[7:0]							
0x2D	AIN1_Low_Limit	R/W	0x00	AIN1_LL[7:0]							
0x2E	AIN2_High_Limit	R/W	0x00	AIN2_HL[7:0]							
0x2F	AIN2_Low_Limit	R/W	0x00	AIN2_LL[7:0]							
0x30	AIN3_High_Limit	R/W	0x00	AIN3_HL[7:0]							
0x31	AIN3_Low_Limit	R/W	0x55	AIN3_LL[7:0]							
0x32	AIN4_High_Limit	R/W	0x00	AIN4_HL[7:0]							
0x33	AIN4_Low_Limit	R/W	0x00	AIN4_LL[7:0]							
0x34	AIN5_High_Limit	R/W	0x00	AIN5_HL[7:0]							
0x35	AIN5_Low_Limit	R/W	0x00	AIN5_LL[7:0]							
0x36	AIN6_High_Limit	R/W	0x00	AIN6_HL[7:0]							
0x37	AIN6_Low_Limit	R/W	0x00	AIN6_LL[7:0]							
0x38	High_Temp_Limit	R/W	0x00	HTL[7:0]							
0x39	High_Temp_HYS	R/W	0x00	HTL_HYS[7:0]							
0x3A	THERM_Temp_Limit	R/W	0x00	THERM_HTL[7:0]							
0x3B	THERM_Temp_HYS	R/W	0x00	THERM_HYS[7:0]							
0x3C	FAN1_COUNT_Limit	R/W	0x00	FAN1_COUNT[7:0]							
0x3D	FAN2_COUNT_Limit	R/W	0x00	FAN2_COUNT[7:0]							
0x3E	Manufacture ID	R/O	0x00	0x59							
0x3F	Device ID	R/O	0x00	0x80							

1.10 Register Description

1.10.1 Configuration

Register Address: 0x00

Register Attribution: Read / Write

Default Data: 0x08 after POR

BIT	7	6	5	4	3	2	1	0
Definition	INIT	GPO_EN	GPI_Set	RESET	INT_C	INT_P	INT_EN	START
Default	0	0	0	0	1	0	0	0

BIT	Name	Description
7	INIT	0 -- (default) 1 -- to reset all registers into their default data, including this bit itself.
6	GPO_EN	0 -- (default) 1 -- to set GPO (pin11) active low.
5	GPI_Set	0 -- (default) 1 -- to clear GPI (pin7), also this bit will be clear after 10ms.
4	RESET	0 -- (default) 1 -- to set RST_O (pin13) output low pulse with 10ms duration time at least. If bits 7 and 6 of Fan/THERM Setup register (Reg Add 0x05) are set as 1 and 0 respectively, then this bit is cleared once the pulse is inactive.
3	INT_C	0 -- to enable INT_O (pin10) output 1 -- (default), to disables the INT_O (pin10) output. This does not affect the Interrupt Status Registers and the device will stop monitoring temperature and voltage. Monitoring will resume upon the clearing of this bit.
2	INT_P	0 -- (default), to select active low output for INT_O (pin10); 1 -- to selects active high output for INT_O (pin10).
1	INT_EN	0 -- (default), to disable INT_O (pin10) output; 1 -- to enable INT_O (pin10) output.
0	START	0 -- (default), to disable all monitoring, and set the chip in shutdown mode; 1 -- to start the monitoring of temperature, input voltage and fan speed.

1.10.2 Interrupt Status 1

Register Address: 0x01

Register Attribution: Read only

Default Data: 0x00 after POR

BIT	7	6	5	4	3	2	1	0
Definition	INIT_IN	AIN6	AIN5	AIN4	AIN3	AIN2	AIN1	AIN0
Default	0	0	0	0	0	0	0	0

BIT	Name	Description
7	INIT_IN	0 -- (default) 1 -- to detect active low input at INT_IN (pin1).
6	AIN6	0 -- (default) 1 -- to detect the event of exceeding high or low limit happens at AIN6 (pin15).
5	AIN5	0 -- (default) 1 -- to detect the event of exceeding high or low limit happens at AIN5 (pin16).
4	AIN4	0 -- (default) 1 -- to detect the event of exceeding high or low limit happens at AIN4 (pin17).
3	AIN3	0 -- (default) 1 -- to detect the event of exceeding high or low limit happens at AIN3 (pin18).
2	AIN2	0 -- (default) 1 -- to detect the event of exceeding high or low limit happens at AIN2 (pin19).
1	AIN1	0 -- (default) 1 -- to detect the event of exceeding high or low limit happens at AIN1 (pin20).
0	AIN0	0 -- (default) 1 -- to detect the event of exceeding high or low limit happens at AIN0 (pin21).

1.10.3 Interrupt Status 2

Register Address: 0x02

Register Attribution: Read Only

Default Data: 0x00 after POR

BIT	7	6	5	4	3	2	1	0
Definition	Reserved	Reserved	THERM_S	GPI_S	TACH2_S	TACH1_S	BTI_S	ALT_S
Default	0	0	0	0	0	0	0	0

BIT	Name	Description
7, 6	Reserved	These 2 bits are reserved for future usage.
5	THERM_S	This bit indicates thermal status. 0 -- (default) 1 -- to indicate measurement temperature exceeds high or low limit setup in THERM or THERM_HYS register (Reg Add, 0x3A and 0x3B). Both continuous interrupt mode and one-time interrupt mode are supported, and mode can be selected by set bit7 of Interrupt Setup Register (Reg Add, 0x04).
4	GPI_S	This bit indicates GPI pin (pin7) status. 0 -- (default) 1 -- to indicate GPI pin (pin7) gets high.
3	TACH2_S	This bit indicates fan2 speed status. 0 -- (default) 1 -- to indicate fan2 speed count exceeds limit setup in FAN2_COUNT_LIMIT (Reg Add, 0x3D), which means fan2 speed is lower than that of setup data.
2	TACH1_S	This bit indicates fan1 speed status. 0 -- (default) 1 -- to indicate fan1 speed count exceeds limit setup in FAN1_COUNT_LIMIT (Reg Add, 0x3C), which means fan1 speed is lower than that of setup data.
1	BTI_S	This bit indicates BTI pin (pin6) status. 0 -- (default) 1 -- to detect the interrupt event happens at BTI pin (pin6).
0	ALT_S	This bit indicates over temperature alert status. 0 -- (default) 1 -- to indicate measurement temperature exceeds high or low limit setup in HTL or HTL_HYS register (Reg Add, 0x38 and 0x39). Both continuous interrupt mode and one-time interrupt mode are supported, and mode can be selected by set bit6 of Interrupt Setup Register (Reg Add, 0x04)..

1.10.4 Interrupt Setup Register 1

Register Address: 0x03

Attribution: Read/Write

Default Data: 0x00 after POR

BIT	7	6	5	4	3	2	1	0
Name	INT_IN_EN	AIN6_EN	AIN5_EN	AIN4_EN	AIN3_EN	AIN2_EN	AIN1_EN	AIN0_EN
Default	0	0	0	0	0	0	0	0

BIT	Name	Description
7	INT_IN_EN	0 -- (default) enable bit7 function of Interrupt Status Register 1 (Reg Add, 0x01); 1 -- disable bit7 function of Interrupt Status Register 1 (Reg Add, 0x01).
6	AIN6_EN	0 -- (default) enable bit6 function of Interrupt Status Register 1 (Reg Add, 0x01); 1 -- disable bit6 function of Interrupt Status Register 1 (Reg Add, 0x01).
5	AIN5_EN	0 -- (default) enable bit5 function of Interrupt Status Register 1 (Reg Add, 0x01); 1 -- disable bit5 function of Interrupt Status Register 1 (Reg Add, 0x01).
4	AIN4_EN	0 -- (default) enable bit4 function of Interrupt Status Register 1 (Reg Add, 0x01); 1 -- disable bit4 function of Interrupt Status Register 1 (Reg Add, 0x01).
3	AIN3_EN	0 -- (default) enable bit3 function of Interrupt Status Register 1 (Reg Add, 0x01); 1 -- disable bit3 function of Interrupt Status Register 1 (Reg Add, 0x01).
2	AIN2_EN	0 -- (default) enable bit2 function of Interrupt Status Register 1 (Reg Add, 0x01); 1 -- disable bit2 function of Interrupt Status Register 1 (Reg Add, 0x01).
1	AIN1_EN	0 -- (default) enable bit1 function of Interrupt Status Register 1 (Reg Add, 0x01); 1 -- disable bit1 function of Interrupt Status Register 1 (Reg Add, 0x01).
0	AIN0_EN	0 -- (default) enable bit0 function of Interrupt Status Register 1 (Reg Add, 0x01); 1 -- disable bit0 function of Interrupt Status Register 1 (Reg Add, 0x01).

1.10.5 Interrupt Setup Register 2

Register Address: 0x04

Attribution: Read/Write

Default Data: 0x00 after POR

BIT	7	6	5	4	3	2	1	0
Name	THERM_MS	ALT_MS	THERM_EN	GPI_EN	TACH2_EN	TACH1_EN	BTI_EN	ALT_EN
Default	0	0	0	0	0	0	0	0

BIT	Name	Description
7	THERM_MS	THERM interrupt mode select bit. 0 -- (default) select continuous interrupt mode; 1 -- select one time interrupt mode.
6	ALT_MS	ALERT interrupt mode select bit. 0 -- (default) select continuous interrupt mode; 1 -- select one time interrupt mode.
5	THERM_EN	0 -- (default) enable bit5 function of Interrupt Status Register 2 (Reg Add, 0x02); 1 -- disable bit5 to function of Interrupt Status Register 2 (Reg Add, 0x02).
4	GPI_EN	0 -- (default) enable bit4 function of Interrupt Status Register 2 (Reg Add, 0x02); 1 -- disable bit4 function of Interrupt Status Register 2 (Reg Add, 0x02).
3	TACH2_EN	0 -- (default) enable bit3 function of Interrupt Status Register 2 (Reg Add, 0x02); 1 -- disable bit3 function of Interrupt Status Register 2 (Reg Add, 0x02).
2	TACH1_EN	0 -- (default) enable bit2 function of Interrupt Status Register 2 (Reg Add, 0x02); 1 -- disable bit2 function of Interrupt Status Register 2 (Reg Add, 0x02).
1	BTI_EN	0 -- (default) enable bit1 function of Interrupt Status Register 2 (Reg Add, 0x02); 1 -- disable bit1 function of Interrupt Status Register 2 (Reg Add, 0x02).
0	ALT_EN	0 -- (default) enable bit0 function of Interrupt Status Register 2 (Reg Add, 0x02); 1 -- disable bit0 function of Interrupt Status Register 2 (Reg Add, 0x02).

1.10.6 FAN/THERM Setup Register

Register Address: 0x05

Attribution: Read/Write

Default Data: 0x14 after POR.

BIT	7	6	5	4	3	2	1	0
Name	RST_O	THERM_O	TACH2_Divisor[1:0]		TACH2_Divisor[1:0]		TACH2_MS	TACH1_MS
Default	0	0	0	1	0	1	0	0

BIT	Name	Description
7	RST_O	PIN13 function select bit. 0 -- (default); 1 -- select this pin as RST_O function mode. Once set this pin as RST_O, bit6 has to be set '0'. If both bit7 and bit6 are set as '0', PIN13 output function is disabled.
6	THERM_O	PIN13 function select bit. 0 -- (default); 1 -- select this pin as THERM_O function mode. Once set this pin as THERM_O, bit7 has to be set '0'. If both bit7 and bit6 are set as '0', PIN13 output function is disabled..
5,4	TACH2_Divisor[1:0]	Fan2 speed setup 00 -- divisor =1; 01 -- divisor =2; (default) 10 -- divisor =4; 11 -- divisor =8; If level sensitive input is selected, bit[4] = 1 will setup active-low input mode (An interrupt will be generated if the TACH2 input is Low); bit[4] = 0 will setup active-high input (an interrupt will be generated if the TACH2 input is High).
3,2	TACH1_Divisor[1:0]	Fan1 speed setup 00 -- divisor =1; 01 -- divisor =2; (default) 10 -- divisor =4; 11 -- divisor =8; If level sensitive input is selected, bit[2] = 1 will setup active-low input mode (An interrupt will be generated if the TACH1 input is Low); bit[2] = 0 will setup active-high input (an interrupt will be generated if the TACH1 input is High).
1	TACH2_MS	TACH2 input mode selection bit 0 -- select tach count mode for TACH2 input pin; 1 -- select level sensitive mode for TACH2 input pin;
0	TACH1_MS	TACH1 input mode selection bit 0 -- select tach count mode for TACH1 input pin; 1 -- select level sensitive mode for TACH1 input pin;

1.10.7 THERM/TEMP_Config

Register Address: 0x06

Attribution: Read / Write

Default Data: 0x01 after POR.

BIT	7	6	5	4	3	2	1	0
Name	T3	T2	T1	T0	TEMP_RS	THERM_PIN_MS	THERM_PIN_POL	THERM_PIN_S
Default	0	0	0	0	0	0	0	1

BIT	Name	Description
7,6,5,4	T[3:0]	Temperature LSB bits. If temperature resolution bit, bit3 (TEMP_RS) = 0, only bit7 is valid, plus MSB Temperature data, (Reg Add, 0x27) to combine complete temperature data with two's binary complement format. Bit7, T[3] -- 0.5 °C; TEMP_RS = 1, bit7 to bit4 are valid and used to expression 0.0625 °C resolution. Bit7, T[3] -- 0.5°C; Bit6, T[2] -- 0.25 °C; Bit5, T[1] -- 0.125 °C; Bit4, T[0] -- 0.0625 °C.
3	TEMP_RS	Temperature Resolution select bit. 0 -- (default) total 9 bits (plus signature) with 0.5oC resolution; 1 -- total 12 bits (plus signature) with 0.0625oC resolution.
2	THERM_PIN_MS	THERM PIN Mode Select 0 -- one-time interrupt mode; 1 -- continuous interrupt mode.
1	THERM_PIN_POL	THERM PIN Output Polarity Select 0 -- active low; 1 -- active high.
0	THERM_PIN_S	THERM PIN Status bit, this bit is read only bit to monitor PIN13 status when this is is used as THERM output function.

1.10.8 Conv_rate 1, conversion rate setup register 1

Register Address & Attribution: 0x07

Attribution: Read / Write

Default Data: 0x00 after POR.

BIT	7	6	5	4	3	2	1	0
Name	CR_MS	Reserved						
Default	0	0	0	0	0	0	0	0

CR bit, bit7 of this register, is used to setup conversion time mode:

0 -- to setup the chip working with every 600ms for one time monitoring cycle;

1 -- to setup the chip working with continuous monitoring working mode.

bit6 to bit0 are reserved with ready only attribution.

1.10.9 Channel Select

Register Address: 0x08

Attribution: Read / Write

Default Data: 0x00 after POR.

BIT	7	6	5	4	3	2	1	0
Name	TEMP_S	AIN6_S	AIN5_S	AIN4_S	AIN3_S	AIN2_S	AIN1_S	AIN0_S
Default	0	0	0	0	0	0	0	0

BIT	Name	Description
7	TEMP_S	Local Temperature Selection bit 0 -- (default), this channel is included in each monitoring cycle; 1 -- local temperature monitoring is skipped in each monitoring cycle. Temperature data will

		return 0 and this item will not generate interrupt anymore.
6	AIN6_S	Analog Input channel 6 selection bit. 0 -- (default), this channel is included in each monitoring cycle;; 1 -- Analog input channel 6 monitoring is skipped in each monitoring cycle. Value data will return 0 and this item will not generate interrupt anymore.
5	AIN5_S	Analog Input channel 5 selection bit. 0 -- (default), this channel is included in each monitoring cycle;; 1 -- Analog input channel 5 monitoring is skipped in each monitoring cycle. Value data will return 0 and this item will not generate interrupt anymore.
4	AIN4_S	Analog Input channel 4 selection bit. 0 -- (default), this channel is included in each monitoring cycle;; 1 -- Analog input channel 4 monitoring is skipped in each monitoring cycle. Value data will return 0 and this item will not generate interrupt anymore.
3	AIN3_S	Analog Input channel 3 selection bit. 0 -- (default), this channel is included in each monitoring cycle;; 1 -- Analog input channel 3 monitoring is skipped in each monitoring cycle. Value data will return 0 and this item will not generate interrupt anymore.
2	AIN2_S	Analog Input channel 2 selection bit. 0 -- (default), this channel is included in each monitoring cycle;; 1 -- Analog input channel 2 monitoring is skipped in each monitoring cycle. Value data will return 0 and this item will not generate interrupt anymore.
1	AIN1_S	Analog Input channel 1 selection bit. 0 -- (default), this channel is included in each monitoring cycle;; 1 -- Analog input channel 1 monitoring is skipped in each monitoring cycle. Value data will return 0 and this item will not generate interrupt anymore.
0	AIN0_S	Analog Input channel 0 selection bit. 0 -- (default), this channel is included in each monitoring cycle;; 1 -- Analog input channel 0 monitoring is skipped in each monitoring cycle. Value data will return 0 and this item will not generate interrupt anymore.

1.10.10 Conv_Rate/Input Config

Register Address: 0x09

Register Attribution: Read / Write

Default Data: 0x00 after POR

BIT	7	6	5	4	3	2	1	0
Name	CR1	CR0	AIN45_P	AIN45	AIN23_P	AIN23	AIN01_P	AIN01
Default	0	0	0	0	0	0	0	0

BIT	Name	Description
7,6	CR[1:0]	Conversion rate Selection bit 00 -- (default), 600ms in each monitoring cycle; 01 -- 300ms in each monitoring cycle; 10 -- 150ms in each monitoring cycle; 11 -- 75ms in each monitoring cycle;
5	AIN45_P	Analog Input channel 4 and channel 5 polarity when used as a differential input pair. 0 -- (default), AIN4 and AIN5 are configured differential pair with normal polarity; 1 -- AIN4 and AIN5 are configured differential pair with reverse polarity. Once bit4 (AIN45) is set as '0', this bit can be ignored.
4	AIN45	Analog Input channel 4 and channel 5 configuration bit. 0 -- (default), setup analog input channel 4 and 5 are single-ended mode independently; 1 -- setup channel 4 and channel 5 as a differential input pair.
3	AIN23_P	Analog Input channel 2 and channel 3 polarity when used as a differential input pair. 0 -- (default), AIN2 and AIN3 are configured differential pair with normal polarity; 1 -- AIN2 and AIN3 are configured differential pair with reverse polarity. Once bit2 (AIN23) is set as '0', this bit can be ignored.
2	AIN23	Analog Input channel 2 and channel 3 configuration bit. 0 -- (default), setup analog input channel 2 and 3 are single-ended mode independently; 1 -- setup channel 2 and channel 3 as a differential input pair.
1	AIN01_P	Analog Input channel 0 and channel 1 polarity when used as a differential input pair. 0 -- (default), AIN0 and AIN1 are configured differential pair with normal polarity; 1 -- AIN0 and AIN1 are configured differential pair with reverse polarity. Once bit0 (AIN01) is set as '0', this bit can be ignored.
0	AIN01	Analog Input channel 0 and channel 1 configuration bit. 0 -- (default), setup analog input channel 0 and 1 are single-ended mode independently; 1 -- setup channel 0 and channel 1 as a differential input pair.

1.10.11 AIN0 to AIN6 Voltage

Register Address: 0x20 to 0x26

Register Attribution: Read Only

Default Data: 0x0000 after POR

Since the input voltage is converted with 10-bit ADC, so it is necessary to use 2-byte reading operation. And the expression range is from 0 to 1024 in decimal, which is corresponding to voltage range from 0 to 2560mV.

	MSB (1st Byte)								LSB (2nd Byte)							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Number	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	0	0	0	0	0	0
Voltage(mV)	1280	640	320	160	80	40	20	10	5.0	2.5	0	0	0	0	0	0

Register Address	Name	Description
0x20	AIN0 Voltage	AIN0...6[9:0] Using 2-byte reading operation gets MSB plus LSB data in Hex. Then converter those into data in decimal format ($DATA_{DEC}$) based on above table. $Voltage = \frac{DATA_{DEC}}{1024} \times 2560\ (mV)$
0x21	AIN1 Voltage	
0x22	AIN2 Voltage	
0x23	AIN3 Voltage	
0x24	AIN4 Voltage	
0x25	AIN5 Voltage	
0x26	AIN6 Voltage	

1.10.12 TEMP_Data, Local Temperature Data

Register Address: 0x27

Register Attribution: Read Only

Default Data: 0x0000.

There were 2 kinds of resolution for selection 9-bit or 13-bit. Set TEMP_RS bit (bit3) of THERM/Temp register (Reg Add, 0x06) as '0', 9-bit format temperature data was selected; TEMP_RS = 1, 12-bit format data was selected.

For LSB data of local temperature, it could be from TEMP_Data register (Reg Add 0x27) via 2-byte reading operation, or from THERM/Temp Config register (Reg Add, 0x06). If LSB data is from THERM/Temp Config register, bit7 to bit4 is valid in 13-bit format, and only bit7 is valid in 9-bit format.

	MSB (1st Byte) [0x27]								LSB (2nd Byte) [0x27 or 0x06]							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
9-bit	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}							
12-bit	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}				
Deg C(°C)	S	64	32	16	8	4	2	1	0.5	0.25	0.125	0.0625				

1.10.13 FAN1, FAN2_Tach

Register Address: 0x28, 0x29

Register Attribution: Read Only

Default Data: 0x00 after POR.

These 2 bytes were stored FAN1 and FAN2 tachometer count number in 8-bit with the range of 0 to 255.

	MSB (1st Byte)							
BIT	7	6	5	4	3	2	1	0
Number	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
COUNT	128	64	32	16	8	4	2	1

Register Address	Name	Description
0x28	FAN1 Tachometer	Using 1-byte reading operation gets data in Hex, Then converter this into data in decimal format (COUNT) based on above table. $RPM = \frac{22.5 \times 10^3 \times 6}{COUNT \times Divisor}$ (revolution per minutes)
0x29	FAN1 Tachometer	

1.10.14 AIN0 to AIN6 High_Limit, AIN0 to AIN6 Low_Limit

Register Address: 0x2A to 0x37

Register Attribution: Read / Write

Default Data: 0x00 after POR.

	definition							
BIT	7	6	5	4	3	2	1	0
Number	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2
Voltage(mV)	1280	640	320	160	80	40	20	10

Register Address	Name	Description
0x2A	AIN0_High_Limit	These 6 registers are used to setup high limit data with 10mV resolution for AIN0 to AIN6 respectively. Once the voltage forced at AIN0 to AIN6 pin exceed setup data in these register, it will generate interrupt respectively. For example, write 0xC8 into register (Reg Add, 0x2A), which means once voltage at AIN0 pin exceeds 2000mV, it will cause AIN0 interrupt.
0x2C	AIN1_High_Limit	
0x2E	AIN2_High_Limit	
0x30	AIN3_High_Limit	
0x32	AIN4_High_Limit	
0x34	AIN5_High_Limit	
0x36	AIN5_High_Limit	
0x2B	AIN0_Low_Limt	These 6 registers are used to setup low limit data with 10mV resolution for AIN0 to AIN6 respectively. Once the voltage forced at AIN0 to AIN6 pin exceed setup data in these register, it will generate interrupt respectively. For example, write 0x14 into register (Reg Add, 0x2A), which means once voltage at AIN0 pin exceeds 200mV, also it will cause AIN0 interrupt.
0x2D	AIN1_Low_Limt	
0x2F	AIN2_Low_Limt	
0x31	AIN3_Low_Limt	
0x33	AIN4_Low_Limt	
0x35	AIN5_Low_Limt	
0x37	AIN6_Low_Limt	

1.10.15 High_Temp_Limit, High_Temp_HYS

Register Address: 0x38, 0x39

Register Attribution: Read / Write

Default Data: 0x00 after POR.

When measurement temperature in each monitoring cycle exceeds the value setup in High_Temp_Limit (Reg Add, 0x38), it will generate over temperature alarm can related interrupt.

Once the temperature drops below the value setup in High_Temp_HYS (Reg Add, 0x39), all alarm and related interrupt will disappear.

1.10.16 THERM_Temp_Limit, THERM_Temp_HYS

Register Address: 0x3A, 0x3B

Register Attribution: Read / Write

Default Data: 0x00 after POR.

1.10.17 FAN1, FAN2_COUNT_Limit

Register Address: 0x3C, 0x3D

Register Attribution: Read / Write

Default Data: 0x00 after POR.

1.10.18 Manufacturer_ID

Register Address: 0x3E

Register Attribution: Read Only

Default Data: 0x59.

1.10.19 Device_ID

Register Address: 0x3F

Register Attribution: Read Only

Default Data: 0x80.

1.11 SMBus Digital Interface

1.11.1 Slave Address

This device has 8 different SMBus or I^{2}C slave addresses shown as below table in read/read mode.

Item	Slave Address	A6	A5	A4	A3	A2	A1	A0	R/W
1	0x51/50	0	1	0	1	0	0	0	1/0
2	0x53/52	0	1	0	1	0	0	1	1/0
3	0x55/54	0	1	0	1	0	1	0	1/0
4	0x57/56	0	1	0	1	0	1	1	1/0
5	0x59/58	0	1	0	1	1	0	0	1/0
6	0x5B/5A	0	1	0	1	1	0	1	1/0
7	0x5D/5C	0	1	0	1	1	1	0	1/0
8	0x5F/5E	0	1	0	1	1	1	1	1/0

1.11.2 Timeout

The chip supports SMBus timeout. If the clock is held low for longer than 30ms (Typ.), the chip will reset its SMBus protocol and be ready for a new transmission. For this reason, the minimum clock frequency should be over 1.0 kHz.

1.11.3 SMBus Protocol

The chip supports four standard SMBus protocols Send Byte, Read Byte, Write Byte and Receive Byte, shown as below tables.

Write Byte

S	Slave Add	R/W	ACK	Reg Add	ACK	Reg Data	ACK	P
	0101, XXX	0	0	XXh	0	XXh	0	

Read Byte

S	Slave Add	R/W	ACK	Reg Add	ACK	S	Slave Add	R/W	ACK	Reg Data	NACK	P
	0101, XXX	0	0	XXh	0		1001100	1	0	0	1	

Send Byte

S	Slave Add	R/W	ACK	Reg Add	ACK	P
	0101, XXX	0	0	XXh	0	

Receive Byte

S	Slave Add	R/W	ACK	Reg Add	NACK	P
	0101, XXX	1	0	XXh	1	

Here S means SMBus Start to communication with master.

P, means communication STOP.

Slave Add, means the chip's SMBus address.

Reg Add, means pointed Register Address.

Reg Data, means data to be written into register or read from register.

1.11.4 Compatible with I^{2}C

The chip is compatible with both SMBus and I^{2}C. And the major difference between SMbus and I^{2}C are shown as below besides logic level. For more information, refer to SMbus specification v2.0 and I^{2}C specification v2.1.

1). this chip supports I^2C fast mode (400kHz) and standard mode (100kHz), which can cover SMBus maximum frequency 100kHz.

2). For SMBus protocol, the minimum frequency is 10kHz. There is no such limitation for I2C.

3). For SMBus protocol, slave device will reset if hold clock at '0' longer than 30ms. There is no timeout limitation for I2C.

4). ARA (Alert Response Address)general call is only valid interrupt in SMbus, not valid in I2C.

1.12 ALERT Output

ALERT pin is an output pin with open drain structure, and it will be pulled low by internal circuits once ALERT trigger happens in normal working mode. It requires an external pull-up resistor. This pin indicates the measured temperature status. Any of below events happens, ALERT pin will be pulled-low. All below situations are called ALERT trigger.

1). local channel temperature exceeds that of high-limit register data;

2). local channel temperature equals or drops lower that of low-limit register data;

3). remote 1 channel temperature exceeds that of high-limit register data;

4). remote 1 channel temperature equals or drops lower that of low-limit register data;

5). remote 2 channel temperature exceeds that of high-limit register data;

6). remote 2 channel temperature equals or drops lower that of low-limit register data;

7). remote 1 diode is open/disconnect;

8). remote 2 diode is open/disconnect;

	High-limit Register Address		Low-limit Register Address	
	MSB	LSB	MSB	LSB
Local Channel	0x05: R/O 0x0B: R/W	N/A	0x06: R/O 0x0C: R/W	N/A
	Default: 0x55, [85°C]		Default: 0x00, [0°C]	
Remote 1 Channel[NOTE5]	0x07: R/O 0x0D: R/W	0x13: R/W	0x08: R/O 0x0E: R/W	0x14: R/W
	Default: 0x55[MSB], 0x00[LSB], [85°C]		Default: 0x00[MSB], 0x00[LSB], [0°C]	
Remote 2 Channel	0x31: R/W	0x36: R/W	0x32: R/W	0x37: R/W
	Default: 0x55[MSB], 0x00[LSB], [85°C]		Default: 0x00[MSB], 0x00[LSB], [0°C]	

Note 5,

1). If set BIT3 of configuration register as '1', the high/low-limit register data will effect remote channel 2, if BIT3 = 0 as default, it will effect remote channel 1.

2). the data format of all channels' registers, including local, remote1 and remote2 should be kept the same as the format of temperature data. There is 2 data formats, depends on RANGE bit is '0' or '1'.

Once ALERT trigger happened, ALERT pin will be asserted and the relevant register bit of STATUS 1 or 2 will be setup too. There are 2 status registers which will affect ALERT pin status, shown as below.

STATUS 1 Register, Add: 0x02

BIT	ALERT	Name	Description
7	No	ADC_B	1 -- means ADC is busy for temperature converting
6	Yes	LTHA	1 --means temperature in local channel is higher than that of setup in local channel high-limit register, alert active
5	Yes	LTLA	1 --means temperature in local channel is lower than that of setup in local channel low-limit register, alert active
4	Yes	R1THA	1 -- means temperature in remote channel 1 is higher than that of setup in remote channel 1 high-limit register, alert active
3	Yes	R1TLA	1 -- means temperature in remote channel 1 is lower than that of setup in remote channel 1 low-limit register, alert active

2	Yes	R1DO	1 -- means remote channel 1 diode is open/disconnected
1	No	R1TM	1 -- means remote channel 1 THERM alarm active
0	No	LTM	1 -- means local channel THERM alarm active

STATUS 2 Register, Add: 0x23

BIT	ALERT	Name	Description
7-5	No	Reserved	Not defined, reserved for usage in the future.
4	Yes	R2THA	1 -- means temperature in remote channel 2 is higher than remote channel 1 set high-limit, alert active
3	Yes	R2TLA	1 -- means temperature in remote channel 2 is lower than remote channel 1 set low-limit, alert active
2	Yes	R2DO	1 -- means remote 2 diode is open/disconnected
1	No	R2TM	1 -- means remote channel 2 THERM alarm active
0	No	ALT	1 -- means alert is activated

ALERT trigger can be masked for local, remote 1, remote 2 or all 3 channels by setting mask bit of Configuration 1 and ALT_CON registers respectively. If set ALTMSK (bit7 of Configuration 1) as 1, there is no ALERT trigger anymore. If set ALT_TM (bit7 of Configuration 1) as 1, PIN8 is configured as THERM 2 function, there is no ALERT trigger too. Marked 'YES' in ALERT column of below table will affect ALERT pin status.

Configuration 1 Register, Add: 0x03(R/O) & 0x09 (R/W)

BIT	ALERT	Name	Description
7	Yes	ALTMSK	0 -- disable to mask all ALERT interrupt function; 1 -- enable to mask all ALERT interrupt function;
6	Yes	STB	0 -- the chip is active and working normally; 1 -- the chip is in standby mode.
5	Yes	ALT_TM	0 -- configure PIN8 as ALERT function; 1 -- configure PIN8 as THERM2 function;
4	No	Reserved	
3	No	RT1_2	0 -- temperature data (MSB, 0x01 and LSB 0x10) is used for remote channel 1; 1 -- temperature data (MSB, 0x01 and LSB 0x10) is used for remote channel 2;
2	No	RANGE	0 -- temperature expression range is 0 to 127^{o}C; 1 -- temperature expression range is -64 to 191^{o}C.
1	Yes	R1MSK	0 -- disable to mask ALERT action caused by remote channel1; 1 -- enable to mask ALERT action caused by remote channel1.
0	Yes	R2MSK	0 -- disable to mask ALERT action caused by remote channel2; 1 -- enable to mask ALERT action caused by remote channel2.

The ALERT consecutive time number (ALT_CON, bit3-0, of ALT_CON register) will affect ALERT trigger. Default 1 time happen will cause ALERT trigger. If set consecutive time number as 4 (ALT_CON, 111x) to prevent temperature noise, ALERT trigger only happens after 4 consecutive times trigger.

ALT_CON Register, Add: 0x22

BIT	ALERT	NAME	Description
7	No	SCL_TO	0 -- to enable SMBus clock time out; 1-- to disable SMBus clock time out;
6	No	SDA_TO	0 -- to enable SMBus data time out; 1-- to disable SMBus data time out;
5	Yes	LTMSK	0 -- disable to mask ALERT action caused by local channel; 1 -- enable to mask ALERT action caused by local channel.
4	No	Reserved	
3-0	Yes	ALT_CON[3:0]	To setup the number of consecutive times to trig ALERT condition, 000x -- 1 001x -- 2 011x -- 3 111x -- 4

Also CH_SEL (bit5-4 of Conv_Rate register, Add: 0x0A) will affect the ALERT trigger, since there is an option which can enable only one channel channel activity. All other disabled channels will not cause ALERT trigger anymore.

ALERT trigger cannot be released automatically even the measurement temperature comes back to temperature between high-limit and low-limit. It is released only by below conditions: Reading STATUS registers or and SMBus ALERT Response (ARA).

1). the trigger conditions disappear, and STATUS 1 and STATUS 2 registers are read already by host;

2). the host sends the command of Alert Response Address (ARA) via SMBus;

1.12.1 Alert Trigger Release Condition 1

Below Figure shows the mechanism of the ALERT pin output interrupt. Once ALERT trigger happens, the ALERT pin will be asserted (active low). And ALERT pin can be released by any of below conditions: 1).Reading both STATUS registers [0x02, 0x23]. 2). SMBus alert response happened.

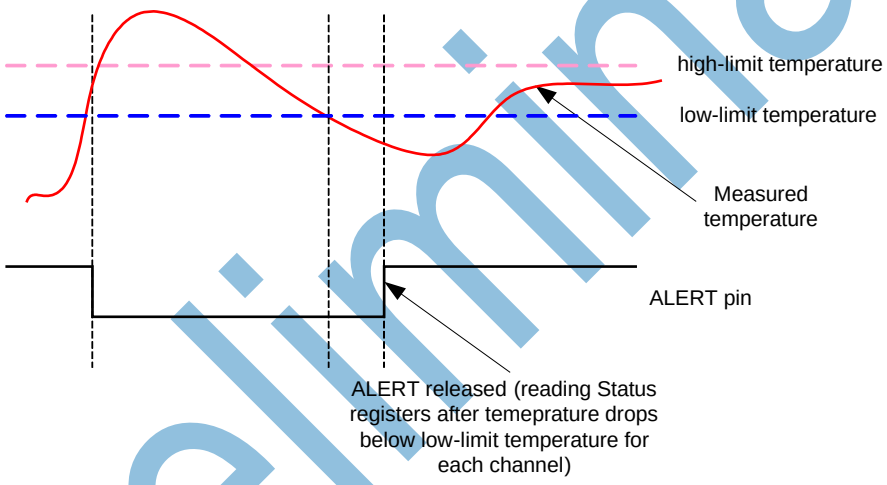


Figure 7 ALERT pin output in interrupt mode

1.12.2 Alert Trigger Release Condition 2

It can be used as a processer interrupt or as SMBus ALERT. When the master detects that ALERT pin is asserted, it will send Alert Response Address (ARA) to general address (0001, 100xb). All devices with active interrupts will respond with client address.

Below Figure shows the mechanism of the ALERT output SMBus Alert mode. In this mode, the ALERT output is connected to the SMBus alert line which has more than one device connected to it. Through such and implementation, SMBus alert mode can assist the master in resolving which salve generates an interrupt. When the measured temperature falls outside of the allowed range, the ALERT pin will be pulled low and the corresponding alert flags in Status Register will be set to 1. The ALERT mask bit will just be set if there is a read command for Status Register or when SMBus ALERT Response Address (ARA) occurs from master (Alert Response Address is 0001100xb). Meanwhile, the chip will generate and return its own address to the master. If the temperature never falls outside of the allowed range, the latched ALERT pin

can release by the reset ALERT mask bit and the latched corresponding alert flags in Status Register can release by reading command for Status Register.

S	Slave Add	R/W	ACK	Reg Add	ACK	P
	0001100	1	0	1001 100xb	1	

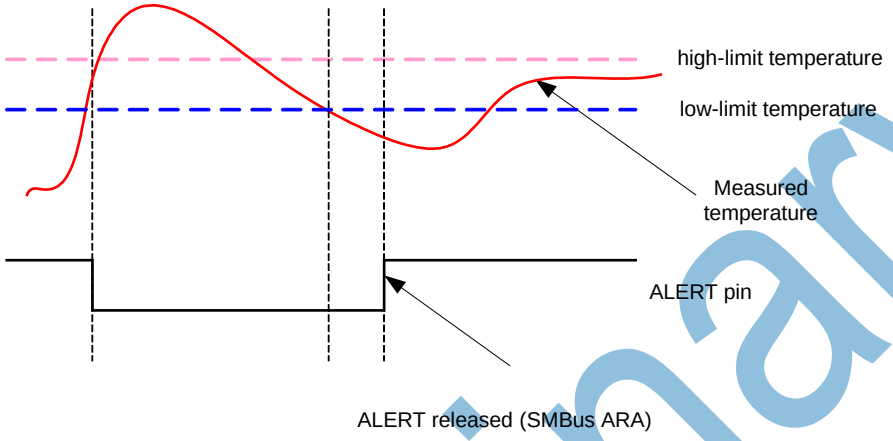


Figure 8 ALERT pin in SMBus ARA

1.13 THERM Output

THERM pin is also an active low output with open drain. The THERM is asserted and pulled low when any of the measured temperatures exceeds the THERM limit temperature programmed by user in Register 0x19, 0x20, 0x39. Once THERM pin outputs low, it will remain asserted and will not be released until all measured temperature is lower than THERM limit minus THERM Hysteresis(also programmable in register add 0x21). When the THERM pin is asserted, THERM Status bits of STATUS1 and STATUS 2 Registers will be set respectively and will not be cleared until the THERM pin is de-asserted. THERM trigger cannot be masked, which is unlike ALERT trigger. Below Figure shows this mechanism.

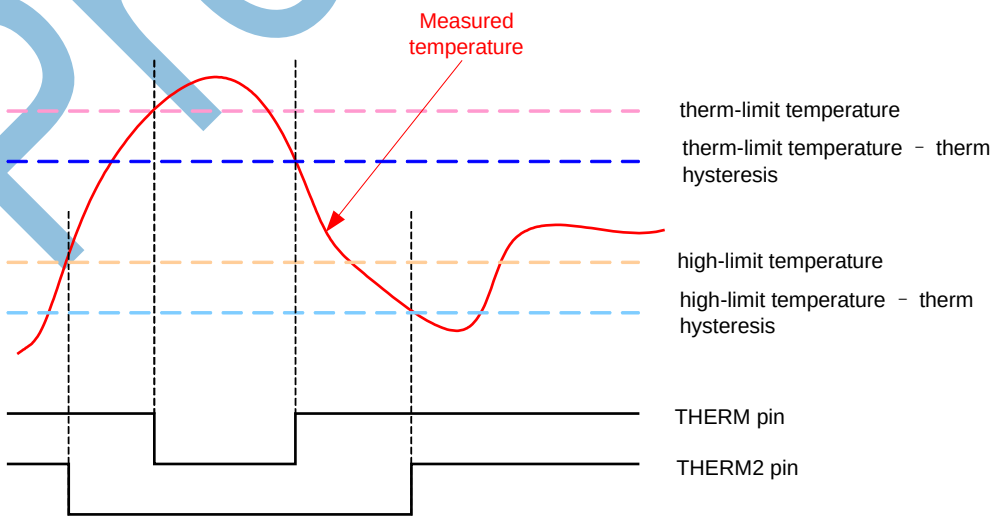


Figure 9 THERM pin and THERM2 pin output

PIN8 can be configured as 2nd THERM PIN (THERM2), by setting bit5 of Configuration 1 register as '1'. Once PIN8 is used as THERM2, only high-limit temperature is used as THERM-limit temperature, and user can ignore low-limit temperature register data. THERM2 pin can be released once all channels temperature drops below high-limit temperature minus hysteresis temperature.

1.14 Remote Diode Fault Alarm and Diode Selection

The chip can detect an open on each remote channel, between DP and DN pins (e.g. external diode is open or disconnected). In each temperature measurement cycle, the chip checks diode fault for each external diode. When a diode open is detected by the chip, the ALERT pin is asserted (ALERT is enabled and NOT masked) and the temperature data is 0xFFh (MSB) and 0xF0 (LSB). Also R1DO/R2DO bit (bit2) of Status1/Status 2 register will be set '1'. When a diode short is detected, the temperature data is also 0xFFh (MSB) and 0xF0 (LSB). Once a thermal diode fault disappears, the R1DO/R2DO bit will be reset as '0', the temperature register gets back to the right data.

The chip is designed to measure both local and remote temperatures. For remote temperature sensing, the chip needs connection to an external diode, which could be a discrete diode or a discrete BJT (PNP type or NPN type) transistor with diode-connected. The external diode also can be substrate parasitic BJT transistor inside CPU or other GPU chips.

For Remote channel, temperature accuracy depends on external PN junction. It is better to select small-signal BJT transistor of proper performance with diode-connected. Proper performance includes below,

1). Vbe is between 250mV at 10uA and 950mv at 300uA;

2). Beta or current DC gain, is equal or larger than 30;

3). base resistance is below 100ohm.

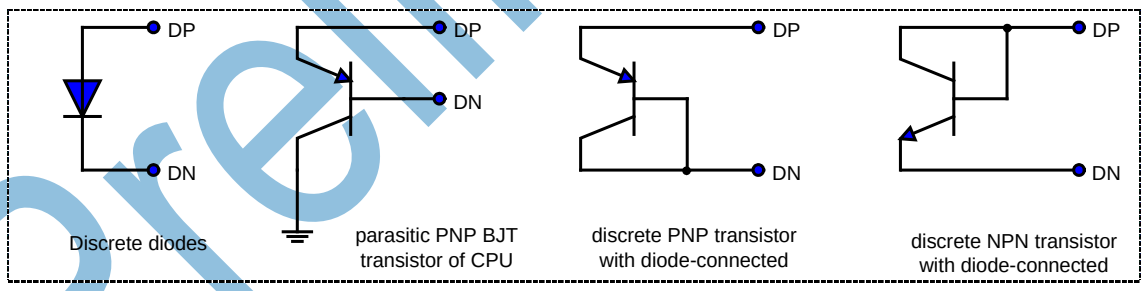


Figure 10 External Diode for Remote Channel

1.15 LOCK

LOCK bit, bit7 of Configuration 2 [Add: 0x24] can lock all registers with R/W attribution, which can prevent writing any data into registers.

LOCK = 0, default, all registers with R/W attribution are writable;

LOCK = 1, all registers with R/W attribution are non-writable even Configuration 2 register.

For example, write 0x80 into this register [address, 0x24] to set LOCK bit as '1'. Also it will lock this register itself. There is only one way to unlock this bit after power-on the chip.

1.16 POR and UVLO

The chip uses volatile memory. To prevent unclean power-supply conditions, which could happen in system application, from corrupting the data in memory and causing an expected situation, a POR voltage detector monitors VCC and clears the memory if VCC falls below threshold voltage (1.1V in typical). When VCC rises above threshold voltage (1.2V in typical), the logic blocks begin operating. Then the chip block will work normally along with VCC rising high enough gradually.

2 Applications Information

2.1 How to Improve Temperature Accuracy

The temperature measurement of the chip is based on semiconductor physics principle --Forward voltage of diode is a function of temperature. The formula is shown as below.

$$V_F = \frac{kT}{q}\ln\left(\frac{I_F}{I_S}\right)$$

Here,

V_F -- forward voltage

I_F -- forward current

I_S -- reverse saturation current

k -- Boltzmann constant

T -- Temperature in K

*q -- Electric charge con*stant

To cover wide temperature range, i.e. -40 °C to 125°C, a very small voltage variation is corresponding to each degree C temperature change. For this chip, 200μV voltage between DP and DN pin stands for about 1°C. Sensylink has applied many ways to improve measurement accuracy in chip circuits design, such as compensation, trimming etc. In real system design, however, some factors that can increase measurement error need to be considered. Most issues that usually occur are highlighted as below.

2.1.1 Serial Resistor (R_S), Differential Capacitor (C_d) of Remote Channel

In most applications, the remote diode could be located noise environment. Generally 200uV stands for about 1°C, any common-mode noise between DP and DN pin will cause temperature measurement error. the better way to use serial resistor (Rs) plus Differential Capacitor (Cd) to filter noise coupled to DP, DN wire. The sensor chip built-in serial resistor cancellation circuits which can remove the temperature measurement error caused by Rs. The maximum resistance does not exceed 1.0kohm for Rs. For the differential capacitor, it will affect setup and sampling time of AD converter, so the maximum capacitance does not exceed 1000pF. For example, Rs = 100ohm, Cd = 100pF. If the remote channel is NOT used, it is better to leave these pins open.

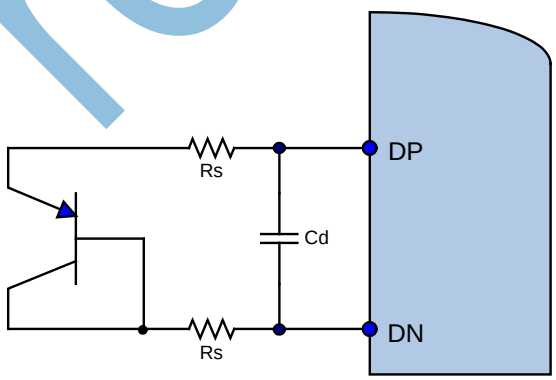


Figure 11 Rs and Cd for Remote Channel

2.1.2 Thermal Response Time

It is very necessary to wait enough time for obvious temperature changing of target due to thermal time constant, e.g. taking food out of refrigerator, temperature changes from -20°Cto 20°C, which could take over ten minutes to reach thermal equilibrium eventually. Enough time is still needed for the target to reach thermal equilibrium, even forcing temperature transient into target object. For example, changing 100°C suddenly around this chip, it will take about 15 minutes to reach thermal equilibrium on this chip die under 1°C accuracy. For remote channel, if using a discrete transistor as thermal diode, the package of transistor is another important consideration which can affect thermal response. For examples, using 2N3904 as thermal diode, SOT-23 package has better thermal contact than TO-92 package.

2.1.3 Self-heating

For local channel, self-heating could affect temperature measurement accuracy. It always brings positive error. It could be estimated as below steps.

Step 1, Estimating the chip power consumption, caused by average operating current and sink current at $\overline{\text{ALERT}}$ pin, $\overline{\text{THERM}}$ pin. for example,

Pd1 = V_{CC} * I_{AOC} = 5.0V * 350uA = 1.75mW

(Assuming Vcc is 5.0V, conversion rate is 8Hz.)

Pd2 = V_{OL} * I_{SINK} = 0.1V *0.5mA *2 = 0.1mW

(Assuming in normal operating, both $\overline{\text{ALERT}}$ pin and $\overline{\text{THERM}}$ pins are active, and pull-up resistors are 10k)

Pd total = Pd1 + Pd2 = 1.75mW + 0.1mW = 1.85mW

Step 2, Estimating junction temperature error caused by power consumption,

delta Tj = Pd total * Theta J-A = 1.85mW * 140°C/W = 0.26°C

2.1.4 Setup by System Software

It is necessary to properly setup/optimize system software to improve reliability and consistency of the temperature data. Below is the sample guideline for reading temperature data with 1Hz frequency.

1). Setup conversion rate register (0x0A) as 2Hz;

2). Read the temperature data 2 times in one second;

3). Average out the above 2 temperature data

4). Do moving-average repeatedly for the last 2 average temperature readings

5). Compensate positive temperature error caused by self-heating, which could be estimated by the calculation in 2.1.4;

6). Compensate error caused by environment temperature around the chip, which could be obtained by another local channel;

7). Output above temperature data once every second.

2.2 PCB Layout

Cautions below are important to improve temperature measurement in PCB layout design.

2.2.1 Device placement

It is better to place the sensor chip away from any thermal source (e.g. power device in board), high speed digital bus (e.g. memory bus), coil device (e.g. inductors) and wireless antenna (e.g. Bluetooth, WiFi, RF). It

is recommended to place the chip close to the remote diode. The better way is to use serial resistor (R_S) plus differential capacitor (C_d) for each remote channel to filter noise.

2.2.2 DP, DN Route in PCB

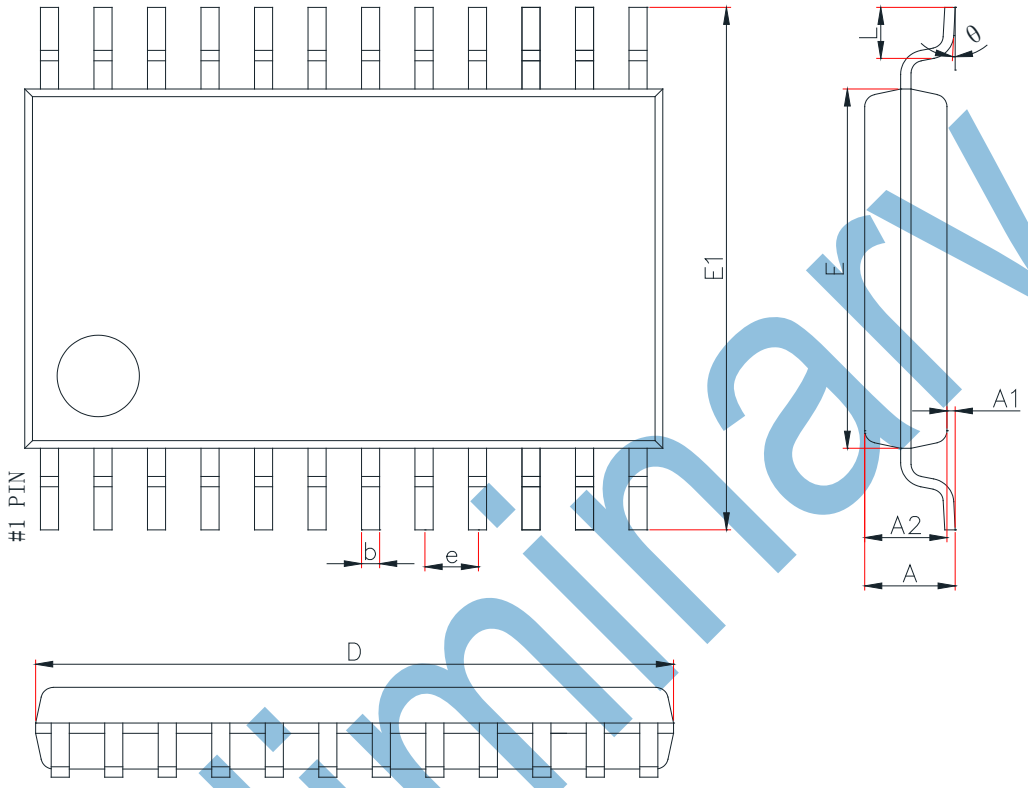
It is better to draw the traces of DP and DN netlist as a pair trace and to make sure that the two are always kept with the same distance and the same layer in PCB board. Also it is better NOT TO change PCB layer for this pair trace, which means to keep trace to the same layer as the chip and remote diode.

2.2.3 Twisted cable and shield

Another method is to use ground shield around the DP, DN pair trace, which could reduce digital noise. Twisted cable with shield is recommended for long distance temperature measurement that uses a discrete diode as the remote channel. Shield is shorted to ground.

Package Outline Dimensions (TSSOP-24)

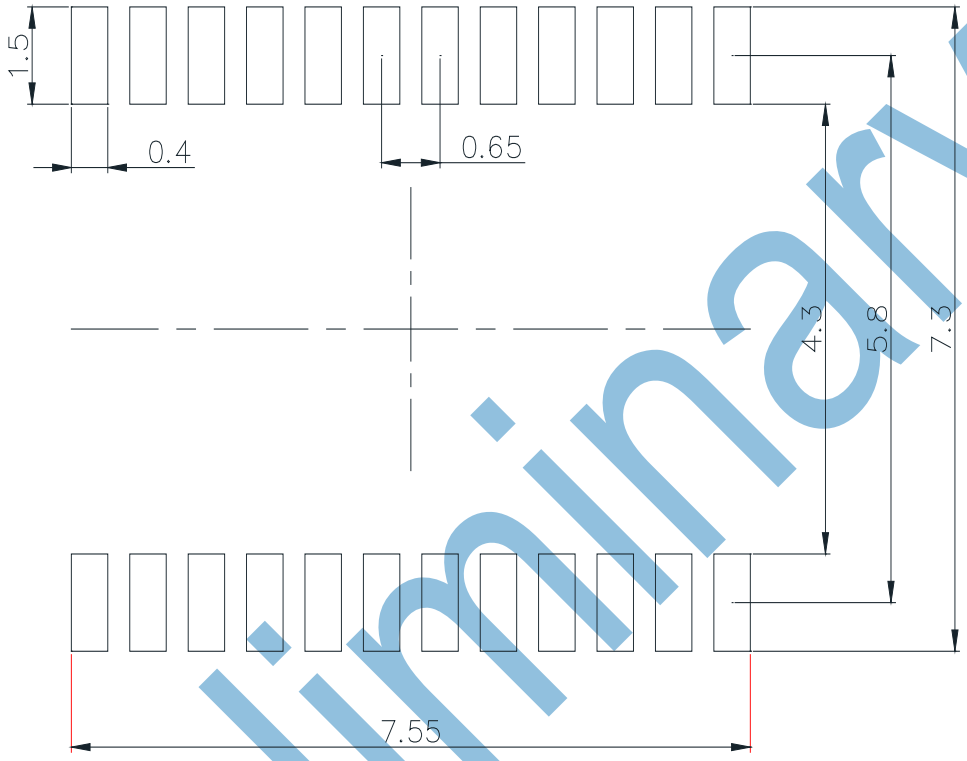
TSSOP-24 **Unit (mm)**



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	7.700	7.900	0.303	0.311
E	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.244	0.260
e	0.650（BSC）		0.026（BSC）	
L	0.400	0.800	0.016	0.031
θ	0°	8°	0°	8°

Recommend Land Pattern Layout (TSSOP-24)

TSSOP-24 **Unit (mm)**



Note:

1 All dimensions are in millimeter

2 Recommend tolerance is within ±0.1mm

3 Change without notice

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