Analog Electronic Circuits – 2024-2025
Design Project Report

Group data

Group number	14
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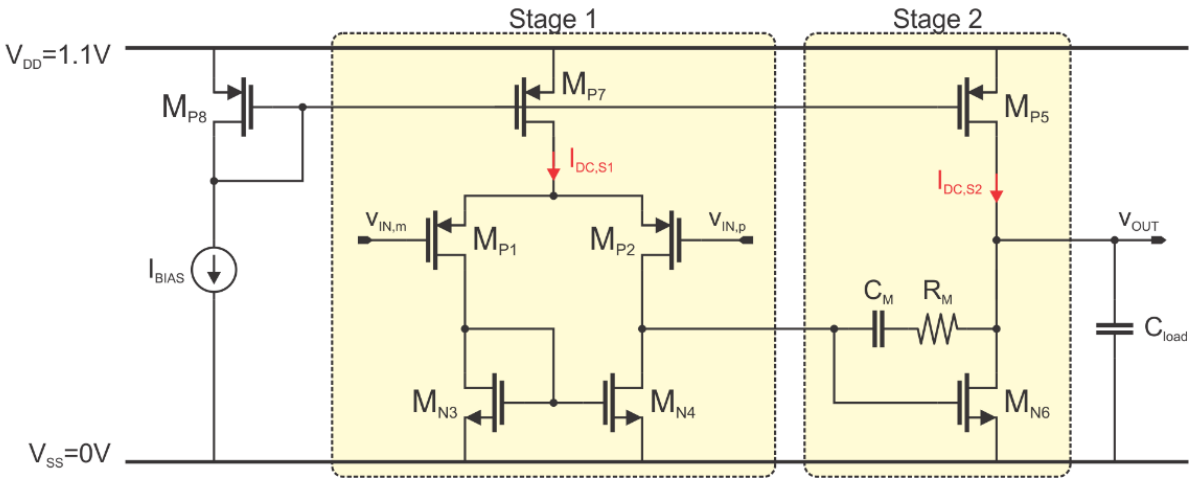
Goal:



Design of the 2stage OpAmp such that it passes the given specifications (insert your specs below):

$C_{load}[pF]$	10
DC gain [dB]	50
f_{GBW} [MHz]	180
Phase margin (PM) [deg]	> 70
Output swing [V]	> 0.7

Plan: Design of the 2-stage OpAmp on paper (10 points)

Calculate the V_{OV}, g_m, I_{DS} and L of each transistor (see exceptions under "*Remark*") and the required C_M and R_M in the OpAmp circuit. For that, insert all your calculations as well as your $\frac{g_m}{g_{ds}}$-, $\frac{g_m}{I_D}$-plots you used for your handcalculations below:

Hints:

- *First, plot $\frac{g_m}{g_{ds}}$ and $\frac{g_m}{I_D}$ across V_{OV} and gatelength L and do it again across V_{GS}, as presented in the 1st session. Think about whether to create the plots for a PMOS or for a NMOS device.*
- *Then, based on those plots, start your calculations.*
- *Furthermore, you can assume the following:*
  (1) the OpAmp is designed in triple-well-technology (i.e. $V_{SB} = 0$); (2) $V_{dsat} \approx V_{OV}$ and $V_{dsat} \geq 50mV$ across V_{OV}; (3) $C_M = \frac{1}{4} \cdot C_L$

Remarks:

- *For Mp5, Mp7 and Mp8 you are not required to calculate the g_m*

Plots used for the handcalculations:

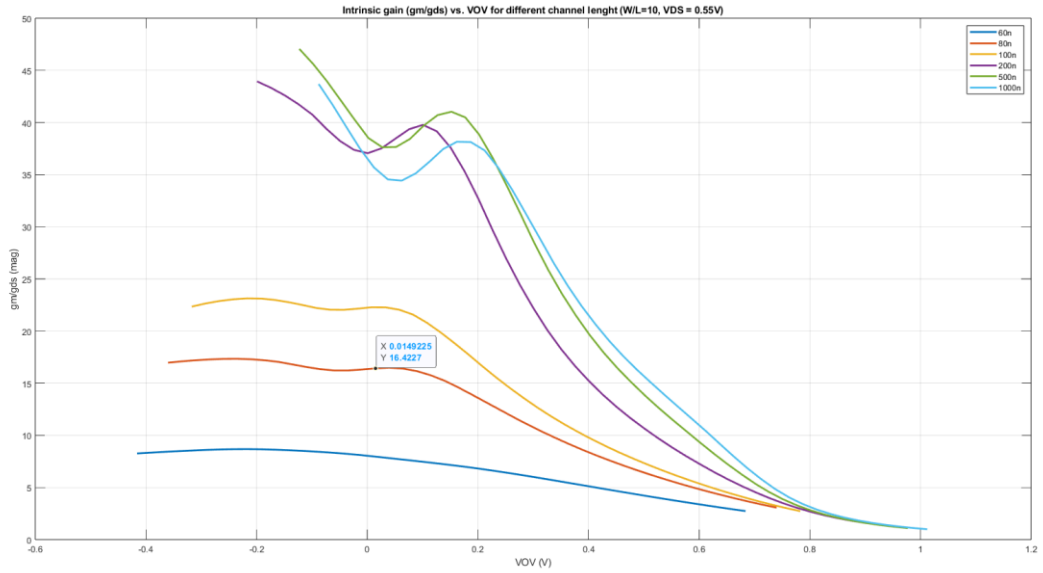


Figure 1: $\frac{g_m}{g_{ds}}$ vs V_{OV} across gatelength L - NMOS

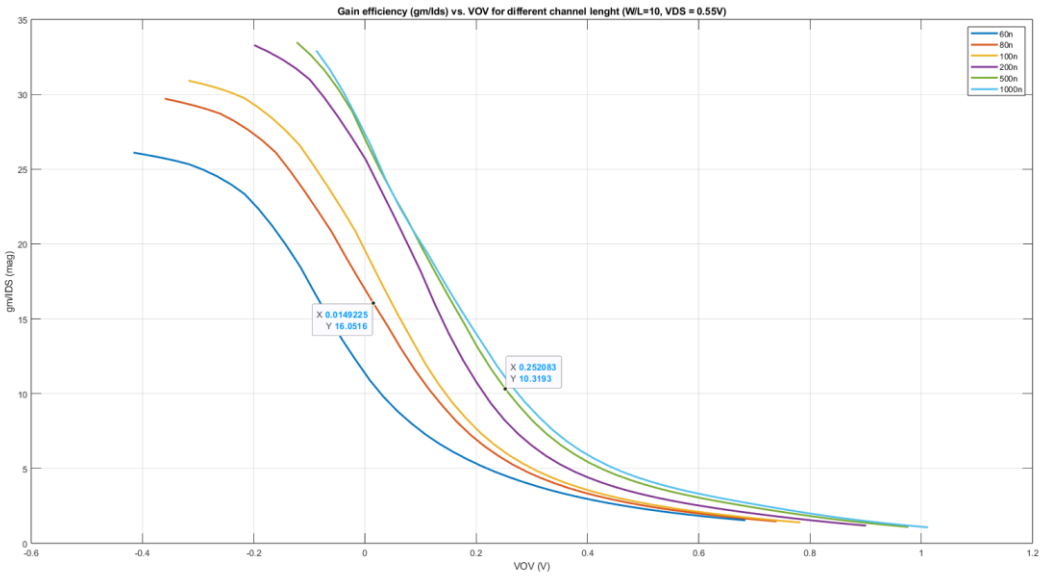


Figure 2: $\frac{g_m}{I_D}$ vs V_{OV} across gatelength L - NMOS

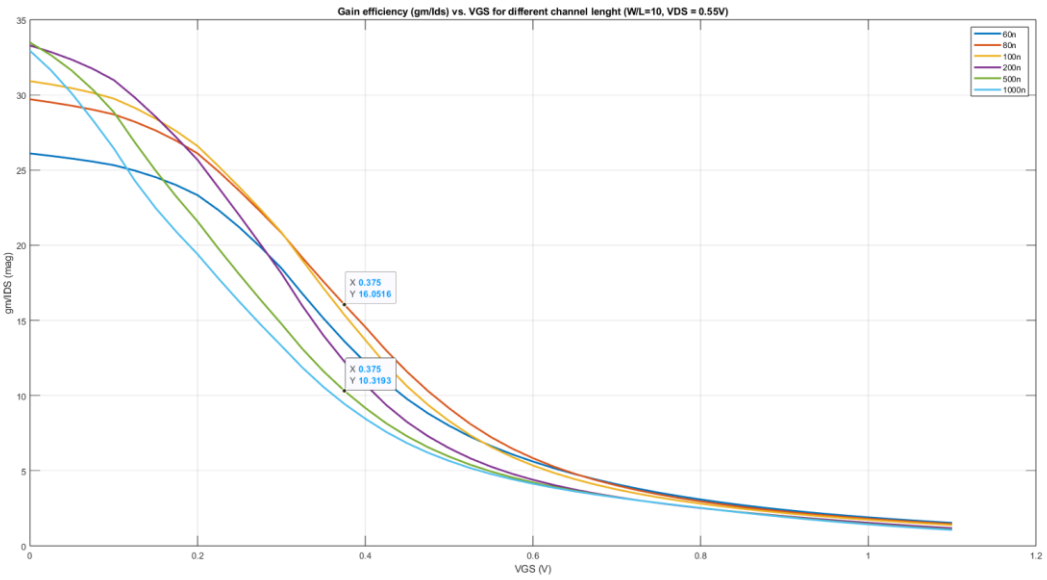


Figure 3: $\frac{g_m}{I_D}$ vs V_{GS} across gatelength L - NMOS

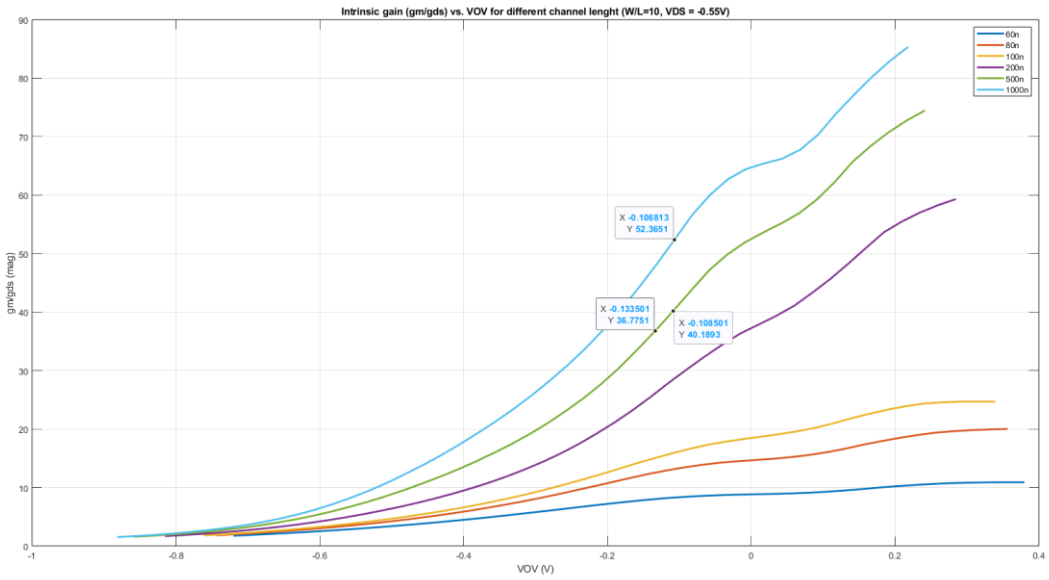


Figure 4: $\frac{g_m}{g_{ds}}$ vs V_{OV} across gatelength L – PMOS

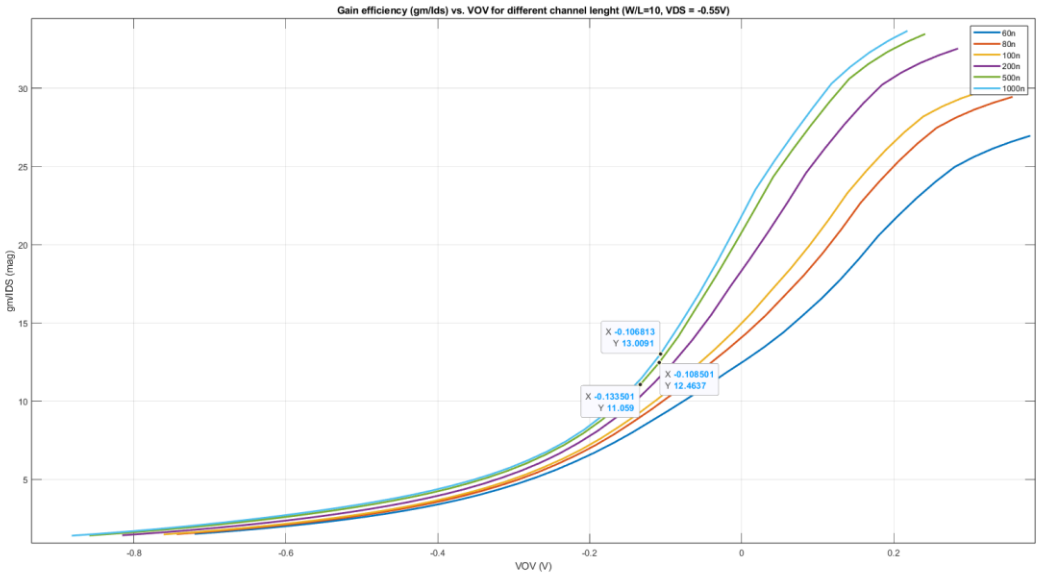


Figure 5: $\frac{g_m}{I_D}$ vs V_{OV} across gatelength L – PMOS

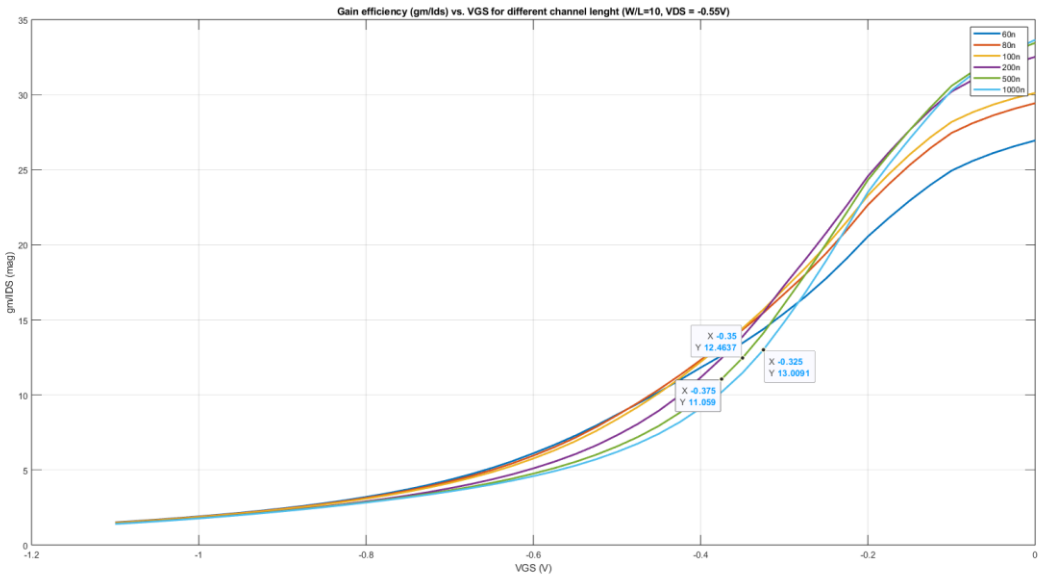


Figure 6: $\frac{g_m}{I_D}$ vs V_{GS} across gatelength L – PMOS

Handcalculations:

1. Constraints

Starting from our constraints, we can already make some choices, assumptions and find some parameters:

- The Miller capacitance C_M is imposed and equals to:

$$C_L/4 = 2.5pF$$

- We want to achieve a DC gain of 50dB (316.227766). We split the gain, and we chose:

First Stage Gain	19.2555
Second Stage Gain	16.4227

Also, we assumed the following for the gains:

Assumptions	Consequences
$L_5 \gg L_6$	$A_{V2} = 16.4227 \approx \frac{gm_6}{gds_6}$
$L_{1,2}, L_{3,4}$ are long	$gds_{1,2} \approx gds_{3,4} \rightarrow A_{V1} = 19.2555 \approx \frac{gm_{1,2}}{2 \cdot gds_{1,2}}$

- The constraint on f_{GBW} gives the value of $gm_{1,2}$:

$$f_{GBW} = \frac{GBW}{2\pi} = \frac{|A_{vo} \cdot p_{dm}|}{2\pi} = \frac{gm_{1,2}}{2 \cdot \pi \cdot C_M} = 180\ MHz$$

$$\Leftrightarrow gm_{1,2} = 2.827mS$$

- We can find the value of gm_6 using the constraint on the PM. But first, we must choose if we either place the second pole p_3 (non-dominant pole) on GBW and cancel it with the zero introduced by R_M or we use a graph to know where we must place p_3 with respect to GBW to have the wanted PM. We decided to do the first approach and that means:

$$\frac{|p_3|}{GBW} = 1$$

$$\Leftrightarrow gm_6 = C_L \cdot GBW = 11.3097\ mS$$

2. Second stage

Now, we can design the second stage. We start with Mn6, and we must consider the following things:

i. We must have a low Vdsat so that the output swing has enough room, in fact $V_{dsat6} < V_{out}$. Speaking of output swing, we must choose an operating point for V_{out}: we decided to go with 0.55V. This choice implies that $\boldsymbol{-V_{ds5} = V_{ds6} = 0.55V}$

ii. Then, the chosen length must be smaller than L_5 and because Mp5 is a current mirror, we already know that for Mp5 we'll take a long channel ($L_5 = 1000nm$). With this length L_6 and V_{OV6}, we must achieve the second stage gain $A_{V2} = 16.4227$. All of this leads us to the following choices using the graph on **Figure 1**:

MN6 Choices	
V_{OV6}	$0.014925V \rightarrow V_{dsat6} \approx 50mV$
L_6	$80nm$

MP5 Choices	
L_5	$1000nm$

Knowing V_{OV6}, we can use the graph on **Figure 2** to find gm_6/IDS_6 and because we know gm_6, we can find the current flowing through the second stage (this current is the same for Mp5):

$$IDS_6 = \frac{gm_6}{16.0516} = 704.584\mu A = IDS_5$$

The only parameter left to choose for the second stage is V_{OV5} (We already know the current and the length of Mp5). We must choose it by respecting the output swing range, $V_{out} < V_{dd} - |V_{dsat5}|$. Also, by choosing the length and Vov of Mp5, we are imposing these values to Mp7 and Mp8 (their gates are connected so the Vov is the same for each one). Using the graph on **Figure 5**:

$$V_{OV5,7,8} = -0.106813V \rightarrow V_{dsat5,7,8} \approx -0.106V$$

Before designing the first stage, we are asked to find $V_{g5,7,8}$ and we can find it by doing the following computation:

$$V_{g5} = V_{gs5} + V_{s5} = V_{gs5} + 1.1.$$

We need to find Vgs5, and we can do it by taking the graph **Figure 6** (because we know gm5/IDS5, we look for which Vgs5 we have this value):

$$V_{G5,7,8} = -0.325 + 1.1 = 0.775V$$

3. First stage

For the first stage, we begin with Mp1,2 (they must be identical so every parameter we choose for one is the same for the other, this is also true for Mn3 and Mn4). We must choose $V_{OV1,2}$ and $L_{1,2}$ to achieve the wanted gain A_{v1} and consider that the length is big:

$$A_{v1} = \frac{gm_1}{2 \cdot gds_1} = 19.2555 \Leftrightarrow \frac{gm_1}{gds_1} = 38.511$$

This leads us to these choices (we find the Vov with an interpolation or by zooming in the graph, but it is less accurate) using the graph on **Figure 4**:

MP1,2 Choices	
$L_{1,2}$	$500nm$
$V_{OV1,2}$	$-0.12079V \rightarrow V_{dsat1,2} \approx -0.120V$

Now because we know $gm_{1,2}$ and $V_{OV1,2}$ we can find $IDS_{1,2} = IDS_{3,4} = 1/2 \cdot IDS_7$ using the graph on **Figure 5**:

$$IDS_{1,2} = IDS_{3,4} = 1/2 \cdot IDS_7 = \frac{gm_1}{11.7732} = 240.121\mu A$$

For Mn3,4, their Vgs is imposed and equals to Vgs6. So, we must find Vgs6 using the graph **Figure 3** knowing gm6/ids6: $V_{gs3,4,6} = 0.375V$. Then, we need to choose a channel length and because this is a current mirror, we'll take a long channel.

However, we didn't take the longest length available because while we were verifying the design using MATLAB, we found out that the pole p_1's frequency (pole on node 1) wasn't that high with respect to f_{GBW}, which we supposed to be true, when we choose a length of 1000nm. In other words, with a length of 1000nm for Mn3,4, the PM is decreased due to the presence of p_1. Decreasing the length makes sure that p_1 is at a higher frequency. In conclusion, we chose:

$$L_{3,4} = 500nm$$

Knowing the value of Vgs and the length, we can use the graph on **Figure 3** to find $gm_{3,4}/IDS_{3,4}$ and we already have the value of $IDS_{3,4}$, so we can find $gm_{3,4}$:

$$gm_{3,4} = 10.3193 \cdot IDS_{3,4} = 2.47788mS$$

Now we can use the graph on **Figure 2** to find $V_{OV3,4}$ because we know gm3/ids3 from the previous point:

$$V_{OV3,4} = 0.25208V \rightarrow V_{dsat3,4} \approx 0.25208V$$

4. Remaining values to compute

The only case left in the table for the transistors is the current for Mp8. We chose the current Ibias flowing through Mp8 to be the smallest current in the circuit:

$$IDS_8 = I_{BIAS} = 480.242\mu A = IDS_8$$

Concerning R_M, we said before that we'll cancel p_3 (non-dominant pole) with the zero introduced by R_M:

$$z_2 = \frac{G_M \cdot gm_6}{C_M \cdot (G_M - gm_6)}$$

$$\frac{G_M \cdot gm_6}{C_M \cdot (G_M - gm_6)} = \frac{-gm_6}{C_L} \Leftrightarrow G_M = \frac{gm_6}{5} = 2.2619mS$$

$$\Leftrightarrow R_M = 442.09\Omega$$

The only value left to derive is the value of Vds7 and we can find it by solving:

$$\begin{aligned} V_{DS7} &= V_{cm} - V_{DD} - V_{GS1} \\ &= 0.3825 - 1.1 + 0.362 \\ &= -0.3555\ V \end{aligned}$$

Where V_{cm} is the middle value of the common mode input range (see table below where we computed the max and min values).

Place the obtained values in the table below. Only the values in here need to be calculated / chosen in the handcalculations. Each value should be chosen with a reason which you have to provide above.

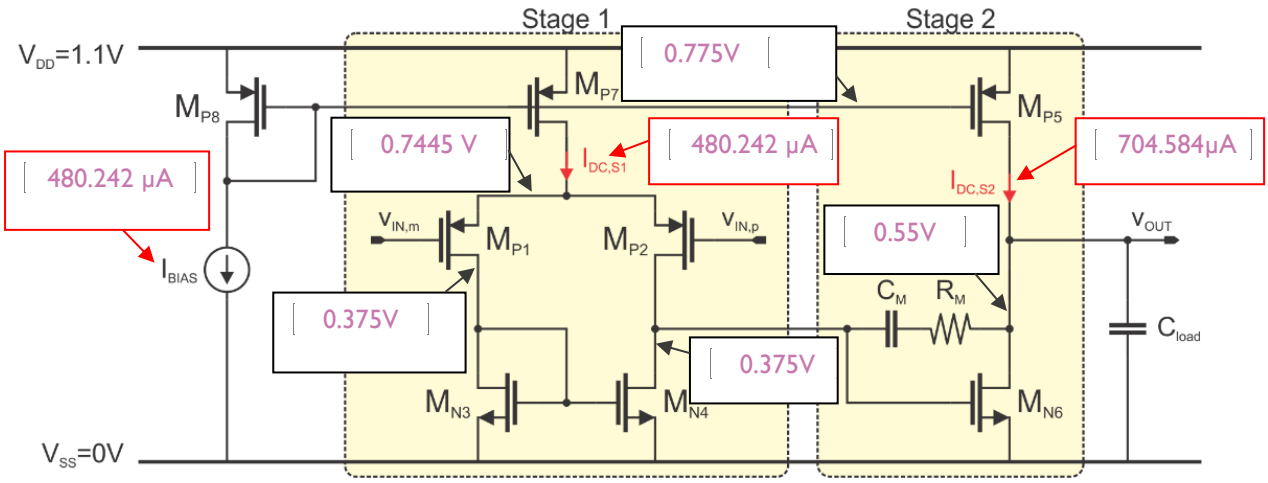
Device	L [nm]	I_{ds} [µA]	V_{OV} [V]	g_m [S]
M_{p1}	500	240.121	-0.120	2.827×10^{-3}
M_{p2}	500	240.121	-0.120	2.827×10^{-3}
M_{n3}	500	240.121	0.25208	2.47788×10^{-3}
M_{n4}	500	240.121	0.25208	2.47788×10^{-3}
M_{p5}	1000	704.584	-0.106	
M_{n6}	80	704.584	0.0149	11.3097×10^{-3}
M_{p7}	1000	480.242	-0.106	
M_{p8}	1000	480.242	-0.106	

Device	Units	Value
R_M	Ω	442.09
I_{BIAS}	A	480.242×10^{-6}

Place all the calculated voltages (in the black box) and all currents (in the red box) on the circuit depicted below and calculate also (include formula):

$V_{cm,in,min}$	$V_{cm,in,min} = V_{GS3} - V_{OV1} + V_{GS1}$ $= 0.375 + 0.120 - 0.362 = 0.133V$
$V_{cm,in,max}$	$V_{cm,in,max} = V_{DD} - \lvert V_{DSAT7}\rvert - \lvert V_{GS1}\rvert$ $= 1.1 - 0.106 - 0.362 = 0.632V$
$V_{out,min}$	$V_{out,min} = V_{DSAT6} = 50\ mV\ (V_{OV6} < 50mV\ and\ V_{DSAT} \geq 50mV)$
$V_{out,max}$	$V_{out,max} = V_{dd} - \lvert V_{DSAT5}\rvert \approx 1.1V - 0.106V = 0.994V$
P_{diss}	$P_{diss} = V_{dd} \times (I_{ds6} + I_{ds7} + I_{BIAS})$ $= 1.1V \times (480.224 \times 2 + 704.478) \times 10^{-6}$

	$= 1.831\ mW$


Stage 1
Stage 2
V_{DD}=1.1V
V_{SS}=0V
M_{P8}
M_{P7}
M_{P5}
M_{P1}
M_{P2}
M_{N3}
M_{N4}
M_{N6}
I_{BIAS}
$I_{DC,S1}$
$I_{DC,S2}$
$V_{IN,m}$
$V_{IN,p}$
V_{OUT}
C_M
R_M
C_{load}
0.775V
0.7445 V
480.242 µA
480.242 µA
704.584µA
0.55V
0.375V
0.375V

Design: Implementation of the OpAmp in MATLAB and LTspice (10 points):

Based on your handcalculations, create your OpAmp design in MATLAB.

Remarks:

- *Please make sure that all widths W are below 1mm*
- *Don't write your values calculated in the previous step as constants in MATLAB but write the full equation in your code.*
- *Values chosen as design choices should match between this table and the one from the handcalculations!*
- *Choose Vincm to be in the center of your input common-mode range. Do this in a 2-step process:*
  - *Use the center of the input common-mode range as calculated in the handcalculations for Vincm.*
  - Have MATLAB calculate the correct Vincm value using the calculated 'vdsat' fields of the transistors in MATLAB.

Fill out both tables depicted below. All values are to be determined in MATLAB.

Device sizes and bias point parameters according to MATLAB

Device	W [µm]	L [nm]	I_{ds} [µA]	V_{ov} [V]	g_m [mS]	g_{ds} [µS]	g_m/g_{ds} [-]	$V_{ds,sat}$ [V]	V_{ds} [V]
M_{p1}	87.95	500	235.90	-0.120	2.83	101.32	27.9313	-0.12388	-0.36950
M_{p2}	87.95	500	235.90	-0.120	2.83	101.32	27.9313	-0.12388	-0.36950
M_{n3}	15.39	500	235.90	0.25370	2.45	92.08	26.6073	0.15966	0.37498
M_{n4}	15.39	500	235.90	0.25370	2.45	92.08	26.6073	0.15966	0.37498
M_{p5}	614.08	1000	704.53	-0.106	9.21	175.32	52.5325	-0.11021	-0.55
M_{n6}	45.24	80	704.53	0.01490	11.31	688.67	16.423	0.06825	0.55
M_{p7}	434.85	1000	471.80	-0.10779	6.20	172.12	36.0214	-0.11142	-0.35550
M_{p8}	440.19	1000	471.80	-0.10807	6.20	195.46	31.72	-0.11161	-0.32419

Device	Units	Value
C_M	pF	2.5
R_M	Ω	442.10
I_{BIAS}	A	$0.47 * 10^{-3}$
$V_{in,cm}$	V	0.3820

Based on the parameters filled in the table above, design your OpAmp in LTspice. The filled-in MATLAB template and final LTspice schematic should be included in your Canvas submission (read the assignment instructions on Canvas to see the full description of the files to include).

Experiment (10 points):

In this section you will simulate the following:

A. Frequency Response in MATLAB and LTspice
B. Noise contribution in LTspice
C. Linearity in LTspice

Note on how to present graphs in general:

- *When you make a graph, put labels on every axis to make clear what you are showing. Also, show the units!*
- *When you plot multiple curves on one graph, add a legend.*

A. Frequency Response in MATLAB and LTspice

Note on how to present graphs in this sub-section:

- ***For magnitude plots use dB (linear scale) vs. Hz (logarithmic scale)***
- ***for phase plots use ° (linear scale) vs. Hz (logarithmic scale).***

Simulate A_v (small voltage gain) with C_M and R_M in MATLAB and LTspice. Then, paste both A_v-curves in separate plots below such that the difference between MATLAB and LTspice can be clearly seen. In addition to that, indicate the resulting phase margin (PM) in both plots.

Plots:

Bode Diagram on LTspice

Figure 7 Frequency Response in LTspice

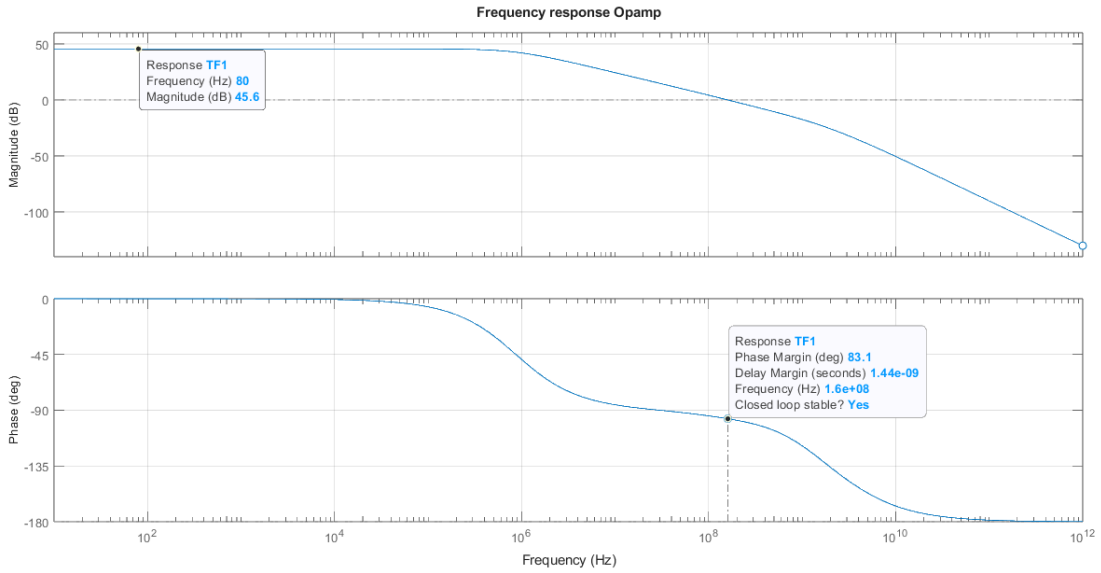


Figure 8 Frequency Response in Matlab

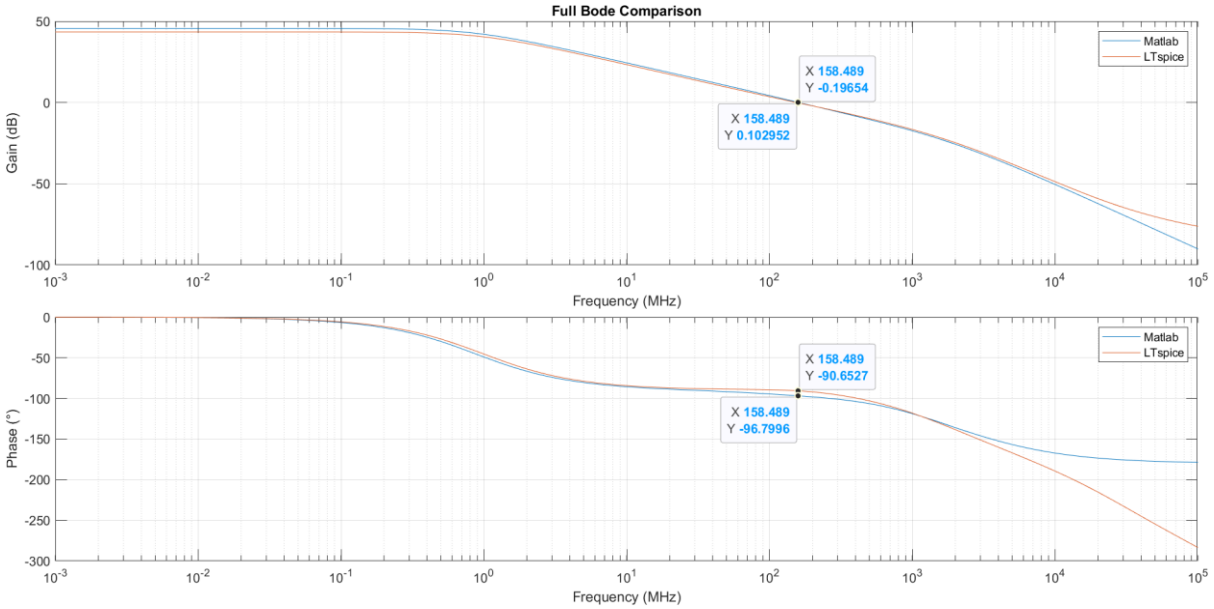


Figure 9 Comparison of the Frequency response between simulation Matlab and LTspice

Simulator	PM (deg)
MATLAB	83.1
LTspice	89.45

Explain, analyze and interpret the results above. Furthermore, if you observe significant differences between MATLAB and LTspice, explain why.

In the results above, we can see that at low frequency, the gain is 45.6 dB for MATLAB and slightly lower for LTSpice. This gain is the DC gain. Fortunately, the difference between MATLAB and LTSpice is very small, and a difference is expected. In fact, we used an approximate expression for the DC gain in MATLAB and we know that LTSpice simulates the circuit with more accurate expressions. However, we can see that the gain value isn't what we wanted, which is 50 dB. This can be explained by the fact that we approximated even more the DC gain expression for the hand calculation and used various assumptions to make the design step easier but more on that at the end, in the conclusion.

Now if we look further at the frequencies, we encounter the first pole which is the dominant pole at 871.6 kHz (from MATLAB). This pole introduces a -20dB/dec decrease in the gain and a -90° shift in the phase. At this point, we can also compute the fGBW ≈ 166 MHz. We can observe that MATLAB and LTSpice results are very close until the gain reaches 0dB.

At 0dB, we can make various observations. The first thing is that f_u (frequency for which gain=1) is not equal to fGBW. This is because in our case, the pole at higher frequency we usually

neglect (p1 at 1700 MHz) is close to 180 MHz (which is our wanted fGBW) and this influences the shape of the frequency response, in fact, fGBW is an asymptotic projection from the dominant pole.

Now, regarding fGBW not being equal to 180MHz, we don't meet the required gain (as we know, the DC gain changes the fGBW) and with the various assumptions we made and the fact that we didn't consider parasitic capacitances, the value of the dominant pole is different from the hand calculation but again, more on that at the end.

Because we put the non-dominant pole p3 and z2 very close, we don't see any increase of +20dB/dec or +90° shift in the frequency response. Also, this is why we have a high PM of 83.1 for MATLAB and 89.45 for LTSpice.

The difference between the PMs can be explained by looking at the higher frequencies. We can see that there is a noticeable difference in the gain and in the phase between MATLAB and LTSpice at these high frequencies. This is because there are many other poles and zeros we neglected with MATLAB and we know that LTSpice takes them into account, giving us a more accurate frequency response. Now knowing that we have these poles/zeros for LTSpice at these higher frequencies, we can understand why the shape of the frequency response is different even around 0dB thus changing the PM.

Simulate A_v in LTspice for the following cases:

a. No compensation network ($C_M = R_M = 0$).

b. With compensation capacitor but no compensation resistor ($R_M = 0$).

c. With both the compensation capacitor and the compensation resistor.

Then, show all 3 cases in separate plots such that the differences are clearly visible. Furthermore, indicate on each plot the resulting PM.

Plot:

Bode Diagram with Cm=Rm=0

Figure 10 Frequency Response with Rm=0 and Cm=0 in LTspice

Bode Diagram with Rm=0

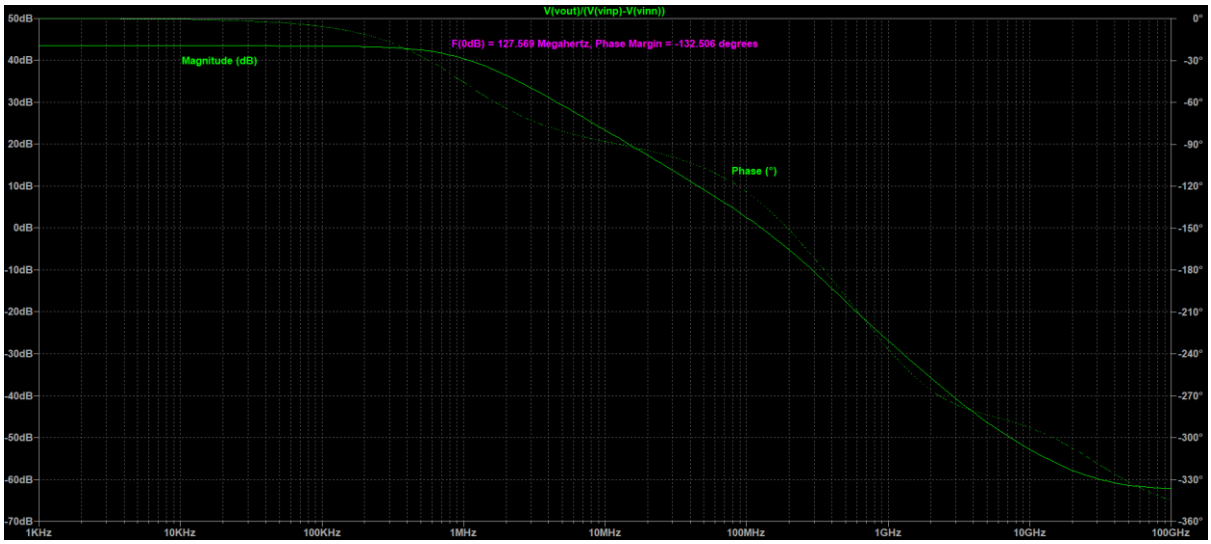


Figure 11 Frequency Response with Rm=0 in LTspice

Bode Diagram in LTspice

Figure 12 Frequency Response in LTspice

Case	PM [deg]
No compensation network	8.25
No compensation resistor	47.5
With both compensation components	89.45

Explain, analyse and interpret the results above (for each case, explain the effect it has on the plots and PM.

We know that the presence of the Miller capacitance decreases the value of the dominant pole and increases the value of the non-dominant one (pole splitting). For Cm=Rm=0, we don't have this pole splitting and that's why here we can see that the dominant pole is around 10MHz rather than 1MHz like we saw previously on the frequency response analysis. Because the dominant pole is at a higher frequency, we have multiple -90 phase shift before achieving a gain of 1 which means that the phase margin is very low. Also, we don't have the zero introduced by the Miller capacitance.

We can see around 3GHz that the phase doesn't do a full -90 phase shift caused by p1, this is due to the presence of the zero z1 (pole/zero doublet).

With Rm=0, we can see that this time, by adding a Miller capacitance, the bandwidth is reduced compared to the previous case. This is because the capacitance puts the dominant pole back at lower frequency. This improves the phase margin compared to the previous case because there are

less poles encountered thus less -90 phase shifts. Now, in the absence of Rm, z2 is an unstable positive zero (around 100MHz). As a result, both p3 and z2 induce -90° to the phase, which reduces the phase margin to 47.5. Also, this zero explains why we have such a steep phase shift as well as a final phase which is much lower than the previous case.

With Cm and Rm, we find the previous frequency response, which was explained and interpreted in point A. The phase margin is close to 90°, which is what we expected given that z2 is now negative. This zero, added by the Miller capacity, also compensates the effect of pole 3 which explains why we can expect 90° for the PM.

B. Noise contribution in LTspice

Simulate the output-referred noise voltage power density $\overline{dv_{out,eq}^2}/\Delta f$ over an appropriate frequency range in LTspice. Then, insert the $\overline{dv_{out,eq}^2}/\Delta f$-plot below (use a logarithmic plot).

Plots:

Power Spectral Density referred to the output

Figure 13 Power Spectral density referred to the output

Explain, analyze and interpret the results above (what regions can you see in the plot, and why?).

Flicker noise is dominant at low frequencies and is inversely proportional to frequency (1/f), which explains the shape of the curve. As the frequency increases, the noise decreases rapidly and approaches zero. In addition, most of our transistors have large gate areas, which affect the overall noise characteristics. In Figure 13, the difference in the noise region is not easily distinguishable due to the large scale, but in Figure 14 the distinction becomes clearer and will be explained below.

Note: We have expressly taken a very wide bandwidth for Figure 13 to support the fact that white noise and thermal noise are not visible even at very high frequency. It also shows that flicker noise is the main noise in the OTA.

Simulate the input-referred noise spectral density by using the .NOISE option in LTspice. Also, by using LTspice, determine the total output integrated noise of the OpAmp. For that, take the integration bandwidth from 10 kHz to $10 \cdot f_{GBW}$. Furthermore, copy and paste the top 9 contributing elements using "View->SPICE Error Log" option and insert that list below.

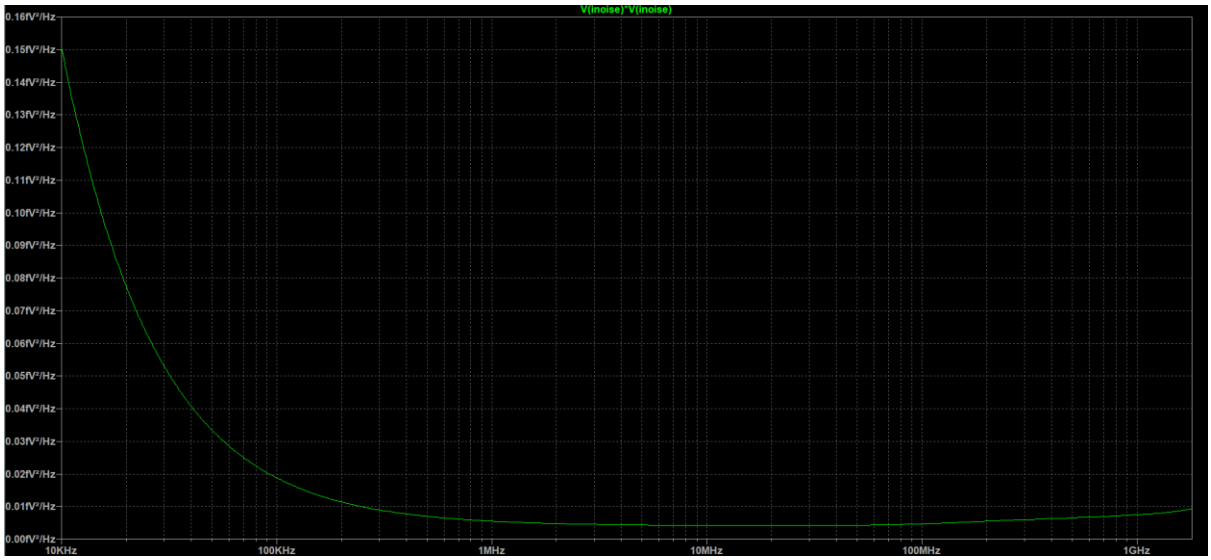


Figure 14 Power Spectral density referred to the input

Explain, analyse and interpret the results in above (what regions can you see in the plot, and why? + why is every transistor ranked the way it is for noise contribution).

out_totnvrms: INTEG(v(onoise))=0.00107747 FROM 10000 TO 1.8e+09

out_mp1nvrms: INTEG(v(mp1))=0.000577633 FROM 10000 TO 1.8e+09
out_mp2nvrms: INTEG(v(mp2))=0.000578732 FROM 10000 TO 1.8e+09
out_mp7nvrms: INTEG(v(mp7))=2.44136e-05 FROM 10000 TO 1.8e+09
out_mp8nvrms: INTEG(v(mp8))=1.04994e-05 FROM 10000 TO 1.8e+09
out_mp5nvrms: INTEG(v(mp5))=1.89833e-05 FROM 10000 TO 1.8e+09
out_mn6nvrms: INTEG(v(mn6))=3.81735e-05 FROM 10000 TO 1.8e+09
out_mn4nvrms: INTEG(v(mn4))=0.000512385 FROM 10000 TO 1.8e+09
out_mn3nvrms: INTEG(v(mn3))=0.000475094 FROM 10000 TO 1.8e+09
out_rmnvrms: INTEG(v(rm))=3.96679e-05 FROM 10000 TO 1.8e+09

In Figure 14, it is easier to distinguish because the scale is in fV²/Hz instead of pv²/Hz for Figure 13. This is normal since the noise is amplified by the OTA. The flicker noise, which dominates at low frequency, is inversely proportional to W*L. Most of our transistor have large gate areas which explains why we are in fV² scale. The white noise and the thermal noise, which appear around 60MHz, increase the noise since these noises are directly proportional to the frequency.

Regarding the values of each transistor with respect to the output, it's possible to see that the values of Mn6, Mp5,7,8 as well as the noise of Rm are very small compared to the others. This is explained

by the fact that the noise of Mp1,2 and Mn3,4 comes from the first stage and therefore, seen from the output, this noise is amplified. The values for the 4 transistors are more or less the same, since all 4 have the same length and the flicker noise is inversely proportional to WL and, as we can see on the graph, contributes most of the noise. Mn6's noise is greater than the other transistors in the second stage and the current mirror because its length is much shorter.

C. Linearity

Explain why gain compression occurs when you increase the input voltage.

Gain compression occurs when the input voltage amplitude increases to the point where the amplifier leaves the linear regime. In that case, the transistors saturate, leading to a decrease in gm and an increase in nonlinear effects. Gain decreases as the amplifier cannot keep up proportionally with increasing input amplitude. But it is also directly dependent on harmonic distortion. In fact, a sin wave has harmonic distortion that is directly proportional to the order of the distortion. The ratio at the second harmonic and the signal at the fundamental frequency is defined as the second harmonic distortion $HD_2 = \frac{A_1 K_2}{2K_1}$. And the same with $HD_3 = \frac{A_1^2 K_3}{4K_1}$. Then we can see that increasing the input amplitude makes the nonlinear behavior more excited. With $K_2 = \frac{1}{2!} \cdot \frac{\partial^2 f(s_{IN})}{\partial s_{IN}^2}\Big|_{s_{IN}=S_{IN}}$ and $K_3 = \frac{1}{3!} \cdot \frac{\partial^3 f(s_{IN})}{\partial s_{IN}^3}\Big|_{s_{IN}=S_{IN}}$. Then for $K_3\ and\ K_1$ with opposite sign the fundamental response that is equal to $K_1 A_1 + \frac{3}{4} K_3 A_1^3$ leads to compression as the cubic term reduces the output amplitude relative to the input. It is important to note that the second harmonic (every even harmonic) are cancelled by the differential operation of the amplifier.

Assume an input voltage is applied such that the full voltage swing (as calculated) is utilized. Does increasing the input voltage still increase the output voltage at this point? Explain.

When the full voltage swing is reached, the amplifier's output voltage reaches its maximum limit. At this point, the amplifier can no longer increase the output, even if the input continues to increase. The output then stabilizes on a plateau around the value of the max output swing, remaining constant despite the increase in input. This is due to the limits of transistors, which can no longer supply additional current or voltage. This plateau marks the end of the amplifier's linear behavior.

BONUS: I didn't set up my large-signal simulation parameters correctly and my gain vs Vin plot is first rising, then stays flat and finally it starts dropping. What would I have expected to see and what could have gone wrong?

The $gain\ vs\ V_{in}$ graph should increase as the transistors enter their active region, remain flat in the linear range and drop as the amplifier enters saturation. This beginning to fall may be due to V_{in} exceeding the common mode range, which causes the transistors to leave their active region and therefore creates compression that reduces gain. Incorrect biasing can also place transistors outside their intended operating point.

Conclusion (10 points):

Conclude your experiment by filling the editable fields in the performance table depicted below

Metric	Units	Specification	from hand-calculations	MATLAB	LTspice
DC gain	magnitude	316.227766	316.227766	191.205	149.108
DC gain	dB	50	50	45.63	43.47
Gain-Bandwidth frequency f_{GBW}	MHz	180	180	166.654	147.198
Dominant pole frequency f_{dom}	kHz	569.209	569.209	871.6	987.191
PM	°	> 70	90	83.1	89.45
$V_{in,cm,max} - V_{in,cm,min}$	V		0.499	0.494	0.504
$V_{out,max} - V_{out,min}$	V	> 0.7	0.944	0.922	0.9145
P_{diss}	mW		1.831	1.8	1.858
$\overline{v_{out,eq}^2}$ (output-referred noise)	V_{rms}				0.00107747 nVrms

Comment about the deviations between hand calculation, MATLAB and LTspice values found above. Conclude what the causes of such deviations are.

First regarding the differences between MATLAB and LTSpice, this is due to LTSpice being more accurate. We can see that in the frequency response where we have poles and zeros appearing at higher frequency, which we didn't consider for MATLAB. Also, the expressions of the poles are more accurate (more parasitic effects) as well as for the gain and so on…

Now concerning the difference between hand calculations and MATLAB, we can first see a huge difference in the DC gain. We can explain by the following facts: first we made some assumptions on the gain in the hand calculations, and we used the more accurate expression in MATLAB.

Assumptions	Consequences
$L_5 \gg L_6$	$A_{V2} = 16.4227 \approx \frac{gm_6}{gds_6}$
$L_{1,2}, L_{3,4}$ are long	$gds_{1,2} \approx gds_{3,4} \rightarrow A_{V1} = 19.2555 \approx \frac{gm_{1,2}}{2 \cdot gds_{1,2}}$

These assumptions affected mostly the gain of the second stage.

For the first stage, it is another assumption we made that affected the gain. The assumption is that the Vds doesn't change that much the properties of the transistors so we can use the graphs derived with Vds=0.55V. This turned out to be wrong because the gds varies with Vds in a non-negligible way.

We can say that these assumptions aren't good. The gain is far from what we expected, and this gain affects also other parameters of the design. In fact, the fGBW depends on the DC gain and the dominant pole. We know that the DC gain changed because of the assumptions we made but the value of the dominant pole also changed. The dominant pole depends on the gds of the transistors of the first stage and we designed everything from the graphs with Vds=0.55V. As stated above, the gds changes with Vds so this assumption is one of the causes of the difference.

However, it is not the only thing that influenced the fGBW, the dominant pole and the PM. There is also the fact that we didn't consider the parasitic capacitances, and this changes the value of every pole.

Other than that, the differences are small, which means the assumptions we made are good and can be explained with the fact that we aren't that accurate when doing hand calculations.

If you have results which are not passing the specifications: conclude for each of those results what the cause is and what you need to do in order to make it pass, if you were repeating this experiment.

Regarding the gain, we would use the more accurate expression for the second stage and for the first stage, change the graphs with the right Vds during the design because the assumption on the gain for the first stage is accurate enough, it is the values of gds that are problematic.

Changing that would also improve the values of the dominant pole as well as the fGBW. But it is not enough. We didn't consider that our fGBW is close to the higher frequency poles and zeros we usually neglect during design. If we were repeating the design, we would take that into account.

Also, the parasitic capacitances in the poles change the overall frequency response thus we would try the experiment with this new knowledge.

Appendix:

Previously, you were expected to include your MATLAB code and LTspice netlist here, but now we changed it so that you must upload them in the Canvas assignment. Read the description of the assignment for details on exactly what files are needed!