IRELE - MA1 Electrical Engineering

ELEC-Y418

CMOS Project

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0.1 Core Assignement

We implement a 5-stage Current-Starved Ring Oscillator (CSRO), as shown in Figure 1. This oscillator generates a periodic waveform whose frequency can be tuned via a reference current I_{ref}.

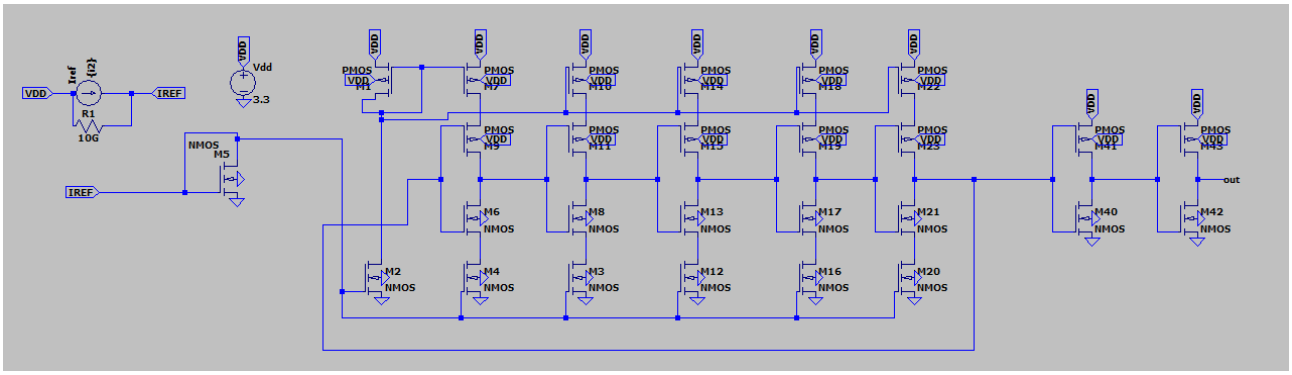

Figure 1: Schematic of the 5-stage Current-Starved Voltage-Controlled Oscillator

The main building blocks and their roles are described below.

- **Mp/Mn (Inverter Pair):**
  - Each stage consists of a CMOS inverter composed of a PMOS and NMOS transistor.
  - The inverter regenerates and restores logic levels while introducing a propagation delay per stage, contributing to oscillation.
  - These transistors are sized with $\text{W/L}_\text{n} = 6\,\mu\text{m}/0.45\,\mu\text{m}$ and $\text{W/L}_\text{p} = 12\,\mu\text{m}/0.45\,\mu\text{m}$ to balance drive strength due to carrier mobility differences ($\mu_n > \mu_p$).
  - The input capacitance of each inverter contributes to the total load capacitance C_{par}, which affects delay.

M1/M2 (Starved Current Sources):

- M1 (PMOS) and M2 (NMOS) are placed in series with the inverter to limit current from above and below, respectively.
- These "starving" devices are biased by a shared control voltage V_{ref}, derived from a current mirror.
- When biased in saturation, they regulate current to each inverter, effectively controlling the oscillation frequency.
- The delay per stage is approximately:

$$\tau \propto \frac{C_{\text{par}} \cdot V_{\text{sw}}}{I_{\text{ref}}}$$

  where V_{sw} is the voltage swing and C_{par} includes inverter input and wiring capacitance.

M5 (Diode-Connected NMOS):

- Provides a self-biased node for the current mirror supplying I_{ref}.
- Functions as a voltage clamp with:

$$V_{\text{ref}} \approx V_{\text{th}} + V_{\text{ov}}$$

  ensuring a stable gate bias for the starved devices (M1/M2).

Bias Mirror:

- The biasing network uses two scaled current mirrors to replicate the reference current:
  - A PMOS mirror with M1 (diode-connected) and five copies: M7, M10, M14, M18, M22.
  - An NMOS mirror with M2 (diode-connected) and five copies: M3, M4, M12, M16, M20.
- The reference transistors M1 and M2 are sized with $W = 3\,\mu\text{m}, L = 0.35\,\mu\text{m}$, while the copies use $W = 6\,\mu\text{m}, L = 0.45\,\mu\text{m}$.
- This gives a mirror ratio of approximately:

$$\frac{(W/L)_{\text{copy}}}{(W/L)_{\text{ref}}} \approx \frac{13.33}{8.57} \approx 1.56,$$

  meaning each stage receives roughly $1.5 \times I_{\text{ref}}$.
- This intentional current scaling increases the charge/discharge current per stage, increasing the oscillation frequency while keeping linearity.

Frequency Formula and Parameter Extraction

The oscillator's frequency follows the analytical model of a current-starved ring oscillator:

$$f = \frac{I_{\text{ref}}}{2N \cdot C_{\text{par}} \cdot V_{\text{DD}}},$$

where:

- I_{ref} is the reference current
- $N = 5$ is the number of inverter stages
- $V_{\text{DD}} = 3.3\,\text{V}$ is the supply voltage
- C_{par} is the effective parasitic capacitance per stage

Linearity Analysis

The oscillator was tested across a reference current range from 1µA to 32µA. A linear fit $f_{\text{fit}}(I) = m \cdot I$ was applied to the frequency data, yielding:

$$m_{\text{fit}} \approx 2.343 \times 10^6 \, \frac{\text{Hz}}{\mu\text{A}}.$$

The relative deviation from this ideal fit is:

$$\delta_i = \frac{f_i - f_{\text{fit}}(I_i)}{f_{\text{fit}}(I_i)}.$$

I (μA)	f_i (Hz)	f_{fit} (Hz)	δ_i (%)
1	2.25861×10^6	2.343×10^6	-3.6
2	4.48254×10^6	4.686×10^6	-4.3
4	8.92045×10^6	9.372×10^6	-4.8
8	1.78739×10^7	1.874×10^7	-4.6
16	3.61929×10^7	3.749×10^7	-3.5
32	7.48232×10^7	7.498×10^7	-0.2

All errors are under 5%, demonstrating excellent linearity.

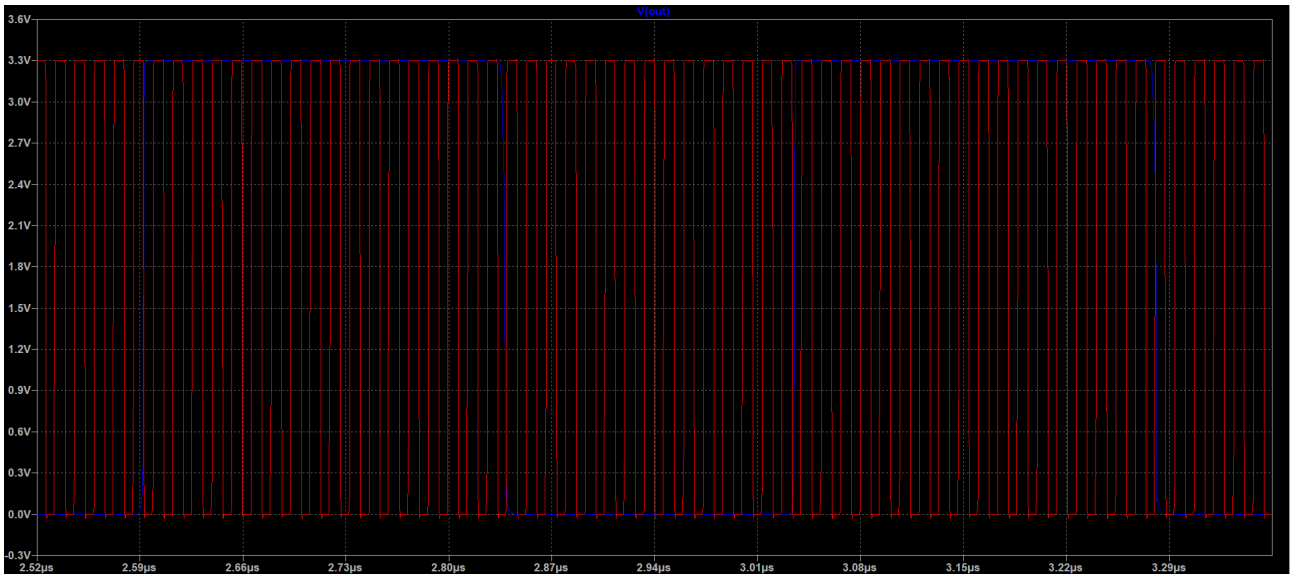

Figure 2: Simulated square waveform at $I = 1\,\mu$A (blue) and $I = 32\,\mu$A (red)

0.2 Sawtooth Generator

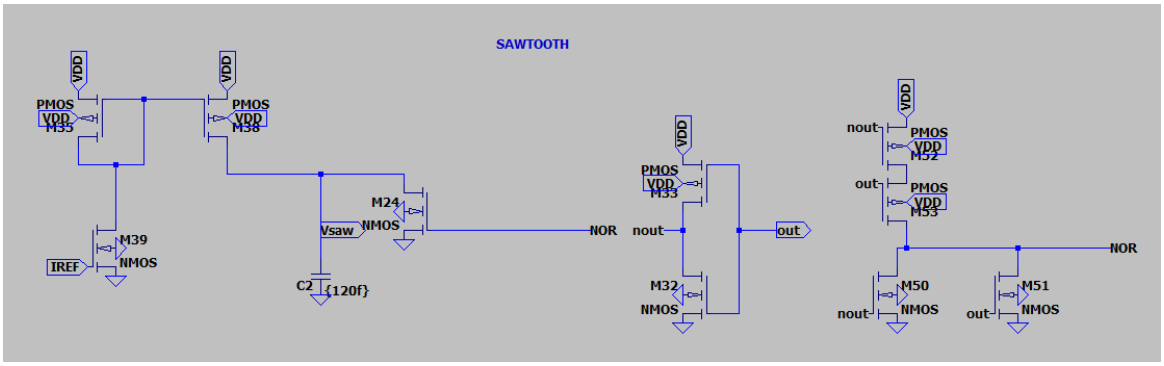

Figure 3: Sawtooth generator circuit

The sawtooth generator is driven by the square wave output of the ring oscillator. The purpose of this block is to generate a ramp voltage that increases linearly between each falling edge of the oscillator output, and resets on every falling edge.

Operating Principle

- A current mirror composed of transistors M5–M39 and M35-M38 biases a constant current I_{ref} into a capacitor $C_2 = 120\,\text{fF}$.
- This results in a linear voltage ramp across V_{saw}, since:

$$I = C \cdot \frac{dV}{dt} \Rightarrow V_{\text{saw}}(t) = \frac{I_{\text{ref}}}{C_2} \cdot t \quad \text{t is the time during a rising ramp}$$

- In our case the equation above is not really justified. But this due to the fact that we size transistors in order to minimize the capacitance value then I is also modified in the current mirror. But behaviour of the sawtooth follow this equation properly
- The ramp is periodically reset by a falling edge of the oscillator output through the NMOS switch M24, which pulls V_{saw} to ground.
- The falling edge detection is implemented using a NOR-based edge detector (M50 to M53), which produces a short pulse whenever the output of the oscillator transitions from high to low.

Simulation Results

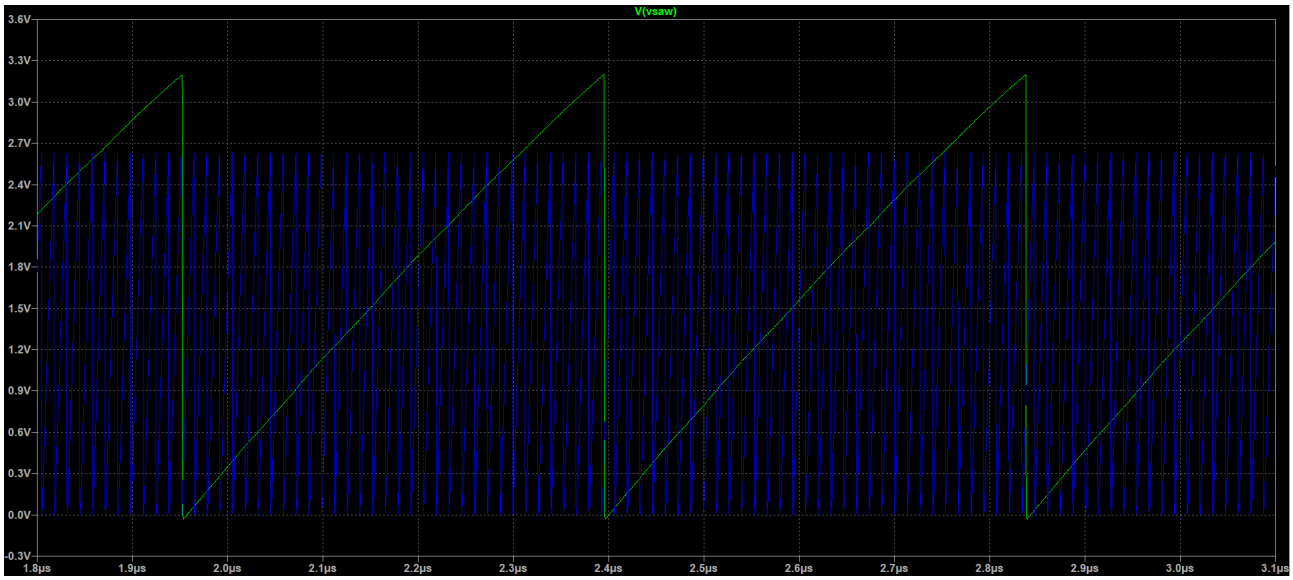

Figure 4: Simulated sawtooth waveform at $I = 1\,\mu$A (green) and $I = 32\,\mu$A (blue)

0.3 PWM Square Wave Gennerator

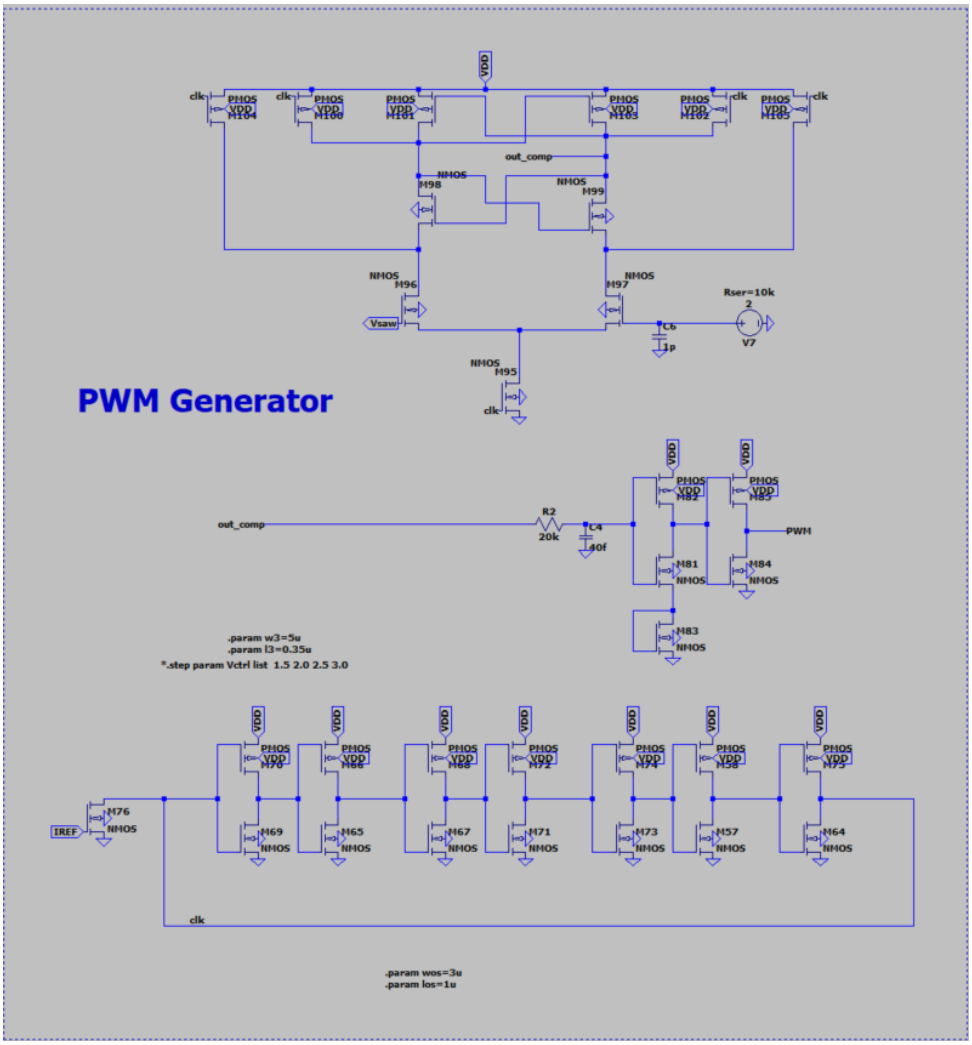

Figure 5: Schematic of the PWM generator.

As you can see, the structure is to use a latch comparator where the sawtooth and a given DC reference are the two signals to compare. For this I need to use a clock ($\approx 330MHz$) that is much faster than the frequency of the sawtooth signal. The clock role is that the comparator makes a decision above or under (3.3V or 0V) at each rising. The problem is that when it is under there is a reset, then when it is under, we have the square wave of the clock. Then to arrange this, we have to go trough a low pass filter that cuts the frequency of the clock. Then to make a clean square wave we go trough two inverter. Concretely, its PMOS (M82) has a width much larger than the NMOS (M85), while its pull-down contains an extra diode-connected NMOS at the bottom. That diode-connected device holds the inverter's source node at about one diode drop above ground, forcing the input gate voltage to rise by the same amount before VGS turns on. By sizing PMOS 82 much stronger than NMOS 85, the inverter's Vout vs Vin curve shifts to the right—so it remains off until the filtered level crosses ≈2.1 V—and then snaps cleanly from 0 to 3.3 V. A second, symmetrically sized inverter then sharpens the edges and delivers a robust, rail-to-rail 0–3.3 V square wave suitable for any downstream digital logic.

Simulation Results

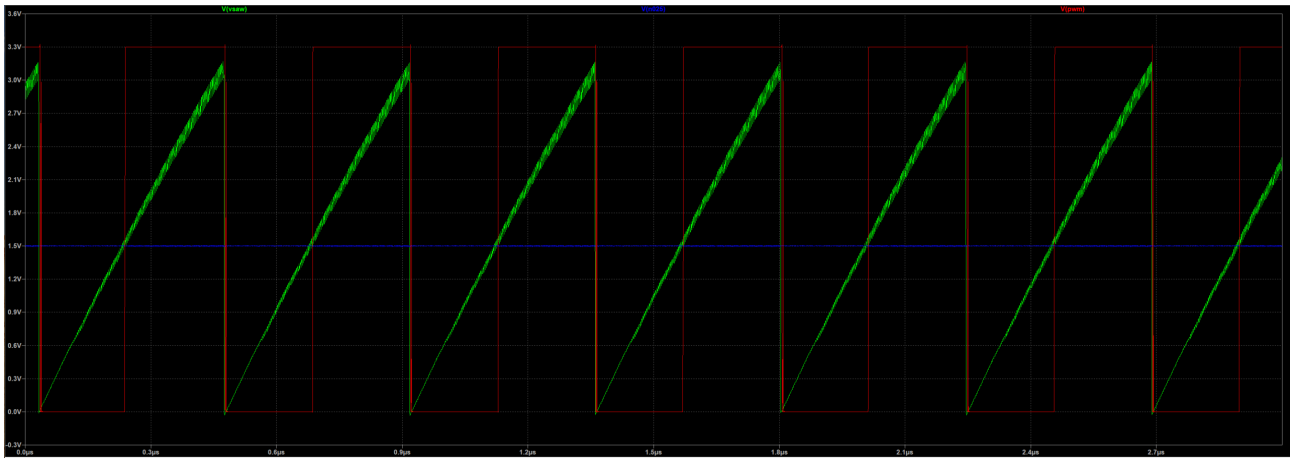

Figure 6: Output of the comparator for $V_{ctrl} = 1.5V$ in red, sawtooth (green) and V_{ctrl} (blue)

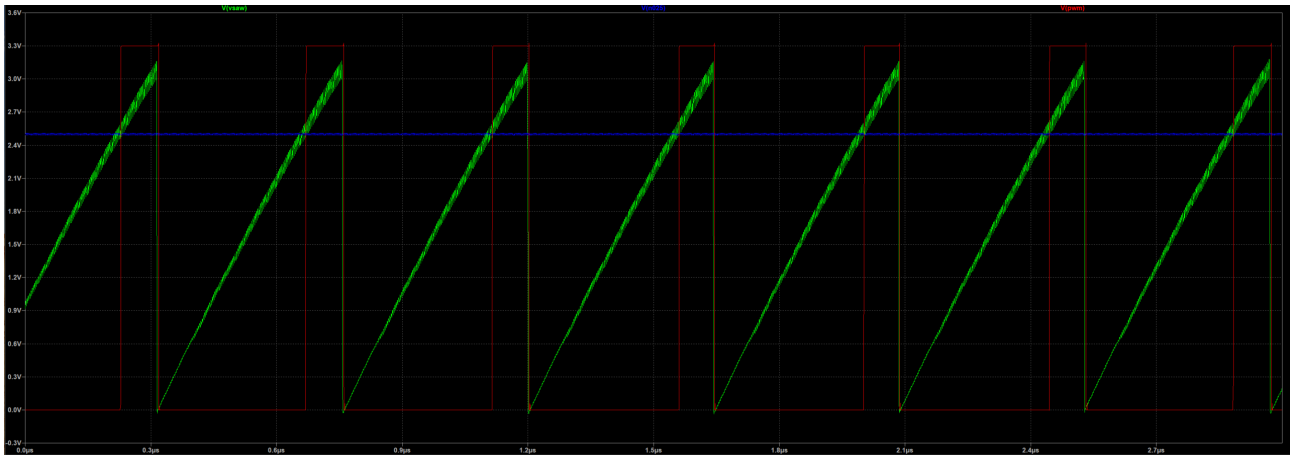

Figure 7: Output of the comparator for $V_{ctrl} = 2.5V$ in red, sawtooth (green) and V_{ctrl} (blue)

We can also observe that the sawtooth ramp becomes slightly noisy when fed into the comparator. However,this added ripple does not have an impact on the output.

0.4 DAC

0.4.1 Digital-to-Analog Converter (DAC)

The DAC is implemented as a binary-weighted current-steering network. Each digital bit is represented by a DC voltage source in series with a 10 kΩ internal resistor. To prevent loading the reference, the reference current I_{ref} is first mirrored through a PMOS current mirror. The mirrored current then feeds an array of NMOS transistors, each sized according to

$$W_i = 2^i \times 0.8\,\mu\text{m},$$

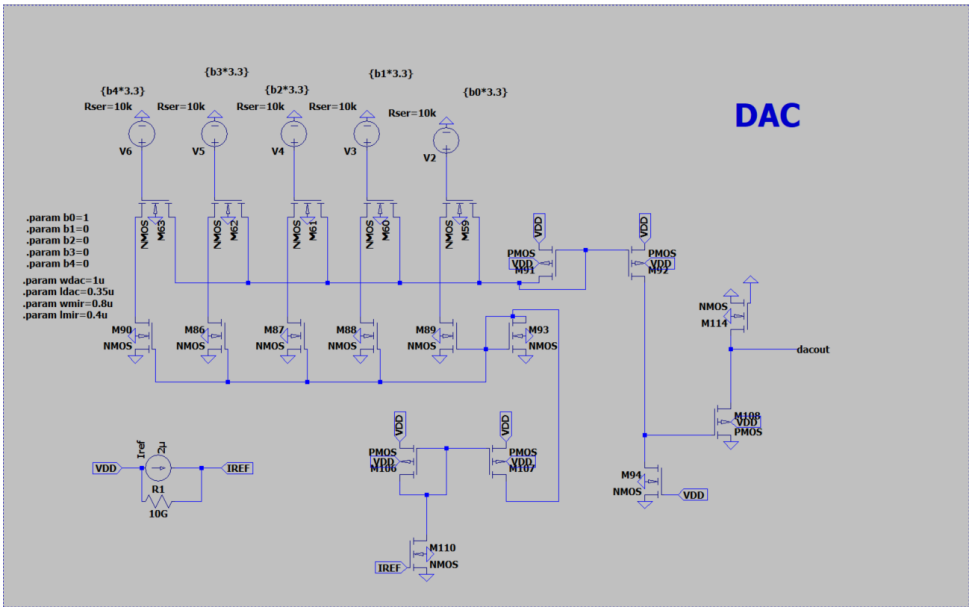

Figure 8: Schematic of the DAC Circuit

with i the bit index (MSB has $i = 4$). This binary weighting ensures that each successive bit conducts half the current of the previous one, producing an output voltage proportional to the weighted digital code.

At the DAC output, a complementary NMOS–PMOS pair tied to ground and V_{DD} forms a precision resistor network, buffering the summed current into a stable control voltage for the oscillator. The sizing and biasing are chosen to guarantee a range between 0.5 MHz and 100 MHz.

Simulation Results

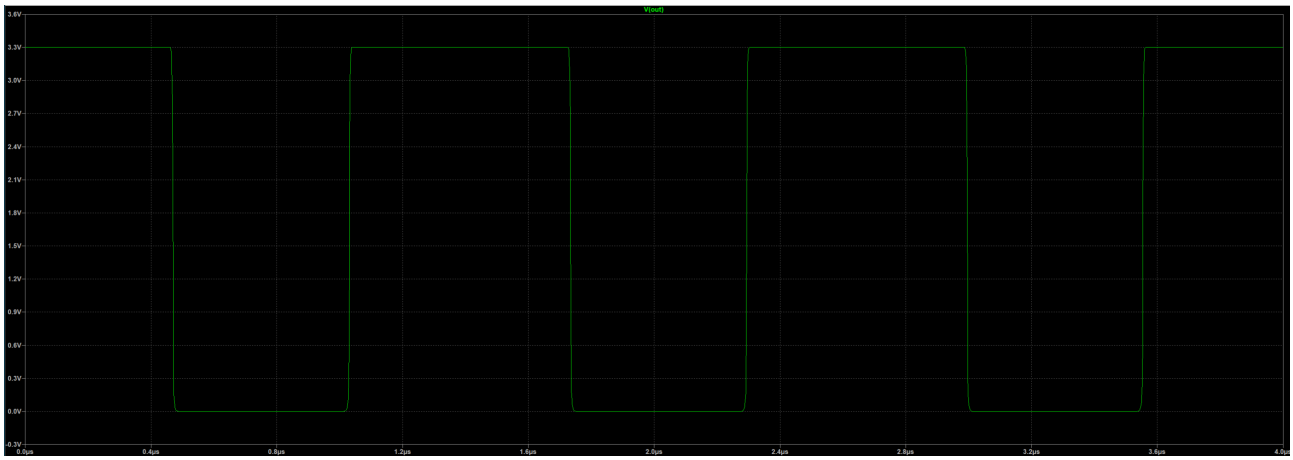

Figure 9: Output of the oscillator for 10000

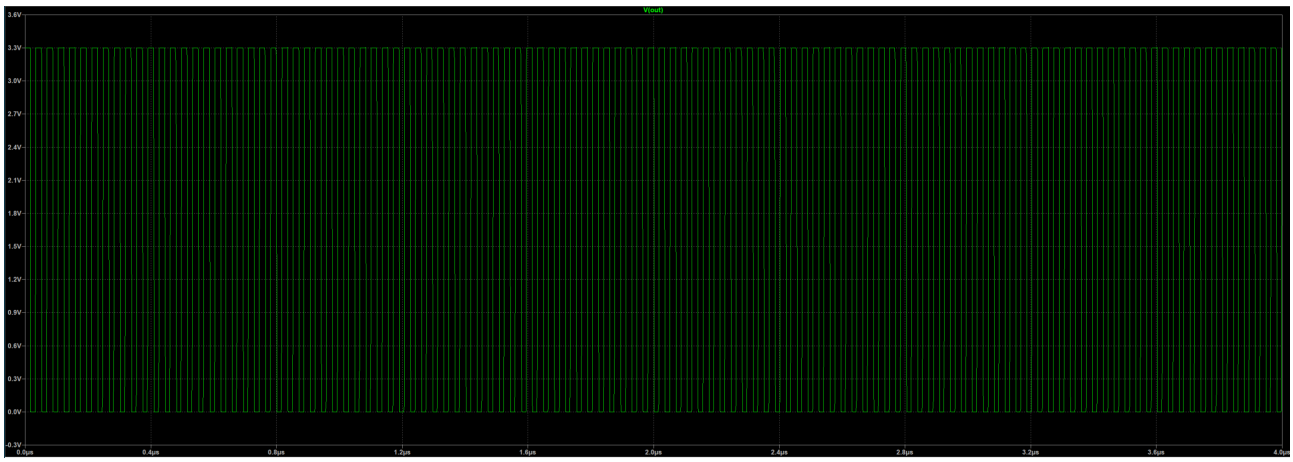

Figure 10: Output of the oscillator for 00100

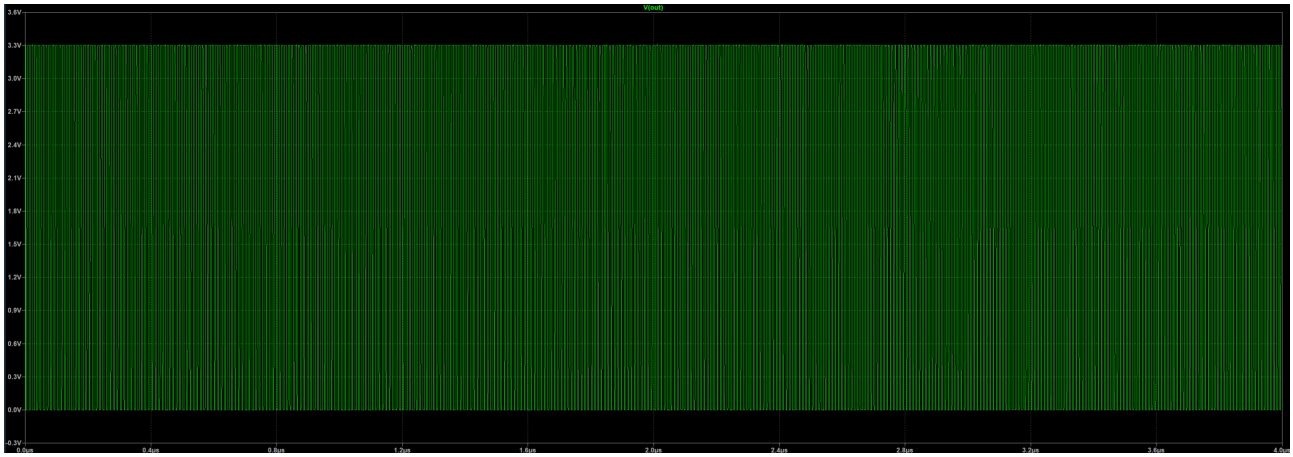

Figure 11: Output of the oscillator for 11111

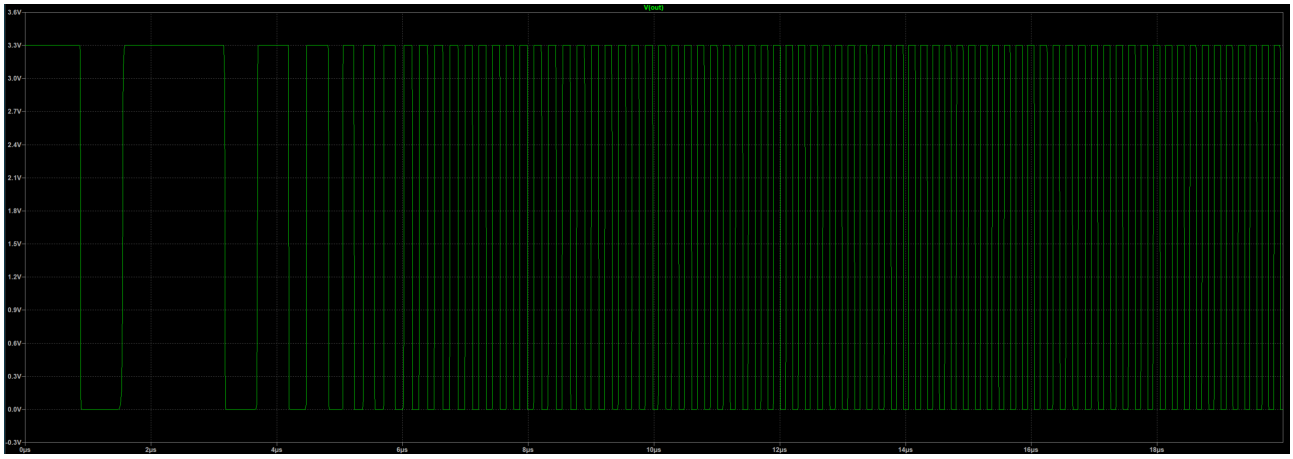

Figure 12: Oscillator output for varying DAC bit patterns: each trace corresponds to a different bit set to '1', demonstrating the change of frequency made by the DAC.