

# ALEXANDER BOLINSKY

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## TECHNICAL STRENGTHS

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Languages	English (native), Japanese (self-taught, N3)
Programming Languages	C++, C, x86 assembly, Python, Verilog, VHDL, JavaScript
Tools	Linux, ROS, ALICA, Git, CMake, Catkin, GDB, Google Test, Gazebo

## ENGINEERING & RESEARCH EXPERIENCE

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Rapyuta Robotics Software Engineer Intern	February 2018 - Current Tokyo, Japan
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- Lead software engineer in developing an autonomous team of omni wheel-equipped robots that collaborate in gathering cubes from the environment and stacking them into a tower. Collaboration and robust team dynamics were achieved using ALICA, and localization was achieved via sensor fusion of odometry and VIVE tracker position estimates. Presented at iROS 2018.
- Designed and implemented core components of an autonomous warehouse robot fleet, including the robots' general and contextual behaviour and integration of range sensors into the costmap for local planning.

LockerDome Web Developer	June 2016 - July 2017 St. Louis, Missouri
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- Developed and tested a custom high-performance database. This involved a detailed understanding of Linux and its system calls, the memory and caching hierarchy, hand-coding architecture-specific x86 assembly, implementing a custom memory manager, asynchronous socket programming, data (de)serialization, and heavy unit testing and profiling. Additionally worked on static type-checking for a front-end javascript framework compiler, implemented a lexer/parser for formatting articles, contributed to the api layer, and connected our ad server with publishing clients.

Institute of Electronics & Electrical Engineers Student Branch Co-President & Treasurer	February 2014 - May 2016 St. Louis, MO
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- Designed and built a force/haptic feedback glove prototype for virtual reality applications. Designed and constructed a "Segway" that utilizes a 9 DOF IMU sensor, an Arduino, and filter and error algorithms for self balancing. Collaborated with several members on projects involving developing for the Oculus Rift, hardware and software design and construction, and 3D printing.

Digital Systems Laboratory Student	August 2014 - December 2014 St. Louis, MO
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- Designed and implemented a ten band stereo audio equalizer in verilog and deployed the design on an FPGA. Components of the design include a Finite Impulse Response (FIR) filter for filtering the ten frequency bands, a Serial Peripheral Interface (SPI), the equalizer itself, and a LabVIEW application/GUI.

## EDUCATION

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Washington University in St. Louis B.S. in Computer Science & Engineering	2012 - 2016
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### Leadership

Judge at GlobalHack VI Million-Dollar Hackathon (2016)

IEEE · Co-President & Treasurer of Student Branch (2014 - 2016)

Men's Squash Team · Co-Captain, Named Harrow Squash Player of the Men's National Championship Team (2014)

### Awards

Third Place at Discovery Competition at Washington University in St. Louis (2017)

Top College Team at GlobalHack V Hackathon (2015)