*IPC-D-279相关，可靠性设计*

*Reliability* is the ability of a product to function under given conditions and for a specified period of time with out exceeding acceptable failure levels.

The （product） life cycle begins at the component level (including the printed

board) and continues through the assembly level; the life cycle includes exposure to the following environments:

• components

• assembly/process

• testing

• storage

• transportation

• operating

Defining the Product Environment

For each environment, in 1.2.3, it is critical to identify, characterize and quantify the parameters listed below:

• Temperature Range

• Time at Temperature

• Temperature Rate of Change

• Kind and number of temperature cycles

• Duty Cycle

• Humidity (moisture) exposure

• Atmospheric pressure conditions (earth, space, both)

• Vibration and shock

• ESD, EOS（Exceeding of Stress，超出绝对指标失效）, EMC, EMI and high voltage exposures and requirements

• Chemical exposures (flux, solvents, salt spray, NBC, decontamination, etc.)

• Radiation (Ionizing, light, UV)

• Contamination (dust, oil, paper)

• Pressure conditions

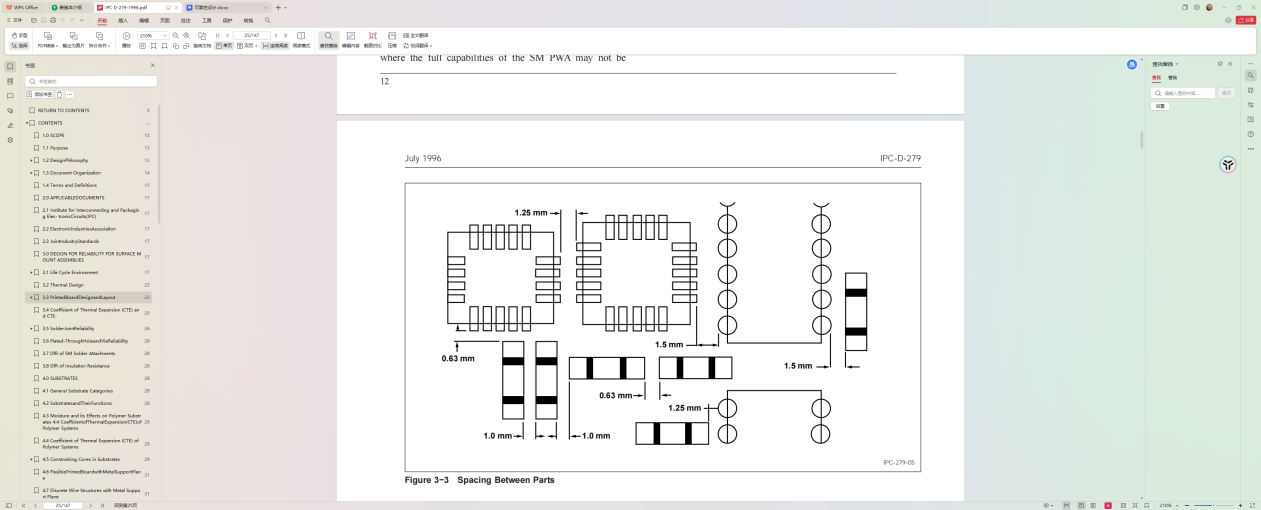
EMC is the ability of electronic systems to operate in the

intended electromagnetic environment at designed levels of performance and efficiency.

3.3.6 Printed Board Trace Widths and Spaces

Minimum trace widths should be reviewed keeping in mind the influence of etching tolerances, undercutting, ‘‘Mouse bites,’’ and plated grain size as well as the possibility for electromigration due to current density, Joule heating and subsequent conductor temperature rise. Minimum trace spacings should be reviewed keeping in mind the influences of DC voltage and possible electrochemical migration, AC voltage and possible corona leakage currents, high humidity and possible electrochemical migration, low air pressure and possible corona leakage currents/premature voltage breakdown, and conductive or corrosive contamination from the ambient. See IPC-D-275,

IPC-SM-782, and IPC-TR-476 and IEC 664.



Where lower junction temperature Tj is required, consider the following avenues particularly applicable to SMT: thermal vias, thermally conductive adhesives from component to printed board, and power and ground planes included in the thermal design. In addition, consider the following moves: sensitive components ‘‘upstream’’ of power dissipaters, power dissipaters further apart to reduce power density, power dissipaters closer to cold wall (edge of card if card clamps are used), and power dissipaters ‘upstream’ of tall components.

Long, tall components such as connectors are ideally placed parallel to the airflow. Placement of these components perpendicular to the airflow results in the generation of recirculation cells which reduce the heat transfer from heat dissipaters or which increase heat transfer to heat sensitive components.

General Substrate Categories Interconnect substrate technologies can be divided into the following categories:

1. Organic based printed wiring board

2. Discrete wiring printed board

3. Ceramic based printed circuit board (thick film, co-fired)

4. Ceramic based printed circuit board (thin film)

Categories 1-3 above can be further classified:

Type 1—Single sided

Type 2—Double sided

Type 3—Multilayer with blind or buried vias

Type 4—Multilayer with blind and/or buried vias

Type 5—Multilayer metal-core board without blind or

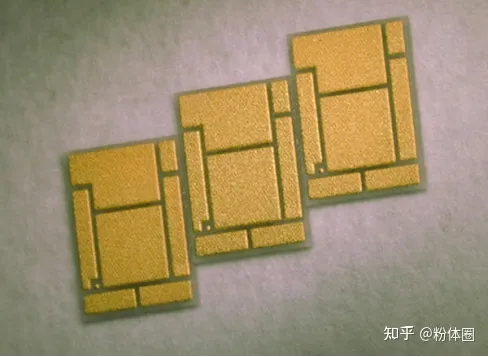
buried vias

Type 6—Multilayer metal-core with blind and/or buried vias

Type 7—Rigid-flex multilayer without blind or buried vias (organic only)

Type 8—Rigid-flex multilayer with blind and/or buried vias (organic only)

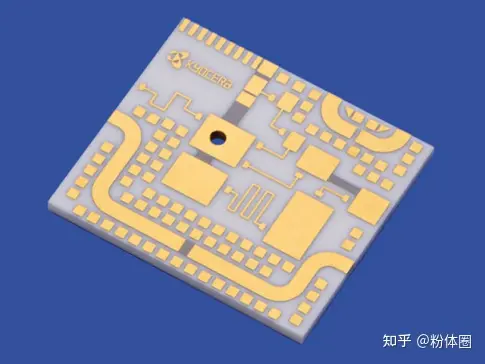
**一、厚膜法**  
厚膜印刷陶瓷基板（ThickPrintingCeramicSubstrate，TPC）是指采用丝网印刷的方式，将导电浆料直接涂布在陶瓷基体上，然后经高温烧结使金属层牢固附着于陶瓷基体上的制作工艺。根据金属浆料粘度和丝网网孔尺寸不同，制备的金属线路层厚度一般为几微米到数十微米的膜层（提高金属层厚度可通过多次丝网印刷实现）。



厚膜金属化基板

**优缺点：**由于丝网印刷工艺限制，TPC基板无法获得高精度线路，因此TPC基板仅在对线路精度要求不高的电子器件封装中得到应用。不过厚膜电路虽然精度粗糙（最小线宽/线距一般大于100μm），**但其优势在于性能可靠，对加工设备和环境要求低，具有生产效率高，设计灵活，投资小，成本低，多应用于电压高、电流大、大功率的场合。**  
**基材：**厚膜集成电路最常用的基片是含量为96％和85％的氧化铝陶瓷；当要求导热性特别好时，可采用氧化铍陶瓷。氮化铝陶瓷虽然导热性能也很好，但大多数金属对氮化铝陶瓷的润湿性并不理想，因此使用氮化铝作为基片材料时需要特殊工艺支持，常见的手段有：①是利用玻璃料作为粘结相使金属层与AlN层达到机械结合；②是添加与AlN能够反应的物质作为粘结相，通过与AlN反应达到化学结合。  
  
**导电浆料：**厚膜导体浆料的选择是决定厚膜工艺的关键因素，它由功能相（即金属粉末，粒径在2μm以内）、粘结相（粘结剂）和有机载体所组成。常见的金属粉末有Au、Pt、Au/Pt、Au/Pd、Ag、Ag/Pt、Ag/Pd、Cu、Ni、Al及W等金属，其中以Ag、Ag/Pd和Cu浆料居多。粘结剂一般是玻璃料或金属氧化物或是二者的混合物，其作用是连结陶瓷与金属并决定着厚膜浆料对基体陶瓷的附着力，是厚膜浆料制作的关键。有机载体的作用主要是分散功能相和粘结相，同时使厚膜浆料保持一定的粘度，为后续的丝网印刷做准备，在烧结过程中会逐渐挥发。

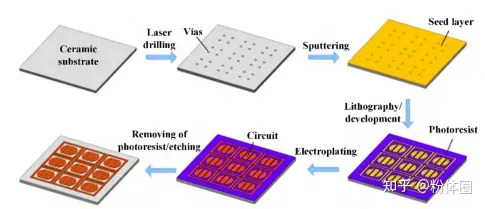
**二、薄膜技术**  
薄膜技术（ThinFilmCeramicSubstrate，TFC）是指采用蒸镀、光刻与刻蚀等方法制备所需材料膜层的技术，薄膜的含义不只是膜的实际厚度，更多的是指在基板上的膜产生方式。厚膜技术是“加法技术”，而薄膜技术是“减法技术”。**使用光刻与刻蚀等工艺使薄膜技术得到的图形特征尺寸更小，线条更清晰，更适合高密度和高频率环境。**



微波集成电路（MIC）基板：高纯度(99.6%)氧化铝基板

薄膜电路的线条细（最小线宽2μm），精度高（线宽误差2μm），但也正因“细小的线”不容起伏，薄膜电路对基片的表面质量要求高，所以用于薄膜电路的基板纯度要求高（常见的是99.6%纯度的氧化铝），同时我们知道陶瓷的高纯度也就代表的加工难度及成本的攀升。此外，细小的线，使其应用于大功率大电流存在较困难，因此主要应用通信领域小电流器件封装。

**三、直接镀铜**  
直接镀铜（Directplatingcopper，DPC）工艺是在陶瓷薄膜工艺加工基础上发展起来的陶瓷电路加工工艺。区别于传统的厚膜和薄膜加工工艺，它的加工更加强化电化学加工要求。通过物理方法实现陶瓷表面金属化以后，采用电化学加工导电铜和功能膜层。

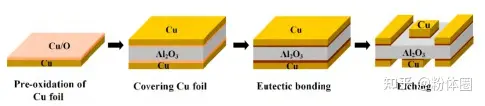


DPC陶瓷基板制备工艺

**工艺简述：**激光在陶瓷基片上制备通孔（利用激光对DPC基板切孔与通孔填铜后，可实现陶瓷基板上下表面的互联，从而满足电子器件的三维封装要求。孔径一般为60μm~120μm），随后利用超声波清洗陶瓷基片；采用磁控溅射技术在陶瓷基片表面沉积金属种子层(Ti/Cu)，接着通过光刻、显影完成线路层制作；采用电镀填孔和增厚金属线路层，并通过表面处理提高基板可焊性与抗氧化性，最后去干膜、刻蚀种子层完成基板制备。

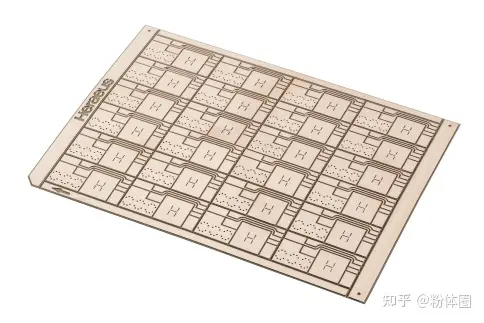
与其他陶瓷表面金属化方法相比，DPC工艺操作温度低，一般在300℃以下，降低了制造工艺成本，同时有效避免了高温对材料的不利影响。DPC基板利用黄光微影技术制作图形电路，线宽可控制在20～30μm，表面平整度可达3μm以下，图形精度误差可控制在±1%之内，非常适合对电路精度要求较高的电子器件封装。其不足之处在于电镀沉积铜层厚度有限，电镀废液污染大，金属层与陶瓷间结合强度稍低。

**四、直接敷铜法**  
直接键合陶瓷基板，（DirectBondedCopperCeramicSubstrate，DBC）：直接敷铜法，在陶瓷表面(主要是Al2O3和AlN)键合铜箔的一种金属化方法。



DBC陶瓷基板制备工艺

其基本原理是在Cu与陶瓷之间引进氧元素，然后在1065~1083℃时形成Cu/O共晶液相，进而与陶瓷基体及铜箔发生反应生成CuAlO2或Cu(AlO2)2，并在中间相的作用下实现铜箔与基体的键合。因AlN属于非氧化物陶瓷，其表面敷铜的关键在于在其表面形成一层Al2O3过渡层，并在过渡层的作用下实现铜箔与基体陶瓷的有效键合。

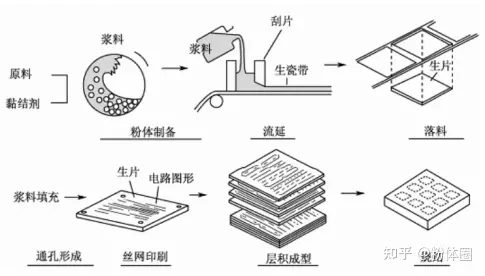


DCB-Al2O3基板（96%）

DBC热压键合的铜箔一般较厚，为100~600μm，具有强大的载流能力，可满足高温、大电流等极端环境的器件封应用要求，是电力电子模块中久经考验的标准器件，在IGBT和LD封装领域优势明显，不过，DBC表面图形最小线宽一般大于100μm，不适合精细线路的制作。

**五、活性金属焊接陶瓷基板**  
由于DBC陶瓷基板制备工艺温度高，金属陶瓷界面应力大，作为活性DBC的升级版本，活性金属焊接陶瓷基板（Active Metal Brazing Ceramic Substrate，AMB）的金属焊料中加入了少量活性元素（Ti、Zr、Hf、V、Nb或Ta等稀土元素制备），可大大降低铜箔与陶瓷基片间的键合温度。  
AMB基板依靠活性焊料与陶瓷发生化学反应实现键合，因此结合强度高，可靠性好。但是该方法成本较高，合适的活性焊料较少，且焊料成分与工艺对焊接质量影响较大。

**六、共烧法**  
共烧多层陶瓷基板因利用厚膜技术将信号线、微细线等无源元件埋入基板中能够满足集成电路的诸多要求，故在近几年获得了广泛的关注。  
共烧法有两种，一种是高温共烧（HTCC），另一种是低温共烧（LTCC），两者工艺流程基本相同，主要生产工艺流程均为浆料配制、流延生带、干燥生坯、钻导通孔、网印填孔、网印线路、叠层烧结以及最后的切片等后处理过程。两种共烧法虽流程大致相同，但烧结的温度却相差很大。



典型的多层陶瓷基板的制造过程

Some materials with higher glass transition temperatures (Tg) such as bismaleimides and polyimides, appear to absorb more water than the lower Tg materials, such as the epoxies.

Polymer systems expand with increasing temperature, demonstrating a glassy phase response below Tg with a CTE or α1 and a rubbery phase response above Tg with a much higher α2, typically 3 times α1. The transition from glassy phase to rubbery phase is gradual, but for most polymer substrates may be characterized by Tg, the glass transition temperature.

Component Selection Strategy The best strategy is to use parts that meet (as a minimum) JEDEC/EIA footprints and which have been qualified for the process flow including rework/repair.

Package Leadframe and Local Materials Leadframe and lead materials with low CTEs, e.g. Alloy42,

Kovar, etc., should be avoided for plastic surface mount components (PSMCs). Such materials lower the composite CTE of components creating large CTE-mismatches with FR-4 or similar printed board materials. Solderability problems have also been encountered with these lead materials.

应该避免用低膨胀系数材料制作plastic surface mount components (PSMCs)元器件。因为这些材料的膨胀系数与FR4相差很大。

Components to Avoid or to Use with Caution

• Printed board with Tg < 125°C （Tg玻璃化温度）

• Printed board with PTH and PTVs aspect ratio > 3:1

• Components not on the preferred parts list

• Components using obsolete technologies

• Components containing liquid and sealed only with rubber

• Components with rotating seals

• Components with thick silver or gold plating or paste as the solderable termination

• Components with corrosive or polar liquids

• Aluminum electrolytics with silver anode (obsolete technology)

• Components with exposed moving electrical contacts

• Electro-Mechanical connections between contact finishes of tin and gold (dissimilar metals)

• Film resistors trimmed more than 50%

• Multilayer ceramic components such as capacitors, inductors, filter networks assembled into PWAs using assembly processes with ∆T/∆t > 4°C/second.

• Solder immersion or wave soldering of surface mount components other than simple chip resistors and chip capacitors.

• Components with ESD susceptibility

• Variable resistors, particularly wire-wound

• Variable capacitors

• Multilayer capacitors trimmed to value

**Typically, solder mask openings are designed 125 µm larger than the component land or through-hole pad. This allows for alignment tolerances during solder mask processing.**

IEEE 1149.1 is the digital boundary scan standard; the proposed IEEE 1149.4 will be the analog testability bus standard.

The three goals in implementing testability are controllability, observability, and partitioning. Controllability is the ability to manipulate signal flow within a circuit. Observability is the measure of the extent to which signal activity can be monitored. Partitioning is the reduction of complex circuitry into a set of minimally interactive subcircuits. For details see Appendix J.

Appropriate DfT technique may be the placement of adequate test pads for bare-board and in-circuit test (ICT). For ICT, supplemental jumpers to be connected or removed as part of the test routine may be required; for bare-board test, test pads at the end-of-net may be required to validate the integrity of PTH and via connections.

Appendix A

Design for Reliability (DfR) of Solder Attachments

Appendix B

Design for Reliability (DfR) of Plated-Through Via (PTV) Structures

Appendix C

Design for Reliability (DfR) of Insulation Resistance

Appendix D

Thermal Considerations

Appendix E

Environmental Stresses

Appendix F

Components

Appendix G

Coefficient of Thermal Expansion

Appendix H

Electrostatic Discharge

APPENDIX I

Solvents

Appendix J

Design for Testability

Appendix K

Design for Manufacturability and Assembly Checklist

Appendix L

Corrosion Basics and Checklist

Appendix M

Solder Joint Variability

Appendix N

Adhesives, Solder Mask and Conformal/Other Coatings

Appendix O

Aerospace and High Altitude Concerns

Appendix P

**ACRONYMS**

PWA - printed wiring assembly

**Eletr0nic enclosure = case + wire + PWAs + assembling + test +support**

**PWA = components + PCB + fabrication + test**

AABUS\* – As Agreed Between User and Supplier

AML – Approved Manufacturer List

AOI\* – Automated Optical Inspection

AR\* - Annular Ring

ATE\* – Automatic Test Equipment

AVL – Approved Vendor List

BER – Bit Error Rate

BGA\* – Ball Grid Array

BIST – Built-In Self-Test

BIT – Built-in Test

BOM\* – Bill of Material

BTC\* – Bottom Terminated Component

CAD\* – Computer-Aided Design

CAE\* – Computer-Aided Engineering

CAIV – Cost as an Independent Variable

CDRL – Contract Data Requirements List

CFD – Computational Fluid Dynamic

COTS – Commercial Off the Shelf

CTE\* – Coefficient of Thermal Expansion

DFA – Design for Assembly

DFC – Design for Cost

DFE – Design for Environment

DFF – Design for Fabrication

DFM\* – Design for Manufacturability

DFR – Design for Reliability

DFT – Design for Test

DFX – Design for Excellence

DRC – Design Rules Check

ECN\* – Engineering Change Notice

EDL – Engineering Drawing List

EEE – Electrical and Electronic Equipment

EMC\* – Electromagnetic Compatibility

EMI\* – Electromagnetic Interference

EMS\* – Electronics Manufacturing Services

EOL – End-of-Life

EOS - Exceeding of Stress

EPA\* – Environmental Protection Agency

ESD\* – Electro-Static Discharge

ESS – Environmental Stress Screening

FAIR – First Article Inspection Report

FBT – Functional Board Test

FEA\* – Finite Element Analysis

FET\* – Field-Effect Transistor

GNED – Global Nuclear Event Detector

HASS – Highly Accelerated Stress Screening

ITAR\* – International Traffic in Arms Regulations

LCA – Life Cycle Assessments

LED\* – Light-Emitting Diode

MCAD\* – Mechanical Computer Aided Design

MRB – Material Review Board

MSL\* – Moisture Sensitivity Level

MTBF\* – Mean Time Between Failures

MTTR – Mean Time To Repair

NSPAR – Non-Standard Parts Approvals Report

OEM\* – Original Equipment Manufacturer

PA – Prior Authorization

PAPL – Project Approved Parts List

PBA\* – Printed Board Assembly

PBB – Polybrominated Biphenyl

PBDE – Polybrominated Diphenyl Ether

PCN – Part Change Notices

PHM – Prognostic Health Management

PoP – Package-on-Package

PTH\* – Plated through-hole

PVC\* – Polyvinyl Chloride

QRD – Quality, Reliability and Durability

RF\* – Radio Frequency

RFP – Request for Proposal

RoHS – Restriction of Hazardous Substances

RP/PoF – Reliability Physics/Physics of Failure

SAT – Simulation Aided Testing

SDRL – Subcontract Data Requirements List

SEU – Single Event Upset

SMT\* – Surface Mount Technology

SoCD – Source Control Drawing

SOW – Statement of Work

TDR\* – Time-Domain Reflectometer

THT – Through-hole Technology

UUT – Unit Under Test

UV – Ultraviolet

WBS – Work Breakdown Structure

WEEE – Waste Electrical and Electronic Equipment