Optimized Designs of Reversible Fault Tolerant BCD adder and Fault Tolerant Reversible Carry Skip BCD Adder

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Abstract*— In recent years, reversible logic has become one of the most important areas of researches because of its applications in several technologies; such as low-power CMOS, Nano-computing and optical computing. In this paper, we have presented designs of a compact and efficient fault tolerant reversible Binary Coded Decimal (BCD) adder as well as a fault tolerant reversible Carry Skip BCD adder. We have proposed new reversible fault tolerant gates and heuristic algorithms to design compact BCD Adders. The proposed reversible fault tolerant BCD adder achieves the improvement as reducing cost of 23.07% on the number of gates, 52.67% on quantum cost, 31.03% on garbage outputs, 29.16% on the number of constant inputs and 23.07% on unit delay over the existing best one. Similarly, the proposed reversible fault tolerant carry skip BCD adder achieves the improvement as reducing cost of 34.72% on the number of gates, 43.24% on quantum cost, 37.5% on garbage outputs, 37.14% on the number of constant inputs and 34.72% on unit delay over the existing best one.

Keywords*— Reversible, UFT, Overflow detection logic, Fault Tolerance and BAFTA etc.

I. INTRODUCTION

With respect to the advancement in modern technology, energy efficient circuitry have gained strong attention of researchers due to low power consuming feature. The higher-level integration and fabrication process is innovated in better logic circuits. Energy loss is also dramatically reduced over few decades due to the invention of reversible logic. According to Landauer in 1960 [1, 2], in logic computation every bit of information loss dissipates $kT \times ln2$ joules of heat energy. Where k is Boltzmann's constant of 1.38×10^{23} J/K and T is the absolute temperature of the environment.

Conventional or irreversible circuits require much power whereas reversible circuits which are fundamentally different from traditional irreversible circuits, require less power than irreversible ones. Reversible logic has showed a feature that using this logic we can recover bit loss from its unique input-output mapping. In 1973, Bennett proved that no energy will be dissipated if the circuit consists of reversible gates only [3]. In recent years, quantum computation become very popular because of its reversible property. Thus, any research work in reversible logic is useful for the future development of modern technologies. Reversible logic circuits are used in numerous applications such as nanotechnology [4], DNA technology and optical computing [5].

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Another feature of reversible logic is fault tolerance that we can apply in any reversible gate to check its internal fault. Fault tolerant method preserves same parity between input and output vectors over one-to-one mapping of reversible circuit.

Bit error which is referred as alteration of the value of the output bits because of internal fault of digital circuit can be detected by parity checking of input-output vectors.

Numbers is stored and processed in computer in straight binary format. In case of storing formats, some floating-point numbers cannot be represented with desired precision [6] as the limitations of floating-point numbers and difficulties on storing formats. So, computation in binary coded decimal format have gained popularity as loss due to precision can be omitted in this format.

Circuits such as Binary Coded Decimal (BCD) adder have great impact in computational process. When the circuit is built using reversible logic, it requires less power and become faster. Various error can be occurred in reversible circuit. So, if we build a circuit that preserves parity of its input and output vector, we can detect its bit error. In this paper, we have proposed an improved fault tolerant reversible BCD adder and an improved fault tolerant reversible carry skip BCD adder. We found that our proposed designs are much better than the existing ones in terms of number of gates, quantum cost, garbage output, constant input and delay.

The paper is organized with the following sections: Section II gives the Basic ideas of Reversible and fault tolerant logic. Section III shows the existing approaches of designing reversible fault tolerant BCD adder and reversible fault tolerant carry skip BCD adder. Section IV introduces the design approaches of the proposed reversible fault tolerant BCD adder and reversible fault tolerant carry skip BCD adder. Section V gives the simulation results of all the proposed circuits and comparison with other existing researches. Finally, the paper is concluded with Section VI.

II. BASIC DEFINITIONS OF REVERSIBLE GATES AND THEIR PROPERTIES

In this section, we have represented the basic ideas and definitions of some popular fault tolerant reversible gates. Quantum realizations of fault tolerant reversible gates have also been illustrated in this section.

A. Reversible Gate

It is an n input, n output circuit that produces a unique output pattern for each possible input pattern (one-to-one correspondence relation).

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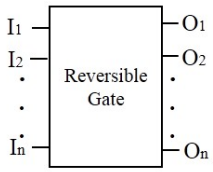

Fig. 1. Block Diagram of a n×n Reversible Gate

For an $n \times n$ reversible gate if the input vector be I_v and the output vector O_v then $Iv = (I_1, I_2, I_3 \ldots I_n)$ and $O_v=(O_1, O_2, O_3 \ldots O_n)$, respectively. The relationship between them is denoted as $(I_v \leftrightarrow O_v)$. Block diagram of an $n \times n$ reversible gate is shown in Fig. 1.

B. Reversible Fault Tolerant Gate

Reversible fault tolerant logic is used to detect error of a reversible gate which constantly preserves same parity between inputs and outputs. This property is $I_1 \oplus I_2 \oplus \ldots \oplus I_n = O_1 \oplus O_2 \oplus \ldots \oplus O_n$ which allows to detect a faulty signal from the circuit's primary output. When a reversible circuit is implemented using only fault tolerant reversible gates, the whole circuit itself preserves parity and thus be able to detect fault [7]. A very popular fault tolerant reversible gate is Fredkin gate(FRG) [10] which is shown in Fig. 2(d).

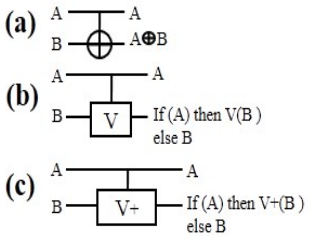

Fig. 2. Quantum Realization of Controlled (a) Not Gate (b) V Gate (c)V^+ Gate

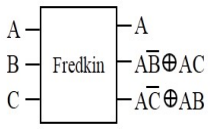

Fig. 2(d). Block Diagram of Fredkin Gate(FRG)

C. Quantum Cost

Quantum cost can be computed by substituting the reversible gates of a circuit by a cascade of elementary quantum gates [8]. Elementary quantum gates realize quantum circuit that are inherently reversible and manipulate qubits rather than pure logic values [9]. The most used elementary quantum gate is NOT gate (a single qubit is inverted), the controlled–NOT (CNOT) gate (the target qubit is inverted if and only if the first qubit is 1), the controlled-V gate (also known as square root of NOT and two consecutive V operations are equivalent to an inversion) and the controlled-V^+ gate (which performs the inverse operation of the V gate and thus is also a square root of NOT) [9]. Graphical representation of C-Not, V and V^+ are shown in Fig. 2(a), Fig. 2(b) and Fig. 2(c) respectively.

D. Garbage Output

Unwanted or unused outputs of a reversible gate which are not used as the input of other reversible gates, are known as garbage outputs. Garbage outputs are needed only to maintain reversibility. Heavy price paid off for each garbage output. The calculation of garbage output can be changed in case of using that gate in different digital circuits. Fig. 2(a) shows that for an EX-OR operation, the Feynman gate produces one garbage output.

E. Constant Input

Sometimes it is needed to apply constant input to any reversible gate for a specific logic operation. Constant input means either 0 or 1. In reversible circuit we have to minimize constant inputs because it may cause delay.

F. Unit Delay

The delay of a logic circuit is the maximum number of 2×2 quantum gates in a path from any input line to any output line. This definition is based on the following two assumptions. Firstly, each gate performs the computation in one unit time. This means that every gate in the given circuit will take the same amount of time for internal logic operation. Secondly, all inputs to the circuit are known before the computation begins. This means that the internal structure and each operation of the gate are known before the calculation. From the above definition, the delay of the logic circuit of Fig. 2(a), 2(b) and 2(c) is obviously one as this circuit has only one quantum gate from its input to output line

III. Previous Works

This section have presented some of the previous approaches of online testability. Subsections III.A and III.B have discussed about those approaches.

A. Reversible Fault Tolerant BCD Adder and Reversible Fault Tolerant Carry Skip BCD adder Using IG Gate [11]

A fault tolerant reversible BCD adder in (Saiful, 2008) is depicted in [11]. It includes two four-bit fault tolerant reversible full adder blocks, six Fredkin gates and a PPHCG gate. The QC of PPHCG is 6. This design produces 40 garbage outputs. It also requires 24 constant inputs. The quantum cost of this circuit is 148. In this research all of the efficiency parameters remain high with respect to our proposed method.

B. Reversible Fault Tolerant BCD Adder and Reversible Fault Tolerant Carry Skip BCD adder Using Hagparast proposed method [12]

In this paper, they used one existing quantum fault tolerant reversible full adder circuit that proposed by (Dastan, 2011) [13] to construct a four bit fault tolerant reversible full adder blocks. This design includes two 4-bit fault tolerant reversible full adder blocks, three NFT gates and two F2G gates. So, in total thirteen fault tolerant reversible gates is required to construct this circuit. The quantum cost of the proposed circuit is 131 and design produces 29 garbage outputs. It also requires 24 constant inputs. This research also remain costly in all of the efficiency parameters with respect to our proposed method.

IV. Proposed Work

The previous Section III, has already described a variety of approaches to construct reversible fault tolerant BCD adder and carry skip BCD adder. In fault tolerant adder circuit, we can detect fault by checking parity of its input and output bits that have already been described in Section II.B. In this section, we present a design approach to construct reversible fault tolerant BCD adder. We have segmented the circuit in three parts. Firstly, we construct a fault tolerant *4*-bit ripple carry adder using BAFTA gate. Secondly, we construct the fault tolerant overflow detection logic of BCD adder using Feynman double gate (F2G) [14], one Fredkin gate(FRG)[10] and one 3-bit ETG[18]. Thirdly, we construct 1-bit BCD adder correction

logic circuit using Feynman double gate[F2G], proposed UFT and BAFTA gate.

A. Proposed Universal Fault Tolerant Gate

In this subsection, a new *4×4* fault tolerant reversible gate namely UFT gate is proposed. The proposed gate and its quantum realization are shown in Fig. 3(a) and Fig. 3(b), respectively. In Fig. 3(b) dotted rectangle is equivalent to a *2×2* CNOT gate. So, quantum cost of the UFT gate is 6. If we construct a truth table of the proposed gate it can be notified from the truth table that the input pattern corresponding to a particular output pattern can be uniquely determined where input-output bit parity is also preserved. A fault tolerant gate MIG [15, 16] like our proposed gate have already been presented but quantum cost of MIG gate is 7 whereas ours is only 6.

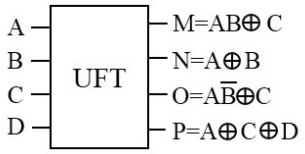

Fig. 3(a). Block Diagram of Proposed UFT Gate

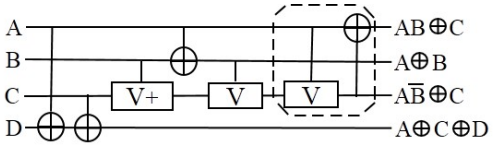

Fig. 3(b). Quantum Realization of Proposed UFT Gate

Lemma 1: UFT is a fault tolerant gate.

Proof: The input vector and output vector of UFT gate are I_v = *{A, B, C, D}* and O_v = *{AB⊕C, A⊕B, AB'⊕C, A⊕C⊕D}* respectively.

Getting input parity by EX-ORing all inputs is

= A⊕B⊕C⊕D

To get output parity, we have to EX-OR all the outputs and we get,

=AB⊕C⊕A⊕B⊕AB'⊕C⊕A⊕C⊕D
=B⊕AB⊕C⊕D⊕AB'
=A(B⊕B')⊕B⊕C⊕D
=A⊕B⊕C⊕D

From above, it is clear that the output parity is equal to input parity and it also satisfies the fault tolerant property described in Section II.B. So, from the above explanation, it is proved that the UFT is a fault tolerant gate.

B. Proposed Babu Avishek Fault Tolerant Adder Gate

In this subsection, a new *5×5* fault tolerant reversible gate namely BAFTA gate is proposed. The proposed gate and its quantum realization are shown in Fig. 4(a) and Fig. 4(b), respectively. In Fig. 4(b) dotted rectangle is equivalent to a *2×2* CNOT gate so the quantum cost of BAFTA gate is 8.

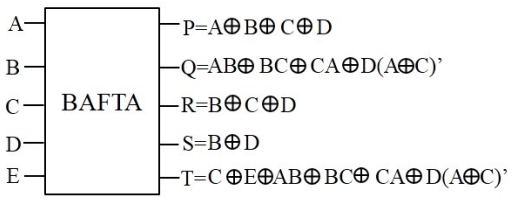

Fig. 4(a). Block Diagram of Proposed BAFTA Gate

If we construct a truth table of the proposed gate, it can be notified from the truth table that the input pattern corresponding to a particular output pattern can be uniquely determined and input-output bit parity is also preserved.

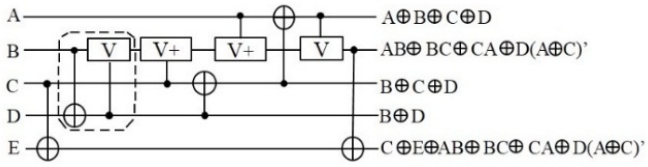

Fig. 4(b). Quantum Realization of Proposed BAFTA Gate

Lemma 2: BAFTA is a fault tolerant gate.

Proof: The input vector and output vector of BAFTA gate be I_v = *{A, B, C, D, E}* and O_v = *{A⊕B⊕C⊕D, AB⊕BC⊕CA⊕D(A⊕C)', B⊕C⊕D, B⊕D, C⊕E⊕AB⊕BC⊕CA⊕D(A⊕C)'}* respectively.

Getting input parity by EX-ORing all inputs is

=A⊕B⊕C⊕D⊕E

To get output parity, we have to EX-OR all the outputs and we get,

=A⊕B⊕C⊕D⊕AB⊕BC⊕CA⊕D(A⊕C)'⊕B⊕C⊕D⊕B⊕D⊕C⊕E⊕AB⊕BC⊕CA⊕D(A⊕C)'
= A⊕B⊕C⊕D⊕E

Which is equal to input parity and it also satisfies the property described in Section II.B. So, from the above explanation, it is shown that the BAFTA is a fault tolerant gate.

C. Design of a Fault Tolerant Full Adder Using BAFTA Gate

Proposed Compact Fault Tolerant Full Adder (*BAFTA*) gate can be used as fault tolerant full adder. It requires only one *BAFTA* gate. Necessary circuit for fault tolerant full adder by using *BAFTA* gate is shown in Fig. 5.

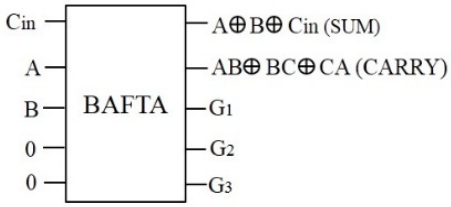

Fig. 5. BAFTA Gate Works as a Fault Tolerant Reversible Full Adder

D. Design Synthesis of Proposed Fault Tolerant Reversible BCD Adders

A fault tolerant reversible BCD adder comprised of three major parts: a *4*-bit parallel or ripple carry adder, overflow detection logic of BCD adder and *1*-bit BCD adder overflow correction logic which are described in subsections IV.D.1, IV.D.2 and IV.D.3 respectively.

1) Proposed Fault Tolerant Reversible 4-bit Ripple Carry Adder

Fault tolerant reversible BCD requires two *4*-bit parallel adders or ripple carry adders. But for better efficiency and to minimize circuitry, we use only one *4*-bit parallel adder. The output of the first *4*-bit parallel adder, which is the partial sum of two BCD numbers, is fed to the overflow detection circuit. Fig. 6 shows the circuitry of a 4-bit parallel or ripple carry adder. **Algorithm I** describe the construction method of 4-bit Ripple Carry Adder.

Algorithm I: Construction of a 4-bit Ripple Carry Adder

Begin

1. Firstly, we have to take four BAFTA gate. For each BAFTA input and output vector are I_{ni} and O_{ni} respectively *(n=1, 2, 3* and 4 for each BAFTA gate and *i = 1, 2, 3, 4, 5* for each input and output vectors of BAFTA gate). Now, $I_{14} = I_{15} = I_{24} = I_{25} = I_{34} = I_{35} = I_{44} = I_{45} \leftarrow 0$
2. For input $I_{11} \leftarrow C_0$, $I_{12} \leftarrow A_0$, $I_{13} \leftarrow B_0$ and for output $O_{11} \rightarrow S_0$ and $O_{12} \rightarrow C_1$
3. For each BAFTA gate $n = 2,\ldots,4$ And for input and output vectors $i = 1, 2, 3$ $I_{n1} \leftarrow C_i$, $I_{n2} \leftarrow A_i$, $I_{n3} \leftarrow B_i$ and for output $O_{n1} \rightarrow S_i$ and $O_{n2} \rightarrow C_{i+1}$

End

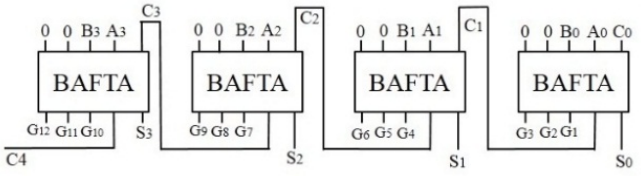

Fig. 6. Fault Tolerant Reversible 4-bit Ripple Carry Adder

2) Proposed Overflow Detection Logic Circuit of BCD Adder

The error detection expression is $((S_1+S_2)\ S_3+C_4)$. In case of adding two BCD numbers, the highest sum is 18. This implies that $((S_2+S_1)S_3)$ and C_4 cannot be true at the same time. The error detection expression (F) can be computed using an Ex- OR instead of an OR operation: $F = ((S_2+S_1)\ S_3 \oplus C_4)$. After that, optimized circuit of a *4*-bit parallel adder is employed to get the final (corrected) output. Fig. 7(a) and Fig. 7(b) shows the overflow detection logic circuit and its block diagram respectively. **Algorithm II** describes the construction method of Overflow Detection Logic Circuit.

Algorithm II: Construction of Overflow Detection Logic Circuit

Begin

Take one F2G[14], one Fredkin(FRG)[10] and one 3-bit ETG[18] respectively. Taking the partial summation output from the 4-bit ripple carry adder, we insert the values in F2G, Fredkin and 3-bit ETG respectively. Let, F2G, Fredkin and 3-bit ETG represented as X, Y and Z respectively.

1. For F2G, input vector written as $I_{X3} = I_{X2} \leftarrow 0$, $I_{X1} \leftarrow S_1$ and output vector $O_{X3} = O_{X1} \rightarrow S_2$.
2. For Fredkin gate, input vector written as $I_{Y1} \leftarrow S_2$, $I_{Y2} \leftarrow S_1$, $I_{Y3} \leftarrow 1$ and output vector $O_{Y1} \rightarrow S_2$, $O_{Y2} \rightarrow I_{Z1}$
3. For 3-bit ETG, input vector written as $I_{Z1} \leftarrow O_{Y2}$, $I_{Z2} \leftarrow S_3$, $I_{Z3} \leftarrow C_4$, $I_{Z4} \leftarrow 0$

End

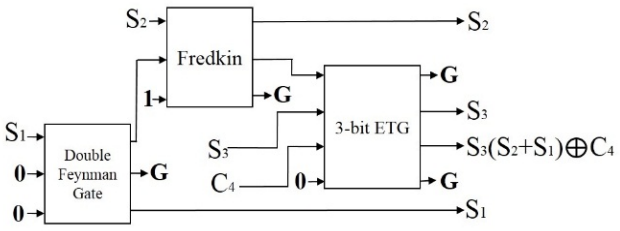

Fig. 7(a) Overflow Detection Circuit

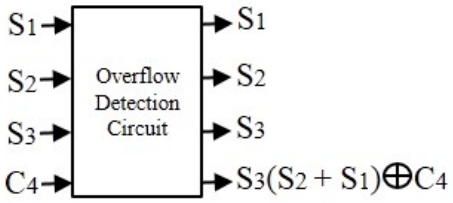

Fig. 7(b) Overflow Detection Circuit Block Diagram

3) Proposed Overflow Correction Logic Circuit of BCD Adder

Overflow correction logic circuit is nothing but an optimized 4-bit parallel or ripple carry adder. Output that comes from overflow detection logic is accepted here as an input to produce correct BCD addition of two binary converted 1-digit decimal number. Fig. 8 shows the elementary circuitry of the proposed overflow correction logic circuit. . **Algorithm III** describes the construction method of Overflow Correction Logic Circuit.

Algorithm III: Construction of Overflow Correction Logic Circuit

Begin

Take three reversible fault tolerant gate namely F2G, BAFTA and UFT respectively. UFT, BAFTA and F2G gate is represented by x, y and z respectively.

1. Input vector of UFT gate written as $I_{x1} \leftarrow F$, $I_{x2} \leftarrow S_1$, $I_{x3} \leftarrow 0$, $I_{x4} \leftarrow 0$ and output vector as $O_{x1} \rightarrow C_{out\_1}$, $O_{x2} \rightarrow \Sigma_1$ and $O_{x4} \rightarrow F$
2. Input vector of BAFTA gate written as $I_{y1} \leftarrow S_2$, $I_{y2} \leftarrow F$, $I_{y3} \leftarrow C_{out\_1}$, $I_{y4} \leftarrow 0$, $I_{y5} \leftarrow 0$ and output vector written as $O_{y1} \rightarrow \Sigma_2$, $O_{y2} \rightarrow C_{out\_2}$, $O_{y4} \rightarrow F$
3. Input vector of F2G written as $I_{z1} \leftarrow F$, $I_{z2} \leftarrow S_3$, $I_{z3} \leftarrow 0$ and output vector written as $O_{z2} \rightarrow \Sigma_3$

End

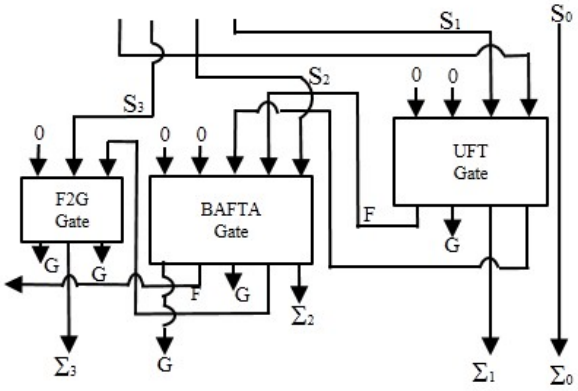

Fig. 8. 1-bit BCD Adder Correction Logic Circuit

4) Proposed Fault Tolerant Reversible BCD Adder

All the above mentioned logic blocks are combined to construct a fault tolerant reversible BCD adder. Fig. 10 shows the compact representation of a fault tolerant BCD adder.

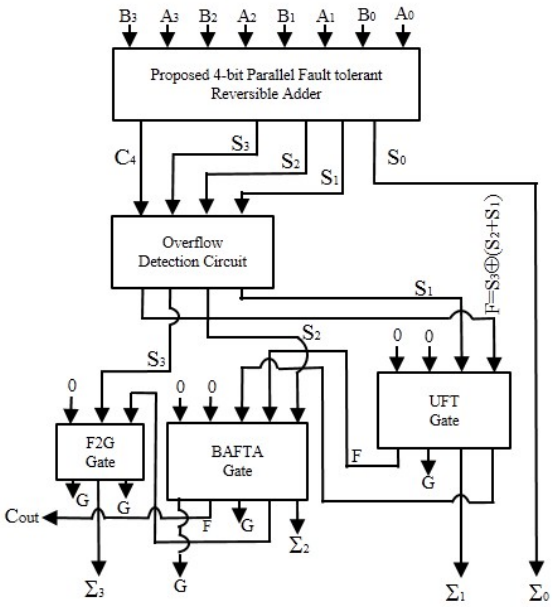

Fig.9. Proposed Fault Tolerant Reversible BCD Adder

E. Proposed Fault Tolerant Reversible Carry Skip BCD Adder

In this paper, we have also presented a fault tolerant reversible carry skip BCD adder. The elementary circuitry of this circuit is shown in Fig. 10.

V. SIMULATION AND COMPARISON

The simulation of the proposed circuit is done using Microwind DSCH 3.5 [19] software on a computer, which has the Intel(R) Core 2-Dou CPU with 2.10 GHz Clock Speed. The simulation result shown in Fig. 11 expresses that the proposed fault tolerant BCD adder give correct outputs for all possible combinations of inputs. Tables I and II show the comparative study of our proposed designs with existing designs for a fault tolerant reversible BCD adder and a fault tolerant reversible carry skip BCD adder respectively. Tables III and IV show the improvement ratio in percentage of our proposed design with the existing designs for a fault tolerant reversible BCD adder and a fault tolerant reversible carry skip BCD adder, respectively. From Tables 2 and 4, we find that the proposed design outperforms the existing ones in terms of number of gates, garbage outputs, quantum costs, constant inputs and unit for a fault tolerant reversible BCD adder and a fault tolerant reversible carry skip BCD adder, respectively.

TABLE I. COMPARISON OF PROPOSED FAULT TOLERANT REVERSIBLE BCD ADDER WITH EXISTING BCD ADDERS

Item	NOG	QC	GO	CI	UD
Existing [11]	23	148	40	35	23
Existing [12]	13	131	29	24	13
Proposed Approach	10	62	20	17	10

QC = Quantum Cost, UD = Unit Delay, CI = Constant Input

TABLE II. COMPARISON OF PROPOSED FAULT TOLERANT REVERSIBLE CARRY SKIP BCD ADDER WITH EXISTING CARRY SKIP BCD ADDERS

Item	NOG	QC	GO	CI	UD
Existing [11]	23	148	40	35	23
Proposed Approach	15	84	25	22	15

QC = Quantum Cost, UD = Unit Delay, CI = Constant Input

TABLE III. IMPROVEMENT RATIO IN PERCENTAGE BETWEEN OUR FAULT TOLERANT COMPACT DESIGN AND THE EXISTING BEST ONE.

Methods	No. of Gate	QC	Garbage	CI	UD
Proposed	10	62	20	17	10
Best Existing[12]	13	131	29	24	13
Improvement Ratio	23.07%	52.67%	31.03%	29.16%	23.07 %

QC = Quantum Cost, UD = Unit Delay, CI = Constant Input

TABLE IV. IMPROVEMENT RATIO IN PERCENTAGE BETWEEN OUR FAULT TOLERANT COMPACT DESIGN AND THE EXISTING BEST ONE.

Methods	No. of Gate	QC	Garbage	CI	UD
Proposed Approach	15	84	25	22	15
Best Existing[11]	23	148	40	35	23
Improvement Ratio	34.72%	43.24%	37.5%	37.14%	34.72%

QC = Quantum Cost, UD = Unit Delay, CI = Constant Input

VI. CONCLUSION

In this paper, we have presented fault tolerant reversible logic syntheses for both Binary Coded Decimal (BCD) adder and Carry Skip BCD adder. The designs have been developed by using fault tolerant reversible logic and it has been found that the proposed designs are much better than the existing ones in terms of number of gates needed, quantum cost required, number of garbage outputs produced, constant inputs needed and delay required. Compact fault tolerant reversible BCD adder and fault tolerant reversible Carry Skip BCD adder can perform much faster than the existing BCD adders. Moreover, quantum costs for the proposed circuits are much less than the existing designs. BCD adders is an important part of some other larger and more complex reversible circuits. Compact and fast BCD adders may also find its use in future quantum computers.

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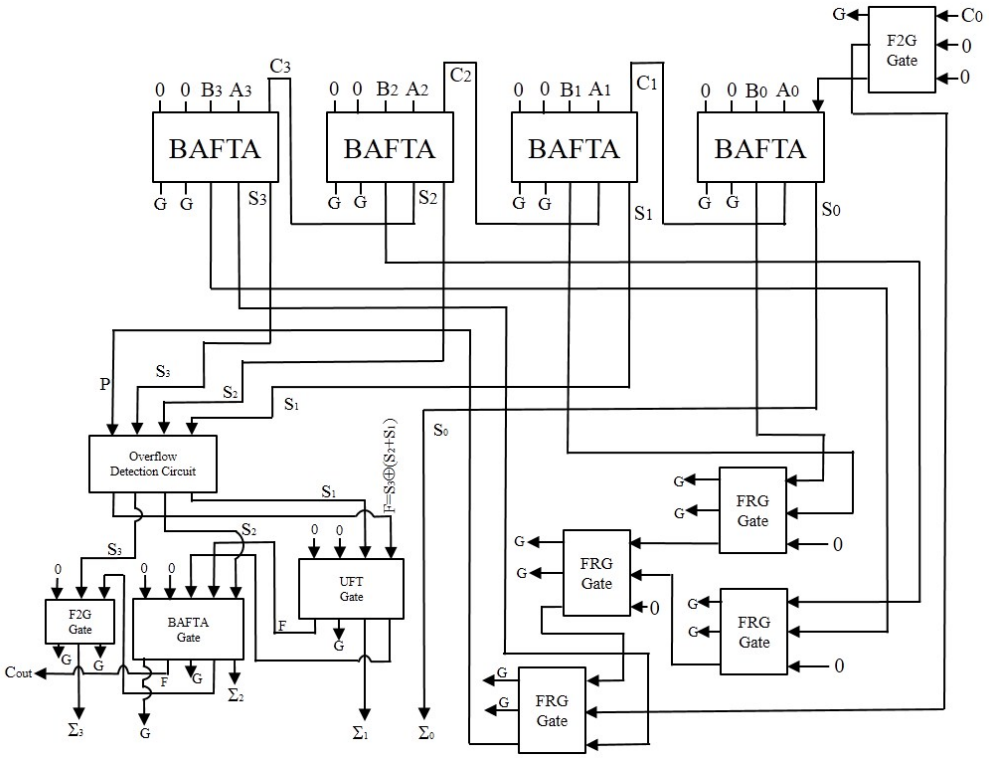

Fig. 10. *Proposed Fault Tolerant Reversible Carry Skip BCD Adder*

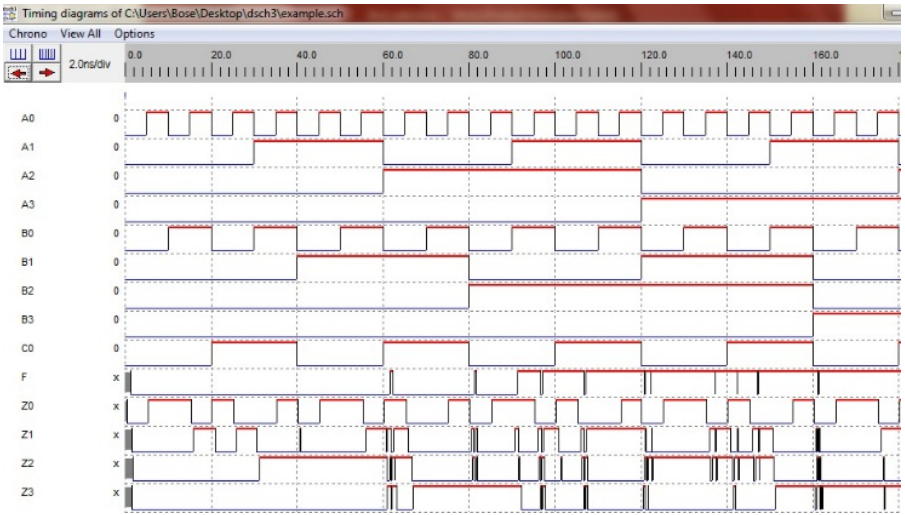

Fig. 11. Simulation Result of The Proposed Fault Tolerant Reversible BCD Adder