A Novel Approach for Constructing Reversible Fault Tolerant *n*-Bit Binary Comparator

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***Abstract*—Nowadays fault tolerant reversible logic is becoming popular and have widely used in reducing power consumption of digital logic design. Reversible logic is used to optimize power by recovering bit loss from its unique input-output mapping. In this paper, for the first time we designed a novel approach for constructing fault tolerant reversible *n*-bit binary comparator. An algorithm has been presented for constructing the novel fault tolerant reversible comparator circuit. We designed two new fault tolerant reversible gates namely AG, and FTSEG to optimize the number of gates, garbage outputs, quantum cost, constant inputs and delay of the circuit. Two lemmas are also presented to prove the fault tolerance or parity preserving property for the proposed two fault tolerant reversible gates AG and FTSEG respectively. The simulation results of the proposed fault tolerant reversible design show that the circuit works correctly.**

Keywords- reversible logic, fault tolerance, garbage output, quantum cost , binary comparator, MSB, etc.

I. INTRODUCTION

Reversible logic has showed a feature that, by using this logic we can recover bit loss from its unique input-output mapping. Fault tolerance is another feature in reversible logic that, it can detect any fault in the internal circuit by input-output parity bit checking. In recent years, fault tolerant reversible logic is massively used in various technologies such as low power CMOS design, optical information processing, DNA computing, bioinformatics, quantum computing [1], thermodynamics and nanotechnology [8]. In traditional irreversible logic, information is lost once and input vector cannot be recovered from its output vector or vice versa. In 1960, Landeur proved that for every bit of information loss dissipates $KT\times ln2$ joules [2] of energy where K is the Boltzmann's constant and T is the absolute temperature [5]. Since reversible gates are free from information loss, internal power dissipation is theoretically zero. Bennett established in 1973 that, a circuit must be built using reversible logic gates to avoid KT×ln2 joules of energy dissipation. Due to one-to-one correspondence between its input and output vectors [3, 4], no information is lost in reversible gate. So, power dissipation would be zero if the circuits consist of only reversible gates [5]. Another feature of reversible logic is fault tolerance that, we can apply in any reversible gate to check its internal fault. Fault tolerant method in reversible logic preserves same parity between input and output vectors over one-to-one mapping of reversible circuit.

Bit error which is referred as alteration of the value of the output bits caused by internal fault of digital circuit, can be detected by parity checking of input-output vectors.

Comparison between two binary numbers has a wide range of application in microprocessors, communication systems, encryption devices, sorting networks etc. So, binary comparator is an essential circuitry in modern VLSI design and nanotechnology [8]. We don't find any reversible binary comparator circuit which is fault tolerant or has parity preserving property. So In this paper, we have presented an *n*-bit fault tolerant reversible binary comparator circuit which uses less number of gates, less number of garbage outputs, less quantum cost and delay. Two lemmas are also presented to prove parity-preserving property of the proposed two fault tolerant gates namely AG and FTSEG respectively. Several theorems are in this paper to prove the efficiency of reversible logic synthesis of proposed *n*-bit comparator. The paper is organized as follows. Section II, specifies the ideas about the reversible fault tolerant gate, basic definition and quantum realization of some fault tolerant reversible gates, which have been used later in this paper. Section III shows some existing non-fault tolerant reversible *n*-bit comparator. Section IV describes the logic synthesis of proposed fault tolerant reversible n-bit comparator. Section V gives the simulation results and summary of the proposed fault tolerant reversible circuits. Finally, the conclusion is given in Section VI.

II. BASIC DEFINATION

In this section, we have represented the basic ideas and definitions of some popular fault tolerant reversible gates. Quantum realizations of fault tolerant reversible gates have also been illustrated in this section.

A. Reversible Gate

It is an *n*-input and *n*-output gate that produces a unique output pattern for each possible input pattern (one-to-one correspondence relation) [6]. For an $n\times n$ reversible gate if the input vector be $I_v = (I_1, I_2,\ldots I_n)$ and the output vector be $O_v = (O_1, O_2,\ldots O_n)$, respectively. The relationship between them is denoted as $(I_v \leftrightarrow O_v)$ [6]. Block diagram of an $n\times n$ reversible gate is shown in fig. 1.

B. Fault Tolerant Gate

It is used to detect error of a reversible gate which constantly preserves same parity values between input and output vectors.

$I_1\oplus I_2\oplus I_3\ldots\oplus I_n = O_1\oplus O_2\oplus O_3\ldots\oplus O_n$ It is the parity preserving property that allows detecting a faulty signal from the circuit's primary output. When a reversible circuit is implemented using only fault tolerant reversible gates, the entire circuit itself preserves parity and thus, it should be able to detect fault [7]. A fault tolerant reversible gate is shown in fig. 3(a).

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C. Quantum Cost

Quantum cost can be computed by substituting the reversible gates of a circuit by cascading of elementary quantum gates [8]. Elementary quantum gates realize quantum circuit, which is inherently reversible and manipulates qubits rather than pure logic values [9]. The mostly used elementary quantum gate is NOT gate (a single qubit is inverted), the Controlled–NOT (CNOT) gate (the target qubit is inverted if and only if the first qubit is 1), the controlled-V gate (also known as square root of NOT and two consecutive V operations are equivalent to an inversion) and the controlled-gate (which performs the inverse operation of the V gate and it is also a square root of NOT) [9].

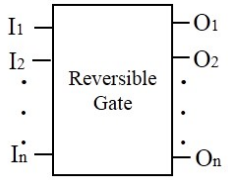

Fig. 1. Block Diagram of $n \times n$ Reversible Gate.

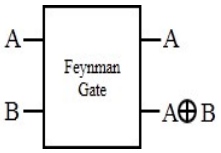

Fig. 2. Feynman Gate.

D. Unit Delay

The delay of a logic circuit is the maximum number of gates in a path from any input line to any output line. This definition is based on the following two assumptions [10]. Firstly, each gate performs the computation in one unit time. This means that every gate in the given circuit will take the same amount of time for internal logic operation. Secondly, all inputs to the circuit are known before the computation begins. This means that the internal structure and each operation of the gate are known before the calculation.

From the above definition, the delay of the logic circuit of Fig. 2 is obviously one as this circuit has only one gate from its input to output line.

E. Garbage Output

Unwanted or unused output of a reversible gate which is not used as the input of other reversible gate, is known as garbage output. Garbage outputs are needed only to maintain reversibility. Heavy price paid off for each garbage output [10]. The calculation of garbage output can be changed in case of using that gate in different digital circuits. Fig. 2 shows that for an EX-OR operation, the Feynman gate produces one garbage output.

F. Constant Input

Sometimes, it is needed to apply constant inputs to any reversible gate for a specific logic operation. Constant input means either 0 or 1. In reversible circuit, we have to minimize constant inputs because it may cause delay.

G. Popular Fault Tolerant Reversible Gates with Quantum Representation

1) Fredkin Gate: The input vector and output vector of a 3×3 Fredkin gate (FRG) are defined as $I_v = \{A, B, C\}$ and $O_v = \{A, A'B \oplus AC, A'C \oplus AB\}$ [11]. Quantum cost of Fredkin gate is 5. Fig. 3(a) and Fig. 3(b) show the block diagram and quantum realization of Fredkin gate, respectively.

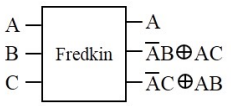

Fig. 3(a). Fredkin Gate.

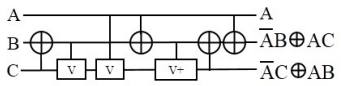

Fig. 3(b). Quantum Realization of Fredkin Gate.

2) Double Feynman Gate: The input and output vector of 3×3 double Feynman gate (F2G) [7] defined as $I_v = \{A, B, C\}$ and $O_v = \{A, A \oplus B, A \oplus C\}$. Fig. 4(a) shows a block diagram of a double Feynman gate with its quantum realization in Fig. 4(b).Quantum cost of Double Feynman Gate is 2.

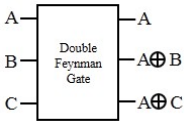

Fig. 4(a). Double Feynman Gate.

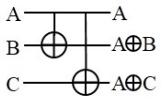

Fig. 4(b). Quantum Realization of Double Feynman Gate.

3) Modified Islam Gate (MIG): The input and output vectors of 4×4 Modified Islam gate or MIG [13] defined as $I_v = \{A, B, C, D\}$ and $O_v = \{A, A \oplus B, AB \oplus C, AB'\oplus C\}$. Fig. 5(a) shows a block diagram of a MIG gate with its quantum realization in Fig. 5(b). Quantum cost of MIG gate is 7.

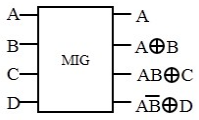

Fig. 5(a). MIG Gate.

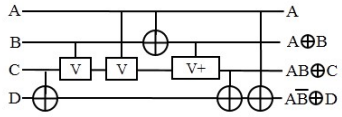

Fig. 5(b). Quantum Realization of MIG Gate.

III. Existing Works and Analysis

A. Reversible Comparator Using Tree Based Revesible Logic

Thapliyal and Ranganathan presented a new reversible n-bit binary comparator based on binary tree structure [14]. The design is based on the necessary properties of the TR [14] gate. In this design approach, each node of tree based reversible binary comparator consists of a *2*-bit reversible binary comparator. This node can compare two *2*-bit numbers $A(A_i, A_{i-1})$ and $B(B_i, B_{i-1})$, to generate two 1-bit outputs P and Q. P will be 1 if $A(A_i, A_{i-1}) > B(B_i, B_{i-1})$, on the other hand Q will be 1 if $A(A_i, A_{i-1}) < B(B_i, B_{i-1})$. Limitations of this design approach are that firstly, it requires so much quantum cost [8, 9]. Secondly, this design is not fault tolerant or parity preserving. Therefore, this design cannot detect any bit fault that is occurred in its internal circuitry. Thirdly, its circuit complexity is also high.

B. Four-Bit Reversible Numerical Comparator Using STG and STAG Gate

Mall at el. presented another Design of *4*-bit Reversible numerical comparator [15] using STG and STAG gate [15]. There are limitations firstly: this design is shown only for *4*-bit and generalization of n-bit comparator is not discussed. Secondly, this design approach is not parity preserving or fault tolerant. Thirdly, this design requires too many gates as well as also have much garbage outputs, quantum cost and constant inputs.

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IV. Proposed Design of Fault Tolerant Reversible *N*-bit Comparator

In this section, we propose a compact and improved version of fault tolerant reversible *n*-bit comparator. A binary comparator compares the magnitude of two binary numbers to determine whether they are equal or one is greater/less than the other. To construct the optimized *n*-bit comparator, we have proposed two new fault tolerant reversible gate named AG and FTSEG in Sections IV.A and IV.B, respectively. Section IV.C shows the design of 1-bit comparator circuit. In case of proposing better design for *n*-bit fault tolerant comparator, three major parts are implemented. The first part is MSB comparator circuit for comparing $(n-1)^{th}$ input (MSB) of two *n*-bit binary number described in Section IV.D. The second is "Greater or Equal" comparator circuit block which is designed to compare the remaining total *(n-1)* bits of two binary numbers with the previous level comparison result of MSB which is described in Section IV.E. Last part is "less than" comparator circuit cell which is used to generate whether the first number is less than the second number or not, described in Section IV.F. These three circuits are combined together to use in designing 2-bit and *n*-bit fault tolerant reversible binary comparators, which has been described in Section IV.G and Section IV.H, respectively

A. Proposed AG Gate

In this **s**ubsection, a new *5×5* fault tolerant reversible gate namely AG gate is proposed. The proposed gate and its quantum realization is shown in Fig. 6(a) and Fig. 6(b), respectively. In Fig. 6(b) each dotted rectangle is equivalent to a *2×2* CNOT gate so the quantum cost of AG gate is 8. If we construct a truth table, It can be notified from the truth table that the input pattern corresponding to a particular output pattern can be uniquely determined and input-output bit parity is also preserved.

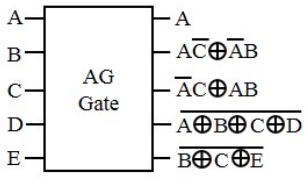

Fig. 6(a). Proposed Fault Tolerant ReversibleAG Gate.

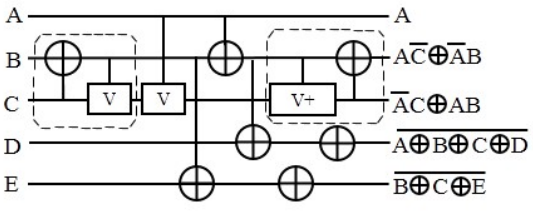

Fig. 6(b). Quantum Realization of Proposed AG Gate.

Lemma 1: Proposed AG Gate is a Fault Tolerant Reversible Gate

Proof: The input vector and output vector of AG gate be I_v = *{A, B, C, D, E}* and O_v = *{A, (AC'⊕A'C), (A'C ⊕AB), (A⊕ B⊕C ⊕D)', (B⊕C⊕E) }* respectively.

From Section II.B, we know that input parity and output parity have to be same in fault tolerant or parity preserving gate.

So, input parity of AG gate is = $A\oplus B\oplus C\oplus D\oplus E$

Outputparity of AG gate is = *A⊕(AC'⊕A'C)⊕(A'C ⊕AB), (A⊕ B⊕C ⊕D)'⊕(B⊕C⊕E)*

= *A(1⊕C')⊕A'C⊕B(A'⊕A)⊕A⊕B⊕C⊕D⊕1⊕B⊕C⊕E⊕1*

= *AC⊕A'C⊕B⊕A⊕D⊕E*

=*C(A⊕A')⊕B⊕A⊕D⊕E*

=*A⊕B ⊕C⊕D⊕E*

Thus, output parity is equal to input parity. As AG gate preserves the parity values of input and output, AG gate is a fault tolerant reversible gate.

B. Proposed FTSEG Gate

In this subsection, a new *4×4* fault tolerant reversible gate namely FTSEG is proposed. The proposed gate and its quantum realization are shown in Fig. 7(a) and Fig. 7(b), respectively. Quantum cost of FTSEG gate is 4. If we construct a truth table, It can be notified from the truth table that the input pattern corresponding to a particular output pattern can be uniquely determined and input-output bit parity is also preserved.

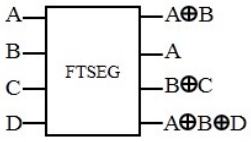

Fig. 7(a). Proposed Fault Tolerant Reversible FTSEG Gate.

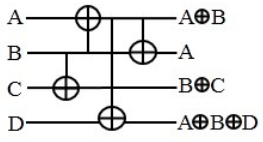

Fig. 7(b). Quantum Representation of Proposed FTSEG Gate.

Lemma 2: Proposed FTSEG Gate is a Fault Tolerant Reversible Gate

Proof: The input vector and output vector of FTSEG gate be I_v = *{A, B, C, D}* and O_v = *{(A⊕B), A, (B⊕C), (A⊕B⊕D)}* respectively.

From Section II.B , we know that input parity and output parity will be same in fault tolerant or parity preserving gate.

Therefore, input parity of FTSEG gate is = $A\oplus B\oplus C\oplus D$

Outupt parity of FTSEG gate is = $A\oplus B\oplus A\oplus B\oplus C\oplus A\oplus B\oplus D$

=$A\oplus B\oplus C\oplus D$

Thus, output parity is equal to input parity. As FTSEG gate preserves the parity values of input and output, FTSEG gate is a fault tolerant reversible gate.

C. Proposed Design of 1-Bit Fault Tolerant Reversible Comparator Circuit

The 1-bit comparator compares two 1-bit of two binary numbers *(A, B)* and determines the result among *(A>B), (A=B)* and *(A<B)*. The truth table of 1-bit comparator is shown in Table I. The proposed AG gate can be used as a *1*-bit comparator. It is well known that *(A>B) = AB'*, *(A=B) = (A⊕B)'* and *(A<B) = A'B*. The gate takes two 1-bit binary numbers as input A and B, and three '0's as constant inputs. The get produces two garbage outputs and three desired outputs that are *(A>B)*, *(A=B)* and *(A<B)*. Proposed 1-bit fault tolerant reversible comparator is shown in Fig. 8.

TABLE I. Truth Table for 1-Bit Binary Comparator

Input		Output		
A	B	A>B	A<B	A=B
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

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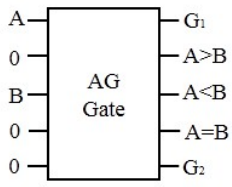

Fig. 8.AG Works as 1-bit Fault Tolerant Reversible Comparator.

D. *Proposed Design of Fault Tolerant Reversible MSB Comparator Circuit for n-Bit*

In this subsection, a fault tolerant MSB (Most Significant Bit) comparator circuit has been proposed. The circuit takes two MSB *($(n-1)^{th}$* bit of two binary numbers*)* A_{n-1} and B_{n-1} from two *n*-bit binary numbers (A, B) and three '0's as constant input for *n*-bit binary comparator. It will produce three outputs based on the bits present at the input level that are P_{n-1} = (A>B), Q_{n-1} = (A<B) and R_{n-1} = (A=B), respectively. Later these outputs are fed into the next level "Greater or Equal " circuit blockwhere total (*n*-1) number of bits have also been compared. The proposed MSB comparator circuit is shown in Fig. 9, where one AG gate produces three necessary outputs and two garbage outputs.

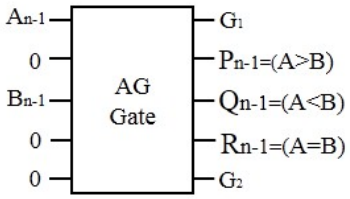

Fig. 9.AGWorks as MSB Fault Tolerant Reversible Comparator Circuit.

E. *Proposed Design of Fault Tolerant Reversible "Greater or Equal " Comparator Circuit and its Block Diagram*

A fault tolerant reversible "Greater or Equal" circuit block for *1*-bit is presented in this subsection which consists of one MIG gate, two Fredkin gates and one Feynman double gate. It takes $(n\text{-}2)^{th}$ bits of two binary numbers *(A, B)* and two more inputs P_{n-1} and R_{n-1} from the previous level of comparison result. Together they work to produce two outputs P_{n-2} = *(A>B)* and R_{n-2} *(A=B)* which indicates whether the given numbers A and B are equal or greater than each other. This proposed circuit is shown in Fig. 10(a). Fig. 10(b) shows the block diagram of "Greater or Equal" comparator circuit block for single-bit.

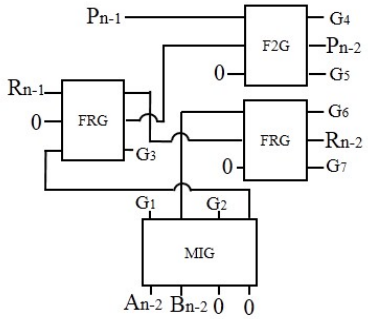

Fig. 10(a). Proposed Design of "Greater or Equal " Comparator Circuit.

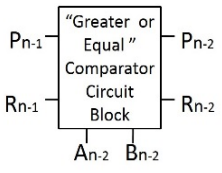

Fig. 10(b). Block Diagram of "Greater or Equal " Comparator Circuit.

F. *Proposed Design of Fault Tolerant Reversible "Less Than" Circuit Cell*

The "Less Than" circuit cell has only one proposed fault tolerant reversible gate named as FTSEG gate. The circuit which is described in previous subsection produces two outputs P_{n-2} (*A>B*) and R_{n-2} (*A=B*) and this step will be repeated until comparing the LSB (Least Significant Bit) of the two binary numbers. If A<B, it is not needed to calculate in each level of bit comparing. We can simply get this result at last step with the help of this circuit and the necessary equation for this is $F_{A<B} = (F_{A>B} \oplus F_{A=B})'$. The design is shown in Fig. 11.

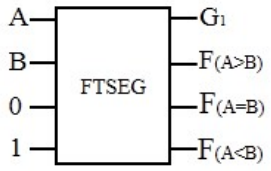

Fig. 11.FTSEG Gate Using as "Less Than"(LT) Comparator Cell.

G. *Proposed Design of Fault Tolerant 2-bit Reversible Comparator*

This subsection, shows the design of *2*-bit fault tolerant reversible binary comparator which consists of a proposed reversible MSB comparator, one single-bit "Greater or Equal" circuit block and single-bit "Less than" cell. A truth table and a design of 2-bit fault tolerant reversible comparator is shown in Table II and Fig. 12, respectively.

TABLE II. TRUTH TABLE FOR 2-BIT BINARY COMPARATOR

Input		Output		
A_1B_1	A_0B_0	$F_{A>B}$	$F_{A<B}$	$F_{A=B}$
$A_1>B_1$	×	1	0	0
$A_1=B_1$	$A_0>B_0$	1	0	0
$A_1<B_1$	×	0	1	0
$A_1=B_1$	$A_0<B_0$	0	1	0
$A_1=B_1$	$A_0=B_0$	0	0	1

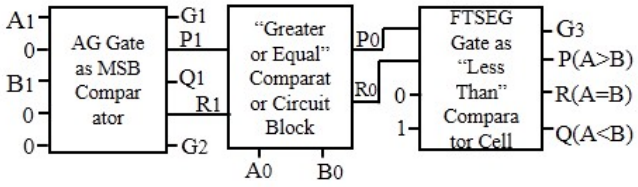

Fig. 12. Proposed Design of Fault Tolerant Reversible 2-Bit Comparator.

H. *Proposed Design of Fault Tolerant n-Bit Reversible Comparator*

We first construct a 1-bit fault tolerant reversible comparator using single AG gate. To construct *n*-bit ($n \geq 2$) fault tolerant comparator, at first we combine one MSB compararor with *(n-1)* number of "Greater or Equal" circuit blocks and at the end one FTSEG gate for "Less Than" comparator circuit cell. Proposed design of fault tolerant *n*-bit reversible comparator is shwon in Fig. 14. **Algorithm I** provides the design methodology for constructing fault tolerant reversible *n*-bit binary comparator. Time complexity of the presented algorithm is O(n) in average case.

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Algorithm I: Constructing a Compact *n*-Bit Fault Tolerant Reversible Binary Comparator

Begin

1. Take one MSB comparator circuit and assume it as M_n. Assume, output result of this block represented as *P*, *Q*, *R*. Let, *A* and *B* two *n*-bit binary numbers which MSB are $(n\text{-}1)^{th}$ bit. I_i and O_i are input and output bit respectively $(i = 1,2,\ldots)$.
2. $M_n[I_1] \leftarrow A_{n-1}$, $M_n[I_2] \leftarrow 0$, $M_n[I_3] \leftarrow B_{n-1}$, $M_n[I_4] \leftarrow 0$, $M_n[I_5] \leftarrow 0$
3. ***If*** $M_n[I_1] > M_n[I_3]$ ***then***
4. $M_n[0_2] = P_{n-1} \leftarrow 1$
5. ***Else if*** $M_n[I_1] < M_n[I_3]$ ***then***
6. $M_n[O_3] = Q_{n-1} \leftarrow 1$
7. ***Else***
8. $M_n[O_4] = R_{n-1} \leftarrow 1$
9. ***End if***
10. For each single bit "Greater or Equal" circuit block
11. ***Loop***
12. ***For*** $k = (n\text{-}1)$ *to* 1
13. Take one single-bit "Greater or Equal" cell Block C_k
14. ***If*** $k = n\text{-}1$ *then*
15. $C_k[I_1] = M_n[O_2] \leftarrow P_{n-1}$
    $C_k[I_2] = M_n[O_4] \leftarrow R_{n-1}$
    $C_k[I_3] \leftarrow A_{n-2}$, $C_k[I_4] \leftarrow B_{n-2}$
16. ***Else***
17. $C_k[I_1] \leftarrow C_{k+1}[O_1] = P_k$
    $C_k[I_2] \leftarrow C_{k+1}[O_2] = R_k$
    $C_k[I_3] \leftarrow A_{k-1}$, $C_k[I_4] \leftarrow B_{k-1}$
18. ***End if***
19. ***End Loop***
20. For the last "Less Than" comparator block, *X*

    $X[I_1] \leftarrow C_1[O_1]$, $X[I_2] \leftarrow C_1[O_2]$, $X[I_3] \leftarrow 0$, $X[I_4] \leftarrow 1$

    $X[O_2] \rightarrow C_1[O_1]$, $X[O_3] \rightarrow C_1[O_2]$, $X[O_4] \rightarrow C_1[O_1] \oplus C_1[O_2] \oplus 1$

End

Theorem I. A fault tolerant reversible *n*-bit binary comparator ($n \geq 2$) can have at least ($4n\text{-}2$) gates where *n* is the number of data bits.

Proof: In Fig. 9, it is shown that MSB comparator circuit requires one AG gate. From Fig. 10(a), we can find that "Greater or Equal" circuit block has one MIG gate, two Fredkin gate and one Feynman double gate. Fig. 11 shows that "less Than" circuit block has only one FTSEG gate. A *n*-bit comparator circuit ($n \geq 2$) requires one MSB comparator circuit, ($n\text{-}1$) number of "Greater or Equal" blocks and one "Less Than" comparator cell, so total number of gates is at least-

$$1+(n\text{-}1)*(1+2+1)+1 = 4n\text{-}2$$

Theorem II. A fault tolerant reversible *n*-bit binary comparator ($n \geq 2$) can be realized with at least ($19n\text{-}7$) quantum cost, where *n* is the number of data bits.

Proof: The MSB comparator circuit requires one AG gate where quantum cost is 8. "Greater or Equal" circuit block has one MIG gate, two Fredkin gate and one Feynman double gate and their quantum cost. are 7, 5 and 2 respectively. Thus, quantum cost of "Greater or Equal" circuit block is 19. "Less Than" comparator cell has only one gate and its quantum cost is 4. An *n*-bit comparator circuit ($n \geq 2$) requirs one MSB comparator circuit, (n-1) number of "Greater or Equal" blocks and one "Less Than" comparator cell. So, total quantum cost is-

$$8+(n\text{-}1)*(7+5+5+2)+4 = 19n\text{-}7$$

Theorem III. A fault tolerant *n*-bit reversible binary comparator ($n \geq 2$)produces at least ($7n$-3) garbage bits where *n* is the number of data bits.

Proof: The MSB comparator curcuit produces two garbage outputs.The "Greater or Equal" circuit block and last "Less Than" comparator cell produces 7 and 1 garbage outputs, respectively. An *n*-bit comparator circuit ($n \geq 2$) requires one MSB comparator circuit, (n-1) number of "Greater or Equal" blocks and one "Less Than" cell. So, total number of garbage output is-

$$3+(n\text{-}1)*7+1 = 7n\text{-}3$$

Example: A 4-bit fault tolerant reversible comparator requires 1 MSB comparator circuit, 3 "Greater or Equal" circuit block and 1 "Less Than" comparator cell, respectively. To construct this binary comparator, (4*4-2) = 14 fault tolerant reversible gate is required which produces (7*4-3) = 25 garbage outputs. Therefore, (19*4-7) = 69 quantum cost is required.

V. Simulation Resuts and Summary

The proposed designs of fault tolerant reversible binary comparators are verified through simulations using Microwind DSCH-3[12]. The simulation results shows that the comparators work correctly for all possible combinations of inputs. The simulation results for 1-bit and 3-bit fault tolerant reversilbe comparators are shown in Fig. 13(a) and Fig. 13.(b), respectively. Table III shows the summary of our proposed design for *2*-bit, *4*-bit, *32*-bitand *64*-bit, respectively. Table IV shows the generalized method of our proposed *n*-bit design for all efficiency parameters.

TABLE III. Summary of The Proposed n-Bit Fault Tolerant Reversible Comparator for 2-Bit, 4-Bit, 32-Bit and 64-Bit.

Number of Bit	Number of Gates	Garbages Output	Quantum Cost	Constant Input	Unit Delay
2-bit Comparator	6	11	31	10	6
32-bit Comparator	126	221	601	160	126
64-bit Comparator	254	445	1209	320	254

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TABLE IV. NUMBER OF GATES, GARBAGES, QUANTUM COST, CONSTANT INPUT AND UNIT DELAY REQUIRED FOR PROPOSED *N*-BIT FAULT TOLERANT REVERSIBLE COMPARATOR

Number of Bit	Gates	Garbages	Quantum Cost	Constant Input	Unit Delay
n-bit Comparator	4*n*-2	7*n*-3	19*n*-7	5*n*	4*n*-2

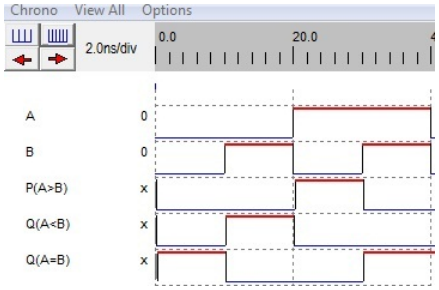

Fig. 13(a). Simulation Result of FaultTolerant Reversible 1-Bit Comparator.

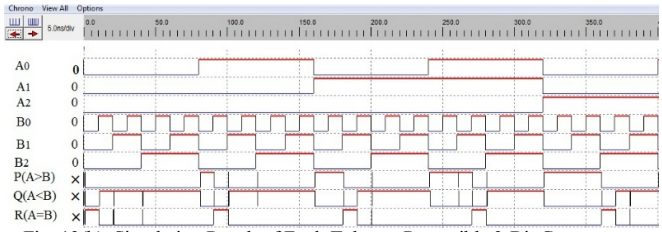

Fig. 13(b). Simulation Result of Fault Tolerant Reversible 3-Bit Comparator.

VI. CONCLUSION

This paper has represented the design synthesis of a novel approach to construct fault tolerant reversible *n*-bit binary comparator. We have also proposed an algorithm to design the compact *n*-bit comparator. In addition, we have proposed two new fault tolerant reversible gates, namely AG and FTSEG respectively and also presented two lemmas to prove parity preserving propoety of the two fault tolerant revesible gate AG and FTSEG. It has also been shown that the proposed circuit has a simple design synthesis and requires optimum numbers of gates, garbage outputs, Quantum cost and constant inputs. Simulation results of the circuit shows that the proposed comparator performs correctly. The design synthesis have also showed that proposed design is more scalable and perform much better than the Existing reversilbe approaches. Comparison of two binary numbers is useful in various applications such as microprocessors, communication systems, encryption devices, sorting networks etc [4,5,8]. So in this paper, we firstly presented parity preserving comparator.

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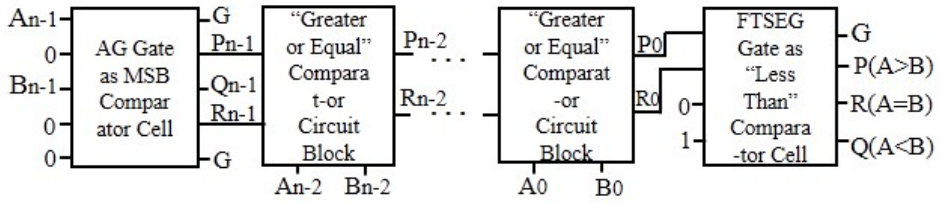

Fig. 14. Proposed Design of Fault Tolerant Reversible *n*-Bit Comparator.

REFERENCES

[1] M. Nielson and I. Chuang. "Quantum computation and quantuminformation", in Cambridge University Press, 2000.

[2] R. Landauer. "Irreversibility and heat generation in the computional process", in IBM Journal of Research and Development, 1961, pp.183-191.

[3] M. Perkowski, A.N. Al-Rabadi, P. Kerntopf, A. Buller, M. Chrzanowska-Jeske, A Mishchenko, M. A. Khan. Coppla, S. Yanushkevich, V. Shmerko and L. Jozwiak. "A general decomposition for reversible logic", in Proc RM' 2001, Startville, pp. 119 - 138, 2001.

[4] M. Perkowski and P. Kerntopf. "Revesible Logic", Invited tutorial, in proc. EURO-MICRO, 2011.

[5] C. H. Bennett. "Logical reversibility of Computation", in IBM J. Res. Dev., 1973, 17:525-532.

[6] H. M. H. Babu, M. R. Islam, A. R. Chowdhury. "Synthesis of full-adder circuit using reversible logic", in 17th international conference on VLSI Design, 2004, pp. 757-760.

[7] B. Parhami. "Fault tolerant reversible circuits", in Proc. of 40th Asimolar conf Signals, Systems and Computers, 2006, pp. 1726-1729.

[8] M. Nielsen and I. Chuang. "Quantum computation and quantum information" in Cambridge University Press, 2000.

[9] R. Wille and R. Drechsler. "BDD based synthesis of reversible logic for large functions ", in DAC, 2009, pp. 270-275.

[10] A. K. Biswas, M. M. Hasan, A. R. Chowdhury and H. M. H. Babu. "Efficient approaches for designing reversible binary coded decimal adders", in Microelectron. J,12, 1693-1703, 2008.

[11] E. Fredkin and T. Toffoli. "Consecutive logic",in International Journal theoretical Physics , vol. 21, pp. 219-253 , 1982.

[12] Microwind DSCH - Schematic Editor and Digital Simulator, http://www.microwind.net/dsch.php.

[13] Saiful Islam, M., Muhammad Mahbubur Rahman, Zerina Begum, and Zulfiquar Hafiz. "Fault tolerant reversible logic synthesis: Carry look-ahead and carry-skip adders." in International Conference on Advances in Computational Tools for Engineering Applications, 2009, pp. 396-401.

[14] Himanshu Thapliyal, Nagarajan Ranganathan and Ryan Ferreira. "Design of a comparator tree based on reversible logic." in *Nanotechnology (IEEE-NANO), 2010 10th IEEE Conference on*. IEEE, 2010.

[15] Mall, Pallavi, A. G. Rao and H. P. Shukla. "Novel Design of Four-Bit Reversible Numerical Comparator." In Ijarcce Vol. 2, Issue 4, April 2013.

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