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Design of Compact Reversible Online Testable Ripple Carry Adder

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***Abstract*— In this paper, we have presented an online testable full adder and an online testable n-bit ripple carry adder. To construct the compact online testable full adder as well as an online testable ripple carry adder, we have proposed a parity preserving adder gate namely CFTFA gate that optimizes the total numbers of gates, garbage outputs, quantum cost and constant inputs of the circuitry. We show that, the proposed designs are much better than the existing approaches considering all the efficiency parameters of reversible logic design. The proposed reversible online testable full adder using CFTFA gate achieves the improvement of 25% on the number of gates, 42.30% on quantum cost and 50% on the number of constant inputs over the existing best one. Several lemmas and an algorithm are presented to show the correctness of our proposed method.**

Keywords*— *reversible logic, CFTFA, quantum cost, garbage output, constant input, E-sop and online testability.

I. INTRODUCTION

In traditional irreversible logic, if information is lost once, input cannot be recovered from its output pattern or vice versa. In 1960, Landeur has proved that for every bit of information loss dissipates $KT\times ln2$ joules [2] of energy where K is Boltzmann's constant and T is the absolute temperature [5]. Reversible logic has showed a feature that using this logic we can recover bit loss from its unique input-output mapping. In recent years reversible logic is massively used in various technologies such as low power CMOS design, optical information processing, DNA computing, bioinformatics, quantum computing [1], thermodynamics and nanotechnology [7]. Bennett established in 1973 that a circuit must be built using reversible logic gates to avoid $KT\times ln2$ joules of energy dissipation. Since reversible gate has one-to-one correspondence between its input and output vectors [3, 4], they are free from information loss. No information is lost in reversible logic, so if the circuits consist of reversible gates [5], power dissipation would be zero.

Bit error which is referred as alteration of the value of the output bits because of internal fault of digital circuit can be detected by parity checking of input-output vectors. Testing of a reversible circuit is an important part of reversible logic design. Testing is very necessary to understand whether the reversible circuit performing its operation correctly or not. It is also very frequent that any error or fault may occur in a reversible circuit while performing operation. Testing approaches are also beginning to develop, and existing work in this area includes [14, 19, 20]. Full Adder is a combinational circuit that performs the arithmetic sum of three input bits. Full adder is a basic circuit that is used to construct other circuits such as BCD Adder, ripple carry adder etc.

In this paper, we have presented a reversible online testable full adder and an n-bit reversible online testable carry skip adder. The paper is organized with the following sections: Section II gives the Basic ideas of Reversible Gate. Section III shows the existing approaches of designing reversible online testable full adder, respectively. Section IV shows the proposed reversible parity preserving gate that is used to construct reversible online testable full adder. Section V introduces the design approach of the proposed online testable full adder and n-bit reversible online testable ripple carry adder. Section VI gives the comparison results of all the proposed circuits and with other existing researches. Finally, the paper is concluded with Section VII.

II. BASIC DEFINITIONS OF REVERSIBLE GATES AND THEIR PROPERTIES

In this section, we have represented the basic ideas and definitions some of the properties of reversible logic. Quantum realization of that properties have been also illustrated in this section.

A. Reversible Gate

It is an n input, n output circuit that produces a unique output pattern [6] for each possible input pattern (one-to-one correspondence relation).

For an $n\times n$ reversible gate if the input vector be I_v and the output vector O_v then $Iv = (I_1, I_2, I_3...I_n)$ and $O_v=(O_1, O_2, O_3...O_n)$, respectively. The relationship between them is denoted as $(I_v \leftrightarrow O_v)$ [6].

B. Online Testability

According to [14], there are two type of testing which one of this is online (concurrent testing) and another is offline (non-concurrent testing), or both can be combined. Online testing is working while the system is performing its normal operation, allowing faults to be detected in real time. Offline testing requires the system or a part of the system to be taken out of operation to perform testing, and generally involves the application of a set of test vectors that will detect all possible faults under a given fault model (a complete test set).

C. Quantum Cost

Quantum cost can be computed by substituting the reversible gates of a circuit by a cascade of elementary quantum gates [7]. Elementary quantum gates realize quantum circuit that are inherently reversible and manipulate qubits

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rather than pure logic values [8]. The most used elementary quantum gate is NOT gate (a single qubit is inverted), the controlled–NOT (CNOT) gate (the target qubit is inverted if and only if the first qubit is 1), the controlled-V gate (also known as square root of NOT and two consecutive V operations are equivalent to an inversion) and the controlled-V^+ gate (which performs the inverse operation of the V gate and thus is also a square root of NOT) [8]. Graphical representation of C-Not, V and V^+ are shown in Fig. 1(a), Fig. 1(b) and Fig. 1(c) respectively.

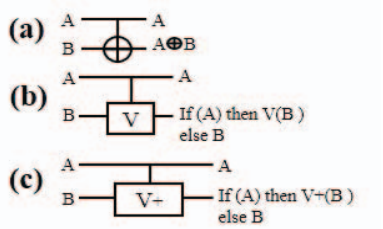

Fig. 1. Quantum Realization of Controlled (a) Not Gate (b) V Gate (c)V^+ Gate

D. Garbage Output

Unwanted or unused outputs of a reversible gate which are not used as the input of other reversible gates, are known as garbage outputs. Garbage outputs are needed only to maintain reversibility. Heavy price paid off for each garbage output [9]. The calculation of garbage output can be changed in case of using that gate in different digital circuits. Fig. 1(a) shows that for an EX-OR operation, the Feynman gate produces one garbage output.

E. Constant Input

Sometimes it is needed to apply constant input to any reversible gate for a specific logic operation. Constant input means either 0 or 1. In reversible circuit we have to minimize constant inputs because it may cause delay.

III. Background Study of Existing Reversible Online Testable Full Adders

This section have presented some of the previous approaches of online testability. Subsections III.A, III.B and III.3 have discussed about those approaches.

A. Testable Circuit Design Using Online Testable Gates

Thapliyal and Vinod [13] proposed an approach using a new *4×4* reversible online testable gate (OTG) that is introduced in their work having parity output at S. The R2 gate [14] is combined with the OTG to design a block that is online testable. Two parity outputs of the testable block (R and S) are compared to check whether the block is faulty or not. In [14], the two pair two-rail checker circuit was constructed using eight R gates, whereas Thapliyal and Vinod constructed the checker circuit using four *3*-bit Toffoli gates [12] and two 3-bit Fredkin gates [12]. To build an online testable adder by using Thapliyal and Vinod proposed approach total eight reversible gate sand total 40 quantum cost will be required. It is very costly with respect to our proposed method. This assumption is shown in table 1.

B. Construction of a Testable Circuit from the ESOP based Circuit [16]

One method for constructing any reversible circuit is to use E-Sop technique and it is referred as Exclusive-or sum of product. As we know Toffoli gate can be used to generate any kind of Boolean expression, in E-Sop technique for each ESOP term (product) of each output a Toffoli gate is added at the end of the circuit. This method was proposed in [15] and creates a circuit with p input lines and q output lines. N. M. Nayeem and J. E. Rice [16] proposed a technique for online testing of E-Sop based circuit. They proposed a gate named *n*-bit ETG [16] (*n*-bit Extended Toffoli gate) which replaces the n-bit Toffoli gate without changing any functionality of the circuit. This method requires a parity line L which is initialized with zero. Though its input and output lines are different, it requires too many ETG gate of *n*-bit (n = 1, 2, 3…). Its quantum cost is also very high with respect to our proposed method. This assumption is shown in Table 1 where this method is compared with respect to our proposed method.

C. Construction of a Testable Circuit from the General Toffoli Circuit [16]

As we know Toffoli can generate any kind of Boolean operation, Toffoli circuits consists of only Toffoli gates including NOTs, CNOTs and negative-control Toffoli gates [16]. Unlike E-SOP circuit, in general Toffoli circuit input lines can become output lines. This technique also requires a parity line L which is initialized with zero. At the beginning and end of the given circuit from each line to *L,* one for each CNOT gate is inserted. An *(n+1)*-bit ETG replaces every *n*-bit Toffoli gate. The connections of the first *n*-bits of the ETG are kept the same as that of *n*-bit Toffoli gate. The last bit of the ETG is connected to *L*. If we construct an online testable full adder using this technique, more reversible gates and quantum cost will be required with respect to our technique. This assumption is shown in table 1 where this technique is compared with respect to our technique.

IV. Design of Proposed Parity Preserving Reversible Gate

In this section, a new parity preserving gate namely CFTFA proposed for to construct online testable full adder. Some of its basic property is also presented.

A. Proposed CFTFA Gate

In this subsection, a new *5×5* reversible gate namely CFTFA gate is proposed. The proposed gate and its quantum realization are shown in Fig. 2(a) and Fig. 2(b), respectively. In Fig. 2(b) each dotted rectangle is equivalent to a *2×2* CNOT gate so the quantum cost of CFTFA gate is 7. It can be notified from the truth table that the input pattern corresponding to a particular output pattern can be uniquely determined and input-output bit parity is also preserved. The timing diagram of the proposed gate is shown in Fig. 2(c).

Lemma 1: CFTFA is a parity preserving reversible gate.

Proof: The input vector and output vector of CFTFA gate be I_v = *{A, B, C, D, E}* and O_v = *{(A⊕C)(B⊕D)⊕BD⊕C, (A⊕C)(B⊕D)⊕BD'⊕C, A⊕B⊕ C⊕D, B⊕D, D⊕E}* respectively.

Getting input parity by EX-ORing all inputs is
=A⊕B⊕C⊕D⊕E
To get output parity, we have to EX-OR all the outputs and we get,
=(A⊕C)(B⊕D)⊕BD⊕C⊕(A⊕C)(B⊕D)⊕BD'⊕C⊕A⊕B⊕C⊕ D⊕B⊕D⊕D⊕E
= A⊕B⊕C⊕D⊕E
Which is equal to input parity and it also satisfies the property. So, from the above explanation, it is shown that the CFTFA is a parity preserving gate.

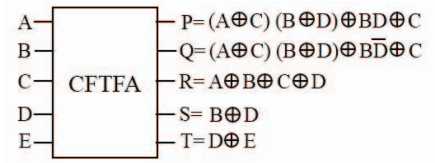

Fig. 2(a). Block Diagram of Proposed CFTFA Gate

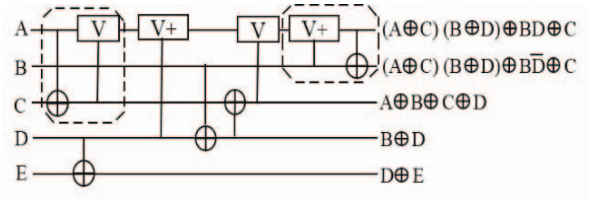

Fig. 2(b). Quantum Realization of Proposed CFTFA Gate

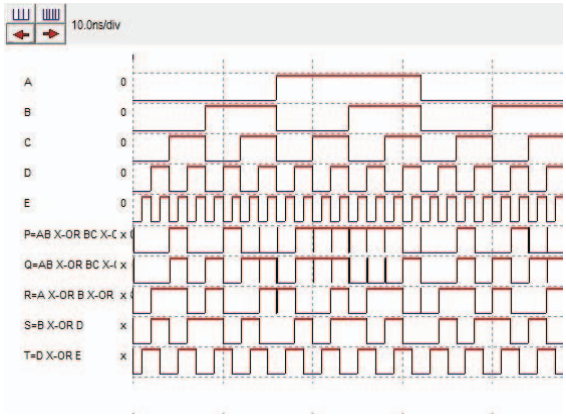

Fig. 2(c). Timing Diagram of Proposed CFTFA Gate

Algorithm I: Constructing a Reversible Full Adder Using CFTFA Gate

Begin

1. Take one CFTFA gate. Let I_n and O_n of its input and output vectors respectively. We have to add two binary numbers A and B. Assume C_{in} is carries return.
2. Input vector of CFTFA gate as a adder represented as $I_1 \leftarrow A$, $I_2 \leftarrow B$, $I_2 \leftarrow 0$, $I_4 \leftarrow C_{in}$, $I_5 \leftarrow 0$
3. Output vector of CFTFA gate as a adder represented as $O_1 \rightarrow C_{out}$, $O_3 \rightarrow Sum$

End

V. Designs of Proposed Online Testable Full Adder and Online Testable *N*-bit Ripple Carry Adder

Reversible online testable adder circuit is able to detect any single bit faults when the circuit is performing its operation. In this section we will describe approach to construct online testable full adder by using CFTFA gate.

A. Design Approach for Online Testable Full Adder Using Proposed CFTFA Gate

In this section, we construct proposed online testable full adder by using CFTFA gate. Elementary circuitry using this approach is shown in Fig. 3.

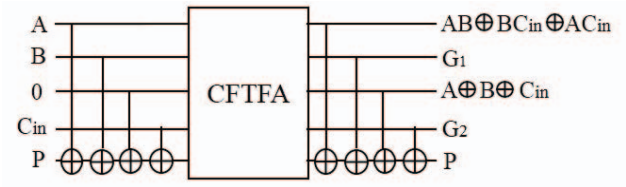

Fig. 3. Online Testable Full Adder Using CFTFA Gate

It is shown above in Lemma 1 that CFTFA is a parity preserving reversible gate. According to parity preserving reversible gate we know that EX-ORing all its inputs to the outputs causes zero. CFTFA gate's last input line has no control on the other input line. So, last line can be used as a parity line P. In order to test the circuit, a CNOT gate is inserted from each input line to the last line (parity line *P*) of CFTFA gate at the beginning and end of the given circuit. Value of the parity line P of CFTFA gate is set to either 0 or 1. If no error is occurred during the operation of the circuit, its value will remain same. E.g. if input of *P* is 0, we get the output result also 0. Now in the resulting circuit, if a single fault occurs in any line or even in last line or parity line P, the output value of parity line will become complementary to its input value. In Fig. 3 one CFTFA gate is used to construct an online testable full adder.

Lemma 2: The proposed online testable full adder circuit using CFTFA gate can detect any bit fault concurrently.

Proof: As described above, we only consider the last line or parity line *P* of CFTFA gate because this line will detect whether any error is occurred or not.

Case 1 Considering Fig. 3, assume a single bit fault occurs in an input line (except parity line *P*) of a CFTFA and propagates to multiple lines.

In an online testable reversible full adder we use only one CFTFA gate. In this manner, three condition arises which are given below.

I. At beginning of the full adder circuit all four line of the *5×5* CFTFA gate is EX-ORed to parity line *P*. Assume the value of parity line *P* is *T*. So, just before the first gate the value of *P* is *X*. Therefore, $X = C_{in} \oplus A \oplus B \oplus 0 \oplus T$

II. Let the end of CFTFA gate, the value of *P* is *Y*. Therefore $Y = C_{in} \oplus A \oplus B \oplus T \oplus C_{in}$

III. Let the end of circuit when all outputs are EX-ORed with parity line, the value of *P* is *L*. Therefore,

$$L = C_{in} \oplus A \oplus B \oplus T \oplus C_{in} \oplus AB \oplus BC_{in} \oplus AC_{in} \oplus B \oplus AB \oplus B$$
$$C_{in} \oplus AC_{in} \oplus A \oplus B \oplus C_{in} \oplus B \oplus C_{in} = T$$

As input faulty value propagates to multiple lines, any single bit error occurring on a line before first CFTFA gate, the value of *Y* must be complementary and it will be *Y'*. As well as *L* will be *L'*.

Therefore, *L'=T'*. As parity line P's output value is complementary to its input value, we can detect a single bit error on it.

Again if any single bit error is occurred on a line after CFTFA gate, *L* will be *L'*. Therefore, *L'=T'* and we can detect a single bit error by examining parity line that discussed above.

Case 2 A fault can also be occurred on parity line *P*. This causes the value of parity line *P* is *T'* as it was initialized with *T*. Thus, the circuits detect fault. *A* single bit fault occurs on any line except parity line *P* can cause other lines faulty. As

parity line *P* has no control on other lines, this faulty value does not propagate to any other line.

From above explanation we have seen if no error is occurred, the parity line value will remain same. Checking the parity line we can detect any single bit fault.

B. Design Approach for Online Testable Ripple Carry Adder using CFTFA Gate

Firstly, in this subsection 4-bit online testable full adder is constructed and then reversible online testable adder is generalized for *n*-bit.

1. *Proposed Online Testable 4-bit Ripple Carry Adder*

   Here four CFTFA gate is needed to construct *4*-bit Ripple carry adder. For two binary number *A* and *B*, A_0 and B_0 is assigned into first CFTFA gate. Another input carry C_{in} or C_0 is also inserted in it. In the second CFTFA gate, A_1 and B_1 is inserted and its *Cin* is assigned from previous CFTFA Gate's C_1 output. This process will be repeated four times. Each and every inputs and outputs are Ex-ored with the parity line *P*. If any single bit error is occurred in the circuit, it will be detected from the parity line. The value of the parity line is inverted from its given value, if any single bit error is occurred. The necessary circuitry of the proposed online testable *4*-bit ripple carry adder is shown in Fig. 4.

2. *Proposed Online Testable n-bit Ripple Carry Adder*

   Proposed online testable reversible *n*-bit ripple carry adder is constructed following the same procedure as online testable reversible 4-bit ripple carry adder. The proposed online testable *n*-bit ripple carry adder is shown in fig. 5.

VI. Comparison Results and Summary

Table I shows the comparative study of our proposed approach with existing design approaches for online testable full adder as well as it presents the improvement ratio in percentage of our proposed approach and existing best approach in several performance matrices such as number of gates, quantum cost etc. Table II shows the summary result of the proposed online testable 4-bit ripple carry adder and *n*-bit ripple carry adder.

TABLE I. Comparison of our Proposed Approaches with Previous Approaches for Online Testable Full Adders

Methods	Number of Gate	QC	GO	CI
Proposed	9	15	2	1
1st Approach of Existing[16]	14	35	3	3
2nd Approach of Existing[16]	12	26	2	2
Existing[13]	8	41	10	8
Improvement Ratio of Proposed Approaches With Respect to 2nd Approach of Existing[16]	25%	42.30%	0%	50%

QC = Quantum Cost, CI = Constant Input, GO= Garbage Output

TABLE II. Summary of Online Testable Ripple Carry adder Using CFTFA Gate

Methods	Number of Gates	QC	Garbage	CI
Proposed online testable 4-bit ripple carry adder	30	54	8	4
Proposed online testable *n*-bit ripple carry adder	$7n+2$	$13n+2$	$2n$	n

QC = Quantum Cost, CI = Constant Input, GO= Garbage Output

VII. Conclusion

This paper has represented the compact design synthesis of an online testable reversible full adder and online testable *n*-bit ripple carry adder. In addition, we have proposed a reversible gates, namely CFTFA gate to construct the adders. We have showed the efficiency of proposed designs over existing approaches using several comparison tables. The main property of both the presented online testable adder and n-bit ripple carry is that one input line of the adder has no control on the other input line which can be used as parity line as well as parity line is used to detect bit errors. As our proposed gates are used to construct reversible online testable full adders, we have presented one algorithm and a design approach for online testable reversible full adder using proposed gate. It has also been shown that the proposed circuit require the optimum numbers of gates, garbage outputs, quantum cost, delay and constant inputs. Lemma 2 presented the proofs of online testability of the proposed adder. As the full adder is used in various circuits such as multiplier, carry skip adder [10], BCD adder, divisor etc., the proposed adders may help to construct these circuits as online testable.

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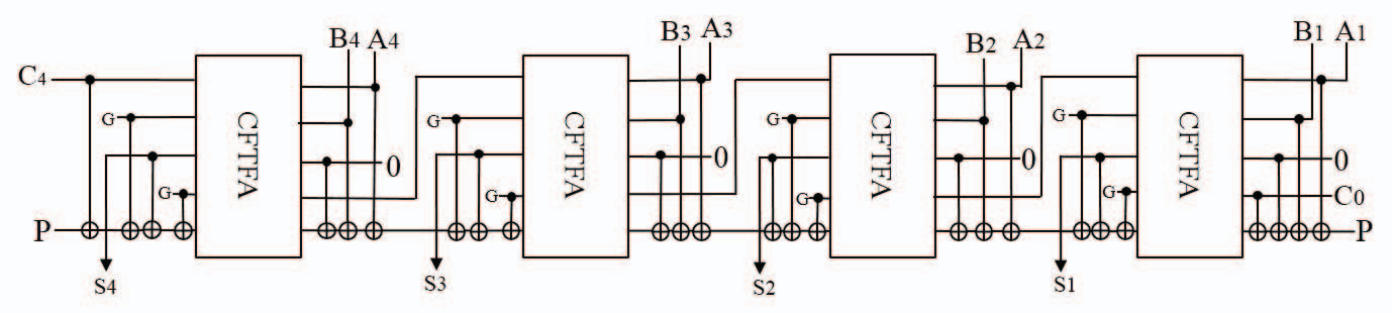

Fig. 4. Proposed Circuitry of Online Testable Reversible 4-bit Ripple Carry Adder

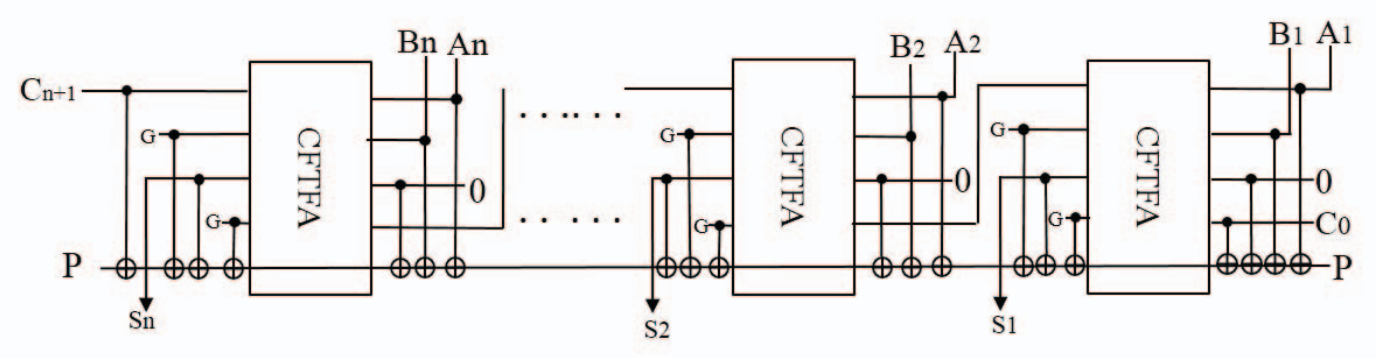

Fig. 5. Proposed Circuitry of Online Testable Reversible *n*-bit Ripple Carry Adder