EE213
Digital Integrated Circuits II

Lecture 08A: Adders

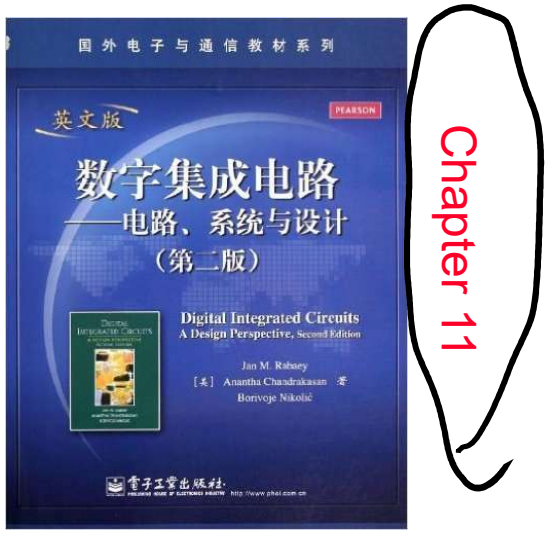
Prof. Pingqiang Zhou

http://sist.shanghaitech.edu.cn/faculty/zhoupq/Teaching/Spr17/Digital-IC-2.html

ShanghaiTech University
School of Information Science and Technology

Materials Were Partly Taken From

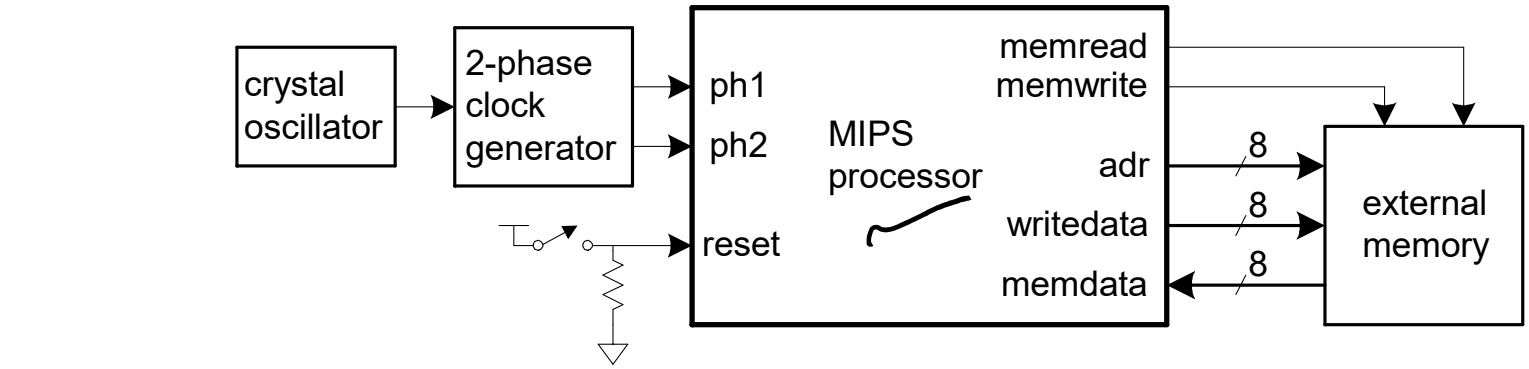
- EE141: Digital Integrated Circuits, Spring 2010. http://bwrcs.eecs.berkeley.edu/Classes/icdesign/ee141_s10/index.htm

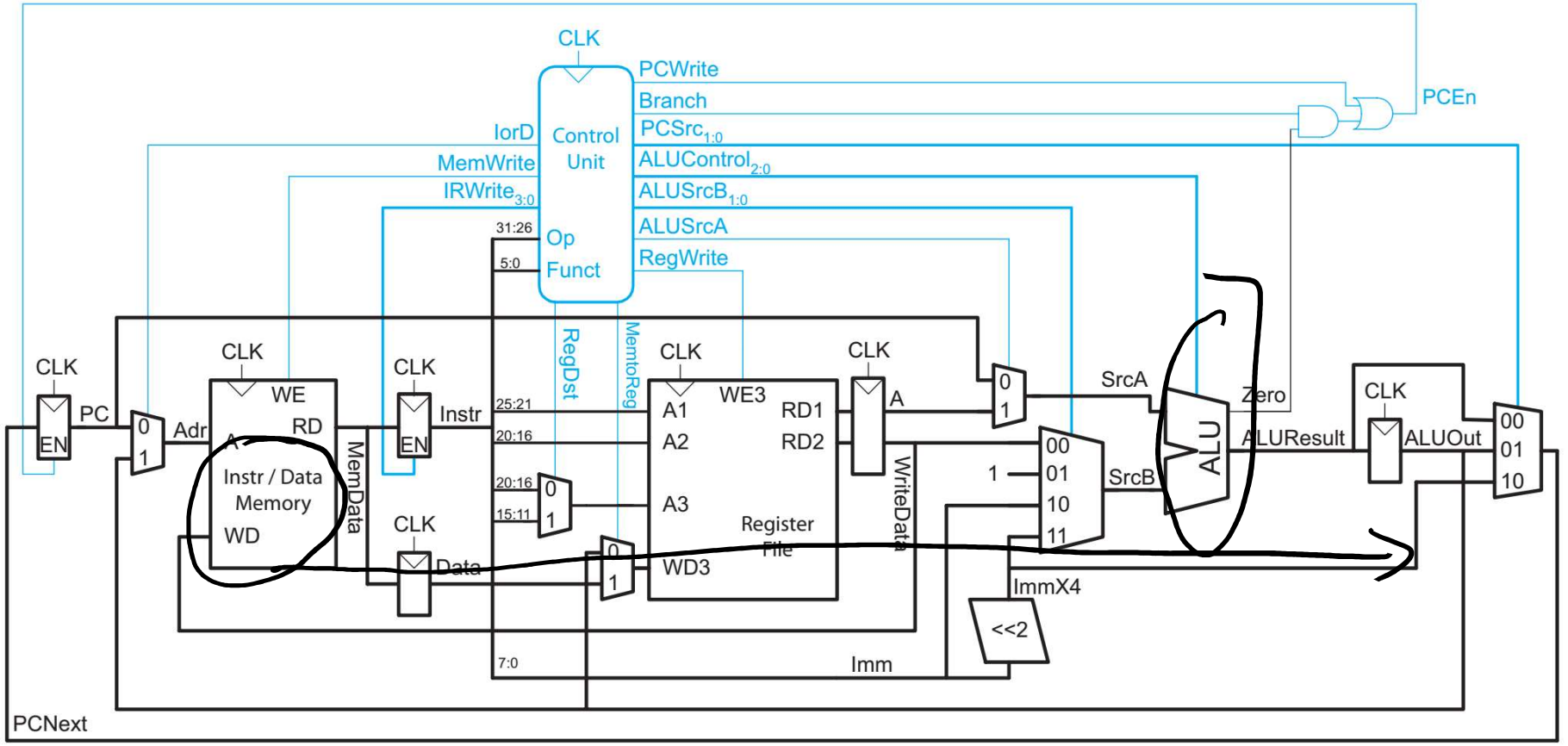


Chapter 11

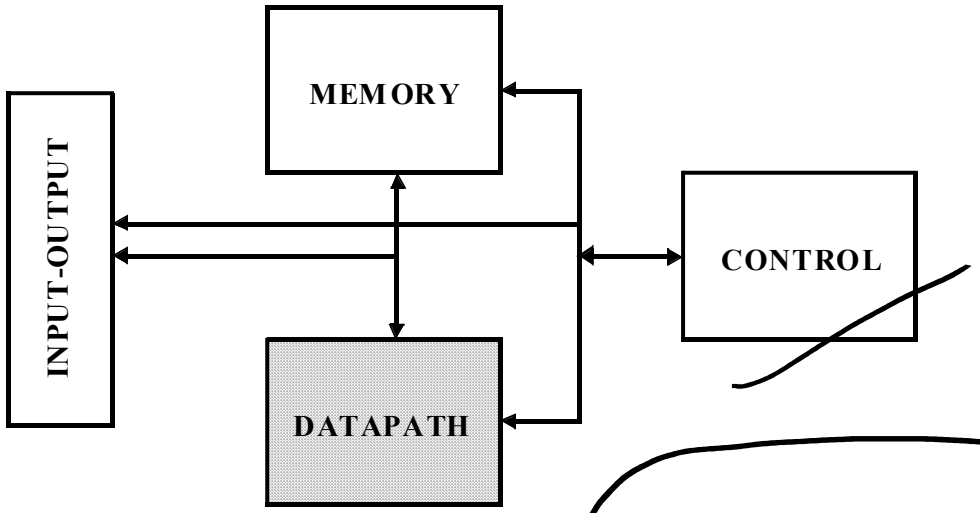
Chapter 10

Review: MIPS Processor



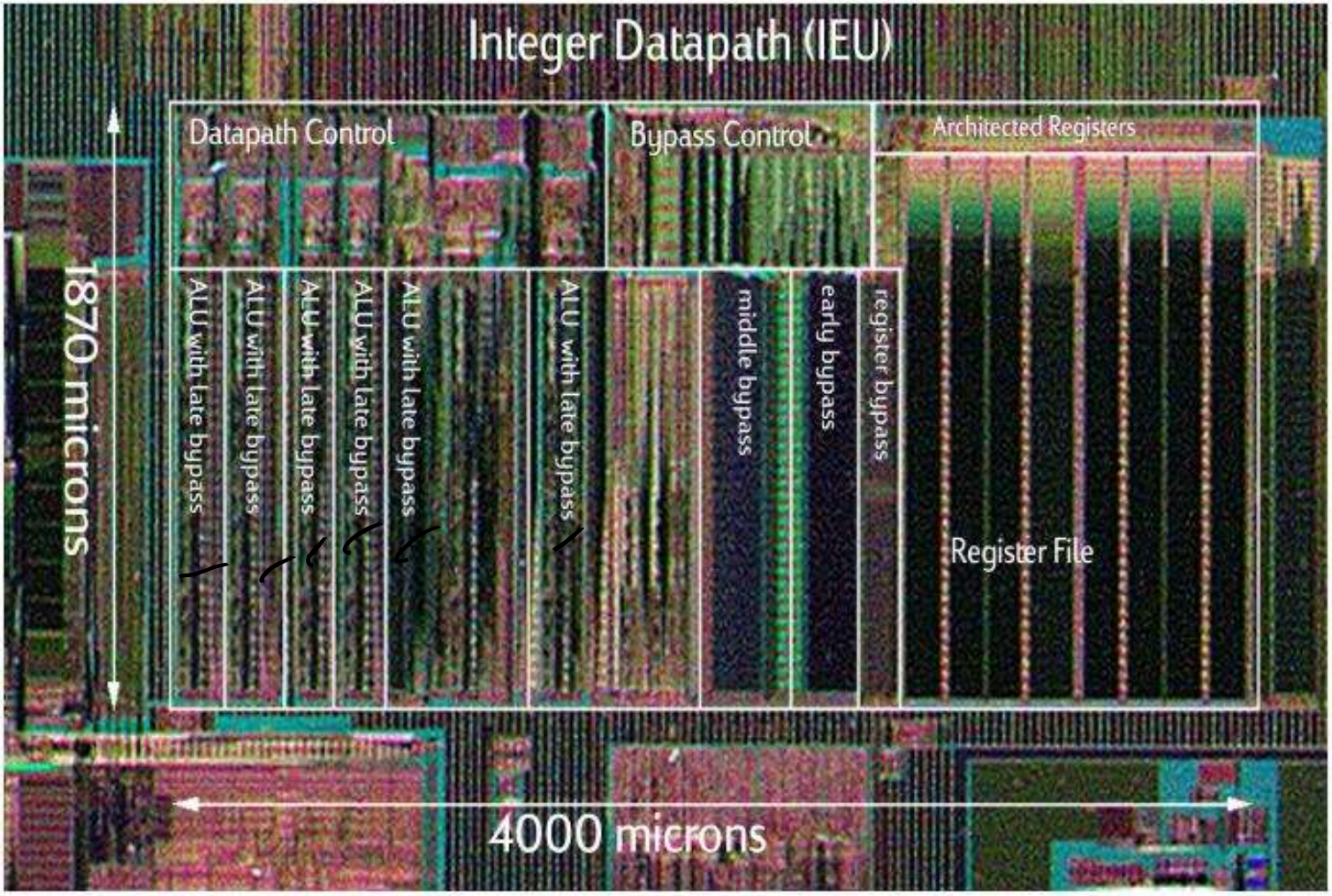


A Generic Digital Processor



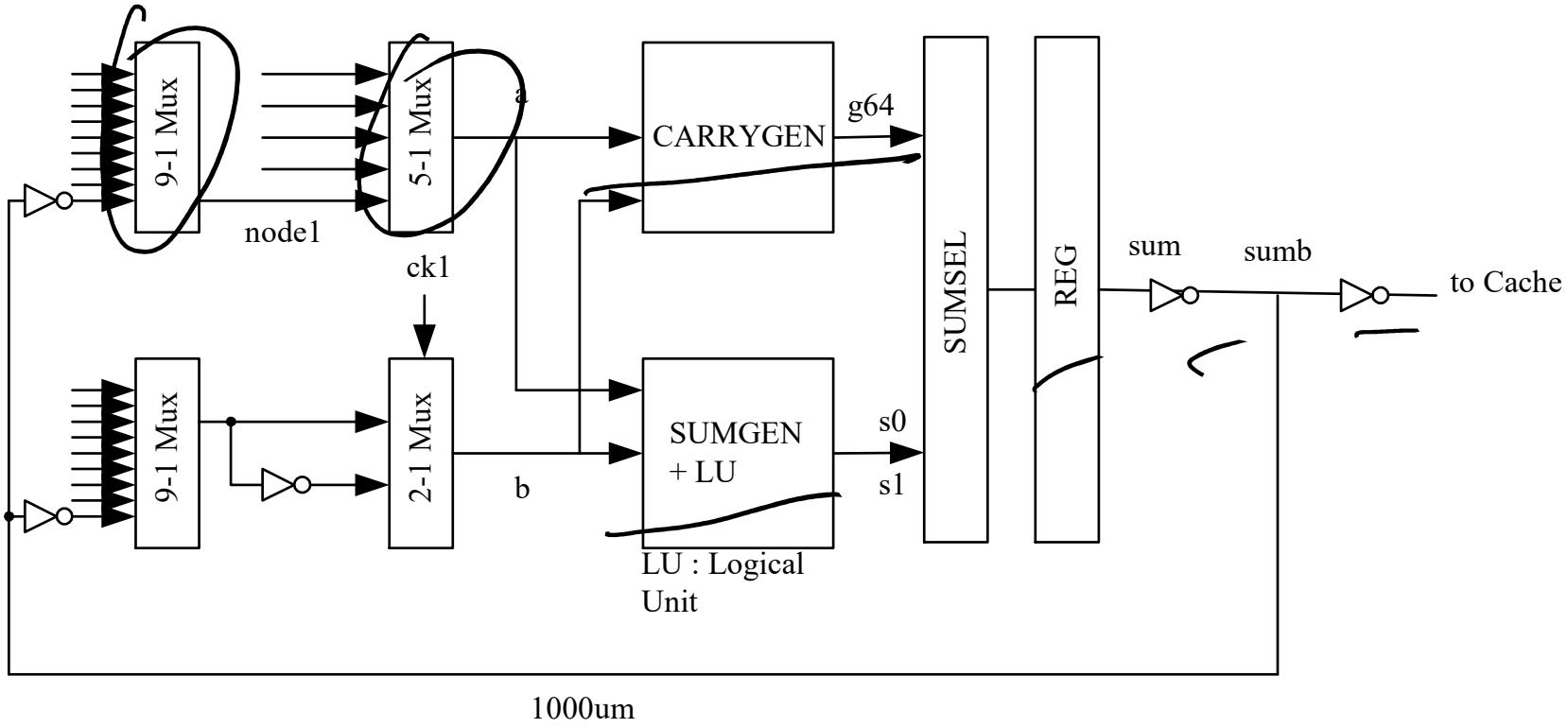
- Datapath
  - Execution units
    - Adder, multiplier, divider, shifter, etc.
  - Register file and pipeline registers
  - Multiplexers, decoders
- Control
  - Finite state machines (PLA, ROM, random logic)
- Interconnect
  - Switches, arbiters, buses
- Memory
  - Caches (SRAMs), TLBs, DRAMs, buffers

An Intel Microprocessor - Itanium



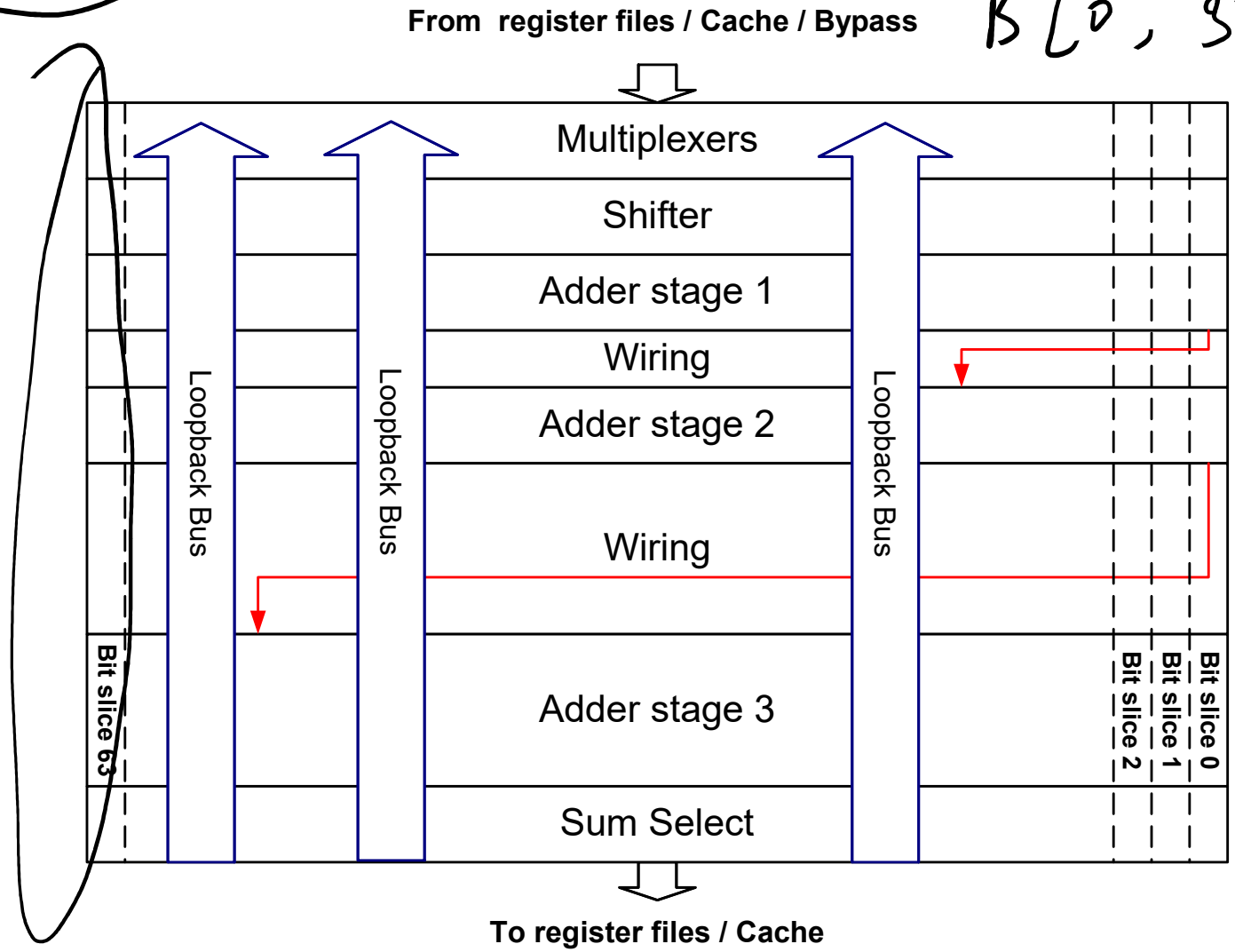
Fetzer, Orton, ISSCC'02

Itanium Integer Datapath (ALU)



Itanium has 6 integer execution units like this.

Bit-Sliced Datapath

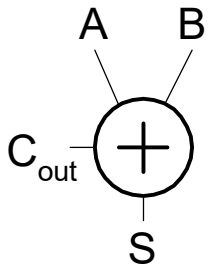


Outline

- Single-bit addition
- Circuit design considerations
  - Static CMOS adder
  - Mirror adder
  - Inversion property
  - Manchester Carry Chain
- Logic design considerations
  - Carry-bypass (or skip) adder
  - Carry-select adder
  - Tree Adder

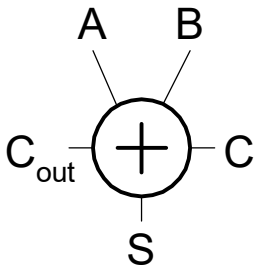
(Single-Bit) Binary Addition

Half Adder



A	B	C_{out}	S
0	0		
0	1		
1	0		
1	1		

Full Adder



A	B	C_{in}	C_{out}	S
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		