Number system	Conversion	Logic Gates								Table	
Binary: 0/1	B->D: add each '1's	AND	- D-	$x \cdot y$	NAND	70-	$\overline{x \cdot y}$	Show input		× 9 f	f=X9
Decimal: 0~9	D->B: divide by 2		→	x + y	NOR	1200	$\frac{1}{x+y}$	and output		000	+74
Hexadecimal: 0~F	B<->H:4bit B=1bit H	NOT	- >>-	\bar{x}	XOR	*	$x \oplus y$	one tab		0 (1	=X⊕Y CXOR)
Significant bit		s and Rules for Boolean						BoolAlg Order			products
1 HIGH	$0\cdot 0=0, 1\cdot 1=1$	$x \cdot x = x$			$x \cdot (y+z) = x \cdot y + x \cdot z$			Parentheses		Add all midterms	
TO LOW	$0 \cdot 1 = 1 \cdot 0 = 0$	$x + \bar{x} = 1$		$x + x \cdot y = x$		(bracket)		where output=1			
	$x = 0, \bar{x} = 1$	$\bar{\bar{x}} = x$			$xy + x\bar{y} = x$ $\overline{xy} = \bar{x} + \bar{y}$			→ NOT		$f = \sum_{i=1}^{n} m_{(f=1)}$	
MOST LEAST,	$ \begin{aligned} x \cdot 0 &= 0 \\ x \cdot 1 &= x \end{aligned} $	$x \cdot y = y \cdot x$ $x \cdot (y \cdot z) = (x \cdot y) \cdot z$			$xy - x + y$ $x + (\bar{x} \cdot y) = x + y$			→ AND → OR		(Canonical term)	
SIGNIFICANT BIT Product of sums	Synthesis and Cost	Multiplex (MUX)		2:1 Multiplex			S		A		
Add all maxterms	Synthesis: add all	Selects one signal		_			. 1		B		
where output=0	min/maxterms into	between multiple		A TO F = ASTBS			40 -10 + fo		[*] [n Hit f	
	minimal cost form	signals		B			80 -11		c —	H-1	
$f = \prod M_{(f=0)}$	Cost = #Gates +	Depends on another		Š			Al -OL fI		D-14		
(Canonical Term)	#inputs	digital signal(s) "S"					BI - LI		S	o SI	
module name (a,b,t,f)	Hierarchy	Common cathode		Lookup table (LUT)			Χ°	x. f	Half Adder		
input a, b, t; output f;	Add sub-modules	Turns on when		Programmable gate array,			X. X. f 00 fo X. Tur f 0 1 fi		a p a p s1 20		
assign f=(~t&a) (t&b);	into main module	segment value is 1		hold interconnection						70000	
endmodule	(similar with functions)	(anode -> 0)			'code' of the gates			51 50 (01001
Full Adder	ai bi in	Always block			output reg out;			ALU		reg out;	<u> </u>
(25) (C1) rao	FULL	Defines behaviour			always@(*)			X - 1 3 6		always@(* begin	,
0(2)	CARRY ADDER CARRY	using procedural			begin					case(??)	
+ 162 lb1 100	CARRY ADDER CARRY	statements		(procedural stmt)			19 -5-132			& default)	
C3 S2 S1 S0	Si out	(output reg ~~)			end			OP ,		endcase end	
ALU example	Karnaugh map	X2X3 00 01 11 10			5-bit K map			- 1			ny group of
X 3 X+y A 3 C	XI X2 F XX2 O I	00 m0 m1 m3 m2 01 m4 m5 m7 m6			++*********			oomplomone .		ants that	
y / 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1	0 0 f0 0 f0 f1 0 1 f1 1 0 f2 1 f2 f3			, ri			Implicant. 15 III /:			ers all 1s ation form)	
3 - 100	$\begin{bmatrix} 1 & 0 & f^2 \\ 1 & 1 & f^3 \end{bmatrix}$ $\begin{bmatrix} 1 & f^2 & f^3 \end{bmatrix}$	1 1 m/2 m/3 m/5 m/4		X4 [6]		SOF, USTITE OS Essor			P.I.: Pls not		
4A11 17 12	2D table! (right)	10 m8 m9m1/m10			A Thr			Prime implicant in contact w			
-				NVV			(PI): groups of 1s			Pls	
Constru	Don't care			(X) XX/00 01 11 10 f(X1/X2/X3/X4)			Sequential circuit		State		
1. Find all prime implic	Output doesn't matter			01 1 0 1 1 = 2111(2,4,6,7,4)			Output depends on input and past		Function of past values, must be		
2. Identify essential p	for my purpose Indicated as 'X'			11 0 X X 0 +2D(0,3,10,13,15)							
3. Choose non-esser	\$70,000 PER PROPERTY PROPERTY SEE (CONSESSED - \$70. 15						values (state)			mbered k D QCt+1)	
0 7 5	O Remember State					Clock Load I O O					
N Q	0 0 Q(t) Q(t)	K-	Clock			(0 0 Q(t) Q(t)			Court La Que de la		
a Da a	10 1 0							Store O G			QCt)
RS Latch	1 1 Oct Dontuse	S			1 1 Don4 use			Gated D Latch Store O 1 Que			. I .
Flip Flop	Positive edge fli				1		Negative edge flip-flop				
Storage element,	DIDIO	D		Qn D Q	•	D-F	7-Q	D - D			
change output at	Latch -	CIK DO CIK CUK à			→ dk						
edge of clock	CIK - Latch - Q	UK PIN BI			posedge			CIK TOK 6 CIK OP Negedge			
Prese tN=0 PresetN-	ACTIVE ON O PresetN	TIVE ON 0 Presetty Synchronou						D[0]	oī ~	CO12 -	
DIPORTOR OFMIO		Dependent on clock			Output changes			DC0 - QL3:01 - QL3:01			
CIK-TOO DO DO	Da CIK-			independent on clock			DD CIK				
ClearN=D	Presetth cleanty Q Cleanty O X ACTIVE ON O	always@(posedge clk)			(resetN, presetN)		DIST - Q[3] OPOSE		osedge clk		
Q=0 ClearN				· · · · ·							
D		Blocking (=)			Non-blocking (<=)			Don't do a 7 21			
CIK-PORPER OF	2 1 1 10000	Assignments in always block are evaluated in		Assignments in always			Put output into b				
ResetN	3 1 1 1 0 0 0							two always block			$\rightarrow + X$
	order (order matte							Poduction Arithmetic Country			
Verilog tips	Bitwise expression			number Relations		Reduction			ncatenate		
No initial statement	Result -> length(in)			n bits >, <, >=, <=, ==		&a la			out={b,a}		
(use always) Draw schematics!	~A, A B, A&B, A^B	!A, A B, A&&B bina ex) 3'		*				en out[5:0] b[1:0]			
- Diam Schellighes;	İ		ex) 3		וטומ				\cup [\cdot . \cup]		
					l			elements			a[3:0]