THE AMERICAN UNIVERSITY IN CAIRO
الجامعة الأمريكية بالقاهرة

Project 1 Report

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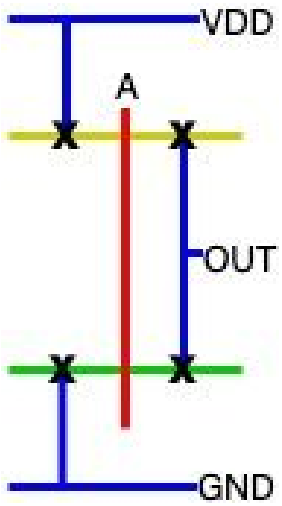
To
Professor. Mohamed Shalan

CSCE 3304-01
Due date: Oct, 26th, 2019

1. **Stick Diagrams, Transistor Sizes, Schematic Designs, and Layouts:**

Inverter:

Stick Diagram:



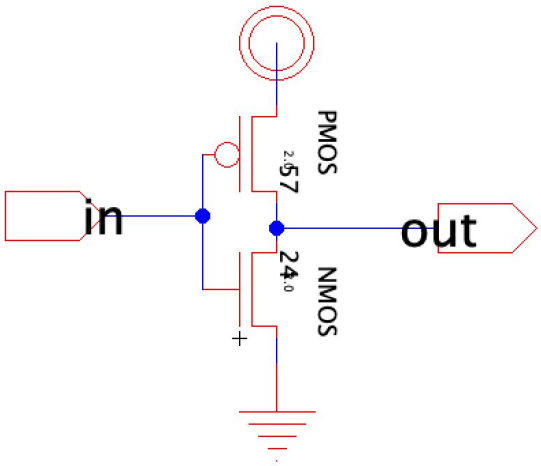
Minimum Estimated height = 1 + 1 + 1 + 1 + 1 = 5 ∗ 8λ = 40λ
Size (1):
PMOS: 3*1*2.4*1 ~ 7 (width)
NMOS: 3*1 = 9

Size(2):
PMOS: 3*1*2.4*2 ~ 14 (width)
NMOS: 3*1*2 = 6

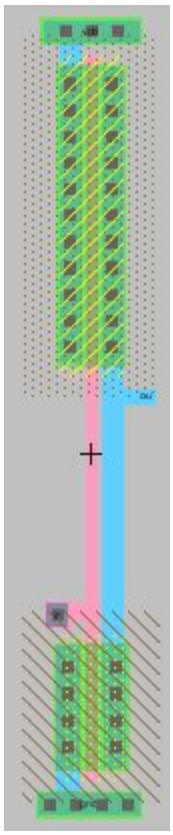
Size(4):
PMOS: 3*1*2.4*4 ~ 29 (width)
NMOS: 3*1*4 = 12
Size(8):
PMOS: 3*1*2.4*8 ~ 57 (width)
NMOS: 3*1*8 = 24

Inverter:

Schematic Diagram:

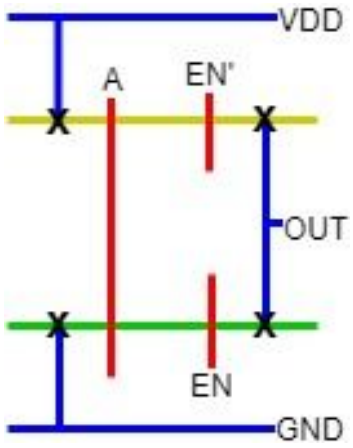


Layout:



Tri-state Inverter:

Stick Diagram:



$Minimum\ \ Estimated\ height\ = 1 + 1\ +\ 1\ + 1\ + 1\ = 5 * 8\lambda = 40\lambda$

Size (1):

PMOS: 3*2*2.4*1 ~ 14 (width)

NMOS: 3*2*1 = 6

Size(2):

PMOS: 3*2*2.4*2 ~ 28 (width)

NMOS: 3*2*2 = 12

Size(4):

PMOS: 3*2*2.4*4 ~ 57 (width)

NMOS: 3*2*4 = 24

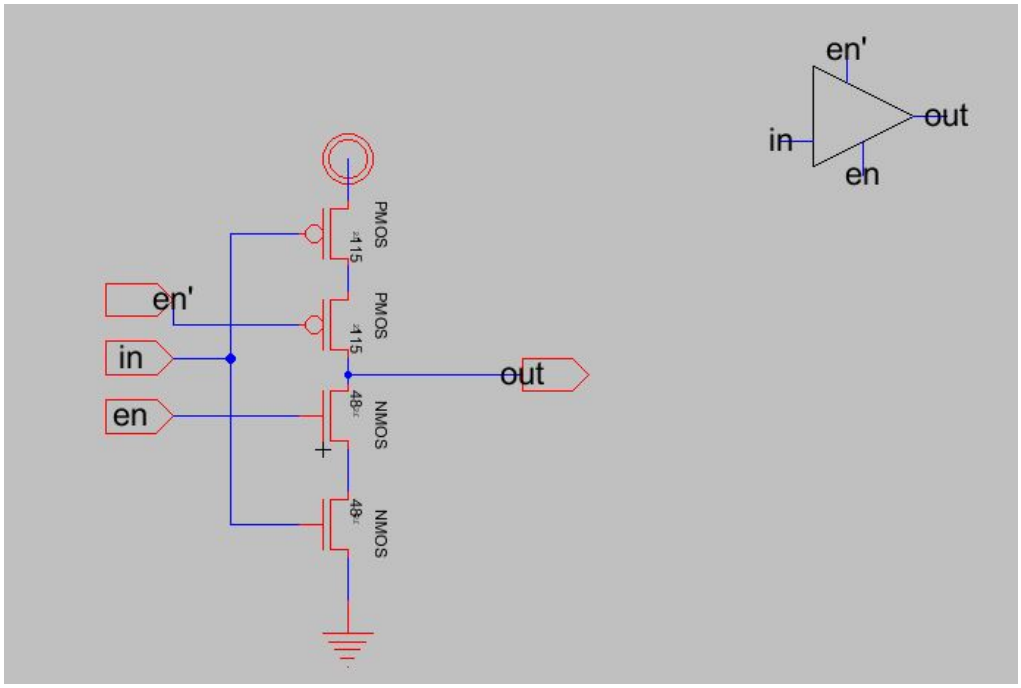
Size(8):

PMOS: 3*2*2.4*8 ~ 115 (width)

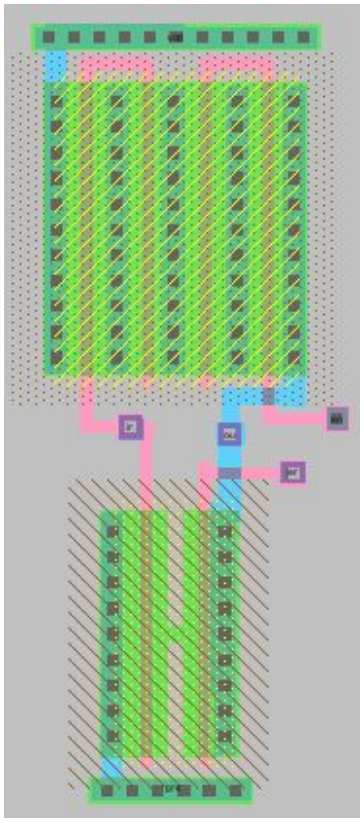
NMOS: 3*2*8 = 48

Tri-state Inverter:

Schematic Diagram:

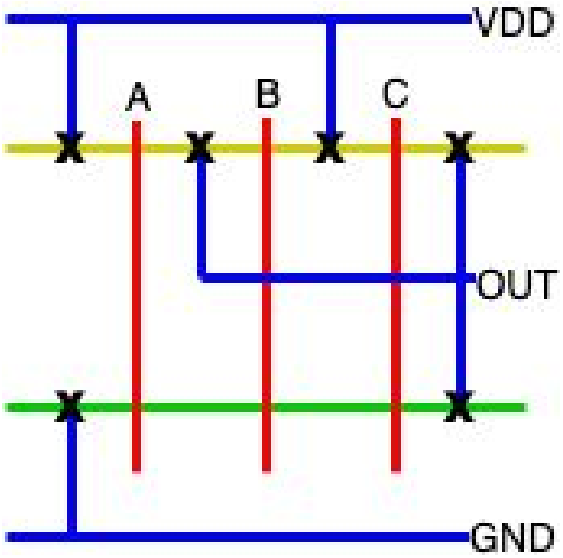


Layout: Width = 68 λ



3-input NAND gate:

Stick Diagram:



Minimum Estimated height $= 1 + 1 + 1 + 1 + 1 = 5 * 8\lambda = 40\lambda$

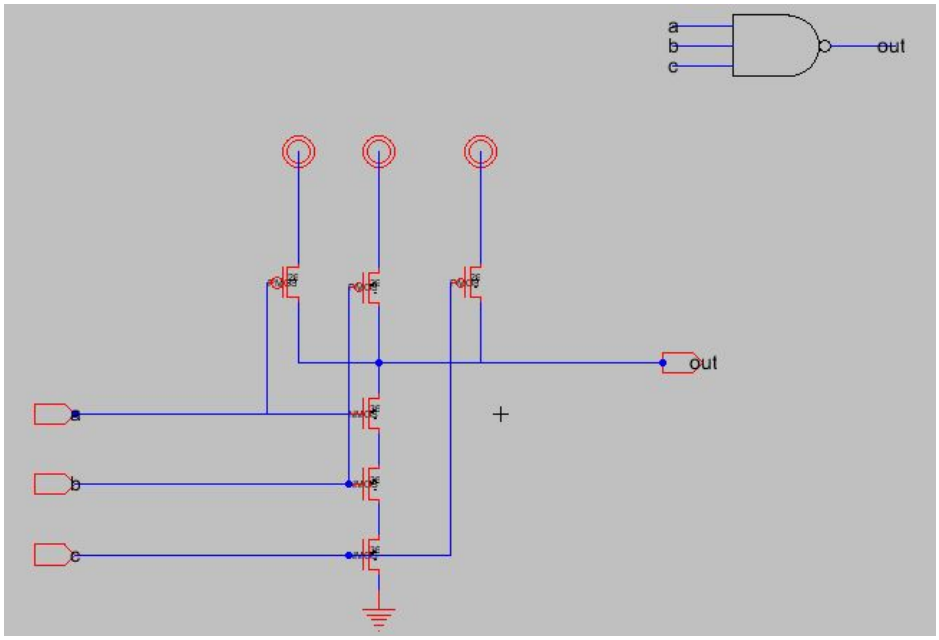
Size (1):
PMOS: 3*1*2.4*1 ~ 7 (width)
NMOS: 3*3*1 = 9

Size(2):
PMOS: 3*1*2.4*2 ~ 14 (width)
NMOS: 3*3*2 = 18

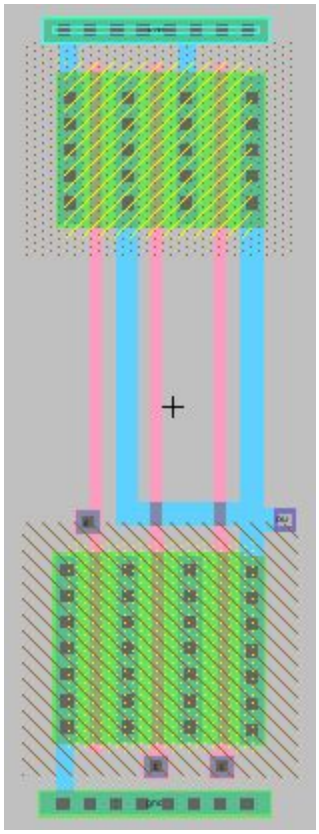
Size(4):
PMOS: 3*1*2.4*4 ~ 29 (width)
NMOS: 3*3*4 = 36

3-input NAND gate:

Schematic Diagram:

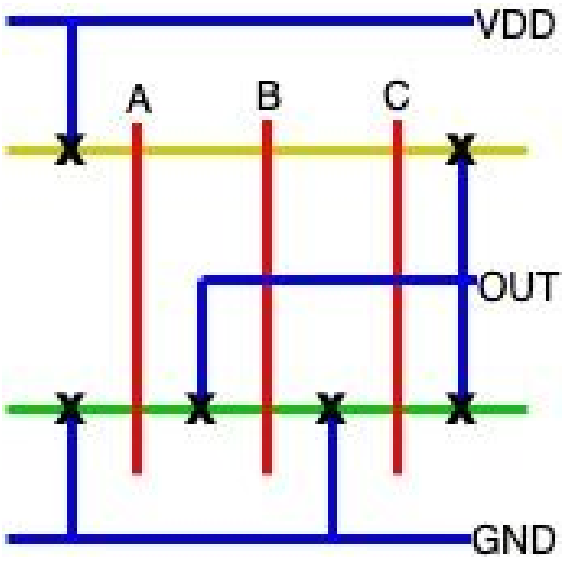


Layout: Width = 56 λ



3 input NOR gate

Stick Diagram:



Minimum Estimated height $= 1 + 1 + 1 + 1 + 1 = 5 * 8\lambda = 40\lambda$

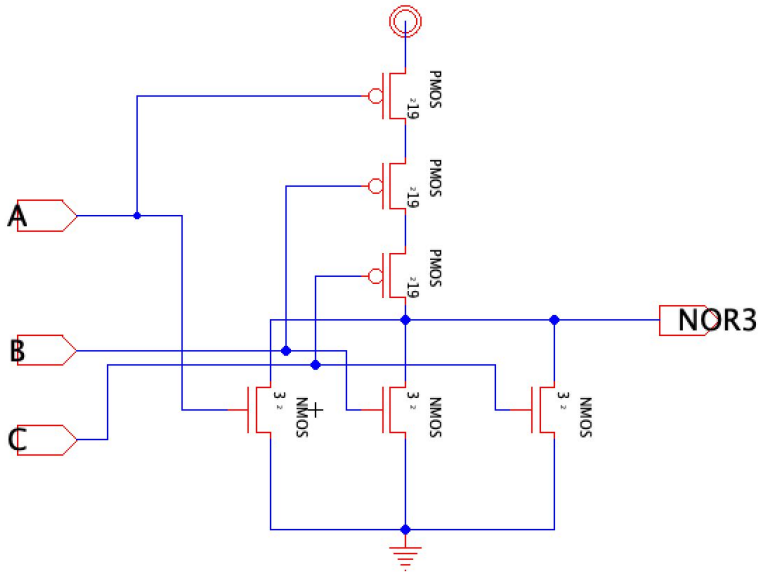
Size (1):
PMOS: 3*3*2.4*1 = 21.6 ~ 22 (width)
NMOS: 3*1*1 = 3

Size(2):
PMOS: 3*3*2.4*2 = 43.2 ~ 44 (width)
NMOS: 3*1*2 = 6

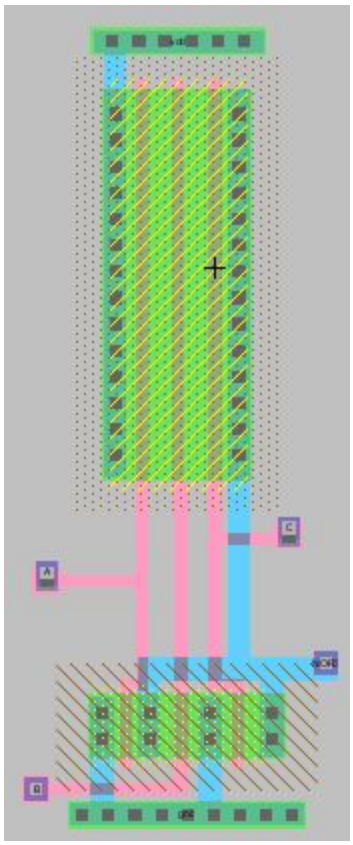
Size(4):
PMOS: 3*3*2.4*4 = 86.4 ~ 87 (width)
NMOS: 3*1*4 = 12

3 input NOR gate:

Schematic Diagram:

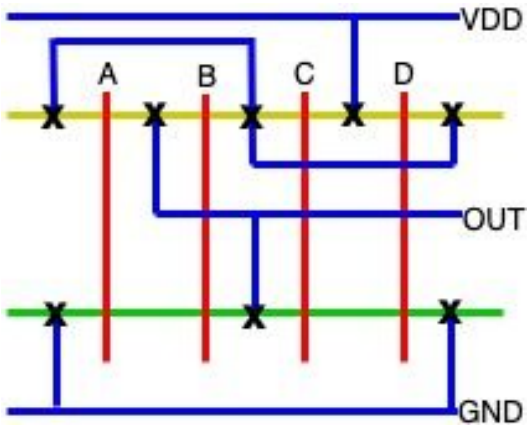


Layout: Width = 60 λ



The complex function: (xy+wz)':

Stick Diagram:



Minimum Estimated height = 1+1+1+1+1+1 = 6*8 λ=48 λ

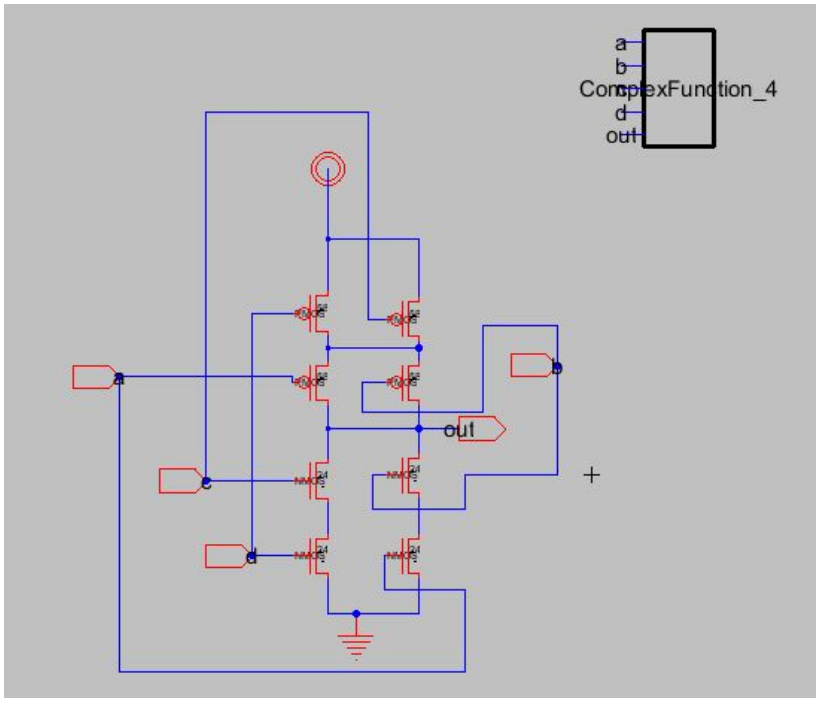
Size (1):
PMOS: 3*2*2.4*1 ~ 16 (width)
NMOS: 3*2*1 = 6

Size(2):
PMOS: 3*2*2.4*2 ~ 29 (width)
NMOS: 3*2*2 = 12

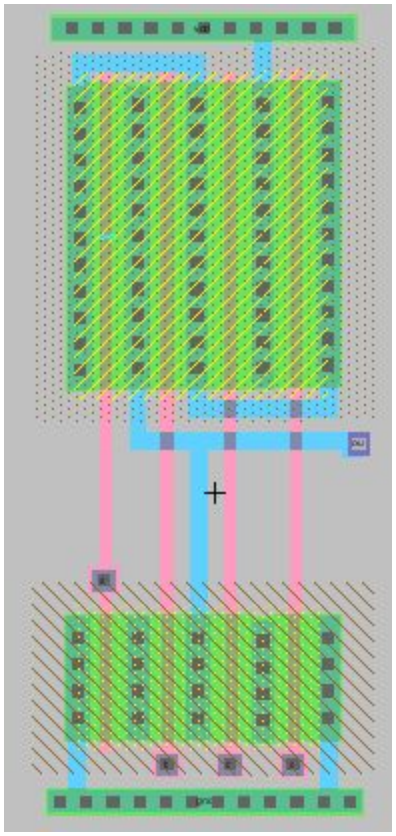
Size(4):
PMOS: 3*2*2.4*4 ~ 58 (width)
NMOS: 3*2*4 = 24

The complex function: (xy+wz)':

Schematic Diagram:



Layout: Width = 72 λ



2. **<u>The Estimated Height For the Cells</u>:** The Height of the Size 8 Tristate Inverter after folding = 164 λ.

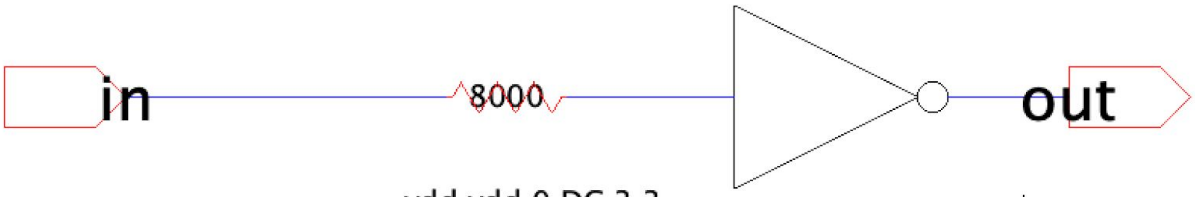
3. **<u>Obtaining The Value of Transition Times:</u>** We used the slope in order to find: **Equations used: ((**(100%)/*transition time*) = 60%/t_time))

At time 0ps: transition = **0ps**
At time 100ps: transition = **166.67ps**
At time 400ps: transition = **666.67ps**
At time 800ps: transition = **1333.33ps**

4. **<u>Obtaining The Value of Cinv:</u>**

Practically:

The following spice code calculate the value of tpd. Then, using the equation tpd=0.69RC, and given that R=8K Ohm, Cinv ~ 12 fF.




```
vdd vdd 0 DC 3.3,
vin in 0 DC pulse 0 3.3 10n 0n 0n 10n 20n,
.tran 0 40n,
.measure tpd param='(tpdr+tpdf)/2'
.measure tpdr
+ TRIG v(in) VAL=1.65 FALL=1
+ TARG v(out) VAL=1.65 RISE=1
.measure tpdf
+ TRIG v(in) VAL=1.65 RISE=1
+ TARG v(out) VAL=1.65 FALL=1
.include scmos18.txt
```

Theoretically:

Using the equation, tinv= KRN CG (1+Kp) , and given that KRN = 293.5223, Kp = 2.4, tinv = 12ps, all in 180nm process, CG = 12.024 fF.

5. **Linear Delay Model Derivations:**

Complex function (Size 1)								
cinv	**0ps**		**100ps**		**400ps**		**800ps**	
	tpdr	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***
1	1.93E-10	1.08E-10	8.74E-11	8.38E-11	1.57E-10	1.02E-10	2.26E-10	1.09E-10
2	2.39E-10	1.58E-10	1.17E-10	1.22E-10	1.97E-10	1.47E-10	2.77E-10	1.66E-10
4	3.15E-10	2.43E-10	1.76E-10	1.96E-10	2.64E-10	2.24E-10	3.62E-10	2.58E-10
8	4.43E-10	3.90E-10	2.92E-10	3.43E-10	3.81E-10	3.67E-10	4.99E-10	4.13E-10

Tpdr: delay = 9.9272E-11 + 2801.6 CL + 0.11922 Transition Time

Tpdf: delay = 5.61E-11 + 3271.8 CL + 0.033932 Transition Time

Complex function (Size 2)								
cinv	**0ps**		**100ps**		**400ps**		**800ps**	
	tpdr	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***
1	1.64E-10	8.24E-11	7.37E-11	6.69E-11	1.32E-10	7.95E-11	1.92E-10	8.25E-11
2	1.93E-10	1.15E-10	8.98E-11	8.81E-11	1.58E-10	1.08E-10	2.25E-10	1.18E-10
4	2.42E-10	1.69E-10	1.21E-10	1.29E-10	2.00E-10	1.56E-10	2.80E-10	1.78E-10
8	3.22E-10	2.59E-10	1.84E-10	2.11E-10	2.72E-10	2.39E-10	3.69E-10	2.76E-10

Tpdr: delay = 9.03E-11 + 1721.5 CL + 0.10242 Transition Time

Tpdrf: delay = 4.97E-11 + 1983.5 CL + 0.025767 Transition Time

Complex function (Size 4)								
cinv	**0ps**		**100ps**		**400ps**		**800ps**	
	tpdr	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***
1	1.42E-10	7.01E-11	6.39E-11	5.71E-11	1.15E-10	6.76E-11	1.67E-10	7.02E-11
2	1.59E-10	8.88E-11	7.33E-11	6.87E-11	1.29E-10	8.39E-11	1.86E-10	9.06E-11
4	1.89E-10	1.22E-10	8.93E-11	9.07E-11	1.55E-10	1.13E-10	2.19E-10	1.27E-10
8	2.39E-10	1.77E-10	1.22E-10	1.34E-10	1.99E-10	1.62E-10	2.75E-10	1.89E-10

Tpdr: delay = 8.40E-11 + 1023.4 CL + 0.085056 Transition Time

Tpdf: delay = 4.78E-11 + 1171.7 CL + 0.019863 Transition Time

NAND (Size 1)								
cinv	**0ps**		**100ps**		**400ps**		**800ps**	
	tpdr	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***
1	2.96E-10	2.12E-11	1.25E-10	7.36E-11	2.31E-10	4.72E-11	3.59E-10	-7.54E-12
2	3.42E-10	7.11E-11	1.64E-10	1.08E-10	2.73E-10	9.09E-11	4.08E-10	4.73E-11
4	4.24E-10	1.54E-10	2.42E-10	1.79E-10	3.50E-10	1.66E-10	4.95E-10	1.38E-10
8	5.75E-10	2.97E-10	4.01E-10	3.16E-10	5.00E-10	3.02E-10	6.51E-10	2.89E-10

Tpdr: delay = 1.5976e-10 + 3304.3 CL + 0.17323 Transition Time

Tpdf: delay = 1.4335e-11 + 3153.1 CL + -0.039767 Transition Time

NAND (Size 2)								
cinv	**0ps**		**100ps**		**400ps**		**800ps**	
	tpdr	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***
1	2.77E-10	-6.92E-12	1.07E-10	5.64E-11	2.13E-10	2.33E-11	3.38E-10	-3.87E-11
2	3.05E-10	2.40E-11	1.31E-10	7.59E-11	2.38E-10	4.98E-11	3.69E-10	-4.72E-12
4	3.54E-10	7.64E-11	1.75E-10	1.13E-10	2.84E-10	9.58E-11	4.21E-10	5.29E-11
8	4.43E-10	1.63E-10	2.61E-10	1.88E-10	3.67E-10	1.75E-10	5.15E-10	1.48E-10

Tpdr: delay = 1.5818e-10 + 1922.1 CL + 0.16984 Transition Time

Tpdf: delay = 6.4403e-12 + 1885.2 CL + -0.051776 Transition Time

NAND (Size 4)								
cinv	**0ps**		**100ps**		**400ps**		**800ps**	
	tpdr	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***
1	2.58E-10	-1.95E-11	9.67E-11	4.75E-11	1.98E-10	1.08E-11	3.16E-10	-5.16E-11
2	2.73E-10	-1.87E-12	1.08E-10	5.79E-11	2.11E-10	2.63E-11	3.34E-10	-3.25E-11
4	3.02E-10	2.94E-11	1.31E-10	7.73E-11	2.37E-10	5.38E-11	3.64E-10	2.08E-12
8	3.53E-10	8.28E-11	1.75E-10	1.16E-10	2.84E-10	1.01E-10	4.19E-10	6.10E-11

Tpdr: delay = 1.5301e-10 + 1073.1 CL + 0.16133 Transition Time

Tpdf: delay = 4.7511e-12 + 1102.9 CL + -0.059561 Transition Time

NOR (Size 1)								
cinv	**0ps**		**100ps**		**400ps**		**800ps**	
	tpdr	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***
1	4.54e-011	1.96E-10	6.31E-11	8.99E-11	5.78E-11	1.57E-10	3.21E-11	2.32E-10
2	4.54E-11	1.96E-10	6.31E-11	8.99E-11	5.78E-11	1.57E-10	3.21E-11	2.32E-10
4	4.54E-11	1.96E-10	6.31E-11	8.99E-11	5.78E-11	1.57E-10	3.21E-11	2.32E-10
8	4.54E-11	1.96E-10	6.31E-11	8.99E-11	5.78E-11	1.57E-10	3.21E-11	2.32E-10

Tpdr: delay = 5.7467e-11 + -0.073134 CL + -0.024188 Transition Time

Tpdf: delay = 1.3681e-10 + 0 CL + 0.098187 Transition Time

NOR (Size 2)								
cinv	**0ps**		**100ps**		**400ps**		**800ps**	
	tpdr	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***
1	1.12E-11	2.36E-10	4.83E-11	9.85E-11	3.05E-11	1.84E-10	-1.11E-11	2.87E-10
2	1.12E-11	2.36E-10	4.83E-11	9.85E-11	3.05E-11	1.84E-10	-1.11E-11	2.87E-10
4	1.12E-11	2.36E-10	4.83E-11	9.85E-11	3.05E-11	1.84E-10	-1.11E-11	2.87E-10
8	1.12E-11	2.36E-10	4.83E-11	9.85E-11	3.05E-11	1.84E-10	-1.11E-11	2.87E-10

Tpdr: delay = 3.4396e-11 + 0 CL + -0.045142 Transition Time

Tpdf: delay = 1.5838e-10 + -1.3441e-12 CL + 0.13229 Transition Time

NOR (Size 4)								
cinv	**0ps**		**100ps**		**400ps**		**800ps**	
	tpdr	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***
1	2.12E-11	2.33E-10	5.97E-11	1.06E-10	4.09E-11	1.86E-10	1.20E-12	2.80E-10
2	2.12E-11	2.33E-10	5.97E-11	1.06E-10	4.09E-11	1.86E-10	1.20E-12	2.80E-10
4	2.12E-11	2.33E-10	5.97E-11	1.06E-10	4.09E-11	1.86E-10	1.20E-12	2.80E-10
8	2.12E-11	2.33E-10	5.97E-11	1.06E-10	4.09E-11	1.86E-10	1.20E-12	2.80E-10

Tpdr: delay = 4.4744e-11 + 0 CL + -0.043058 Transition Time

Tpdf: delay = 1.6152e-10 + 2.2642e-12 CL + 0.12226 Transition Time

inverter (Size 1)								
cinv	**0ps**		**100ps**		**400ps**		**800ps**	
	tpdr	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***
1	1.86E-10	1.23E-10	8.29E-11	7.65E-11	1.50E-10	1.11E-10	2.15E-10	1.32E-10
2	2.52E-10	1.94E-10	1.22E-10	1.88E-10	2.08E-10	1.72E-10	2.90E-10	2.10E-10
4	3.54E-10	3.05E-10	2.01E-10	2.00E-10	2.98E-10	2.70E-10	4.04E-10	3.33E-10
8	5.19E-10	4.83E-10	3.58E-10	3.65E-10	4.52E-10	4.32E-10	5.83E-10	5.27E-10

Tpdr: delay = 8.2915e-11 + 3747.1 CL + 0.12506 Transition Time

Tpdf: delay = 6.0642e-11 + 3915.1 CL + 0.063911 Transition Time

inverter(Size 2)								
cinv	**0ps**		**100ps**		**400ps**		**800ps**	
	tpdr	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***
1	1.51E-10	8.72E-11	6.56E-11	5.85E-11	1.22E-10	8.05E-11	1.76E-10	9.22E-11
2	1.99E-10	1.38E-10	1.22E-10	8.05E-11	1.63E-10	1.24E-10	2.30E-10	1.47E-10
4	2.72E-10	2.17E-10	1.38E-10	1.36E-10	2.26E-10	1.93E-10	3.13E-10	2.35E-10
8	3.86E-10	3.42E-10	2.29E-10	2.36E-10	3.26E-10	3.04E-10	4.39E-10	3.72E-10

Tpdr: delay = 7.6614e-11 + 2491 CL + 0.10351 Transition Time

Tpdf: delay = 3.6249e-11 + 2748.2 CL + 0.054656 Transition Time

Inverter(Size 4)								
cinv	**0ps**		**100ps**		**400ps**		**800ps**	
	tpdr	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***
1	1.12E-10	7.04E-11	4.95E-11	4.62E-11	1.39E-10	1.47E-10	1.30E-10	7.43E-11
2	1.43E-10	1.03E-10	6.51E-11	6.17E-11	1.18E-10	9.11E-11	1.65E-10	1.11E-10
4	1.93E-10	1.55E-10	9.02E-11	9.25E-11	1.60E-10	1.36E-10	2.21E-10	1.69E-10
8	2.68E-10	2.37E-10	1.39E-10	1.47E-10	2.24E-10	2.08E-10	3.07E-10	2.60E-10

Tpdr: delay = 6.1921e-11 + 1528.4 CL + 0.08319 Transition Time

Tpdf: delay = 4.506e-11 + 1585.5 CL + 0.047439 Transition Time

Inverter(Size 8)								
cinv	**0ps**		**100ps**		**400ps**		**800ps**	
	tpdr	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***
1	8.02E-11	6.37E-11	3.90E-11	3.58E-11	6.82E-11	5.43E-11	9.22E-11	6.98E-11
2	1.00E-10	8.30E-11	6.82E-11	5.42E-11	8.36E-11	7.23E-11	1.14E-10	9.22E-11
4	1.32E-10	1.16E-10	8.37E-11	7.22E-11	1.10E-10	1.00E-10	1.50E-10	1.28E-10
8	1.82E-10	1.68E-10	8.82E-11	9.62E-11	1.52E-10	1.45E-10	2.06E-10	1.86E-10

Tpdr: delay = 4.8684e-11 + 999.8 CL + 0.048173 Transition Time

Tpdf: delay = 3.5721e-11 + 1080.3 CL + 0.036034 Transition Time

Tristate Inverter (Size 1)								
cinv	**0ps**		**100ps**		**400ps**		**800ps**	
	tpdr	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***
1	1.73E-10	1.13E-10	9.92E-11	8.95E-11	1.46E-10	1.07E-10	1.97E-10	1.17E-10
2	2.24E-10	1.63E-10	1.42E-10	1.27E-10	1.91E-10	1.51E-10	2.52E-10	1.72E-10
4	3.09E-10	2.47E-10	2.24E-10	2.02E-10	2.72E-10	2.28E-10	3.44E-10	2.62E-10
8	4.66E-10	3.93E-10	3.89E-10	3.50E-10	4.29E-10	3.71E-10	5.04E-10	4.14E-10

Tpdr: delay = 9.1413e-11 + 3462.8 CL + 0.077955 Transition Time

Tpdf: delay = 6.2056e-11 + 3248.6 CL + 0.033573 Transition Time

Tristate inverter (Size 2)								
cinv	**0ps**		**100ps**		**400ps**		**800ps**	
	tpdr	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***
1	1.39E-10	9.52E-11	7.89E-11	7.35E-11	1.84E-10	8.88E-11	1.18E-10	8.87E-11
2	1.70E-10	1.25E-10	1.10E-10	9.50E-11	1.45E-10	1.17E-10	1.91E-10	1.33E-10
4	2.22E-10	1.78E-10	1.45E-10	1.37E-10	1.92E-10	1.63E-10	2.76E-10	2.45E-10
8	3.12E-10	2.66E-10	2.31E-10	2.18E-10	2.76E-10	2.45E-10	3.46E-10	2.84E-10

Tpdr: delay = 6.0731e-11 + 1135.2 CL + 0.069413 Transition Time

Tpdf: delay = 5.7515e-11 + 1147.4 CL + 0.031827 Transition Time

Tristate Inverter (Size 4)								
cinv	**0ps**		**100ps**		**400ps**		**800ps**	
	tpdr	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***
1	1.15E-10	8.76E-11	6.71E-11	6.53E-11	9.78E-11	7.99E-11	1.29E-10	9.45E-11
2	1.15E-10	8.76E-11	7.81E-11	7.70E-11	1.13E-10	9.57E-11	1.48E-10	1.12E-10
4	1.63E-10	1.36E-10	1.00E-11	9.93E-11	1.41E-10	1.24E-10	1.82E-10	1.45E-10
8	2.16E-10	1.90E-10	1.45E-10	1.43E-10	1.89E-10	1.72E-10	2.41E-10	2.03E-10

Tpdf: delay = 6.0731e-11 + 1135.2 CL + 0.069413 Transition Time

Tpdr: delay = 5.7515e-11 + 1147.4 CL + 0.031827 Transition Time

Tristate Inverter (Size 8)								
cinv	**0ps**		**100ps**		**400ps**		**800ps**	
	tpdr	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***	***tpdr***	***tpdf***
1	3.33E-10	-5.41E-11	1.81E-10	4.18E-11	2.61E-10	-8.27E-12	8.50E-10	-5.42E-10
2	3.54E-10	-3.89E-11	2.04E-10	4.96E-11	2.81E-10	4.46E-12	2.26E-10	-8.66E-11
4	3.53E-10	-3.89E-11	2.45E-10	6.37E-11	3.21E-10	2.73E-11	4.65E-10	-5.55E-10
8	4.69E-10	3.43E-11	3.32E-10	8.93E-11	4.01E-10	6.59E-11	5.42E-10	-3.62E-12

Tpdr: delay = 2.3802e-10 + 1033 CL + 0.24345 Transition Time

Tpdf: delay = -1.3908e-11 + 1693 CL + -0.37451 Transition Time

6. **Spice Codes:**

For (1cinv):

(For 2,4,8 we multiply the value of cinv in the cloud by each constant)

(0ps)

```
vdd vdd 0 DC 3.3,
vin in 0 DC pulse 0 3.3 10n 0ps 0ps 10n,
cload out 0 12fF,
.tran 0 40n,
.measure tpdr
+ TRIG v(in) VAL=1.65 FALL=1
+ TARG v(out) VAL=1.65 RISE=1
.measure tpdf
+ TRIG v(in) VAL=1.65 RISE=1
+ TARG v(out) VAL=1.65 FALL=1
.include scmos18.txt
```

(100ps)

```
vdd vdd 0 DC 3.3,
vin in 0 DC pulse 0 3.3 10n 166.67ps 166.67ps 10n,
cload out 0 12fF,
.tran 0 40n,
.measure tpdr
+ TRIG v(in) VAL=1.65 FALL=1
+ TARG v(out) VAL=1.65 RISE=1
.measure tpdf
+ TRIG v(in) VAL=1.65 RISE=1
+ TARG v(out) VAL=1.65 FALL=1
.include scmos18.txt
```

(400ps)

```
vdd vdd 0 DC 3.3,
vin in 0 DC pulse 0 3.3 10n 666.67ps 666.67ps 10n,
cload out 0 12fF,
.tran 0 40n,
.measure tpdr
+ TRIG v(in) VAL=1.65 FALL=1
+ TARG v(out) VAL=1.65 RISE=1
.measure tpdf
+ TRIG v(in) VAL=1.65 RISE=1
+ TARG v(out) VAL=1.65 FALL=1
.include scmos18.txt
```

(800ps)

```
vdd vdd 0 DC 3.3,
vin in 0 DC pulse 0 3.3 10n 1333.33ps 1333.33ps 10n,
cload out 0 12fF,
.tran 0 40n,
.measure tpdr
+ TRIG v(in) VAL=1.65 FALL=1
+ TARG v(out) VAL=1.65 RISE=1
.measure tpdf
+ TRIG v(in) VAL=1.65 RISE=1
+ TARG v(out) VAL=1.65 FALL=1
.include scmos18.txt
```

Students Contributions

Mohamed Elatroush:

- 3-input NOR Gate (size 1, 2, 4) with simulation
- Folding of the largest transistor (Tri-state size 8) to minimize the height
- Estimation for all cells height
- Deriving the total rising and falling times from the transition times
- Obtaining tpdr and tpdf for some cells using the spice codes provided above

Hadeel Mabrouk:

- Stick Diagrams
- 3-input NAND Gate (size 1, 2, 4) with simulation
- Complex Function (size 1, 2, 4) with simulation
- Obtaining tpdr and tpdf for some cells using the spice codes provided above
- Derivation of the linear delay models

Omar Abougabal:

- Inverter cell (size 1 , 2, 4, 8) with simulation
- Tri-state buffer (size 1 ,2, 4, 8) with simulation
- Modification of Tri-state buffer stick diagram
- Deriving the value of the Cinv using spice simulation
- Obtaining tpdr and tpdf for some cells using the spice codes provided above