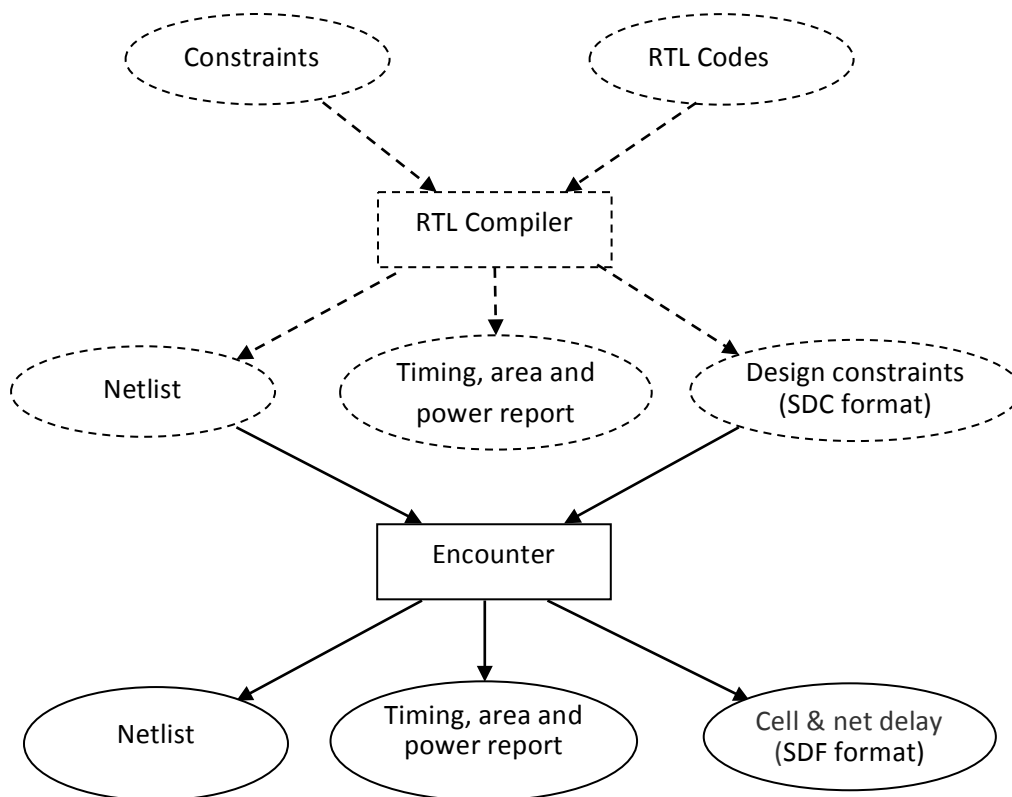


Lab 6: Placement and Routing

In this lab, you will run placement and routing for the synthesized netlist of Lab 4 using Cadence Encounter. The objective of this lab is to give you a hands-on experience with:

1. Placement and Routing.
2. Circuit timing, area, power analysis after placement and routing.

We will go through the following design flow in this lab:



Please refer to the posted document `encounter-instructions.docx` regarding how to use Cadence Encounter to do placement and routing.

Lab Tasks:

1. Go through the placement and routing flow.
2. Based on timing, area, and power report, fine tune the parameters in placement and routing flow to optimize the design. The goals are:

- Small clock period while no timing violation for both setup time and hold time. For running both of setup and hold time violation checking at same time, you may need to also select Hold at “Optimize”→”Optimize Design” step. If your design still has violations, you may need to modify the .sdc file, e.g., changing the clock period. You will find out that the clock period needs to be loosed due to the introduction of wire delay in placement and routing for setup time violation checking. Besides, you may have hold time violation, which is not checked during synthesis in Lab 5.
- Small area. You may need to tune the parameters in the floorplan step. But remember, if you restrict the area too much, the design may become unroutable and timing may be hurt.
- Less power consumption. We cannot control power consumption too much in an automatic layout flow. We will just let the software handle it in this lab. You will learn other power saving techniques in later labs.

Please report the best clock period, area and power consumption that you can achieve.