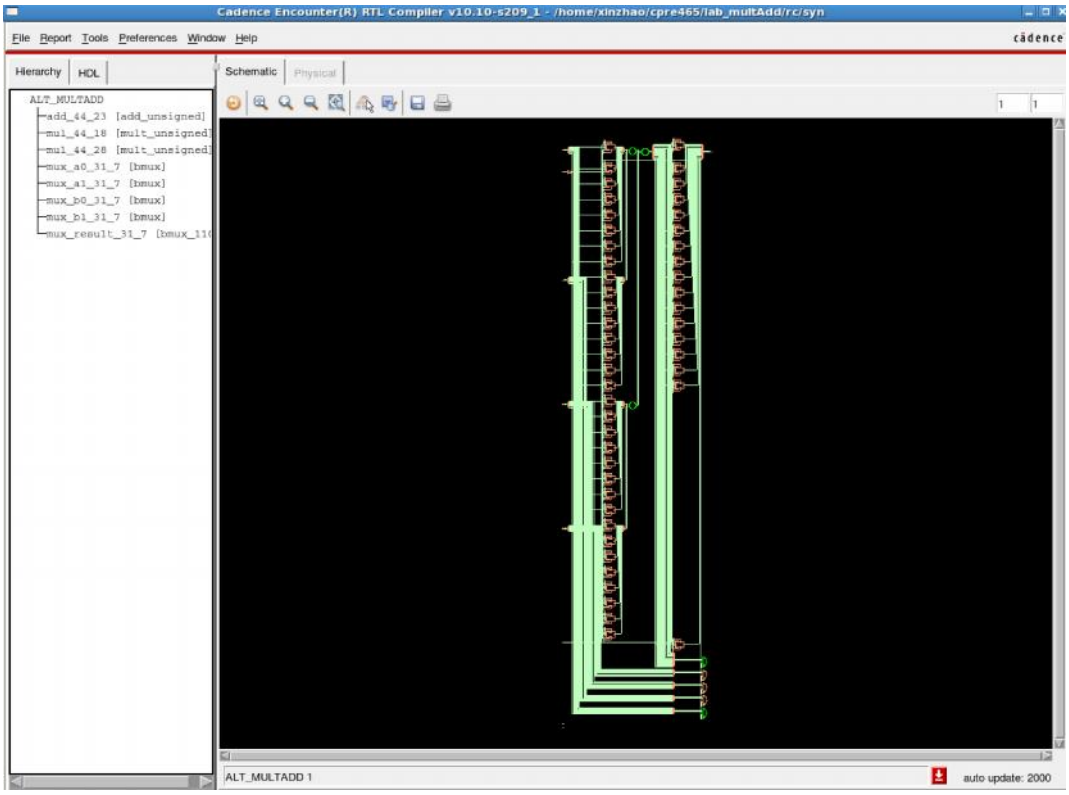
Tutorial for Cadence RTL Compiler

1. Setting up: Please download the file rc.rar and decompress it to a newly created project directory. Go to the folder named "rc". It should have 3 folders, named libdir, rtl and syn.
   - libdir: contains the library files the tool will use.
   - rtl: contains the Verilog codes needed to be synthesized. Please copy your Verilog file which already made in Lab 1 to this folder and renamed it as "ALT_MULTADD.v". Please do not include your test bench file because that is for simulation only.
   - syn: contains run_dir (which holds the results of running synthesis) and scripts (which holds the scripts for running synthesis). More importantly, in the scripts folder, there are 3 files. They are:
     1) design.sdc: contains the constraints you want to add to the design. They are already set. Please note in the Verilog file you made in Lab 1, if you changed the port names that are defined in the Lab 1 instruction, you need to modify this file to adapt to your port names.
     2) read_rtl.tcl: is a script used to read in your Verilog file. Please note if you have more than one Verilog files to be read in, you need to add lines in this file to read all your Verilog files.
     3) run_synth.tcl: is the top level script to drive the synthesis tool. This file will use the other 2 files.

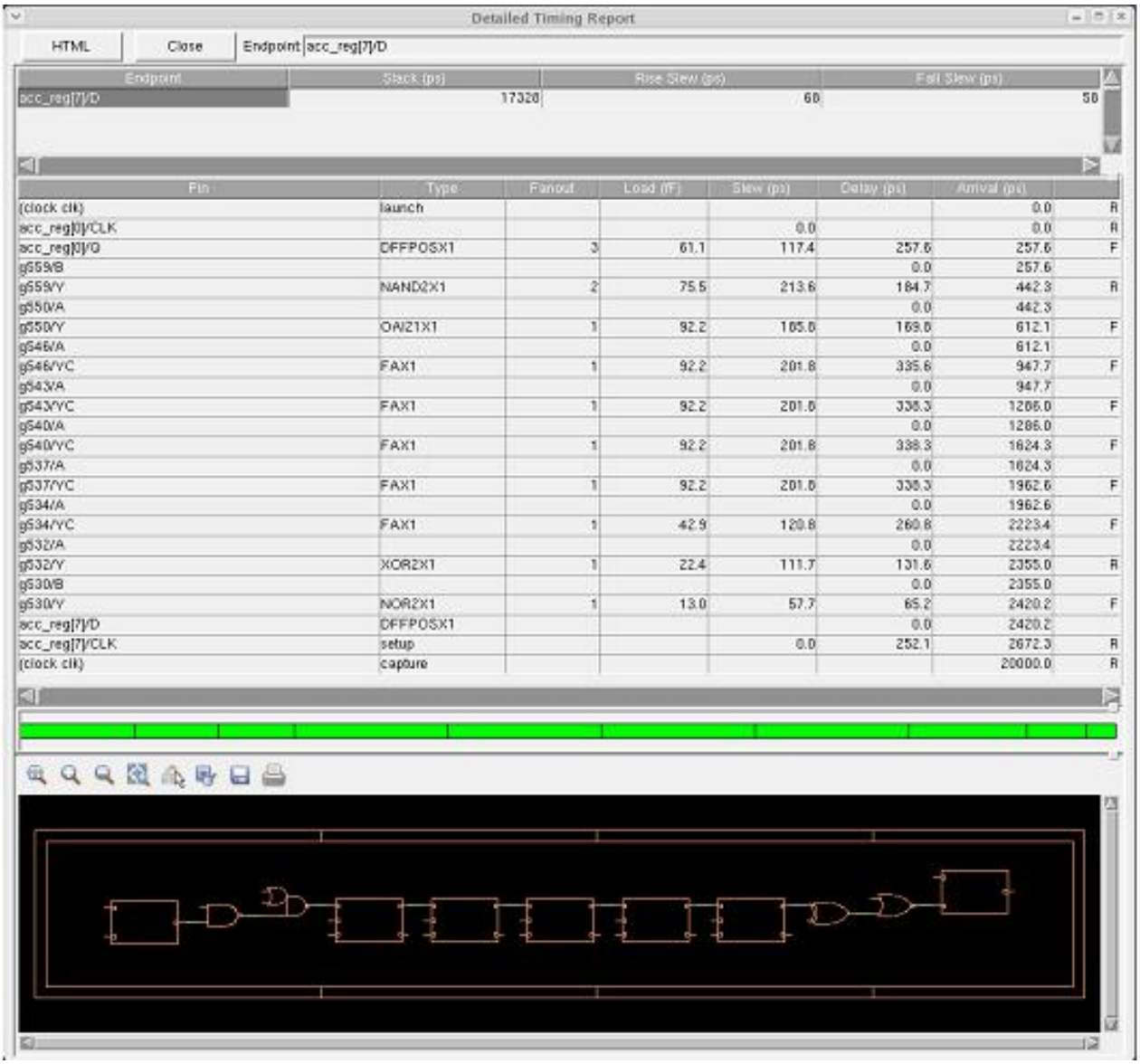
2. Starting RTL Compiler: Open a new terminal. In the newly created project directory, type "source /etc/software/edi" and hit Enter. Go to the syn directory. Then type “rc –gui” to invoke RTL Compiler, our synthesis tool from Cadence.

3. Performing synthesis: You can perform synthesis by running the script that is already made for you. Go to File -> Source Script from the File menu of the Menu Bar. Select the run_synth.tcl in the "scripts" folder. Click OK. The tool will do the synthesis job for you. Just wait for the result. A gate level schematic will be shown in the gui window as below:



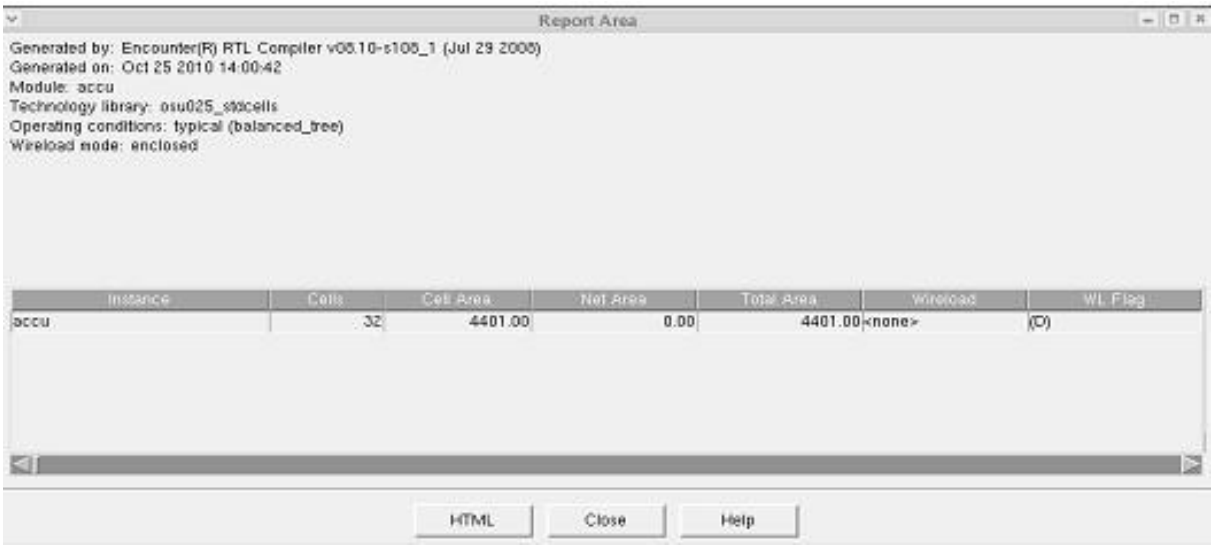
Please find the log file in the "syn" folder, and search for the keyword "error" to make sure there is no error happened during the synthesis.

4. Timing report: You can check the timing report by going to Report -> Timing -> Worst Path. (You may also generate a plain text version of the timing report by type "report timing" in the command window.)



Note that for the report in the diagram above, the “Slack time” is 17328ps. Since it is positive, the tool is telling you that the signal arrives at the FF on the right much earlier than necessary. This means that the circuit can work with a much higher clock frequency. If you want your design to run at a higher frequency, you need to change the design.sdc file. There is a constraint to set up the clock period. Change it to what you want. And re-run the whole flow again.

5. Area report: For the area report, go to Report -> Netlist -> Area. (You may also generate a plain text version of area report by type "report area" in the command window.) Check the total area. If we ask the synthesis tool to produce a faster circuit, this value is likely to increase.



6. Power report: To report the power, go to Report -> Power -> detailed report. (You may also generate a plain text version of power report by type "report power" in the command window.)

   The power, timing and area reports are also generated by scripts and are stored in the run_dir folder. Please check it.