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EE 465 Lab 2
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Standard Cell Design: D-Flip-Flop

Introduction

This lab consisted of building a D-Flip-Flop (DFF) using inverters, transmission gates, and tri-state buffers. Those components were created at the transistor level and saved into instances for easier use. A test bench was created to simulate the output of the DFF. Once the functionality of the DFF was verified, a layout was created and checked against the schematic (LVS).

Building the DFF

The DFF consisted of three main components all made from CMOS transistors. Those components are the inverter, transmission gate, and tri-state buffer as shown in Figure 1. Symbols of those components were made in Cadence to allow them to be used as basic building blocks for the DFF as seen in Figure 2.

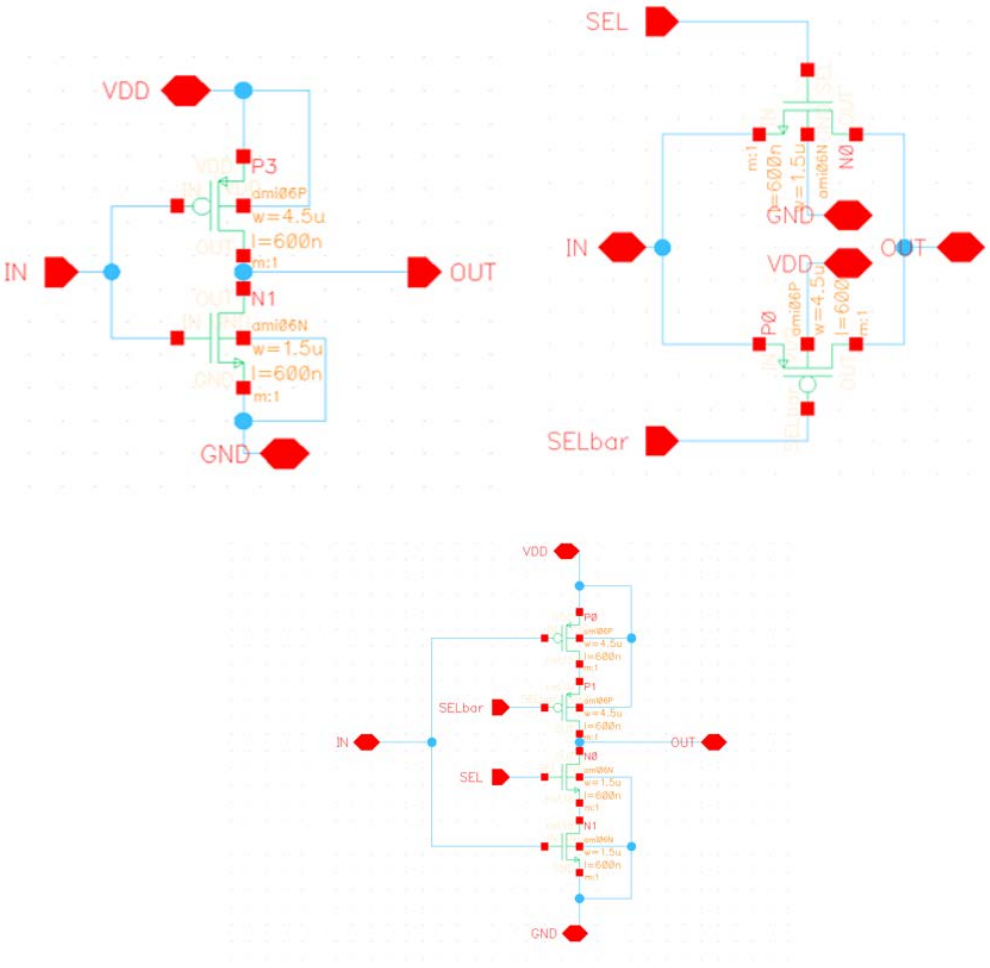

Figure 1: Inverter (top left), Transmission Gate (top right), and Tri-State Buffer (bottom) schematics

After the symbols were made, the DFF was built. The DFF takes inputs D, VDD, VSS, CLK, and CLK_Bar, and has output Q and Qbar. Qbar was not used in this lab. The basic operation consists of the output changing to the value of the D after one clock cycle on the leading edge of CLK going high, and staying the same value otherwise.

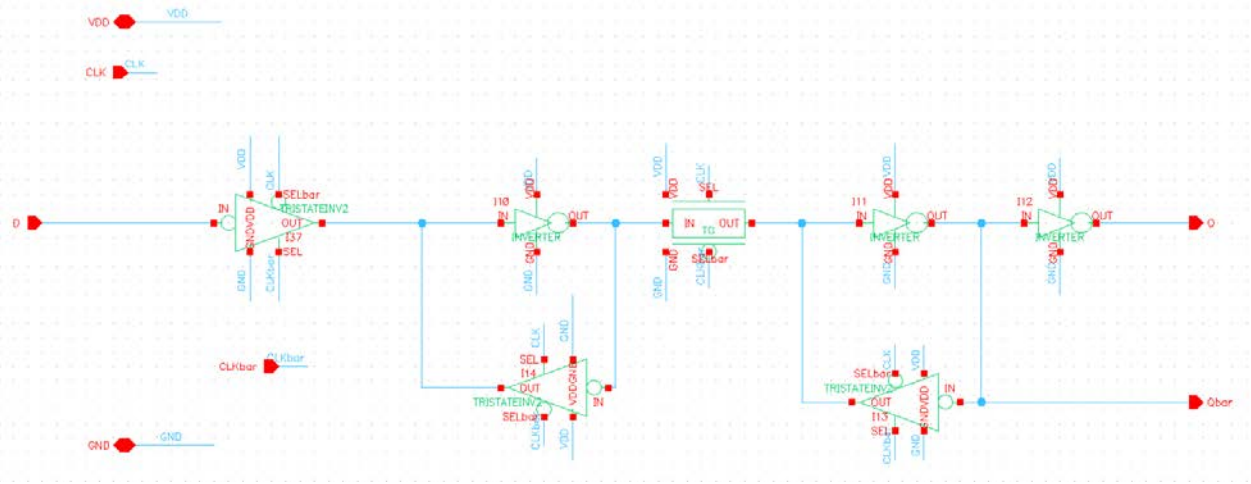

Figure 2: D-Flip-Flop schematic

A test bench was created to test the DFF for functionality and is shown in Figure 3. Two Vpulse signals were used to generate a changing input at D and to vary the CLK input. VDD was set to 5 VDC and small capacitors were placed between Q and ground to allow for simulation.

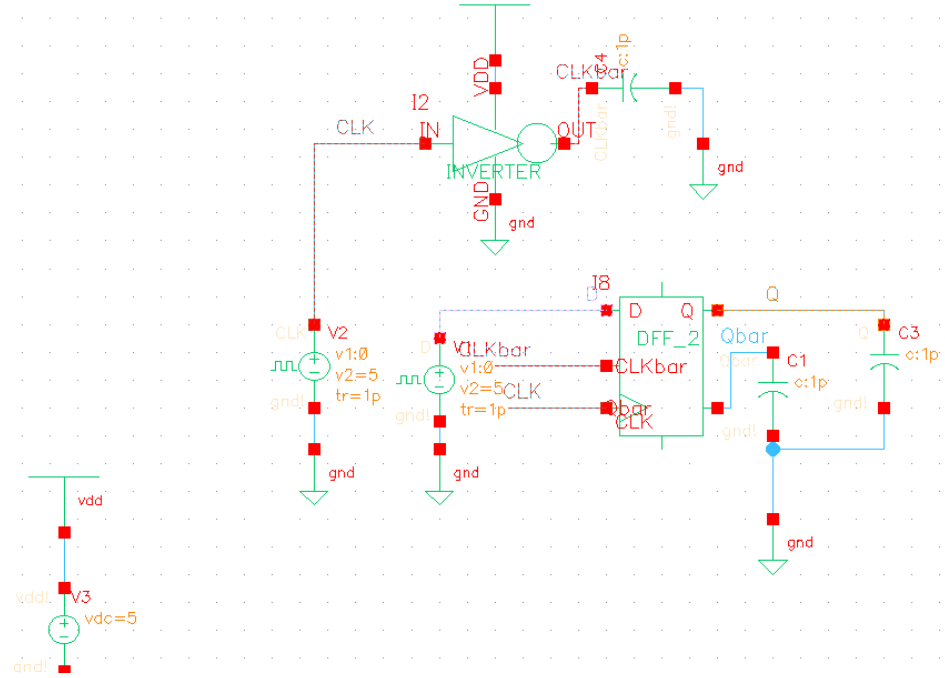

Figure 3: D-Flip-Flop Test bench schematic

The simulation output shown in Figure 4 below shows that the DFF is functioning correctly. When the input D changes on the positive edge of a clock cycle, the output Q changes to the value of D after one clock cycle.

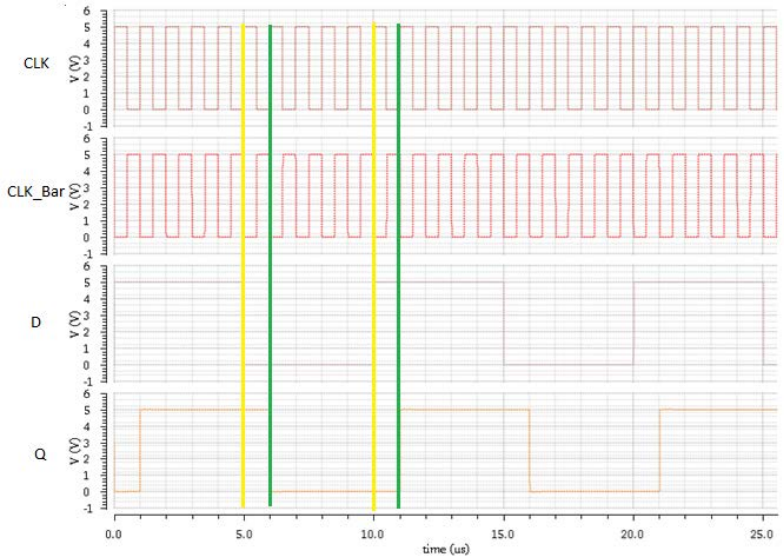

Figure 4: D-Flip-Flop output

The layout of the DFF is shown below in Figure 5. The blue mostly horizontal lines are metal 1, the pink mostly vertical lines are metal 2, the orange/red is the poly, the green shaded areas make up the PMOS transistors, and the green boxes filled with white space make up the NMOS transistors. All of the little squares are pins and vias.

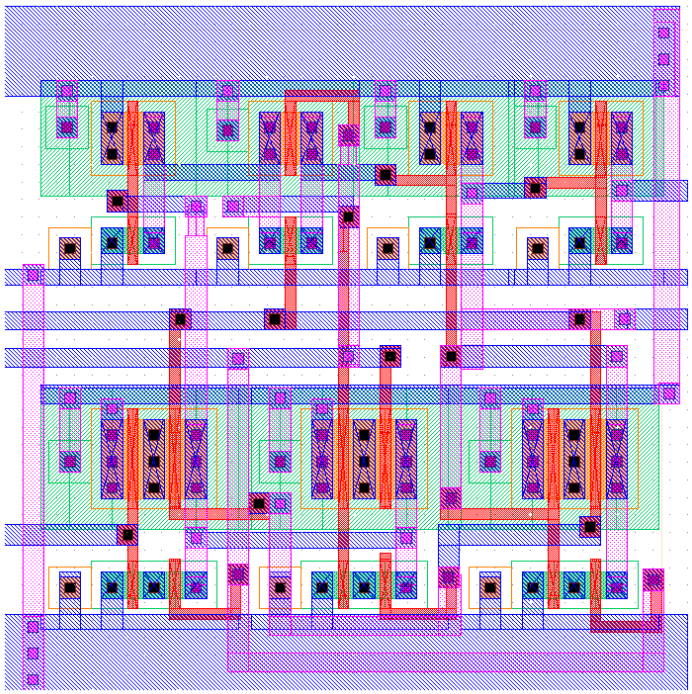

Figure 5: D-Flip-Flop layout

Once the layout was complete, an LVS (Layout Vs Schematic) check was completed to verify that the object built in the layout was functionally the same as the schematic. The LVS passed after correcting a few errors such as the metal being too close in some areas.

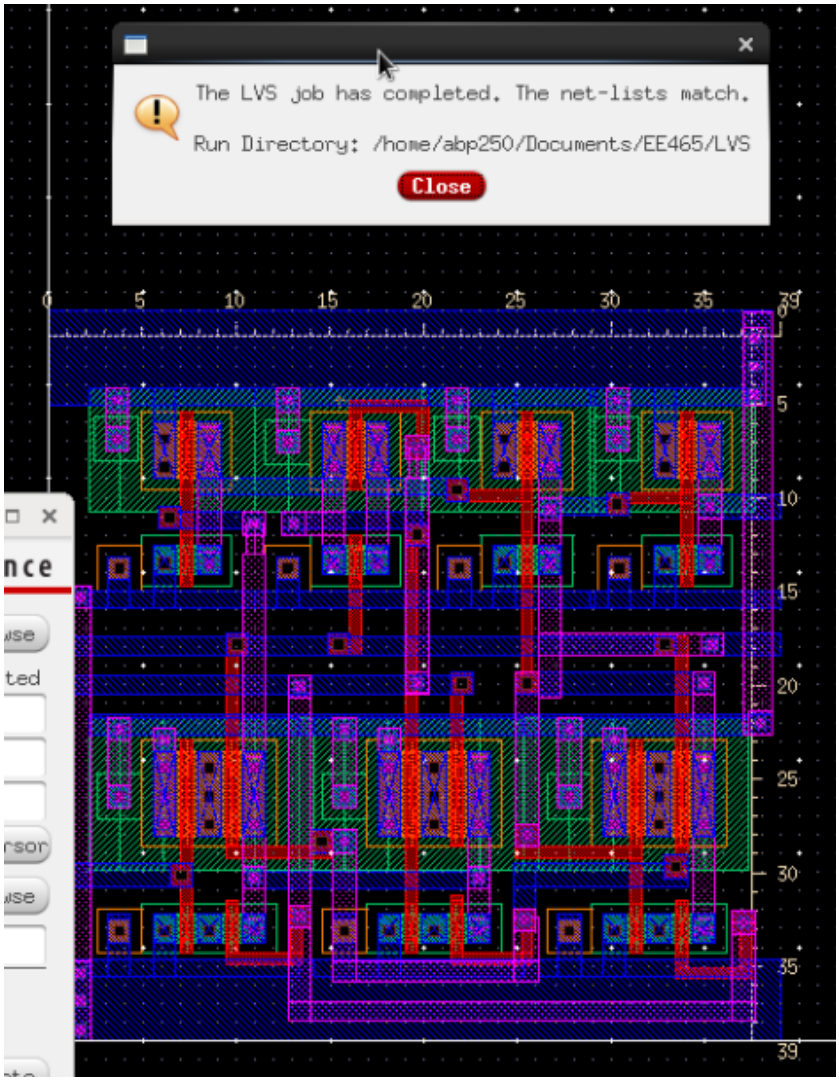

Figure 6: D-Flip-Flop LVS match

Conclusion

The DFF worked as it was supposed to. There were small errors that created bad results such as an incorrectly sized transistor or switching Phi and Phi_Bar. The layout did not have size restraints, but we chose to make it as small as we could.