EE/CprE 465 -- Fall 2015

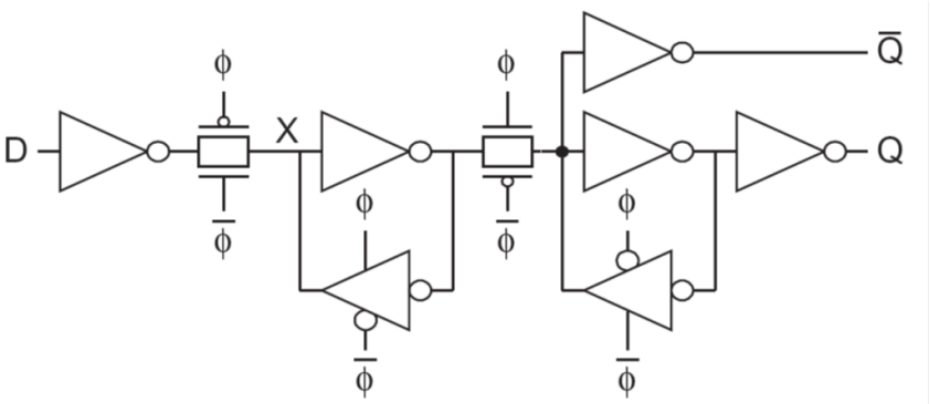
Lab 2: Standard Cell Design

Standard cells are the basic cells which are commonly used in digital design. Usually they consists of basic logic gates, buffers, DFFs, multiplexers, and even half and full adders, etc. If the whole circuit is a building, standard cells are the bricks. And the performance of the standard cells determines the performance of the circuit to a large extent.

In this lab, we will build a standard cell, DFF, with Cadence Virtuoso. The objective of this lab is to get a hands-on experience with several skills that we have learned in EE330:

1. Building schematic
2. Drawing layout
3. LVS and DRC

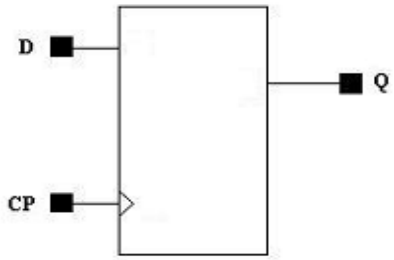
The design of the DFF comes from Figure 10.19(b) in p.393 of your textbook. For your convenience, it is also given below. However, we will not implement $\overline{Q}$ in this lab.



In addition, we are posting the TCBN65GPLUS TSMC 65nm Core Library Databook (DBTCBN65GPLUSBC_121B.pdf). The DFF in this lab is functionally the same as the cell named DFQDx in the TSMC library. The interface and the truth table of the cell DFQDx (i.e., of our DFF) are given below.

DFQDx

D Flip−Flop, Single Output



Truth Table

INPUT		OUTPUT
CP	D	Q
↑	0	0
↑	1	1
0	x	Q
1	x	Q

In addition to the interface and the truth table, the Databook contains many other information characterizing the cell. We will learn about standard cell characterization in Lab 3.

For setting up Virtuoso, please follow: http://wikis.ece.iastate.edu/vlsi/index.php/Cadence_6.1_Setup

For using Virtuoso, please refer to EE330 Lab 2 (building schematic and simulation) and Lab 3 (layout LVS and DRC): http://class.ece.iastate.edu/ee330/

Lab Tasks:

1. Build the schematic in the Virtuoso. Then perform enough simulations to verify the function of the DFF.

2. Draw the layout of the DFF. Designing a high-quality standard cell library is very complicated. For example, each cell needs to be at a given height, VDD and GND wires need to be laid out at specific locations, and the layout area, delay, power, etc. should be minimized. In this lab, we will ignore all those issues. The only requirement is to have a functionally-correct cell.

3. Perform LVS and DRC.