Lab 7 Report

In this lab, we need to find another way to increase clock speed. To do this, we will be “pipelining” the design by adding registers in-between gates of the circuit to split the data path into various segments. Each segment will take less time than the overall circuit so the overall throughput will be higher.

# 1 Observation & correction:

## Before fix:

module ALT\_MULTADD(iCLK, iRST\_N, iSEL, iA0, iA1, iB0, iB1, oR);

input iCLK, iRST\_N, iSEL, iA0, iA1, iB0, iB1;

output oR;

wire iCLK, iRST\_N, iSEL;

wire [7:0] iA0, iA1, iB0, iB1;

reg [7:0] A0, A1, B0, B1;

reg [16:0] oR;

always @ (posedge iCLK, negedge iRST\_N)begin

A0 <= iA0;

A1 <= iA1;

B0 <= iB0;

B1 <= iB1;

if(iRST\_N)begin

if(iSEL) begin

oR <= A0 \* B0 + A1 \* B1;

end

else begin

oR <= A0 \* B0 + A1 \* B1 + A0 \* A1 \* B0 \* B1;

end

end

else begin

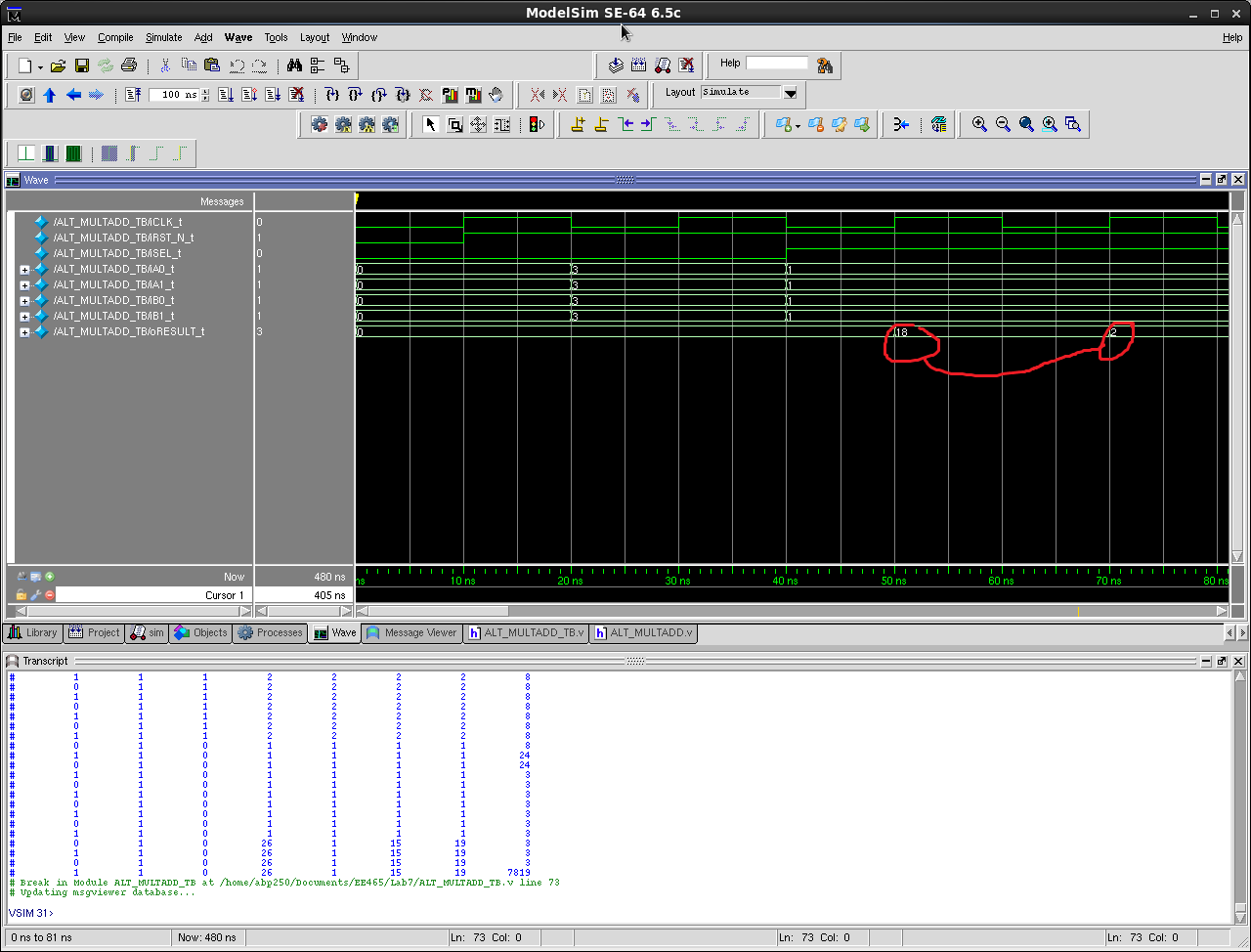
oR <= 0;

end

end

endmodule

### Simulation:



# Test control

# iCLK\_t iRST\_N\_t iSEL\_t iA0\_t iA1\_t iB0\_t iB1\_t oRESULT\_t

# 0 0 0 0 0 0 0 0

# 1 1 0 0 0 0 0 0

# 0 1 0 3 3 3 3 0

# 1 1 0 3 3 3 3 0

# 0 1 1 1 1 1 1 0

# 1 1 1 1 1 1 1 18

# 0 1 1 1 1 1 1 18

# 1 1 1 1 1 1 1 2

# 0 1 1 1 1 1 1 2

# 1 1 1 1 1 1 1 2

# 0 1 1 1 1 1 1 2

# 1 1 1 1 1 1 1 2

# 0 1 1 1 1 1 1 2

# 1 1 1 1 1 1 1 2

# 0 1 0 2 2 2 2 2

# 1 1 0 2 2 2 2 3

# 0 1 0 2 2 2 2 3

This is not correct, we need the first output from oRESULT to correspond to the input from the previous clock cycle.

## After fix:

module ALT\_MULTADD(iCLK, iRST\_N, iSEL, iA0, iA1, iB0, iB1, oR);

input iCLK, iRST\_N, iSEL, iA0, iA1, iB0, iB1;

output oR;

wire iCLK, iRST\_N, iSEL;

wire [7:0] iA0, iA1, iB0, iB1;

reg SEL;

reg [7:0] A0, A1, B0, B1;

reg [16:0] oR;

always @ (posedge iCLK, negedge iRST\_N)begin

A0 <= iA0;

A1 <= iA1;

B0 <= iB0;

B1 <= iB1;

SEL <= iSEL;

if(iRST\_N)begin

if(SEL) begin

oR <= A0 \* B0 + A1 \* B1;

end

else begin

oR <= A0 \* B0 + A1 \* B1 + A0 \* A1 \* B0 \* B1;

end

end

else begin

oR <= 0;

end

end

endmodule

Simulation:

`timescale 10ns/1ns

module ALT\_MULTADD\_TB ();

reg iCLK\_t, iRST\_N\_t, iSEL\_t;

reg [7:0] iA0\_t, iA1\_t, iB0\_t, iB1\_t;

wire [16:0] oRESULT\_t;

ALT\_MULTADD X(iCLK\_t, iRST\_N\_t, iSEL\_t, iA0\_t, iA1\_t, iB0\_t, iB1\_t, oRESULT\_t);

initial $display ("Test control");

initial $display ("%10s %10s %10s %10s %10s %10s %10s %10s",

"iCLK\_t", "iRST\_N\_t", "iSEL\_t", "iA0\_t", "iA1\_t",

"iB0\_t", "iB1\_t", "oRESULT\_t");

initial $monitor ("%10b %10b %10b %10d %10d %10d %10d %10d",

iCLK\_t, iRST\_N\_t, iSEL\_t, iA0\_t, iA1\_t, iB0\_t, iB1\_t, oRESULT\_t);

initial begin

iCLK\_t = 0;

iRST\_N\_t = 0;

iSEL\_t = 0;

iA0\_t = 0;

iA1\_t = 0;

iB0\_t = 0;

iB1\_t = 0;

#1

iRST\_N\_t = 1;

#1

iA0\_t = 3;

iA1\_t = 3;

iB0\_t = 3;

iB1\_t = 3;

#2

iSEL\_t = 1;

iA0\_t = 1;

iA1\_t = 1;

iB0\_t = 1;

iB1\_t = 1;

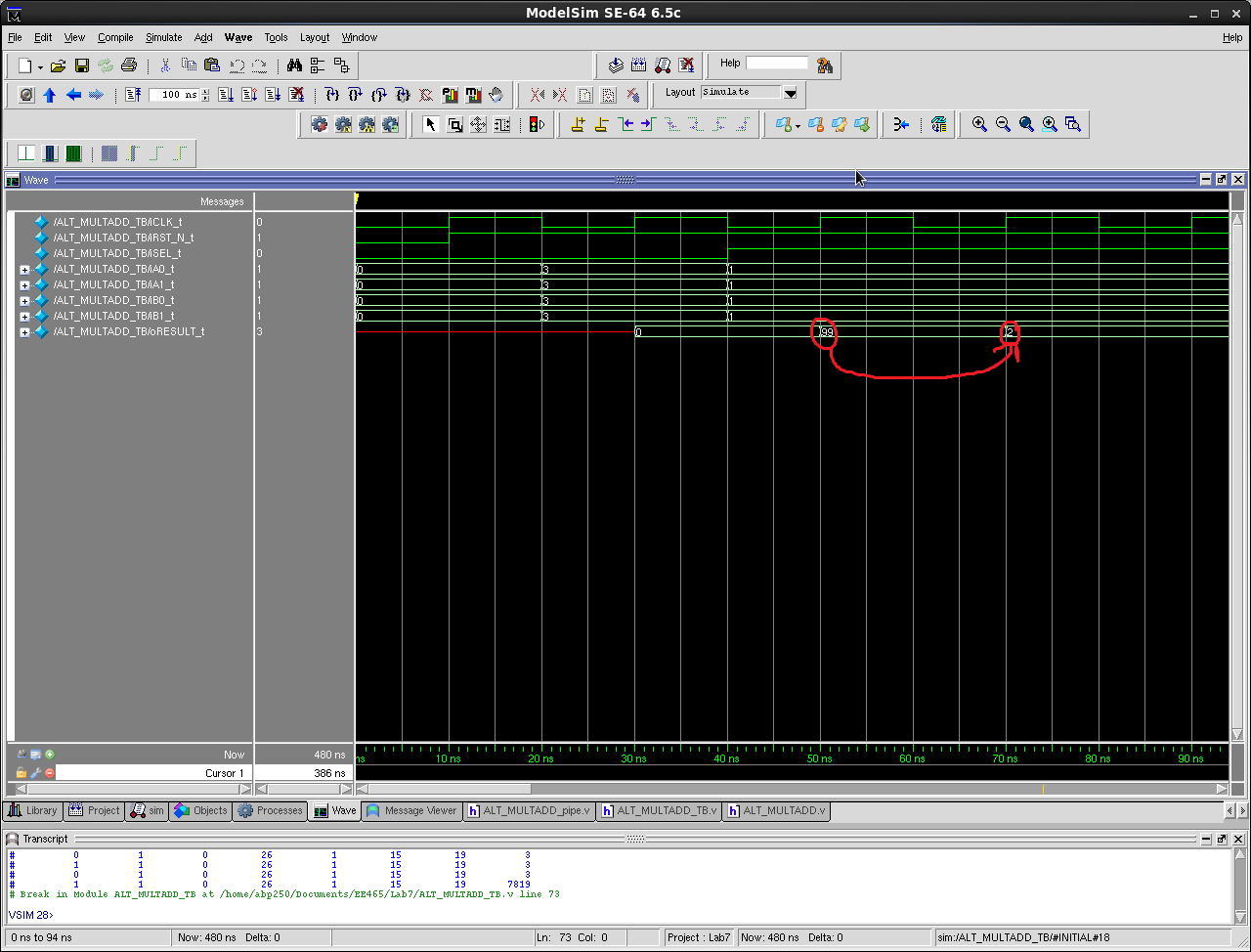
#4

$stop;

end

always #1 iCLK\_t = ~iCLK\_t;

endmodule



Good, the transition of oResult from 99 to 2 shows that the new design is working properly.

# Test control

# iCLK\_t iRST\_N\_t iSEL\_t iA0\_t iA1\_t iB0\_t iB1\_t oRESULT\_t

# 0 0 0 0 0 0 0 x

# 1 1 0 0 0 0 0 x

# 0 1 0 3 3 3 3 x

# 1 1 0 3 3 3 3 0

# 0 1 1 1 1 1 1 0

# 1 1 1 1 1 1 1 99

# 0 1 1 1 1 1 1 99

# 1 1 1 1 1 1 1 2

# 0 1 1 1 1 1 1 2

# 1 1 1 1 1 1 1 2

# 0 1 1 1 1 1 1 2

# 1 1 1 1 1 1 1 2

# 0 1 1 1 1 1 1 2

# 1 1 1 1 1 1 1 2

# 0 1 0 2 2 2 2 2

# 1 1 0 2 2 2 2 2

# 0 1 0 2 2 2 2 2

# 1 1 0 2 2 2 2 24

# 0 1 0 2 2 2 2 24

# 1 1 0 2 2 2 2 24

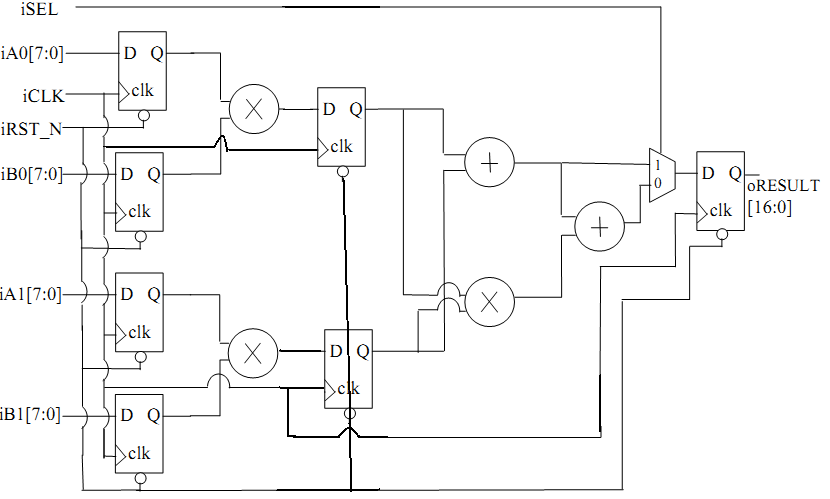
# 0 1 0 2 2 2 2 24

# 1 1 0 2 2 2 2 24

# 0 1 0 2 2 2 2 24

# 2 Pipelining

## Schematic:



## & Code:

module ALT\_MULTADD\_pipe(iCLK, iRST\_N, iSEL, iA0, iA1, iB0, iB1, oR);

input iCLK, iRST\_N, iSEL, iA0, iA1, iB0, iB1;

output oR;

wire iCLK, iRST\_N, iSEL;

wire [7:0] iA0, iA1, iB0, iB1;

reg SEL, SEL1;

reg [7:0] A0, A1, B0, B1, M0, M1;

reg [16:0] oR;

always @ (posedge iCLK)begin

A0 <= iA0;

A1 <= iA1;

B0 <= iB0;

B1 <= iB1;

M0 <= A0 \* B0;

M1 <= A1 \* B1;

SEL1 <= iSEL;

SEL <= SEL1;

if(iRST\_N)begin

if(SEL) begin

oR <= M0 + M1;

end

else begin

oR <= M0 + M1 + M0 \* M1;

end

end

else begin

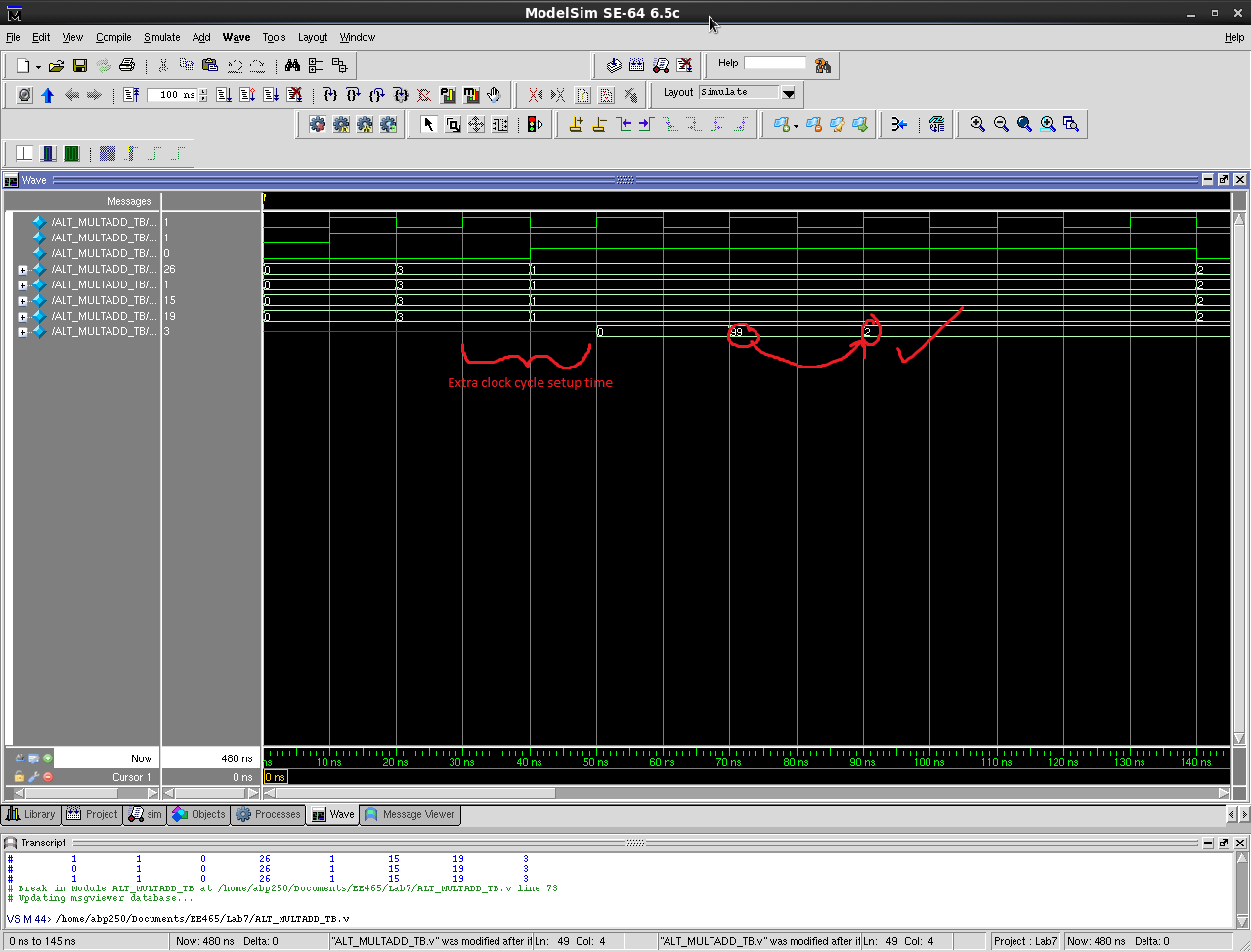
oR <= 0;

end

end

endmodule

# 3 Pipelined Design Waveform:

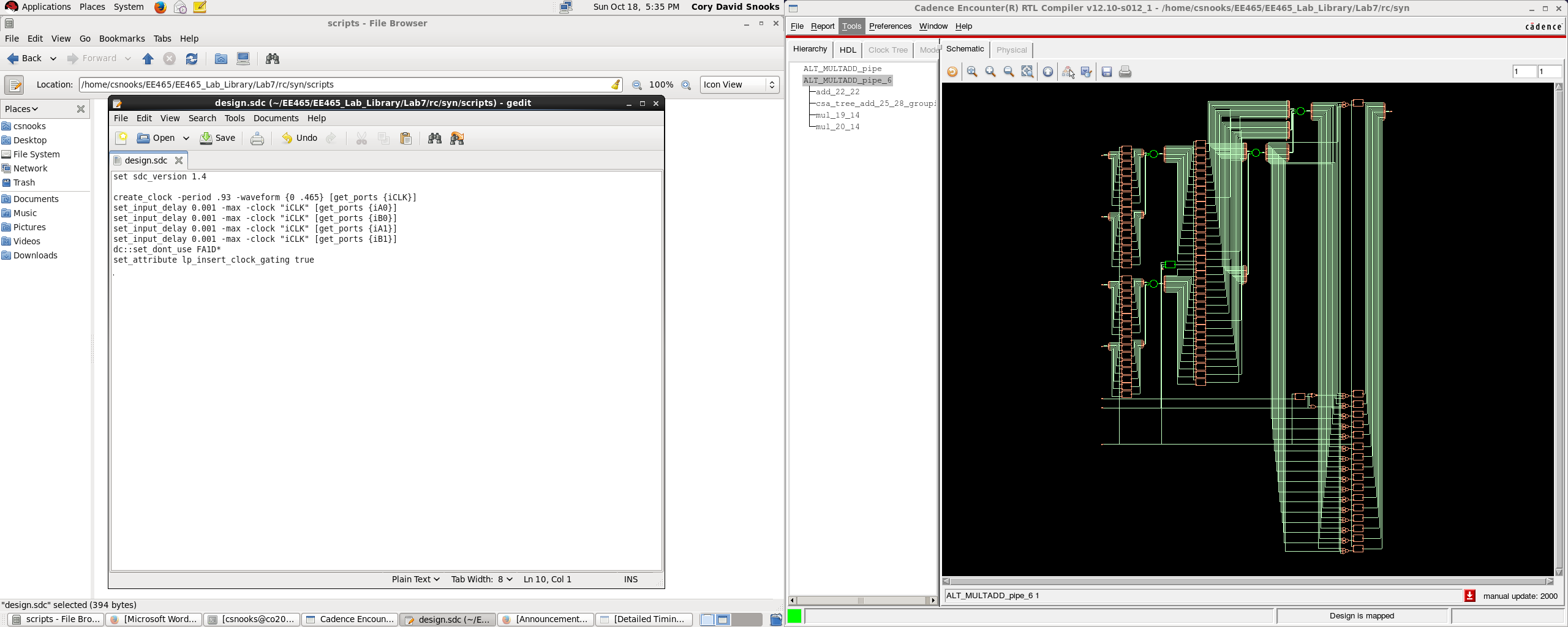


As you can see, the pipelining causes an extra clock cycle before output register outputs but throughput and functioning is still the same.

# 4 Synthesis:

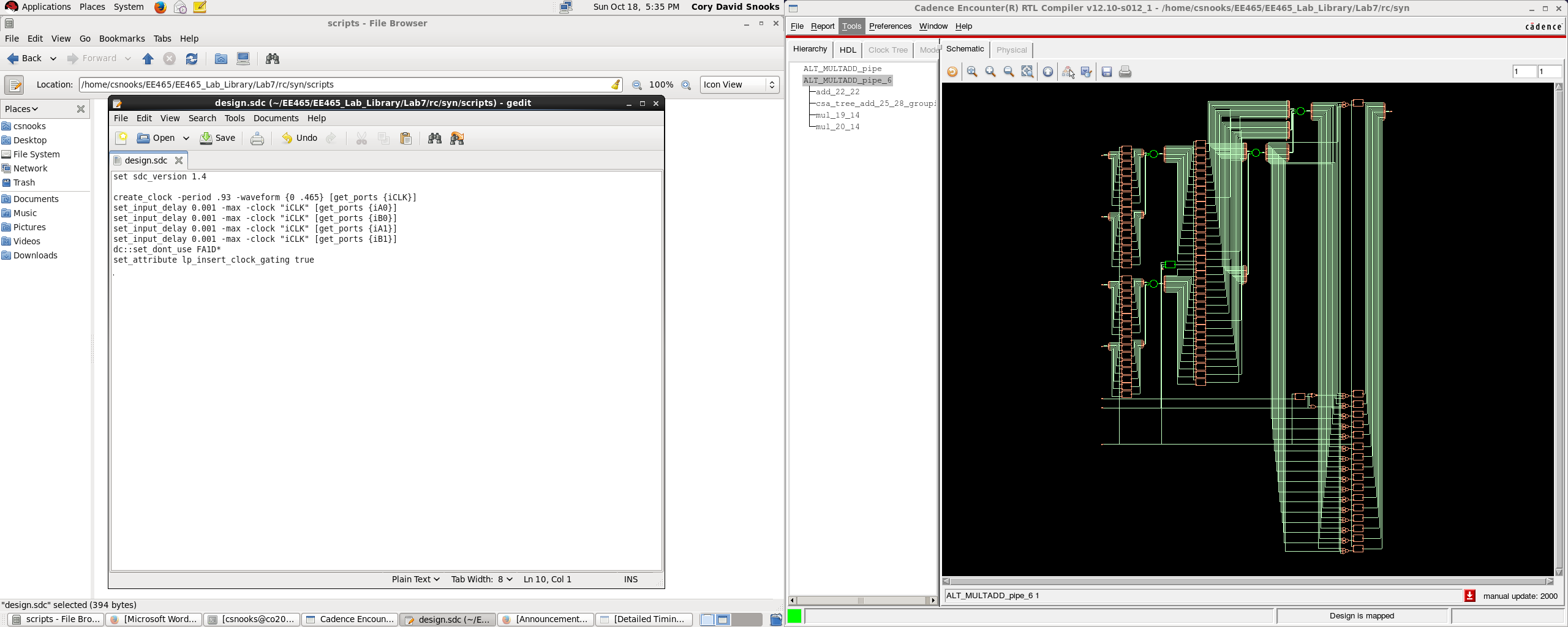
We synthesized both the circuits from above and compared differences between un-piped and piped designs.

## Design constraints:



After tuning the clock period, the lowest we were able to achieve is .93 ns.

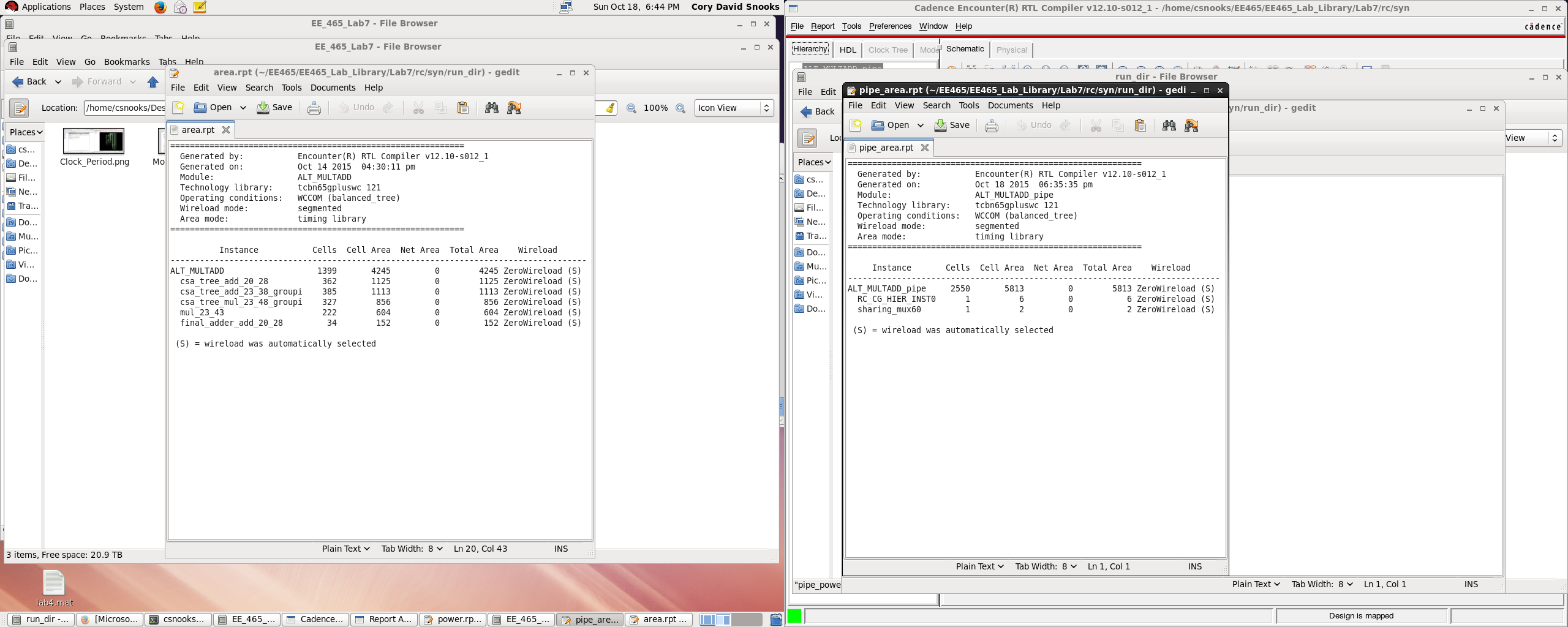
## Synthesized Schematic:



We see the registers located in-between the first logic computation stage and the second. This is what we want to see.

## Area report comparison:

We will compare the differences in area consumption between piped and non-piped designs.



### Non-Pipelined:

Instance Cells Cell Area Net Area Total Area Wireload

-------------------------------------------------------------------------------------

ALT\_MULTADD 1399 4245 0 4245 ZeroWireload (S)

csa\_tree\_add\_20\_28 362 1125 0 1125 ZeroWireload (S)

csa\_tree\_add\_23\_38\_groupi 385 1113 0 1113 ZeroWireload (S)

csa\_tree\_mul\_23\_48\_groupi 327 856 0 856 ZeroWireload (S)

mul\_23\_43 222 604 0 604 ZeroWireload (S)

final\_adder\_add\_20\_28 34 152 0 152 ZeroWireload (S)

### Pipelined:

Instance Cells Cell Area Net Area Total Area Wireload

----------------------------------------------------------------------------

ALT\_MULTADD\_pipe 2550 5813 0 5813 ZeroWireload (S)

RC\_CG\_HIER\_INST0 1 6 0 6 ZeroWireload (S)

sharing\_mux60 1 2 0 2 ZeroWireload (S)

The area increased from 4245 to 5813. This is expected because of the inserted registers which require extra area.

### Retime enabled:

Instance Cells Cell Area Net Area Total Area Wireload

---------------------------------------------------------------------------------------------------------

ALT\_MULTADD\_pipe 1370 3820 0 3820 ZeroWireload (S)

csa\_tree\_add\_25\_28 605 1517 0 1517 ZeroWireload (S)

mul\_19\_14 262 675 0 675 ZeroWireload (S)

mul\_20\_14 249 669 0 669 ZeroWireload (S)

final\_adder\_add\_25\_28\_Y\_final\_adder\_add\_22\_22 130 384 0 384 ZeroWireload (S)

sharing\_mux 25 64 0 64 ZeroWireload (S)

sharing\_mux59 25 57 0 57 ZeroWireload (S)

RC\_CG\_HIER\_INST0 1 6 0 6 ZeroWireload (S)

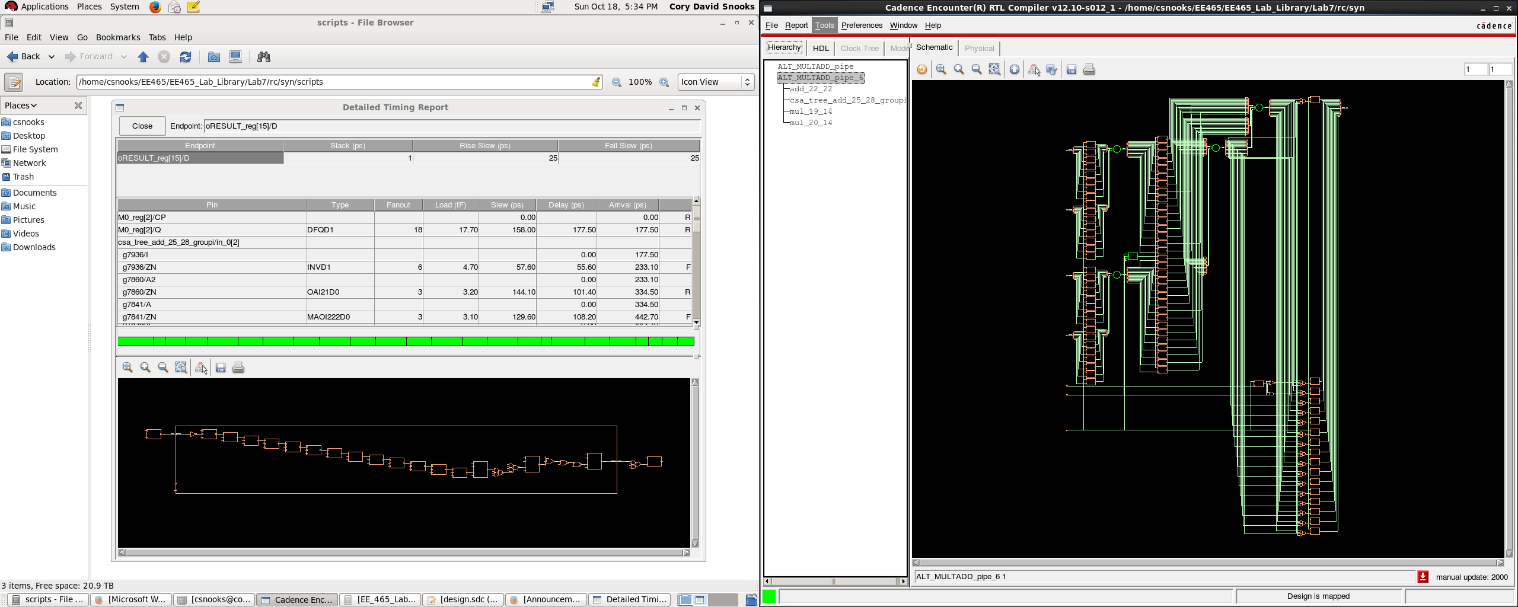
sharing\_mux60 1 2 0 2 ZeroWireload (S)

We can see that the types of cells synthesized is different from when retime was not enabled.

## Timing Comparison:

Here, we will compare the timing of the non-pipelined vs the pipelined logic.

Here are the pipelined timing reports:



### Pipelined:

Pin Type Fanout Load Slew Delay Arrival

(fF) (ps) (ps) (ps)

--------------------------------------------------------------------------

(clock iCLK) launch 0 R

M1\_reg[3]/CP 0 0 R

M1\_reg[3]/Q DFQD4 5 9.4 33 +127 127 F

g11957/I +0 127

g11957/ZN CKND4 6 9.2 26 +25 152 R

csa\_tree\_add\_25\_28\_g13816/I +0 152

csa\_tree\_add\_25\_28\_g13816/ZN CKND2 5 8.7 33 +28 180 F

csa\_tree\_add\_25\_28\_g8295/A2 +0 180

csa\_tree\_add\_25\_28\_g8295/ZN CKND2D2 1 3.4 34 +31 211 R

csa\_tree\_add\_25\_28\_g8105/A2 +0 211

csa\_tree\_add\_25\_28\_g8105/ZN ND2D3 6 6.8 34 +34 245 F

csa\_tree\_add\_25\_28\_g7643/B1 +0 245

csa\_tree\_add\_25\_28\_g7643/ZN MOAI22D1 2 2.3 43 +64 309 F

csa\_tree\_add\_25\_28\_g7515/A1 +0 309

csa\_tree\_add\_25\_28\_g7515/ZN CKND2D1 2 3.3 54 +42 351 R

g13591/A2 +0 351

g13591/ZN CKND2D2 2 2.3 23 +30 380 F

g319/A1 +0 380

g319/Z OA21D1 2 2.8 31 +62 443 F

g10928/A1 +0 443

g10928/ZN NR2XD1 2 2.1 32 +27 470 R

g10931/A1 +0 470

g10931/ZN MOAI22D1 1 1.1 32 +26 496 F

g12279/A1 +0 496

g12279/ZN CKND2D1 1 1.2 32 +27 522 R

g12278/B +0 522

g12278/ZN IOA21D1 2 2.8 43 +35 557 F

g13149/A2 +0 557

g13149/ZN NR2XD1 3 3.8 46 +45 602 R

g11685/A1 +0 602

g11685/ZN NR2XD1 1 2.1 25 +26 628 F

g11684/A1 +0 628

g11684/ZN NR2D2 3 3.3 46 +34 663 R

g12706/A1 +0 663

g12706/ZN NR3D1 1 1.7 31 +26 689 F

g13640/A1 +0 689

g13640/ZN NR2XD1 1 4.0 48 +36 724 R

g13249/A1 +0 724

g13249/ZN CKND2D4 8 8.8 33 +32 757 F

g11694/I +0 757

g11694/ZN CKND0 1 1.2 32 +29 786 R

g35/A1 +0 786

g35/ZN NR2D1 2 2.4 25 +22 808 F

g12966/A1 +0 808

g12966/ZN OAI21D1 1 1.2 47 +35 843 R

g845/A1 +0 843

g845/ZN ND3D1 1 1.2 46 +41 884 F

g844/A1 +0 884

g844/ZN ND2D1 1 1.1 26 +26 909 R

oRESULT\_reg[11]/D DFQD1 +0 909

oRESULT\_reg[11]/CP setup 0 +31 940 R

- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

(clock iCLK) capture 940 R

--------------------------------------------------------------------------

Cost Group : 'iCLK' (path\_group 'iCLK')

Timing slack : 0ps

Start-point : M1\_reg[3]/CP

End-point : oRESULT\_reg[11]/D

### Non- Pipelined:

Pin Type Fanout Load Slew Delay Arrival

(fF) (ps) (ps) (ps)

-----------------------------------------------------------------

(clock iCLK) launch 0 R

A0\_reg[5]/CP 0 0 R

A0\_reg[5]/Q DFQD1 16 19.0 169 +183 183 R

mul\_23\_43/A[5]

g3067/A2 +0 183

g3067/ZN ND2D1 2 2.2 62 +59 242 F

g2991/A2 +0 242

g2991/ZN XNR2D1 2 3.3 44 +112 354 F

g3097/A1 +0 354

g3097/Z XOR3D1 2 3.3 48 +190 544 R

g3092/A1 +0 544

g3092/ZN XNR3D1 2 2.3 40 +193 737 R

g2881/A1 +0 737

g2881/ZN NR2D1 2 2.2 24 +24 761 F

g2856/B +0 761

g2856/ZN AOI21D1 3 3.6 94 +71 832 R

g2855/I +0 832

g2855/ZN INVD1 1 1.2 28 +27 859 F

g2842/A1 +0 859

g2842/Z AO21D1 2 2.8 32 +62 921 F

g2831/A1 +0 921

g2831/ZN XNR2D1 9 10.8 80 +111 1032 F

mul\_23\_43/Z[7]

csa\_tree\_mul\_23\_48\_groupi/in\_0[7]

g4897/B1 +0 1032

g4897/ZN MOAI22D1 2 2.2 88 +75 1108 F

g4859/B1 +0 1108

g4859/ZN AOI22D1 2 3.3 104 +90 1198 R

g4981/A1 +0 1198

g4981/ZN XNR3D1 2 2.1 39 +203 1401 R

g4681/A1 +0 1401

g4681/ZN CKND2D1 2 2.1 43 +32 1433 F

g4669/A1 +0 1433

g4669/ZN INR2D1 2 2.4 28 +58 1490 F

g4654/A1 +0 1490

g4654/ZN MOAI22D1 9 10.7 213 +127 1618 R

csa\_tree\_mul\_23\_48\_groupi/out\_0[7]

csa\_tree\_add\_23\_38\_groupi/in\_0[7]

g6496/B1 +0 1618

g6496/ZN MAOI22D1 2 1.5 78 +94 1712 R

g6404/B2 +0 1712

g6404/Z OA22D0 2 3.3 74 +112 1824 R

g6587/A1 +0 1824

g6587/ZN XNR3D1 2 3.7 51 +207 2031 R

g6578/A2 +0 2031

g6578/ZN XNR3D1 2 3.2 47 +201 2232 R

g6247/B +0 2232

g6247/ZN MAOI222D1 2 2.8 113 +93 2325 F

g6564/A2 +0 2325

g6564/ZN XNR3D1 2 2.3 40 +212 2536 R

g6189/A1 +0 2536

g6189/ZN NR2D1 2 2.1 40 +23 2560 F

g6124/B +0 2560

g6124/Z AO21D1 3 3.6 36 +85 2645 F

g6122/A2 +0 2645

g6122/ZN AOI21D1 2 2.4 73 +53 2697 R

g6121/B1 +0 2697

g6121/ZN MOAI22D1 1 0.8 44 +65 2763 R

csa\_tree\_add\_23\_38\_groupi/out\_0[16]

g491/A1 +0 2763

g491/Z AO22D0 1 1.1 47 +76 2838 R

oRESULT\_reg[16]/D DFQD1 +0 2838

oRESULT\_reg[16]/CP setup 0 +35 2874 R

- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

(clock iCLK) capture 3000 R

-----------------------------------------------------------------

Cost Group : 'iCLK' (path\_group 'iCLK')

Timing slack : 126ps

Start-point : A0\_reg[5]/CP

End-point : oRESULT\_reg[16]/D

The setup rise time is much shorter for the pipelined version as you can see it is 940ps for the pipelined and 3000 ps for the non-pipelined version.

### Retime Enabled:

============================================================

Generated by: Encounter(R) RTL Compiler v12.10-s012\_1

Generated on: Oct 18 2015 06:50:41 pm

Module: ALT\_MULTADD\_pipe

Technology library: tcbn65gpluswc 121

Operating conditions: WCCOM (balanced\_tree)

Wireload mode: segmented

Area mode: timing library

============================================================

Pin Type Fanout Load Slew Delay Arrival

(fF) (ps) (ps) (ps)

--------------------------------------------------------------------

(clock iCLK) launch 0 R

retime\_s2\_31\_reg/CP 0 0 R

retime\_s2\_31\_reg/Q DFQD2 12 16.4 55 +155 155 F

csa\_tree\_add\_25\_28/in\_3[9]

g20821/I +0 155

g20821/ZN INVD4 16 18.0 47 +41 196 R

g20970/A2 +0 196

g20970/ZN IOA21D1 1 3.6 50 +81 277 R

g20531/A2 +0 277

g20531/ZN NR2XD2 8 8.2 36 +38 315 F

g20966/B1 +0 315

g20966/Z AO22D1 2 2.3 33 +87 402 F

g20245/A2 +0 402

g20245/ZN NR2D1 1 2.2 59 +47 449 R

g20223/B +0 449

g20223/ZN IAO21D2 1 2.1 28 +21 470 F

g20997/CI +0 470

g20997/S FICOND2 4 4.7 42 +96 567 R

g20121/B1 +0 567

g20121/ZN MAOI22D1 2 2.4 73 +78 645 R

g20083/B1 +0 645

g20083/ZN MOAI22D1 3 4.5 110 +82 727 R

g20059/A +0 727

g20059/ZN MAOI222D1 1 1.2 84 +72 800 F

csa\_tree\_add\_25\_28/out\_0[13]

sharing\_mux59/in\_0[13]

g691/A1 +0 800

g691/Z AO21D1 2 2.1 29 +73 872 F

sharing\_mux59/z[13]

final\_adder\_add\_25\_28\_Y\_final\_adder\_add\_22\_22/B[13]

g1837/A2 +0 872

g1837/ZN NR2XD0 1 1.1 38 +34 907 R

retime\_s3\_13\_reg/D DFQD1 +0 907

retime\_s3\_13\_reg/CP setup 0 +33 940 R

- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

(clock iCLK) capture 940 R

--------------------------------------------------------------------

Cost Group : 'iCLK' (path\_group 'iCLK')

Timing slack : 0ps

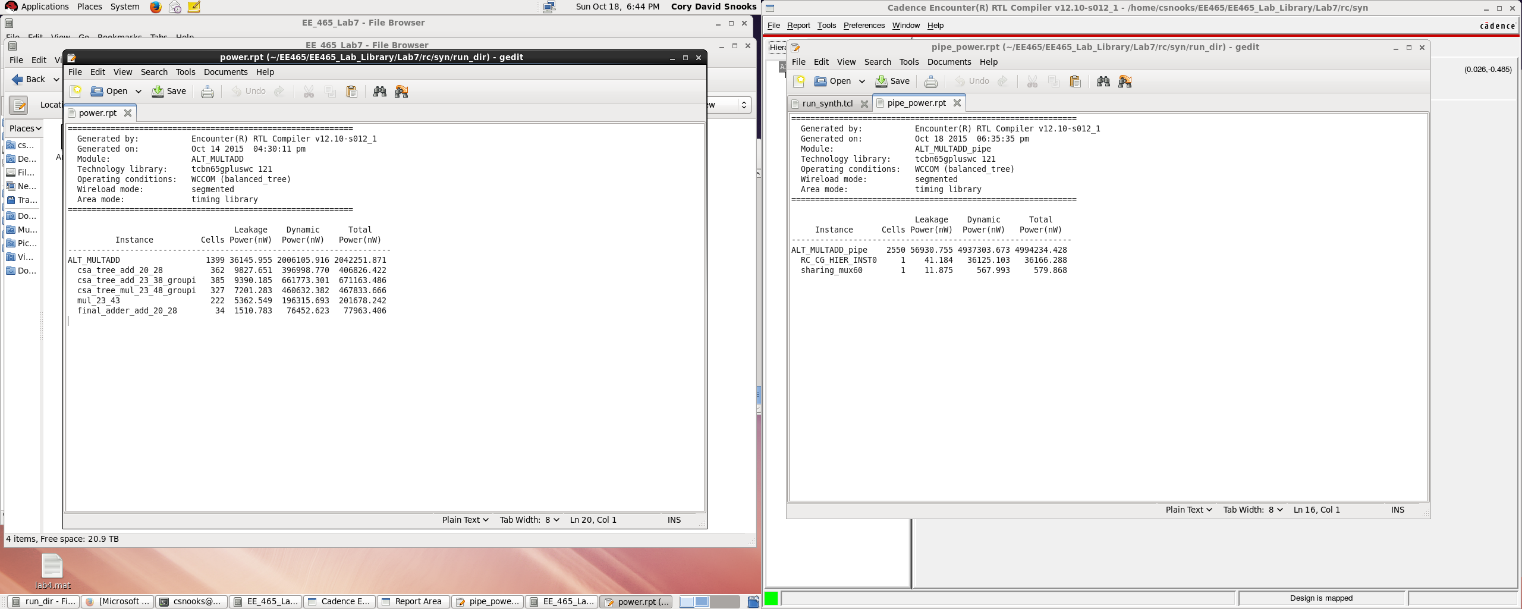
Start-point : retime\_s2\_31\_reg/CP

End-point : final\_adder\_add\_25\_28\_Y\_final\_adder\_add\_22\_22/retime\_s3\_13\_reg/D

With retime enabled, we see don’t see much change other than the types and number of gates used. The slack time is same as the pipelined without retime enabled.

## Power Comparison:

We will compare the power consumption of the non-piplined vs the pipelined logic.



### Non-pipelined:

Instance Cells Power(nW) Power(nW) Power(nW)

--------------------------------------------------------------------

ALT\_MULTADD 1399 36145.955 2006105.916 2042251.871

csa\_tree\_add\_20\_28 362 9827.651 396998.770 406826.422

csa\_tree\_add\_23\_38\_groupi 385 9390.185 661773.301 671163.486

csa\_tree\_mul\_23\_48\_groupi 327 7201.283 460632.382 467833.666

mul\_23\_43 222 5362.549 196315.693 201678.242

final\_adder\_add\_20\_28 34 1510.783 76452.623 77963.406

### Pipelined:

Leakage Dynamic Total

Instance Cells Power(nW) Power(nW) Power(nW)

-----------------------------------------------------------

ALT\_MULTADD\_pipe 2550 56930.755 4937303.673 4994234.428

RC\_CG\_HIER\_INST0 1 41.184 36125.103 36166.288

sharing\_mux60 1 11.875 567.993 579.868

### Pipelined Retime:

Leakage Dynamic Total

Instance Cells Power(nW) Power(nW) Power(nW)

--------------------------------------------------------------------

ALT\_MULTADD\_pipe 1370 31988.559 3570951.409 3602939.968

csa\_tree\_add\_25\_28 605 13603.837 1339405.062 1353008.898

mul\_19\_14 262 5674.255 447626.928 453301.183

mul\_20\_14 249 5647.303 420800.942 426448.246

final\_adde..der\_add\_22\_22 130 2550.018 384372.458 386922.476

sharing\_mux 25 456.713 47143.090 47599.803

sharing\_mux59 25 362.531 36462.034 36824.565

RC\_CG\_HIER\_INST0 1 41.184 27935.244 27976.429

sharing\_mux60 1 11.899 320.077 331.976

As you can see, the pipelined design’s power is much higher than the non-pipelined version. The pipelined version is more than double the power consumption.

## Gate Report Comparison:

### Pipelined:

Gate Instances Area Library

------------------------------------------------

AN2D2 2 5.040 tcbn65gpluswc

AN2D4 4 17.280 tcbn65gpluswc

AN2XD1 49 105.840 tcbn65gpluswc

AN3XD1 1 2.520 tcbn65gpluswc

AO21D1 14 35.280 tcbn65gpluswc

AO22D0 1 2.880 tcbn65gpluswc

AO22D1 6 19.440 tcbn65gpluswc

AO22D2 2 7.920 tcbn65gpluswc

AOI21D1 17 36.720 tcbn65gpluswc

AOI21D2 8 25.920 tcbn65gpluswc

AOI22D0 1 2.520 tcbn65gpluswc

AOI22D1 9 22.680 tcbn65gpluswc

AOI22D2 10 43.200 tcbn65gpluswc

AOI31D2 1 4.320 tcbn65gpluswc

...

MAOI222D1 39 112.320 tcbn65gpluswc

MAOI22D1 12 34.560 tcbn65gpluswc

MOAI22D0 5 14.400 tcbn65gpluswc

MOAI22D1 93 267.840 tcbn65gpluswc

MUX2ND0 4 11.520 tcbn65gpluswc

ND2D0 20 28.800 tcbn65gpluswc

ND2D1 371 534.240 tcbn65gpluswc

ND2D2 219 551.880 tcbn65gpluswc

ND2D3 9 29.160 tcbn65gpluswc

ND2D4 8 34.560 tcbn65gpluswc

ND3D1 24 51.840 tcbn65gpluswc

ND3D2 16 51.840 tcbn65gpluswc

ND4D1 1 2.520 tcbn65gpluswc

NR2D0 4 5.760 tcbn65gpluswc

NR2D1 39 56.160 tcbn65gpluswc

NR2D2 18 45.360 tcbn65gpluswc

NR2D3 4 12.960 tcbn65gpluswc

NR2D4 1 4.320 tcbn65gpluswc

NR2XD0 67 96.480 tcbn65gpluswc

NR2XD1 69 173.880 tcbn65gpluswc

NR2XD2 35 151.200 tcbn65gpluswc

NR2XD3 2 12.240 tcbn65gpluswc

NR2XD4 2 15.840 tcbn65gpluswc

NR3D1 2 6.480 tcbn65gpluswc

OA21D1 14 35.280 tcbn65gpluswc

OA21D2 1 2.880 tcbn65gpluswc

OAI21D1 44 95.040 tcbn65gpluswc

OAI21D2 11 35.640 tcbn65gpluswc

OAI21D4 3 19.440 tcbn65gpluswc

OAI221D1 2 6.480 tcbn65gpluswc

OAI22D1 14 35.280 tcbn65gpluswc

OAI22D2 4 17.280 tcbn65gpluswc

OAI31D1 2 5.040 tcbn65gpluswc

OR2D0 1 2.160 tcbn65gpluswc

OR2D1 16 34.560 tcbn65gpluswc

OR2XD1 5 10.800 tcbn65gpluswc

XNR2D1 10 36.000 tcbn65gpluswc

XNR3D1 6 36.720 tcbn65gpluswc

XOR2D1 7 25.200 tcbn65gpluswc

XOR3D1 9 55.080 tcbn65gpluswc

------------------------------------------------

total 2550 5812.560

Type Instances Area Area %

-------------------------------------------------------

sequential 82 621.360 10.7

inverter 506 657.720 11.3

buffer 31 59.040 1.0

clock\_gating\_integrated\_cell 1 6.480 0.1

logic 1930 4467.960 76.9

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total 2550 5812.560 100.0

### Non-pipelined:

Gate Instances Area Library

------------------------------------------------

AN2XD1 24 51.840 tcbn65gpluswc

AO21D1 4 10.080 tcbn65gpluswc

AO221D0 2 7.200 tcbn65gpluswc

AO22D0 25 72.000 tcbn65gpluswc

AOI211XD0 1 2.520 tcbn65gpluswc

AOI21D1 12 25.920 tcbn65gpluswc

AOI22D1 54 136.080 tcbn65gpluswc

CKND0 2 2.160 tcbn65gpluswc

CKND1 37 39.960 tcbn65gpluswc

CKND2D1 53 76.320 tcbn65gpluswc

CKXOR2D1 4 14.400 tcbn65gpluswc

CMPE42D1 1 16.560 tcbn65gpluswc

DFQD1 50 342.000 tcbn65gpluswc

FCICIND1 3 14.040 tcbn65gpluswc

FICIND1 3 31.320 tcbn65gpluswc

HA1D0 11 63.360 tcbn65gpluswc

IAO21D1 2 5.040 tcbn65gpluswc

IND2D1 21 45.360 tcbn65gpluswc

INR2D1 7 15.120 tcbn65gpluswc

INR2XD0 21 45.360 tcbn65gpluswc

INVD1 50 54.000 tcbn65gpluswc

MAOI222D0 10 28.800 tcbn65gpluswc

MAOI222D1 198 570.240 tcbn65gpluswc

MAOI22D1 91 262.080 tcbn65gpluswc

MOAI22D1 141 406.080 tcbn65gpluswc

MUX2D0 1 3.240 tcbn65gpluswc

MUX2ND0 3 8.640 tcbn65gpluswc

ND2D1 187 269.280 tcbn65gpluswc

NR2D1 25 36.000 tcbn65gpluswc

NR2XD0 45 64.800 tcbn65gpluswc

OA21D1 11 27.720 tcbn65gpluswc

OA221D0 1 3.600 tcbn65gpluswc

OA22D0 20 57.600 tcbn65gpluswc

OAI211D1 1 2.520 tcbn65gpluswc

OAI21D1 14 30.240 tcbn65gpluswc

OAI221D0 4 11.520 tcbn65gpluswc

OAI22D1 42 105.840 tcbn65gpluswc

OR2D1 1 2.160 tcbn65gpluswc

OR2XD1 1 2.160 tcbn65gpluswc

XNR2D1 14 50.400 tcbn65gpluswc

XNR3D1 120 734.400 tcbn65gpluswc

XNR4D1 1 9.000 tcbn65gpluswc

XOR2D1 3 10.800 tcbn65gpluswc

XOR3D1 78 477.360 tcbn65gpluswc

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total 1399 4245.120

Type Instances Area Area %

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sequential 50 342.000 8.1

inverter 89 96.120 2.3

logic 1260 3807.000 89.7

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total 1399 4245.120 100.0

# Conclusion:

### Pipelined:

Gate Instances Area Library

------------------------------------------------

AN2XD1 11 23.760 tcbn65gpluswc

AO21D1 5 12.600 tcbn65gpluswc

AO22D0 27 77.760 tcbn65gpluswc

AO22D1 29 93.960 tcbn65gpluswc

AO22D2 1 3.960 tcbn65gpluswc

AOI21D0 1 2.160 tcbn65gpluswc

AOI21D1 25 54.000 tcbn65gpluswc

AOI21D2 2 6.480 tcbn65gpluswc

AOI221D0 4 11.520 tcbn65gpluswc

AOI22D1 47 118.440 tcbn65gpluswc

...

MUX2ND0 1 2.880 tcbn65gpluswc

ND2D0 7 10.080 tcbn65gpluswc

ND2D1 169 243.360 tcbn65gpluswc

ND2D2 6 15.120 tcbn65gpluswc

ND2D3 2 6.480 tcbn65gpluswc

ND2D4 1 4.320 tcbn65gpluswc

NR2D0 10 14.400 tcbn65gpluswc

NR2D1 39 56.160 tcbn65gpluswc

NR2D3 1 3.240 tcbn65gpluswc

NR2XD0 55 79.200 tcbn65gpluswc

NR2XD1 4 10.080 tcbn65gpluswc

NR2XD2 2 8.640 tcbn65gpluswc

NR2XD3 2 12.240 tcbn65gpluswc

NR2XD4 1 7.920 tcbn65gpluswc

NR3D0 1 2.160 tcbn65gpluswc

OA21D1 9 22.680 tcbn65gpluswc

OA22D0 3 8.640 tcbn65gpluswc

OA22D1 1 3.240 tcbn65gpluswc

OAI211D0 1 2.520 tcbn65gpluswc

OAI21D0 6 12.960 tcbn65gpluswc

OAI21D1 22 47.520 tcbn65gpluswc

OAI221D0 3 8.640 tcbn65gpluswc

OAI22D1 46 115.920 tcbn65gpluswc

OAI22D2 3 12.960 tcbn65gpluswc

OAI31D0 1 2.520 tcbn65gpluswc

OR2D1 3 6.480 tcbn65gpluswc

OR2XD1 5 10.800 tcbn65gpluswc

SDFQND0 2 15.840 tcbn65gpluswc

XNR2D1 17 61.200 tcbn65gpluswc

XNR3D1 23 140.760 tcbn65gpluswc

XNR3D4 1 10.440 tcbn65gpluswc

XNR4D1 1 9.000 tcbn65gpluswc

XOR2D1 2 7.200 tcbn65gpluswc

XOR3D1 28 171.360 tcbn65gpluswc

XOR3D2 1 6.840 tcbn65gpluswc

XOR4D1 1 9.000 tcbn65gpluswc

------------------------------------------------

total 1370 3820.320

Type Instances Area Area %

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sequential 109 771.480 20.2

inverter 134 163.080 4.3

clock\_gating\_integrated\_cell 1 6.480 0.2

logic 1126 2879.280 75.4

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total 1370 3820.320 100.0

The overall result of pipelining is an increase of the maximum stable clock frequency of the circuit but an increase in the area required due to the extra registers. So if area was not a concern, pipelining would be a good option to increase the clock speed limits.