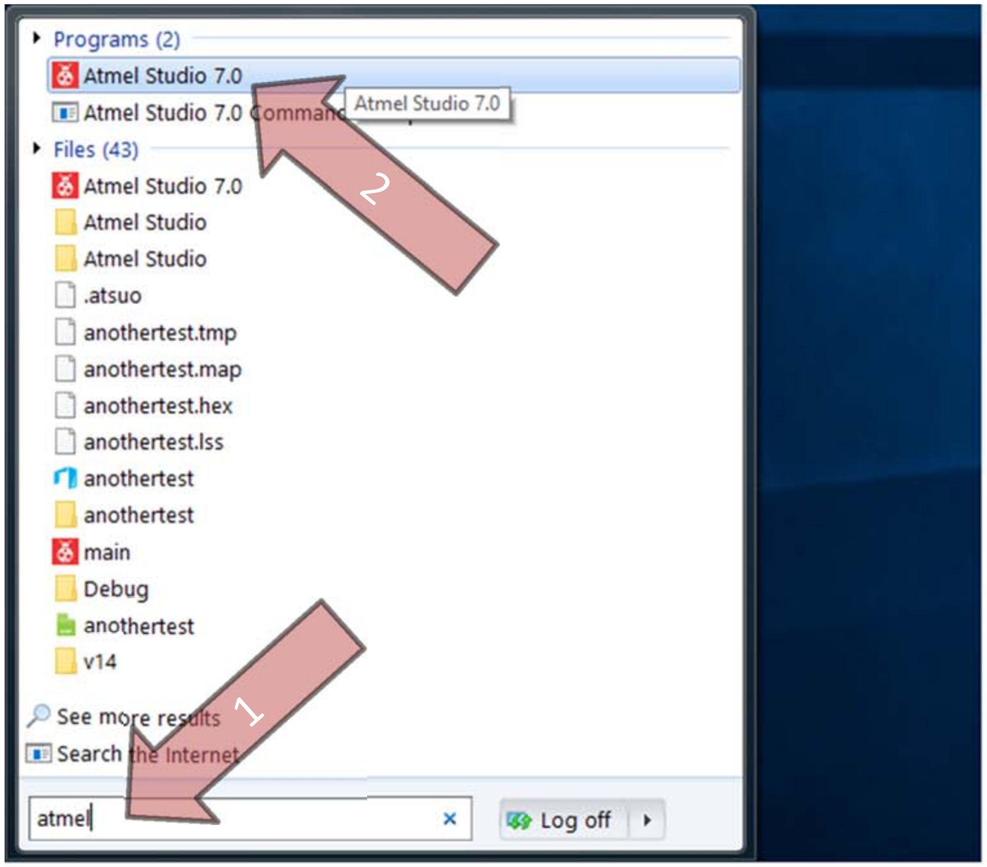
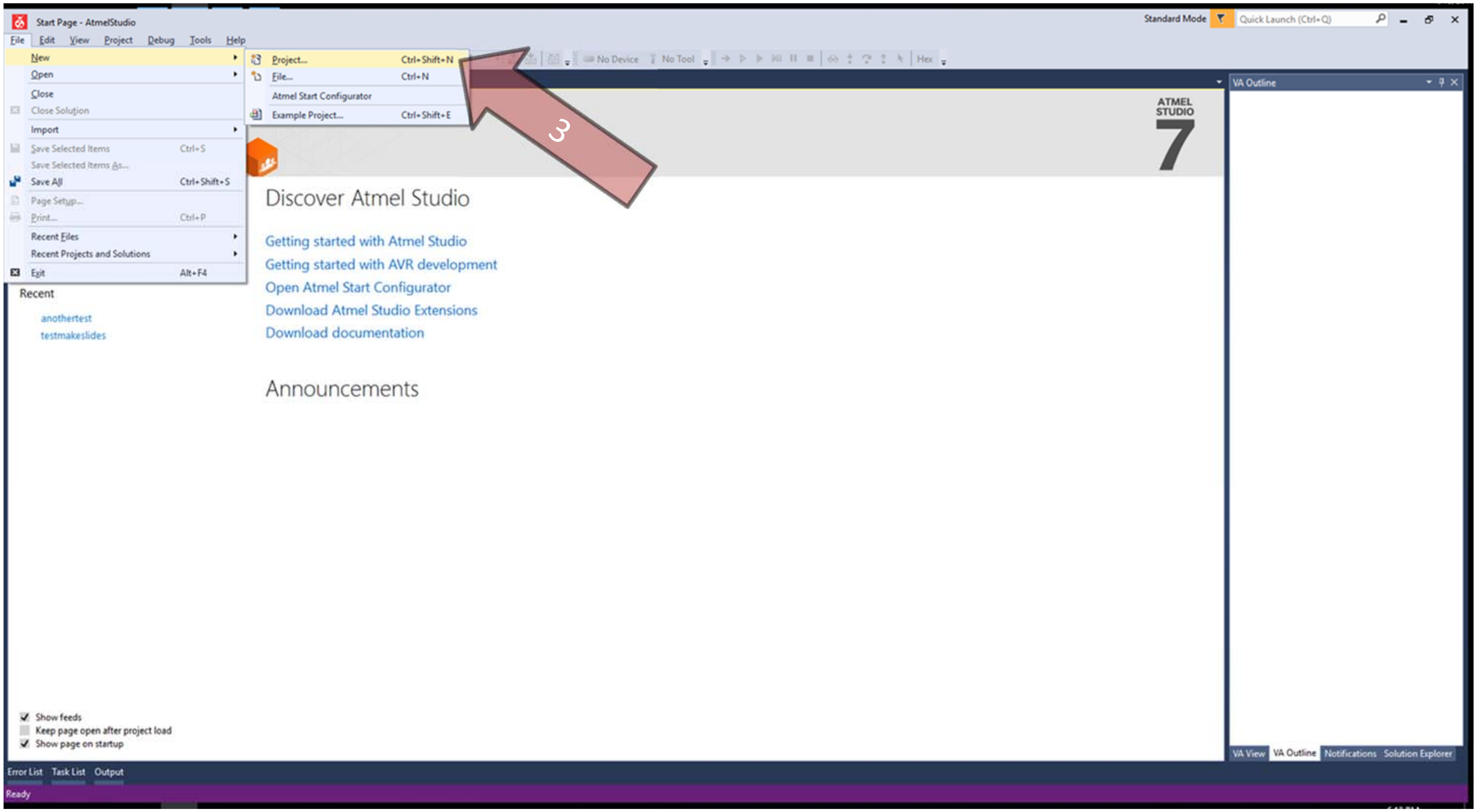
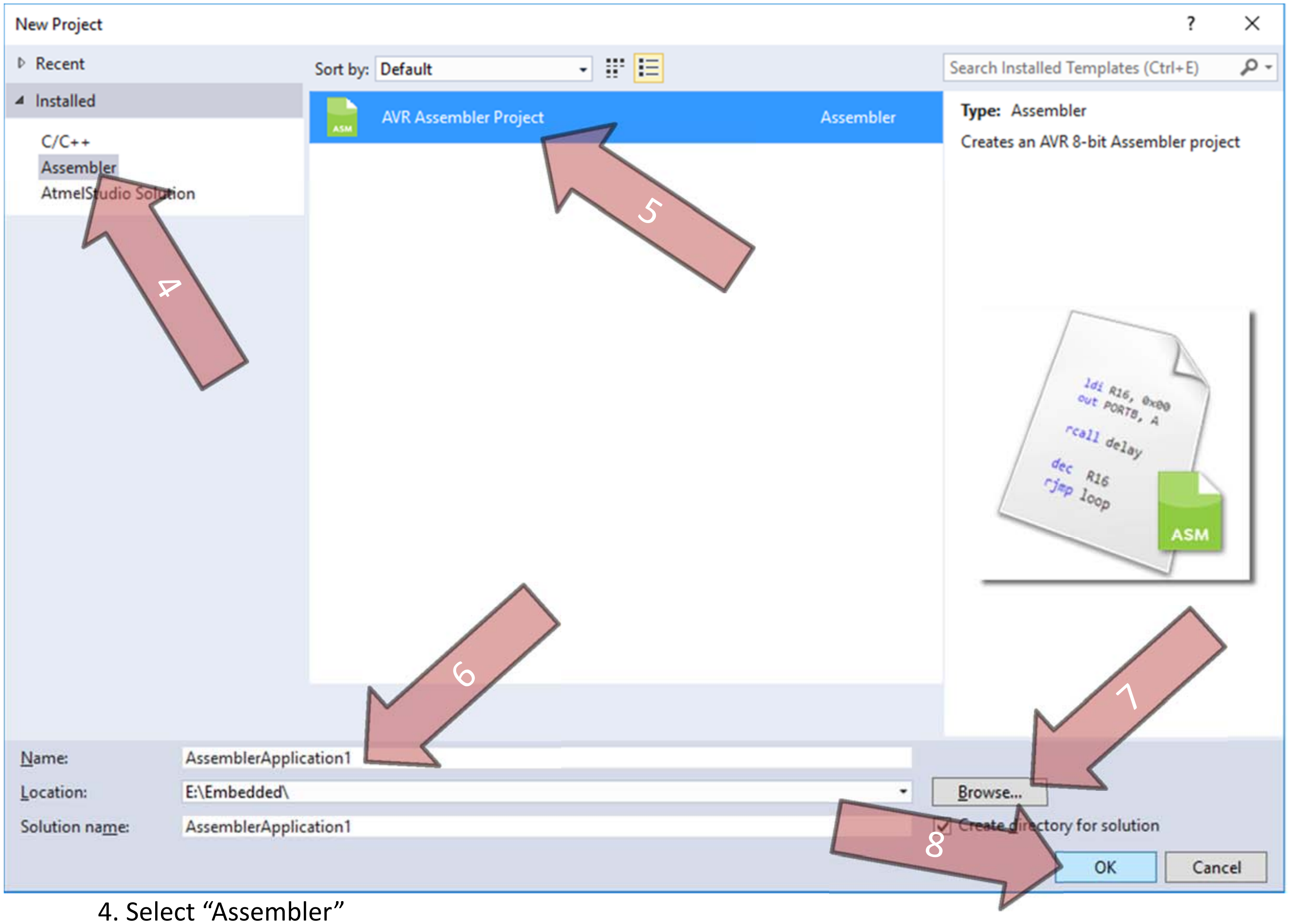
AVR Simulation Tutorial (v3.0)



1. Search for Atmel in the start menu
2. Locate Atmel Studio 7.0 and open it



3. When the program opens, navigate to "File" -> "New" -> "Project…" and click it


New Project

Sort by: Default

Search Installed Templates (Ctrl+E)

AVR Assembler Project — Assembler

Type: Assembler

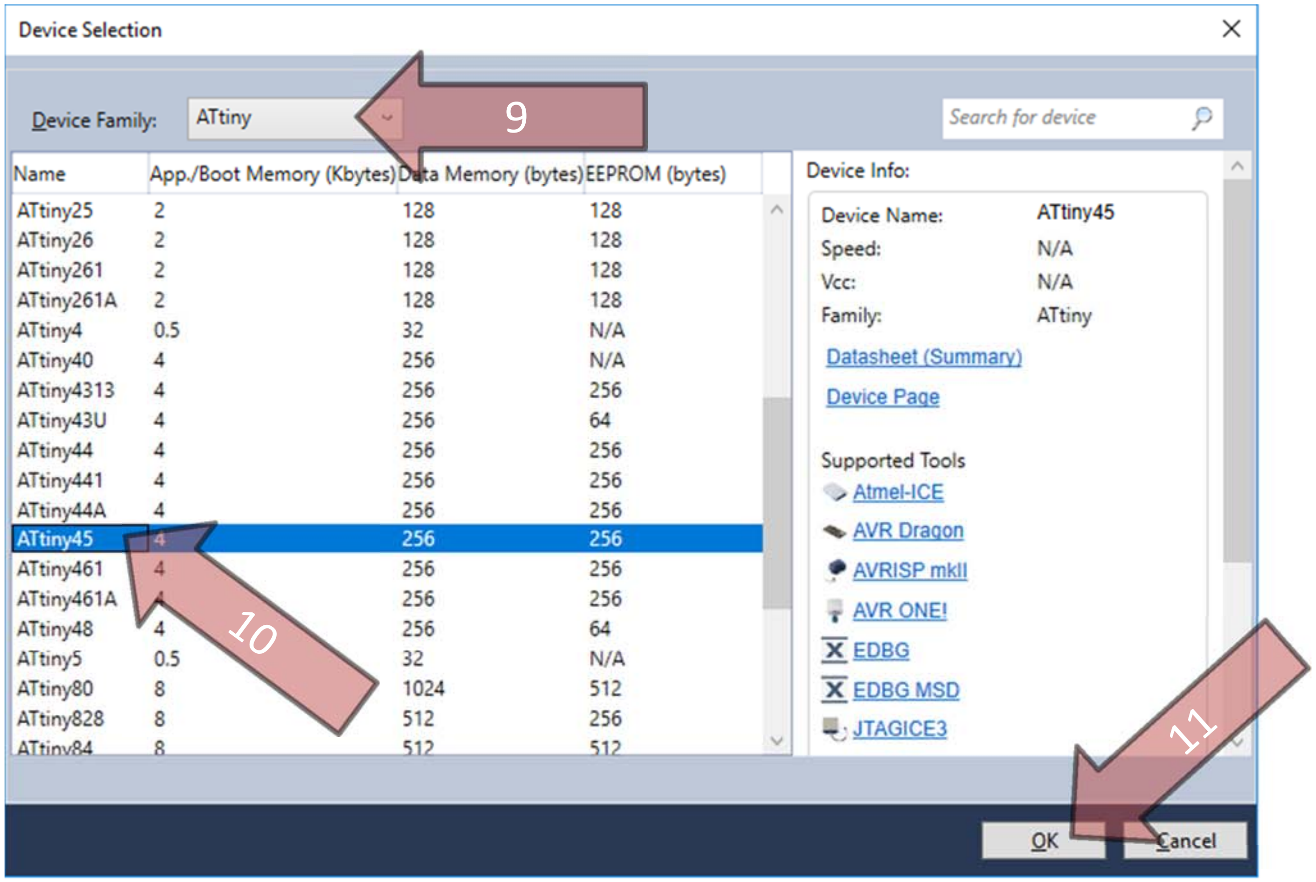
Creates an AVR 8-bit Assembler project

Name: AssemblerApplication1

Location: E:\Embedded\

Solution name: AssemblerApplication1

4. Select “Assembler”
5. Select “AVR Assembler Project”
6. Name the Project
7. Select the save location
8. Click “OK”



Device Family: ATtiny

Name	App./Boot Memory (Kbytes)	Data Memory (bytes)	EEPROM (bytes)
ATtiny25	2	128	128
ATtiny26	2	128	128
ATtiny261	2	128	128
ATtiny261A	2	128	128
ATtiny4	0.5	32	N/A
ATtiny40	4	256	N/A
ATtiny4313	4	256	256
ATtiny43U	4	256	64
ATtiny44	4	256	256
ATtiny441	4	256	256
ATtiny44A	4	256	256
ATtiny45	4	256	256
ATtiny461	4	256	256
ATtiny461A	4	256	256
ATtiny48	4	256	64
ATtiny5	0.5	32	N/A
ATtiny80	8	1024	512
ATtiny828	8	512	256
ATtiny84	8	512	512

Device Info:

Device Name:	ATtiny45
Speed:	N/A
Vcc:	N/A
Family:	ATtiny

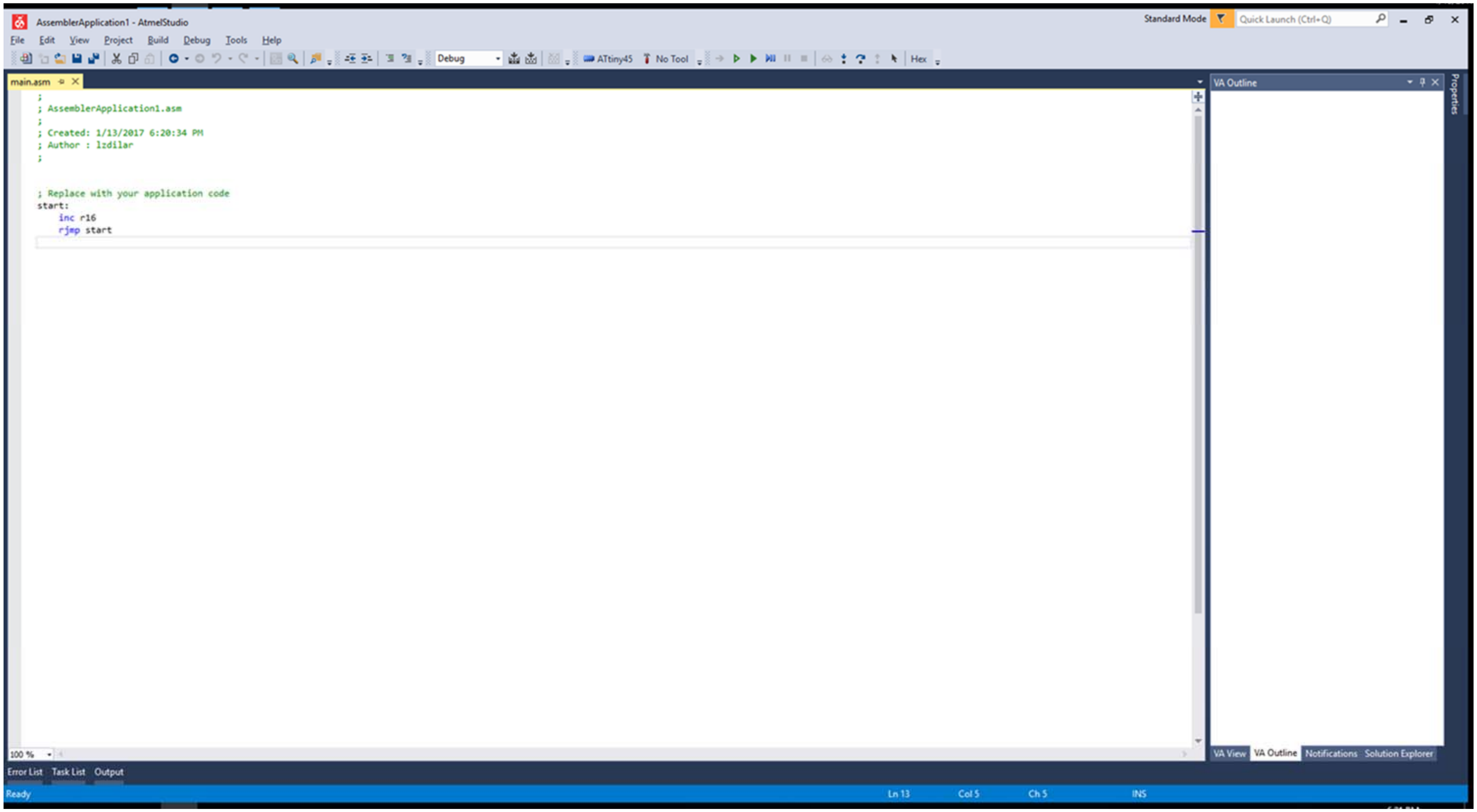
Datasheet (Summary)

Device Page

Supported Tools

- Atmel-ICE
- AVR Dragon
- AVRISP mkII
- AVR ONE!
- EDBG
- EDBG MSD
- JTAGICE3

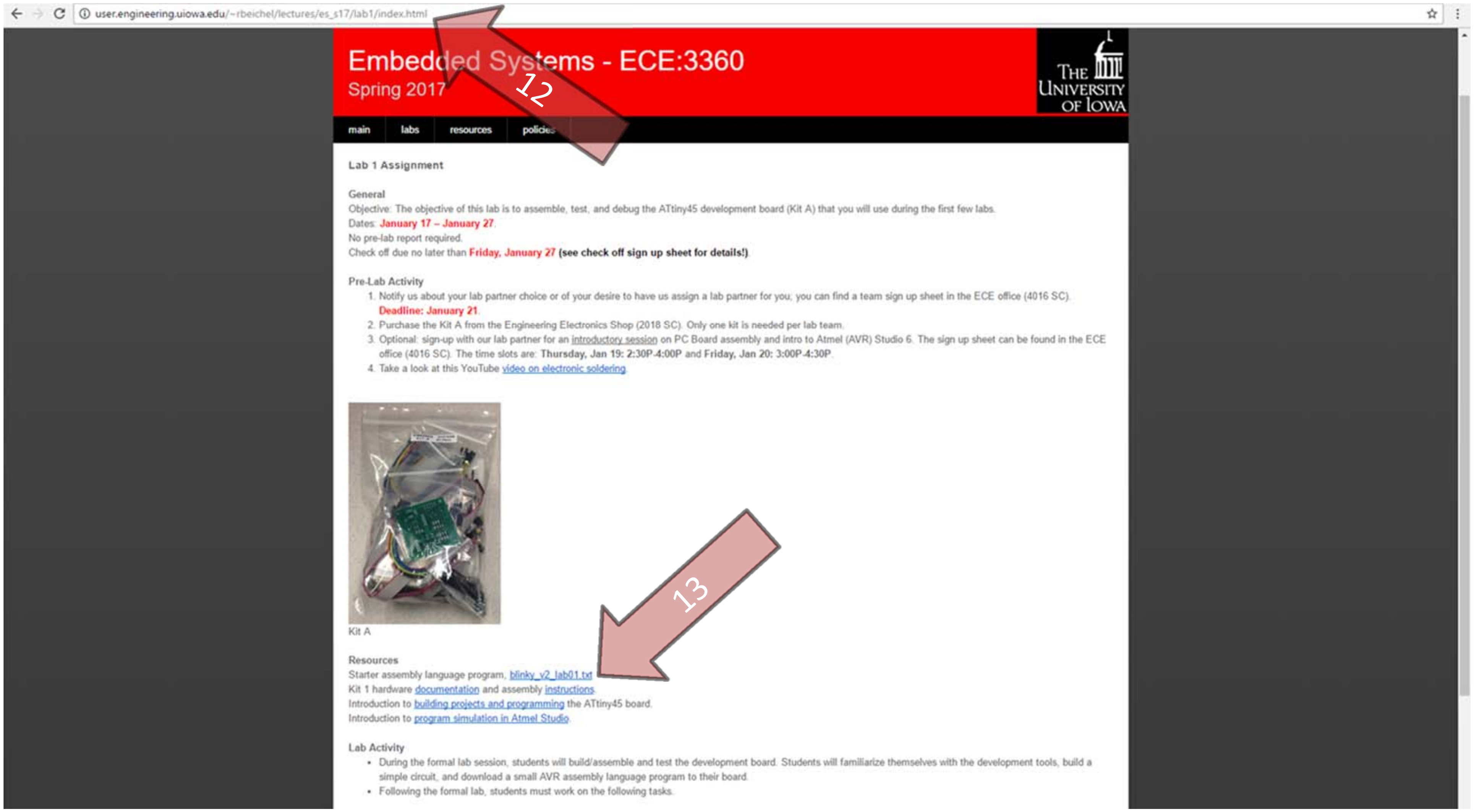
9. Select “ATtiny” from the drop down
10. Select “ATtiny45” from the list
11. Click “OK”


AssemblerApplication1 - AtmelStudio
File Edit View Project Build Debug Tools Help
Debug
ATtiny45
No Tool
Hex
main.asm
VA Outline
VA View VA Outline Notifications Solution Explorer
Error List Task List Output
Ready Ln 13 Col 5 Ch 5 INS

```
;
; AssemblerApplication1.asm
;
; Created: 1/13/2017 6:20:34 PM
; Author : lzdilar
;


; Replace with your application code
start:
    inc r16
    rjmp start
```

The main.asm file should appear with some default code


user.engineering.uiowa.edu/~rbeichel/lectures/es_s17/lab1/index.html
12
13
The University of Iowa
main
labs
resources
policies

Embedded Systems - ECE:3360

Spring 2017

Lab 1 Assignment

General

Objective: The objective of this lab is to assemble, test, and debug the ATtiny45 development board (Kit A) that you will use during the first few labs.
Dates: **January 17 – January 27**.
No pre-lab report required.
Check off due no later than **Friday, January 27** **(see check off sign up sheet for details!)**

Pre-Lab Activity

1. Notify us about your lab partner choice or of your desire to have us assign a lab partner for you; you can find a team sign up sheet in the ECE office (4016 SC). **Deadline: January 21**.
2. Purchase the Kit A from the Engineering Electronics Shop (2018 SC). Only one kit is needed per lab team.
3. Optional: sign-up with our lab partner for an introductory session on PC Board assembly and intro to Atmel (AVR) Studio 6. The sign up sheet can be found in the ECE office (4016 SC). The time slots are: **Thursday, Jan 19: 2:30P-4:00P** and **Friday, Jan 20: 3:00P-4:30P**.
4. Take a look at this YouTube video on electronic soldering.

Kit A

Resources

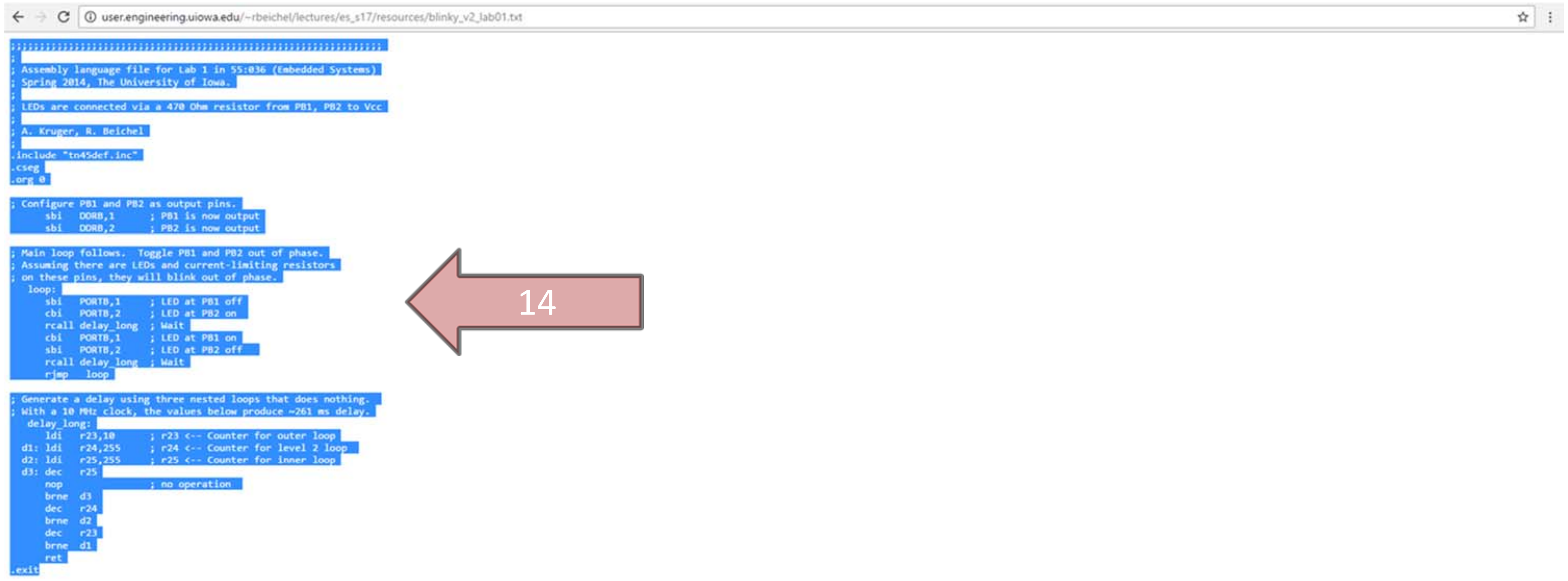
Starter assembly language program, blinky_v2_lab01.txt
Kit 1 hardware documentation and assembly instructions.
Introduction to building projects and programming the ATtiny45 board.
Introduction to program simulation in Atmel Studio.

Lab Activity

- During the formal lab session, students will build/assemble and test the development board. Students will familiarize themselves with the development tools, build a simple circuit, and download a small AVR assembly language program to their board.
- Following the formal lab, students must work on the following tasks.

12. Navigate to the class website for Lab 1

13. Click on the blinky.txt


user.engineering.uiowa.edu/~rbeichel/lectures/es_s17/resources/blinky_v2_lab01.txt
14

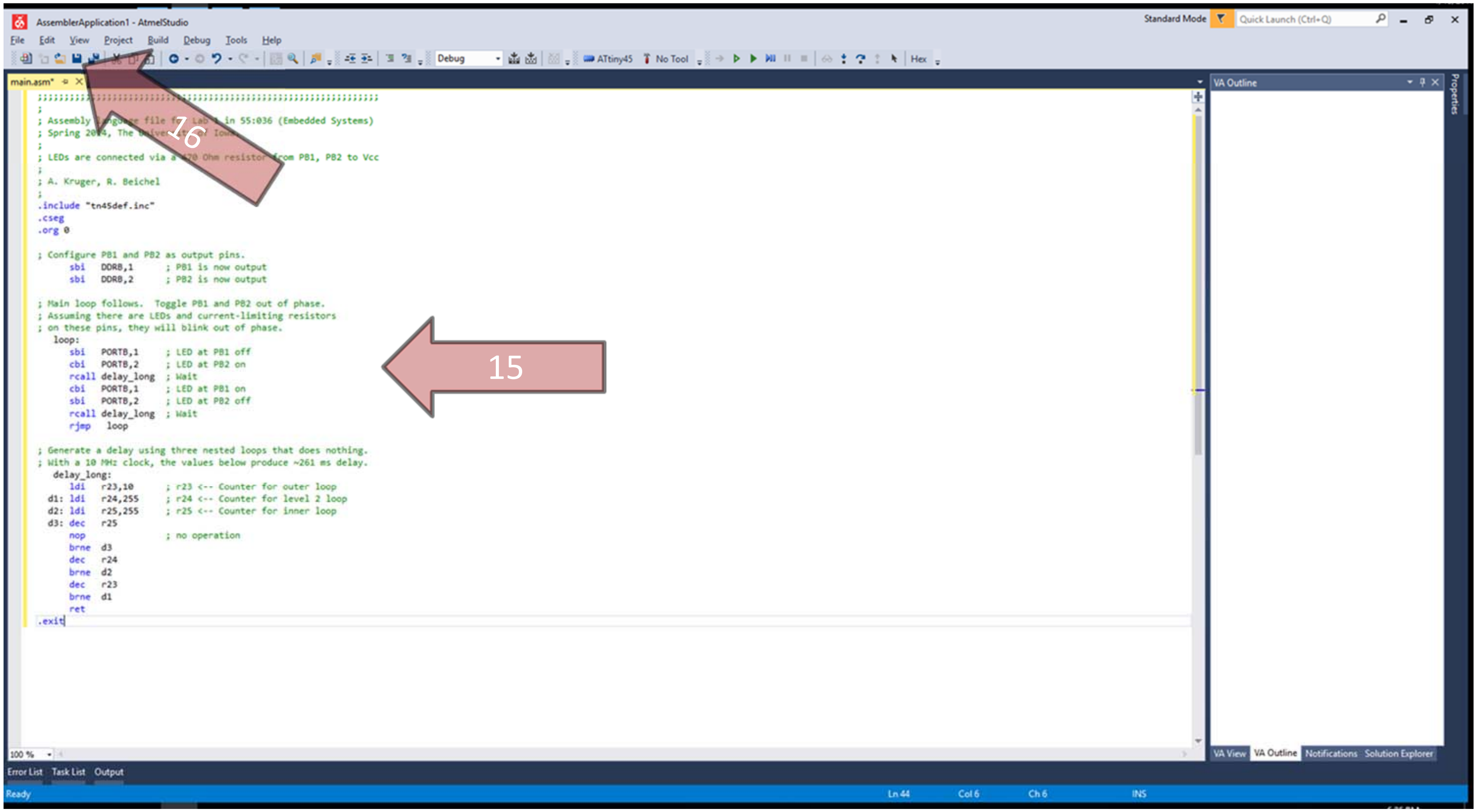
```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
; Assembly language file for Lab 1 in 55:036 (Embedded Systems)
; Spring 2014, The University of Iowa.
;
; LEDs are connected via a 470 Ohm resistor from PB1, PB2 to Vcc
;
; A. Kruger, R. Beichel
;
.include "tn45def.inc"
.cseg
.org 0

; Configure PB1 and PB2 as output pins.
      sbi   DDRB,1       ; PB1 is now output
      sbi   DDRB,2       ; PB2 is now output

; Main loop follows.  Toggle PB1 and PB2 out of phase.
; Assuming there are LEDs and current-limiting resistors
; on these pins, they will blink out of phase.
   loop:
      sbi   PORTB,1      ; LED at PB1 off
      cbi   PORTB,2      ; LED at PB2 on
      rcall delay_long   ; Wait
      cbi   PORTB,1      ; LED at PB1 on
      sbi   PORTB,2      ; LED at PB2 off
      rcall delay_long   ; Wait
      rjmp   loop

; Generate a delay using three nested loops that does nothing.
; With a 10 MHz clock, the values below produce ~261 ms delay.
   delay_long:
      ldi   r23,10       ; r23 <-- Counter for outer loop
  d1: ldi   r24,255      ; r24 <-- Counter for level 2 loop
  d2: ldi   r25,255      ; r25 <-- Counter for inner loop
  d3: dec   r25
      nop                ; no operation
      brne  d3
      dec   r24
      brne  d2
      dec   r23
      brne  d1
      ret
.exit
```

14. Copy all of the code


AssemblerApplication1 - AtmelStudio
File Edit View Project Build Debug Tools Help
Debug
ATtiny45
No Tool
main.asm*
16
15
VA Outline
Ready
Ln 44
Col 6
Ch 6
INS

```
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; A. Kruger, R. Beichel
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.org 0

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   loop:
      sbi   PORTB,1     ; LED at PB1 off
      cbi   PORTB,2     ; LED at PB2 on
      rcall delay_long  ; Wait
      cbi   PORTB,1     ; LED at PB1 on
      sbi   PORTB,2     ; LED at PB2 off
      rcall delay_long  ; Wait
      rjmp   loop

; Generate a delay using three nested loops that does nothing.
; With a 10 MHz clock, the values below produce ~261 ms delay.
   delay_long:
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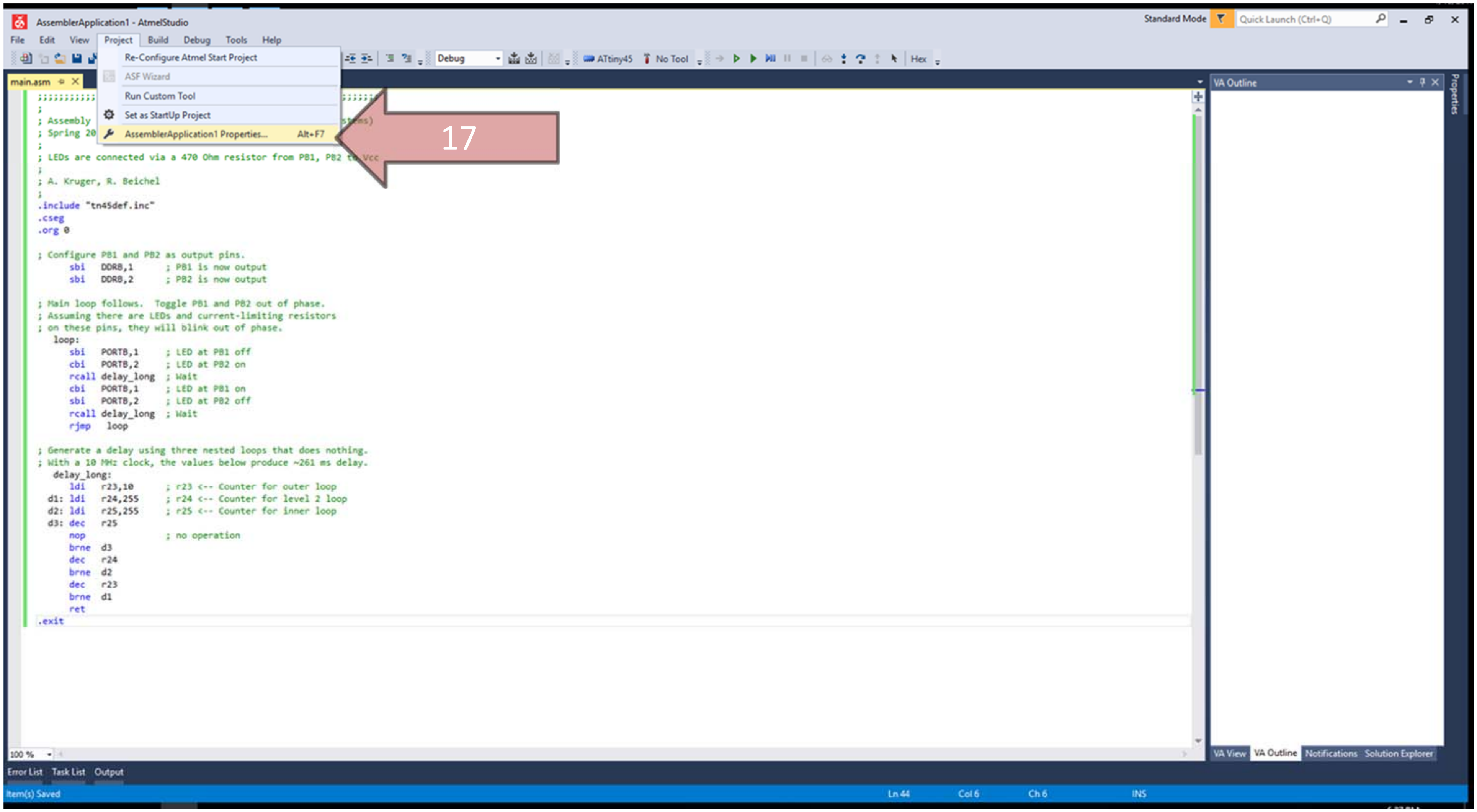
  d1: ldi   r24,255     ; r24 <-- Counter for level 2 loop
  d2: ldi   r25,255     ; r25 <-- Counter for inner loop
  d3: dec   r25
      nop               ; no operation
      brne  d3
      dec   r24
      brne  d2
      dec   r23
      brne  d1
      ret
.exit
```

15. Paste the code into main.asm

16. Save main.asm


AssemblerApplication1 - AtmelStudio
File Edit View Project Build Debug Tools Help
Re-Configure Atmel Start Project
ASF Wizard
Run Custom Tool
Set as StartUp Project
AssemblerApplication1 Properties... Alt+F7
Debug
ATtiny45
No Tool
Hex
main.asm
VA Outline
17
Standard Mode
Quick Launch (Ctrl+Q)
100 %
Error List Task List Output
VA View VA Outline Notifications Solution Explorer
Item(s) Saved
Ln 44 Col 6 Ch 6 INS

```
;;;;;;;;;;;
;
; Assembly
; Spring 20
;
; LEDs are connected via a 470 Ohm resistor from PB1, PB2 to Vcc
;
; A. Kruger, R. Beichel
;
.include "tn45def.inc"
.cseg
.org 0

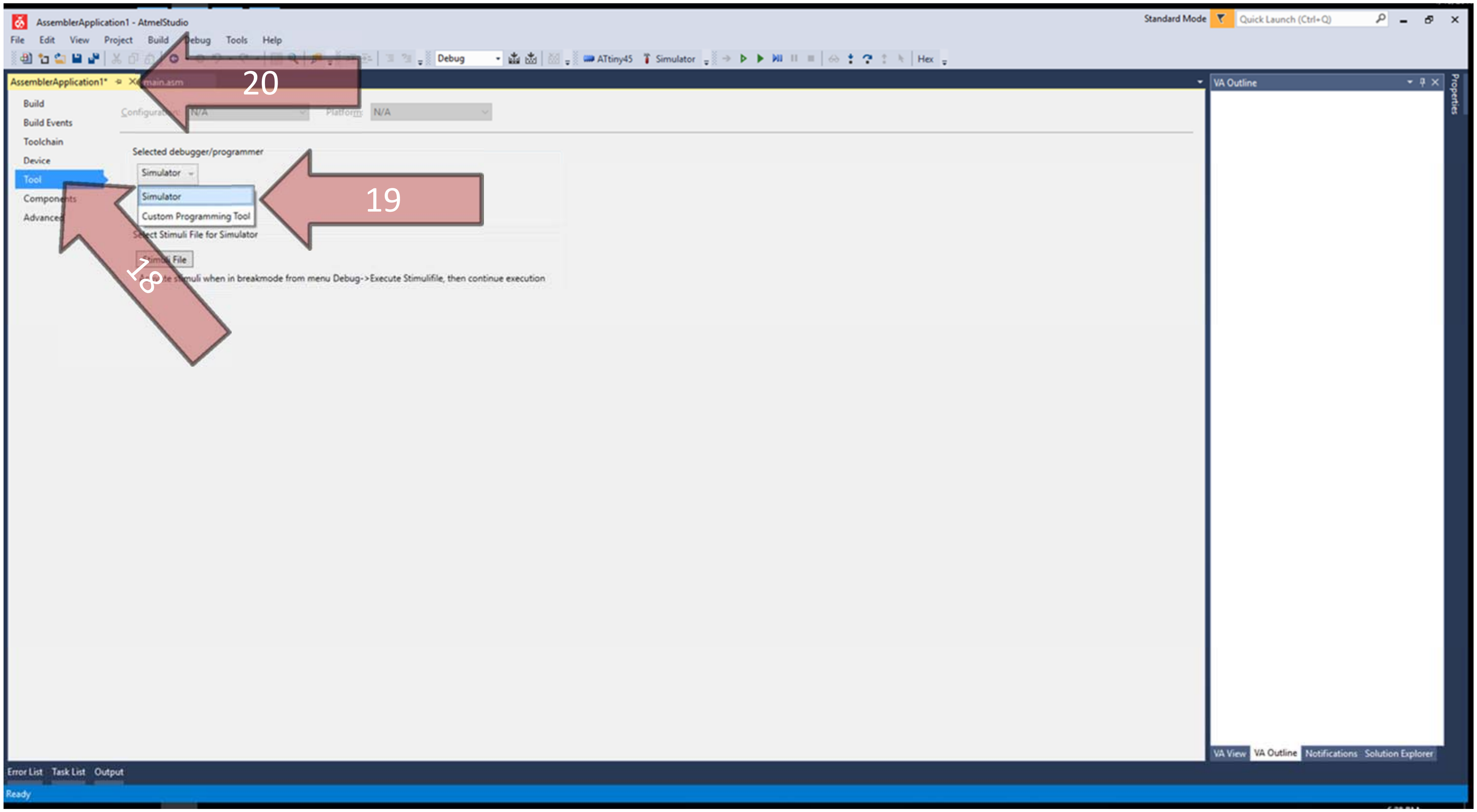
; Configure PB1 and PB2 as output pins.
      sbi   DDRB,1      ; PB1 is now output
      sbi   DDRB,2      ; PB2 is now output

; Main loop follows.  Toggle PB1 and PB2 out of phase.
; Assuming there are LEDs and current-limiting resistors
; on these pins, they will blink out of phase.
   loop:
      sbi   PORTB,1     ; LED at PB1 off
      cbi   PORTB,2     ; LED at PB2 on
      rcall delay_long  ; Wait
      cbi   PORTB,1     ; LED at PB1 on
      sbi   PORTB,2     ; LED at PB2 off
      rcall delay_long  ; Wait
      rjmp   loop

; Generate a delay using three nested loops that does nothing.
; With a 10 MHz clock, the values below produce ~261 ms delay.
   delay_long:
      ldi   r23,10      ; r23 <-- Counter for outer loop
  d1: ldi   r24,255     ; r24 <-- Counter for level 2 loop
  d2: ldi   r25,255     ; r25 <-- Counter for inner loop
  d3: dec   r25
      nop               ; no operation
      brne  d3
      dec   r24
      brne  d2
      dec   r23
      brne  d1
      ret
.exit
```

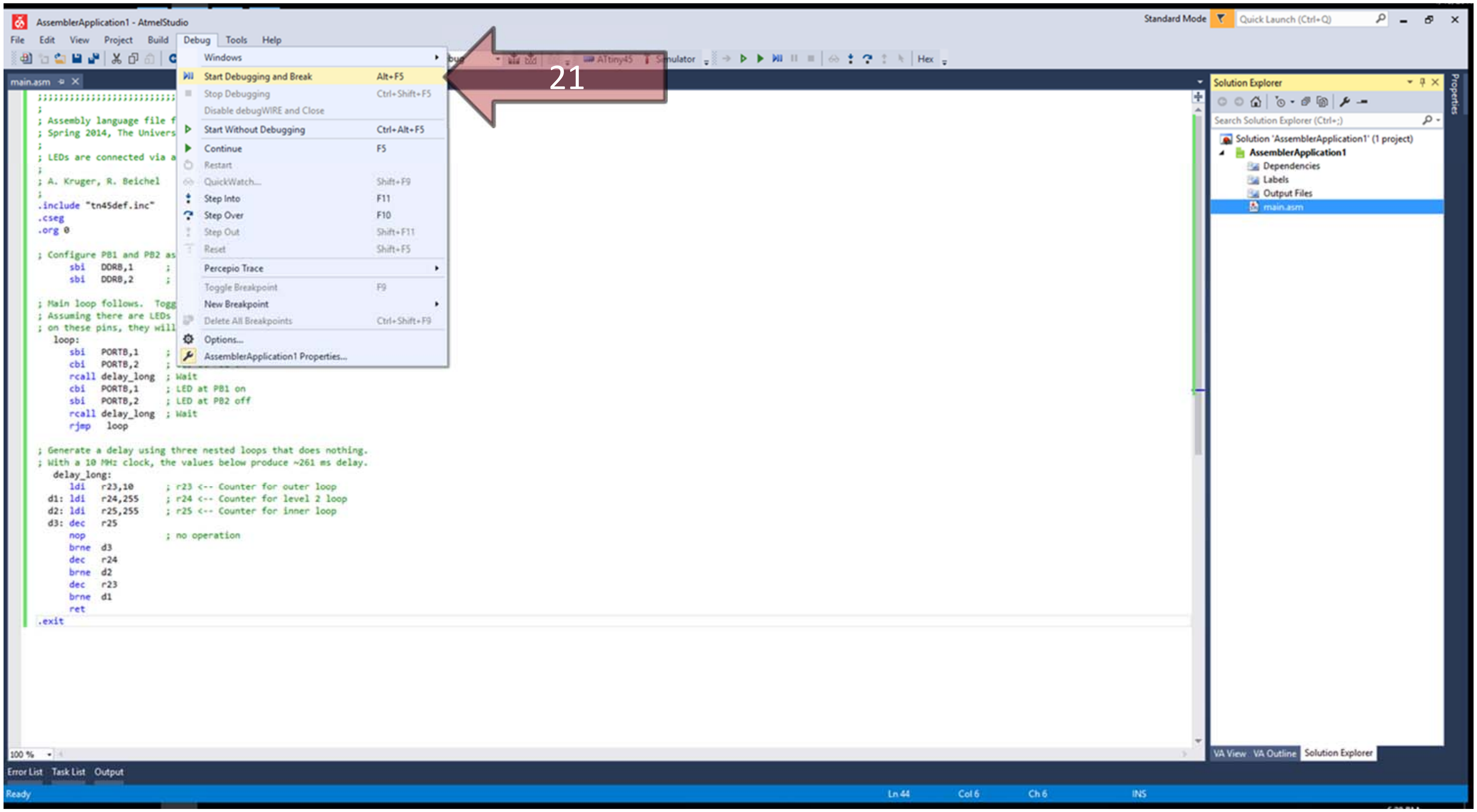
Note: Steps 17 to 20 only need to be done the first time you debug

17. Navigate to “Project” -> “<ProjectName> Properties…” and click it



Selected debugger/programmer: Simulator

18. Select “Tool”
19. Select “Simulator” from the drop down
20. Close the window



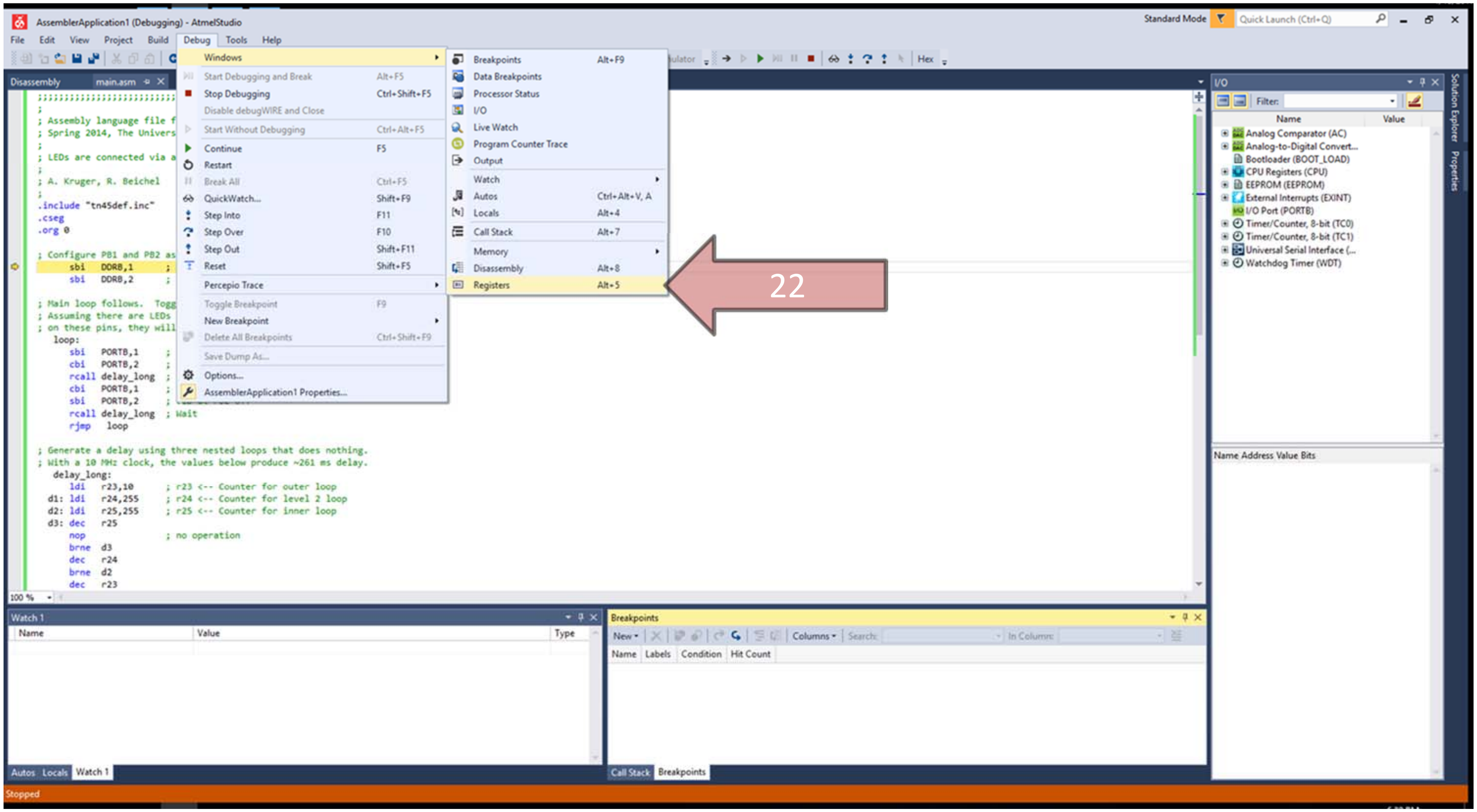
```
;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
; Assembly language file f
; Spring 2014, The Univers
;
; LEDs are connected via a
;
; A. Kruger, R. Beichel
;
.include "tn45def.inc"
.cseg
.org 0

; Configure PB1 and PB2 as
      sbi   DDRB,1      ;
      sbi   DDRB,2      ;

; Main loop follows.  Togg
; Assuming there are LEDs
; on these pins, they will
   loop:
      sbi   PORTB,1     ;
      cbi   PORTB,2     ;
      rcall delay_long  ; Wait
      cbi   PORTB,1     ; LED at PB1 on
      sbi   PORTB,2     ; LED at PB2 off
      rcall delay_long  ; Wait
      rjmp   loop

; Generate a delay using three nested loops that does nothing.
; With a 10 MHz clock, the values below produce ~261 ms delay.
   delay_long:
      ldi   r23,10      ; r23 <-- Counter for outer loop
  d1: ldi   r24,255     ; r24 <-- Counter for level 2 loop
  d2: ldi   r25,255     ; r25 <-- Counter for inner loop
  d3: dec   r25
      nop               ; no operation
      brne  d3
      dec   r24
      brne  d2
      dec   r23
      brne  d1
      ret
.exit
```

21. Navigate to
"Debug" -> "Start Debugging and Break" and click it



```
;;;;;;;;;;;;;;;;;;;;;;;;;;
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; Assembly language file f
; Spring 2014, The Univers
;
; LEDs are connected via a
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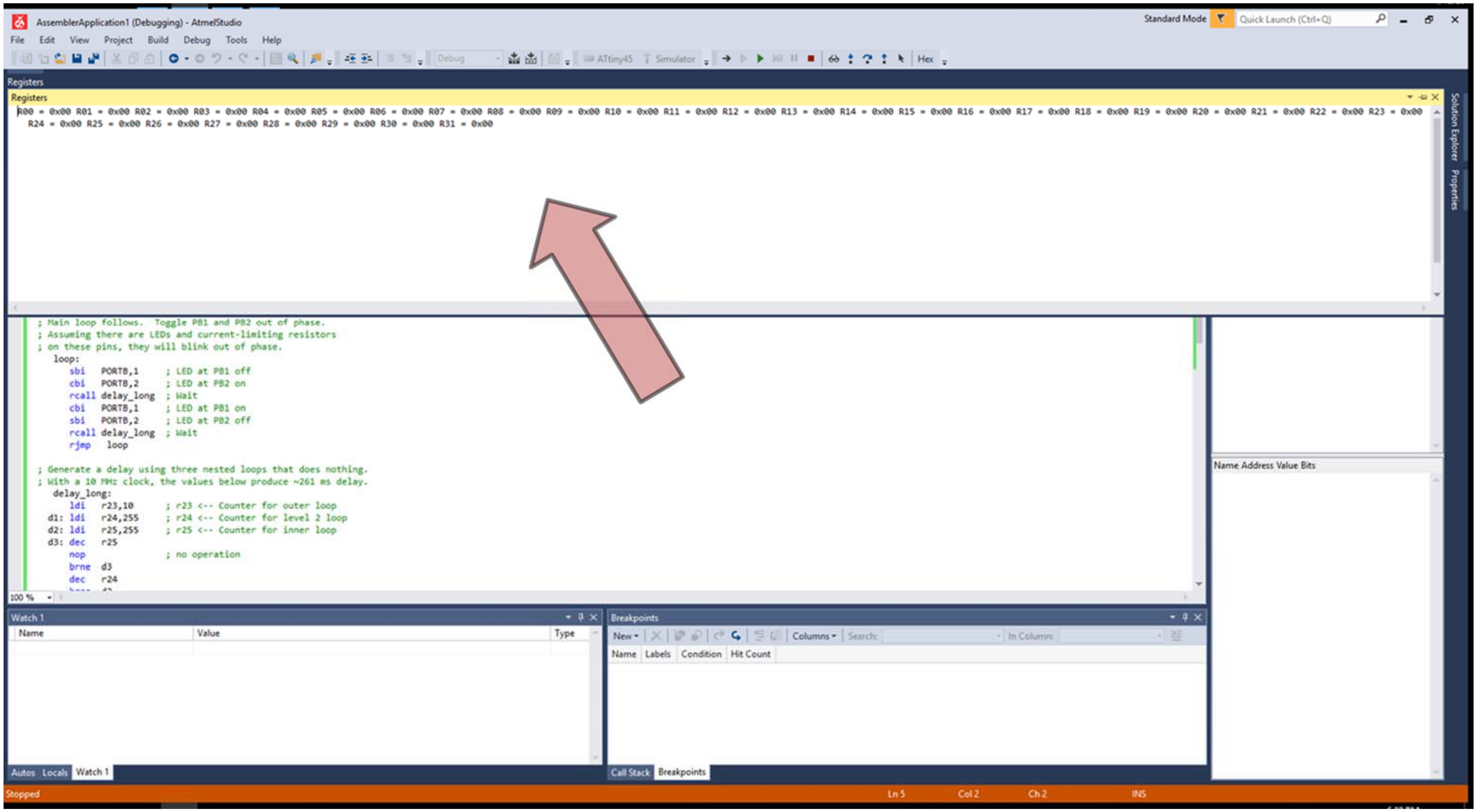
; A. Kruger, R. Beichel
;
.include "tn45def.inc"
.cseg
.org 0

; Configure PB1 and PB2 as
       sbi    DDRB,1        ;
       sbi    DDRB,2        ;

; Main loop follows.  Togg
; Assuming there are LEDs
; on these pins, they will
  loop:
       sbi    PORTB,1       ;
       cbi    PORTB,2       ;
       rcall  delay_long    ;
       cbi    PORTB,1       ;
       sbi    PORTB,2       ;
       rcall  delay_long    ; Wait
       rjmp   loop

; Generate a delay using three nested loops that does nothing.
; With a 10 MHz clock, the values below produce ~261 ms delay.
  delay_long:
       ldi    r23,10        ; r23 <-- Counter for outer loop
   d1: ldi    r24,255       ; r24 <-- Counter for level 2 loop
   d2: ldi    r25,255       ; r25 <-- Counter for inner loop
   d3: dec    r25
       nop                  ; no operation
       brne   d3
       dec    r24
       brne   d2
       dec    r23
```

22. Navigate to
"Debug" -> "Windows" -> "Registers" and click it to show the register values


AssemblerApplication1 (Debugging) - AtmelStudio
File Edit View Project Build Debug Tools Help
Debug
ATtiny45
Simulator
Hex
Registers
Watch 1
Breakpoints
Stopped
Ln 5
Col 2
Ch 2
INS

```
R00 = 0x00 R01 = 0x00 R02 = 0x00 R03 = 0x00 R04 = 0x00 R05 = 0x00 R06 = 0x00 R07 = 0x00 R08 = 0x00 R09 = 0x00 R10 = 0x00 R11 = 0x00 R12 = 0x00 R13 = 0x00 R14 = 0x00 R15 = 0x00 R16 = 0x00 R17 = 0x00 R18 = 0x00 R19 = 0x00 R20 = 0x00 R21 = 0x00 R22 = 0x00 R23 = 0x00
  R24 = 0x00 R25 = 0x00 R26 = 0x00 R27 = 0x00 R28 = 0x00 R29 = 0x00 R30 = 0x00 R31 = 0x00
```

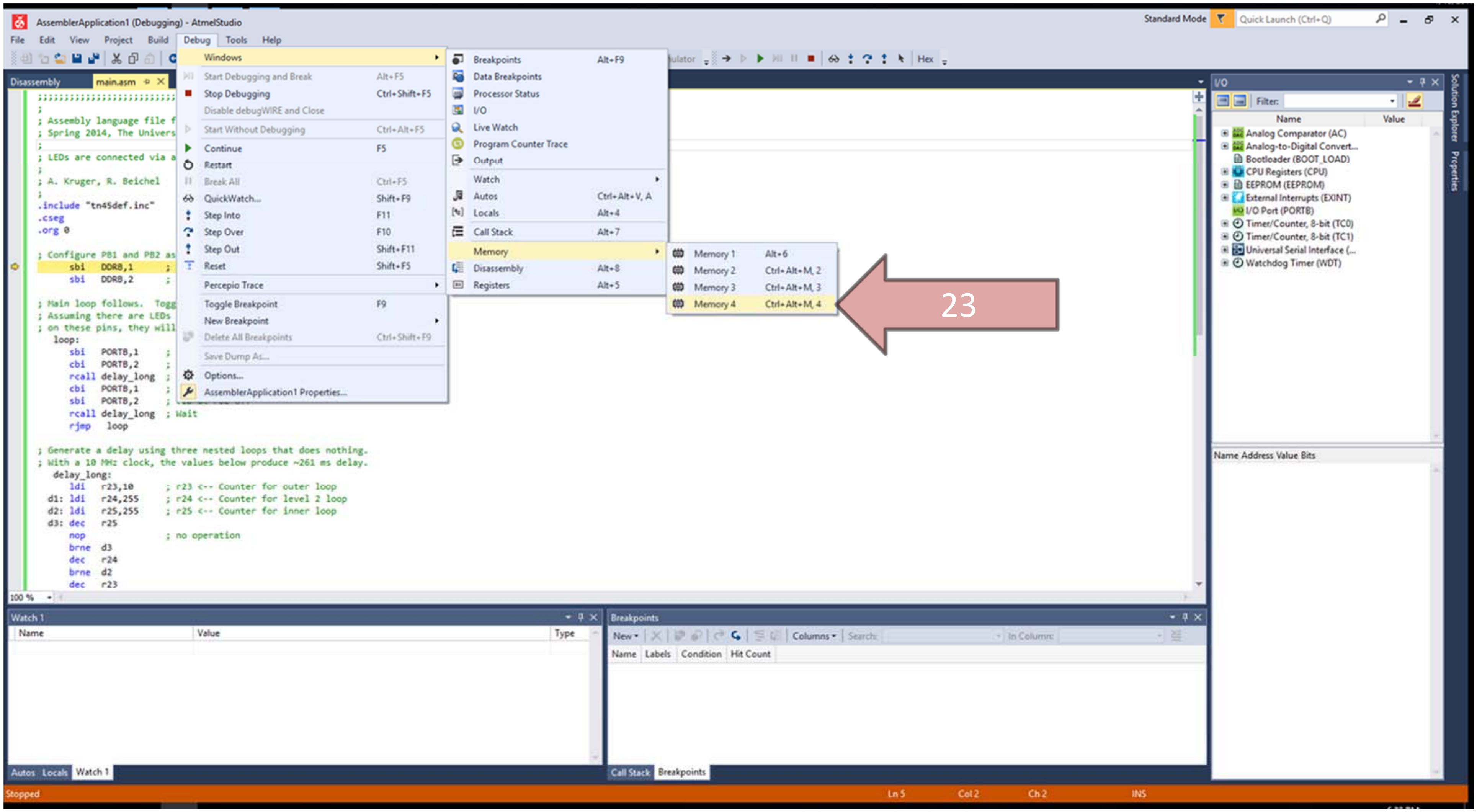
```
; Main loop follows.  Toggle PB1 and PB2 out of phase.
; Assuming there are LEDs and current-limiting resistors
; on these pins, they will blink out of phase.
  loop:
     sbi   PORTB,1     ; LED at PB1 off
     cbi   PORTB,2     ; LED at PB2 on
     rcall delay_long  ; Wait
     cbi   PORTB,1     ; LED at PB1 on
     sbi   PORTB,2     ; LED at PB2 off
     rcall delay_long  ; Wait
     rjmp   loop

; Generate a delay using three nested loops that does nothing.
; With a 10 MHz clock, the values below produce ~261 ms delay.
  delay_long:
     ldi   r23,10      ; r23 <-- Counter for outer loop
 d1: ldi   r24,255     ; r24 <-- Counter for level 2 loop
 d2: ldi   r25,255     ; r25 <-- Counter for inner loop
 d3: dec   r25
     nop               ; no operation
     brne  d3
     dec   r24
```

Name	Value	Type

Name	Labels	Condition	Hit Count

The list of registers and their values



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.include "tn45def.inc"
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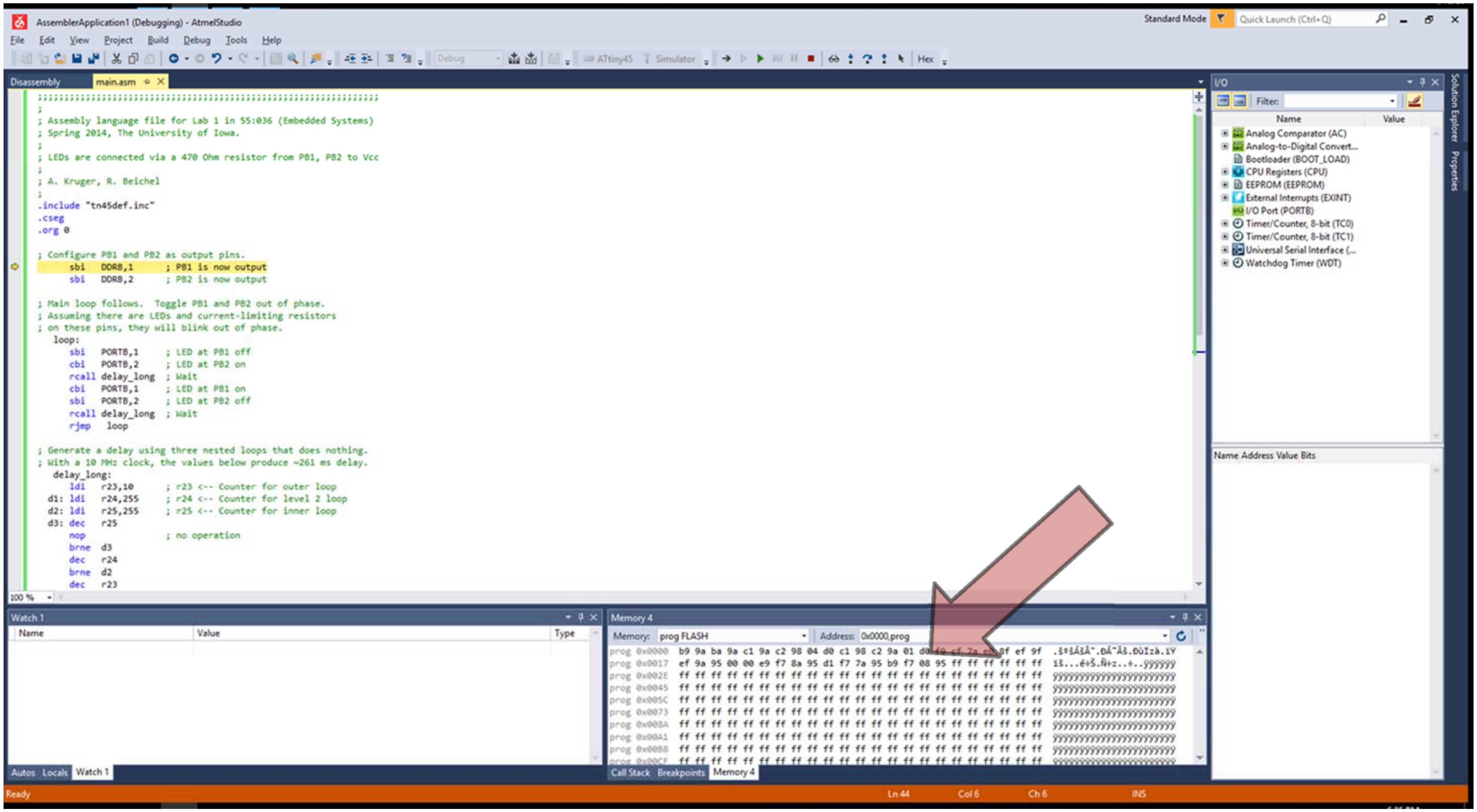
; Configure PB1 and PB2 as
        sbi   DDRB,1      ;
        sbi   DDRB,2      ;

; Main loop follows.  Togg
; Assuming there are LEDs
; on these pins, they will
    loop:
        sbi   PORTB,1     ;
        cbi   PORTB,2     ;
        rcall delay_long  ;
        cbi   PORTB,1     ;
        sbi   PORTB,2     ;
        rcall delay_long  ; Wait
        rjmp   loop

; Generate a delay using three nested loops that does nothing.
; With a 10 MHz clock, the values below produce ~261 ms delay.
    delay_long:
        ldi   r23,10      ; r23 <-- Counter for outer loop
    d1: ldi   r24,255     ; r24 <-- Counter for level 2 loop
    d2: ldi   r25,255     ; r25 <-- Counter for inner loop
    d3: dec   r25
        nop               ; no operation
        brne  d3
        dec   r24
        brne  d2
        dec   r23
```

23. Navigate to
"Debug" -> "Windows" -> "Memory" -> "Memory 4" and click it to show the memory values


AssemblerApplication1 (Debugging) - AtmelStudio
File Edit View Project Build Debug Tools Help
Disassembly
main.asm
I/O
Analog Comparator (AC)
Analog-to-Digital Convert...
Bootloader (BOOT_LOAD)
CPU Registers (CPU)
EEPROM (EEPROM)
External Interrupts (EXINT)
I/O Port (PORTB)
Timer/Counter, 8-bit (TC0)
Timer/Counter, 8-bit (TC1)
Universal Serial Interface (...
Watchdog Timer (WDT)
Watch 1
Memory 4
Ready
Ln 44 Col 6 Ch 6 INS

```
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; Assembly language file for Lab 1 in 55:036 (Embedded Systems)
; Spring 2014, The University of Iowa.
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; LEDs are connected via a 470 Ohm resistor from PB1, PB2 to Vcc
;
; A. Kruger, R. Beichel
;
.include "tn45def.inc"
.cseg
.org 0

; Configure PB1 and PB2 as output pins.
      sbi   DDRB,1      ; PB1 is now output
      sbi   DDRB,2      ; PB2 is now output

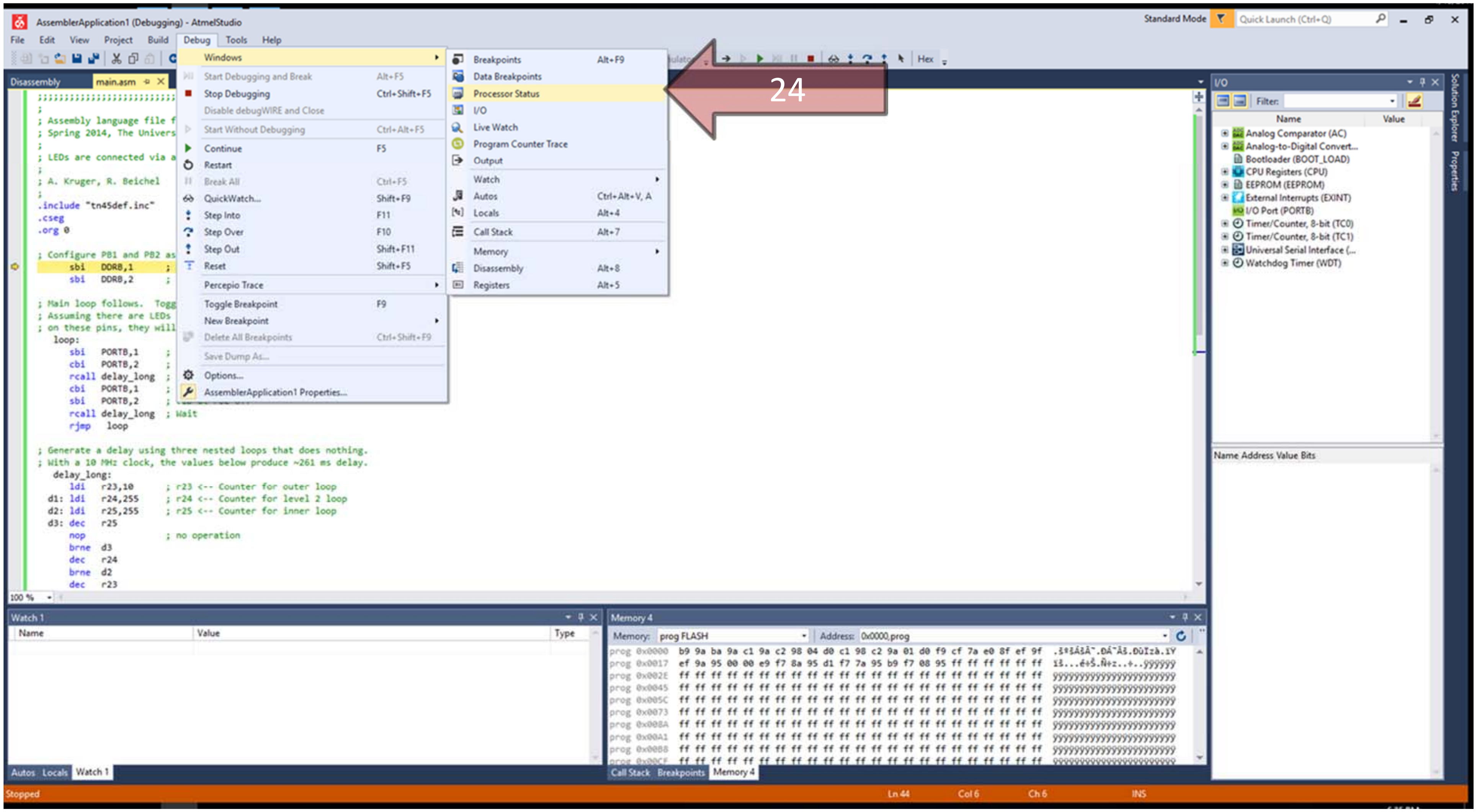
; Main loop follows.  Toggle PB1 and PB2 out of phase.
; Assuming there are LEDs and current-limiting resistors
; on these pins, they will blink out of phase.
   loop:
      sbi   PORTB,1     ; LED at PB1 off
      cbi   PORTB,2     ; LED at PB2 on
      rcall delay_long  ; Wait
      cbi   PORTB,1     ; LED at PB1 on
      sbi   PORTB,2     ; LED at PB2 off
      rcall delay_long  ; Wait
      rjmp   loop

; Generate a delay using three nested loops that does nothing.
; With a 10 MHz clock, the values below produce ~261 ms delay.
   delay_long:
      ldi   r23,10      ; r23 <-- Counter for outer loop
  d1: ldi   r24,255     ; r24 <-- Counter for level 2 loop
  d2: ldi   r25,255     ; r25 <-- Counter for inner loop
  d3: dec   r25
      nop               ; no operation
      brne  d3
      dec   r24
      brne  d2
      dec   r23
```

Memory: prog FLASH   Address: 0x0000,prog

```
prog 0x0000  b9 9a ba 9a c1 9a c2 98 04 d0 c1 98 c2 9a 01 d0 f9 cf 7a e0 8f ef 9f  .¹š¹šÁšÂ˜.ÐÁ˜Âš.ÐùÏzà.ïŸ
prog 0x0017  ef 9a 95 00 00 e9 f7 8a 95 d1 f7 7a 95 b9 f7 08 95 ff ff ff ff ff ff  ïš...é÷Š.Ñ÷z..÷..ÿÿÿÿÿÿ
prog 0x002E  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x0045  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x005C  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x0073  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x008A  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x00A1  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x00B8  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x00CF  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
```

The memory locations and their values



```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
; Assembly language file f
; Spring 2014, The Univers
;
; LEDs are connected via a
;
; A. Kruger, R. Beichel
;
.include "tn45def.inc"
.cseg
.org 0

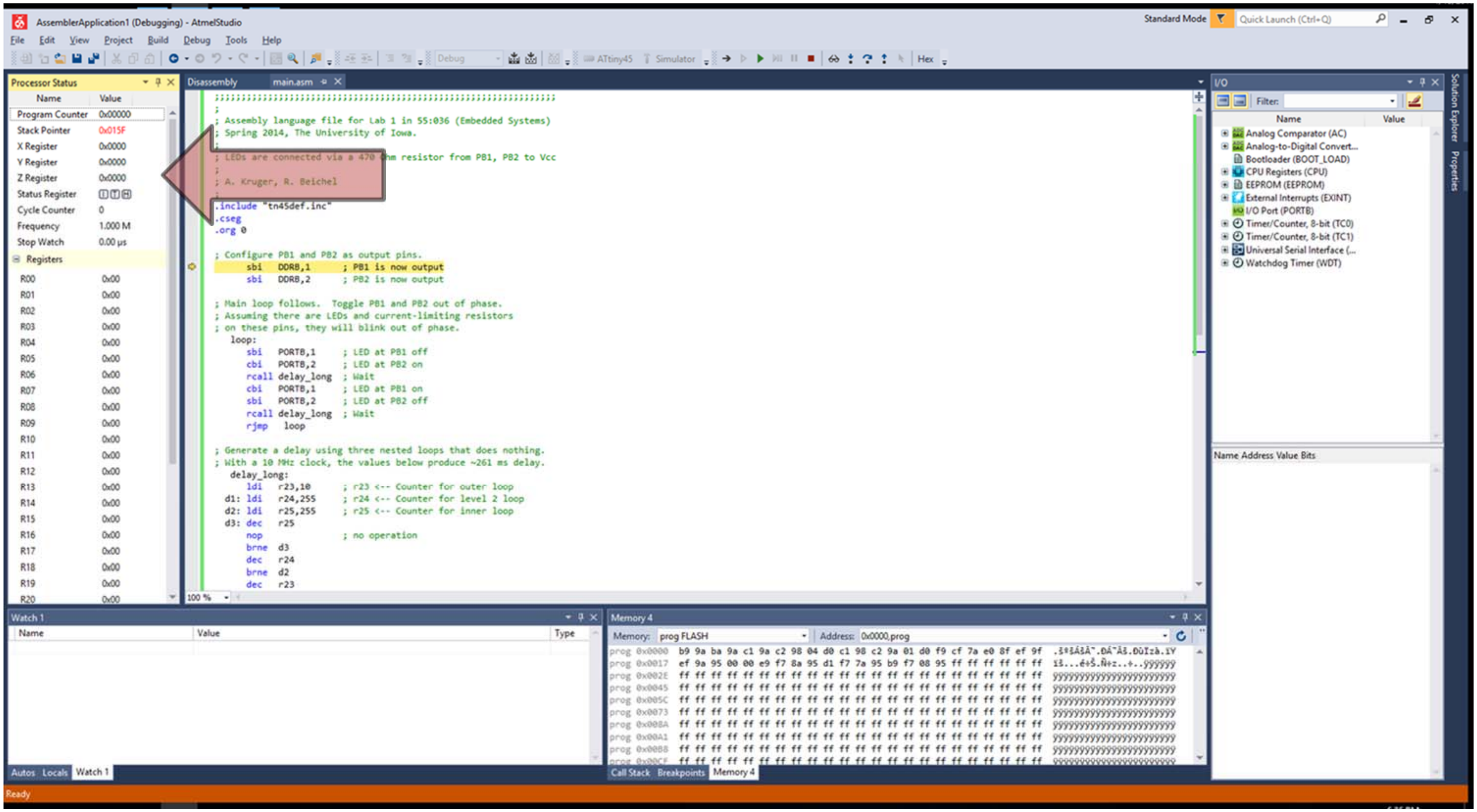
; Configure PB1 and PB2 as
        sbi   DDRB,1       ;
        sbi   DDRB,2       ;

; Main loop follows.  Togg
; Assuming there are LEDs
; on these pins, they will
    loop:
        sbi   PORTB,1      ;
        cbi   PORTB,2      ;
        rcall delay_long   ;
        cbi   PORTB,1      ;
        sbi   PORTB,2      ;
        rcall delay_long   ; Wait
        rjmp   loop

; Generate a delay using three nested loops that does nothing.
; With a 10 MHz clock, the values below produce ~261 ms delay.
    delay_long:
        ldi   r23,10       ; r23 <-- Counter for outer loop
    d1: ldi   r24,255      ; r24 <-- Counter for level 2 loop
    d2: ldi   r25,255      ; r25 <-- Counter for inner loop
    d3: dec   r25
        nop                ; no operation
        brne  d3
        dec   r24
        brne  d2
        dec   r23
```

```
prog 0x0000  b9 9a ba 9a c1 9a c2 98 04 d0 c1 98 c2 9a 01 d0 f9 cf 7a e0 8f ef 9f  .¹š¹šÁšÂ˜.ÐÁ˜Âš.Ðùϲzà.ïŸ
prog 0x0017  ef 9a 95 00 00 e9 f7 8a 95 d1 f7 7a 95 b9 f7 08 95 ff ff ff ff ff ff  ïš•..é÷Š•Ñ÷z•¹÷.•ÿÿÿÿÿÿ
prog 0x002E  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x0045  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x005C  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x0073  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x008A  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x00A1  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x00B8  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x00CF  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
```

24. Navigate to “Debug” -> “Windows” -> “Processor Status” and click it to show the values of the stack pointer, status register, cycle counter, and more



Name	Value
Program Counter	0x00000
Stack Pointer	0x015F
X Register	0x0000
Y Register	0x0000
Z Register	0x0000
Status Register	
Cycle Counter	0
Frequency	1.000 M
Stop Watch	0.00 µs
Registers	
R00	0x00
R01	0x00
R02	0x00
R03	0x00
R04	0x00
R05	0x00
R06	0x00
R07	0x00
R08	0x00
R09	0x00
R10	0x00
R11	0x00
R12	0x00
R13	0x00
R14	0x00
R15	0x00
R16	0x00
R17	0x00
R18	0x00
R19	0x00
R20	0x00

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
; Assembly language file for Lab 1 in 55:036 (Embedded Systems)
; Spring 2014, The University of Iowa.
;
; LEDs are connected via a 470 Ohm resistor from PB1, PB2 to Vcc
;
; A. Kruger, R. Beichel
;
.include "tn45def.inc"
.cseg
.org 0

; Configure PB1 and PB2 as output pins.
      sbi   DDRB,1      ; PB1 is now output
      sbi   DDRB,2      ; PB2 is now output

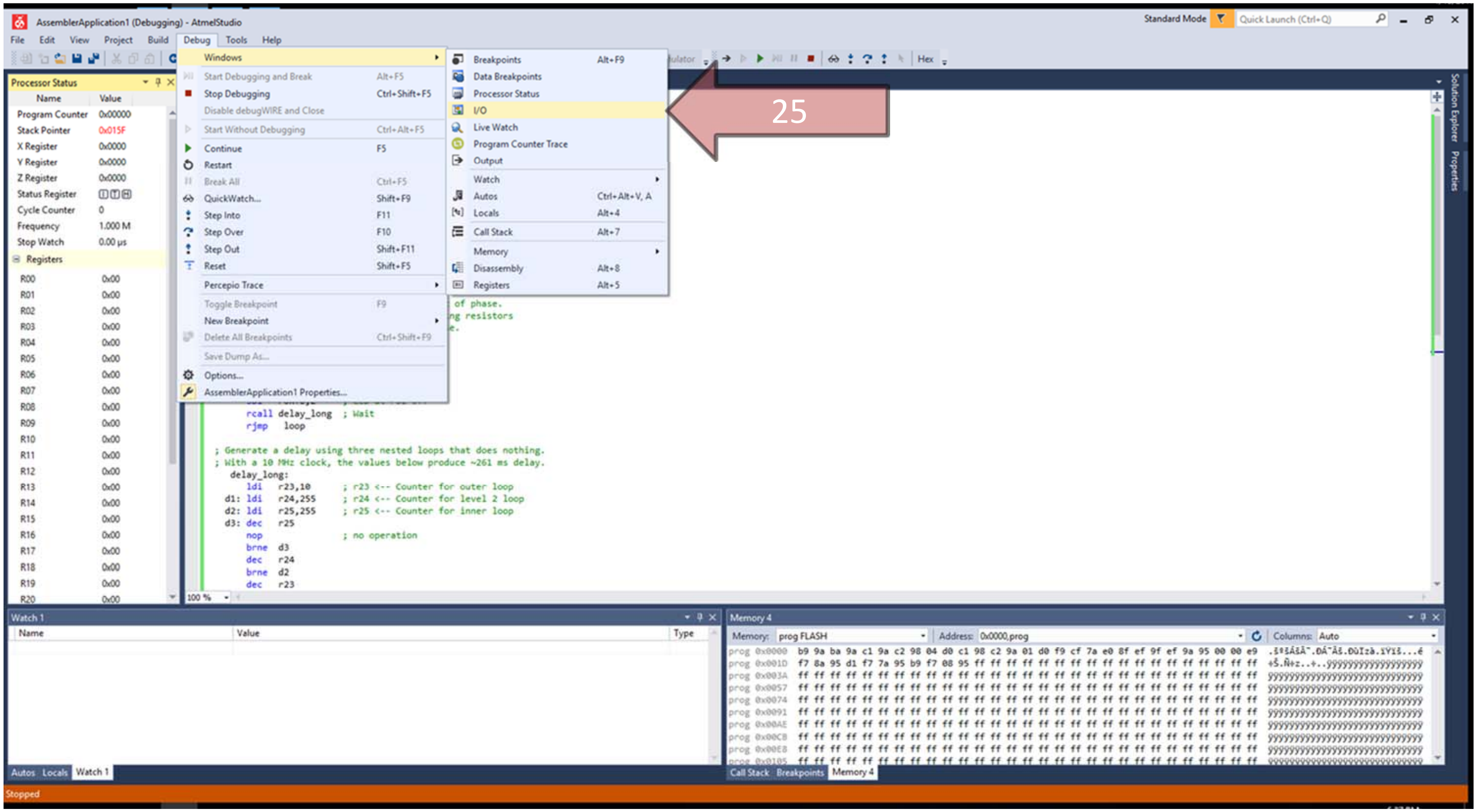
; Main loop follows.  Toggle PB1 and PB2 out of phase.
; Assuming there are LEDs and current-limiting resistors
; on these pins, they will blink out of phase.
   loop:
      sbi   PORTB,1     ; LED at PB1 off
      cbi   PORTB,2     ; LED at PB2 on
      rcall delay_long  ; Wait
      cbi   PORTB,1     ; LED at PB1 on
      sbi   PORTB,2     ; LED at PB2 off
      rcall delay_long  ; Wait
      rjmp   loop

; Generate a delay using three nested loops that does nothing.
; With a 10 MHz clock, the values below produce ~261 ms delay.
   delay_long:
      ldi   r23,10      ; r23 <-- Counter for outer loop
  d1: ldi   r24,255     ; r24 <-- Counter for level 2 loop
  d2: ldi   r25,255     ; r25 <-- Counter for inner loop
  d3: dec   r25
      nop               ; no operation
      brne  d3
      dec   r24
      brne  d2
      dec   r23
```

Memory: prog FLASH   Address: 0x0000,prog

```
prog 0x0000  b9 9a ba 9a c1 9a c2 98 04 d0 c1 98 c2 9a 01 d0 f9 cf 7a e0 8f ef 9f  .¹šºšÁšÂ˜.ÐÁ˜Âš.ÐùÏzà.ïŸ
prog 0x0017  ef 9a 95 00 00 e9 f7 8a 95 d1 f7 7a 95 b9 f7 08 95 ff ff ff ff ff ff  ïš•..é÷Š•Ñ÷z•¹÷.•ÿÿÿÿÿÿ
prog 0x002E  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x0045  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x005C  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x0073  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x008A  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x00A1  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x00B8  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x00CF  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
```

The processor status



Processor Status

Name	Value
Program Counter	0x00000
Stack Pointer	0x015F
X Register	0x0000
Y Register	0x0000
Z Register	0x0000
Status Register	
Cycle Counter	0
Frequency	1.000 M
Stop Watch	0.00 µs
Registers	
R00	0x00
R01	0x00
R02	0x00
R03	0x00
R04	0x00
R05	0x00
R06	0x00
R07	0x00
R08	0x00
R09	0x00
R10	0x00
R11	0x00
R12	0x00
R13	0x00
R14	0x00
R15	0x00
R16	0x00
R17	0x00
R18	0x00
R19	0x00
R20	0x00

```
                                    of phase.
                                  ng resistors
                                  e.

        rcall delay_long  ; Wait
        rjmp   loop

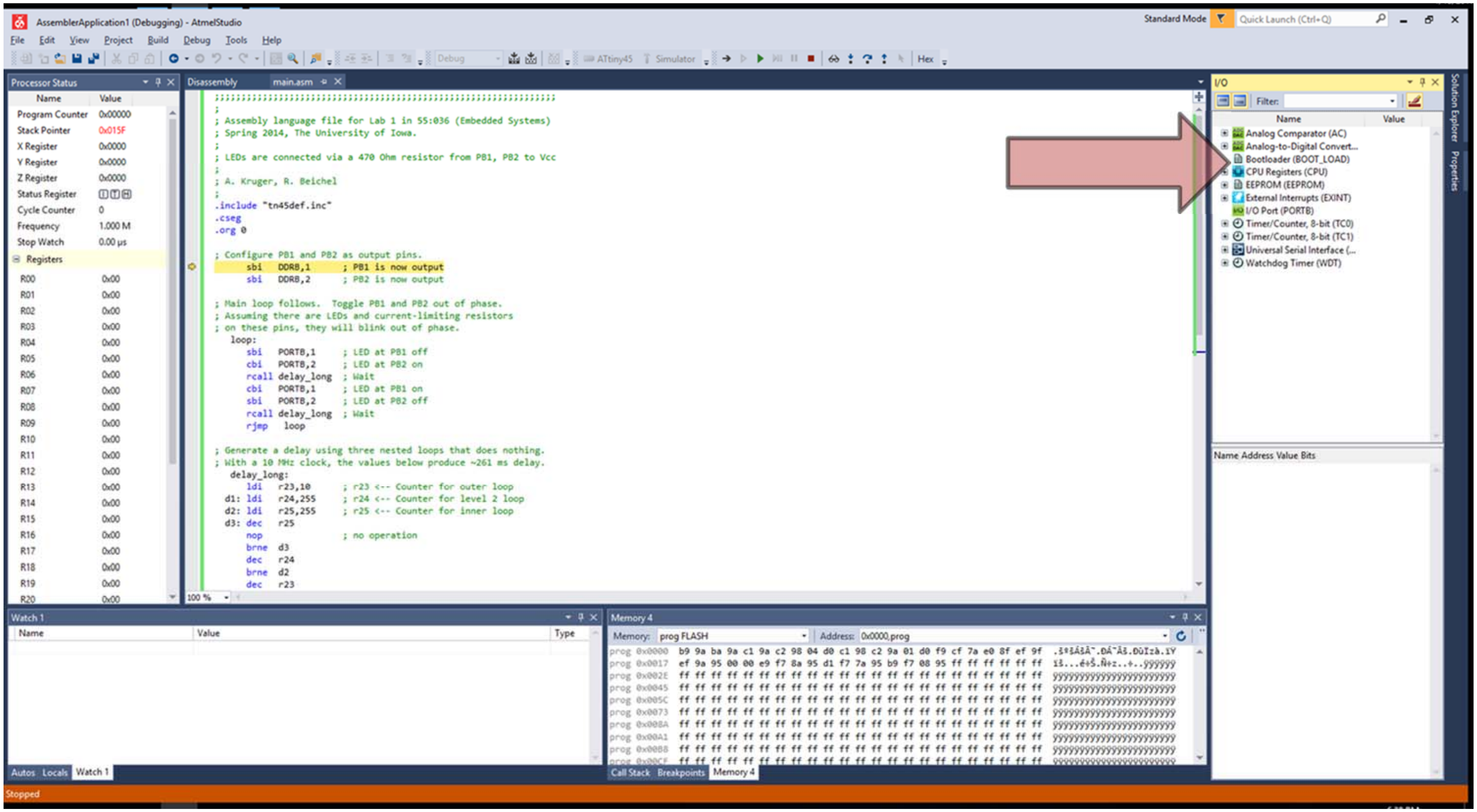
  ; Generate a delay using three nested loops that does nothing.
  ; With a 10 MHz clock, the values below produce ~261 ms delay.
     delay_long:
        ldi    r23,10       ; r23 <-- Counter for outer loop
    d1: ldi    r24,255      ; r24 <-- Counter for level 2 loop
    d2: ldi    r25,255      ; r25 <-- Counter for inner loop
    d3: dec    r25
        nop                 ; no operation
        brne   d3
        dec    r24
        brne   d2
        dec    r23
```

Name	Value	Type

Memory 4 — Memory: prog FLASH — Address: 0x0000,prog — Columns: Auto

```
prog 0x0000  b9 9a ba 9a c1 9a c2 98 04 d0 c1 98 c2 9a 01 d0 f9 cf 7a e0 8f ef 9f ef 9a 95 00 00 e9
prog 0x001D  f7 8a 95 d1 f7 7a 95 b9 f7 08 95 ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x003A  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x0057  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x0074  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x0091  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x00AE  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x00CB  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x00E8  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x0105  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
```

25. Navigate to “Debug” -> “Windows” -> “I/O” and click it to simulate I/O



Name	Value
Program Counter	0x00000
Stack Pointer	0x015F
X Register	0x0000
Y Register	0x0000
Z Register	0x0000
Status Register	I T H
Cycle Counter	0
Frequency	1.000 M
Stop Watch	0.00 µs
Registers	
R00	0x00
R01	0x00
R02	0x00
R03	0x00
R04	0x00
R05	0x00
R06	0x00
R07	0x00
R08	0x00
R09	0x00
R10	0x00
R11	0x00
R12	0x00
R13	0x00
R14	0x00
R15	0x00
R16	0x00
R17	0x00
R18	0x00
R19	0x00
R20	0x00

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
; Assembly language file for Lab 1 in 55:036 (Embedded Systems)
; Spring 2014, The University of Iowa.
;
; LEDs are connected via a 470 Ohm resistor from PB1, PB2 to Vcc
;
; A. Kruger, R. Beichel
;
.include "tn45def.inc"
.cseg
.org 0

; Configure PB1 and PB2 as output pins.
      sbi   DDRB,1      ; PB1 is now output
      sbi   DDRB,2      ; PB2 is now output

; Main loop follows.  Toggle PB1 and PB2 out of phase.
; Assuming there are LEDs and current-limiting resistors
; on these pins, they will blink out of phase.
   loop:
      sbi   PORTB,1     ; LED at PB1 off
      cbi   PORTB,2     ; LED at PB2 on
      rcall delay_long  ; Wait
      cbi   PORTB,1     ; LED at PB1 on
      sbi   PORTB,2     ; LED at PB2 off
      rcall delay_long  ; Wait
      rjmp   loop

; Generate a delay using three nested loops that does nothing.
; With a 10 MHz clock, the values below produce ~261 ms delay.
   delay_long:
      ldi   r23,10      ; r23 <-- Counter for outer loop
  d1: ldi   r24,255     ; r24 <-- Counter for level 2 loop
  d2: ldi   r25,255     ; r25 <-- Counter for inner loop
  d3: dec   r25
      nop               ; no operation
      brne  d3
      dec   r24
      brne  d2
      dec   r23
```

100 %

Name	Value
Analog Comparator (AC)	
Analog-to-Digital Convert...	
Bootloader (BOOT_LOAD)	
CPU Registers (CPU)	
EEPROM (EEPROM)	
External Interrupts (EXINT)	
I/O Port (PORTB)	
Timer/Counter, 8-bit (TC0)	
Timer/Counter, 8-bit (TC1)	
Universal Serial Interface (...	
Watchdog Timer (WDT)	

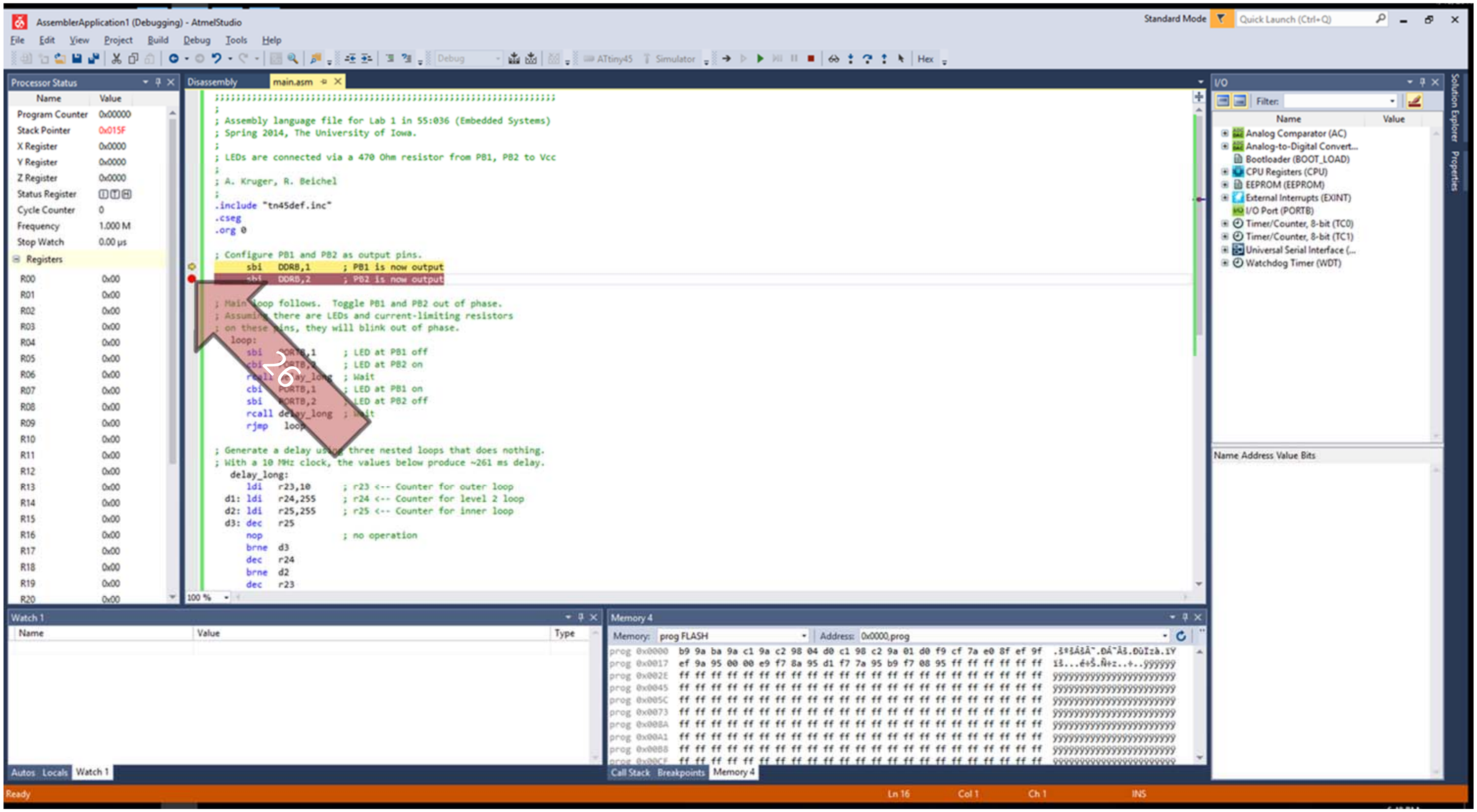
Name Address Value Bits

Name	Value	Type

Memory: prog FLASH   Address: 0x0000,prog

```
prog 0x0000  b9 9a ba 9a c1 9a c2 98 04 d0 c1 98 c2 9a 01 d0 f9 cf 7a e0 8f ef 9f  .¹š º šÁšÂ˜.ÐÁ˜Âš.ÐùÏzà.ïŸ
prog 0x0017  ef 9a 95 00 00 e9 f7 8a 95 d1 f7 7a 95 b9 f7 08 95 ff ff ff ff ff ff  ïš•..é÷Š•Ñ÷z•¹÷.•ÿÿÿÿÿÿ
prog 0x002E  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x0045  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x005C  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x0073  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x008A  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x00A1  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x00B8  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x00CF  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
```

The I/O panel which allows you to simulate I/O like button presses while debugging



Processor Status

Name	Value
Program Counter	0x00000
Stack Pointer	0x015F
X Register	0x0000
Y Register	0x0000
Z Register	0x0000
Status Register	I T H
Cycle Counter	0
Frequency	1.000 M
Stop Watch	0.00 µs
Registers	
R00	0x00
R01	0x00
R02	0x00
R03	0x00
R04	0x00
R05	0x00
R06	0x00
R07	0x00
R08	0x00
R09	0x00
R10	0x00
R11	0x00
R12	0x00
R13	0x00
R14	0x00
R15	0x00
R16	0x00
R17	0x00
R18	0x00
R19	0x00
R20	0x00

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
; Assembly language file for Lab 1 in 55:036 (Embedded Systems)
; Spring 2014, The University of Iowa.
;
; LEDs are connected via a 470 Ohm resistor from PB1, PB2 to Vcc
;
; A. Kruger, R. Beichel
;
.include "tn45def.inc"
.cseg
.org 0

; Configure PB1 and PB2 as output pins.
      sbi   DDRB,1        ; PB1 is now output
      sbi   DDRB,2        ; PB2 is now output

; Main loop follows.  Toggle PB1 and PB2 out of phase.
; Assuming there are LEDs and current-limiting resistors
; on these pins, they will blink out of phase.
 loop:
      sbi   PORTB,1       ; LED at PB1 off
      cbi   PORTB,2       ; LED at PB2 on
      rcall delay_long    ; Wait
      cbi   PORTB,1       ; LED at PB1 on
      sbi   PORTB,2       ; LED at PB2 off
      rcall delay_long    ; Wait
      rjmp   loop

; Generate a delay using three nested loops that does nothing.
; With a 10 MHz clock, the values below produce ~261 ms delay.
 delay_long:
      ldi   r23,10        ; r23 <-- Counter for outer loop
  d1: ldi   r24,255       ; r24 <-- Counter for level 2 loop
  d2: ldi   r25,255       ; r25 <-- Counter for inner loop
  d3: dec   r25
      nop                 ; no operation
      brne  d3
      dec   r24
      brne  d2
      dec   r23
```

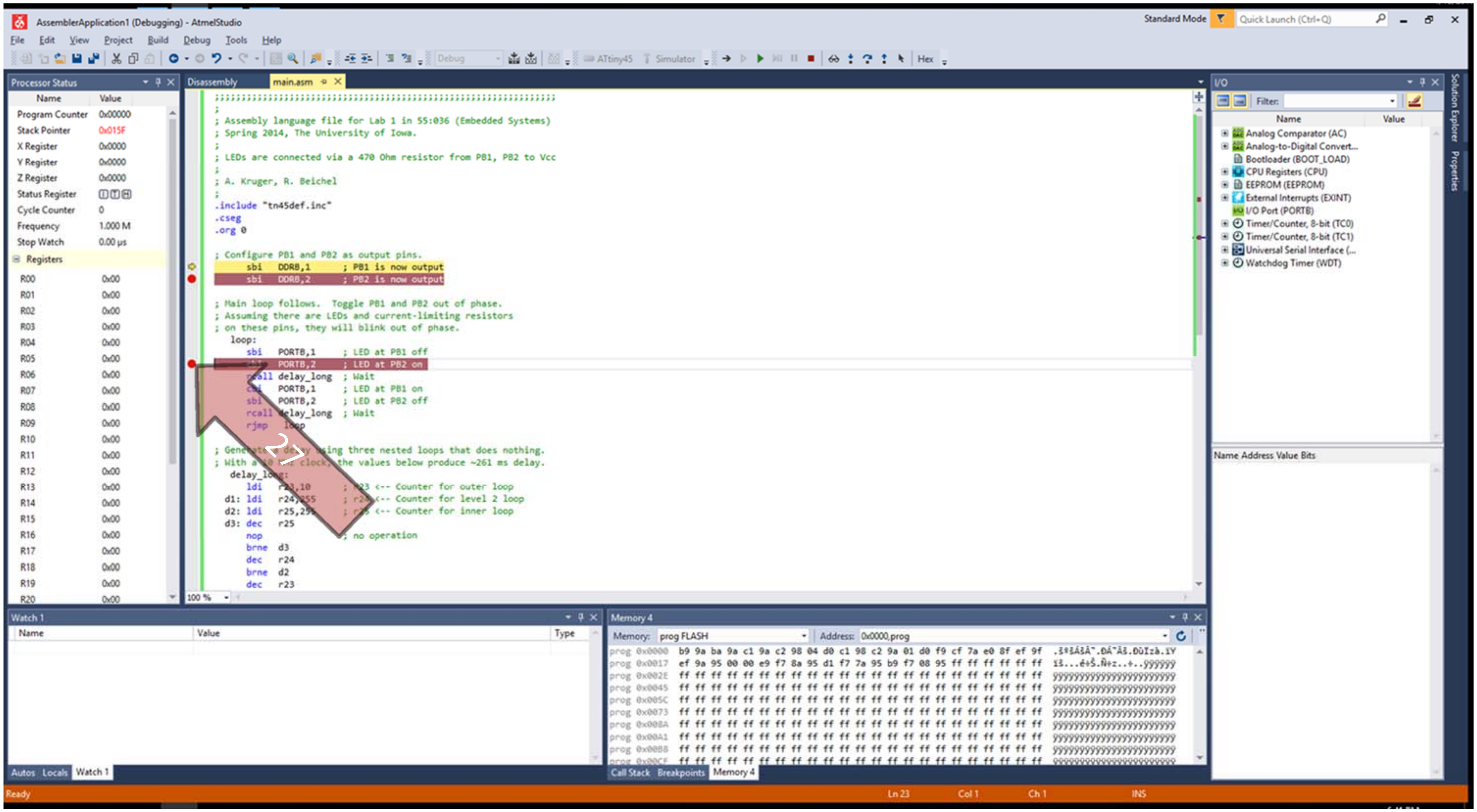
Name	Value	Type

Memory 4 — Memory: prog FLASH — Address: 0x0000,prog

```
prog 0x0000  b9 9a ba 9a c1 9a c2 98 04 d0 c1 98 c2 9a 01 d0 f9 cf 7a e0 8f ef 9f  .¹š º šÁšÂ˜.ÐÁ˜Âš.ÐùÏzà.ïŸ
prog 0x0017  ef 9a 95 00 00 e9 f7 8a 95 d1 f7 7a 95 b9 f7 08 95 ff ff ff ff ff ff  ïš•..é÷Š•Ñ÷z•¹÷.•ÿÿÿÿÿÿ
prog 0x002E  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x0045  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x005C  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x0073  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x008A  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x00A1  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x00B8  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x00CF  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
```

Breakpoints are extremely useful for debugging

26. Set a breakpoint by clicking in the column to the left of the instruction you want to stop before (where the red dot is in the image above)



```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
; Assembly language file for Lab 1 in 55:036 (Embedded Systems)
; Spring 2014, The University of Iowa.
;
; LEDs are connected via a 470 Ohm resistor from PB1, PB2 to Vcc
;
; A. Kruger, R. Beichel
;
.include "tn45def.inc"
.cseg
.org 0

; Configure PB1 and PB2 as output pins.
      sbi   DDRB,1      ; PB1 is now output
      sbi   DDRB,2      ; PB2 is now output

; Main loop follows.  Toggle PB1 and PB2 out of phase.
; Assuming there are LEDs and current-limiting resistors
; on these pins, they will blink out of phase.
   loop:
      sbi   PORTB,1     ; LED at PB1 off
      cbi   PORTB,2     ; LED at PB2 on
      rcall delay_long  ; Wait
      cbi   PORTB,1     ; LED at PB1 on
      sbi   PORTB,2     ; LED at PB2 off
      rcall delay_long  ; Wait
      rjmp  loop

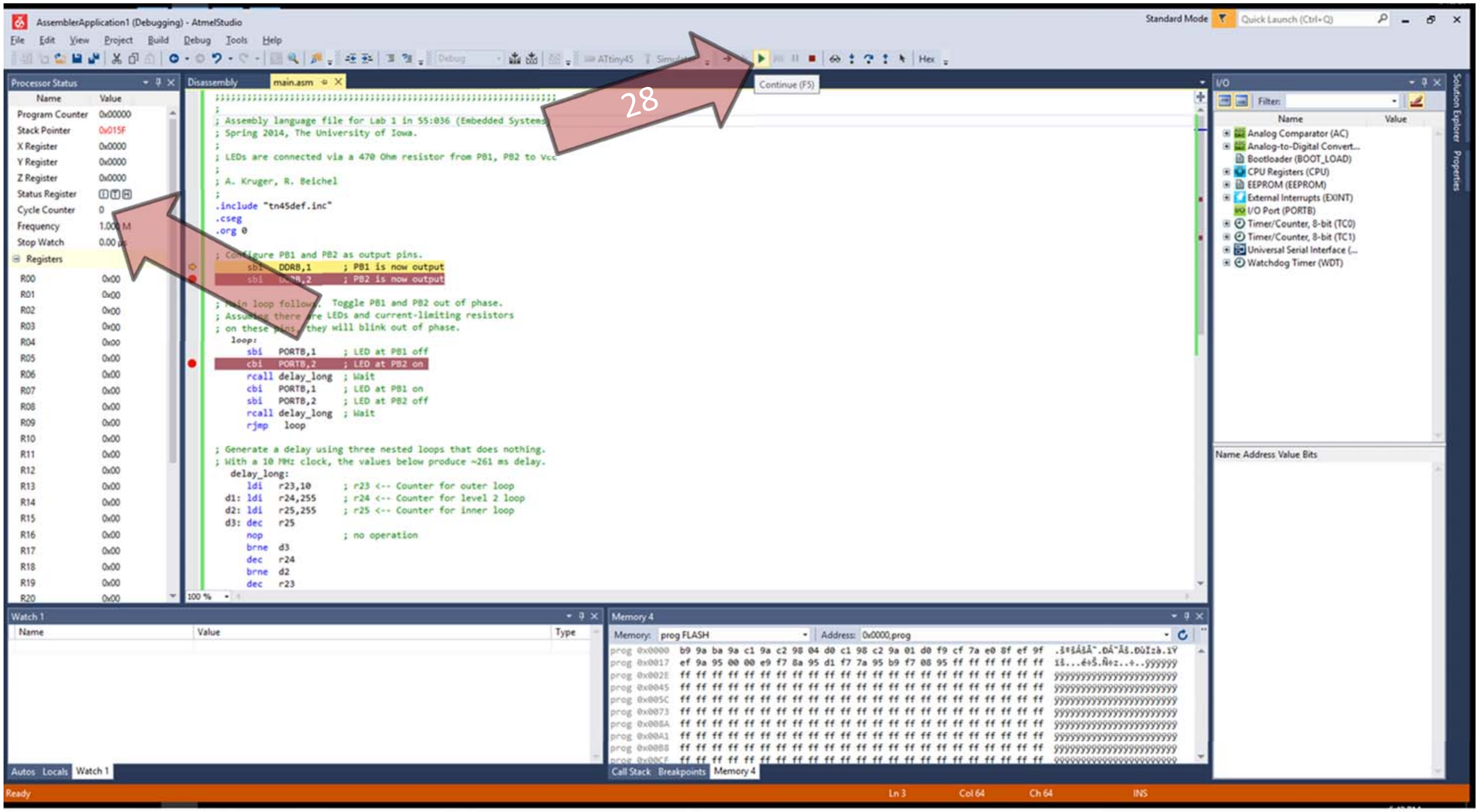
; Generate a delay using three nested loops that does nothing.
; With a 10 MHz clock, the values below produce ~261 ms delay.
   delay_long:
      ldi   r23,10      ; r23 <-- Counter for outer loop
  d1: ldi   r24,255     ; r24 <-- Counter for level 2 loop
  d2: ldi   r25,255     ; r25 <-- Counter for inner loop
  d3: dec   r25
      nop               ; no operation
      brne  d3
      dec   r24
      brne  d2
      dec   r23
```

Name	Value
Program Counter	0x00000
Stack Pointer	0x015F
X Register	0x0000
Y Register	0x0000
Z Register	0x0000
Status Register	
Cycle Counter	0
Frequency	1.000 M
Stop Watch	0.00 µs
Registers	
R00	0x00
R01	0x00
R02	0x00
R03	0x00
R04	0x00
R05	0x00
R06	0x00
R07	0x00
R08	0x00
R09	0x00
R10	0x00
R11	0x00
R12	0x00
R13	0x00
R14	0x00
R15	0x00
R16	0x00
R17	0x00
R18	0x00
R19	0x00
R20	0x00

```
Memory: prog FLASH   Address: 0x0000,prog
prog 0x0000  b9 9a ba 9a c1 9a c2 98 04 d0 c1 98 c2 9a 01 d0 f9 cf 7a e0 8f ef 9f
prog 0x0017  ef 9a 95 00 00 e9 f7 8a 95 d1 f7 7a 95 b9 f7 08 95 ff ff ff ff ff ff
prog 0x002E  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x0045  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x005C  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x0073  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x008A  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x00A1  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x00B8  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
```

AssemblerApplication1 (Debugging) - AtmelStudio
File Edit View Project Build Debug Tools Help
Processor Status
Disassembly
main.asm
I/O
Analog Comparator (AC)
Analog-to-Digital Convert...
Bootloader (BOOT_LOAD)
CPU Registers (CPU)
EEPROM (EEPROM)
External Interrupts (EXINT)
I/O Port (PORTB)
Timer/Counter, 8-bit (TC0)
Timer/Counter, 8-bit (TC1)
Universal Serial Interface (...
Watchdog Timer (WDT)
Watch 1
Memory 4
Ready
Ln 23 Col 1 Ch 1 INS
27

27. Insert another breakpoint


AssemblerApplication1 (Debugging) - AtmelStudio
File Edit View Project Build Debug Tools Help
28
Continue (F5)
Disassembly
main.asm
I/O
Filter:
Analog Comparator (AC)
Analog-to-Digital Convert...
Bootloader (BOOT_LOAD)
CPU Registers (CPU)
EEPROM (EEPROM)
External Interrupts (EXINT)
I/O Port (PORTB)
Timer/Counter, 8-bit (TC0)
Timer/Counter, 8-bit (TC1)
Universal Serial Interface (...
Watchdog Timer (WDT)
Name Address Value Bits
Watch 1
Autos Locals Watch 1
Call Stack Breakpoints Memory 4
Ready Ln 3 Col 64 Ch 64 INS

Processor Status

Name	Value
Program Counter	0x00000
Stack Pointer	0x015F
X Register	0x0000
Y Register	0x0000
Z Register	0x0000
Status Register	I T H
Cycle Counter	0
Frequency	1.000 M
Stop Watch	0.00 µs
Registers	
R00	0x00
R01	0x00
R02	0x00
R03	0x00
R04	0x00
R05	0x00
R06	0x00
R07	0x00
R08	0x00
R09	0x00
R10	0x00
R11	0x00
R12	0x00
R13	0x00
R14	0x00
R15	0x00
R16	0x00
R17	0x00
R18	0x00
R19	0x00
R20	0x00

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
; Assembly language file for Lab 1 in 55:036 (Embedded Systems
; Spring 2014, The University of Iowa.
;
; LEDs are connected via a 470 Ohm resistor from PB1, PB2 to Vcc
;
; A. Kruger, R. Beichel
;
.include "tn45def.inc"
.cseg
.org 0

; Configure PB1 and PB2 as output pins.
      sbi   DDRB,1        ; PB1 is now output
      sbi   DDRB,2        ; PB2 is now output

; Main loop follows.  Toggle PB1 and PB2 out of phase.
; Assuming there are LEDs and current-limiting resistors
; on these pins, they will blink out of phase.
  loop:
      sbi   PORTB,1       ; LED at PB1 off
      cbi   PORTB,2       ; LED at PB2 on
      rcall delay_long    ; Wait
      cbi   PORTB,1       ; LED at PB1 on
      sbi   PORTB,2       ; LED at PB2 off
      rcall delay_long    ; Wait
      rjmp   loop

; Generate a delay using three nested loops that does nothing.
; With a 10 MHz clock, the values below produce ~261 ms delay.
  delay_long:
      ldi   r23,10        ; r23 <-- Counter for outer loop
  d1: ldi   r24,255       ; r24 <-- Counter for level 2 loop
  d2: ldi   r25,255       ; r25 <-- Counter for inner loop
  d3: dec   r25
      nop                 ; no operation
      brne  d3
      dec   r24
      brne  d2
      dec   r23
```

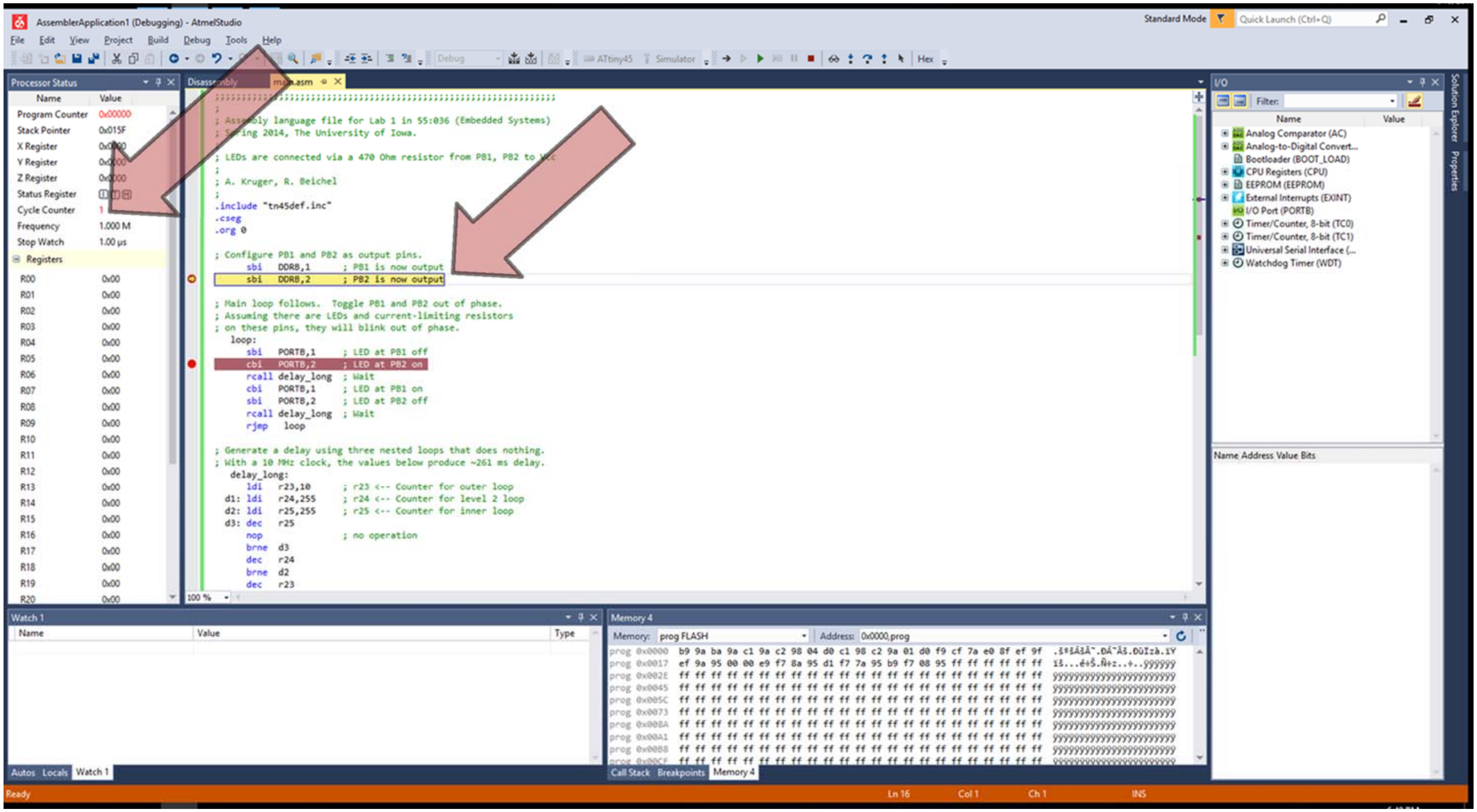
Memory 4

Memory: prog FLASH Address: 0x0000,prog

```
prog 0x0000  b9 9a ba 9a c1 9a c2 98 04 d0 c1 98 c2 9a 01 d0 f9 cf 7a e0 8f ef 9f  .š°šÁšÂ˜.ÐÁ˜Âš.ÐùÏzà.ïŸ
prog 0x0017  ef 9a 95 00 00 e9 f7 8a 95 d1 f7 7a 95 b9 f7 08 95 ff ff ff ff ff ff  ïš•..é÷Š•Ñ÷z•¹÷.•ÿÿÿÿÿÿ
prog 0x002E  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x0045  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x005C  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x0073  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x008A  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x00A1  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x00B8  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x00CF  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
```

Notice that the “Cycle Counter” shows zero

28. Click “Continue” to run the program until it reaches the next breakpoint



Processor Status

Name	Value
Program Counter	0x00000
Stack Pointer	0x015F
X Register	0x0000
Y Register	0x0000
Z Register	0x0000
Status Register	
Cycle Counter	1
Frequency	1.000 M
Stop Watch	1.00 µs
Registers	
R00	0x00
R01	0x00
R02	0x00
R03	0x00
R04	0x00
R05	0x00
R06	0x00
R07	0x00
R08	0x00
R09	0x00
R10	0x00
R11	0x00
R12	0x00
R13	0x00
R14	0x00
R15	0x00
R16	0x00
R17	0x00
R18	0x00
R19	0x00
R20	0x00

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
; Assembly language file for Lab 1 in 55:036 (Embedded Systems)
; Spring 2014, The University of Iowa.
;
; LEDs are connected via a 470 Ohm resistor from PB1, PB2 to Vcc
;
; A. Kruger, R. Beichel
;
.include "tn45def.inc"
.cseg
.org 0

; Configure PB1 and PB2 as output pins.
      sbi   DDRB,1      ; PB1 is now output
      sbi   DDRB,2      ; PB2 is now output

; Main loop follows.  Toggle PB1 and PB2 out of phase.
; Assuming there are LEDs and current-limiting resistors
; on these pins, they will blink out of phase.
   loop:
      sbi   PORTB,1     ; LED at PB1 off
      cbi   PORTB,2     ; LED at PB2 on
      rcall delay_long  ; Wait
      cbi   PORTB,1     ; LED at PB1 on
      sbi   PORTB,2     ; LED at PB2 off
      rcall delay_long  ; Wait
      rjmp   loop

; Generate a delay using three nested loops that does nothing.
; With a 10 MHz clock, the values below produce ~261 ms delay.
   delay_long:
      ldi   r23,10      ; r23 <-- Counter for outer loop
  d1: ldi   r24,255     ; r24 <-- Counter for level 2 loop
  d2: ldi   r25,255     ; r25 <-- Counter for inner loop
  d3: dec   r25
      nop               ; no operation
      brne  d3
      dec   r24
      brne  d2
      dec   r23
```

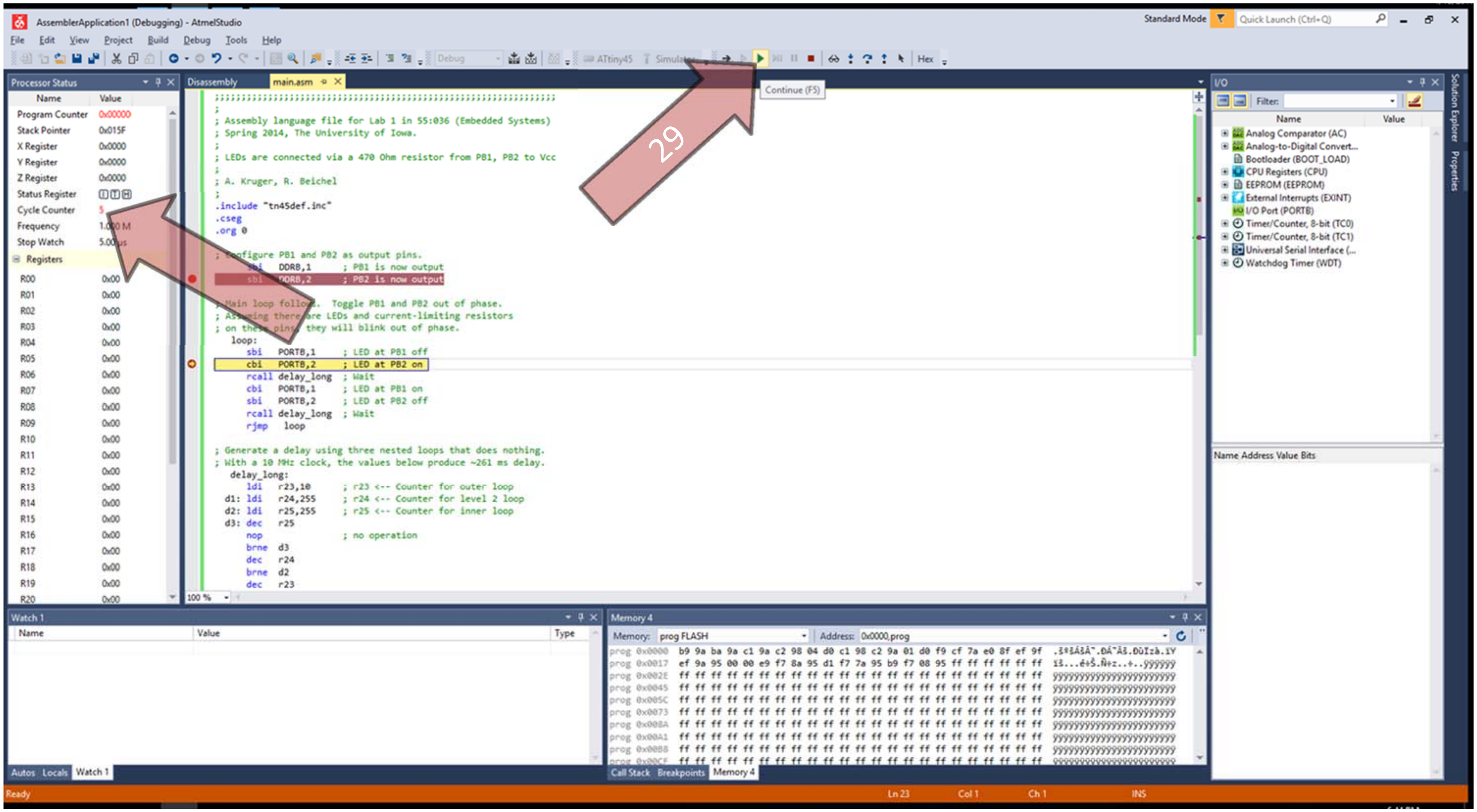
100 %

Memory 4

Memory: prog FLASH   Address: 0x0000,prog

```
prog 0x0000  b9 9a ba 9a c1 9a c2 98 04 d0 c1 98 c2 9a 01 d0 f9 cf 7a e0 8f ef 9f  .¹šºšÁšÂ˜.ÐÁ˜Âš.ÐùÏzà.ïŸ
prog 0x0017  ef 9a 95 00 00 e9 f7 8a 95 d1 f7 7a 95 b9 f7 08 95 ff ff ff ff ff ff  ïš•..é÷Š•Ñ÷z•¹÷.•ÿÿÿÿÿÿ
prog 0x002E  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x0045  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x005C  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x0073  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x008A  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x00A1  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x00B8  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
prog 0x00CF  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
```

Notice that the highlighted instruction is the first one that was marked with a breakpoint and that the “Cycle Counter” has been incremented by 1



Name	Value
Program Counter	0x00000
Stack Pointer	0x015F
X Register	0x0000
Y Register	0x0000
Z Register	0x0000
Status Register	I T H
Cycle Counter	5
Frequency	1.000 M
Stop Watch	5.00 us
Registers	
R00	0x00
R01	0x00
R02	0x00
R03	0x00
R04	0x00
R05	0x00
R06	0x00
R07	0x00
R08	0x00
R09	0x00
R10	0x00
R11	0x00
R12	0x00
R13	0x00
R14	0x00
R15	0x00
R16	0x00
R17	0x00
R18	0x00
R19	0x00
R20	0x00

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
; Assembly language file for Lab 1 in 55:036 (Embedded Systems)
; Spring 2014, The University of Iowa.
;
; LEDs are connected via a 470 Ohm resistor from PB1, PB2 to Vcc
;
; A. Kruger, R. Beichel
;
.include "tn45def.inc"
.cseg
.org 0

; Configure PB1 and PB2 as output pins.
      sbi   DDRB,1       ; PB1 is now output
      sbi   DDRB,2       ; PB2 is now output

; Main loop follows.  Toggle PB1 and PB2 out of phase.
; Assuming there are LEDs and current-limiting resistors
; on these pins, they will blink out of phase.
  loop:
      sbi   PORTB,1      ; LED at PB1 off
      cbi   PORTB,2      ; LED at PB2 on
      rcall delay_long   ; Wait
      cbi   PORTB,1      ; LED at PB1 on
      sbi   PORTB,2      ; LED at PB2 off
      rcall delay_long   ; Wait
      rjmp   loop

; Generate a delay using three nested loops that does nothing.
; With a 10 MHz clock, the values below produce ~261 ms delay.
  delay_long:
      ldi   r23,10       ; r23 <-- Counter for outer loop
  d1: ldi   r24,255      ; r24 <-- Counter for level 2 loop
  d2: ldi   r25,255      ; r25 <-- Counter for inner loop
  d3: dec   r25
      nop                ; no operation
      brne  d3
      dec   r24
      brne  d2
      dec   r23
```

100 %

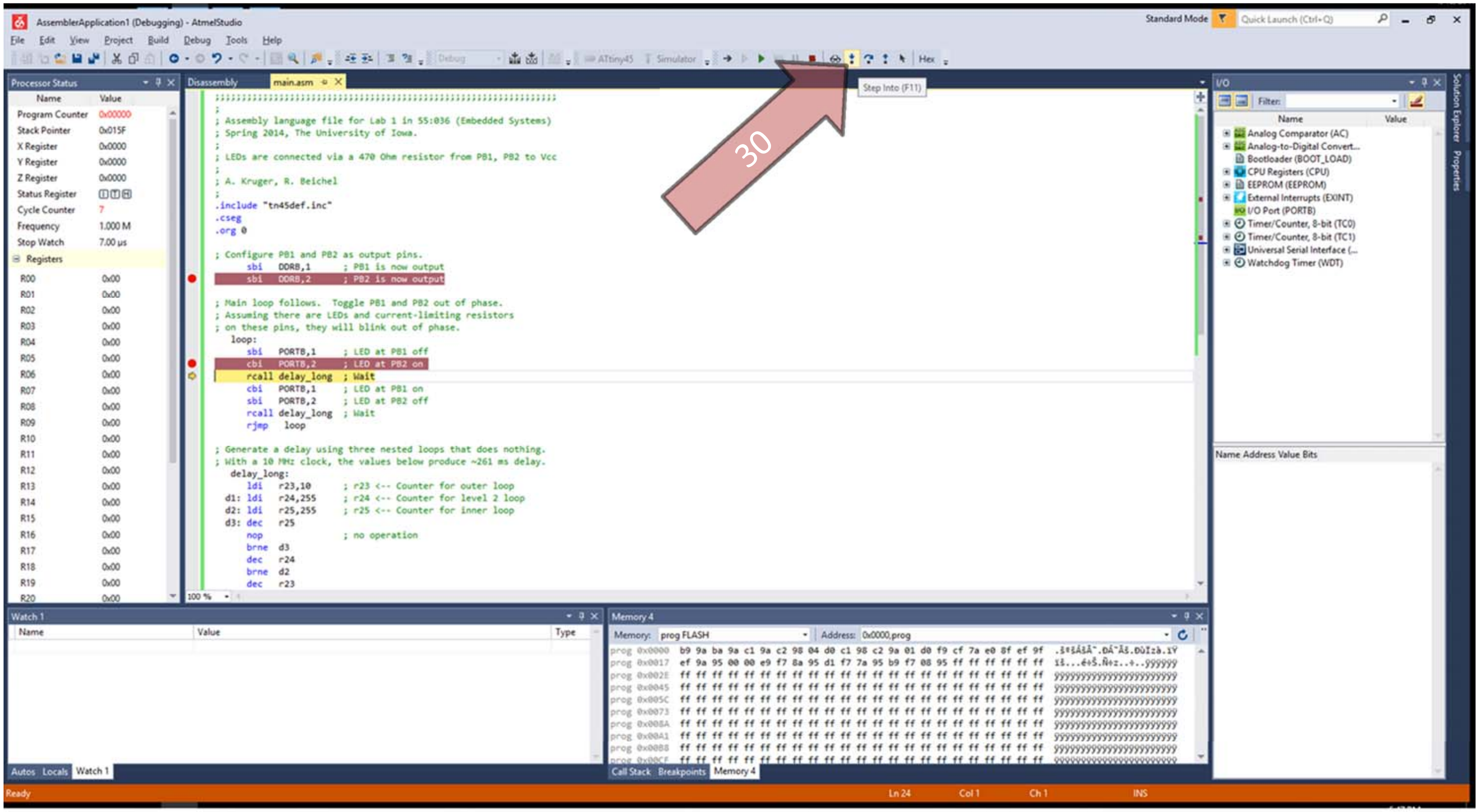
Memory 4

Memory: prog FLASH   Address: 0x0000,prog

```
prog 0x0000  b9 9a ba 9a c1 9a c2 98 04 d0 c1 98 c2 9a 01 d0 f9 cf 7a e0 8f ef 9f
prog 0x0017  ef 9a 95 00 00 e9 f7 8a 95 d1 f7 7a 95 b9 f7 08 95 ff ff ff ff ff ff
prog 0x002E  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x0045  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x005C  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x0073  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x008A  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x00A1  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x00B8  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x00CF  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
```

29. Click “Continue” again to navigate to the next breakpoint

Notice that the “Cycle Counter” now shows 5


AssemblerApplication1 (Debugging) - AtmelStudio
File Edit View Project Build Debug Tools Help
Step Into (F11)
30
Processor Status
Disassembly
main.asm
I/O
Watch 1
Memory 4

Name	Value
Program Counter	0x00000
Stack Pointer	0x015F
X Register	0x0000
Y Register	0x0000
Z Register	0x0000
Status Register	
Cycle Counter	7
Frequency	1.000 M
Stop Watch	7.00 µs
Registers	
R00	0x00
R01	0x00
R02	0x00
R03	0x00
R04	0x00
R05	0x00
R06	0x00
R07	0x00
R08	0x00
R09	0x00
R10	0x00
R11	0x00
R12	0x00
R13	0x00
R14	0x00
R15	0x00
R16	0x00
R17	0x00
R18	0x00
R19	0x00
R20	0x00

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
; Assembly language file for Lab 1 in 55:036 (Embedded Systems)
; Spring 2014, The University of Iowa.
;
; LEDs are connected via a 470 Ohm resistor from PB1, PB2 to Vcc
;
; A. Kruger, R. Beichel
;
.include "tn45def.inc"
.cseg
.org 0

; Configure PB1 and PB2 as output pins.
      sbi   DDRB,1      ; PB1 is now output
      sbi   DDRB,2      ; PB2 is now output

; Main loop follows.  Toggle PB1 and PB2 out of phase.
; Assuming there are LEDs and current-limiting resistors
; on these pins, they will blink out of phase.
   loop:
      sbi   PORTB,1     ; LED at PB1 off
      cbi   PORTB,2     ; LED at PB2 on
      rcall delay_long  ; Wait
      cbi   PORTB,1     ; LED at PB1 on
      sbi   PORTB,2     ; LED at PB2 off
      rcall delay_long  ; Wait
      rjmp   loop

; Generate a delay using three nested loops that does nothing.
; With a 10 MHz clock, the values below produce ~261 ms delay.
   delay_long:
      ldi   r23,10      ; r23 <-- Counter for outer loop
  d1: ldi   r24,255     ; r24 <-- Counter for level 2 loop
  d2: ldi   r25,255     ; r25 <-- Counter for inner loop
  d3: dec   r25
      nop               ; no operation
      brne  d3
      dec   r24
      brne  d2
      dec   r23
```

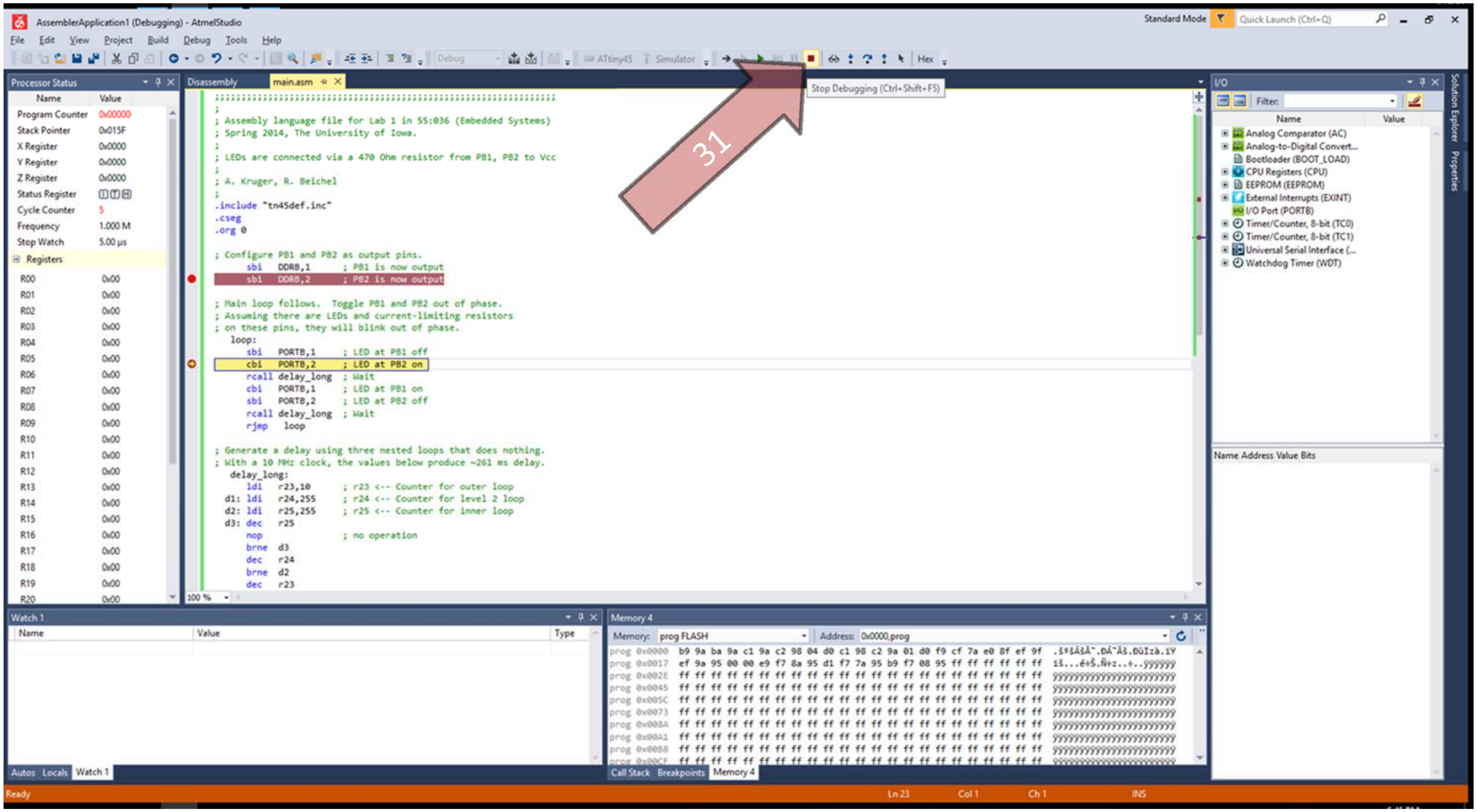
I/O: Analog Comparator (AC), Analog-to-Digital Convert..., Bootloader (BOOT_LOAD), CPU Registers (CPU), EEPROM (EEPROM), External Interrupts (EXINT), I/O Port (PORTB), Timer/Counter, 8-bit (TC0), Timer/Counter, 8-bit (TC1), Universal Serial Interface (..., Watchdog Timer (WDT)

Memory: prog FLASH   Address: 0x0000,prog

```
prog 0x0000  b9 9a ba 9a c1 9a c2 98 04 d0 c1 98 c2 9a 01 d0 f9 cf 7a e0 8f ef 9f
prog 0x0017  ef 9a 95 00 00 e9 f7 8a 95 d1 f7 7a 95 b9 f7 08 95 ff ff ff ff ff ff
prog 0x002E  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x0045  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x005C  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x0073  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x008A  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x00A1  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x00B8  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x00CF  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
```

Ready   Ln 24   Col 1   Ch 1   INS

30. Click “Step Into” to execute the line of code the debugger is currently on and stop at the next one



Name	Value
Program Counter	0x00000
Stack Pointer	0x015F
X Register	0x0000
Y Register	0x0000
Z Register	0x0000
Status Register	ITH
Cycle Counter	5
Frequency	1.000 M
Stop Watch	5.00 µs
Registers	
R00	0x00
R01	0x00
R02	0x00
R03	0x00
R04	0x00
R05	0x00
R06	0x00
R07	0x00
R08	0x00
R09	0x00
R10	0x00
R11	0x00
R12	0x00
R13	0x00
R14	0x00
R15	0x00
R16	0x00
R17	0x00
R18	0x00
R19	0x00
R20	0x00

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
; Assembly language file for Lab 1 in 55:036 (Embedded Systems)
; Spring 2014, The University of Iowa.
;
; LEDs are connected via a 470 Ohm resistor from PB1, PB2 to Vcc
;
; A. Kruger, R. Beichel
;
.include "tn45def.inc"
.cseg
.org 0

; Configure PB1 and PB2 as output pins.
      sbi   DDRB,1      ; PB1 is now output
      sbi   DDRB,2      ; PB2 is now output

; Main loop follows.  Toggle PB1 and PB2 out of phase.
; Assuming there are LEDs and current-limiting resistors
; on these pins, they will blink out of phase.
   loop:
      sbi   PORTB,1     ; LED at PB1 off
      cbi   PORTB,2     ; LED at PB2 on
      rcall delay_long  ; Wait
      cbi   PORTB,1     ; LED at PB1 on
      sbi   PORTB,2     ; LED at PB2 off
      rcall delay_long  ; Wait
      rjmp   loop

; Generate a delay using three nested loops that does nothing.
; With a 10 MHz clock, the values below produce ~261 ms delay.
   delay_long:
      ldi   r23,10      ; r23 <-- Counter for outer loop
  d1: ldi   r24,255     ; r24 <-- Counter for level 2 loop
  d2: ldi   r25,255     ; r25 <-- Counter for inner loop
  d3: dec   r25
      nop               ; no operation
      brne  d3
      dec   r24
      brne  d2
      dec   r23
```

Name | Value | Type

Memory: prog FLASH Address: 0x0000,prog

```
prog 0x0000  b9 9a ba 9a c1 9a c2 98 04 d0 c1 98 c2 9a 01 d0 f9 cf 7a e0 8f ef 9f
prog 0x0017  ef 9a 95 00 00 e9 f7 8a 95 d1 f7 7a 95 b9 f7 08 95 ff ff ff ff ff ff
prog 0x002E  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x0045  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x005C  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x0073  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x008A  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x00A1  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x00B8  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
prog 0x00CF  ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
```

Name | Value

Analog Comparator (AC)
Analog-to-Digital Convert...
Bootloader (BOOT_LOAD)
CPU Registers (CPU)
EEPROM (EEPROM)
External Interrupts (EXINT)
I/O Port (PORTB)
Timer/Counter, 8-bit (TC0)
Timer/Counter, 8-bit (TC1)
Universal Serial Interface (...
Watchdog Timer (WDT)

Name Address Value Bits

31. Stop the debugger by clicking “Stop Debugging”