1. Introduction

The goal of Lab 2 was to….

2. Schematic

Figure 1 shows the provided circuit design that we used to blink two LEDs.

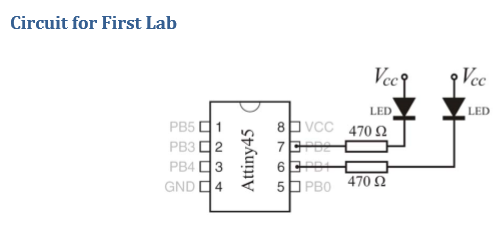


Figure 1: Circuit with two LEDs on PB2 and PB1

3. Discussion

Most time was spent setting up our board and AVR drivers, but upon our first successful flash, we set to work in calculating our needed clock cycle count. To start, we enabled breakpoints to reveal the total cycle count of an unedited loop. We then used that cycle count to derive a formula made up of 3 variables (X1, X 2 , and X 3) to represent the increment counters of our nested loop registers (r23, r24, r25). After incorporating the cycle count of the “nop”, “brne”, “dec”, and “ldi” operations (each taking 4 counts aside from their final execution) we ended up with the following formula:

C = X3 \* (4 + (X2 \* (4 + ( X1 \* 4)))) – (X3 \* X2)

By using the default values of 255, 255, and 10, our C output was 2608690, which accurately represented the number given in simulation. We changed our variables around freely until we landed on a C value that was incredibly close to the required .2484s.

Our final values were r23 = 11, r24 = 226, and r25 = 249, as shown below from our formula calculation.

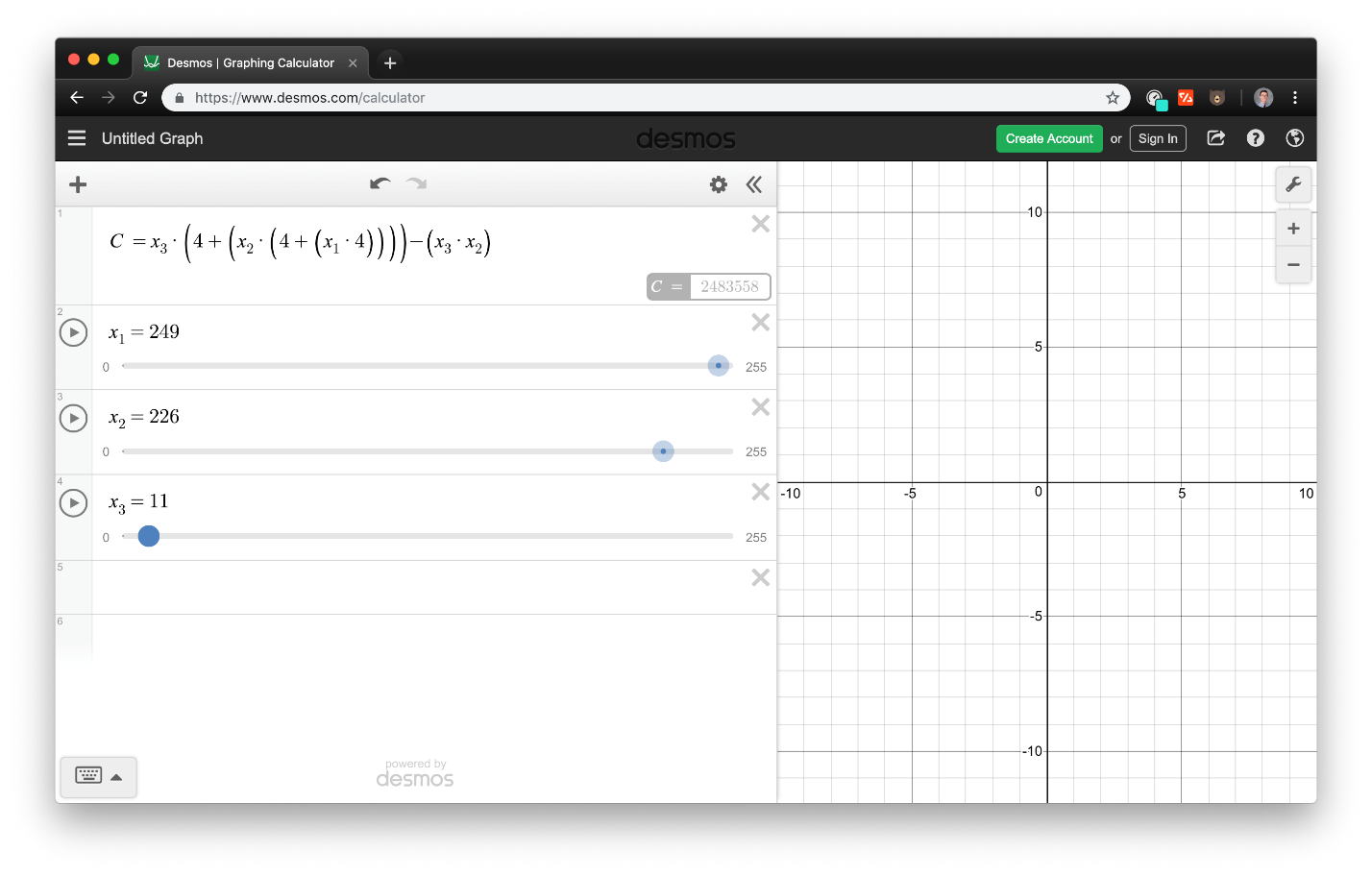


Figure 2: Our resultant calculation

4. Conclusion

In this lab, I grew comfortable calculating cycle counts of individual methods, as well as deploying and simulating assembly code on my own laptop. I also learned proper soldering methods for the first time, which was empowering to have confidence on when headed into future projects.

5. Appendix A: Source Code

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; Assembly language file for Lab 1 in 55:036 (Embedded Systems)

; Spring 2014, The University of Iowa.

;

; LEDs are connected via a 470 Ohm resistor from PB1, PB2 to Vcc

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; A. Kruger, R. Beichel

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; Modifiations for a .2484s long delay instead of .261s

; Done by Alex Powers and Ben Mitchinson

.include "tn45def.inc"

.cseg

.org 0

; Configure PB1 and PB2 as output pins.

sbi DDRB,1 ; PB1 is now output

sbi DDRB,2 ; PB2 is now output

; Main loop follows. Toggle PB1 and PB2 out of phase.

; Assuming there are LEDs and current-limiting resistors

; on these pins, they will blink out of phase.

loop:

sbi PORTB,1 ; LED at PB1 off

cbi PORTB,2 ; LED at PB2 on

rcall delay\_long ; Wait

cbi PORTB,1 ; LED at PB1 on

sbi PORTB,2 ; LED at PB2 off

rcall delay\_long ; Wait

rjmp loop

; Generate a delay using three nested loops that does nothing.

; With a 10 MHz clock, the values below produce ~261 ms delay.

delay\_long:

ldi r23,11 ; r23 <-- Counter for outer loop

d1: ldi r24,226 ; r24 <-- Counter for level 2 loop

d2: ldi r25,249 ; r25 <-- Counter for inner loop

d3: dec r25

nop ; no operation

brne d3

dec r24

brne d2

dec r23

brne d1

ret

.exit