ABSTRACT:

In this experiment, Cadence Virtuoso Software is introduced, which offers a simulation environment for our Verilog code so that we can check that it functions as it should. On the basis of this, we created the schematic for a two-input NAND gate, designed its symbol, and calculated the rise time and fall time for the NAND gate under four distinct scenarios using bit and pulse. The input and output ports' transient responses were also watched. The circuit design project required the creation of a special directory.

KEYWORDS:

2-input NAND Gate, Rise time, Fall time, Propagation delay

OBJECTIVES:

1. To login in to the Cadence Server shell and start the Cadence virtuoso software
2. To create a working library
3. To draw the schematic of a 2-input NAND gate in Cadence Virtuoso Schematic Editor
4. To create a symbol view of the NAND gate from the schematic
5. To simulate the NAND gate using MMSIM Spectre.
6. To determine the rise time and fall time of the output waveforms.

INTRODUCTION:

This experiment introduces how to use Cadence Virtuoso Software to design a 2-input NAND Gate. It teaches us to create a library and draw the required schematic and simulate the circuit.

THEORY:

A NAND gate is a universal gate that can observe how gates like OR, AND, and NOT operate. Two parallel pMOS transistors and two series nMOS transistors make up a CMOS NAND gate.

Two series nMOS transistors and two parallel pMOS transistors make up a two-input CMOS NAND gate.

TRUTH TABLE for NAND Gate:

A	B	Pull Down Network	Pull up Network	Output (Y)
0	0	OFF	ON	1
0	1	OFF	ON	1
1	0	OFF	ON	1
1	1	ON	OFF	0

SIMULATION:

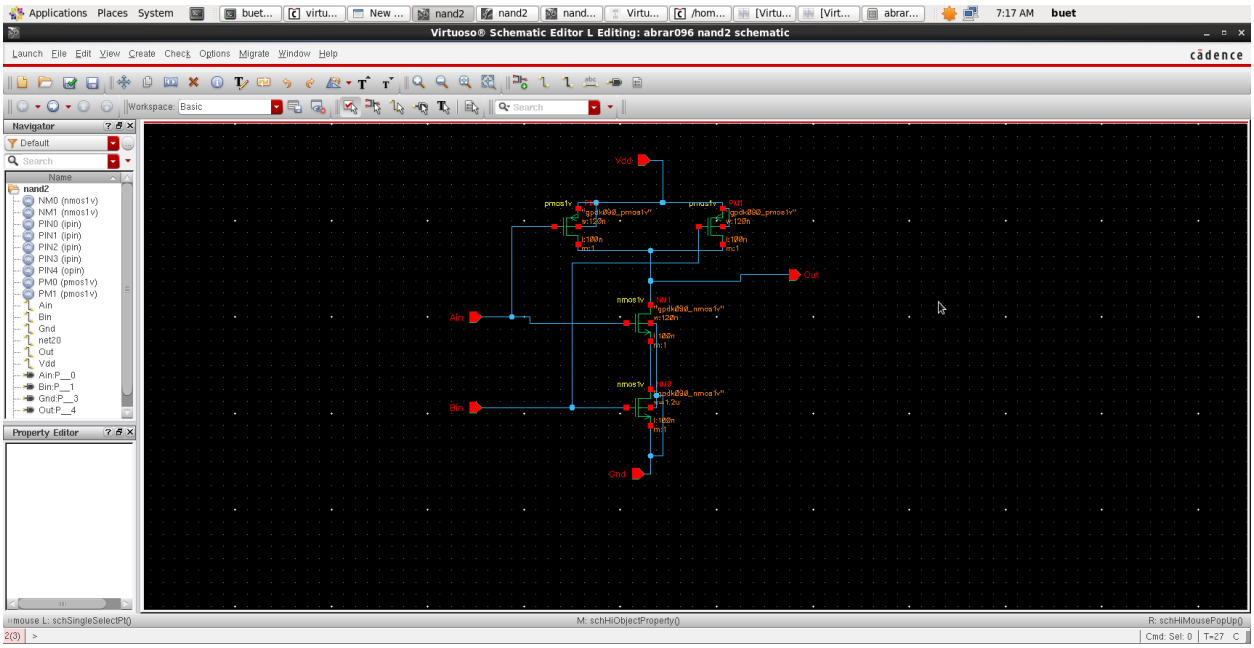

Figure 01: **Schematic Drawing for p*mos*=240 nm, n*mos*=120 nm.**

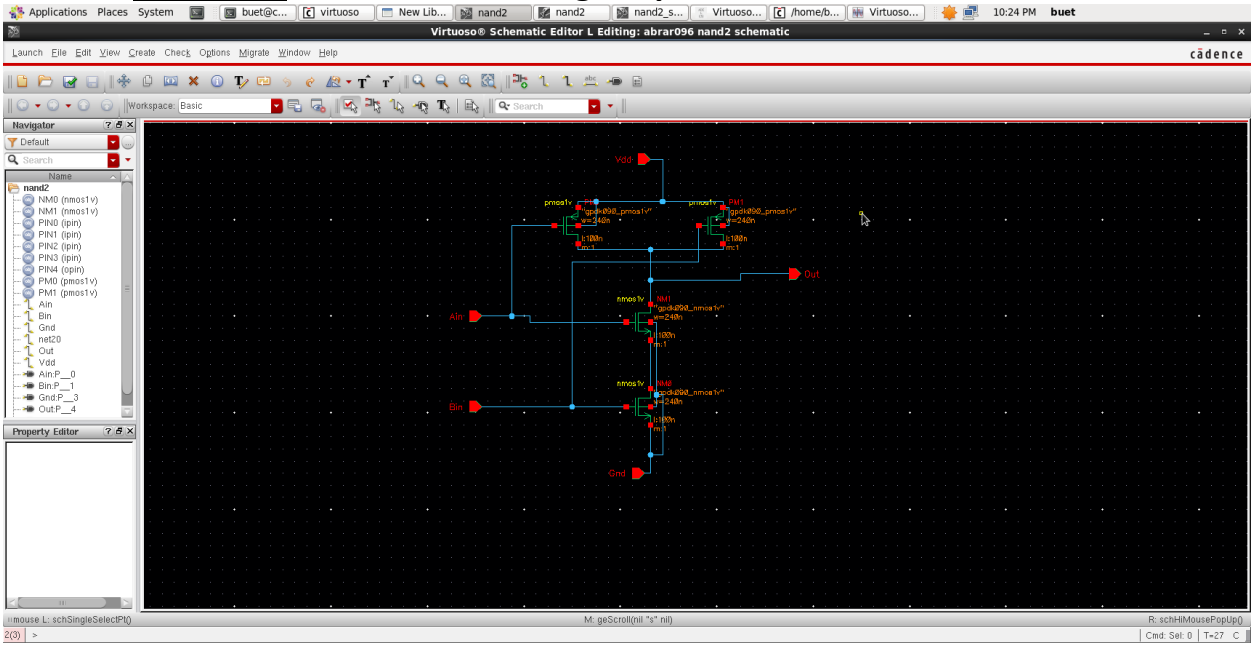

Figure 02: **Schematic Drawing for p*mos*=240 nm, n*mos*=240 nm.**

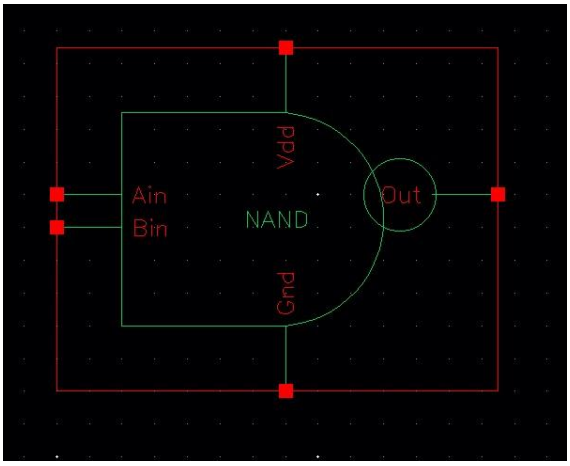

Figure 03: **Symbol.**

SIMULATION RESULT:

- **For p*mos*=240 nm, n*mos*=2400 nm.**

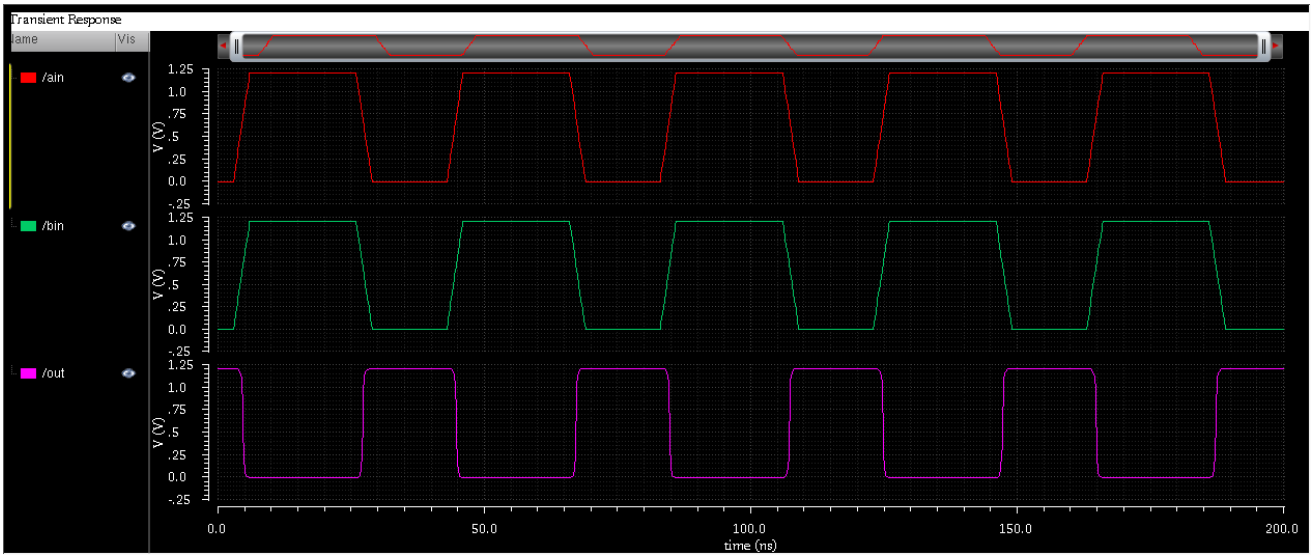

Figure 04: **Output wave forms for p*mos*=240 nm, n*mos*=240 nm.**

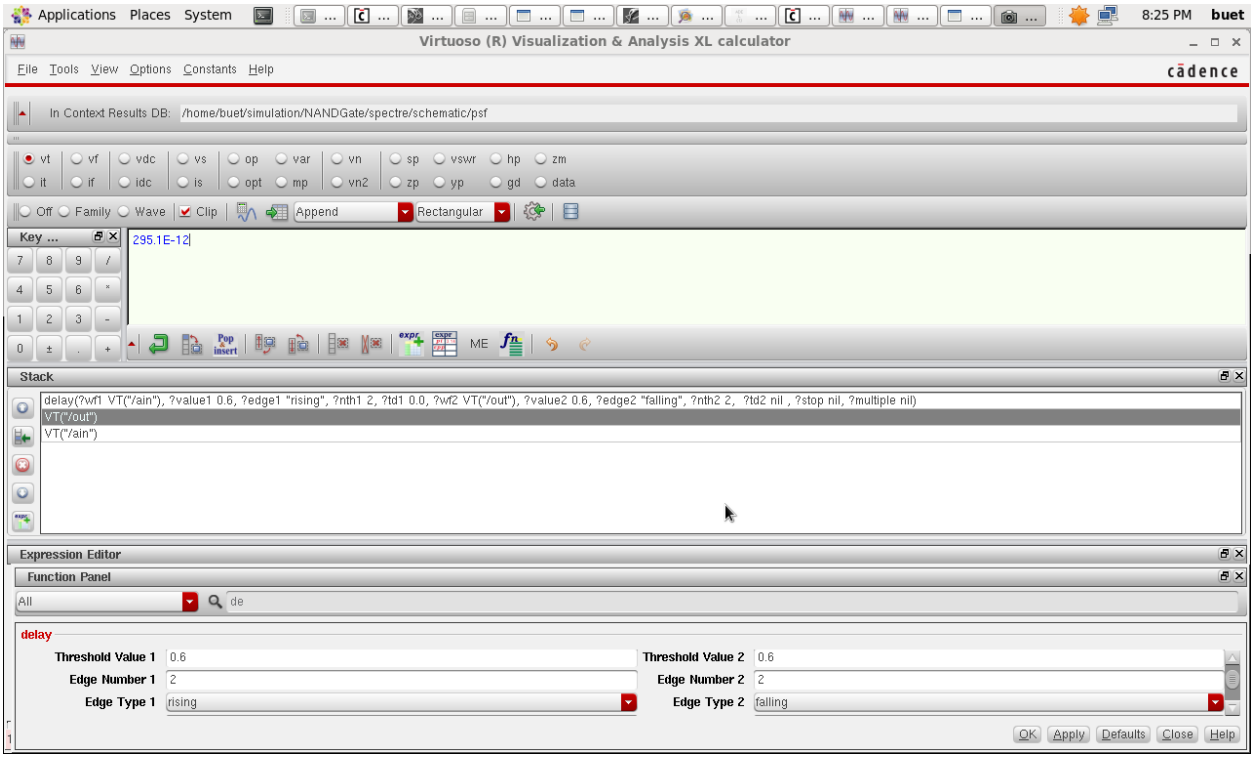

Figure 05: **Delay for p*mos*=240 nm, n*mos*=240 nm.**

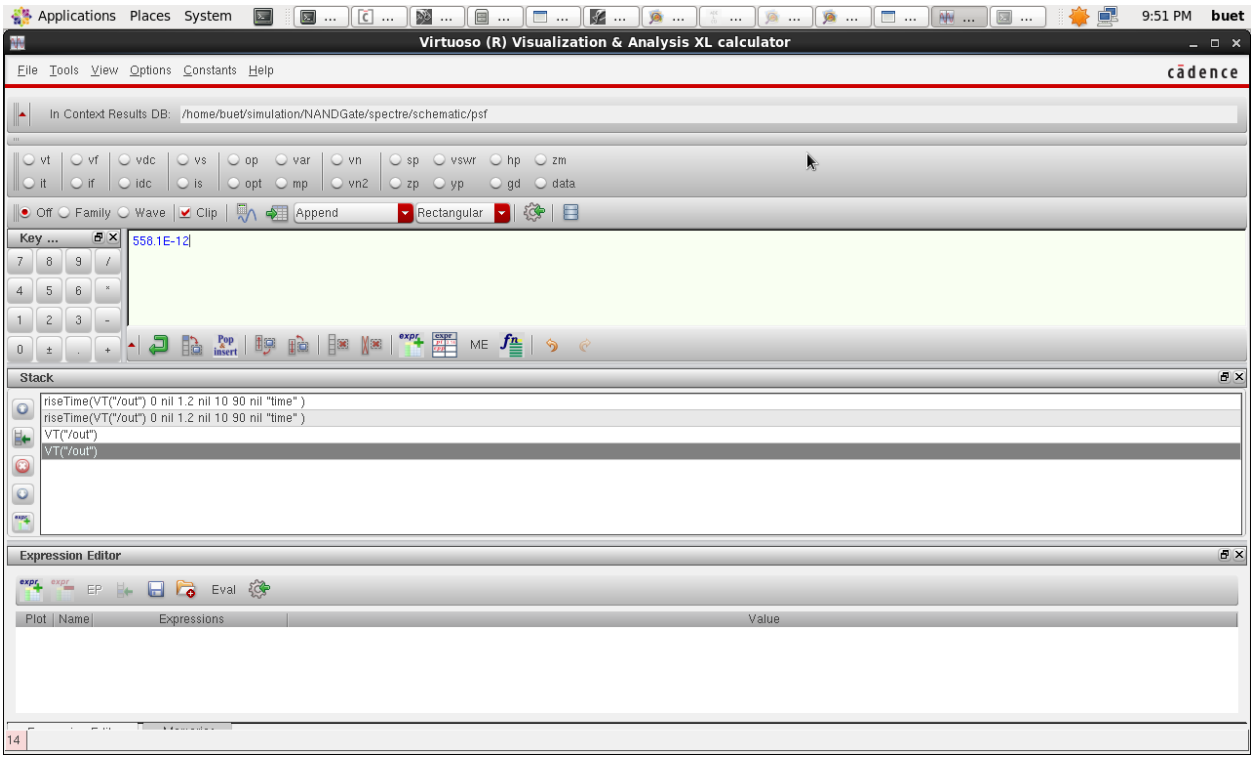

Figure 06: **Risetime for p*mos*=240 nm, n*mos*=240 nm.**

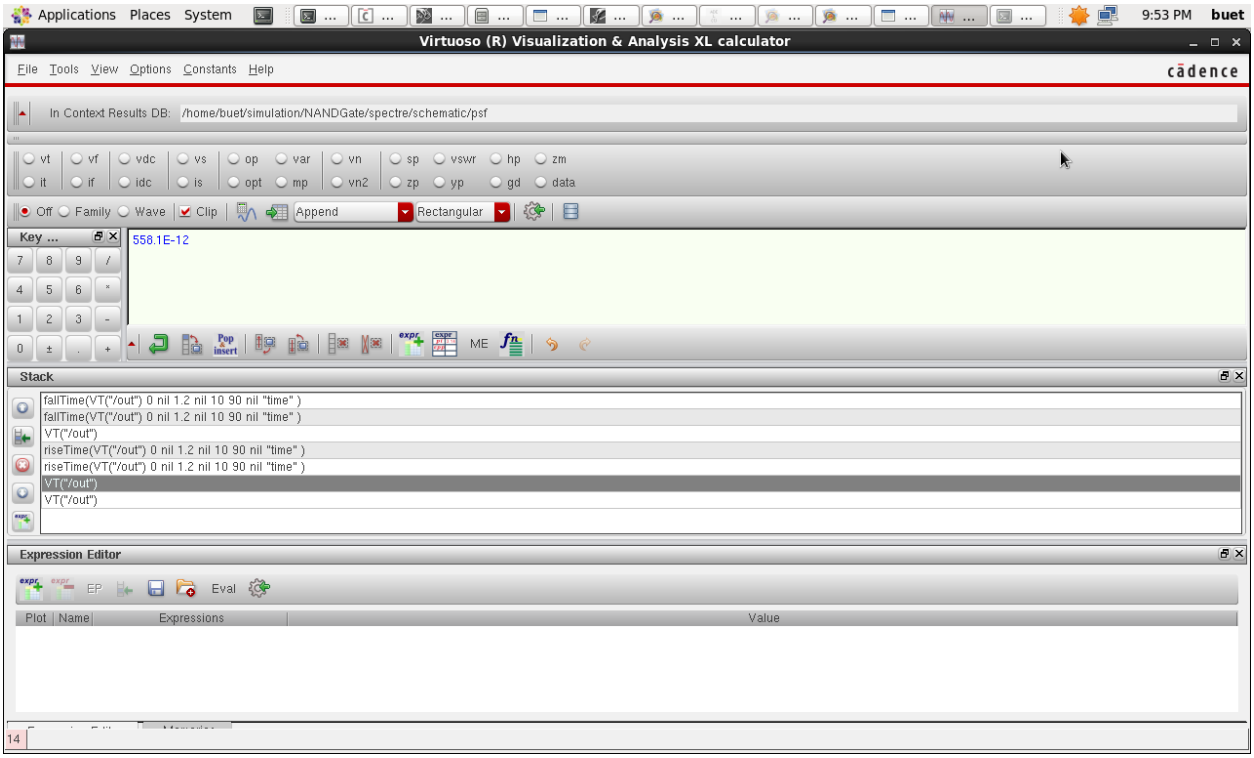

Figure 07: **Falltime for p*mos*=240 nm, n*mos*=240 nm.**

PROPAGATION DELAY:

For pmos=240 nm, nmos=240 nm:

Propagation delay rise time - 295.1 E-12
Propagation delay fall time - 295.1 E-12
Rise Time :558.1 E-12; Fall Time: 558.1 E-12

❖ ***For pmos=240 nm, nmos=120 nm:***

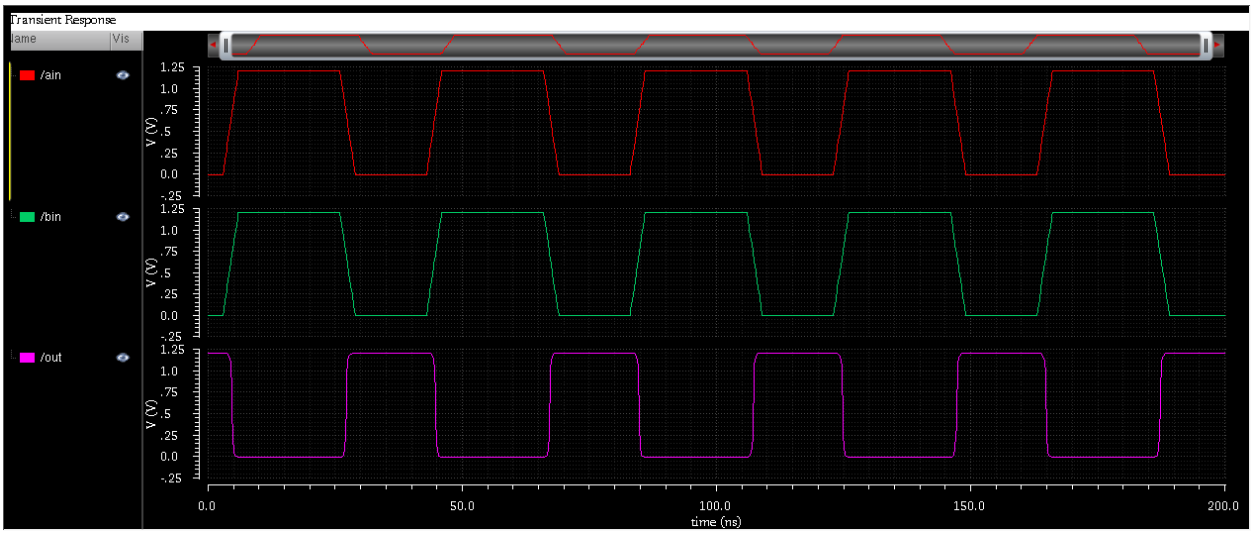

Figure 08: **Output wave forms for p*mos*=240 nm, n*mos*=120 nm.**

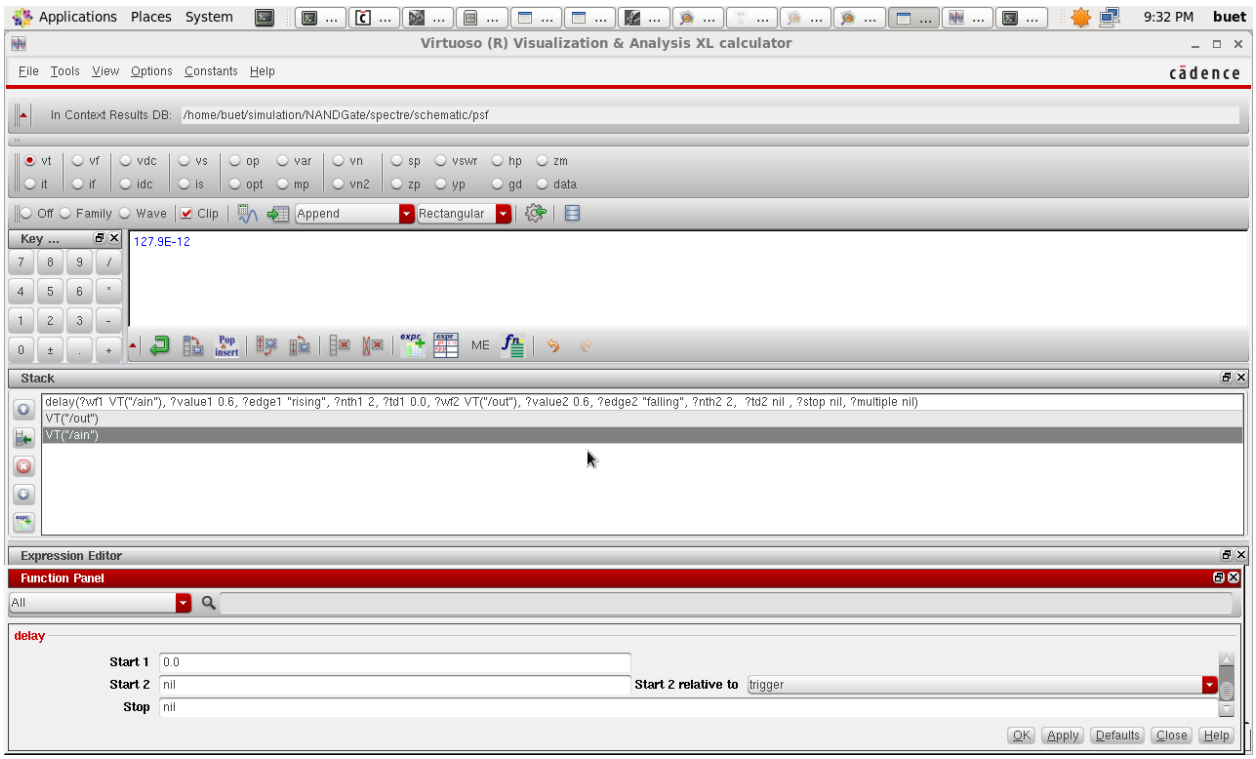

Figure 09: **Delay for p*mos*=240 nm, n*mos*=120 nm.**

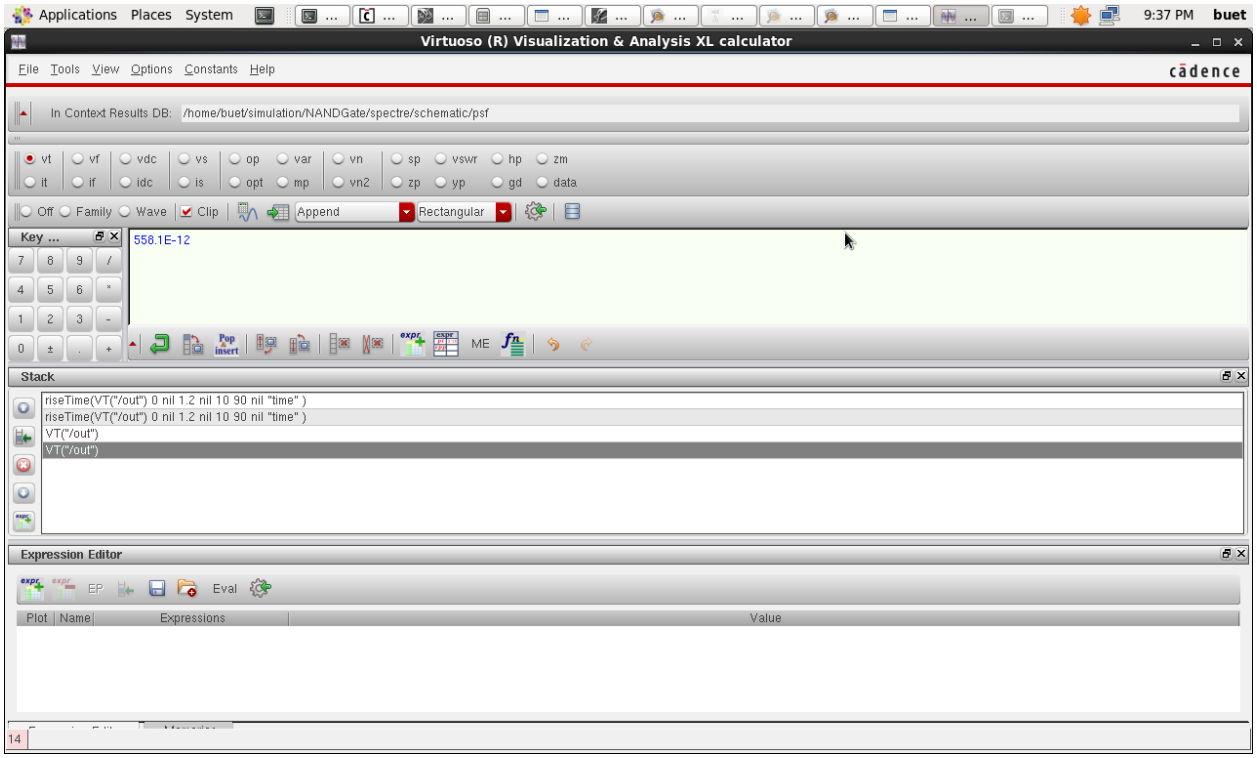

Figure 10: **risetime for p*mos*=240 nm, n*mos*=120 nm.**

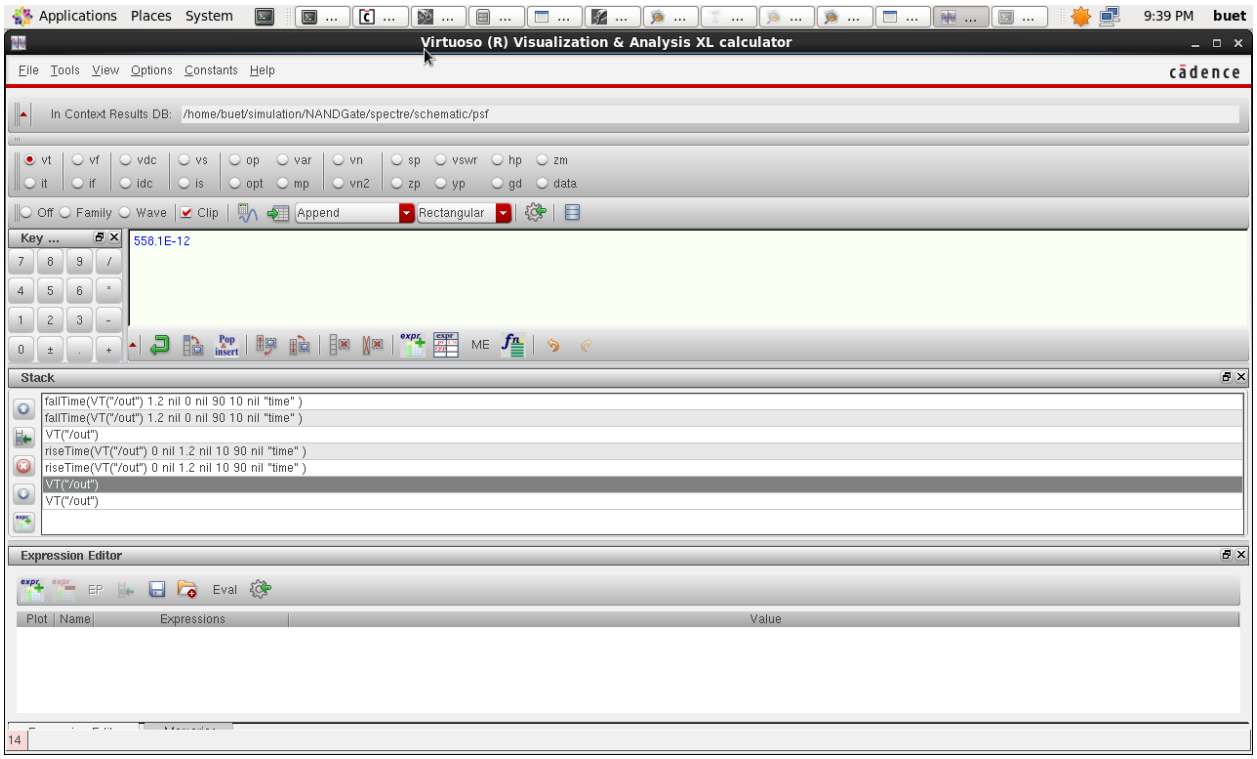

Figure 11: **Falltime Output wave forms for p*mos*=240 nm, n*mos*=120 nm.**

PROPAGATION DELAY:

For pmos=240 nm , nmos=120 nm:

Propagation delay rise time - 127.9 E-12
Propagation delay fall time - 127.9 E-12
Rise Time : 558.1 E-12; Fall Time : 558.1 E-12

TOOLS USED:

1. Cadence Virtuoso.
2. Virtual Box.

CONCLUSION:

We became familiar with Cadence Software through this project. We chose the essential specifications and waveforms before designing the schematic for a 2-input NAND gate. We created a truth table and contrasted the simulated outcome with it.

REFERENCES:

1. Lab Manual.
2. Cadence Tutorial.