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PROJECT PART 1: DESIGNING OF FOLDED CASCODE OTA

COURSE CODE: ECE-GY 6403

FUNDAMENTALS OF ANALOG INTEGRATED CIRCUIT DESIGN

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Objective:

The objective of this project is to design a Folded Cascode Operational Transconductance Amplifier (OTA) and its bias voltage circuit. The requirements are as follows:

- $Gain$ > 70 dB
- $f3dB$ > 10 kHz
- $Slew\ Rate$ > 30 $V/\mu s$
- $Phase\ Margin$ > 60°
- $Power\ consumption$ < 200 µW
- VDD = 1.2 V
- CL = 2 pF

Circuit Design:

By first examining the provided specifications, we identified the boundaries of our intended project.

For instance, we determine the lowest output current required to achieve a Slew Rate larger than the specified value with the specified capacitance.

$I_{out,min}$ = Slew Rate × Capacitance = 60µA
Which flows through M9 and M10 transistors

Similarly, the maximum output current through each of those top transistors will be:

$I_{9,10,max}$=1/2$P_{max}V_{dd}$=1/2x200x1.2=83.33 μA

To make sure that our designed amplifier works well, we will first need to be assured that the transistor MB provides at least the same current as M9 and M10. It is to be noted that transistor MB works as a current source load for the input transistors M1 and M2.

The following design approach was followed as we moved forward to the completion of the project:

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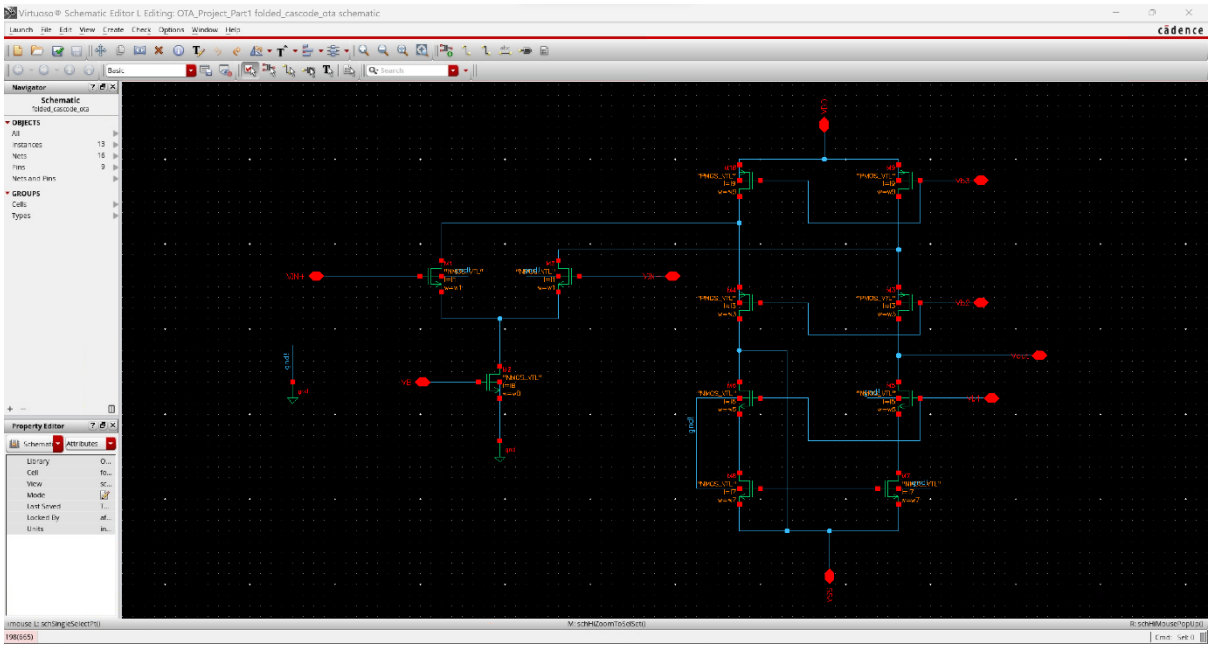

FIG: FOLDED CASCODE OTA SCHEMATIC.

The above configuration has a gain given by:

$$A = gm1(gm3ro3(ro9||ro2)) \;||(gm5ro5(ro7||ro8))$$

Here, A = Gain of the amplifier
gm = transconductance of the transistor

We assumed that all the transistors were biased at the edge of saturation, and the bias voltages were set, assuming the transistor was of the same shape and size. The handmade calculations to derive the values are attached at the end of this report.

Different values were put in, adjusting the transistor dimensions and bias voltages to meet the specifications in the operating region, as we were unable to produce a good output voltage swing, specific gain, and bandwidth through DC, AC, and transient analyses of the circuit.

We advanced gradually, changing the dimensions of the transistor widths and their biasing voltages as required to increase the transconductance, consequently, final output gain without the change of source current.

TRANSISTOR NAMES	TRANSISTOR VALUES (WL)	BIAS VOLTAGE NAMES	BIAS VOLTAGE VALUES
M2, M1	15 µm / 0.20 nm	Vb1	670 mV
M4, M3	105 µm / 0.5 µm	Vb2	720 mV
M6, M5	10 µm / 0.5 µm	Vb3	655 mV
M8, M7	85 µm / 0.5 µm	VB	580 mV
M10, M9	85 µm / 1 µm		
MB	127um/ 1um		

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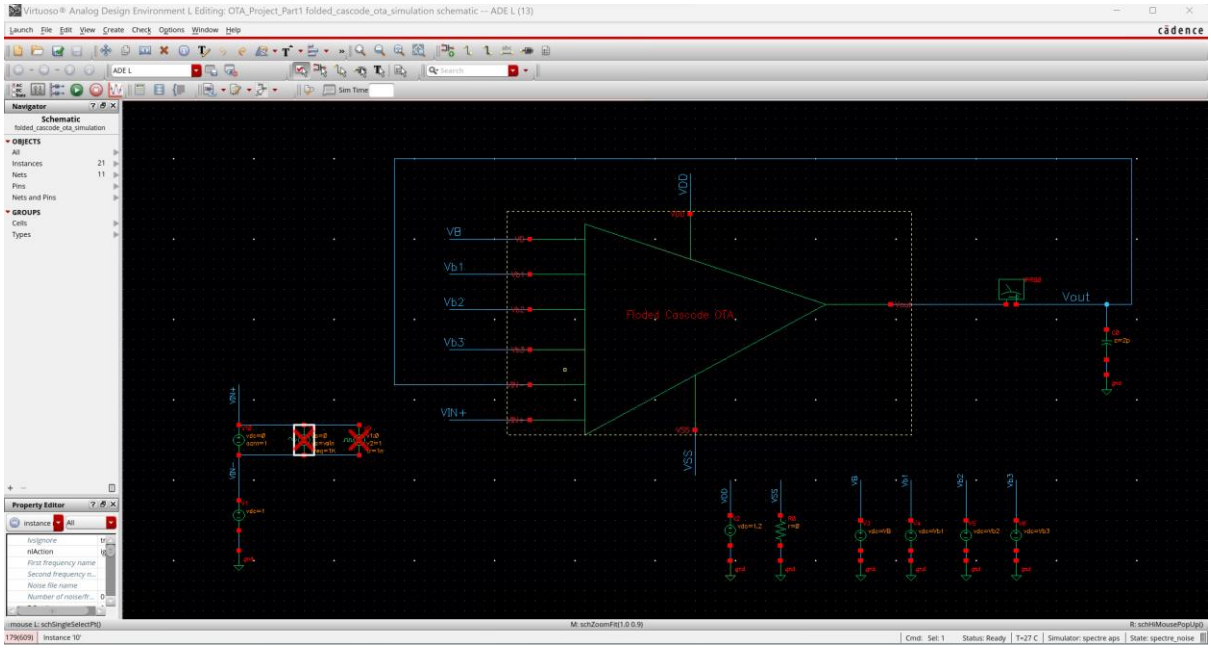

FIG: TEST BENCH FOR SIMULATING THE OTA PARAMETERS.

AC/STB Simulation for Loop Gain and Phase Margin:

We have performed the following stb simulation to find the Gain (in dB20), Phase Margin (PM). The following are the stb simulation parameters, along with the Loop gain (in dB20). From the simulation, we can see that the

Loop gain (in dB20) = 70.0501 dB (Requirement: Loop gain > 70 dB)
Phase Margin (PM) = 61.99 deg (Requirement: PM>60 deg)
3dB Bandwidth = 17.19KHZ

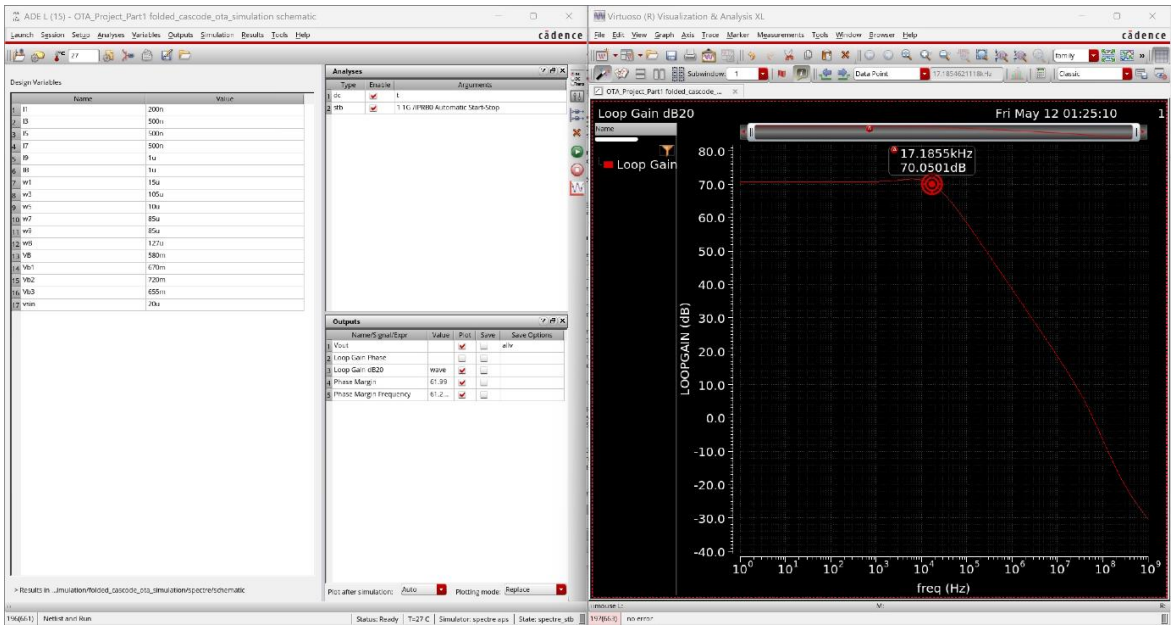

FIG: STB SIMULATION

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Slew Rate Calculation Using Step Input:

The slew rate is defined as the change in output voltage per unit of time and is measured between 10% to 90% of the output signal limits.

In between 10% and 90% of the rail voltage, VDD, we consider the slew rate to be linear. The slew rate is nonlinear when transistors fall out of the saturation region or high currents flow.

The slew rate from this Folded Cascode OTA is:

Slew Rate = 48.39 MV/sec

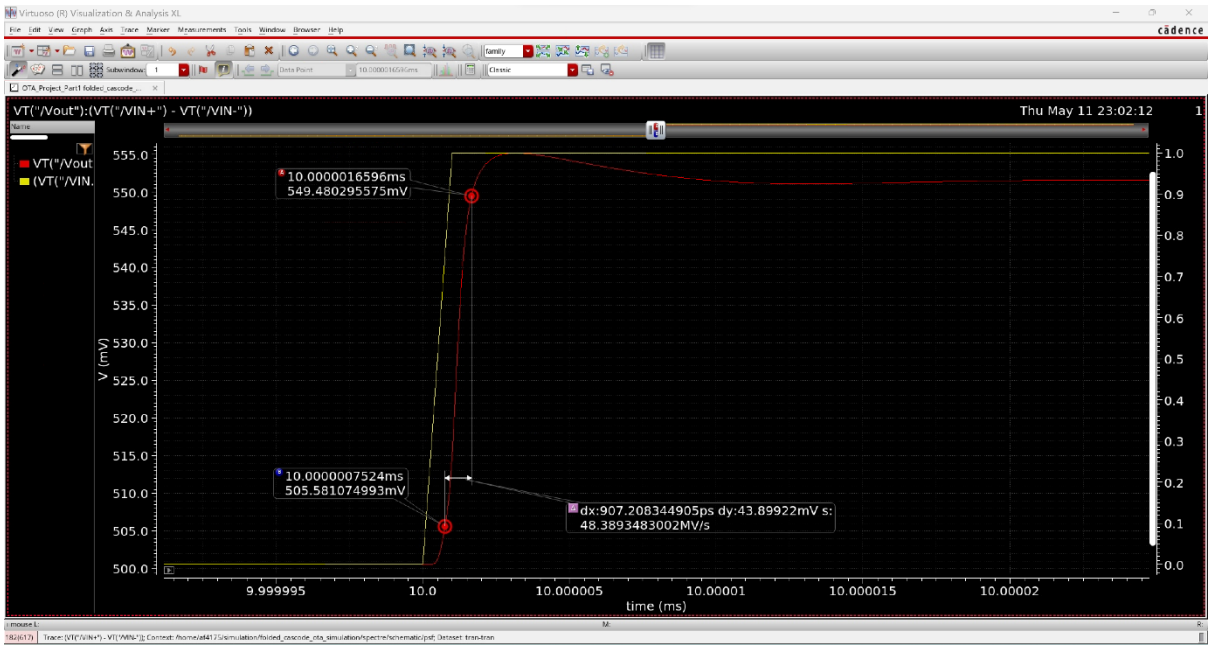
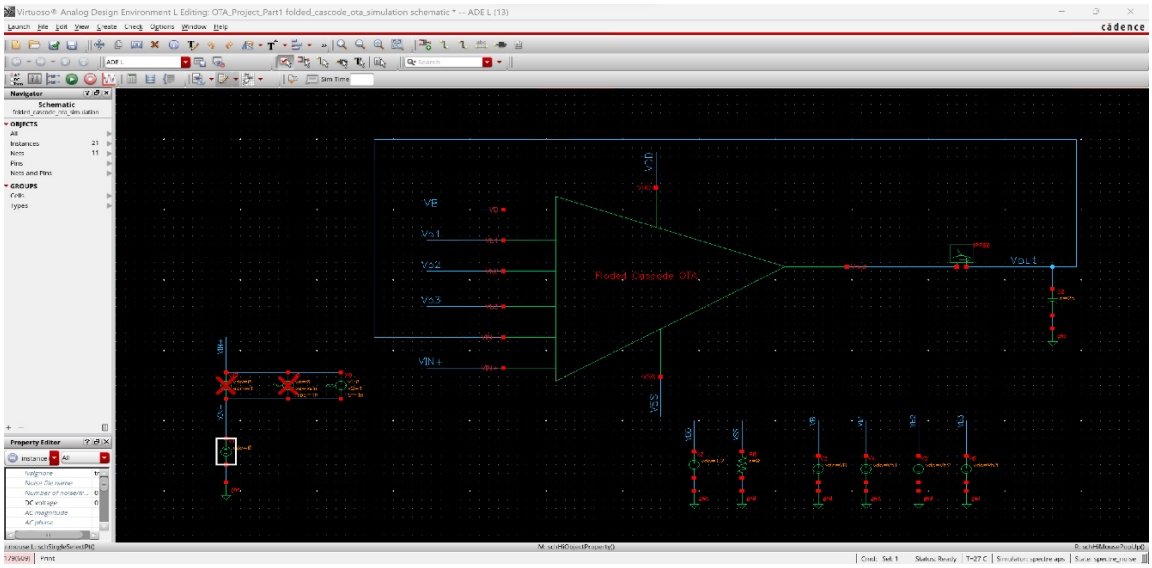


FIG: GRAPH FOR FINDING SLEW RATE.

The following circuit configuration was used to calculate the slew rate of the circuit with the following parameters:



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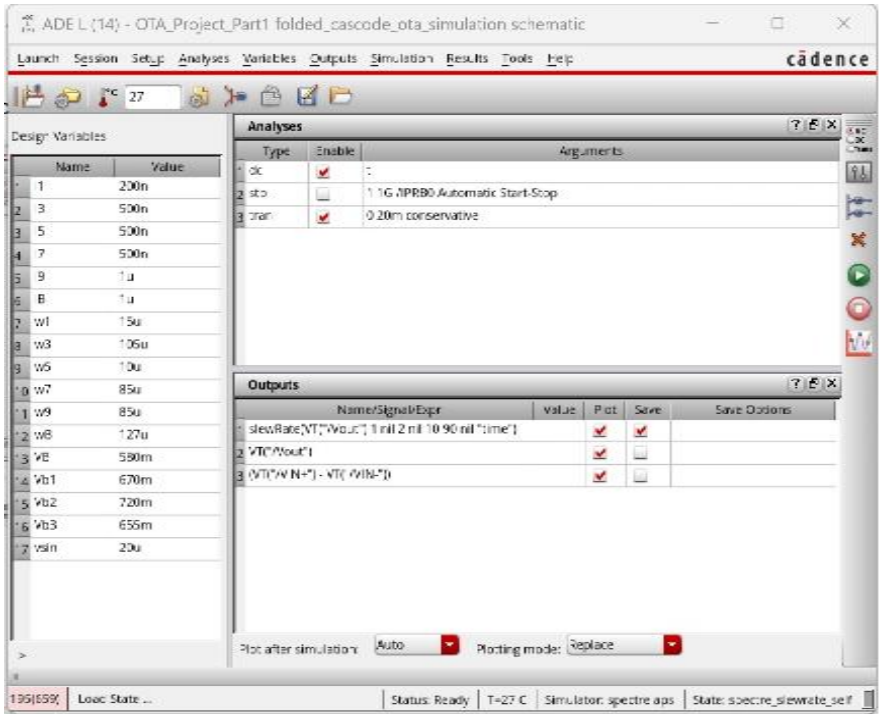

FIG: SLEW RATE CALCULATION PARAMETERS IN ADEL WINDOW.

Noise Analysis:

To calculate the input-referred noise of the circuit, we have used noise analysis. The noise summary and the input-referred noise of the circuit are given below:

Input Referred Noise = 0.00535mW

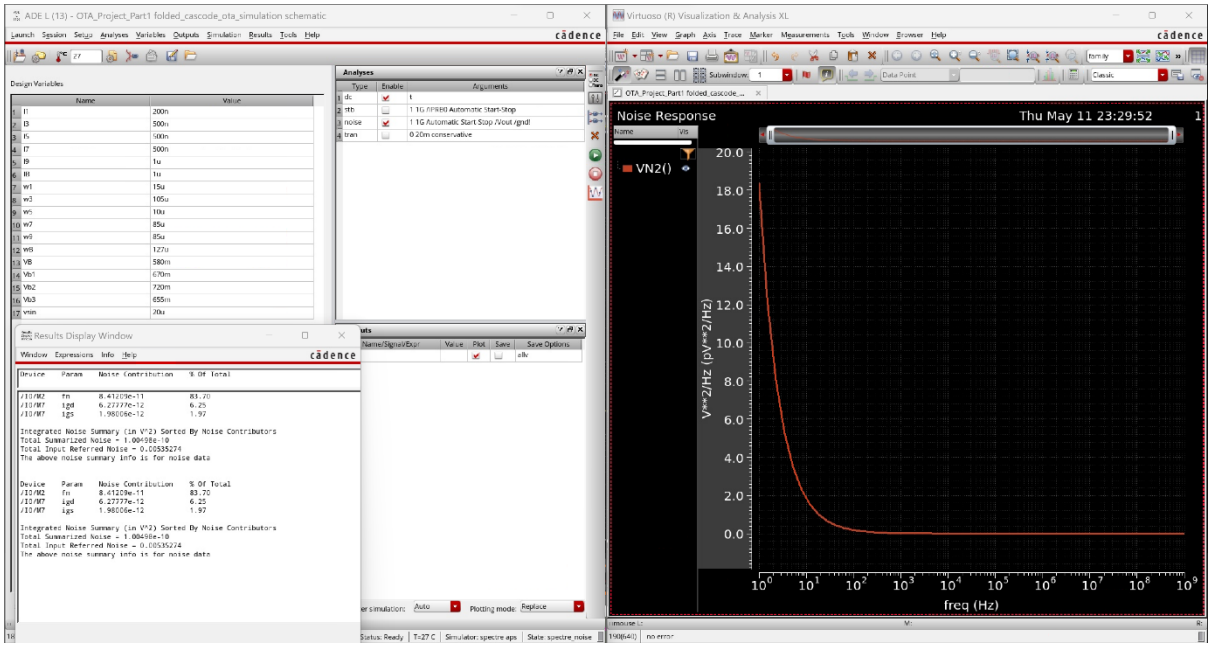

FIG: NOISE ANALYSIS WITH NOISE SUMMARY.

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POWER CONSUMPTION:

To find the power consumption of the system, we have used the DC analysis. From the DC analysis, we have seen that the circuit's.

Power consumption = 1.275mW = 127.5uW (Requirement Power Consumption<200uW)

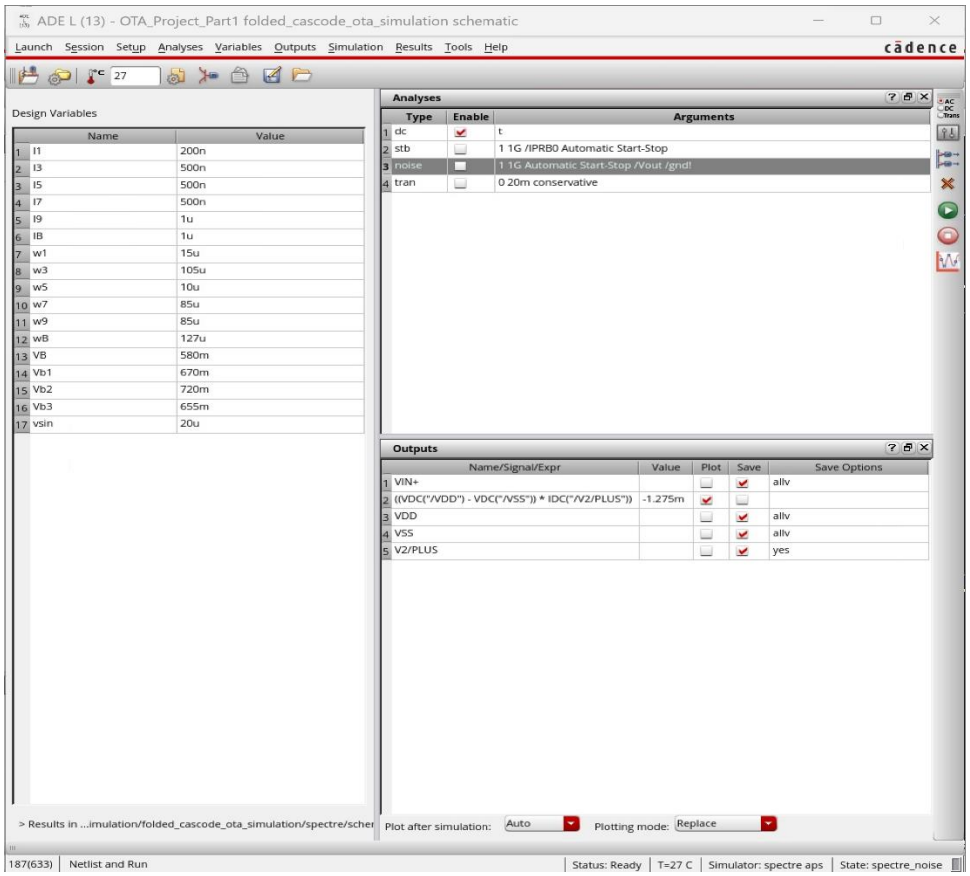

FIG: POWER CONSUMPTION CALCULATION

Outcomes:

We have achieved the outcomes after going through the experiment:

- DC Gain: 70.0501 dB
- 3dB Bandwidth: 17.19KHz
- Slew Rate: 48.39 MV/s
- Phase Margin: 61.99 deg
- Power Consumption: 127.5uW

Parameters	Hand Calculated Values	Simulated Values
I_D at M_{10} & M_9	80 µA	80 µA
I_D at M_B	60 µA	60 µA
V_{b1}	890 mV	670 mV
V_{b2}	392 mV	720mV
V_{b3}	645 mV	655 mV
V_B	≥ 600 mV	580 mV

A_V	≈ 72.23 dB	70.0501 dB
f_{3dB}	≈ 19.4 kHz	17.19 kHz
Phase margin	180+ ∠A(jω)	61.99
Slew Rate	≈ 40 V/µs	48.39 V/µs

Discussion:

After careful observation from the above comparison table, we see variations in the simulation results and calculated values. One of the main reasons behind this can be the experimental parameter values that have played a pivotal role in putting the transistor into more of an unwanted operating region rather than our intended one. Also, it should be noted that while doing the simulations, we considered using an ideal transistor with channel length modulation only. For simplicity, we ignored the other important parameters, such as body effect and transistor nonlinearity. But most importantly, a reasonable estimation of a general transistor behavior was made within finite limits between simulations and calculations utilizing revisions in the calculations and simulation parameters.

Conclusion:

A step-by-step design procedure for a Folded Cascode OTA is explained in this report. We started with some requirements and, in the end, were able to satisfy those, both theoretically and through simulation. Moreover, a comparison chart is drawn to verify the outcomes.

Acknowledgements:

This project work would not have been possible without the tremendous efforts provided by the course instructors and teaching assistants in developing the foundational background knowledge upon which this project stands.

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Hand Calculations:

Given, requirements:

DC Gain > 70 dB

ω_{3dB} > 10 kHz

Slew Rate > 30 V/μs

Phase Margin > 60°

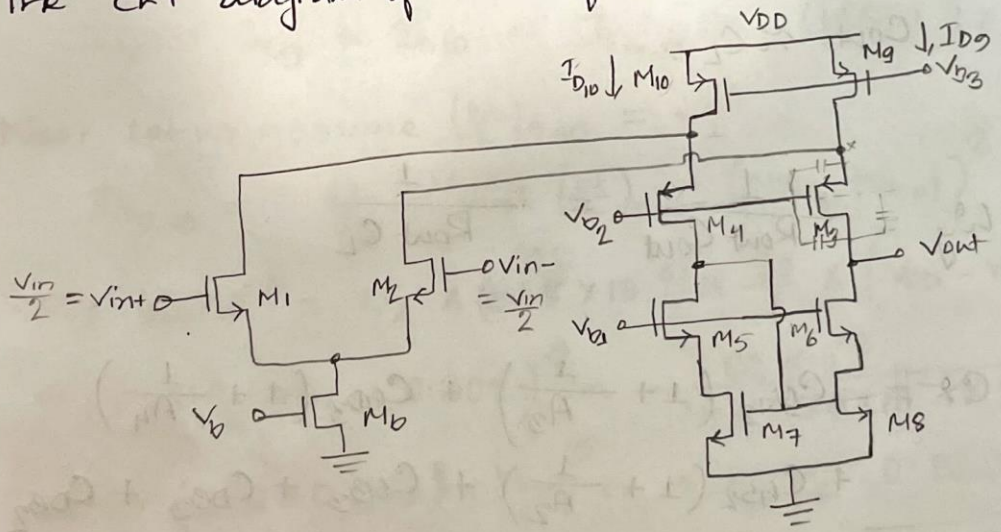
Power Consumption < 200 μW

For this configuration to achieve 70 dB gain

V_{DD} = 1.2 V

C_L = 2 pF

The CKT diagram of the folded Cascode Amplifier



We know that,

Gain, $A_V = -G_m R_{out}$

Now,

$$G_m = \frac{I_{out}}{V_{in}} = -g_{m1}$$

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Now,

$$R_{out} = R_{up} \parallel R_{down}$$

$$= (g_{m3} r_{o3} (r_{o9} \parallel r_{o2})) \parallel (g_{m5} r_{o5} (r_{o7} \parallel r_{o8}))$$

Thus,

$$A_V = -g_{m1} \left[(g_{m3} r_{o3} (r_{o9} \parallel r_{o2})) \parallel (g_{m5} r_{o5} (r_{o7} \parallel r_{o8})) \right]$$

Now to find the transfer function we do the following

$$C_{out} = C_L + C_p \quad \text{as } C_p \ll C_L$$

$$\therefore C_{out} \approx C_L$$

Now,

$$\therefore \omega_y = \frac{1}{R_{out} C_{out}} = \frac{1}{R_{out} C_L}$$

Here,

$$C_x = C_{GB_3} \left(1 + \frac{1}{A_3}\right) + C_{GD_3} \left(1 + \frac{1}{A_4}\right) + C_{GS_2} \left(1 + \frac{1}{A_2}\right) + C_{SB_3} + C_{DB_3} + C_{DB_2}$$

$$R_x = \frac{1}{g_{m3}} \parallel r_{o4} \parallel r_{o2} \approx \frac{1}{g_{m3}} \quad \left(\text{As } \frac{1}{g_{m3}} \ll r_{o4} \parallel r_{o2}\right)$$

$$\therefore \omega_x = \frac{1}{R_x C_x} = \frac{g_{m3}}{C_x}$$

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∴ Transfer function:

$$A(s) = \frac{1}{(1+s/\omega_y)(1+s/\omega_x)}$$

To find the aspect ratio (W/L):

If we consider power consumption to be

$$P = 192\ \mu W$$

Then,

$$I_D = \frac{P}{V_{DD}} = \frac{192\ \mu W}{1.2\ V} = 160\ \mu A$$

As M_9 & M_{10} ~~has~~ is similar thus $\left(\frac{W}{L}\right)_9 = \left(\frac{W}{L}\right)_{10}$

$$I_{D9} = I_{D10} = I_{D9,10} = (160/2) = 80\ \mu A$$

Now, let us assume $\left(\frac{W}{L}\right)_{9,10} = \frac{20}{1}$

$$I_{D9,10} = 1/2\ \mu_p C_{ox} \left(\frac{W}{L}\right)_{9,10} \left(V_{SG_{9,10}} - |V_{THP}|\right)^2$$

or, $80 \times 10^{-6} = 1/2 \times (126 \times 10^{-6}) \times \frac{20}{1} \times \left(V_{DD} - V_{b3} - |V_{THP}|\right)^2$

or, $\left(1.2 - V_{b3} - 0.302\right)^2 = \frac{80 \times 10^{-6}}{1/2 \times 126 \times 10^{-6} \times \frac{20}{1}}$

or, $\left(1.2 - 0.302 - V_{b3}\right)^2 = 0.0635$

or, $0.898 - V_{b3} = \sqrt{0.0635}$

or, $V_{b3} = 0.898 - 0.252$

or, $V_{b3} = 0.645$

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Now,

$$V_{ov9,10} = V_{SG1} - |V_{thp}|$$
$$= V_{DD} - V_{b3} - |V_{thp}|$$
$$= (1.2 - 0.645 - 0.302)\ V$$
$$= 0.253\ V$$

For transistor M_8 & M_7 at the edge of saturation

$$V_{ov7,8} = V_{GS8} - V_{thn}$$

Let us assume $\left(\frac{W}{L}\right)_{7,8} = \frac{10}{1}$

Now,

$$I_{D7,8} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_{7,8} (V_{GS8} - V_{thn})^2$$

or, $(80 \times 10^{-6}) = \frac{1}{2} (265 \times 10^{-6}) \times \left(\frac{10}{1}\right) (V_{GS8} - 0.322)^2$

or, $(V_{GS8} - 0.322)^2 = \frac{80 \times 10^{-6}}{\frac{1}{2} \times 265 \times 10^{-6} \times \frac{10}{1}}$

or, $V_{GS8} - 0.322 = \sqrt{0.0604}$

or, $V_{GS8} = 0.322 + 0.246 = 0.568\ V$

Now, for M_5 & M_6 to be at the edge of saturation

~~$V_{b1} = V_{G5}$~~ $V_{GS8} = V_{b1} - V_{thn}$

or, $V_{b1} = V_{GS8} + V_{thn}$

or, $V_{b1} = 0.89\ V$

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For, M_3 & M_4 to be in saturation region edge

$$V_{ov3,4} = V_{b_{13}} - |V_{Tnp}|$$

$$\text{or, } V_{ov3,4} = (V_{DD} - V_{ovg,10} - V_{b_2}) - |V_{Tnp}|$$

$$\text{or, } V_{ov3,4} = 0.947\, V_{b_2} - 0.302$$

$$\text{or, } V_{b_2} = 0.645 - 0.253 = 0.392\text{V}$$

Now,

$$V_b \approx 700\text{mV}$$

Here,

$$r_{o1} = r_{o2} = 357587.47\ \Omega$$

$$r_{o3} = r_{o4} = 322076.55\ \Omega$$

$$r_{o5} = r_{o6} = 1412096\ \Omega$$

$$r_{o7} = r_{o8} = 1212427.2\ \Omega$$

$$r_{o9} = r_{10} = 290601.48\ \Omega$$

Now,

$$r_{o9} \parallel r_{o2} = 160317\ \Omega$$

$$r_{o7} \parallel r_{o8} = r_{o7}$$

$$\therefore g_{m3} = \sqrt{2\mu_p C_{ox} \left(\frac{W}{L}\right)_{4,3} \times I_{D3,4}} = \sqrt{2 \times 126 \times 10^{-6} \times 10 \times 40 \times 10^{-6}}$$

$$= 3.17 \times 10^{-4}\ \text{A/V}$$

$$\therefore g_{m5} = \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right)_{5,6} I_{D5,6}} = \sqrt{2 \times 265 \times 10^{-6} \times 10 \times 40 \times 10^{-6}}$$

$$= 4.6 \times 10^{-4}\ \text{A/V}$$

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$\therefore R_{down} = g_{m5} r_{o5} r_{o7}$

$= 4.6\times10^{-4} \times 1.41 \times 10^{3}$ (struck)

$= (4.6\times10^{-4} \times 1412019.6 \times 1212427.2)\ \Omega$

$= 787506692.7\ \Omega$

$\therefore R_{up} = g_{m3} r_{o3} (r_{o1} \| r_{o2})$

$= (3.17\times10^{-4} \times 322076.55 \times 160317)\ \Omega$

$= 16368087.77\ \Omega$

$\therefore R_{out} = R_{up} \| R_{down} = 5316955.781$

$= 7514466696\ \Omega$ (struck)

$\therefore g_{m1} = \sqrt{2 \mu_n C_{ox} \left(\frac{W}{L}\right)_{1,2} I_D}$

$= \sqrt{2\times265\times10^{-6}\times10 \times \left(\frac{1}{2}\times\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{th})^2\right.}$

$= \sqrt{2\times265\times10^{-6}\times10 \times (0.5\times265\times10^{-6}\times(0.6-0.568-0.322)^2}$

$= \sqrt{2\times265\times10^{-6}\times10\times0.000114325}$

$= 0.0007685\ A/V$

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$$\therefore |A_v| = |-g_{m_1} R_{out}|$$

$$= |-(0.0007685 \times \frac{53169.55 \cdot 781}{7875066 \cdot 4662})|$$

$$= 4086.08$$

$$\therefore 20\log|A_v| = 72.23$$

$$\therefore \text{Slew rate} = \frac{dI_{out}}{C_L} = \frac{80.4A}{2 \times 10^{-12} F} = 40\ V/\mu s$$

$$\therefore \omega_y = \frac{1}{R_{out} C_L} = 19.9\ KHz$$