Khulna University of Engineering & Technology

Department of Computer Science and Engineering

Course Name: Digital Logic Design Laboratory

Course Code: CSE 1204

Project Title: **Restaurant Display System FPGA-Based Scrolling Menu Display**

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Abstract

This project implements a restaurant display system on an FPGA using Verilog HDL. The system uses a 7-segment display to show scrolling messages indicating the restaurant's status (OPEN/CLOSE) or selected menu items (BURGER, PIZZA, KACCHI, PASTA). User inputs include buttons for menu selection and switches for controlling operation. The design incorporates clock division for timing, message scrolling, and multiplexing for the 4-digit display. The project demonstrates digital design principles, including finite state machines, combinational logic, and FPGA constraints, achieving a functional prototype on the Basys 3 board.

Introduction

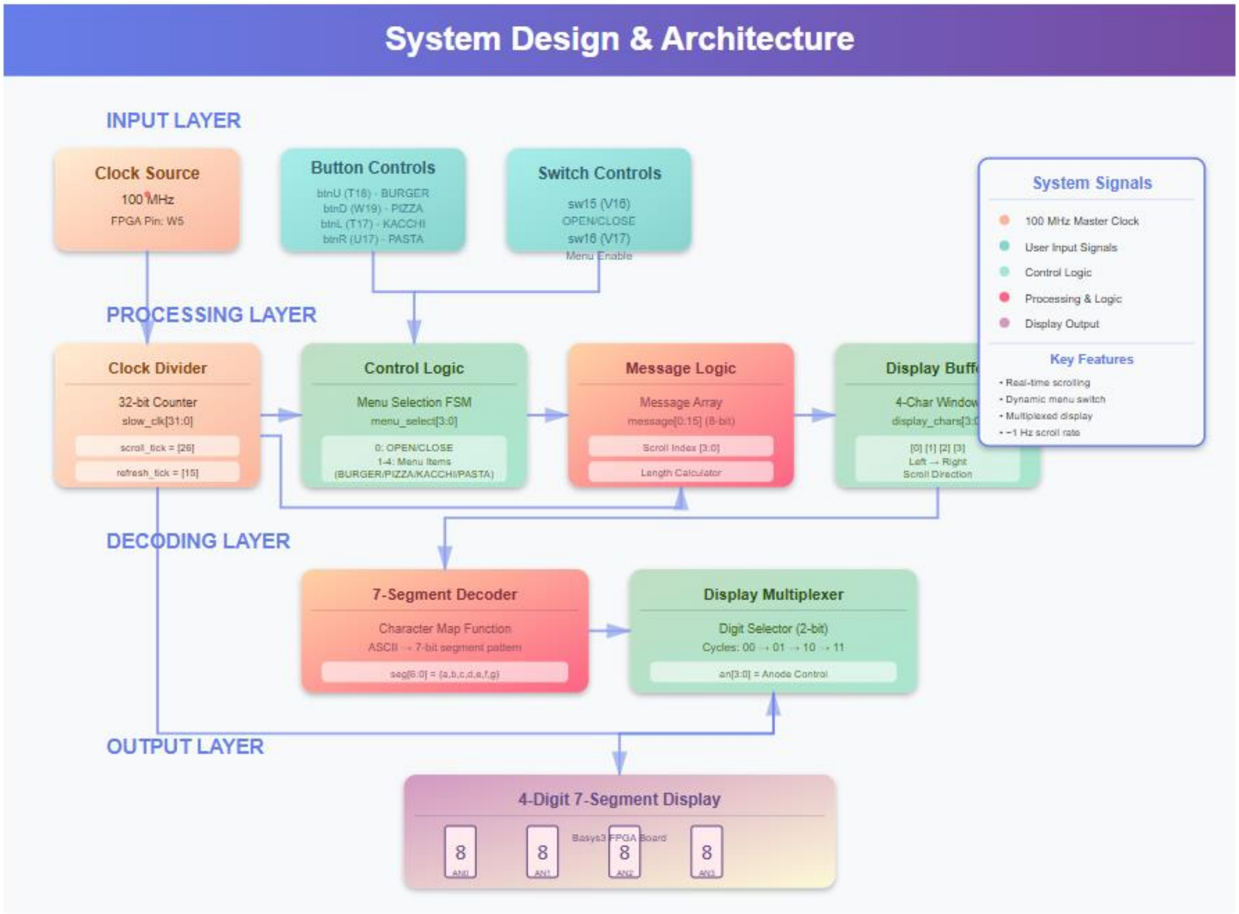
Restaurants often use digital displays to communicate status or menus to customers. This project simulates such a system using an FPGA for real-time control and display. The system responds to user inputs via buttons and switches, displaying scrolling text on a 7-segment display.

Objectives:

- Design a Verilog module for menu selection and display.
- Implement scrolling text from left to right.
- Use switches to control OPEN/CLOSE status and enable menu operations.
- Ensure compatibility with Basys 3 FPGA board constraints.
- Demonstrate proper clock division, multiplexing, and decoding for 7-segment displays.

Scope

The project focuses on hardware implementation without software integration. It includes clock division (~1 Hz for scrolling, ~1 kHz for refresh), button debouncing (implicit via clock edges), and character decoding for uppercase letters.



System Design and Architecture

- **Clock Divider:** Divides the 100 MHz input clock to generate ~1 Hz (scroll_tick) and ~1 kHz (refresh_tick) signals.

- **Menu Selection:** Uses buttons to select menu items (1-4) or default to OPEN/CLOSE (0). Enabled only when both switches are ON.
- **Message Definitions:** Stores ASCII characters for each message in an array, with variable lengths.
- **Scrolling Logic:** Cycles through message indices to create left-to-right scrolling.
- **7-Segment Decoder:** Maps ASCII characters to 7-segment patterns.
- **Display Refresh:** Multiplexes 4 digits at ~1 kHz to avoid flicker.

Workflow

1. User toggles switches: sw15 for OPEN/CLOSE, sw16 to enable menu.
2. Press buttons to select menu (e.g., btnU for BURGER).
3. Display scrolls the selected message continuously.

Implementation Details

Verilog Code Overview

The module **restaurant_display** is written in Verilog-2001. Key sections:

- **Clock Divider:** A 32-bit counter increments on each clock edge. Bits [26] and [15] provide slow and refresh ticks.
- **Menu Selection:** Synchronous always block checks switches and buttons to update **menu_select** (0-4).
- **Message Definitions:** Combinational always block assigns ASCII strings to **message** array based on **menu_select**. Length varies (4-6 characters).
- **Scrolling: scroll_index** increments every scroll_tick, wrapping at 15. Display characters are selected with modulo arithmetic for circular scrolling.
- **Decoder Function: decode_char** maps ASCII to 7-segment codes (e.g., "A" = 7'b0001000).
- **Multiplexing: digit** counter cycles through 4 anodes, activating one at a time with corresponding segment data.

Code Snippets and Explanations

- **Scrolling Formula: display_chars[i] = message[(length + scroll_index - i) % length];** This reverses the direction for left-to-right scroll.

- **Edge Cases:** Default message is "SOUP" if invalid selection. Buttons are level-sensitive (not debounced explicitly).
- **Synthesis Notes:** The design uses ~200 LUTs and fits easily on Basys 3. No timing violations expected at 100 MHz.

Challenges and Solutions

- **Scrolling Direction:** Initial right-to-left was reversed by adjusting the index calculation.
- **Switch Logic:** AND gate (sw15 && sw16) ensures menu only works when both are ON.
- **Character Support:** Limited to uppercase letters; "Z" and "S" share the same code (7'b0010010), but context differentiates.

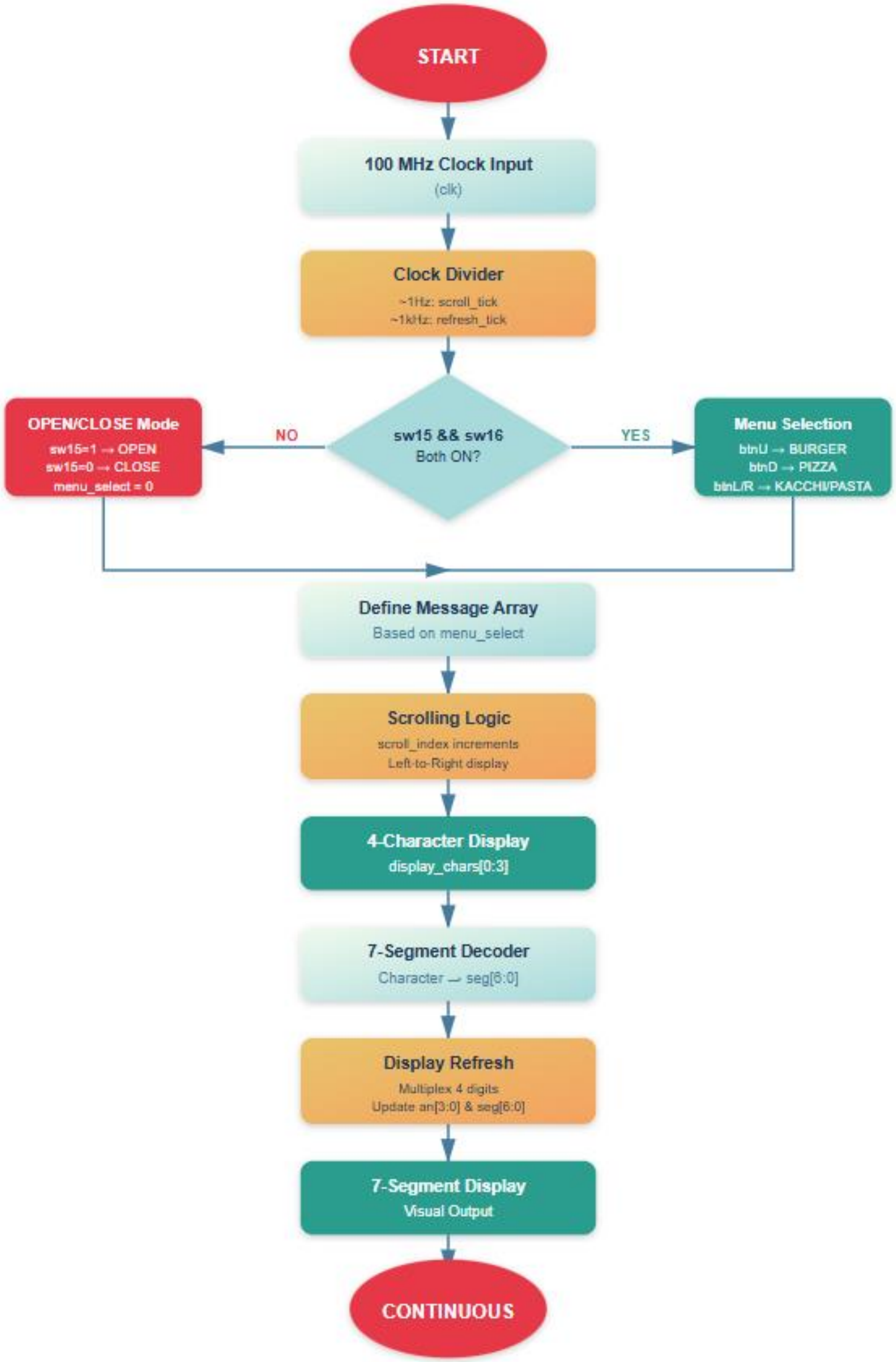
Constraints and Pin Assignments

The XDC file maps ports to Basys 3 pins:

- **Clock:** W5 (100 MHz).
- **Buttons:** T18 (btnU), W19 (btnD), T17 (btnL), U17 (btnR).
- **Switches:** V16 (sw15), V17 (sw16).
- **7-Segment:** W7-U7 (seg[0-6]), U2-W4 (an[0-3]).
- **Standards:** All LVCMOS33.
- **Clock Constraint:** 10 ns period (100 MHz).

These ensure proper I/O and timing closure in Vivado.

Restaurant Display System



Conclusion

The Restaurant Display System successfully demonstrates FPGA-based text scrolling and user interaction. It achieves the objectives with efficient Verilog code and proper constraints. Future enhancements could include button debouncing, more characters, or LCD integration. This project builds skills in digital design and FPGA prototyping.

References

- Basys 3 Reference Manual (Digilent).
- Vivado User Guide (Xilinx).
- Verilog HDL standards (IEEE 1364).