BW, Routing, Stack Up, Silicon Area

Feb 25th, 2020

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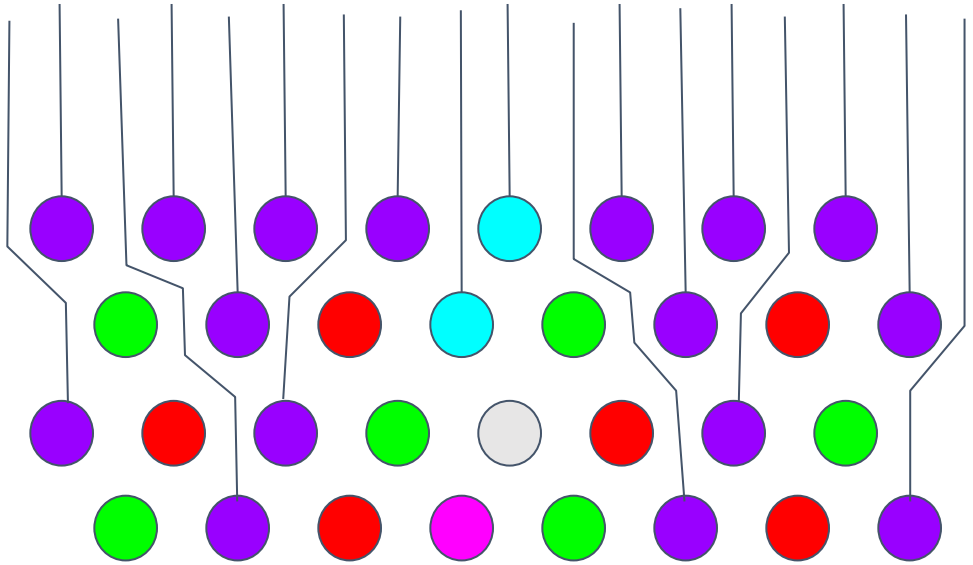
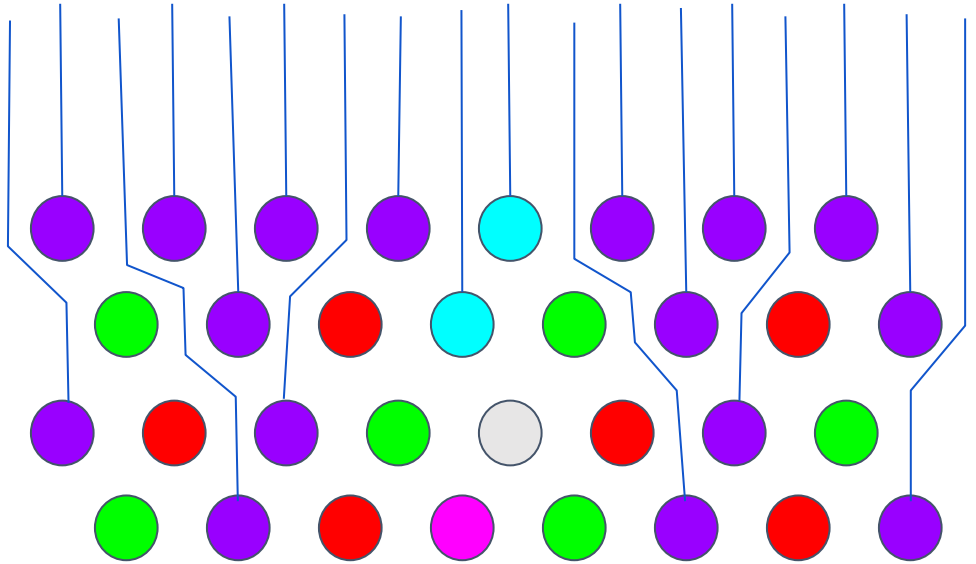
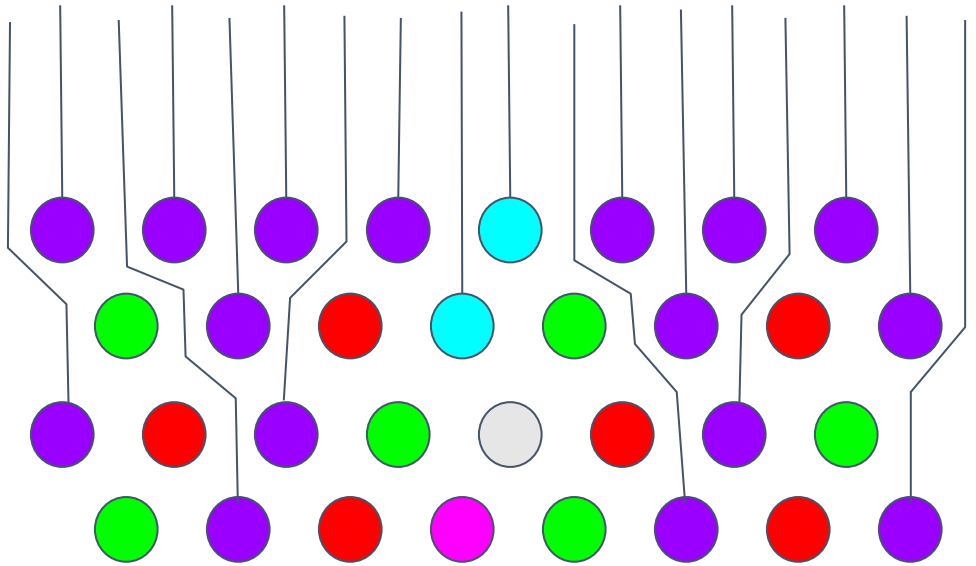
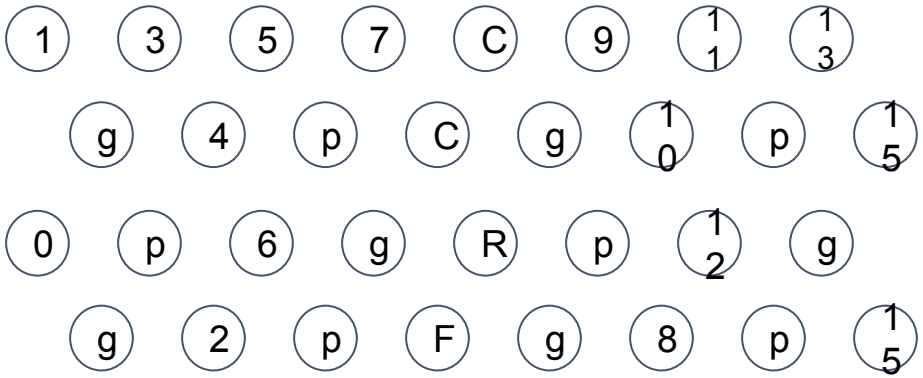
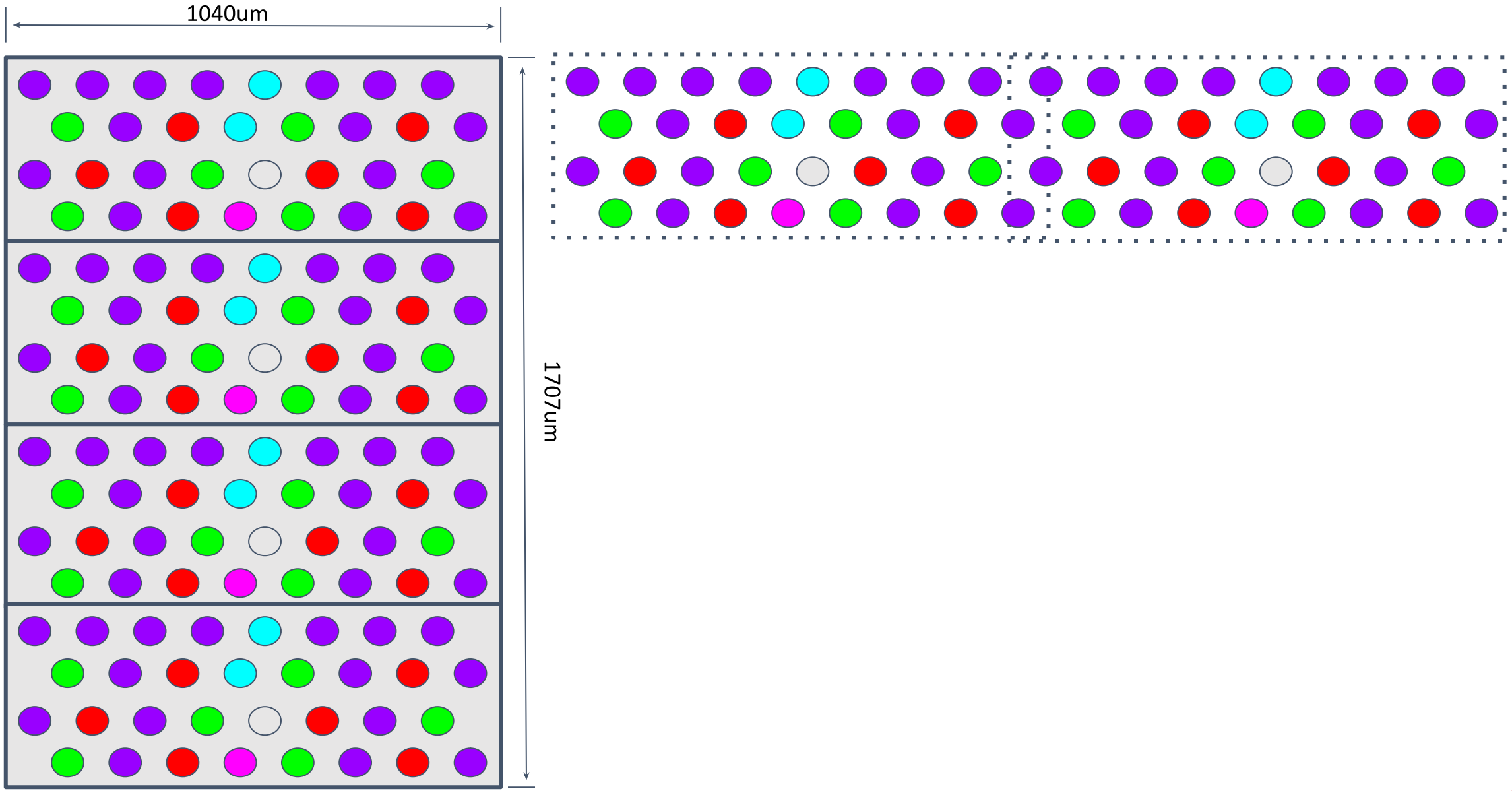
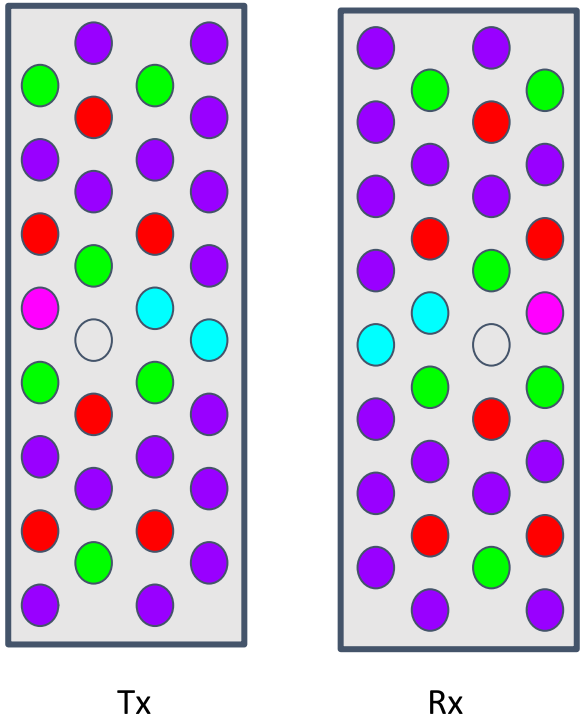


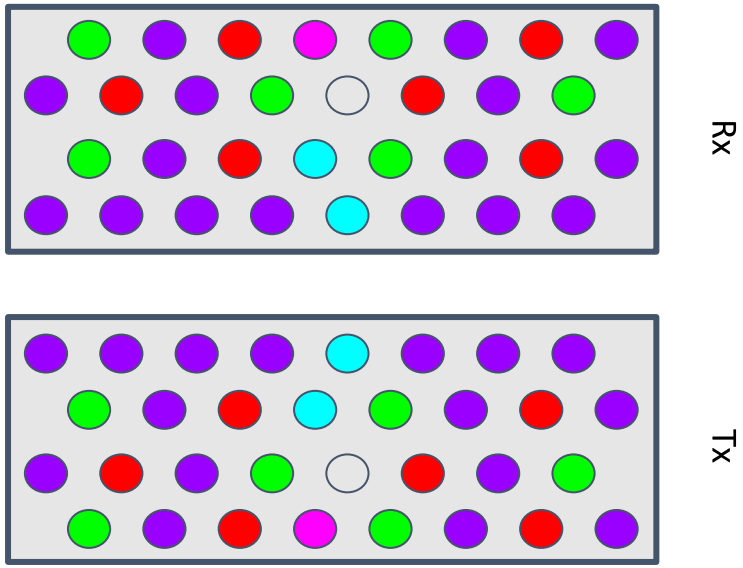


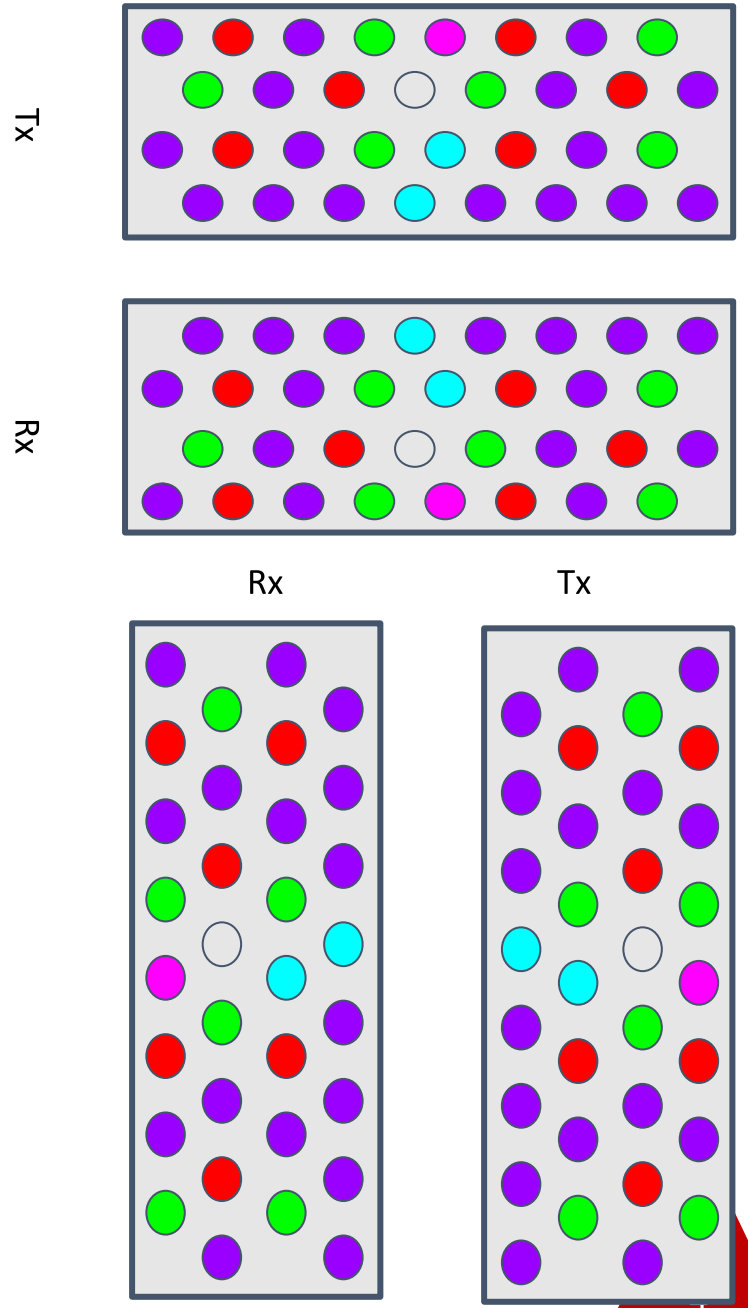



1 3 5 7 C 9 11 13
g 4 p C g 10 p 15
0 p 6 g R p 12 g
g 2 p F g 8 p 15

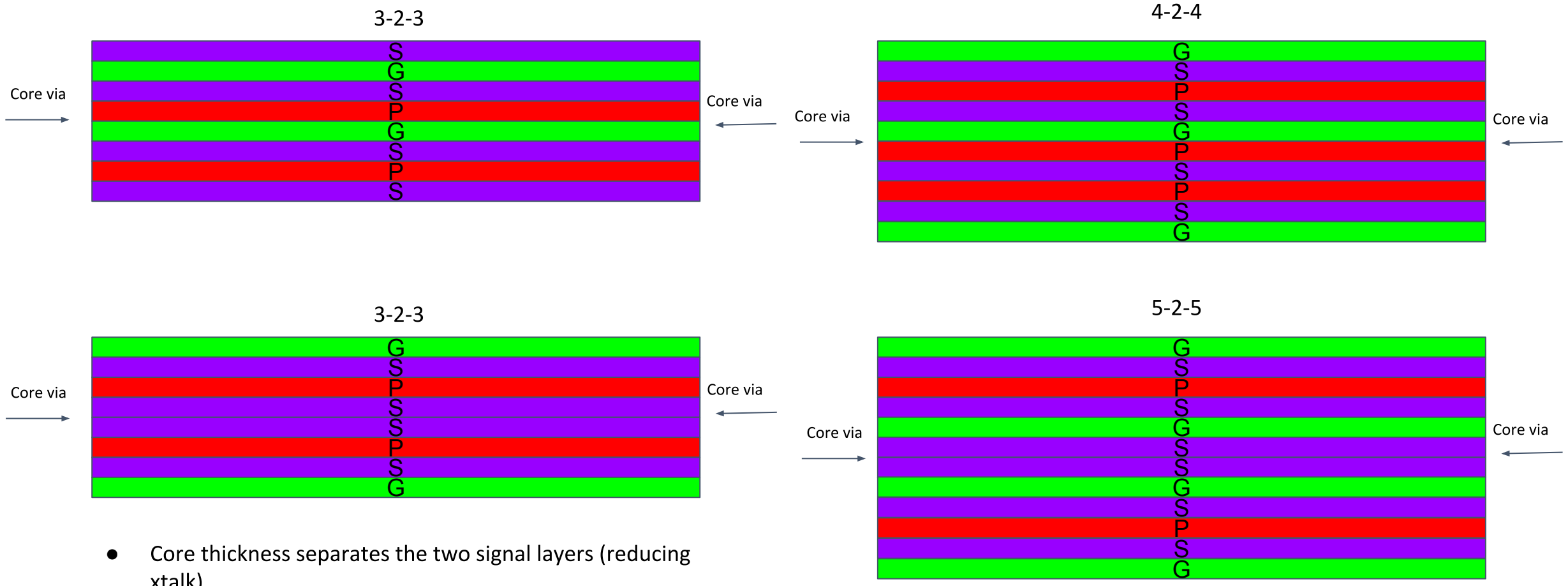

1040um
1707um







Organic Substrate Stack Up Options



- Core thickness separates the two signal layers (reducing xtalk)
- Any routing layers on the bottom will perfom worse than on the top (via down through core vias and back up through core vias)

BW, Routing Layers, Silicon Area

# of lanes/layer	16	16	16	16
# of routing layers	1	2	3	4
# of slices	5	5	5	5
Max DDR speed (Gb/s)	4	4	4	4
Total Bandwidth(Gb/s)	320	640	960	1280
Total Bandwidth (GB/s)	40	80	120	160
Pacakge Stack Up	2-2-2	3-2-3	3-2-3	4-2-4

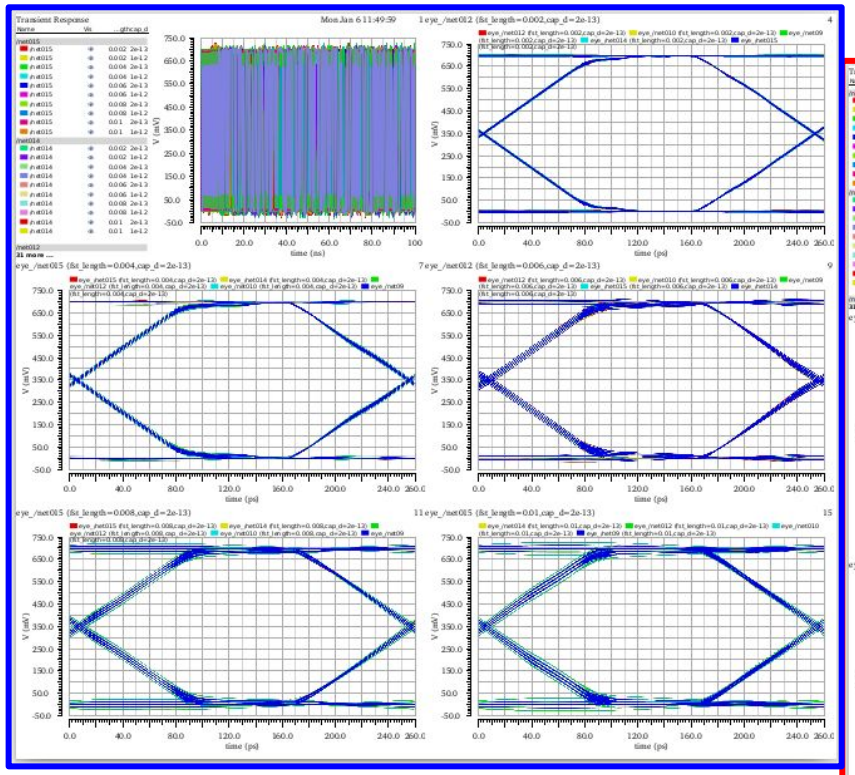
Area per 16 lanes	
W (um)	1040
L (um)	426.75
x pitch (um)	130
y pitch (um)	106.68

Total Silicon Area (sq.mm)	2.2191	4.4382	6.6573	8.8764
W (um)	5.2	5.2	5.2	5.2
L(um)	0.42675	0.8535	1.28025	1.707

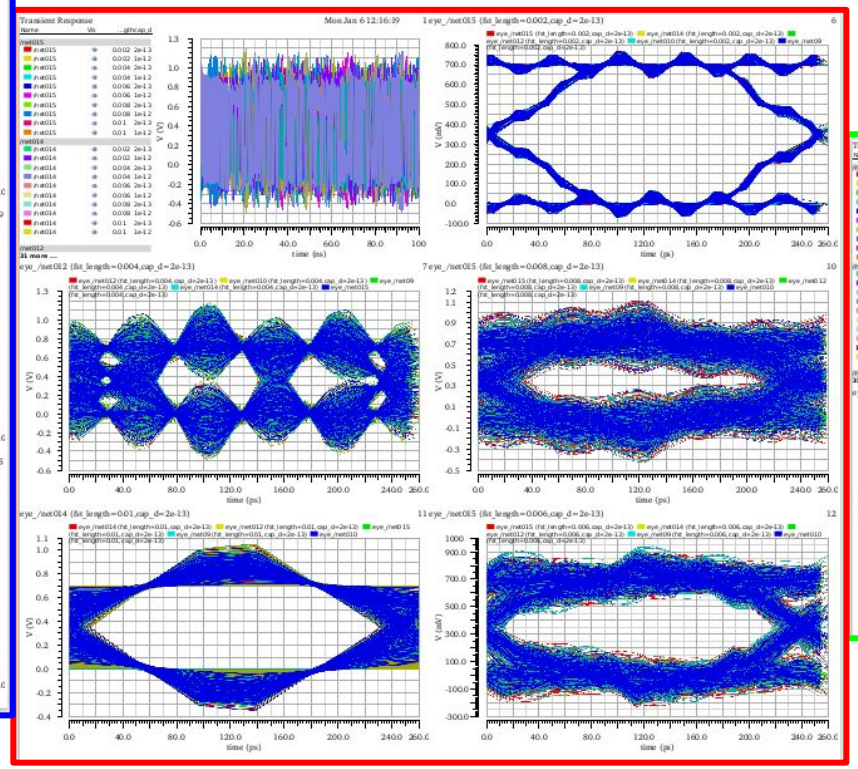
16	16	16	16	16	L1
16	16	16	16	16	L2
16	16	16	16	16	L3
16	16	16	16	16	L4
Stack 4	Stack 3	Stack 2	Stack 1	Stack 0	
Link					

16	Slice

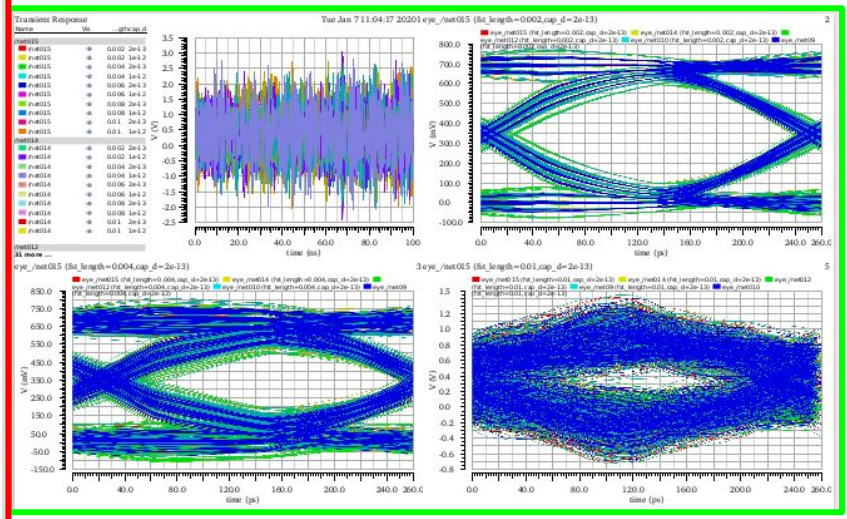
Driver + Channel - What If Analysis



Source Termination (40Ω) + Various Channel Lengths [2mm-10mm]
BW Target (4Gb/s DDR)
Organic Substrate (GX92 material, 25/25)



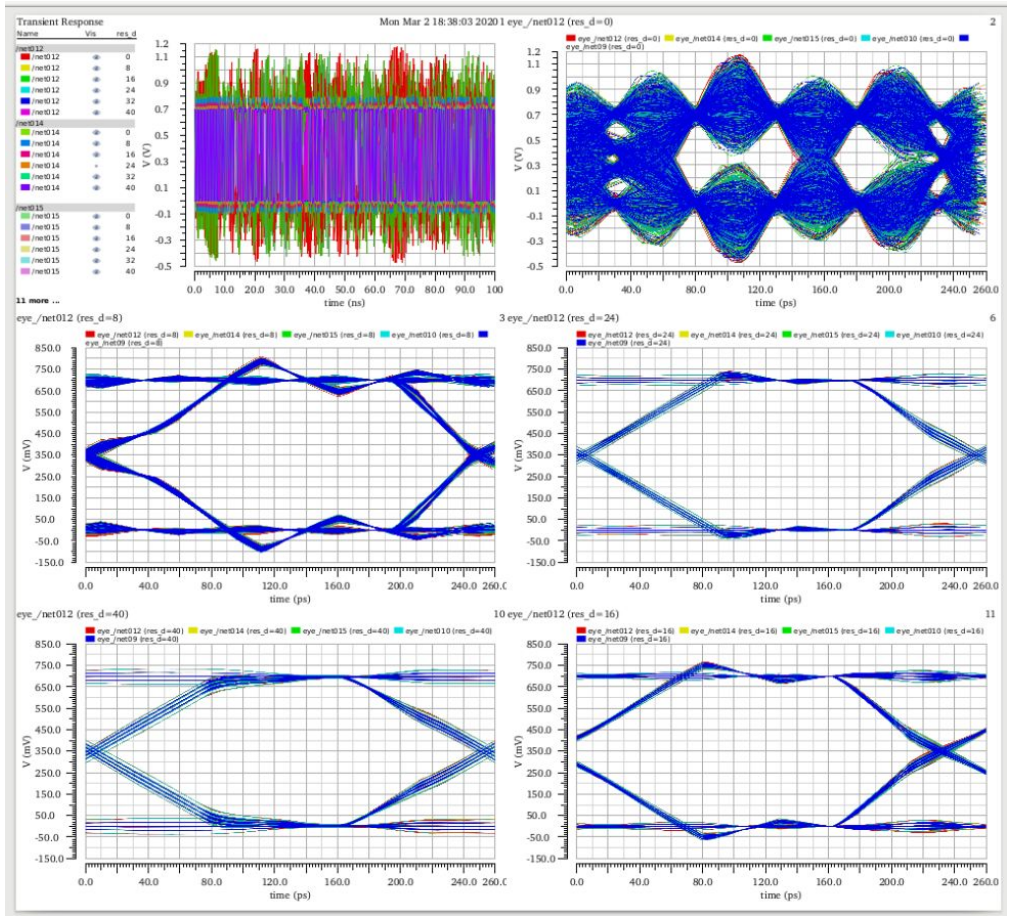
Source Termination (0Ω) + Various Channel Lengths [2mm-10mm]
BW Target (4Gb/s DDR)
Organic Substrate (GX92 material, 25/25)



No Termination + Various Channel Lengths [2mm-10mm] + **Receiver Capacitance [200fF)**
BW Target (4Gb/s DDR)
Organic Substrate (GX92 material, 25/25)

T_r , T_f = 100ps, Bt period = 250ps

Driver + Channel - What If Analysis



Source Termination = 0Ω

Source Termination = 8Ω

Source Termination = 24Ω

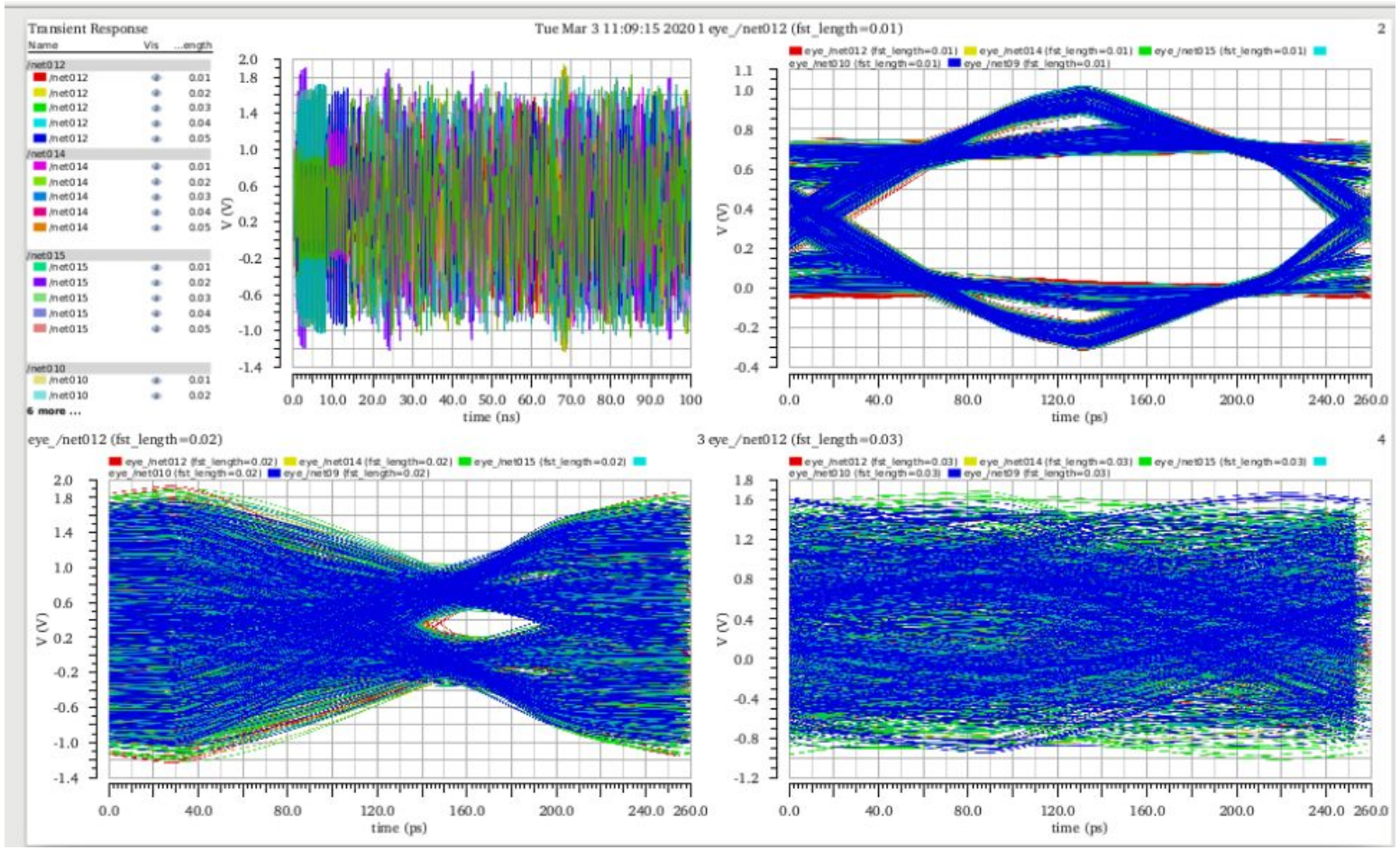
Source Termination = 40Ω

Source Termination = 16Ω

T_r , T_f = 100ps, Bt period = 250ps

Source Termination (0Ω - 8Ω - 16Ω -24Ω-40Ω) + **Channel Length [4mm]** +
Cap_driver = 200fF+ High Impedance Load [10K]
BW Target (4Gb/s DDR)
Organic Substrate (GX92 material, 25/25)

Driver + Channel - What If Analysis



Channel Length = 10mm

Channel Length = 20mm

Channel Length = 30mm

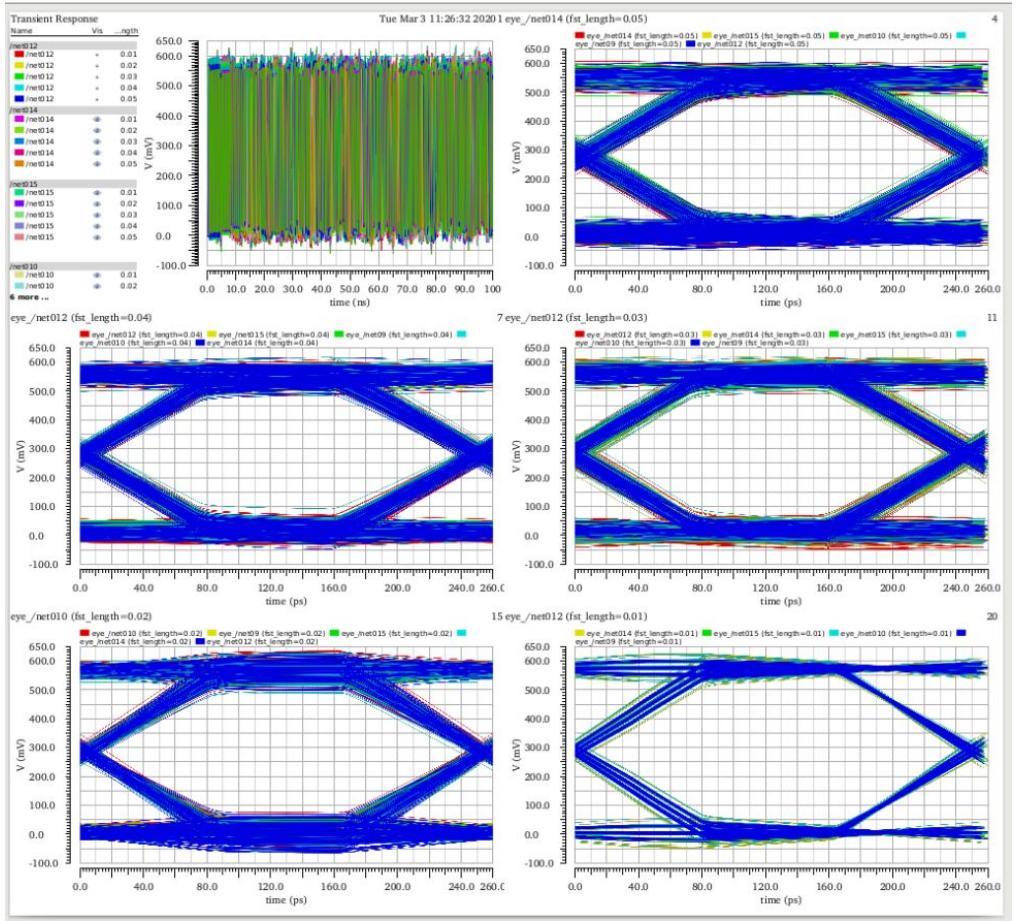
T_r , T_f = 100ps, Bt period = 250ps

Source "Termination" (8Ω) + **Channel Length [10mm-20mm-30mm]** + Cap_driver = 100fF+ Cap_receiver = 100fF+ High Impedance Load [10K]

BW Target (4Gb/s DDR)

Organic Substrate (GX92 material, 25/25)

Driver + Channel - Far End Termination



Channel Length = 50mm

Channel Length = 40mm

Channel Length = 30mm

Channel Length = 20mm

Channel Length = 10mm

T_r , T_f = 100ps, Bt period = 250ps

Source "Termination" (8Ω) + Channel Length [10mm-50mm] + Cap_driver = 100fF+ Cap_receiver = 100fF+ Load Termination [**40Ω**]

BW Target (4Gb/s DDR)

Organic Substrate (GX92 material, 25/25)