Vdd discussion for BoW

Vdd in 0.7 spec

- Where possible BoW IO should reside on the VDD rail to simplify design of chiplets
- and provide current to controller logic from the BoW recommended bump patterns.
- BoW should support a range of voltages from 0.7 nominal to 0.95 nominal (0.66 to 0.99 with standard +/- 5% power supply tolerances) where possible.
- All BoW implementations must support at least 0.9V nominal (0.85 to 0.95V).
- https://github.com/opencomputeproject/ODSA-BoW

Objectives

- BoW aims to span packaging technologies – from regular bumps to micro bumps
- BoW aims to span process nodes
  - Not strain newer nodes
  - If possible go back
- Should we aim to reuse existing PHYs? To minimize verification costs?
- In the following – Company Name => a viewpoint from an engineer at the company. Does not imply company endorsement unless the engineer says so.

Options

Option 1: Leave things as is, current range

Option 2: Choose a new range, same width different center – lower for newer process technology

Option 3: Choose a new range, same width different center – higher

Option 4: Choose a broader range

Option 5: Choose two ranges for interoperation with older technologies

This discussion: zero in on an option with feedback from a wider community

Xilinx: Benefits of new proposal:

- We don't see chiplets in the AIB EMIB/interposer world can be reused for organic substrate so BoW choice of 0.9V doesn't benefits interoperability. BoW and AIB signals definition are different as well.
- We believe BoW spec with following characteristics can greatly accelerate chiplets ecosystem buildup:
  - Available IP and proveness, Ease of design, Low BOM Cost, Device ecosystem and Test infrastructure
  - Preferably, Dual- or Multi-role enables industry support without "dedicated cost" to it if the interface is unused
    - Especially important in early phase of market adoption, often "chicken-and-egg" situation
  - Roadmap to both higher data rates and lower energy/bits to optimize for different use cases

	BoW (with 0.9V I/O)	BoW using Industry-standard I/Os
Industry-standard I/Os	-	adopt LP-DDRx, DDRx standards I/O
Optimized for organic substrate	Goal is to support both organic and interposer	Y
Roadmap to lower energy/bit Roadmap to higher max data rates	-	Y LP5 VDDQ 0.3V (unterm): 1-4Gbps (short ch) LP5 VDDQ 0.5V required (term): 4-16Gbps (short ch)
Ease of design / Lower design cost	-	Y I/O IPs readily available from multi-vendors
Dual-role possible	-	Y (Chiplets and Memory)
Lower BOM cost	N (need extra 0.9V rail, dedicated usage)	Y (standard rail, dual-role flexibility)
Device availability / maturity timeline		Y (/ soon for latest standards)
Test infrastructure		Readily available, multi-vendors

Open Silicon

From my experience having worked as a circuit designer for a long time in multiple processes it is extremely challenging the get 1.1V tolerant input design on an advanced process.As an example MIPI DSI which is used for display needs a Voh spec of 1.1V of the TX. To design this we had to use stacked thin gate devices to avoid gate oxide breakdown and there were no thick gate devices available and a higher supply voltage for the I/O causing increase in area and power. Point is the standard must draw a line on how far back do you want to support older generation process? If LPDDR is already going for low voltage supply why not start with that ?

Open Silicon

I don’t see why anyone would try to use a D2D PHY as a replacement for HBM PHY.

The two sides of the HBM link are designed on different process and are hooked up by a Silicon Interposer.

So what is the need for D2D PHY in this market?

Where D2D PHY makes a difference is between SOC and non memory peripherals

Point is we need to consider addressing the electrical spec for widest market possible.

Generally the memory vendors find it very difficult to migrate to lower node process and hence a lower voltage

By being compatible to HBM are we not making the D2D PHY restrictive when in fact there does not seem to be a compelling reason to replace the existing HBM PHY with D2D PHY

Open Silicon

The intent to be a “one size fits all” though noble is not practical

The HBM I/O SPEC looks something like below

1.2V I/O voltage +/-5% • 0.75V, 0.85V core voltage +10/-5% at uBump

LPDDR supports a lower voltage.

If we want to support both then it has to be clearly articulated that the D2D PHY I/O voltage is specific to the use case to make sure it is interoperable within standard.

Designing a D2D PHY which works on HBM is not going to be I/O circuit compatible with LPDDR I/O for the very reasons articulated earlier from a circuit point of view

Perhaps we can make the D2D standard for the voltage generic with a caveat stating that the implementation of I/O voltage is specific to the use case

IBM

To weigh in, we should allow for a range of voltages to address present/future technology Vmax. Also, 0.9V and below makes sense for the currently available techs and allows for further reduction likely required by future techs. Forcing I/O to allow for 1.1V is very problematic from a circuit design point and a power standpoint as has been detailed in the discussion.

Xilinx

In the context of HBM IO for D2D, or even LP-DDR for D2D, or any IO definitions, one would need to think in terms of which IOs are considered for inter-operation taking their nominal voltages into account. One would need to look at natural grouping of voltages specified for these IOs and group only the ones that are in the same cluster. We see there being two natural groups

- Group 1 - HBM2/E, LPDDR4, current BoW 0.9v,….. AND
- Group 2- HBM3, LPDDR5, BoW with compatible voltage in this group …….

One can consider a highly flexible IO that can span the two groups, but that should be out side the scope of BoW. Within one group also, one need to pick one inert-operation as a Requried voltage for standardization (more on this below)> So When Bapi mention HBM3, I take it we are talking inter-operation of HBM3 with LPDDR5 with whatever BoW is in this group (by the way our view is that BoW should not define new IO type, but leverage the ones that exist in that group and more focus on re-characterization of those for in-package channel).

- Now for inter-operation, voltage for each group need to be picked, What should be common voltage for group 1, and what should it be for Group 2. Some guiding principles
- If in a group one IO define V1max and V1min and second IO defines V2max and V2 min, then common operating voltage should be no more than the Min(Max V1, MaxV2) or it could be lower, but not lower than the Min of the operating rage of either,
- Lower voltage is better for power. , So go over lower volateg with the Max Min range of intersection of allowed voltages.

- So now For Group 1, seems candidate Required Voltage choice is 1.1 or 0.9.
- For group 2, it could be would be 0.4V or 0.5 (need to analyze – not sure if 0.5 is within tolerance of standard HBM5 IO)

Options

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Option 2: Choose a new range, same width different center – lower

Option 3: Choose a new range, same width different center – higher

Option 3: Choose a broader range

Option 3: Choose two ranges

This discussion: zero in on an option with feedback from a wider community