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signature page of this Agreement shall constitute due and proper execution of this Agreement by the applicable party.

Bunch of Wires Specification

Mark Kuemerle, Ramin Farjad, Behzad Bahador, Bapi Vinnakota (the Open Domain Specif

1. Introduction

The Bunch of Wires (BoW) specification is a very simple, open and interoperable physical interface between any 2 or more chiplets or chip-scale-packages (CSP) on a common package.

1.1. Overview

This specification will describe the BoW interface. The specification also leaves open the possibility of pin-compatible interfaces that operate at higher data rates for increased throughput per chip edge. This specification also describes a terminated mode that operates at increased data rates. It is also possible that in the future other BoW-compatible technology enhancements will further increase throughput per chipedge. Examples of this include previous discussions on a Turbo mode using simultaneous bidirectional communication. That mode is not covered in this draft.

1.1.1. Objectives

The BoW interface is intended to meet the following design objectives:

- Be inexpensive to implement
- Portable across process nodes ranging from 28nm to 5nm
- Portable across multiple bump pitches
- Have the Flexibility to support advancing packaging technology
- Be unencumbered by technology license costs
- Very low power (<‘pJ/bit)
- Very low latency

1.1.2. Advantages

The Bunch of Wires interface provides several key advantages for chiplet based systems:

- Can operate at higher data rates per pin than existing parallel standards
  - -or- lower data rates for compatibility with existing parallel standards

- Can be implemented in legacy technologies (process nodes) with generally available IP
- Terminated mode can be implemented in less effort than a traditional SERDES
- Does not require silicon based interconnect
- Is not constrained or intended to be used with a specific bump pitch
  - Two BoW interfaces can each be implemented at different bump pitches and can be directly connected on an organic substrate, through fanout technology or through silicon based interconnect.

While the advantages and simplicity are excellent benefits, the BoW interface does require more package routing traces than other serial based XSR or USR interconnect. This drives BoW implementations that need the highest bandwidth to use fine bump pitches and 'stacked' BoW implementations, adding some complexity and cost in test and packaging. Lower bandwidth implementations are free to use more standard packaging technology with coarse bump pitch.

1.1.3. Scope

The scope of this document and of any contributions to this document are limited to:

1. The specification of the BoW interface that specifies the following functionality:
   a. Operating modes
   b. Physical design
   c. Test and testability
   d. Operation
   e. Management controls
   f. Methods to verify and validate compliance with this specification
   g. Recommended bump patterns and signal ordering
   h. Performance estimates
   i. Other functions or design practices that may be deemed necessary to meet the design objectives listed above

2. The following activities are outside the scope of this document and contributions to this document:
   a. Physical implementations of the interface
   b. Integration of the interface with system-level data flow e.g. adapting a standard PHY-layer abstraction such as PIPE interface to the BoW
   c. The actual use of this interface in systems
   d. The use of this interface outside a package

3. The following activities are intended to be addressed in subsequent versions of this specification:

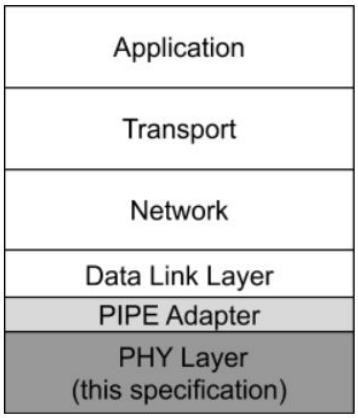
    a. Test enablement
    b. Compliance points
    c. Initialization
    d. Security

1.1.4. Compliance Summary

Table summarizes the compliance points that shall be met in order to meet the BoW requirements. Each of the compliance points is discussed in the specification.

1.2. BoW Architecture

The BoW interfaces implement a physical-layer or PHY interconnect protocol, implementing Layer 1 of the 5-layer TCP/IP reference model.



1.2.1. BoW Configurations

There are multiple possible BoW configurations. All versions of the implementation must be interoperable with the minimum definition. All implementations are source synchronous parallel interfaces using a differential clock. Beyond the basic implementation, adding termination provides higher performance per mm of beachfront bandwidth but is more complex to design.

- All BoW configurations are intended to be used in multi-chiplet designs
- The full range of operating frequencies is expected to be documented in a data sheet.
- All BoW implementations uses source synchronous clocking with data transmission aligned to clock edges.

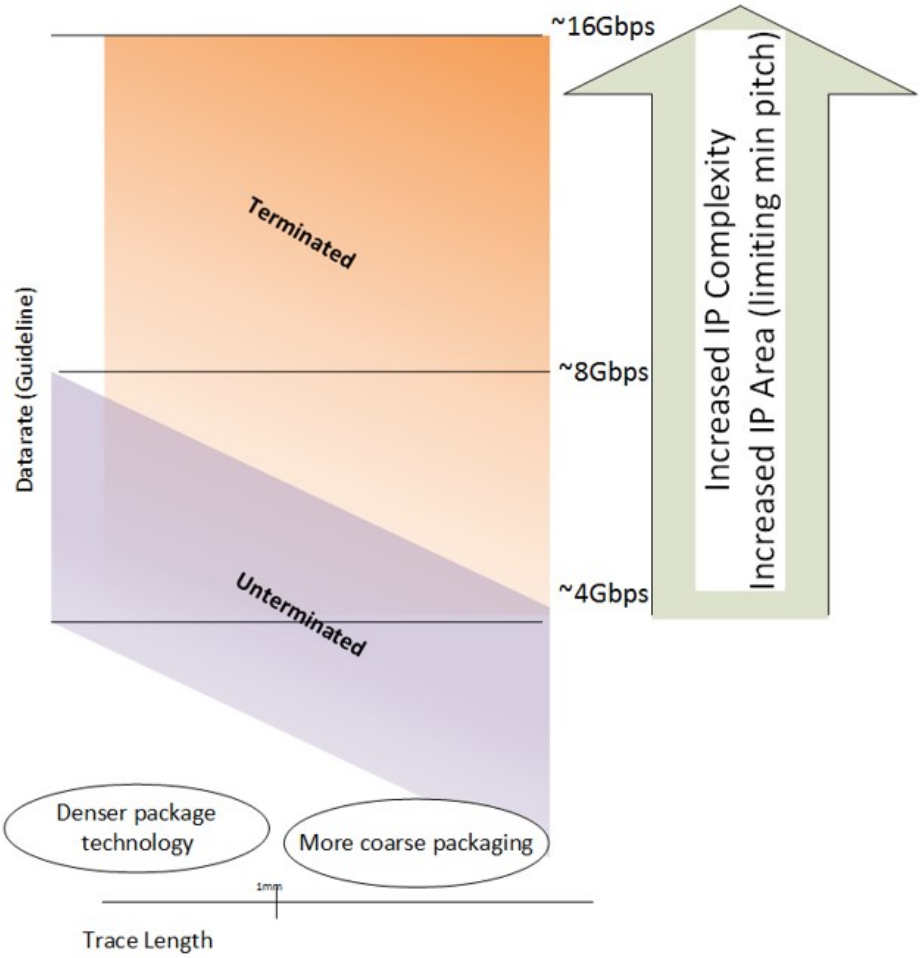
The separate implementation of the interface are specified such that they can be connected to one another. **When two interfaces are connected, data rate for the operating mode must be configured such that both ends support the data rate.**

All BoW implementations must support the minimum configuration of BoW (2Gbps datarate, 1 Ghz clock rate, un-terminated IO)

- The throughput per wire on a BoW interface implementation will be affected by:
- The choice of packaging technology
- The physical distance between the chiplets being connected: Faster data rates may be easier with chiplets that are physically closer
- Bump spacing: Coarse bumps may allow for circuitry to enable faster data rates.

The BoW specification provides for optional technology to increase the data rate per wire. But it is also possible for basic BoW implementation implemented with advanced packaging or between physically close chiplets to offer a higher data rate per wire than a terminated BoW interface in some configurations.

A high level view of the BoW Interface Data-rate ranges is shown below:



Note that the BoW Unterminated mode can support datarates of >5Gbps only when trace length is minimized (<1mm) due to reflections.

BoW A BoW implementation shall support a clock rate no greater than 2.5 Gigahertz (GHz) / 5 Gbps DDR data rate for typical trace lengths and 4.0 GHz / 8 Gbps DDR data rate for traces <1mm.
DDR is double datarate defined as one data bit per rising and falling edge of the clock. Laminate trace lengths for BoW mode should be limited to 10mm to avoid reflections.

Terminated mode Termination mode is expected to use lane termination to minimize signal reflection and improve the data rate per line, improving the data rate per millimeter of chiplet edge. Data is always expected to be transmitted at the Double Data Rate. A terminated implementation shall support a minimum clock rate no greater than 8 GHz and Double Data Rate operation.

Configuration	Clock Data relationship	Operating Clock rate	Operating Data rate	Termination
BoW	DDR	<= 2.5 GHz <= 4Ghz	<= 5 Gbps <= 8 Gbps	No, up to 10mm No *<1mm only
Termination Mode	DDR	<= 8 GHz	<= 16 Gbps	Yes

1.2.2. BoW Interface

The BoW interface defines three signal types:

- Data signals
  - Inputs (RX): data input signals received by the interface
  - Outputs (TX): data output signals transmitted from the interface
- Clocks
  - Data clock out (ns_fwd_clk), sent to the receiving chiplet
  - Data clock in (fs_fwd_clk): received from the receiving chiplet
- FEC
  - Optional FEC bits (1 bit recommended)

2. Design Assumptions

Short connections
Organic substrate spacing
Low loss implementations
Need low end2end latency
Low power

3. Standard Compatibility

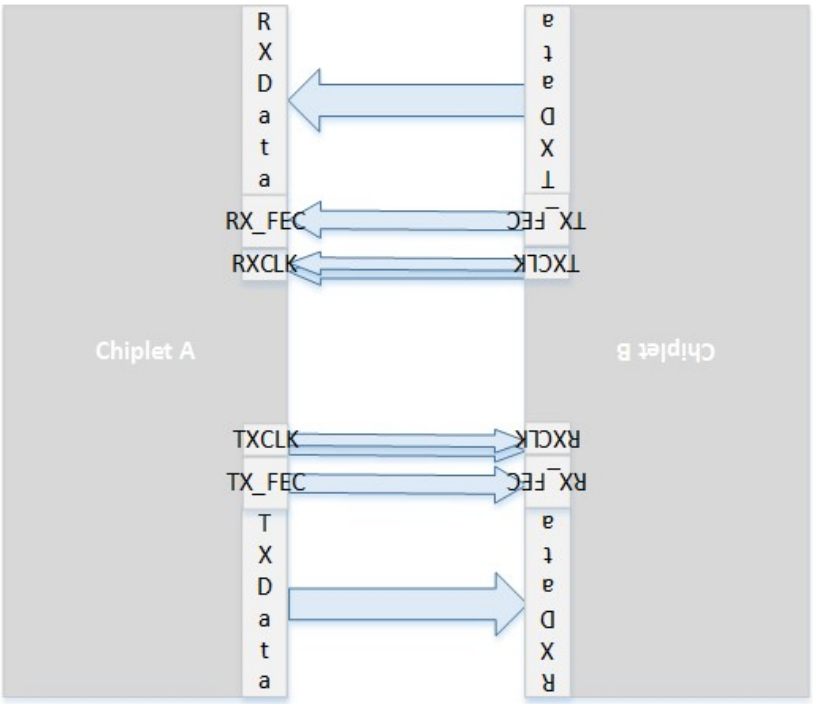
The Bunch of Wires (BoW) is a simple Double Data Rate source synchronous interface that has much in common with other parallel interfaces including Intel AIB, High Bandwidth Memory and other simple source synchronous interfaces.

- A defined dataword width of 16 data bits per differential clock
- Support only for Double Data Rate (DDR) mode to simplify clocking
- Multiple supported datarates and modes
  - BoW Unterminated is most similar to AIB using un-terminated CMOS IO to reduce power at low datarates
  - BoW Terminated uses terminated IO to improve SI and datarates

Due to reduced ESD requirements, the BoW specification is not expected to be compliant to off-package IO standards, though it may interoperate with other chiplets using CMOS IO buffers.

4. Interface Specifications

4.1. Block Diagram



4.2. Signals

Function	# Bumps	Bump Names	Notes
TX Data	16	TXDQ [15:0]	
TX Data Clock	2	TXCLK+/TXCLK-	Differential
TX Data FEC (optional)	1-2	TXFEC	RS(34, 32) or other
RX Data	16	RXDQ [15:0	
RX Data Clock	2	RXCLK+/RXCLK-	Differential
TX Data FEC (optional)	1-2	TXFEC	RS(34, 32) or other

4.3. Calibration Mode Signals

<To be included in a future release of the specification>

5. Timing

5.1. Supported Datarates

BOW supports the following datarates:

Clock Rate	Datarate	SDR/DDR	Termination	Hybrid TX/RX	Mode
1-2.5 GHz	2Gbps-5Gbps	DDR	No	No	BoW
1-4 GHz	2Gbps-8 Gbps*	DDR	Yes	No	*for traces < 1 mm
2-8 GHz	4Gbps-16Gbps	DDR	Yes	No	Terminated mode

At a minimum all BoW implementations must support the minimum 1 Ghz clock rate, 2Gbps datarate using unterminated IO. For ease of integration, increased datarates should support 1 Gbps increments from the floor 2Gbps datarate.

5.2. Clocking

Rising to rising and rising to falling edge specifications for the TX clock rate (TXCLK pin) must achieve better than +/- 5% accuracy.

Additional requirements will be documented in future releases of the specification.

6. Electrical Specifications

6.1. Voltages

Where possible BoW IO should reside on the VDD rail to simplify design of chiplets and provide current to controller logic from the BoW recommended bump patterns. BoW should support a range of voltages from 0.7 nominal to 0.95 nominal (0.66 to 0.99 with standard +/- 5% power supply tolerances) where possible. All BoW implementations must support at least 0.9V nominal (0.85 to 0.95V).

6.2. ESD Requirements

BOW IO should be designed to support 50 V CDM (Charged Device Model) and 250 V HBM (Human Body Model). This requirement is similar to other die to die interface standards.

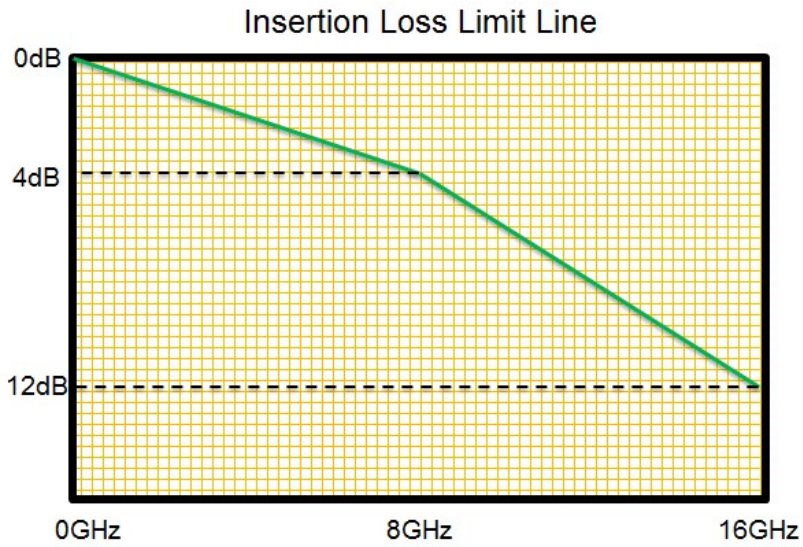
6.3. Termination Requirements

BoW datarates (Typically 5Gbps, up to 8Gbps for <1mm trace length) do not require termination. Higher datarates (up to 16 Gbps) requires termination,

and must be built with selectable termination.

6.4. Target Channel Requirements

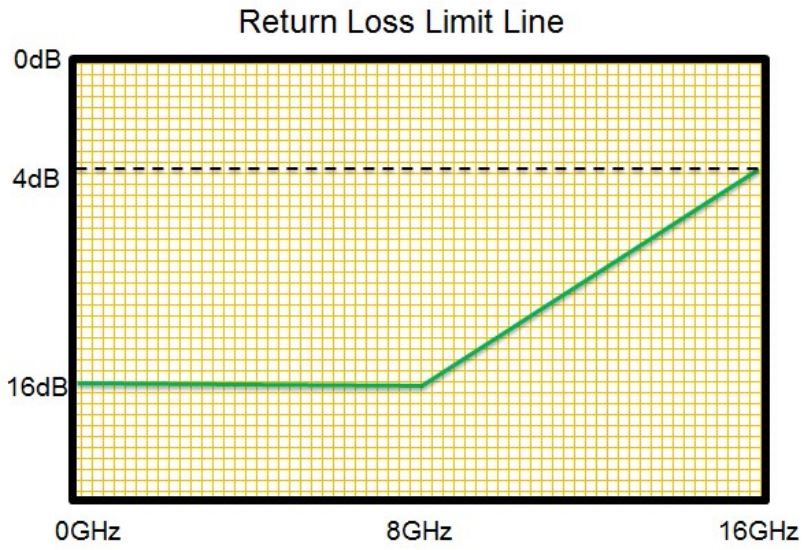
6.4.1. Channel loss line limits



BoW channel limit is limited by the round trip reflection delay and limited to <10mm for a 5Gbaud with proper slew rate control

Enabling termination enables longer channel regardless of baud rate, but to minimize the equalization requirement, it shall meet the provided Insertion Loss limit line.

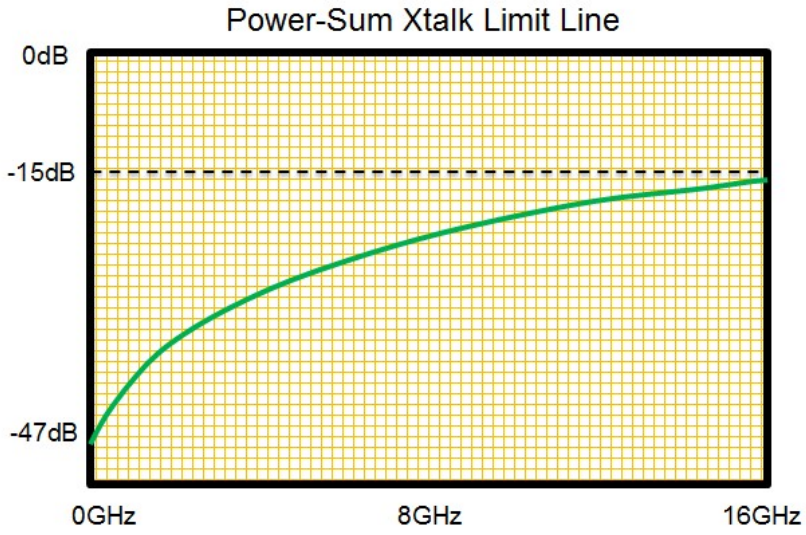
6.4.2. Return loss line limits



BoW channel is expected to be unterminated in the default mode and does not need to follow any Return Loss spec.

Enabling Termination mode requires meeting the provided Return Loss limit line for proper operation and meeting target BER.

6.4.3. Power Sum Crosstalk Limit Line



Crosstalk is defined in form of the sum of crosstalk power of all aggressors on a target trace.

The proposed power-sum crosstalk spec for termination mode: PS Xtalk Limit = -10 dB -37dB.e^(-f/8GHz)

A victim trace in between two aggressor traces on the same package substrate layer with air gap spacing of 50 um (or more) with at least a reference plane under or above will meet the proposed power-sum crosstalk limit.

7. Logic Interface

<To be completed in subsequent version of specification>

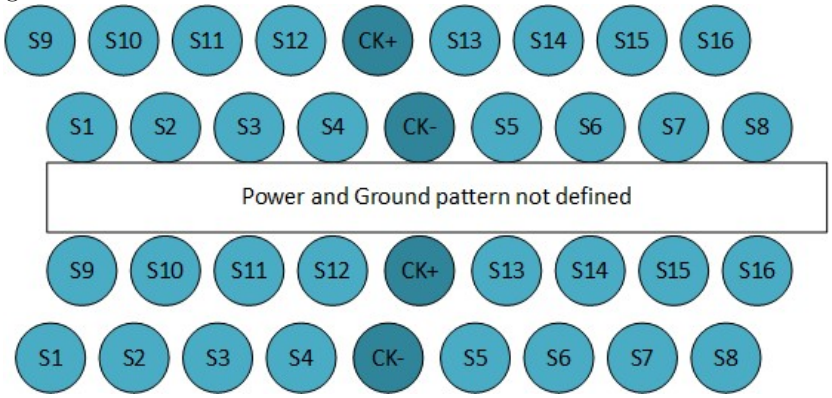
8. Physical Constraints

8.1. Signal Ordering

8.2. Preferred Bump Patterns

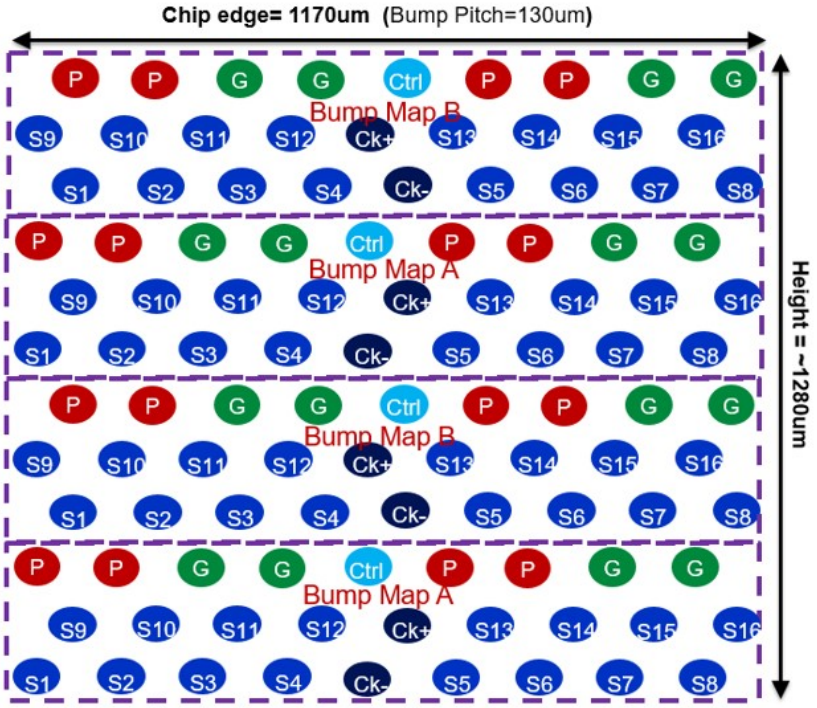
BoW does not dictate a specific bump pitch but does have a defined bump pattern. By not specifying a bump pitch, implementations can be built on both legacy and leading edge technologies. Specifying a signal pattern, however, allows package routing between interfaces with limited signal crossings.

BoW can be implemented with any number of stacked interfaces, however such stacking should implement the bump pattern with an alternating stagger of signals.



Additional interfaces alternate as shown above.

Example Bump Pattern (based on 130 um staggered bump pitch) shown below:



9. Testability

<addressed in subsequent version of specification>

9.1. Loopback Test

9.2. IEEE 1149.1

10. Document History

Date	Version	Notes
09/20/2019	0.7	Initial version for release

11. Known Feature Request

Date	Notes
09-06-2019	Microbump compatibility - addressed with non-specified bump pitch
09-06-2019	Ultra short high speed unterminated - addressed