1.1.1. Serial Port Registers

(UART1 **B**ase **A**ddress Refers to the Register of index 57h-54h, IDSEL = AD18/SB of PCI Configuration Register)

(UART2 **B**ase **A**ddress Refers to the Register of index A3h-A0h, IDSEL = AD18/SB of PCI Configuration Register)

(UART3 **B**ase **A**ddress Refers to the Register of index A7h-A4h, IDSEL = AD18/SB of PCI Configuration Register)

(UART4 **B**ase **A**ddress Refers to the Register of index ABh-A8h, IDSEL = AD18/SB of PCI Configuration Register)

IO Address	Register Name	Section
BA + 0h	Transmit/Receive Data Buffer (DLAB=0)	11.2.14
BA + 0h	LSB of Baud Rate Generator Divisor Latches (DLAB=1)	11.2.14
BA + 1h	Interrupt Enable Register (DLAB=0)	11.2.14
BA + 1h	MSB of Baud Rate Generator Divisor Latches (DLAB=1)	11.2.14
BA + 2h	Interrupt Identification Register	11.2.14
BA + 2h	FIFO Control Register	11.2.14
BA + 3h	Line Control Register	11.2.14
BA + 4h	Modem Control Register	11.2.14
BA + 5h	Line Status Register	11.2.14
BA + 6h	Modem Status Register	11.2.14
BA + 7h	Scratchpad Register	11.2.14

1.1.2. Serial Port Registers

The system programmer may access any of the UART registers. These registers control UART operations including transmission and reception of data.

(UART1 **Base Address** Refers to the Register of index 57h-54h in SB PCI Configuration Register)

(UART2 **Base Address** Refers to the Register of index A3h-A0h in SB PCI Configuration Register)

(UART3 **Base Address** Refers to the Register of index A7h-A4h in SB PCI Configuration Register)

(UART4 **Base Address** Refers to the Register of index ABh-A8h in SB PCI Configuration Register)

I/O Port: Base Address + 0h

Register Name: Transmit/Receive Data Buffer (DLAB=0)

Reset Value: --

7	6	5	4	3	2	1	0
TD/RD							

An output to this register stores a byte into the UART's transmit holding buffer. An input gets a byte from the receive buffer of the UART. These are two separate registers within the UART. To access this register, the Divisor Latch Access Bit (DLAB) must be zero. DLAB is bit 7 in the line control register 3.

Bit	Name	**Attribute**	Description
7-0	TD/RD	R/W	**Read:** This register holds the received incoming data byte. **Write:** This register contains the data byte to be transmitted.

I/O Port: Base Address + 0h

Register Name: LSB of Baud Rate Generator Divisor Latches (DLAB=1)

Reset Value: 01h

7	6	5	4	3	2	1	0
LBR							

The UART contains a programmable baud generator that is capable of taking any clock input from DC to 24 MHz and dividing it by any divisor from 2 to 2^{16}-1. The output frequency of the baud generator is 16 X the baud [divisor # = (frequency input) / (baud rate X 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization to ensure proper operation of the baud generator. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded. The Table listed below provides decimal divisors to use with crystal frequencies of 1.8432 MHz and 24 MHz, respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. Using a divisor of zero is not recommended.

Bit	Name	**Attribute**	Description
7-0	LBR	R/W	This register contains the LSB (Least Significant Byte) of divisor latches.

TABLE Baud Rates, Divisors and Crystals

Baud Rate	1.8432 MHz Crystal		24 MHz Crystal	
	Decimal Divisor for 16 X Clock	Percent Error	Decimal Divisor for 16 X Clock	Percent Error
50	2304	-	30000	-
75	1536	-	20000	-
110	1047	0.026	13636	-
134.5	857	0.058	11152	-
150	768	-	10000	-
300	384	-	5000	-
600	192	-	2500	-
1200	96	-	1250	-
1800	64	-	833	-
2000	58	0.69	750	-
2400	48	-	625	-
3600	32	-	417	-
4800	24	-	312	-
7200	16	-	208	-
9600	12	-	156	-
19200	6	-	78	-
38400	3	-	39	-
56000	2	2.68	26	-
115200	1	-	13	-

I/O Port: Base Address + 1h

Register Name: Interrupt Enable Register (DLAB=0)

Reset Value: 00h

7	6	5	4	3	2	1	0
Reserved				MSI	RLSI	THREI	RDAI

This register enables the five types of UART interrupts. Each interrupt can individually activate the interrupt (INTR) output signal. It is possible to totally disable the interrupt system by resetting bit 0 through 3 of the Interrupt Enable Register (IER). Similarly, setting bits of the IER register to a logic 1 enables the selected interrupt(s). Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the INTR output signal. All other system functions operate in their normal manner, including the settings of the Line Status and MODEM Status Registers. Table II shows the contents of the IER. Details on each bit are listed as follows.

Bit	Name	**Attribute**	Description
7-4	Rsvd	RO	Reserved. Must be always ‘0’
3	MSI	R/W	Modem Status Interrupt 0: Disable 1: Enable
2	RLSI	R/W	Received Line Status Interrupt 0: Disable 1: Enable
1	THREI	R/W	Transmitter Holding Register Empty Interrupt 0: Disable 1: Enable
0	RDAI	R/W	Received Data Available Interrupt 0: Disable 1: Enable

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I/O Port: Base Address + 1h

Register Name: MSB of Baud Rate Generator Divisor Latches (DLAB=1)

Reset Value: 00h

7	6	5	4	3	2	1	0
MBR							

Bit	Name	Attribute	Description
7-0	MBR	R/W	This register contains the MSB (Most Significant Byte) of divisor latches.

I/O Port: Base Address + 2h

Register Name: Interrupt Identification Register

Reset Value: 01h

7	6	5	4	3	2	1	0
FIFOE		Rsvd		FIFOM	PT		IP

In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the interrupt Identification Register. The four levels of interrupt conditions in order of priority are Receiver Line Status, Received Data Ready, Transmitter Holding Register Empty, and MODEM Status.

When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is complete. Table II shows the contents of the IIR. Details on each bit are listed as follows:

Bit	Name	Attribute	Description
7-6	FIFOE	RO	These two bits are set to ‘1’ when the FIFO Control Register bit 0 = ‘1’.
5-4	Rsvd	RO	Reserved. Must be returned all ‘0’s.
3	FIFOM	RO	In non-FIFO Mode This bit is a ‘0’. In FIFO Mode This bit is set to ‘1’ along with bit 2 when a timeout interrupt is pending

2-1	PT	RO	Indicate the Highest Priority Interrupt Pending 00: Modem Status Interrupt (Lowest Priority) 01: Transmitter Holding Register Empty Interrupt 10: Received Data Ready Interrupt 11: Receiver Line Status Interrupt (Highest Priority)
0	IP	RO	Interrupt Pending 0: Interrupt Pending 1: No Interrupt Pending

TABLE Interrupt Control Functions

FIFO Mode Only	Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 3	**Bit 2**	**Bit 1**	**Bit0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Rest Control**
0	0	0	1	-	None	None	-
0	1	1	0	Highest	received line status	overrun error, parity error, framing error or break Interrupt	reading the line status register
0	1	0	0	Second	received data available	received data available or trigger level reached	reading the receiver buffer register or the FIFO dropping below the trigger level
1	1	0	0	Second	character timeout Indication	no characters have been removed from or Input to the RCVR FIFO during the last 4 Characters times and there is at least 1 character in it during this time.	reading the receiver buffer register
0	0	1	0	Third	transmitter holding register empty	transmitter holding register empty	reading the IIR register (if the source of interrupt is available) or writing into the transmitter holding register
0	0	0	0	Fourth	MODEM Status	clear to send, data set ready , ring Indicator, or data carrier detect	reading the MODEM Status register

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I/O Port: Base Address + 2h

Register Name: FIFO Control Register

Reset Value: 00h

7	6	5	4	3	2	1	0
TL		Rsvd			CTF	CRF	FE

This is a write only register at the same location as the IIR (the IIR is a read only register). This register is used to enable the FIFOs, clear the FIFOs, set the RCVR FIFO trigger level, and select the type of DMA signaling.

Bit	Name	**Attribute**	Description
7-6	TL	WO	These two bits are used to set the trigger level (bytes) for Receive FIFO interrupt 00: 1 byte 01: 4 bytes 10: 8 bytes 11: 14 bytes
5-3	Rsvd	RO	Reserved.
2	CTF	WO	Writing a ‘1’ to this bit will clear all bytes in transmitted FIFO and reset its counter to 0. The shift register is not cleared
1	CRF	WO	Writing a ‘1’ to this bit will clear all bytes in received FIFO and reset its counter to 0. The shift register is not cleared
0	FE	WO	Setting this bit to a "1" enables both the transmitted and received FIFOs. Clearing this bit to a "0" disables both the transmitted and received FIFOs and clears all bytes from both FIFOs. When changing from FIFO Mode to non-FIFO (16450) mode, data are automatically cleared from the FIFOs. This bit must be a 1 when other bits in this register are written to or they will not be properly programmed.

I/O Port: Base Address + 3h

Register Name: Line Control Register

Reset Value: 00h

7	6	5	4	3	2	1	0
DLAB	BC	SP	EOP	PE	NSB	SCN	

The system programmer specifies the format of the asynchronous data communications exchange and sets the Divisor Latch Access bit via the Line Control Register (LCR). The programmer can also read the contents of the Line Control Register. The read capability simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. Table II shows the contents of the LCR. Details on each bit are listed as follows:

Bit	Name	**Attribute**	Description
7	DLAB	R/W	Divisor Latch Access Bit (DLAB). It must be set to '1' to access the divisor latch of the baud generator during a Read or Write operation. It must be set to a '0' to access the Receive Buffer, the Transmitter Holding Register or the interrupt Enable Register.
6	BC	R/W	Break Control Bit. It causes a break condition to be transmitted to the receiving UART. 0: Disable the break 1: Force the serial out (SOUT) to the Spacing ('0') State
5	SP	R/W	This bit is the Stick Parity bit. When bits 3, 4 and 5 are logic 1s, the Parity bit is transmitted and checked as a '0'. If bits 3 and 5 are '1's and bit 4 is a '0', the Parity bit is transmitted and checked as a '1'. If bit 5 is a logic 0, Stick Parity is disabled.
4	EOP	R/W	Even/Odd parity bit selected when parity is enabled 0: Odd parity selected 1: Even parity selected
3	PE	R/W	Parity Enabled/Disabled. 0: Parity disabled 1: Parity enabled When this bit is set to a '1', a parity bit will be generated between the last data word and STOP bit when data is being transmitted, and check the parity bit when data is being received.

Bit	Name	Attribute	Description
2	NSB	R/W	13 Stop bit. This bit specifies the number of Stop bits transmitted and received in each serial character. Set 0: One Stop bit is generated in the transmitted data. Set 1: One and a half stop bits are generated for a 5-bit word length characters. Two stop bits are generated for either 6-, 7-, or 8-bit word length characters. The receiver checks the first Stop bit only, regardless of the number of Stop bits selected.
1-0	SCN	R/W	These two bits specify the number of bits in each transmitted and received serial characters. 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits

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I/O Port: Base Address + 4h

Register Name: Modem Control Register

Reset Value: 00h

7	6	5	4	3	2	1	0
Rsvd			LBF	INTE	Rsvd	RTS	DTR

This register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table II and are described as below.

Bit	Name	Attribute	Description
7-5	Rsvd	RO	Reserved. Must be all ‘0’s
4	LBF	R/W	This bit provides the loop back feature for diagnostic testing of the Serial Port. When this bit is

Bit	Name	Attribute	Description
			set to ‘1’, the following occurs: 1) The Transmitter serial out (SOUT) is set to the Marking State (‘1’). 2) The receiver Serial Input (SIN) is disconnected. 3) The output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input. 4) All MODEM Control inputs (CTS#, **DSR#**, **RI#** and DCD#) are disconnected. 5) The four MODEM Control outputs (DTR#, **RTS#**, OUT1 and OUT2) are internally connected to the four MODEM Control inputs (CTS#, **DSR#**, **RI#** and DCD#). 6) The Modem Control output pins are forced to be inactive high. 7) Data transmitted are immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the Serial Port. In the diagnostic mode, the receiver and the transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.
3	INTE	R/W	Interrupt Enable. This bit is used to enable a UART interrupt. When OUT2 is a ‘0’, the serial port interrupt output is forced to the high impedance state - disabled. When OUT2 is a ‘1’, the serial port interrupt output is enabled.
2	Rsvd	RO	Reserved.
1	RTS	R/W	This bit controls the Request To Send (**RTS#**) output. When this bit is set to a ‘1’, the **RTS#** output is forced to a ‘0’. When this bit is a ‘0’, the **RTS#** output is forced to a ‘1’.
0	DTR	R/W	This bit controls the Data Terminal Ready (DTR#) output. When this bit is set to a ‘1’, the DTR# output is forced to a ‘0’. When this bit is a ‘0’, the DTR# output is forced to a ‘1’.

I/O Port: Base Address + 5h

Register Name: Line Status Register

Reset Value: 60h

7	6	5	4	3	2	1	0
EB	TEMT	THRE	BI	FE	PE	OE	DR

This register provides status information to the CPU concerning the data transfer.

Bit	Name	**Attribute**	Description
7	EB	R/W	This bit is permanently set to a logic "0" in the 450 mode. In the FIFO mode, this bit is set to a logic "1" when there is at least one parity error, framing error or break indication in the FIFO. This bit is cleared when the LSR is read if there are no subsequent errors in the FIFO.
6	TEMT	R/W	Transmitter Empty (TEMT). This bit is set to a '1' whenever the Transmitter Holding Register (THR) and Transmitter Shift Register (TSR) are both empty. It is reset to a '0' whenever either the THR or TSR contains a data character. This bit is a read only bit. In the FIFO mode, this bit is set whenever the THR and TSR are both empty,
5	THRE	R/W	Transmitter Holding Register Empty (THRE). This bit indicates that the Serial Port is ready to accept a new character for transmission. In addition, this bit causes the Serial Port to issue an interrupt when the Transmitter Holding Register interrupt enable is set high. The THRE bit is set to a '1' when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. This bit is reset to '0' whenever the CPU loads the Transmitter Holding Register. In the FIFO mode, this bit is set when the transmit FIFO is empty. It is cleared when at least 1 byte is written to the transmit FIFO. This bit is a read only bit.

Bit	Name	Attribute	Description
4	BI	R/W	Break Interrupt (BI). This bit is set to a '1' whenever the received data input is held in the Spacing state ('0') for longer than a full word transmission time (that is, the total time of the start bit + data bits + parity bits + stop bits). The BI is reset after the CPU reads the contents of the Line Status Register. In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. When a break occurs, only one zero character is loaded into the FIFO. Restarting after a break is received requires the serial data (RXD) to be '1' for at least 1/2 bit time.
3	FE	R/W	Framing Error (FE). This bit indicates that the received character does not have a valid stop bit. This bit is set to a '1' whenever the stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE is reset to a '0' whenever the Line Status Register is read. In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. The Serial Port will try to resynchronize after a framing error. To do this, it assumes that the framing error was due to the next start bit, so it samples this 'start' bit twice and then takes in the 'data'.
2	PE	R/W	Parity Error (PE). This bit indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE is set to a '1' upon detection of a parity error and is reset to a '0' whenever the Line Status Register is read. In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO.
1	OE	R/W	Overrun Error (OE). This bit indicates that the data in the Receiver Buffer Register were not read before the next character was transferred into the register, thereby destroying the previous character. In FIFO mode, an overrun error will occur only when the FIFO is full and the next character has been completely received in the shift register. The character in the shift register is overwritten but not transferred to the FIFO. The OE indicator is set to a '1' immediately upon detection of an overrun condition, and reset whenever the Line Status Register is read.
0	DR	R/W	Data Ready (DR). It is set to a '1' whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. This bit is reset to a '0' by reading all of the data in the Receiver Buffer Register or the FIFO.

I/O Port: Base Address + 6h

Register Name: Modem Status Register

Reset Value: x0h

7	6	5	4	3	2	1	0
DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS

This register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to logic 1s whenever a control input from the MODEM changes state. They are reset to logic 0s whenever the CPU reads the MODEM Status Register. The contents of the MODEM Status Register are indicated in Table II and described as below.

Bit	Name	**Attribute**	Description
7	DCD	R/W	This bit is the complement of the Data Carrier Detect (DCD#) input. If bit 4 of the MCR is set to '1', this bit is equivalent to OUT2 in the Modem Control Register.
6	RI	R/W	This bit is the complement of the Ring Indicator (**RI#**) input. If bit 4 of the MCR is set to '1', this bit is equivalent to OUT1 in the Modem Control Register.
5	DSR	R/W	This bit is the complement of the Data Set Ready (**DSR#**) input. If bit 4 of the MCR is set to '1', this bit is equivalent to DTR# in the Modem Control Register.
4	CTS	R/W	This bit is the complement of the Clear To Send (CTS#) input. If bit 4 of the MCR is set to '1', this bit is equivalent to **RTS#** in the Modem Control Register.
3	DDCD	R/W	Delta Data Carrier Detect (DDCD). This bit is set to '1' whenever the DCD# input to the chip has changed the state since the last time the MSR (Modem Status Register) was read. It is reset to a '0' whenever the MODEM Status Register is read.
2	TERI	R/W	Trailing Edge of Ring Indicator (TERI). This bit is set to '1' whenever the **RI#** input has been changed from '0' to '1'. It is reset to '0' whenever the MODEM Status Register is read.
1	DDSR	R/W	Delta Data Set Ready (DDSR). This bit indicates that the **DSR#** input to Vortex86DX has changed the state since the last time the MSR (Modem Status Register) was read. This bit is set to '1'" whenever **DSR#** input from the MODEM has changed the state. It is reset to '0' whenever the MODEM Status Register is read.
0	DCTS	R/W	Delta Clear To Send (DCTS). This bit indicates that the CTS# input to the Vortex86DX has

Bit	Name	Attribute	Description
			changed the state since the last time the MSR (Modem Status Register) was read. This bit is set to ‘1’" whenever CTS# input from the MODEM has changed the state. It is reset to ‘0’ whenever the MODEM Status Register is read.

Note: *Whenever bit 0, 1, 2 or 3 is set to a logic "1", a MODEM Status Interrupt is generated.*

I/O Port: Base Address + 7h

Register Name: Scratchpad Register

Reset Value: --

7	6	5	4	3	2	1	0
SR							

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a scratchpad register used by the programmer to hold data temporarily.

Bit	Name	Attribute	Description
7-0	SR	R/W	This 8-bit read/write register has no effect on the operation of the Serial Port. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.