1.1.1. SPI Control Registers

(**B**ase **A**ddress Refers to the Register of index 43h-40h, IDSEL = AD11/NB of PCI Configuration Register)

IO Address	Register Name	Section
BA + 08h	External SPI Output Data Register	11.2.16
BA + 09h	External SPI Input Register	11.2.16
BA + 0Ah	External SPI Control Register	11.2.16
BA + 0Bh	External SPI Status Register	11.2.16
BA + 0Ch	External SPI Chip Select Register	11.2.16
BA + 0Dh	External SPI Error Status Register	11.2.16

NB of PCI Configuration Register

Register Offset: 43h – 40h

Register Name: SPI Base Address Register

Reset Value: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBA																												Rsvd		MIO	En

Bit	Name	Attribute	Description
31-4	PBA	R/W	SPI Base Address A[31-4]. Size is 16 bytes. If it is I/O space, it only uses A[15-4]. If it is memory space, it use A[31-4].
3-2	RSVD	RO	Reserved.
1	MIO	R/W	Memory or I/O space select. 1: Memory space 0: I/O space
0	En	R/W	SPI Base address is enabled when set.

1.1.2. SPI Control Registers

BASE_ADDR defined on NB PCI CFG 40h

Register Offset: BASE_ADDR+08h

Register Name: External SPI Output Data Register

Reset Value: --

7	6	5	4	3	2	1	0
OUTDAT							

Bit	Name	Attribute	Description
7-0	OUTDAT	WO	Data output to SPI when write. No function when read.

Register Offset: BASE_ADDR+09h

Register Name: External SPI Input Register

Reset Value: FFh

7	6	5	4	3	2	1	0
INDAT							

Bit	Name	Attribute	Description
7-1	INDAT	RO	Data input from SPI when read. Preload data from SPI when write

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Register Offset: BASE_ADDR+0Ah

Register Name: External SPI Control Register

Reset Value: 15h

7	6	5	4	3	2	1	0
RSVD			FIEN	CKDIV			

Bit	Name	Attribute	Description
7-5	RSVD	RO	Reserved
4	FIEN	R/W	FIFO mode enable when set.
3-0	CKDIV	R/W	SPI clock divided. The SPI clock is DRAM clock/(2 * SPI clock divided) , 0 is not allowed

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Register Offset: BASE_ADDR+0Bh

Register Name: External SPI Status Register

Reset Value: 10h

7	6	5	4	3	2	1	0

BUSY	FIFU	IDR	ODC	RSVD

Bit	Name	Attribute	Description
7	BUSY	RO	SPI controller is BUSY.
6	FIFU	RO	FIFO full
5	IDR	RO	Input data ready when set.
4	ODC	RO	Output complete/FIFO empty when set.
3-0	RSVD	RO	Reserved

Register Offset: BASE_ADDR+0Ch

Register Name: External SPI Chip Select Register

Reset Value: 01h

7	6	5	4	3	2	1	0
Reserved							CS

Bit	Name	Attribute	Description
7-1	RSVD	RO	Reserved
0	CS	R/W	0: SPI CS# is low, 1: SPI CS# is high

Register Offset: BASE_ADDR+0Dh

Register Name: External SPI Error Status Register

Reset Value: 00h

7	6	5	4	3	2	1	0
RSVD			WCTE	DOLE	FIURE	FIORE	RSVD

Bit	Name	Attribute	Description
7-5	RSVD	RO	Reserved
4	WCTE	R/WC	Error status 4, Write SPI Control Register when controller is busy. Write 1 to clear.
3	DOLE	R/WC	Error status3, Input data overlap. Write 1 to clear.
2	FIURE	R/WC	Error status2, FIFO under-run. Write 1 to clear.
1	FIORE	R/WC	Error status1, FIFO over-run. Write 1 to clear.
0	RSVD	RO	Reserved