### 1.1.1. I2C Registers

(**B**ase **A**ddress Refers to the Register of index D7h-D4h, IDSEL = AD18/SB of PCI Configuration Register)

| IO Address | Register Name | Section |
|---|---|---|
| BA + 00h | I2C0 Control Register | 11.2.24 |
| BA + 01h | I2C0 Status Register | 11.2.24 |
| BA + 02h | I2C0 MY_Address Register | 11.2.24 |
| BA + 03h | I2C0 TX_Address Register | 11.2.24 |
| BA + 04h | I2C0 Transmit/Receive Data | 11.2.24 |
| BA + 05h | I2C0 Clock Frequency Control1 | 11.2.24 |
| BA + 06h | I2C0 Clock Frequency Control2 | 11.2.24 |
| BA + 07h | I2C0 Extra Control Register | 11.2.24 |
| BA + 08h | I2C1 Control Register | 11.2.24 |
| BA + 09h | I2C1 Status Register | 11.2.24 |
| BA + 0Ah | I2C1 MY_Address Register | 11.2.24 |
| BA + 0Bh | I2C1 TX_Address Register | 11.2.24 |
| BA + 0Ch | I2C1 Transmit/Receive Data | 11.2.24 |
| BA + 0Dh | I2C1 Clock Frequency Control1 | 11.2.24 |
| BA + 0Eh | I2C1 Clock Frequency Control2 | 11.2.24 |
| BA + 0Fh | I2C1 Extra Control Register | 11.2.24 |

### 1.1.2. I2C Registers

**Register Offset:** BA + 0h

**Register Name:** I2C0 Control Register

**Reset Value:** 00h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Sw_Inten | RX_Inten | TX_Inten | Nak_Inten | ARL_Inten | STP_Inten | STOP | NAKEn |

| Bit | Name | Attribute | Description |
|---|---|---|---|
| 7 | Sw_Inten | R/W | Slave write interrupt enable. When enabled, it will generate interrupt signal at slave mode to request software writing TX Data.<br>This bit is only needed at slave mode |
| 6 | RX_Inten | R/W | RX interrupt enable. When enabled, it will generate interrupt signal while RX Data buffer has data to be read |
| 7 | TX_Inten | R/W | TX interrupt enable. When enabled, it will generate interrupt signal while TX_Data or Tx_Addr was sent out successfully. |
| 4 | Nak_Inten | R/W | Nak Interrupt enable. When enabled, it will generate interrupt signal while master mode receive unpredictable “Nak” from outside slave |
| 3 | ARL_Inten | R/W | Arbitration loss interrupt enable. When enabled, it will generate interrupt signal while arbitration loss occurs |
| 2 | STP_Inten | R/W | Slave mode stop interrupt enable. When enabled, it will generate interrupt signal |

| Bit | Name | Attribute | Description |
|---|---|---|---|
| | | | while slave mode is ended by outside master issuing STOP. |
| 1 | STP | R/W | Writing a 1 to this bit will cause the hardware to send NAK+Stop signal after current byte transfer. It will be auto cleared while STOP is sent out on the i2c bus. This should be used only when the device is a master. |
| 0 | NAKEn | R/W | 1: This causes the $I^2C$-bus controller to send an Nak after each byte.<br>0: This causes the $I^2C$-bus controller to send an Ack after each byte.<br>This bit is only needed at slave mode |

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**Register Offset:** BA + 1h

**Register Name:** I2C0 Status Register

**Reset Value:** 01h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Sw_Req | RX_Rdy | TX_Done | Nak_err | ARL | SlaveSTP | BBusy | MS_ |

| Bit | Name | Attribute | Description |
|---|---|---|---|
| 7 | Sw_Req | R/WC | 1: Slave request software to write TX data<br>Write 1 to this bit will clear to “0” |
| 6 | RX_Rdy | R/WC | 1: Master/Slave has data to be read<br>Write 1 to this bit will clear to “0” |
| 5 | TX_Done | R/WC | 1: Master/Slave send TX_Address or TX data successfully<br>Write 1 to this bit will clear to “0” |
| 4 | Nak_err | R/WC | 1: Unpredictable Nak is received<br>Write 1 to this bit will clear to “0” |
| 3 | ARL | R/WC | 1: Arbitration loss .<br>Write 1 to this bit will clear to “0” |
| 2 | SlaveSTP | R/WC | 1: Slave receive STOP condition<br>Write 1 to this bit will clear to “0” |
| 1 | BBUSY | RO | The bus is considered to be busy after the Start condition and free again at a certain time interval after the Stop condition. |
| 0 | MS_ | RO | 1 : Master mode (Default)<br>0 : Slave mode |

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**Register Offset:** BA + 2h

**Register Name:** I2C0 My_Address Register

**Reset Value:** 00h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| My Slave Address | | | | | | | Rsvd |

| Bit | Name | Attribute | Description |
|---|---|---|---|
| 7-1 | My_Addr | R/W | 7-bits slave address which is checked by internal slave module. If address is match it will switch to slave mode. Processor can write proper value into this register to identify itself |
| 0 | Rsvd | RO | Reserved |

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**Register Offset:** BA + 3h

**Register Name:** I2C0 Transmit Address Register

**Reset Value:** 00h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TX Slave Address | | | | | | | R/W |

| Bit | Name | Attribute | Description |
|---|---|---|---|
| 7-0 | TX_Addr | R/W | 8-bit address register for Master to start a transaction. Processor can write this register to generate START + Slave Address + R/W on i2c bus. If Processor write a macrocode into this register, it will send out macrocode and switch to high-speed mode at proper timing. |

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**Register Offset:** BA + 4h

**Register Name:** I2C0 Transmit/Receive Data Register

**Reset Value:** 00h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Data | | | | | | | |

| Bit | Name | Attribute | Description |
|---|---|---|---|
| 7-0 | Data | R/W | 8-bit data register for $I^2C$-bus Tx/Rx operation. Processor can write this register to transmit DATA or read this register to receive data |

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**Register Offset:** BA + 5h

**Register Name:** I2C0 Clock Frequency Control1

**Reset Value:** 0ah

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PreScale1 | | | | | | | |

| Bit | Name | Attribute | Description |
|---|---|---|---|
| 7-0 | PreScale1 | R/W | Processor can write this register value from 0 to 255 to control the frequency of SCLH<br>At high speed Mode, SCLH frequency = 33M÷(PreScale1),<br>PS: If PreScale1 < 10, SCLH frequency = 33M÷10 = 3.3Mhz |

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**Register Offset:** BA + 6h

**Register Name:** I2C0 Clock Frequency Control2

**Reset Value:** 88h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Fast | PreScale2 | | | | | | |

| Bit | Name | Attribute | Description |
|---|---|---|---|
| 7 | Fast | R/W | 1: Fast mode , 0: Standard Mode |
| 6-0 | PreScale2 | R/W | Processor can write this register value from 0 to 255 to control the frequency of SCL<br>At F/S Mode, SCL frequency = 33M÷(PreScale1) ÷(PreScale2+1) |

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**Register Offset:** BA + 7h

**Register Name:** I2C0 Extra Control Register

**Reset Value:** 00h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| I2c_RST | TX_hit_RX | Rsv | | | | | |

| Bit | Name | Attribute | Description |
|---|---|---|---|
| 7 | I2c_RST | R/W | Write “1” will reset i2c controller except pre-scale registers (for keep the speed setting). After reset, Controller will send out 10 dummy clocks to ensure no any slave driving data because of incomplete operation of the Master (maybe other master), auto clear after reset complete. |
| 6 | TX_hit_RX | R/O | Indicate the TX address is written but may not send out because the slave is driving first bit of data on bus,<br>After data in rx_buffer is read back by software , hardware will continue to read slave and nak it at the end, then send re-start + address. |
| 5-0 | Rsv | RO | Reserved |

**Register Offset:** BA + 8h

**Register Name:** I2C1 Control Register

**Reset Value:** 00h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Sw_Inten | RX_Inten | TX_Inten | Nak_Inten | ARL_Inten | STP_Inten | STOP | NAKEn |

| Bit | Name | Attribute | Description |
|---|---|---|---|
| 7 | Sw_Inten | R/W | Slave write interrupt enable. When enabled, it will generate interrupt signal at slave mode to request software writing TX Data.<br>This bit is only needed at slave mode |
| 6 | RX_Inten | R/W | RX interrupt enable. When enabled, it will generate interrupt signal while RX Data buffer has data to be read |
| 7 | TX_Inten | R/W | TX interrupt enable. When enabled, it will generate interrupt signal while TX_Data or Tx_Addr was sent out successfully. |
| 4 | Nak_Inten | R/W | Nak Interrupt enable. When enabled, it will generate interrupt signal while master mode receive unpredictable “Nak” from outside slave |
| 3 | ARL_Inten | R/W | Arbitration loss interrupt enable. When enabled, it will generate interrupt signal while arbitration loss occurs |
| 2 | STP_Inten | R/W | Slave mode stop interrupt enable. When enabled, it will generate interrupt signal while slave mode is ended by outside master issuing STOP. |
| 1 | STP | R/W | Writing a 1 to this bit will cause the hardware to send NAK+Stop signal after current byte transfer. It will be auto cleared while STOP is sent out on the i2c bus. This should be used only when the device is a master. |
| 0 | NAKEn | R/W | 1: This causes the $I^2C$-bus controller to send an Nak after each byte.<br>0: This causes the $I^2C$-bus controller to send an Ack after each byte.<br>This bit is only needed at slave mode |

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**Register Offset:** BA + 9h

**Register Name:** I2C1 Status Register

**Reset Value:** 01h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Sw_Req | RX_Rdy | TX_Done | Nak_err | ARL | SlaveSTP | Bbusy | MS_ |

| Bit | Name | Attribute | Description |
|---|---|---|---|
| 7 | Sw_Req | R/WC | 1: Slave request software to write TX data<br>Write 1 to this bit will clear to “0” |
| 6 | RX_Rdy | R/WC | 1: Master/Slave has data to be read<br>Write 1 to this bit will clear to “0” |
| 5 | TX_Done | R/WC | 1: Master/Slave send TX_Address or TX data successfully<br>Write 1 to this bit will clear to “0” |
| 4 | Nak_err | R/WC | 1: Unpredictable Nak is received<br>Write 1 to this bit will clear to “0” |

| Bit | Name | Attribute | Description |
|---|---|---|---|
| 3 | ARL | R/WC | 1: Arbitration loss .<br>Write 1 to this bit will clear to “0” |
| 2 | SlaveSTP | R/WC | 1: Slave receive STOP condition<br>Write 1 to this bit will clear to “0” |
| 1 | BBUSY | RO | The bus is considered to be busy after the Start condition and free again at a certain time interval after the Stop condition. |
| 0 | MS_ | RO | 1 : Master mode (Default)<br>0 : Slave mode |

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**Register Offset:** BA + Ah

**Register Name:** I2C1 My_Address Register

**Reset Value:** 00h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| My Slave Address | | | | | | | Rsvd |

| Bit | Name | Attribute | Description |
|---|---|---|---|
| 7-1 | My_Addr | R/W | 7-bits slave address which is checked by internal slave module. If address is match it will switch to slave mode. Processor can write proper value into this register to identify itself |
| 0 | Rsvd | RO | Reserved |

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**Register Offset:** BA + Bh

**Register Name:** I2C1 Transmit Address Register

**Reset Value:** 00h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TX Slave Address | | | | | | | R/W |

| Bit | Name | Attribute | Description |
|---|---|---|---|
| 7-0 | TX_Addr | R/W | 8-bit address register for Master to start a transaction. Processor can write this register to generate START + Slave Address + R/W on i2c bus. If Processor write a macrocode into this register, it will send out macrocode and switch to high-speed mode at proper timing. |

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**Register Offset:** BA + Ch

**Register Name:** I2C1 Transmit/Receive Data Register

**Reset Value:** 00h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Data | | | | | | | |

| Bit | Name | Attribute | Description |
|---|---|---|---|
| 7-0 | Data | R/W | 8-bit data register for $I^2C$-bus Tx/Rx operation. Processor can write this register to transmit DATA or read this register to receive data |

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**Register Offset:** BA + Dh

**Register Name:** I2C1 Clock Frequency Control1

**Reset Value:** 0ah

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PreScale1 | | | | | | | |

| Bit | Name | Attribute | Description |
|---|---|---|---|
| 7-0 | PreScale1 | R/W | Processor can write this register value from 0 to 255 to control the frequency of SCLH<br>At high speed Mode, SCLH frequency = 33M÷(PreScale1),<br>PS: If PreScale1 < 10, SCLH frequency = 33M÷10 = 3.3Mhz |

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**Register Offset:** BA + Eh

**Register Name:** I2C1 Clock Frequency Control2

**Reset Value:** 88h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Fast | PreScale2 | | | | | | |

| Bit | Name | Attribute | Description |
|---|---|---|---|
| 7 | Fast | R/W | 1: Fast mode , 0: Standard Mode |
| 6-0 | PreScale2 | R/W | Processor can write this register value from 0 to 255 to control the frequency of SCL<br>At F/S Mode, SCL frequency = 33M÷(PreScale1) ÷(PreScale2+1) |

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**Register Offset:** BA + Fh

**Register Name:** I2C1 Extra Control Register

**Reset Value:** 00h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| I2c_RST | TX_hit_RX | Rsv | | | | | |

| Bit | Name | Attribute | Description |
|---|---|---|---|
| 7 | I2c_RST | R/W | Write “1” will reset i2c controller except pre-scale registers (for keep the speed setting). After reset, Controller will send out 10 dummy clocks to ensure no any slave driving data because of incomplete operation of the Master (maybe other master), auto clear after reset complete. |
| 6 | TX_hit_RX | R/O | Indicate the TX address is written but may not send out because the slave is driving first bit of data on bus,<br>After data in rx_buffer is read back by software , hardware will continue to read slave and nak it at the end, then send re-start + address. |
| 5-0 | Rsv | RO | Reserved |