power

File: power.kicad_sch

Connectors

File: connector.kicad_sch

Ethernet

File: ethernet.kicad_sch

wiredmbus

File: mbus.kicad_sch

SDCard

File: sdcard.kicad_sch

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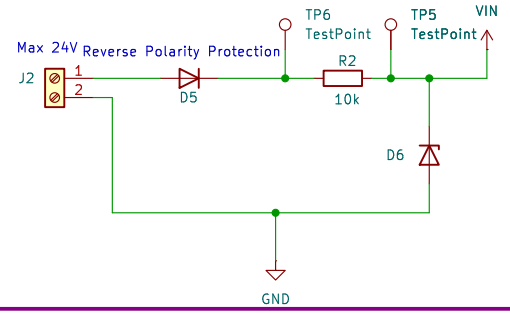
Deigned By: Jones Kisaka
Abstract Machines

Sheet: /
File: s0-base-board.kicad_sch

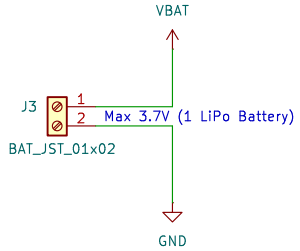
Title: S0 Base Board

Size: A4	Date: 2025-02-26	**Rev: v0.1.0**
KiCad E.D.A. 9.0.2		Id: 1/6

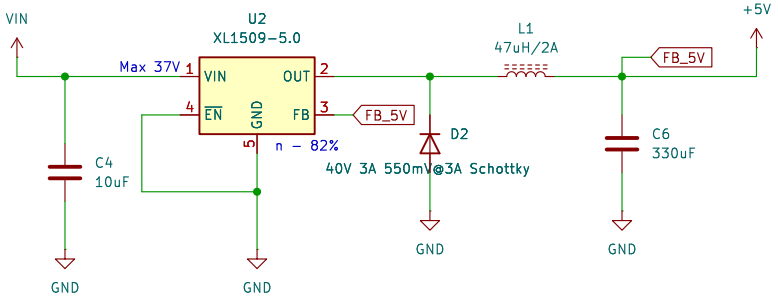
Reverse Polarity Protection



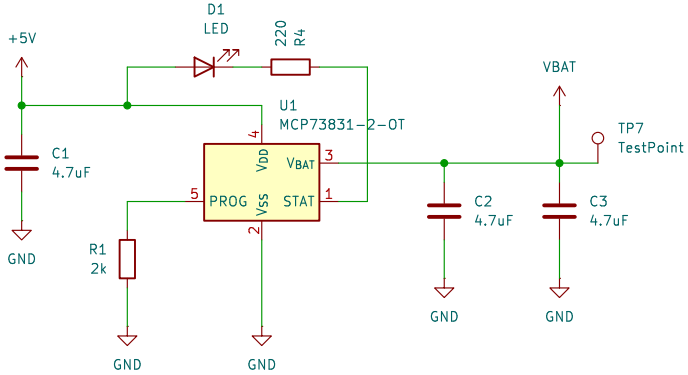
BAT



VIN – 5V CONV



BATTERY CHARGER



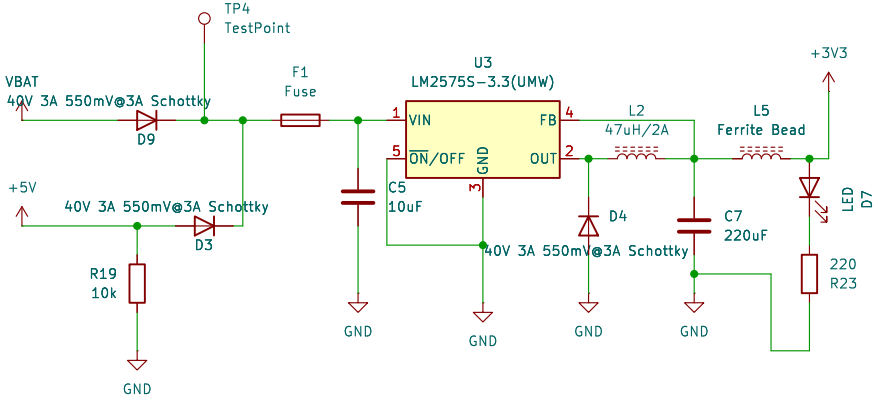
CURRENT REGULATION SET
Fast charge current regulation can be scaled by placing
a programming resistor (RPROG) from the PROG input
to VSS. The program resistor and the charge current
are calculated using the following equation:

Ireg = 1000V/Rprog

where: Rprog is in kOhms
Ireg is charging current in milliamps.

Ireg = 1000V/2
= 500mA

5V – 3.3V CONV



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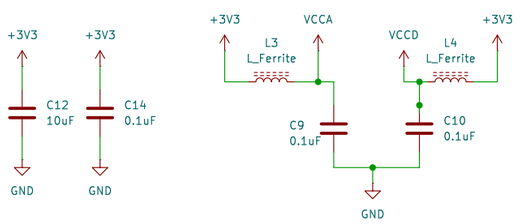
Sheet: /power/
File: power.kicad_sch

Title: S0 Base Board

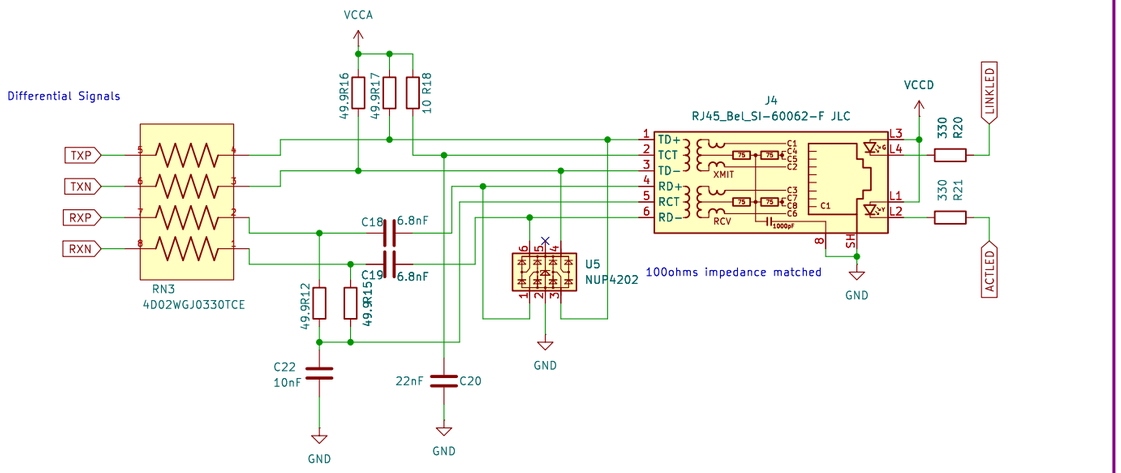
Size: A4	Date: 2025-02-26	**Rev: v0.1.0**
KiCad E.D.A. 9.0.2		Id: 2/6

DECOUPLING CAPS

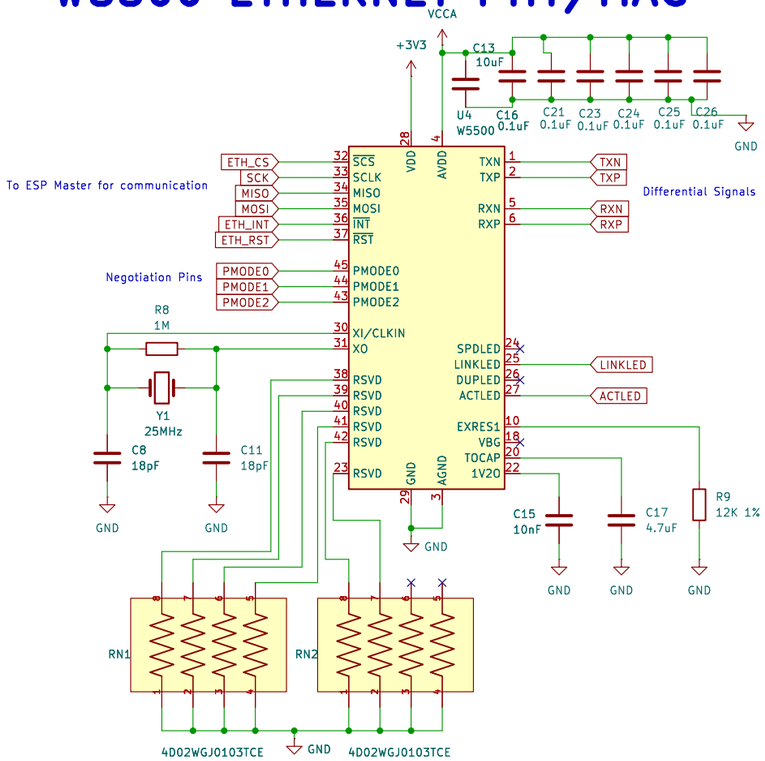
Decoupling Caps help ensure stable operation
Filtering noise
Maintain a steady power supply.



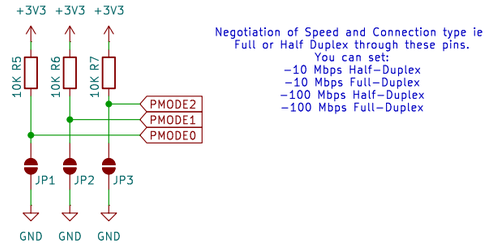
JACK & MAGNETICS



W5500 ETHERNET PHY/MAC



AUTO-NEGOTIATING MODES



Negotiation of Speed and Connection type ie
Full or Half Duplex through these pins.
You can set:
-10 Mbps Half-Duplex
-10 Mbps Full-Duplex
-100 Mbps Half-Duplex
-100 Mbps Full-Duplex

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File: ethernet.kicad_sch

Title: S0 Base Board

Size: A3	Date: 2025-02-26	**Rev: v0.1.0**
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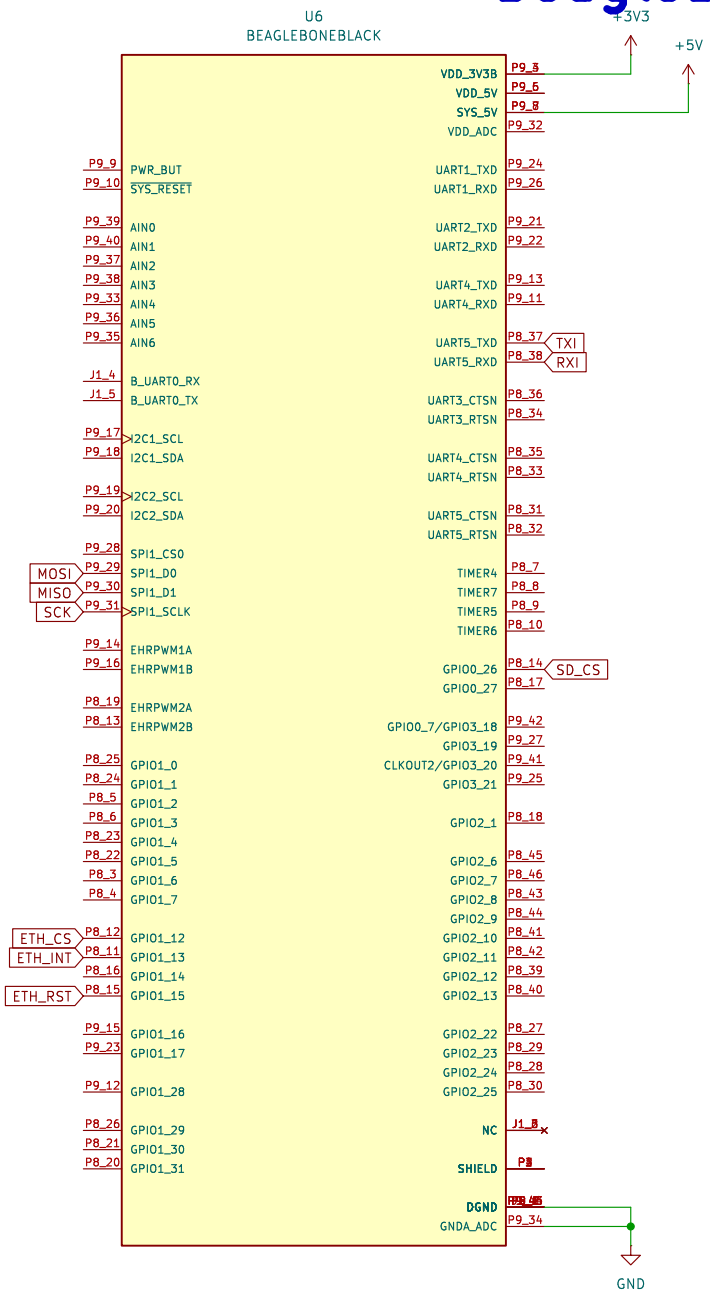
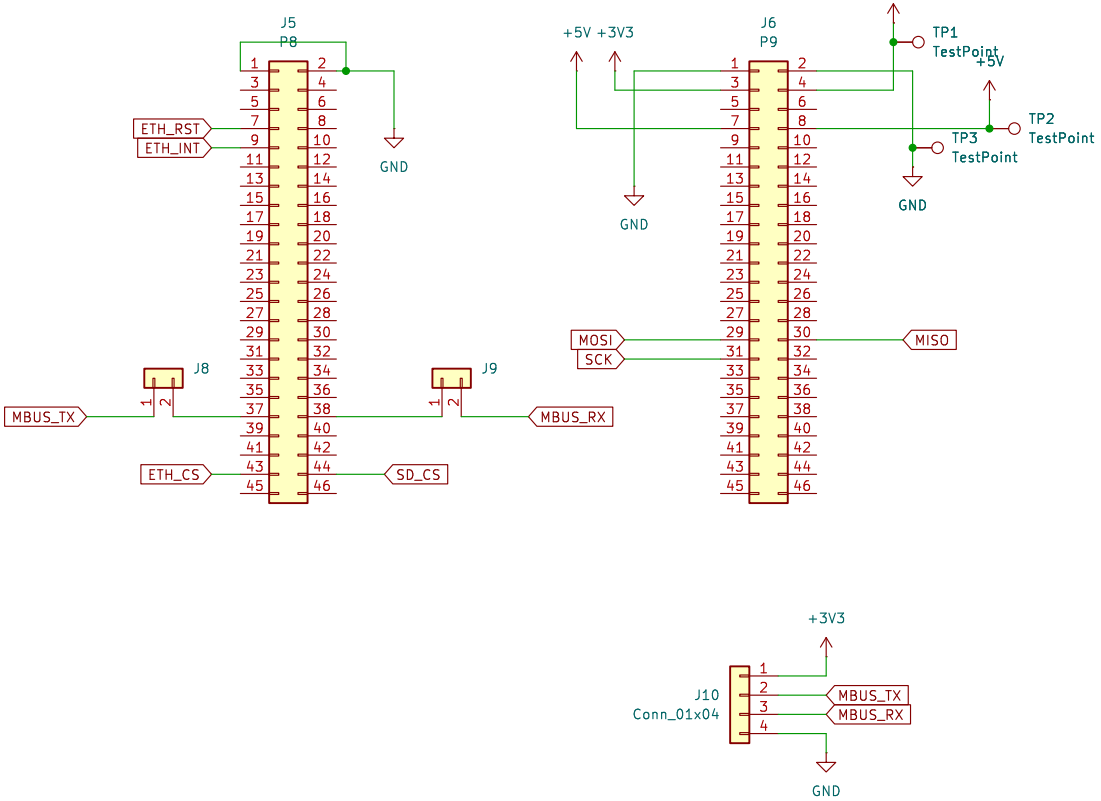
BeagleBone Cape Board



Female Pin Headers connected to the BeagleBone Cape



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Sheet: /Connectors/
File: connector.kicad_sch

Title: S0 Base Board

Size: A4	Date: 2025-02-26	**Rev: v0.1.0**
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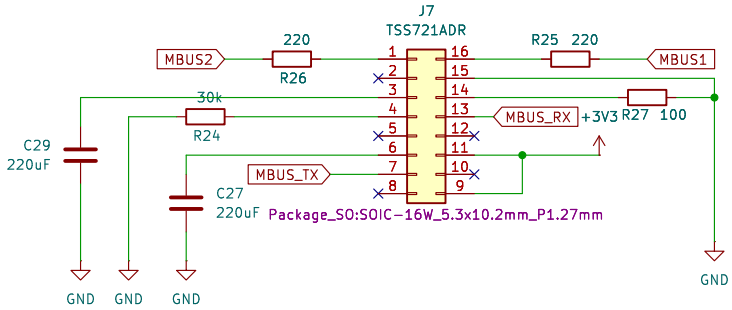

PIN	NAME	DESCRIPTION
1	BUSL2	Meter-Bus
2	VB	Differential Bus Voltage after Rectifier
3	STC	Support Capacitor
4	RIDD	Current Adjust Input
5	PF	Power Fail Output
6	SC	Sampling Capacitor
7	MBUS_TX	Data Output Inverted
8	TX	Data Output
9	BAT	Logic Level Adjust
10	VS	Switch for Bus or Battery Supply output
11	VDD	Voltage Regulator Output
12	RX	Data Input
13	MBUS_RX	Data Input Inverted
14	RIS	Adjust input for modulation current
15	GND	Ground
16	BUSL1	Meter-Bus

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Sheet: /wiredmbus/
File: mbus.kicad_sch

Title: S0 Base Board

Size: A4	Date: 2025-02-26	**Rev: v0.1.0**
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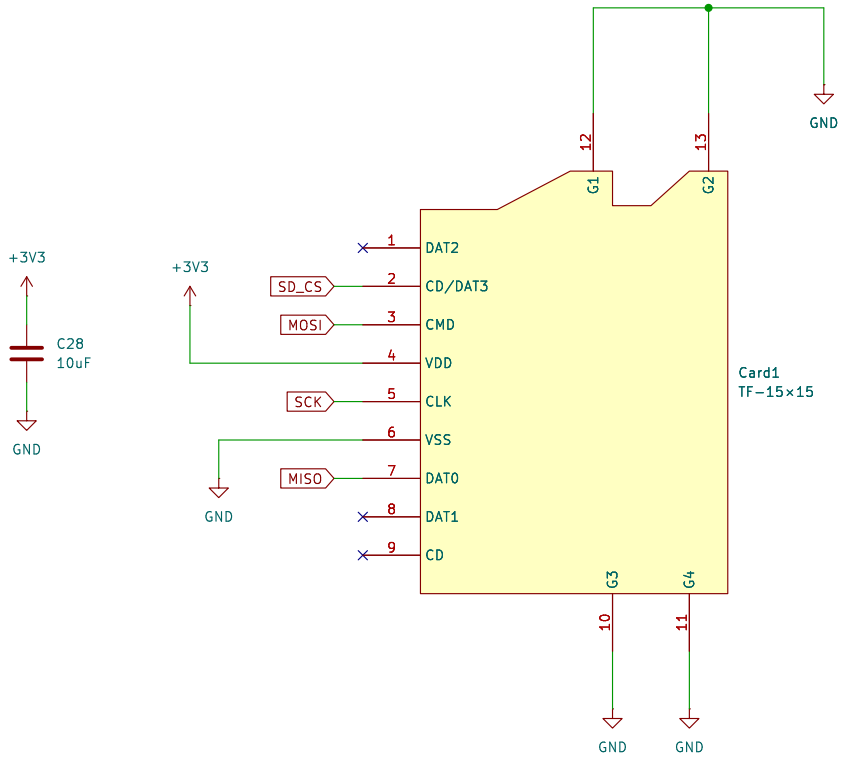

SD Domain to SPI Domain Conversion Table.

PIN	SD DOMAIN	SPI DOMAIN
1	DAT2	NC
2	CD/DAT3	CHIP SELECT
3	CMD/DATA IN	MOSI
4	VDD	VDD
5	CLK	SERIAL CLOCK
6	VSS	GROUND
7	DAT0/DATA OUT	MISO
8	DAT1	NC
9	CD	NC

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Title: S0 Base Board

Size: A4	Date: 2025-02-26	**Rev: v0.1.0**
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