



Digital Design Verification

Lab Manual # 40 – Integrating Multiple UVCs

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Submitted To: NCDC

Release: 1.0

Date: 8-Aug-2024

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Task 1: Integrating Multiple UVC

Running Base Test

- 1. For every UVC (YAPP, Clock and reset, HBUS and Channel) add the following to your run.f.
 - An incdir reference to the UVC sv directory (depending upon the location of UVC in reference to your current working directory)
 - UVC package filename.
 - UVC interface filename.
- 2. Run a simulation with <code>base_test</code> only. Check the topology report carefully to make sure all of your UVCs are instantiated and configured correctly. Copy the topology report into a new file for future reference.

Name uvm_test_top env chan0 rx_agent driver rsp_port recording seq_item_po recording d monitor item collect recording channel_id checks_enab coverage ent recording_de sequencer rsp_export recording	ba: roi chi chi uvi _detail in rt uvi _detail in ini			
uvm_test_top env chan0 rx_agent driver rsp_port recording seq_item_po recording_dchannel_id recording channel_id recording channel_id checks_enab coverage_en recording_dcsequencer rsp_export	ba: roi cha cha cha uvr _detail inv rt uvr _detail inv _inv	se_test uter_tb annel_env annel_rx_agent annel_rx_driver m_analysis_port teoral		@2942 @3026 @3111 @3294
env chan0 rx_agent driver rsp_port recording seq_item_po recording channel_id recording dimonitor item_collect recording channel_id checks_enab coverage_ent recording_desequencer rsp_export	roi cha cha cha uvi _detail in rt uvi _detail in _in	uter_tb annel_env annel_rx_agent anel_rx_driver m_analysis_port teoral		@3026 @3111 @3294
chan0 rx_agent driver rsp_port recording seq_item_po recording_d monitor item_collec: recording_d channel_id checks_enab coverage_en recording_d sequencer rsp_export	cha cha cha uvr _detail in rt uvr _detail in in	annel_env annel_rx_agent annel_rx_driver m_analysis_port tegral		@3111 @3294
driver rsp_port recording seq_item_po recording_d recording_d monitor item_collec recording channel_id checks_enab coverage_en recording_d sequencer rsp_export	cha cha uvn _detail in rt uvn _detail in in	annel_rx_agent annel_rx_driver m_analysis_port tegral		
driver rsp_port recording seq_item_po recording_d recording_d monitor item_collec recording channel_id checks_enab coverage_en recording_d sequencer rsp_export	cha uvr _detail in rt uvr _detail in in	annel_rx_driver m_analysis_port tegral		64662
recording seq_item_po recording channel_id recording_d monitor item_collec recording channel_id checks_enab coverage_en recording_d sequencer rsp_export	uvr _detail in rt uvr _detail in in	m_analysis_port tegral		
recording seq_item_po recording channel_id recording_d monitor item_collec recording channel_id checks_enab coverage_en recording_d sequencer rsp_export	rt uvi _detail in _in			@4153
seq_item_po recording channel_id recording_d monitor item_collec recording channel_id checks_enab coverage_en recording_d sequencer rsp_export	rt uv _detail in _in	m seq item pull port		'd1
channel_id recording_d monitor item_collec recording channel_id checks_enab coverage_en recording_d sequencer rsp_export	_detail in in		t -	@4104
recording_d monitor item_collec recording channel_id checks_enab coverage_en recording_d sequencer rsp_export		tegral	32	'd1
monitor item_collec recording channel_id checks_enab coverage_en recording_d sequencer rsp_export	atail in	tegral	32	'h0
item_collec recording channel_id checks_enab coverage_en recording_d sequencer rsp_export	ctart iii	tegral	32	'd1
recording channel_id checks_enab coverage_en recording_d sequencer rsp_export	cha	annel_rx_monitor		@3285
channel_id checks_enab coverage_en recording_d sequencer rsp_export	ted_port uv	m_analysis_port		@3383
checks enab coverage en recording d sequencer rsp_export	_detail in	tegral	32	'd1
coverage_en recording_d sequencer rsp_export	in ⁻	tegral	32	'h0
recording_d sequencer rsp_export	le in	tegral	1	'h1
sequencer rsp_export		tegral	1	'h1
rsp_export	etail in	tegral	32	'd1
	cha	annel_rx_sequencer m_analysis_export		@3358
recording	uvr	m_analysis_export		@3473
		tegral	32	'd1
seq_item_ex		m_seq_item_pull_imp		@4023
recording		tegral	32	'd1
recording_d		tegral	32	'd1
arbitration		ray	0 0	
lock_queue		ray tegral	32	- 'd1
num_last_re		tegral	32	'd1
num_last_rs is active				UVM ACTIVE
recording_deta		m_active_passive_enu tegral	32	'd1
channel id		tegral	32	'h0
checks enable		tegral	1	'h1
coverage enable		tegral	1	'h1
recording detai		tegral	32	'd1
chan1	ch	annel env	-	@3088
rx agent	ch	annel_rx_agent annel_rx_driver		@4207
driver	ch	annel rx driver		@4896
rsp port	uvi	m_analysis_port		@5041
recording	detail in	tegral	32	'd1
seq item po		m seq item pull port		@4993
recording		tegral	32	'd1
channel id		tegral	32	'h1
recording d		tegral	32	'd1
monitor		annel_rx_monitor		@4204
item_collec		m_analysis_port		@4291
recording		tegral	32	'd1







	OUTPUT DEBUG CONSOLE	TERMINAL PORTS TEROSHDL: L	OC DED	ORT TEROSHDL: TIMING
		TERMINAL PORTS TEROSHDE: L	.UG KEPI	
	item collected port	uvm analysis port		@5177
	recording detail	integral	32	'd1
	channel id	integral	32	'h2
	checks enable	integral	1	'h1
	coverage enable	integral	ī	'h1
	recording detail	integral	32	'd1
	sequencer	channel rx sequencer	-	@5157
	rsp export	uvm_analysis_export		@5262
	recording detail	integral	32	'd1
	seq item export	uvm seq item pull imp	-	@5802
	recording detail	integral	32	'd1
	recording detail	integral	32	'd1
	arbitration queue	array	0	-
	lock queue	array	0	
	num last regs	integral	32	'd1
	num_last_rsps	integral	32	'd1
	is active	uvm active passive enum	1	UVM ACTIVE
	recording detail	integral	32	'd1
	annel id	integral	32	'h2
	ecks enable	integral	1	'h1
	verage enable	integral	1	'h1
			32	'd1
	cording_detail	integral	32	
clkr		clock_and_reset_env		@3200
	ent	clock_and_reset_agent		@5978
	driver	clock_and_reset_driver		@6009
	rsp_port	uvm_analysis_port	-	@6110
	recording_detail	integral	32	'd1
	seq_item_port	uvm_seq_item_pull_port		@6059
	recording_detail	integral	32	'd1
	recording_detail	integral	32	'd1
	sequencer	clock and reset sequencer		@6089
	rsp_export	uvm analysis export		@6199
	recording detail	integral	32	'd1
	seq item export	uvm seq item pull imp		@6747
	recording detail	integral	32	'd1
	recording detail	integral	32	'd1
	arbitration queue	array	0	
	lock queue	array	0	
	num_last_reqs	integral	32	'd1
	num last rsps	integral	32	'd1
	recording detail	integral	32	'd1
		integral	32	'd1
hbus	cording_detail		-	
	stors[0]	hbus_env		@3217 @5883
	sters[0]	hbus_master_agent		@6883
	driver	hbus_master_driver		@7502
	rsp_port	uvm_analysis_port		@7653
	recording_detail	integral	32	'd1
	seq_item_port	uvm_seq_item_pull_port		@7604
	recording_detail	integral	32	'd1
	random_delay	integral	1	'h0
	master_id	integral	32	'h0
	recording_detail	integral	32	'd1
	sequencer	hbus master sequencer		@6915
		uvm analysis export		@6975
	rsp_export			
	rsp_export recording_detail	integral	- 32	'd1
vad objects	rsp_export			
xed objects	rsp_export recording_detail	integral	- 32	'd1
xed objects	rsp_export recording_detail seq item export	integral uvm seq item pull imp	- 32 -	'd1 @7523
xed objects	rsp_export recording_detail seq_item_export recording_detail	integral uvm seq item pull imp	- 32 -	'd1 @7523 'd1
xed objects	rsp_export recording_detail seq_item_export recording_detail seq_item_port	integral uvm seq item pull imp integral uvm seq_item_pull_port	- 32 - 32	'd1 @7523 'd1 @7604
ed objects	rsp_export recording_detail seq_item_export recording_detail seq_item_port recording_detail	integral uvm seq item pull imp integral uvm_seq_item_pull_port integral	32 - 32 - 32	'd1 @7523 'd1 @7604 'd1
xed objects	rsp_export recording_detail seq_item_export recording_detail seq_item_port recording_detail random_delay	integral uvm seq item pull imp integral uvm_seq_item_pull_port integral integral integral	32 - 32 - 32 1	'd1 @7523 'd1 @7604 'd1 'h0
ed objects	rsp_export recording_detail seq_item_export recording_detail seq_item_port recording_detail random_delay master_id	integral uvm seq item pull imp integral uvm_seq_item_pull_port integral integral integral integral	32 - 32 - 32 1 32	'd1 @7523 'd1 @7604 'd1 'h0
n.e.	recording_detail seq_item_export recording_detail seq_item_port recording_detail random_delay master_id recording_detail	integral uvm seq item pull imp integral uvm seq item_pull_port integral integral integral integral integral integral	32 - 32 - 32 1 32 32 32	'd1 @7523 'd1 @7604 'd1 'h0 'h0
n.e.	rsp_export recording_detail seq_item_export recording_detail seq_item_port recording_detail random_delay master_id recording_detail equencer	integral uvm seq item pull imp integral uvm seq item_pull_port integral integral integral integral hbus_master_sequencer	32 - 32 - 32 1 32 32 -	'd1 @7523 'd1 @7604 'd1 'h0 'h0 'd1 @6915
n.e.	rsp_export recording_detail seq_item_export recording_detail seq_item_port recording_detail random_delay master_id recording_detail equencer rsp_export	integral uvm seq item pull imp integral uvm_seq_item_pull_port integral integral integral integral integral inbus_master_sequencer uvm_analysis_export	32 - 32 - 32 1 32 32 32	'd1 @7523 'd1 @7604 'd1 'h0 'h0 'd1 @6915 @6975
n.e.	rsp_export recording_detail seq_item_export recording_detail seq_item_port recording_detail random_delay master_id recording_detail equencer rsp_export recording_detail	integral uvm seq item pull imp integral uvm seq item_pull_port integral integral integral integral hbus master_sequencer uvm_analysis_export integral	32 - 32 - 32 1 32 32 - - 32 32	'd1 @7523 'd1 @7604 'd1 'h0 'd1 @6915 @6975 'd1
n e	rsp_export recording_detail seq_item_export recording_detail seq_item_port recording_detail random_delay master_id recording_detail equencer rsp_export recording_detail seq_item_export	integral uvm seq item pull imp integral uvm seq item pull port integral integral integral integral hbus master sequencer uvm analysis export integral uvm_seq_item_pull_imp	32 - 32 - 32 1 32 32 - - 32 -	'd1 @7523 'd1 @7604 'd1 'h0 'd1 @6915 @6975 'd1 @7523
n e	recording_detail seq_item_export recording_detail seq_item_port recording_detail random_delay master_id recording_detail equencer rsp_export recording_detail seq_item_export recording_detail	integral uvm seq item pull imp integral uvm_seq_item_pull_port integral integral integral integral integral integral integral integral integral uvm_analysis_export integral uvm_seq_item_pull_imp integral	32 - 32 - 32 1 32 32 - 32 - 32	'd1 @7523 'd1 @7604 'd1 'h0 'h0 'd1 @6915 @6975 'd1 @7523
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n e	rsp_export recording_detail seq_item_export recording_detail seq_item_port recording_detail random_delay master_id recording_detail equencer rsp_export recording_detail seq_item_export recording_detail seq_item_export recording_detail arbitration_queue	integral uvm seq item pull imp integral uvm seq item_pull_port integral integral integral integral integral bus master_sequencer uvm_analysis_export integral uvm_seq_item_pull_imp integral integral integral integral integral integral integral integral array	32 - 32 1 32 32 - 32 32 - 32 32 - 32 0	'd1 @7523 'd1 @7604 'd1 'h0 'd1 @6915 @6975 'd1 @7523 'd1 'd1
n e	recording detail seq item export recording_detail seq item_port recording_detail random delay master_id recording_detail equencer rsp_export recording_detail seq_item_export recording_detail recording_detail recording_detail recording_detail recording_detail arbitration_queue lock_queue	integral uvm seq item pull imp integral uvm_seq_item_pull_port integral integral integral integral integral integral integral integral ivm_seq_item_pull_imp integral ivm_seq_item_pull_imp integral integral integral integral integral array array	32 - 32 1 32 - 32 - 32 - 32 0 0	'd1 @7523 'd1 @7604 'd1 'h0 'h0 'd1 @6915 @6975 'd1 'd1 'd1
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s	recording_detail seq_item_export recording_detail seq_item_port recording_detail random_delay master_id recording_detail equencer resp_export recording_detail seq_item_export recording_detail seq_item_export recording_detail arbitration_queue lock_queue num_last_resps	integral uvm seq item pull imp integral uvm seq item_pull_port integral integral integral integral integral bus master sequencer uvm_analysis_export integral uvm_seq_item_pull_imp integral integral array array integral integral array integral integral integral integral integral integral integral integral integral	32 - 32 - 32 1 32 32 - - 32 32 0 0 32 32 32	'd1 @7523 'd1 @7604 'd1 'h0 'h0 'd1 @6915 @6975 'd1 @7523 'd1 'd1
S	recording detail seq item export recording_detail seq_item_port recording_detail random_delay master_id recording_detail equencer rsp_export recording_detail seq_item_export recording_detail respiration_queue lock_queue num_last_resps_onitor	integral uvm seq item pull imp integral uvm_seq_item_pull_port integral	32 - 32 1 32 32 32 - 32 - 32 - 32 - 32 -	'd1 @7523 'd1 @7604 'd1 'h0 'h0 'd1 @6915 @6975 'd1 'd1 'd1 '-
s m i	recording detail seq item export recording_detail seq item_port recording_detail recording_detail random delay master_id recording_detail equencer rsp_export recording_detail seq_item_export recording_detail recording_detail recording_detail arbitration_queue lock_queue num_last_reqs_num_last_rsps_ionitor s_active	integral uvm seq item pull imp integral uvm_seq_item_pull_port integral integral integral integral integral ivm_seq_item_pull_imp integral uvm_seq_item_pull_imp integral	32 - 32 - 32 1 32 32 - 32 - 32 - 32 - 32	'd1 @7523 'd1 @7604 'd1 'h0 'h0 'd1 @6915 @6975 'd1 @7523 'd1 'd1 - 'd1 'e6799 UVM_ACTIVE
s m i	rsp_export recording_detail seq_item_export recording_detail seq_item_port recording_detail random_delay master_id recording_detail equencer rsp_export recording_detail seq_item_export recording_detail seq_item_export recording_detail arbitration_queue lock_queue num_last_rsps num_last_rsps onitor s_active aster_id	integral uvm seq item pull imp integral uvm seq item_pull_port integral integral integral integral integral integral integral integral uvm seq item_pull_imp integral uvm seq item_pull_imp integral integral array array integral	32 - 32 - 32 1 32 - 32 - 32 - 32 - 32 -	'd1 @7523 'd1 @7604 'd1 'h0 'h0 'd1 @6915 @6975 'd1 @7523 'd1 'd1
s m i m r	rsp_export recording_detail seq_item_export recording_detail seq_item_port recording_detail random_delay master_id recording_detail equencer rsp_export recording_detail seq_item_export recording_detail recording_detail recording_detail recording_detail recording_detail recording_detail recording_detail respective in export respective in export respective in export respective in export recording_detail recording_detail seq_item_export recording_detail recording_detail	integral uvm seq item pull imp integral uvm_seq_item_pull_port integral	32 - 32 - 32 1 32 - 32 - 32 - 32 - 32 -	'd1 @7523 'd1 @7604 'd1 'h0 'h0 'd1 @6915 @6975 'd1 'd1 'd1 'd1 'd1 'd1 'd1 'd1 'd1 'd1
m i m mon	recording detail seq item export recording_detail seq item_port recording_detail recording_detail random delay master_id recording_detail seq_item_export recording_detail seq_item_export recording_detail recording_detail recording_detail recording_detail recording_detail recording_detail recording_detail recording_detail resording_detail resording_detail recording_detail recording_detail recording_detail recording_detail recording_detail recording_detail recording_detail recording_detail recording_detail	integral uvm seq item pull imp integral uvm_seq_item_pull_port integral integral integral integral integral integral uvm_seq_item_pull_imp integral uvm_seq_item_pull_imp integral hbus_monitor uvm_active_passive_enum integral hbus_monitor	32 - 32 1 32 32 - 32 32 - 32 32 - 32 32 - 32 32 - 32 32 - 1 32 32 - 1 32 32 - 1	'd1 @7523 'd1 @7604 'd1 'h0 'h0 'd1 @6915 @6975 'd1 @7523 'd1 'd1 'd1 '- 'd1 'd1 'e6799 UVM_ACTIVE 'h0 'd1 @6799
m i m mon	rsp_export recording_detail seq item export recording_detail seq_item_port recording_detail random_delay master_id recording_detail equencer rsp_export recording_detail seq_item_export recording_detail seq_item_export recording_detail arbitration_queue lock_queue num_last_resps num_last_rsps onitor s_active uster_id ecording_detail itor item_collected_port	integral uvm seq item pull imp integral uvm_seq_item_pull_port integral integral integral integral integral integral uvm_seq_item_pull_imp integral uvm seq_item_pull_imp integral	32 - 32 1 32 32 - 32 32 0 0 32 32 . 1 32 32	'd1 @7523 'd1 @7604 'd1 'h0 'h0 'd1 @6915 @6975 'd1 @7523 'd1 'd1 '- 'd1 'd1 'e6799 UVM_ACTIVE 'h0 'd1 'e6799 @6849
m i m r mon i	recording detail seq item export recording_detail seq item port recording_detail seq_item_port recording_detail random_delay master id recording_detail equencer rsp_export recording_detail seq_item_export recording_detail itor tem_collected_port recording_detail	integral uvm seq item pull imp integral uvm_seq_item_pull_port integral hous_monitor uvm_active_passive_enum integral integral hous monitor uvm_analysis_port integral	32 - 32 1 32 32 - 32 32 - 32 32 - 32 32 - 32 32 32 - 32 32 32 - 32 32 32 32 32 32 32 32 32 32 32 32 32	'd1 @7523 'd1 @7604 'd1 'h0 'h0 'd1 @6915 @6975 'd1 'd1 'd1 'd1 'd1 'd1 'e6799 UVM ACTIVE 'h0 'd1 (e6799 @6849 'd1
m i m r mon i c	recording detail seq item export recording_detail seq item port recording_detail seq_item_port recording_detail random delay master_id recording_detail equencer rsp_export recording_detail seq_item_export recording_detail recording_detail recording_detail arbitration_queue lock_queue num_last_resps_ounlion s_active_detail recording_detail recording_detail recording_detail itor tem_collected_port recording_detail itor tem_collected_port recording_detail hecks_enable	integral uvm seq item pull imp integral uvm_seq_item_pull_port integral integral integral integral integral integral uvm_seq_item_pull_imp integral uvm_seq_item_pull_imp integral hbus_monitor uvm_active_passive_enum integral hbus_monitor uvm_analysis_port integral	32 - 32 1 32 32 - 32 32 0 0 32 32 - 1 32 - 1 32 32 - 1 32 32 - 1 32 32 - 1 32 32 - 1 32 32 - 1 32 32 - 1 3	'd1 @7523 'd1 @7604 'd1 'h0 'h0 'd1 @6915 @6975 'd1 @7523 'd1 'd1 'd1 '- 'd1 'd1 'e6799 UVM_ACTIVE 'h0 'd1 'd1 'd6799 @6849 'd1 'h1
m i m r mon i c	rsp_export recording_detail seq item export recording_detail seq_item_port recording_detail random_delay master_id recording_detail equencer rsp_export recording_detail seq_item_export recording_detail seq_item_export recording_detail arbitration_queue lock_queue num_last_rsps onitor s_active aster_id ecording_detail itor tem_collected_port recording_detail itor tem_collected_port recording_detail hecks_enable overage_enable	integral uvm seq item pull imp integral uvm_seq_item_pull_port integral integral integral integral integral integral integral integral ivm seq_item_pull_imp integral	32 - 32 1 32 - 32 - 32 - 32 32 - 32 32 - 32 32 1 32 32 1 1 1 1	'd1 @7523 'd1 @7604 'd1 'h0 'h0 'd1 @6915 @6975 'd1 @7523 'd1 'd1 'd1 - 'd1 'd1 - 'd1 'd1 'd1 - 'd1 'd1 'd1 'd1 - 'd1
m i i m r mon i c c	recording detail seq item export recording_detail seq item port recording_detail seq_item_port recording_detail random_delay master id recording_detail equencer rsp_export recording_detail seq_item_export recording_detail seq_item_export recording_detail arbitration_queue lock_queue num_last_reqs num_last_resps sonitor s_active laster id lecording_detail itor tem_collected_port recording_detail hecks_enable lecording_detail ecording_detail ecording_detail	integral uvm seq item pull imp integral uvm_seq_item_pull_port integral	32 - 32 1 32 32 32 - 32 32 32 32 32 32 32 32 32 32 32 32 32	'd1 @7523 'd1 @7604 'd1 'h0 'h0 'd1 @6915 @6975 'd1 'd1 'd1 'd1 'd1 'd1 'e6799 UVM ACTIVE 'h0 'd1 (e6799 (e6849 'd1 'h1 'h1
m i m r mon i c c c n	recording detail seq item export recording_detail seq_item_port recording_detail masters	integral uvm seq item pull imp integral uvm_seq_item_pull_port integral	32 - 32 1 32 32 32 9 0 0 32 2 - 1 1 32 32 32 1 1 1 32 32 32 32 32 32 32 32 32 32	'd1 @7523 'd1 @7604 'd1 'h0 'h0 'h0 'd1 @6915 @6975 'd1 @7523 'd1 'd1 'd1 '- 'd1 'e6799 UVM_ACTIVE 'h0 'd1 @6799 @6849 'd1 'h0 'h1 'h1 'h1
m im r mon i c c r num num	rsp_export recording_detail seq item export recording_detail seq_item_port recording_detail recording_detail recording_detail recording_detail equencer rsp_export recording_detail seq_item_export recording_detail recording_detail arbitration_queue lock_queue num_last_resp num_last_resp sonitor s_active aster_id ecording_detail itor tem_collected_port recording_detail itor tem_collected_port recording_detail hecks_enable overage_enable ecording_detail _masters _slaves	integral uvm seq item pull imp integral uvm_seq_item_pull_port integral integral integral integral integral integral integral integral ivm seq_item_pull_imp integral	32 - 32 1 32 32 - 32 32 9 0 0 32 32 32 - 32 32 1 1 32 32 32 32 32 32 32 32 32 32 32 32 32	'd1 @7523 'd1 @7604 'd1 'h0 'h0 'd1 @6915 @6975 'd1 @7523 'd1
m i m ron i cl c r num num che	recording detail seq item export recording_detail seq_item_port recording_detail masters	integral uvm seq item pull imp integral uvm_seq_item_pull_port integral	32 - 32 1 32 32 32 9 0 0 32 2 - 1 1 32 32 32 1 1 1 32 32 32 32 32 32 32 32 32 32	'd1 @7523 'd1 @7604 'd1 'h0 'h0 'h0 'd1 @6915 @6975 'd1 @7523 'd1 'd1 'd1 '- 'd1 'e6799 UVM_ACTIVE 'h0 'd1 @6799 @6849 'd1 'h0 'h1 'h1 'h1







```
@7705
  agent
                             yapp_agent
    driver
                            yapp_driver
uvm analysis port
                                                                @7868
     rsp port
       recording detail
                            integral
      seq_item_port
                            uvm seq item pull port
       recording_detail
                             integral
      recording_detail
                             integral
                             yapp_monitor
                                                               @7740
'd1
    monitor
     recording detail
                            integral
                                                                @7847
                            yapp_sequencer
    sequencer
      rsp export
                            uvm analysis export
                                                                @7957
       recording detail
                            integral
      seq item export
                            uvm seq item pull imp
                                                                @8505
        recording_detail
                            integral
      recording_detail
                             integral
      arbitration_queue
     lock_queue
num_last_reqs
                            array
                                                         32
                            integral
     num last rsps
                            integral
    is_active
                            uvm active passive enum
                                                                UVM ACTIVE
    recording_detail
                             integral
  recording_detail
                             integral
recording_detail
                             integral
```

Running Simple Test

- 3. Run a simulation in GUI mode using simple_test and verify as follows:
 - a. Add YAPP UVC monitor transactions to the waveform viewer.
 - b. Add all three Channel UVC monitor transactions to the waveform viewer.
 - c. Use the transactions to confirm packets are passed correctly through the router and collected at the right channel.

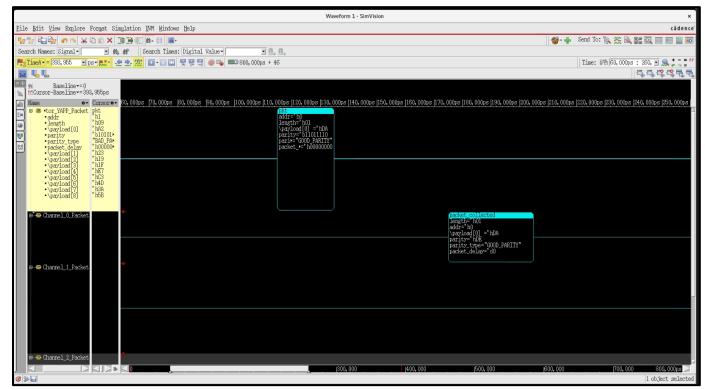


Figure 1-Channel 0





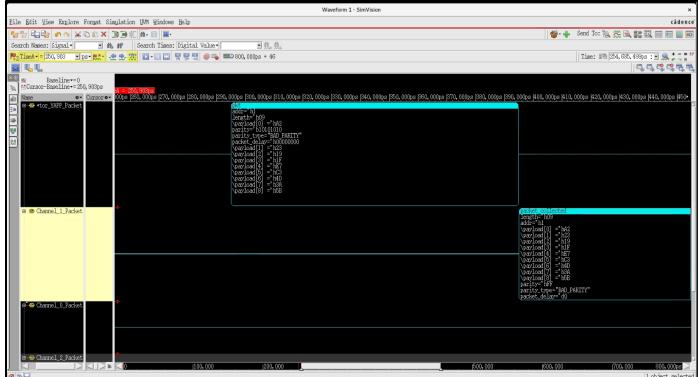


Figure 2-Channel 1

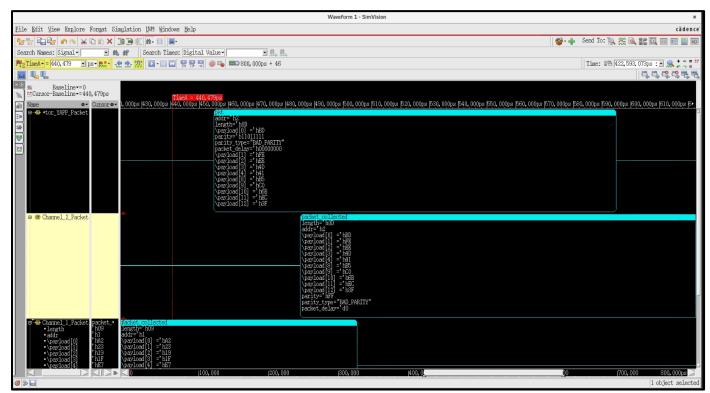


Figure 3-Channel 3





Further Integration Testing

4. Write a new YAPP sequence in the yapp/sv/yapp_tx_seqs.sv file to generate packets for all four channels (including the illegal address 3). The packets should have incrementing payload sizes from 1 to 22 and parity distribution of 20% bad parity (88 packets in total).

Hint: You could create packets using nested loops for address and payload.

- 5. Create a new test, test_uvc_integration, in the router_test_lib.sv file to perform the following:
 - a. Set the run_phase default sequence of the YAPP UVC to the sequence created above.
 - b. Set the run_phase default sequence of the HBUS UVC to set up the router with register field maxpktsize = 20 and enable the router (register field router_en = 1).

Hint: There is a sequence defined for this in the HBUS master sequences hbus_master_seqs.sv.

Hint: The hierarchical path name for the HBUS configuration setting can be read from the topology report.

6. Run a simulation and check the results to see that the three channels are properly addressed, that there is an error signal when parity is wrong, and that packets are dropped if bigger than maxpktsize or have illegal addresses.

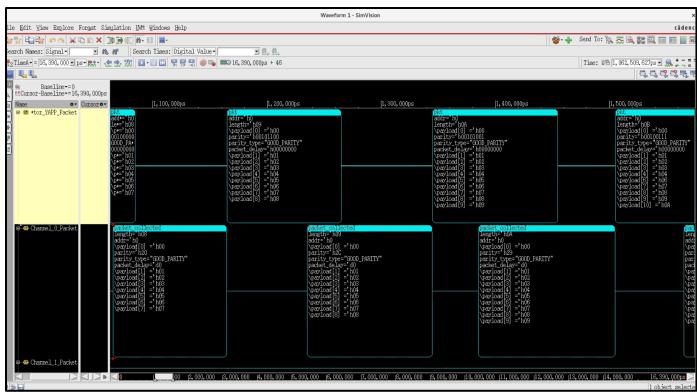


Figure 4-Channel 0





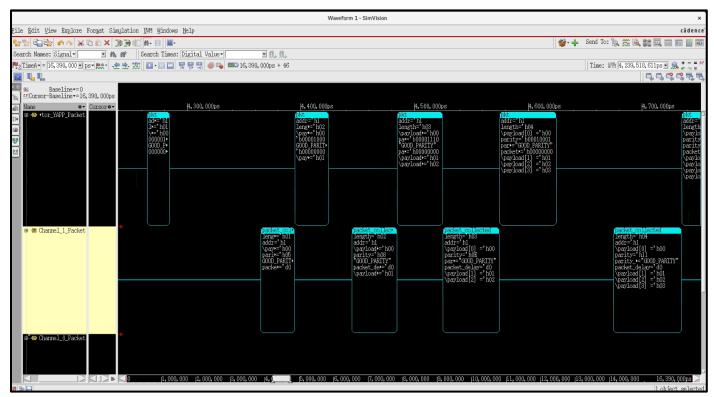


Figure 5-Channel 1

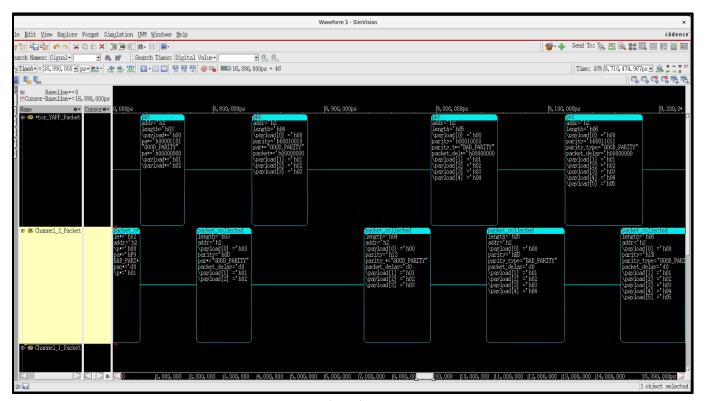


Figure 6-Channel 2





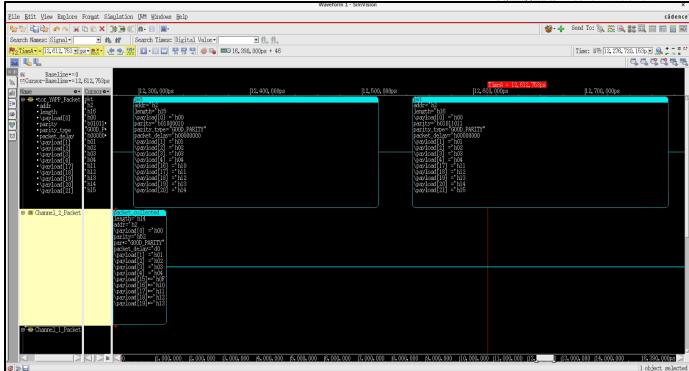


Figure 7-Packet size greater than 20

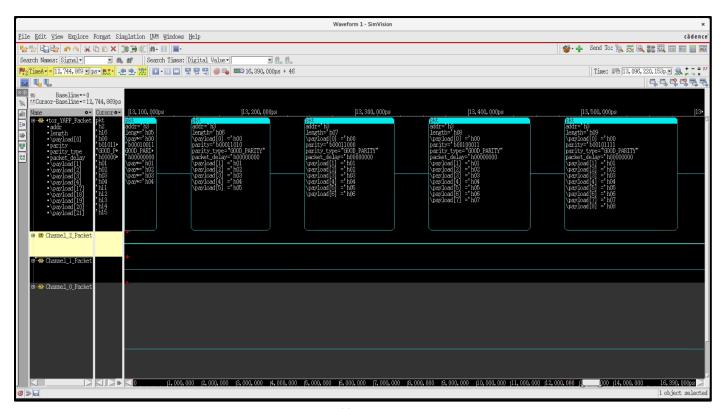


Figure 8-Addr=3

THE END

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