Digital Design Verification

Lab Manual # 40 – Integrating Multiple UVCs

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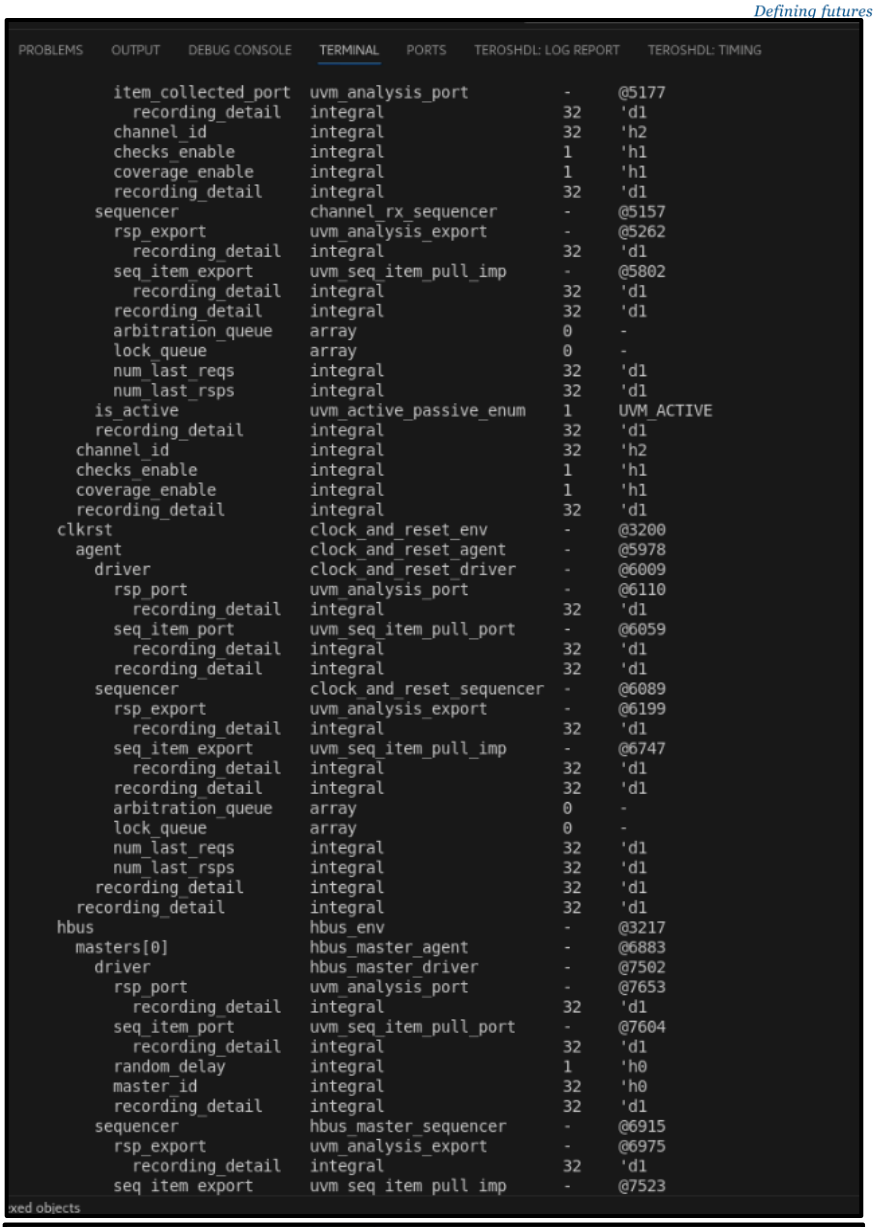
Task 1: Integrating Multiple UVC

Running Base Test

1. For every UVC (YAPP, Clock and reset, HBUS and Channel) add the following to your run.f.
   - An incdir reference to the UVC sv directory (depending upon the location of UVC in reference to your current working directory)
   - UVC package filename.
   - UVC interface filename.
2. Run a simulation with `base_test` only. Check the topology report carefully to make sure all of your UVCs are instantiated and configured correctly. Copy the topology report into a new file for future reference.

```
UVM_INFO router_test_lib.sv(13) @ 0: uvm_test_top [base_test] [BASE TEST] BUILD PHASE E
UVM_INFO router_tb.sv(21) @ 0: uvm_test_top.env [router_tb] [Router TB] BUILD PHASE EXE
UVM_INFO ../channel/sv/channel_rx_monitor.sv(68) @ 0: uvm_test_top.env.chan0.rx_agent.m
UVM_INFO ../channel/sv/channel_rx_monitor.sv(68) @ 0: uvm_test_top.env.chan1.rx_agent.m
UVM_INFO ../channel/sv/channel_rx_monitor.sv(68) @ 0: uvm_test_top.env.chan2.rx_agent.m
UVM_INFO @ 0: reporter [UVMTOP] UVM testbench topology:
--------------------------------------------------------------------------------
Name                          Type                      Size  Value
--------------------------------------------------------------------------------
uvm_test_top                  base_test                 -     @2942
  env                         router_tb                 -     @3026
    chan0                     channel_env               -     @3111
      rx_agent                channel_rx_agent          -     @3294
        driver                channel_rx_driver         -     @4002
          rsp_port            uvm_analysis_port         -     @4153
            recording_detail  integral                  32    'd1
          seq_item_port       uvm_seq_item_pull_port    -     @4104
            recording_detail  integral                  32    'd1
          channel_id          integral                  32    'h0
          recording_detail    integral                  32    'd1
        monitor               channel_rx_monitor        -     @3285
          item_collected_port uvm_analysis_port         -     @3383
            recording_detail  integral                  32    'd1
          channel_id          integral                  32    'h0
          checks_enable       integral                  1     'h1
          coverage_enable     integral                  1     'h1
          recording_detail    integral                  32    'd1
        sequencer             channel_rx_sequencer      -     @3358
          rsp_export          uvm_analysis_export       -     @3473
            recording_detail  integral                  32    'd1
          seq_item_export     uvm_seq_item_pull_imp     -     @4023
            recording_detail  integral                  32    'd1
          recording_detail    integral                  32    'd1
          arbitration_queue   array                     0     -
          lock_queue          array                     0     -
          num_last_reqs       integral                  32    'd1
          num_last_rsps       integral                  32    'd1
        is_active             uvm_active_passive_enum   1     UVM_ACTIVE
        recording_detail      integral                  32    'd1
      channel_id              integral                  32    'h0
      checks_enable           integral                  1     'h1
      coverage_enable         integral                  1     'h1
      recording_detail        integral                  32    'd1
    chan1                     channel_env               -     @3088
      rx_agent                channel_rx_agent          -     @4207
        driver                channel_rx_driver         -     @4896
          rsp_port            uvm_analysis_port         -     @5041
            recording_detail  integral                  32    'd1
          seq_item_port       uvm_seq_item_pull_port    -     @4993
            recording_detail  integral                  32    'd1
          channel_id          integral                  32    'h1
          recording_detail    integral                  32    'd1
        monitor               channel_rx_monitor        -     @4204
          item_collected_port uvm_analysis_port         -     @4291
            recording_detail  integral                  32    'd1
          channel_id          integral                  32    'h1
```



```
PROBLEMS   OUTPUT   DEBUG CONSOLE   TERMINAL   PORTS   TEROSHDL: LOG REPORT   TEROSHDL: TIMING

        item_collected_port  uvm_analysis_port          -     @5177
          recording_detail   integral                  32    'd1
        channel_id           integral                  32    'h2
        checks_enable        integral                  1     'h1
        coverage_enable      integral                  1     'h1
        recording_detail     integral                  32    'd1
      sequencer              channel_rx_sequencer      -     @5157
        rsp_export           uvm_analysis_export       -     @5262
          recording_detail   integral                  32    'd1
        seq_item_export      uvm_seq_item_pull_imp     -     @5802
          recording_detail   integral                  32    'd1
        recording_detail     integral                  32    'd1
        arbitration_queue    array                     0     -
        lock_queue           array                     0     -
        num_last_reqs        integral                  32    'd1
        num_last_rsps        integral                  32    'd1
      is_active              uvm_active_passive_enum   1     UVM_ACTIVE
      recording_detail       integral                  32    'd1
    channel_id               integral                  32    'h2
    checks_enable            integral                  1     'h1
    coverage_enable          integral                  1     'h1
    recording_detail         integral                  32    'd1
  clkrst                     clock_and_reset_env       -     @3200
    agent                    clock_and_reset_agent     -     @5978
      driver                 clock_and_reset_driver    -     @6009
        rsp_port             uvm_analysis_port         -     @6110
          recording_detail   integral                  32    'd1
        seq_item_port        uvm_seq_item_pull_port    -     @6059
          recording_detail   integral                  32    'd1
        recording_detail     integral                  32    'd1
      sequencer              clock_and_reset_sequencer -     @6089
        rsp_export           uvm_analysis_export       -     @6199
          recording_detail   integral                  32    'd1
        seq_item_export      uvm_seq_item_pull_imp     -     @6747
          recording_detail   integral                  32    'd1
        recording_detail     integral                  32    'd1
        arbitration_queue    array                     0     -
        lock_queue           array                     0     -
        num_last_reqs        integral                  32    'd1
        num_last_rsps        integral                  32    'd1
      recording_detail       integral                  32    'd1
    recording_detail         integral                  32    'd1
  hbus                       hbus_env                  -     @3217
    masters[0]               hbus_master_agent         -     @6883
      driver                 hbus_master_driver        -     @7502
        rsp_port             uvm_analysis_port         -     @7653
          recording_detail   integral                  32    'd1
        seq_item_port        uvm_seq_item_pull_port    -     @7604
          recording_detail   integral                  32    'd1
        random_delay         integral                  1     'h0
        master_id            integral                  32    'h0
        recording_detail     integral                  32    'd1
      sequencer              hbus_master_sequencer     -     @6915
        rsp_export           uvm_analysis_export       -     @6975
          recording_detail   integral                  32    'd1
        seq_item_export      uvm_seq_item_pull_imp     -     @7523
xed objects
```

```
          recording_detail   integral                  32    'd1
        seq_item_port        uvm_seq_item_pull_port    -     @7604
          recording_detail   integral                  32    'd1
        random_delay         integral                  1     'h0
        master_id            integral                  32    'h0
        recording_detail     integral                  32    'd1
      sequencer              hbus_master_sequencer     -     @6915
        rsp_export           uvm_analysis_export       -     @6975
          recording_detail   integral                  32    'd1
        seq_item_export      uvm_seq_item_pull_imp     -     @7523
          recording_detail   integral                  32    'd1
        recording_detail     integral                  32    'd1
        arbitration_queue    array                     0     -
        lock_queue           array                     0     -
        num_last_reqs        integral                  32    'd1
        num_last_rsps        integral                  32    'd1
      monitor                hbus_monitor              -     @6799
      is_active              uvm_active_passive_enum   1     UVM_ACTIVE
      master_id              integral                  32    'h0
      recording_detail       integral                  32    'd1
    monitor                  hbus_monitor              -     @6799
      item_collected_port    uvm_analysis_port         -     @6849
        recording_detail     integral                  32    'd1
      checks_enable          integral                  1     'h1
      coverage_enable        integral                  1     'h1
      recording_detail       integral                  32    'd1
    num_masters              integral                  32    'h1
    num_slaves               integral                  32    'h0
    checks_enable            integral                  1     'h1
    coverage_enable          integral                  1     'h1
    recording_detail         integral                  32    'd1
```

```
uvc                          yapp_env                    -     @3002
  agent                      yapp_agent                  -     @7705
    driver                   yapp_driver                 -     @7735
      rsp_port               uvm_analysis_port           -     @7868
        recording_detail     integral                    32    'd1
      seq_item_port          uvm_seq_item_pull_port      -     @7817
        recording_detail     integral                    32    'd1
      recording_detail       integral                    32    'd1
    monitor                  yapp_monitor                -     @7740
      recording_detail       integral                    32    'd1
    sequencer                yapp_sequencer              -     @7847
      rsp_export             uvm_analysis_export         -     @7957
        recording_detail     integral                    32    'd1
      seq_item_export        uvm_seq_item_pull_imp       -     @8505
        recording_detail     integral                    32    'd1
      recording_detail       integral                    32    'd1
      arbitration_queue      array                       0     -
      lock_queue             array                       0     -
      num_last_reqs          integral                    32    'd1
      num_last_rsps          integral                    32    'd1
    is_active                uvm_active_passive_enum     1     UVM_ACTIVE
    recording_detail         integral                    32    'd1
  recording_detail           integral                    32    'd1
recording_detail             integral                    32    'd1
--------------------------------------------------------------------------
```

Running Simple Test

3. Run a simulation in GUI mode using simple_test and verify as follows:
   a. Add YAPP UVC monitor transactions to the waveform viewer.
   b. Add all three Channel UVC monitor transactions to the waveform viewer.
   c. Use the transactions to confirm packets are passed correctly through the router and collected at the right channel.

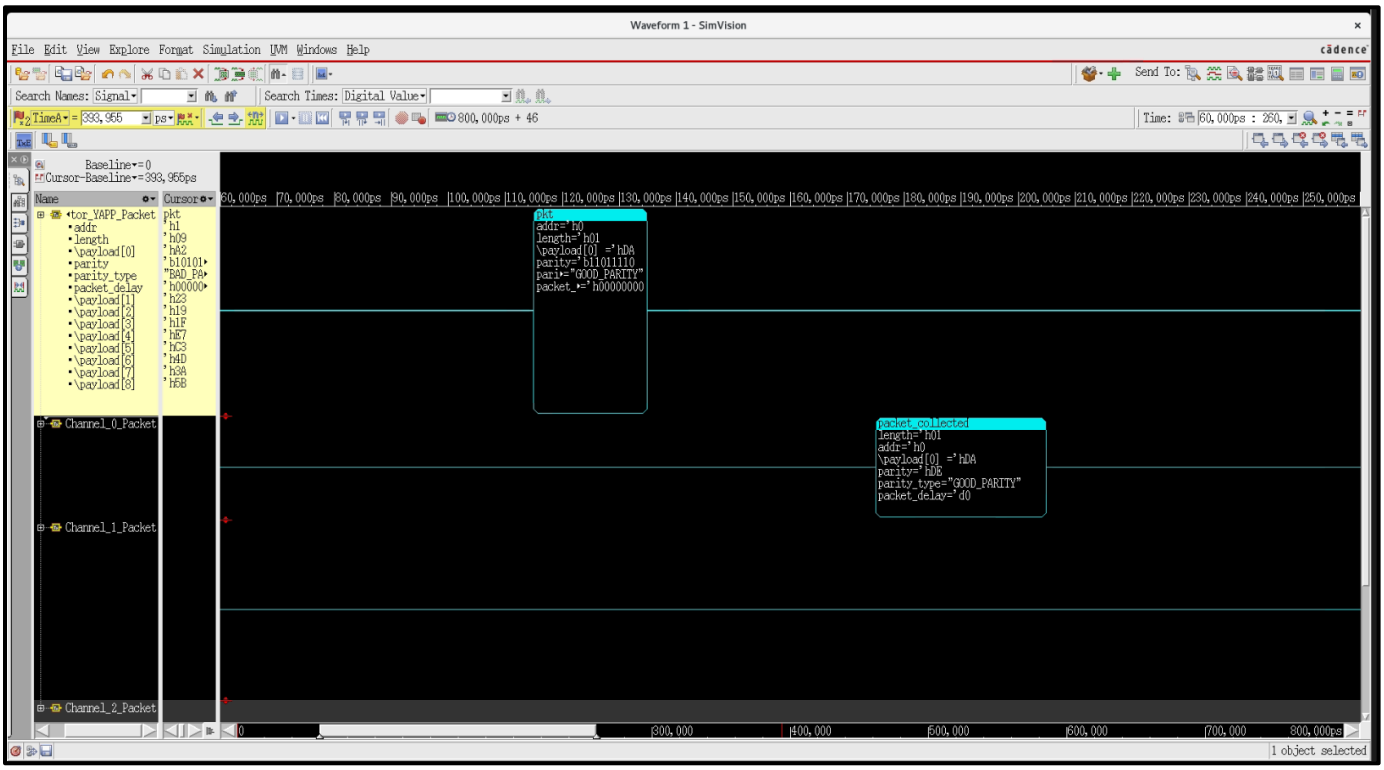


Figure 1-Channel 0

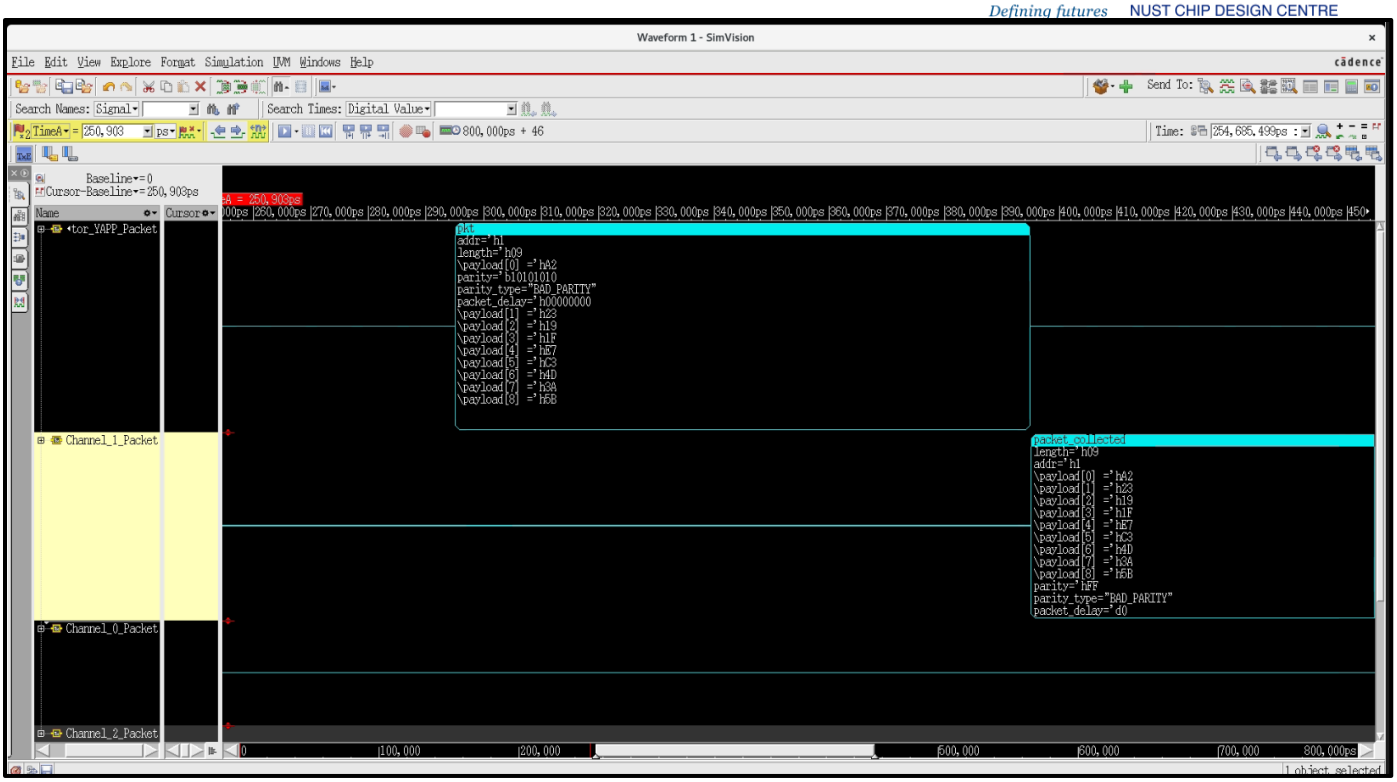


Figure 2-Channel 1

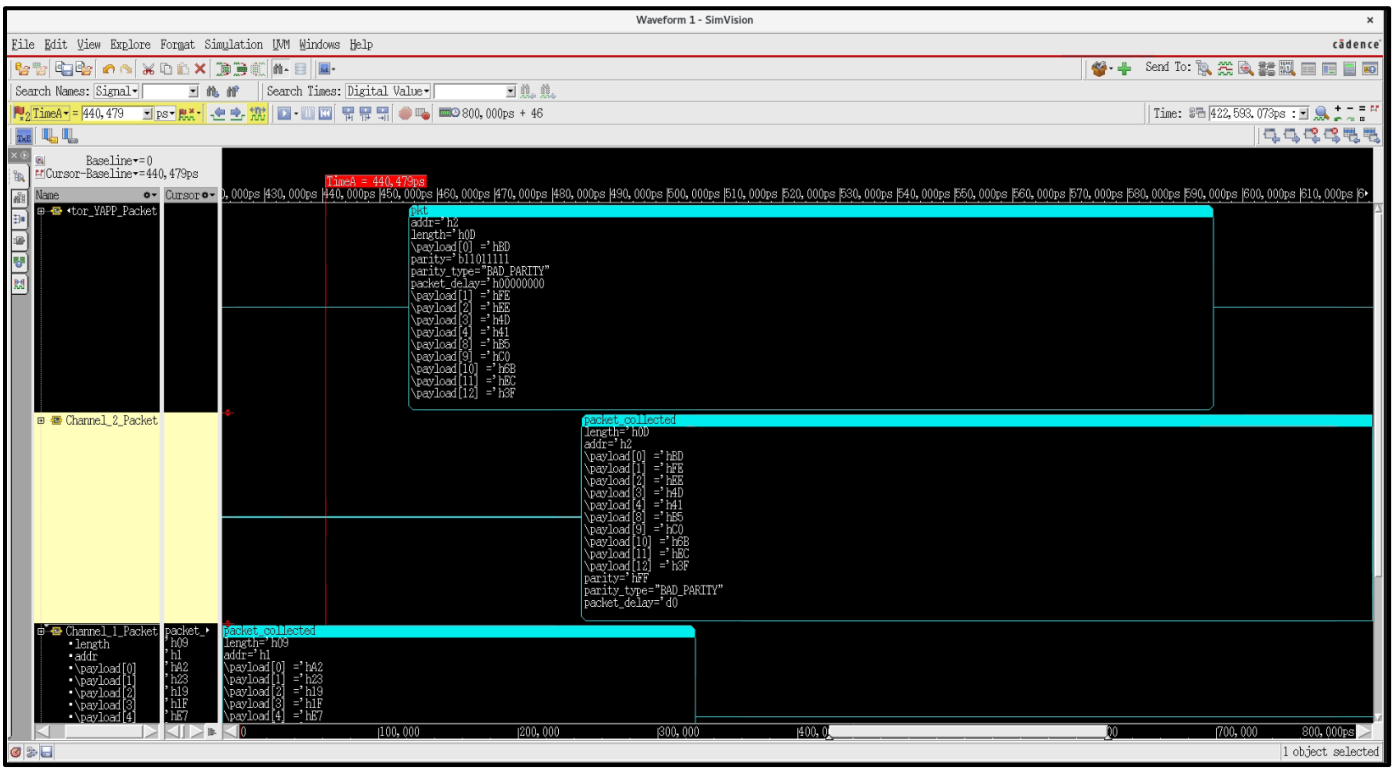


Figure 3-Channel 3

Further Integration Testing

4. Write a new YAPP sequence in the yapp/sv/yapp_tx_seqs.sv file to generate packets for all four channels (including the illegal address 3). The packets should have incrementing payload sizes from 1 to 22 and parity distribution of 20% bad parity (88 packets in total).

   Hint: You could create packets using nested loops for address and payload.

5. Create a new test, test_uvc_integration, in the router_test_lib.sv file to perform the following:
   a. Set the run_phase default sequence of the YAPP UVC to the sequence created above.
   b. Set the run_phase default sequence of the HBUS UVC to set up the router with register field maxpktsize = 20 and enable the router (register field router_en = 1).

   Hint: There is a sequence defined for this in the HBUS master sequences hbus_master_seqs.sv.
   Hint: The hierarchical path name for the HBUS configuration setting can be read from the topology report.

6. Run a simulation and check the results to see that the three channels are properly addressed, that there is an error signal when parity is wrong, and that packets are dropped if bigger than maxpktsize or have illegal addresses.

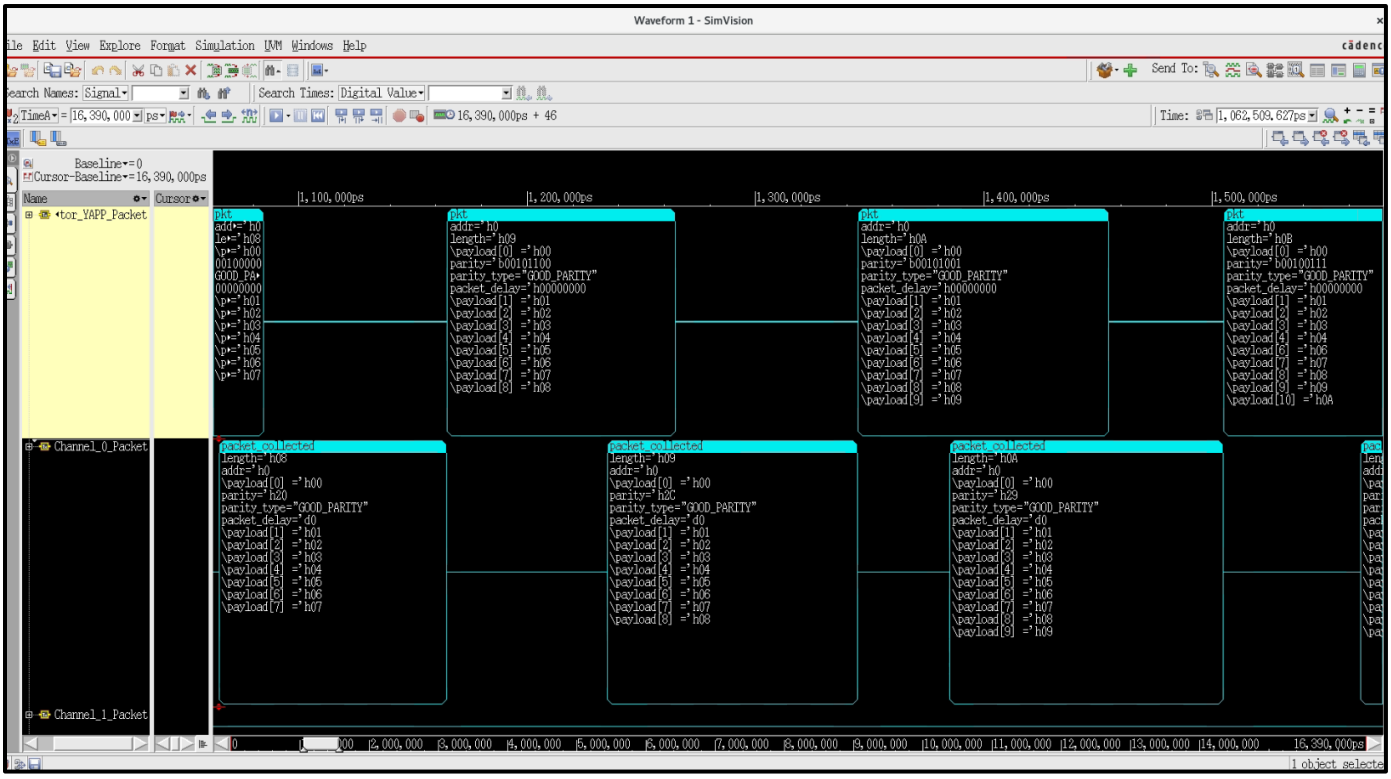


Figure 4-Channel 0

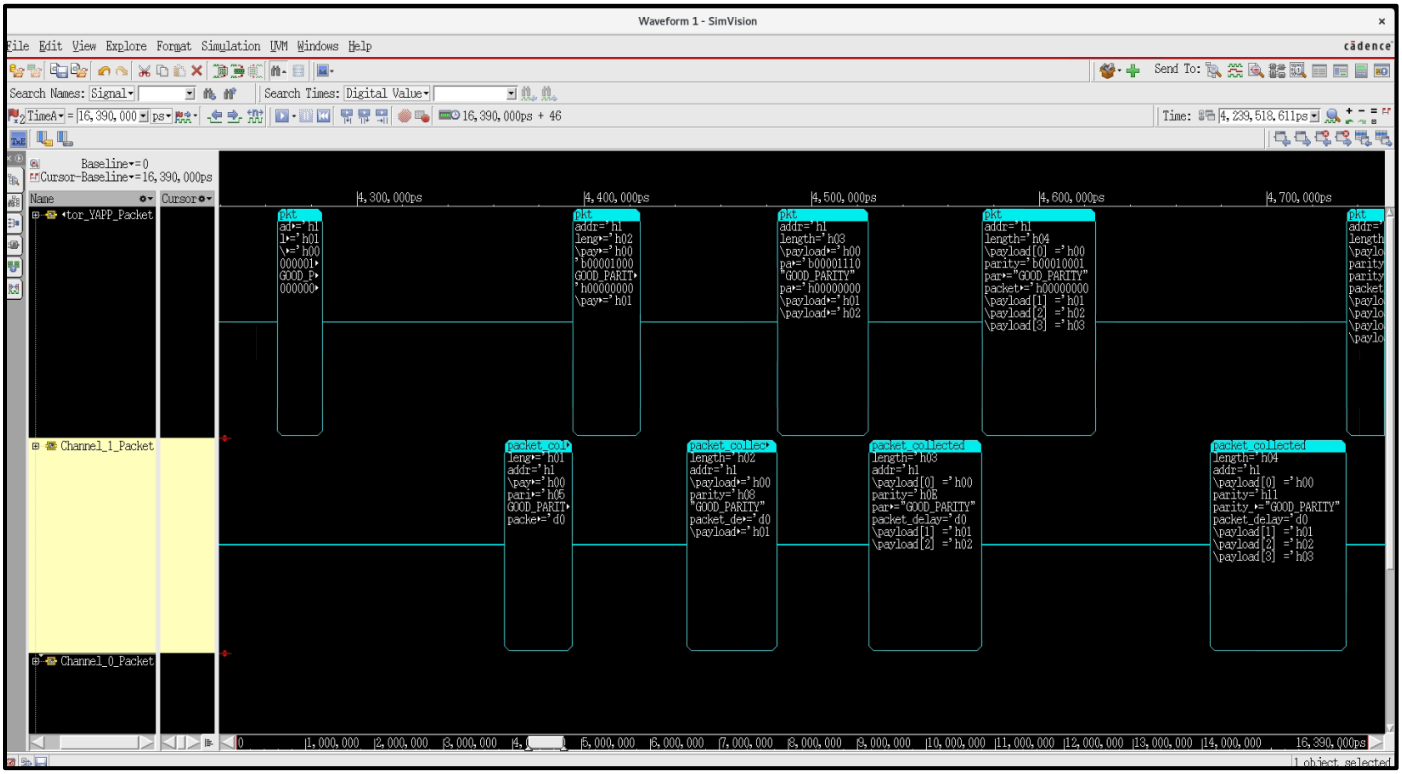


Figure 5-Channel 1

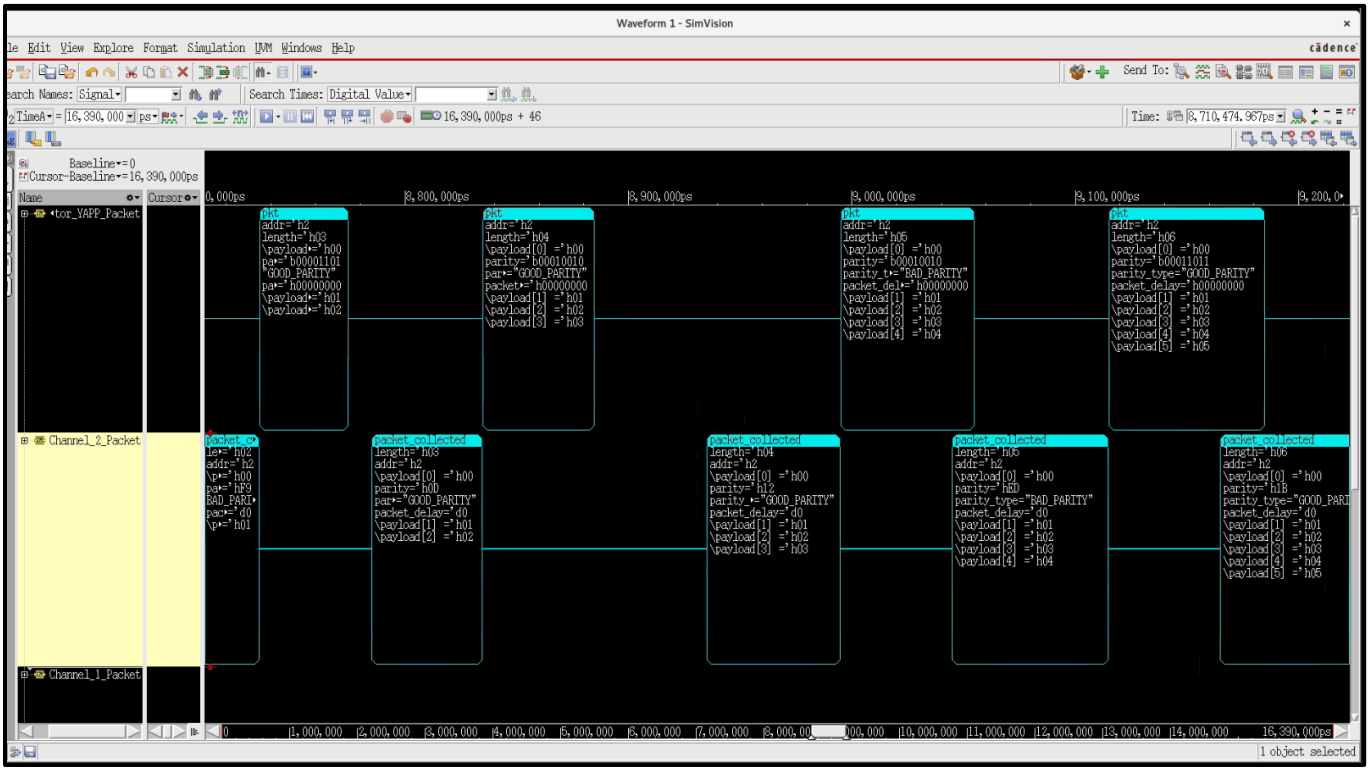


Figure 6-Channel 2

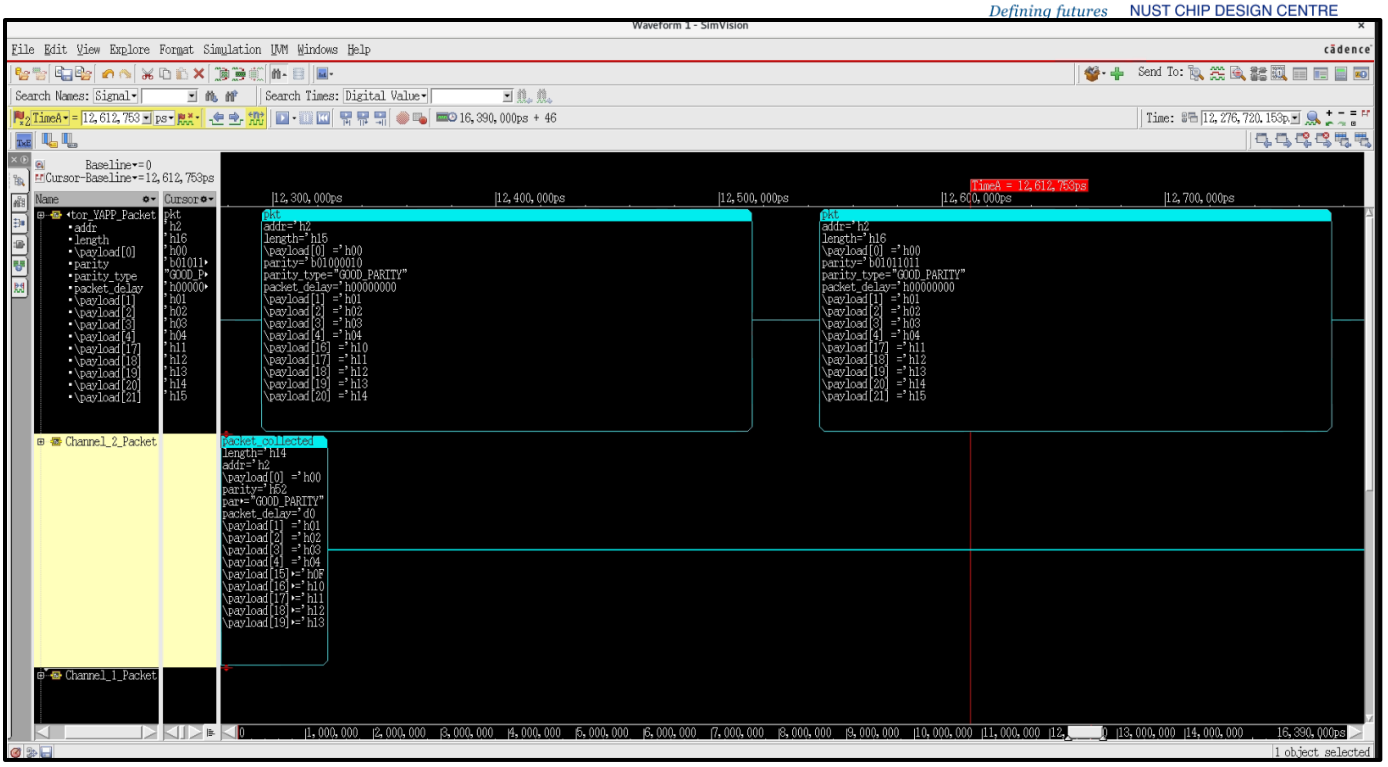


Figure 7-Packet size greater than 20

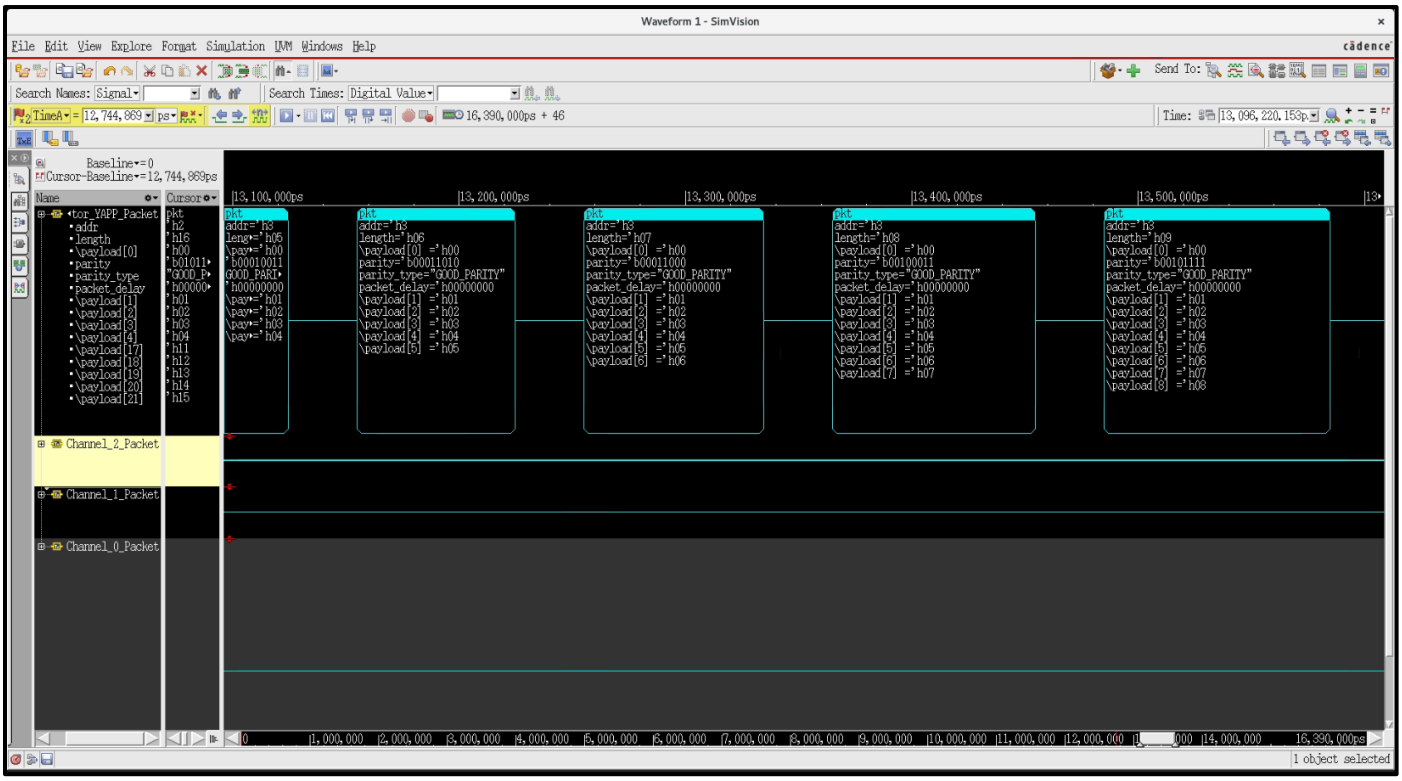


Figure 8-Addr=3

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