



Digital Design Verification

Lab Manual # 39 – Generating UVM Sequences & Connection to the DUT

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Task 1: Generating UVM Sequences

Running a Test Using a New Sequence

Create a new test in the file `router_test_lib.sv` from the `tb` directory:

Call the test `incr_payload_test` and extend from `base_test`.

Add a `uvm_config_wrapper::setto` to set the `run_phased` default sequence to `yapp_incr_payload_seq`.

Add a `set_type_override()` method to use the `short_yapp_packet` data type defined in Lab 4.

Run the test and verify the results. Setting verbosity to `UVM_FULL` will allow you to see which default sequence is executed in the `run_phase()`.

The screenshot shows a Verilog simulation in Visual Studio Code. The terminal window displays the following UVM test results:

```
UVM INFO ../sv/yapp_tx_driver.sv(23) @ 0: uvm_test_top.env.uvc.agent.driver [yapp_driver] Running Simulation Driver!
UVM INFO ../sv/yapp_tx_monitor.sv(14) @ 0: uvm_test_top.env.uvc.agent.monitor [yapp_monitor] Running Simulation Monitor!
UVM INFO ../sv/yapp_tx_sequencer.sv(10) @ 0: uvm_test_top.env.uvc.agent.sequencer [yapp_sequencer] Running Simulation Sequencer!
UVM INFO ../sv/yapp_tx_agent.sv(11) @ 0: uvm_test_top.env.uvc.agent [yapp_agent] Running Simulation Agent!
UVM INFO ../sv/yapp_env.sv(17) @ 0: uvm_test_top.env.uvc [yapp_env] Running Simulation Environment!
UVM INFO router_tb.sv(21) @ 0: uvm_test_top.env [router_tb] Running Simulation Router Tb!
UVM INFO router_test_lib.sv(27) @ 0: uvm_test_top [incr_payload_test] Running Simulation Base Test!
UVM INFO /home/cc/mnt/XC7000P389/tools/methodology/UVM/CMS-1.1d/sv/src/seq/uvm_sequencer_base.svh(1391) @ 0: uvm_test_top.env.uvc.agent.sequencer [PHASESEQ] Starting default sequence 'yapp_incr_payload_seq' for phase 'run'
SDI/Verilog Transaction Recording Facility Version 23.09-s006
SDI2 Transaction Recording API Version 23.09-s006
UVM INFO ../sv/yapp_tx_monitor.sv(9) @ 0: uvm_test_top.env.uvc.agent.monitor [yapp_monitor] Executing Monitor Run Phase!
UVM INFO ../sv/yapp_tx_seqs.sv(21) @ 0: uvm_test_top.env.uvc.agent.sequencer@yapp_incr_payload_seq [yapp_incr_payload_seq] raise objection
UVM INFO ../sv/yapp_tx_seqs.sv(143) @ 0: uvm_test_top.env.uvc.agent.sequencer@yapp_incr_payload_seq [yapp_incr_payload_seq] Executing yapp_incr_payload_seq sequence
UVM INFO /home/cc/mnt/XC7000P389/tools/methodology/UVM/CMS-1.1d/sv/src/seq/uvm_sequencer_base.svh(1385) @ 0: uvm_test_top.env.uvc.agent.sequencer [PHASESEQ] No default phase sequence for phase 'pre_reset'
UVM INFO ../sv/yapp_tx_driver.sv(17) @ 0: uvm_test_top.env.uvc.agent.driver [yapp_driver] Packet is
-----
Name      Type      Size Value
-----
req       short packet  -  @3787
addr      integral      2  'h1
length    integral      6  'he
payload   da(integral) 14  -
[0]       integral      8  'hb
[1]       integral      8  'h1
[2]       integral      8  'h2
[3]       integral      8  'h3
[4]       integral      8  'h4
...
[9]       integral      8  'h9
[10]      integral      8  'ha
[11]      integral      8  'hb
[12]      integral      8  'hc
[13]      integral      8  'hd
parity    integral      8  b111000
parity_type_e  parity_type_e 1  GOOD PARITY
packet_delay  integral      32  'h14
begin_time  time          64  0
depth      int           32  d2
parent sequence (name) string          21  yapp_incr_payload_seq
parent sequence (full name) string          58  uvm_test_top.env.uvc.agent.sequencer.yapp_incr_payload_seq
sequencer  string         36  uvm_test_top.env.uvc.agent.sequencer
-----
UVM INFO /home/cc/mnt/XC7000P389/tools/methodology/UVM/CMS-1.1d/sv/src/seq/uvm_sequencer_base.svh(1385) @ 0: uvm_test_top.env.uvc.agent.sequencer [PHASESEQ] No default phase sequence for phase 'reset'
UVM INFO /home/cc/mnt/XC7000P389/tools/methodology/UVM/CMS-1.1d/sv/src/seq/uvm_sequencer_base.svh(1385) @ 0: uvm_test_top.env.uvc.agent.sequencer [PHASESEQ] No default phase sequence for phase 'post_reset'
UVM INFO /home/cc/mnt/XC7000P389/tools/methodology/UVM/CMS-1.1d/sv/src/seq/uvm_sequencer_base.svh(1385) @ 0: uvm_test_top.env.uvc.agent.sequencer [PHASESEQ] No default phase sequence for phase 'pre_configure'
UVM INFO /home/cc/mnt/XC7000P389/tools/methodology/UVM/CMS-1.1d/sv/src/seq/uvm_sequencer_base.svh(1385) @ 0: uvm_test_top.env.uvc.agent.sequencer [PHASESEQ] No default phase sequence for phase 'configure'
UVM INFO /home/cc/mnt/XC7000P389/tools/methodology/UVM/CMS-1.1d/sv/src/seq/uvm_sequencer_base.svh(1385) @ 0: uvm_test_top.env.uvc.agent.sequencer [PHASESEQ] No default phase sequence for phase 'pre_main'
UVM INFO /home/cc/mnt/XC7000P389/tools/methodology/UVM/CMS-1.1d/sv/src/seq/uvm_sequencer_base.svh(1385) @ 0: uvm_test_top.env.uvc.agent.sequencer [PHASESEQ] No default phase sequence for phase 'main'
UVM INFO /home/cc/mnt/XC7000P389/tools/methodology/UVM/CMS-1.1d/sv/src/seq/uvm_sequencer_base.svh(1385) @ 0: uvm_test_top.env.uvc.agent.sequencer [PHASESEQ] No default phase sequence for phase 'post_main'
```

Name	Type	Size	Value
req	short packet	-	@3787
addr	integral	2	'h1
length	integral	6	'he
payload	da(integral)	14	-
[0]	integral	8	'hb
[1]	integral	8	'h1
[2]	integral	8	'h2
[3]	integral	8	'h3
[4]	integral	8	'h4
...
[9]	integral	8	'h9
[10]	integral	8	'ha
[11]	integral	8	'hb
[12]	integral	8	'hc
[13]	integral	8	'hd
parity	integral	8	b111000
parity_type_e	parity_type_e	1	GOOD PARITY
packet_delay	integral	32	'h14
begin_time	time	64	0
depth	int	32	d2
parent sequence (name)	string	21	yapp_incr_payload_seq
parent sequence (full name)	string	58	uvm_test_top.env.uvc.agent.sequencer.yapp_incr_payload_seq
sequencer	string	36	uvm_test_top.env.uvc.agent.sequencer

Testing Your Sequences

Create a new test in the file `tb/router_test_lib.sv`:

Call the test `exhaustive_seq_test` and extend from `base_test`.

Add a `uvm_config_wrapper::setto` to set the `run_phased` default sequence to `yapp_exhaustive_seq`.

Add a `set_type_override()` method to use the `short_yapp_packet` data type

```

Name      Type      Size  Value
-----
req        short packet  -  @3999
addr        integral    2    'h1
length      integral    6    'he
payload     da(integral) 14
            {0}      integral    8    'h5f
            {1}      integral    8    'h74
            {2}      integral    8    'h2b
            {3}      integral    8    'h23
            {4}      integral    8    'h37
...
[9]         integral    8    'h82
[10]        integral    8    'h9a
[11]        integral    8    'h8c
[12]        integral    8    'h9c
[13]        integral    8    'h6d
parity      integral    8    'b10000110
parity_type parity_type_e 1    GOOD PARITY
packet_delay integral    32    'h7
begin_time  time        64    20
depth       int         32    'd3
parent sequence (name) string      4    seq2
parent sequence (full name) string      61    uvm_test_top.env.uvc.agent.sequencer.yapp_exhaustive_seq.seq2
sequencer   string      36    uvm_test_top.env.uvc.agent.sequencer

xmsin: "W,RNDCS: These constraints and variables contribute to the set of conflicting constraints (view the extended help for this message using 'xmhlp xmsin RNDCS' for guidelines on how debug the issue):
In ../sv/yapp_packet.sv
Line 78: ( addr != 2'h2 )

Variable Type      Status      Current Value      Source
-----
addr      (bit [1:0])  RANDOM    <unassigned>      ../sv/yapp_packet.sv ; line 11

'uvm_do_with(req, {addr == 2;})

xmsin: "W,RNDCS: The randomize method call failed. The unique id of the failed randomize call is 6.
Observed simulation time : 30 NS + 1.
UVM WARNING ../sv/yapp_tx_seqs.sv(97) @ 30: uvm_test_top.env.uvc.agent.sequencer@yapp_exhaustive_seq.seq2 [RNDFLD] Randomization failed in uvm_do_with action
UVM INFO ../sv/yapp_tx_driver.sv(17) @ 30: uvm_test_top.env.uvc.agent.driver [yapp_driver] Packet 15
Name      Type      Size  Value
-----
req        short packet  -  @3999
addr        integral    2    'h8
length      integral    6    'h8
payload     da(integral) 0
parity      integral    8    'b6

```

```

UVM INFO ../sv/yapp_tx_seqs.sv(35) @ 100: uvm_test_top.env.uvc.agent.sequencer@yapp_exhaustive_seq [yapp_exhaustive_seq] drop objection
UVM INFO /home/cc/mnt/XCELIUM2309/tools/methodology/UVM/CDS-1.1d/sv/src/base/uvm_objection.svh(1245) @ 100: reporter [TEST_DONE] All end-of-test objections have been dropped. Calling stop tasks
UVM INFO /home/cc/mnt/XCELIUM2309/tools/methodology/UVM/CDS-1.1d/sv/src/base/uvm_objection.svh(1268) @ 100: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase

--- UVM Report catcher Summary ---

Number of demoted UVM FATAL reports : 0
Number of demoted UVM ERROR reports : 0
Number of demoted UVM WARNING reports : 0
Number of caught UVM FATAL reports : 0
Number of caught UVM ERROR reports : 0
Number of caught UVM WARNING reports : 0

--- UVM Report Summary ---

** Report counts by severity
UVM INFO : 47
UVM WARNING : 1
UVM ERROR : 0
UVM FATAL : 0

** Report counts by id
[PHASESEQ] 13
[RNDFLD] 1
[RNTST] 1
[TEST_DONE] 2
[UVMTOP] 1
[exhaustive seq test] 2
[router tb] 2
[yapp_012_seq] 1
[yapp_111_seq] 1
[yapp_2_seq] 4
[yapp_agent] 1
[yapp_driver] 11
[yapp_env] 1
[yapp_exhaustive_seq] 2
[yapp_incr_payload_seq] 1
[yapp_monitor] 2
[yapp_repeat_addr_seq] 1
[yapp_sequencer] 1
Simulation complete via $finish(1) at time 100 NS + 33
/home/cc/mnt/XCELIUM2309/tools/methodology/UVM/CDS-1.1d/sv/src/base/uvm_root.svh:457 $finish;
xcelium> exit
TOOL: Xrun(64)
[coldcdc-0053 tb]s
23.09-s006: Exiting on Jun 26, 2025 at 15:30:28 PKT (total: 00:00:16)

```

Testing Your Sequences and Fixing Randomization Errors

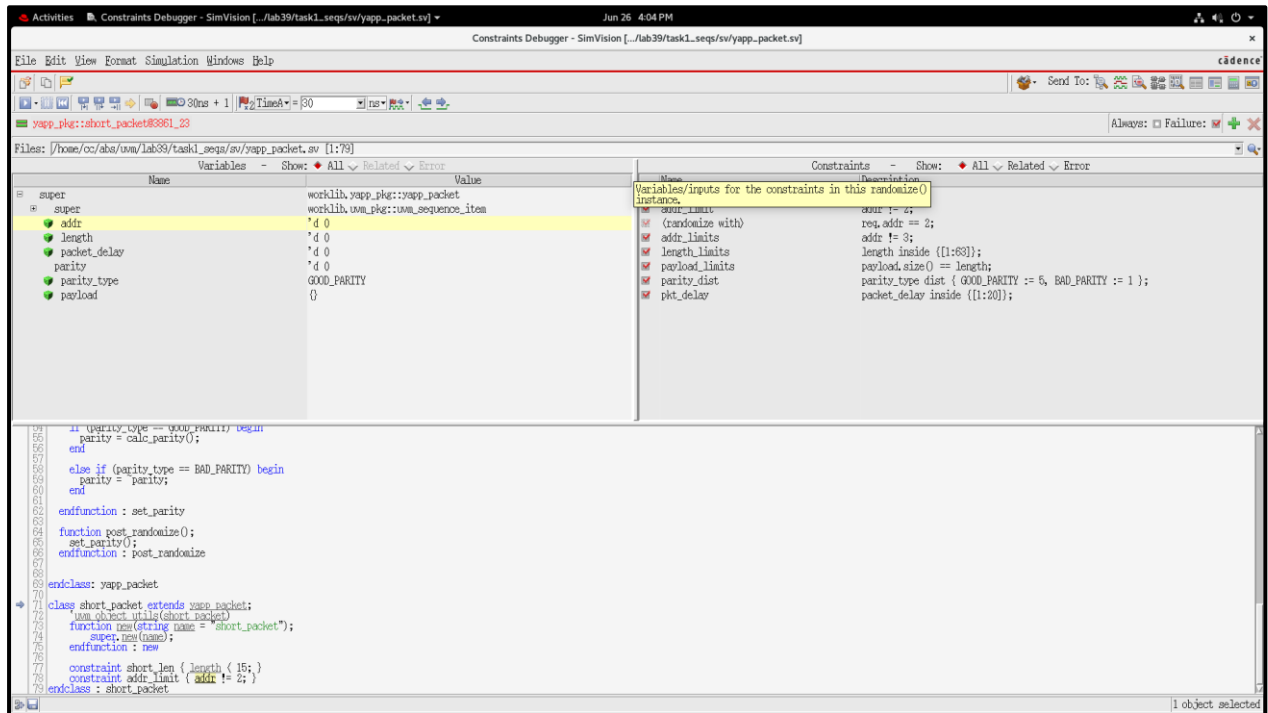
- Use the randomization and transaction debug features to answer the following questions:
- Why do you get randomization violations?
Answer: Due to conflicting constraints in short_packet_class and yapp_012_seq and yapp_repeat_addr_seq, we get errors.
- What happens to the packet when a constraint violation is found?

Answer: No randomize occurs.

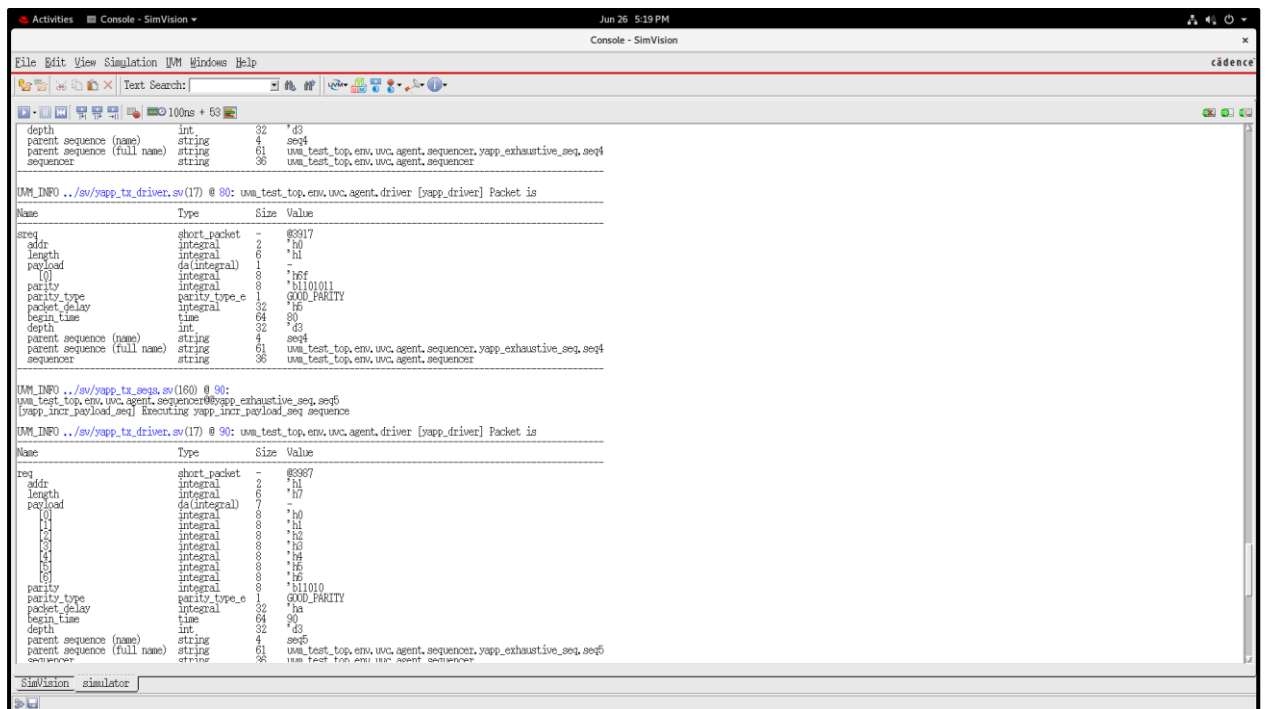
How could you fix these violations?

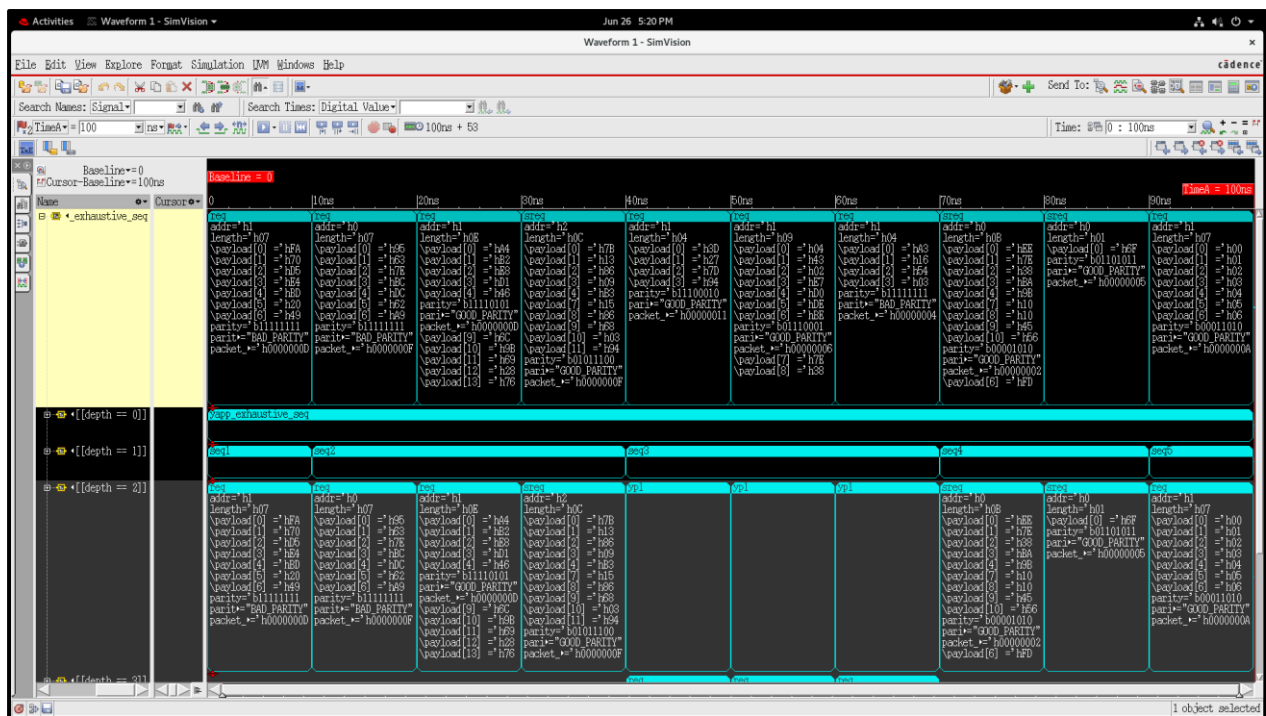
Answer: By turning off the constraint mode of `addr!=2` in `short_packet_class` using `constraint_mode(0)`.

Before Fixing Randomization Errors:

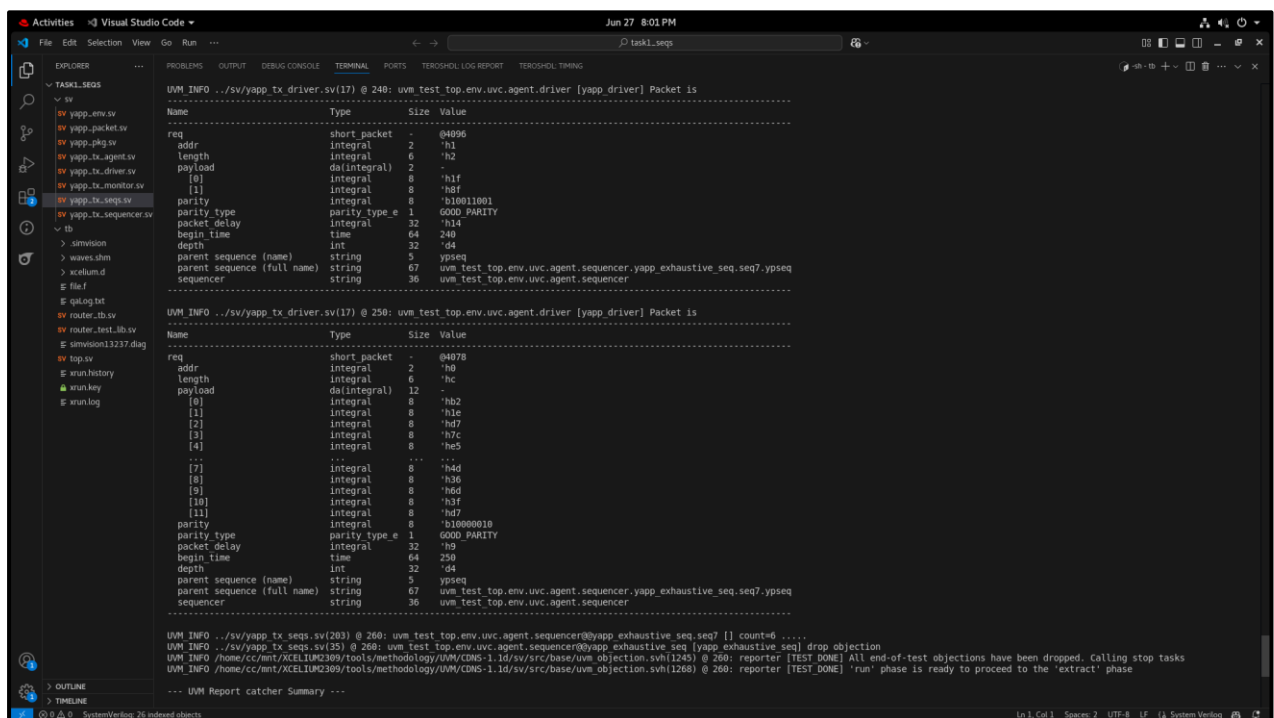


After Fixing Randomization Errors:





Add `yapp_rnd_seq` and `six_yapp_seq` to the `yapp_exhaustive_seq` and verify their behavior in simulation.

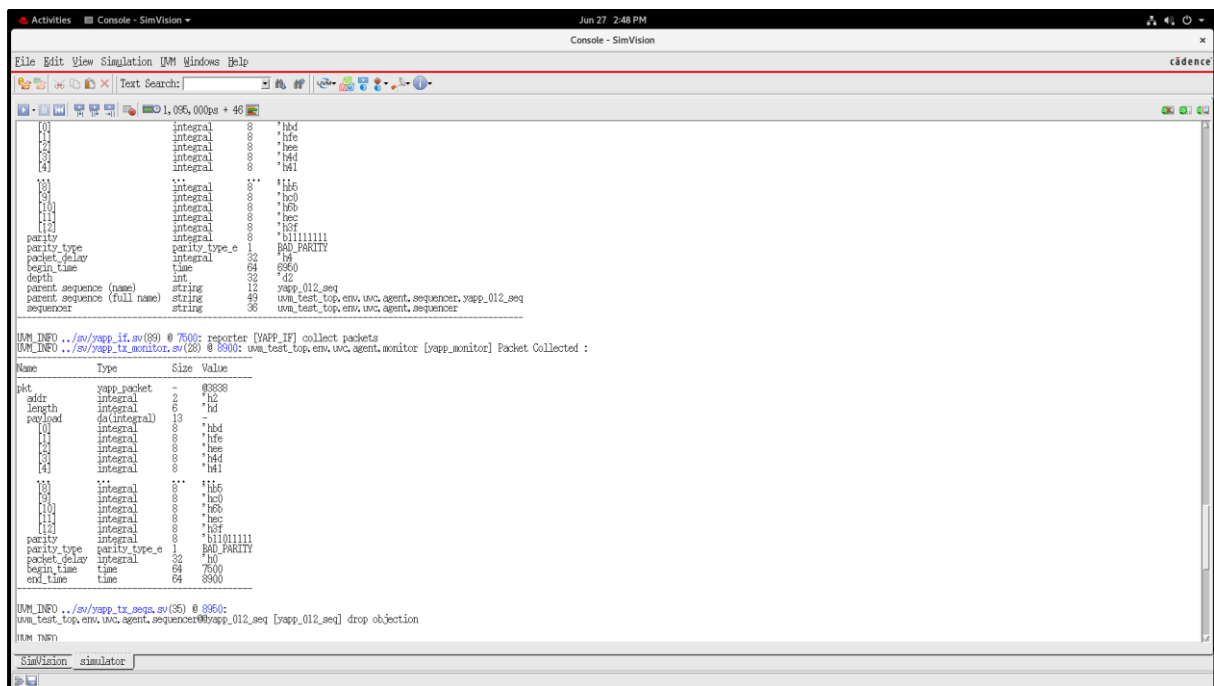


```
UVM INFO ../sv/yapp_tx_seqs.sv(184) @ 180: uvm_test_top.env.uvc.agent.sequencer@yapp_exhaustive_seq.seq6 [yapp_rnd_seq] Executing yapp_rnd_seq sequence.
UVM INFO ../sv/yapp_tx_seqs.sv(185) @ 180: uvm_test_top.env.uvc.agent.sequencer@yapp_exhaustive_seq.seq6 [] count=10 .....
UVM INFO ../sv/yapp_tx_driver.sv(17) @ 186: uvm_test_top.env.uvc.agent.driver [yapp_driver] Packet is
-----
Name      Type      Size  Value
-----
req        short_packet -    @3851
addr       integral  2      'h1
length     integral  6      'h1
payload    ds(integral) 1
           [0]      integral 8      'heb
           parity   integral 8      'b1101110
           parity_type_e 1      GOOD_PARITY
packet_delay integral 32      'h2
begin_time time      64      100
depth      int       32      'd3
parent sequence (name) string    4      seq6
parent sequence (full name) string    61      uvm_test_top.env.uvc.agent.sequencer.yapp_exhaustive_seq.seq6
sequencer  string    36      uvm_test_top.env.uvc.agent.sequencer
-----
UVM INFO ../sv/yapp_tx_driver.sv(17) @ 118: uvm_test_top.env.uvc.agent.driver [yapp_driver] Packet is
-----
Name      Type      Size  Value
-----
req        short_packet -    @3982
addr       integral  2      'h0
length     integral  6      'h8
payload    ds(integral) 8
           [0]      integral 8      'h88
           [1]      integral 8      'hde
           [2]      integral 8      'hcc
           [3]      integral 8      'hfg
           [4]      integral 8      'hda
           [5]      integral 8      'hfg
           [6]      integral 8      'h7e
           [7]      integral 8      'h73
           parity   integral 8      'b1100100
           parity_type_e 1      GOOD_PARITY
packet_delay integral 32      'h11
begin_time time      64      110
depth      int       32      'd3
parent sequence (name) string    4      seq6
parent sequence (full name) string    61      uvm_test_top.env.uvc.agent.sequencer.yapp_exhaustive_seq.seq6
sequencer  string    36      uvm_test_top.env.uvc.agent.sequencer
-----
UVM INFO ../sv/yapp_tx_driver.sv(17) @ 120: uvm_test_top.env.uvc.agent.driver [yapp_driver] Packet is
-----
Name      Type      Size  Value
-----
req        short_packet -    @3835
addr       integral  2      'h1
length     integral  6      'he
```

Lab Task 2: Connecting to the DUT Using Virtual Interfaces

Testing the DUT

Initial Simulation Without the DUT




```
Jun 27 8:06 PM
Console - SimVision
cadence

File Edit View Simulation UVM Windows Help
Text Search:

[2] integral 8 hce
[3] integral 8 h4d
[4] integral 8 h41
...
[10] integral 8 h16
[9] integral 8 hcd
[11] integral 8 hcd
[11] integral 8 hcd
[12] integral 8 h3f
parity integral 8 h10111111
parity_type parity_type_e 1 BAD_PARITY
packet_delay integral 32 h0
begin_time time 64 7500
end_time time 64 8900

*** ROUTER (DUT) Parity Error Identified: Expected:fff Computed:fff ***
UVM_INFO ../sw/mw_tx_segs.sv(35) @ 8950:
uvm_test_top.env.uvc.agent.sequencer@0app_012_seq [vapp_012_seq] drop objection
UVM_INFO
/home/cc/ant/XCELTIUM239/tools/methodology/UVM/CINS-1.14/sw/src/base/uvm_objection.svh(1245)
@ 10960: reporter [TEST_DONE] All end-of-test objections have been dropped. Calling
stop task
UVM_INFO
/home/cc/ant/XCELTIUM239/tools/methodology/UVM/CINS-1.14/sw/src/base/uvm_objection.svh(1268)
@ 10960: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
UVM_INFO ../sw/vapp_tx_driver.sv(48) @ 10960: uvm_test_top.env.uvc.agent.driver
[vapp_driver] Report: VAPP TX driver sent 3 packets
UVM_INFO ../sw/vapp_tx_monitor.sv(44) @ 10960: uvm_test_top.env.uvc.agent.monitor
[vapp_monitor] Report: VAPP Monitor Collected 3 Packets

--- UVM Report catcher Summary ---

Number of denoted UVM_FATAL reports : 0
Number of denoted UVM_ERROR reports : 0
Number of denoted UVM_WARNING reports : 0
Number of caught UVM_FATAL reports : 0
Number of caught UVM_ERROR reports : 0
Number of caught UVM_WARNING reports : 0

--- UVM Report Summary ---

** Report counts by severity
UVM_INFO : 43
UVM_WARNING : 0
UVM_ERROR : 0

SimVision simulator
```

THE END