Digital Design Verification

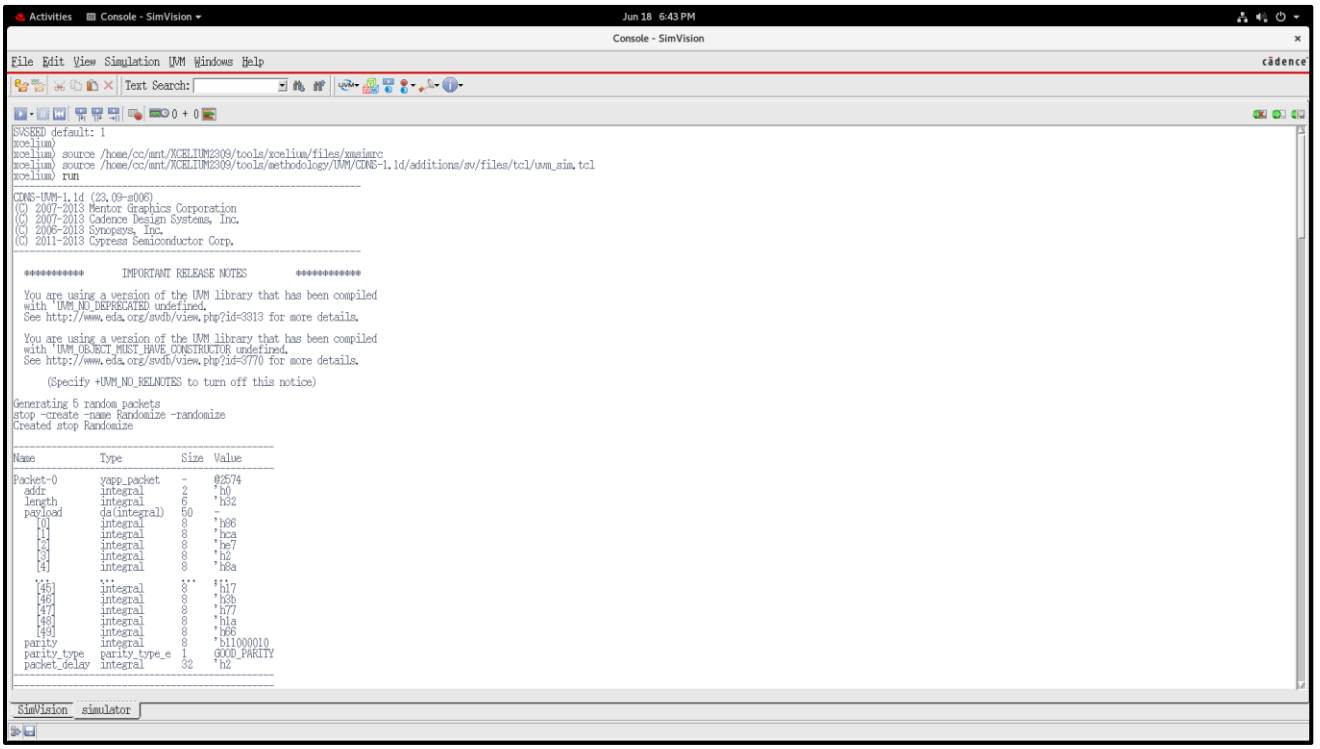
Lab Manual # 37 – Creating a Stimulus Model, Test and Testbench Components

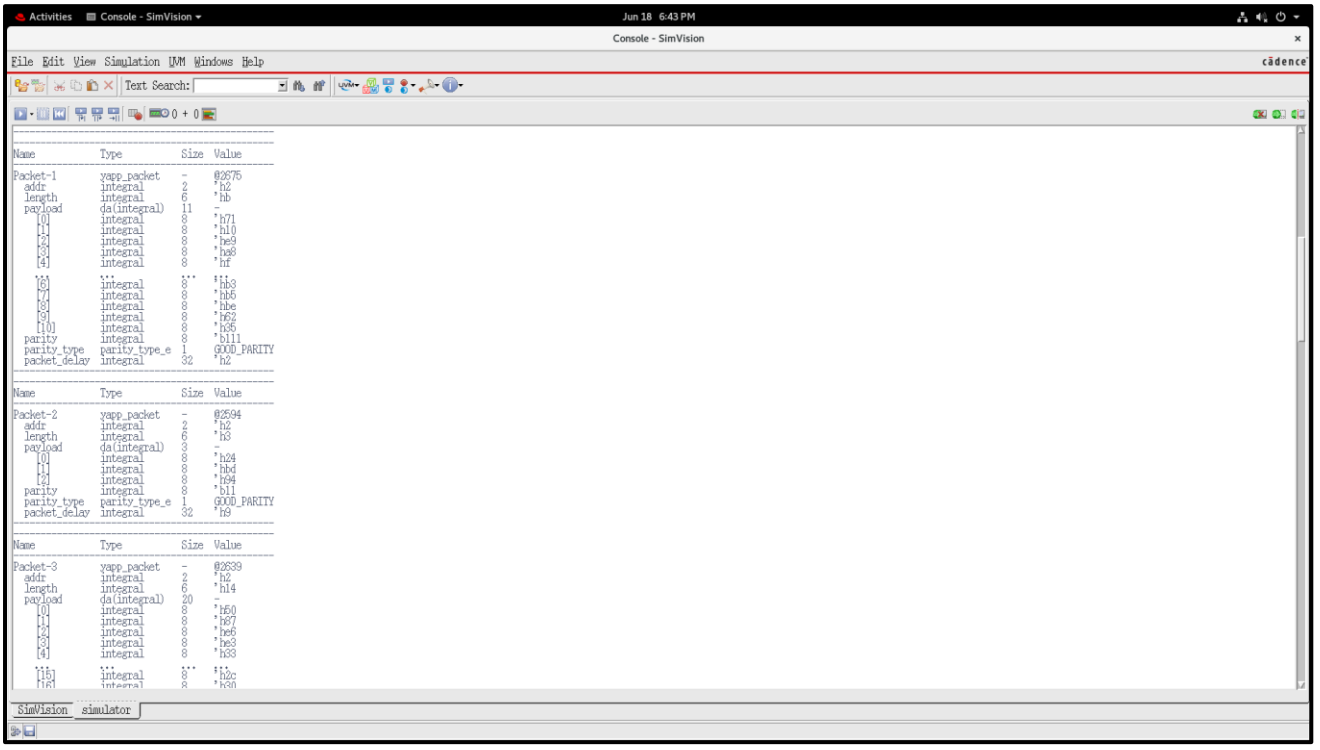
Name: Ayesha Binte Safiullah

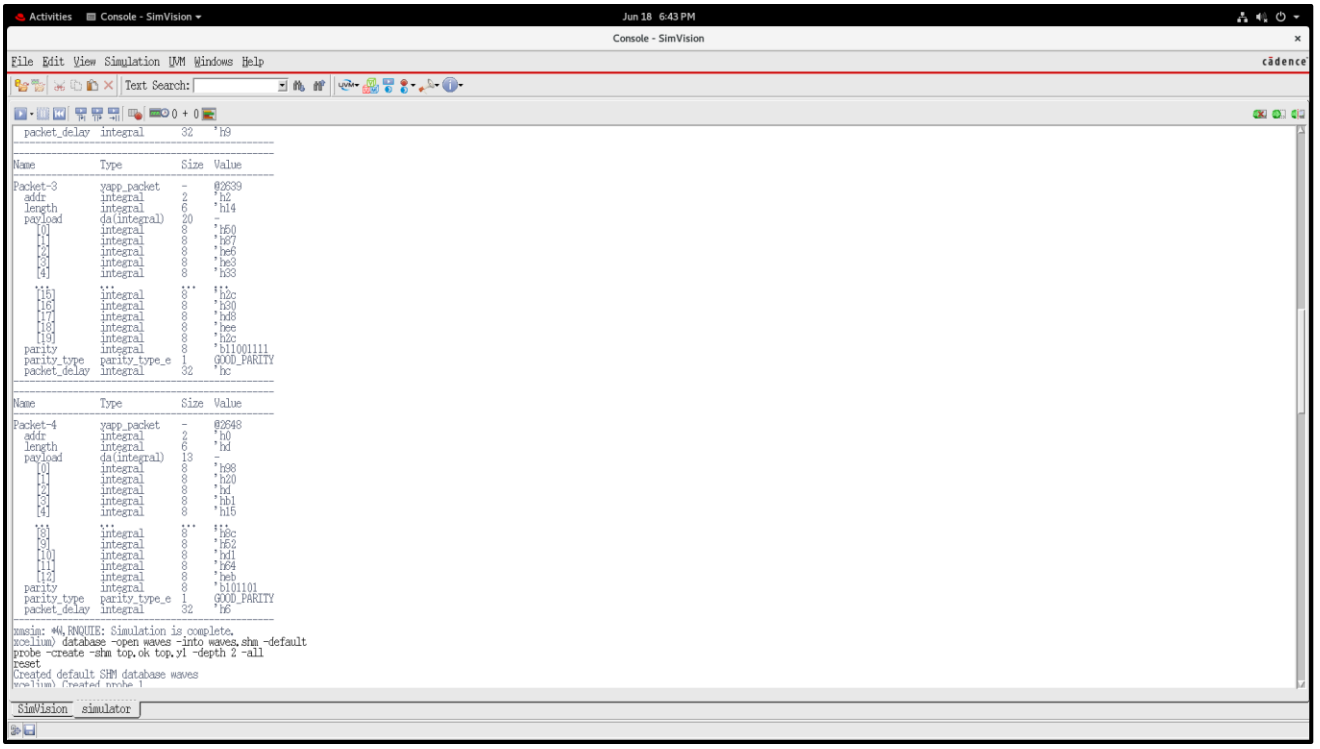
Submitted To: NCDC

Task 1: Creating Data Item and a Simple Test

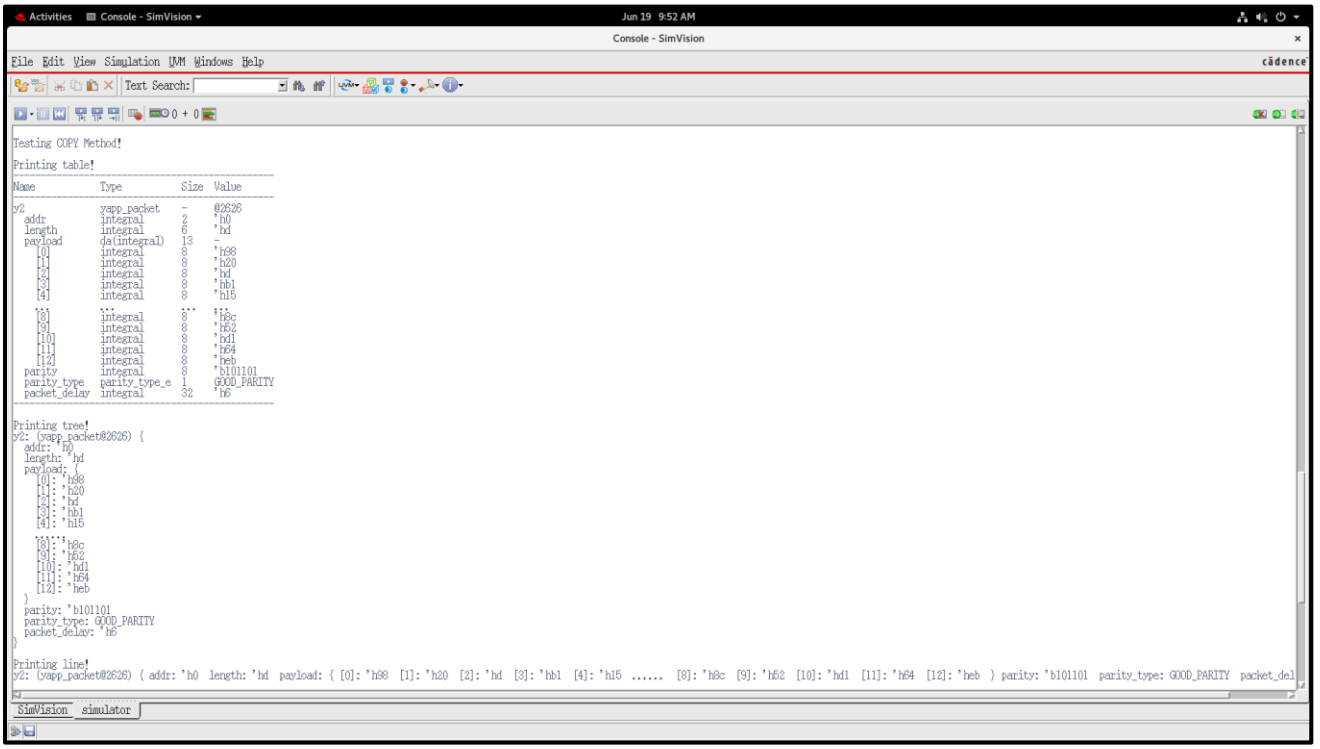
- **Generation of five random packets using for loop**



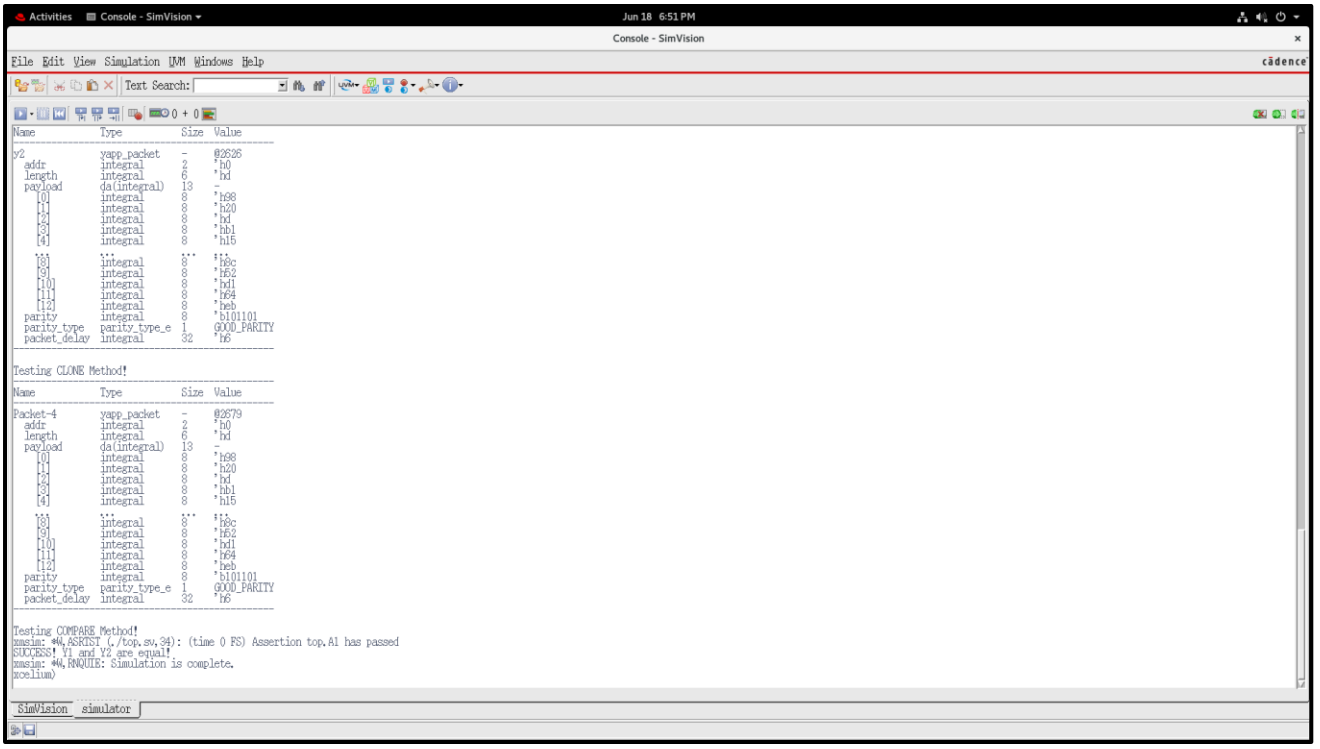




- **Testing Copy Method with uvm_default_tree, uvm_default_table and uvm_default_line:**



- **Testing Clone and Compare Method:**



Task 2: Creating Test and Testbench Components

- **Does the printed topology match your expectations for the UVM hierarchy?**

  Yes.

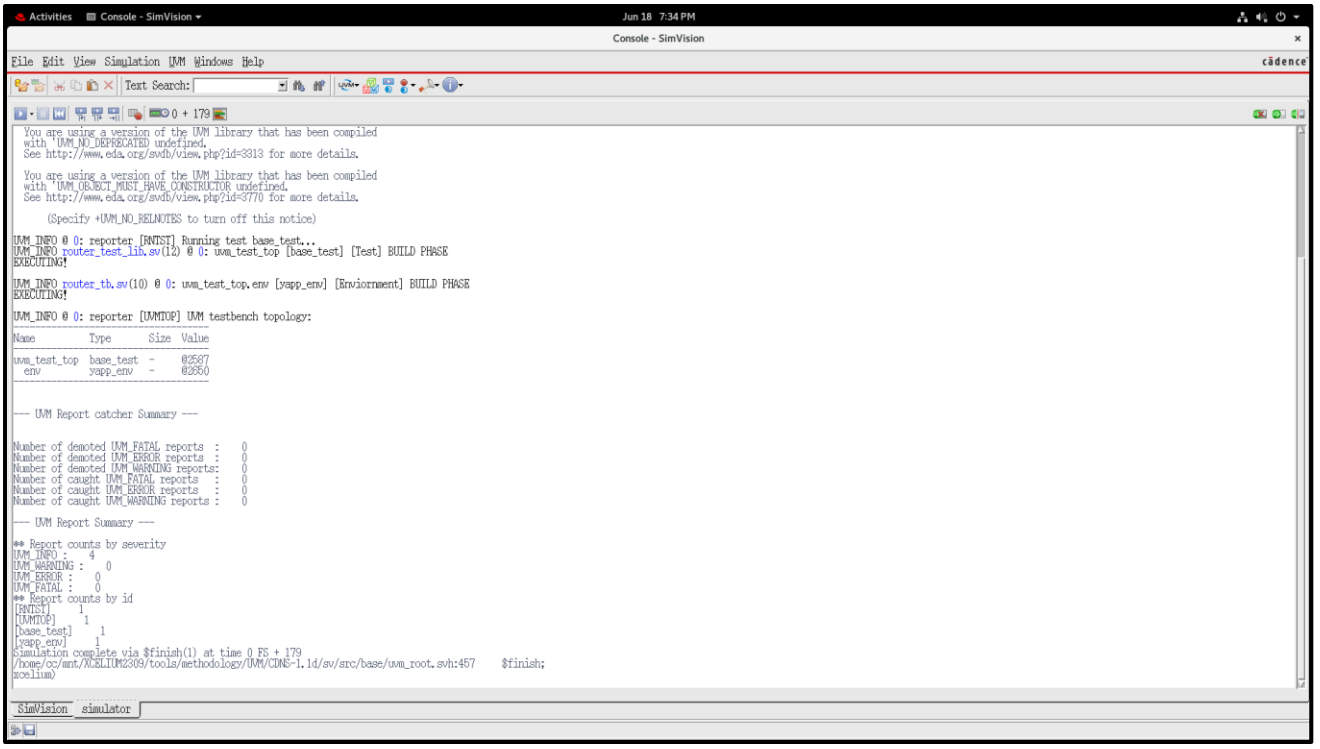
- **Which test class is being executed?**

  Base_test

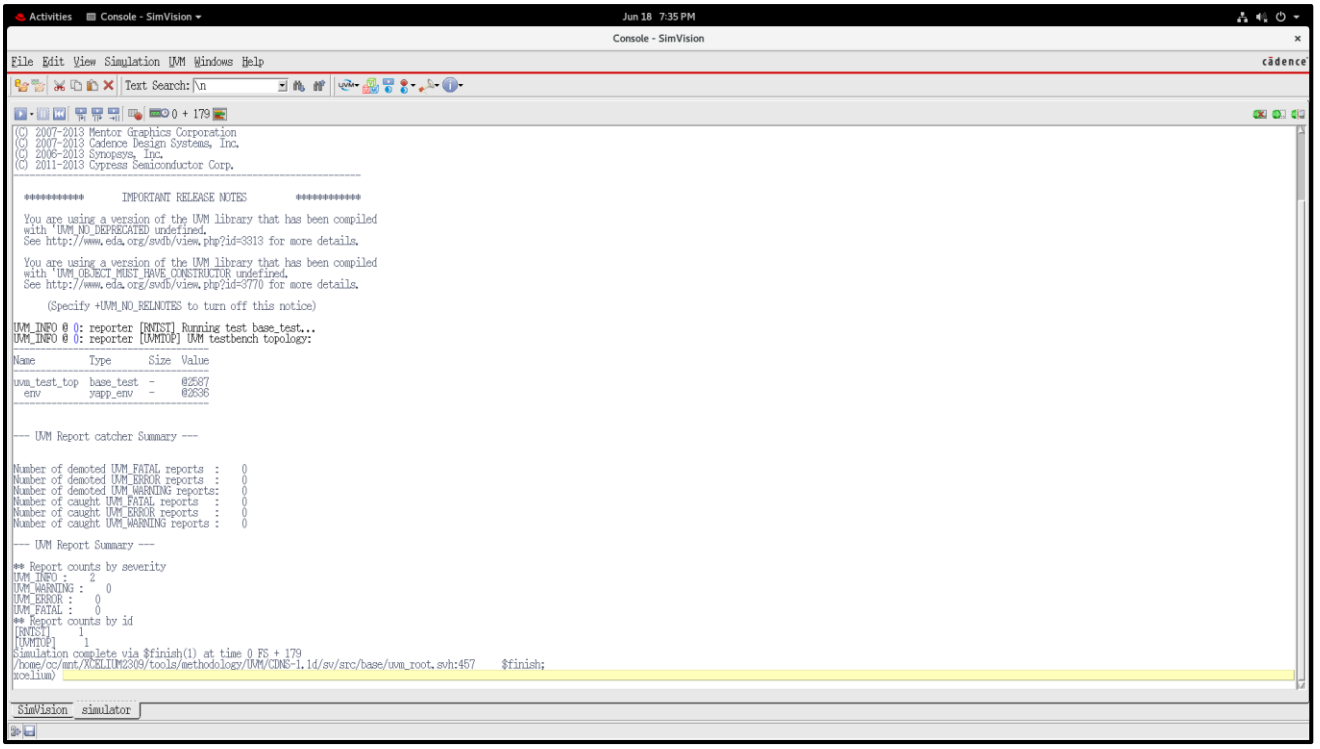
- **Do you see build phase reports from both test and testbench?**

  Yes.

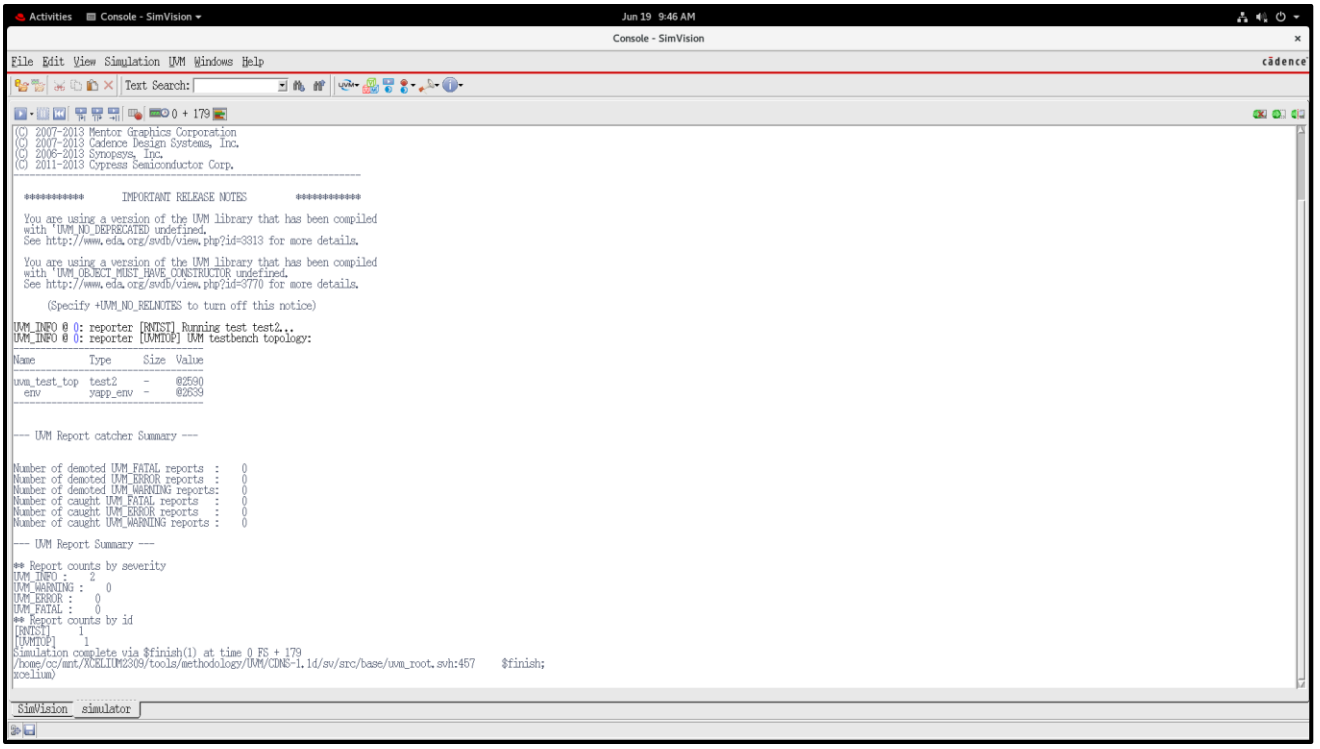
- **Testing UVM_VERBOSITY=UVM_HIGH for base_test:**



- **Testing UVM_VERBOSITY=UVM_LOW for base_test:**



- **Testing test2:**



- **What is the minimum amount of code for test2, given that we are inheriting from base_test?**

  The class needs to be registered in factory using uvm_component_utils and a constructor needs to be declared.

THE END