



Digital Design Verification
Lab Manual # 37 – Creating a Stimulus
Model, Test and Testbench
Components

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Submitted To: NCDC

Task 1: Creating Data Item and a Simple Test

- Generation of five random packets using for loop

The screenshot shows the Cadence SimVision console window. The title bar indicates 'Jun 18 6:43 PM' and 'Console - SimVision'. The menu bar includes 'File', 'Edit', 'View', 'Simulation', 'UVM', 'Windows', and 'Help'. The toolbar contains various icons for file operations, search, and simulation control. The main text area displays the following content:

```
SOURCE default: 1
xcelium) source /home/cc/mt/XCELIUM2309/tools/xcelium/files/xsimarc
xcelium) source /home/cc/mt/XCELIUM2309/tools/methodology/UVM/CDCS-1.1d/additions/sv/files/tcl/uvm_sim.tcl
xcelium) run

CDCS-UVM-1.1d (23.09-a006)
(C) 2007-2013 Mentor Graphics Corporation
(C) 2007-2013 Cadence Design Systems, Inc.
(C) 2006-2013 Synopsys, Inc.
(C) 2011-2013 Cypress Semiconductor Corp.

***** IMPORTANT RELEASE NOTES *****

You are using a version of the UVM library that has been compiled
with 'UVM_NO_DEPRECATED' undefined.
See http://www.eda.org/svdb/view.php?id=3313 for more details.

You are using a version of the UVM library that has been compiled
with 'UVM_NO_DEPRECATED' undefined.
See http://www.eda.org/svdb/view.php?id=3770 for more details.

(Specify +UVM_NO_DEPRECATED to turn off this notice)

Generating 5 random packets
stop -create -name Randomize -randomize
Created stop Randomize

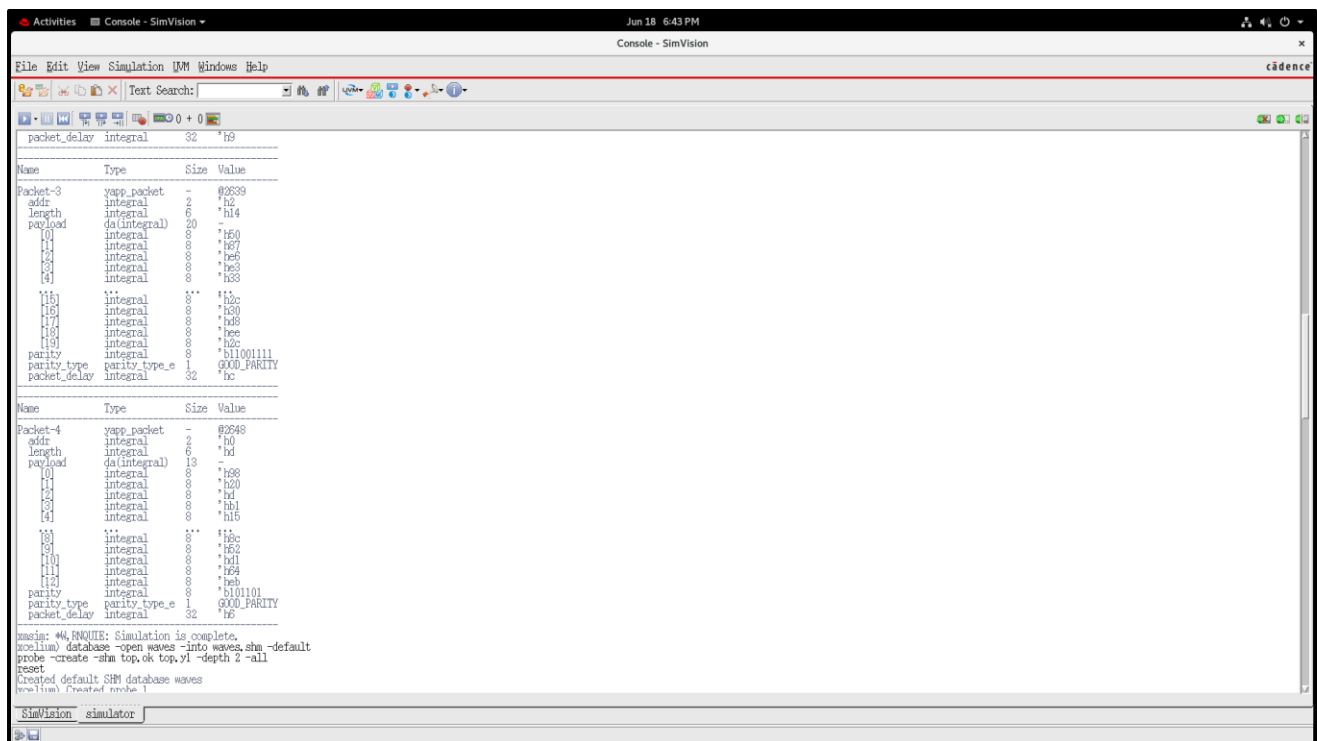
Name      Type      Size  Value
-----
Packet-0  yapp_packet  -    02674
addr      integral    2     'h0
length    integral    6     'h32
payload   da(integral) 50    -
[0]       integral    8     'h86
[1]       integral    8     'hca
[2]       integral    8     'h67
[3]       integral    8     'h2
[4]       integral    8     'h8a
[5]       ...
[6]       integral    8     'h17
[7]       integral    8     'h3b
[8]       integral    8     'h77
[9]       integral    8     'h1a
[10]      integral    8     'h66
parity    integral    8     b11000010
parity_type parity_type_e 1     GOOD_PARITY
packet_delay integral    32    'h2
```

The screenshot shows the Cadence SimVision console window, displaying the results of generating five random packets. The title bar indicates 'Jun 18 6:43 PM' and 'Console - SimVision'. The menu bar includes 'File', 'Edit', 'View', 'Simulation', 'UVM', 'Windows', and 'Help'. The toolbar contains various icons for file operations, search, and simulation control. The main text area displays the following content:

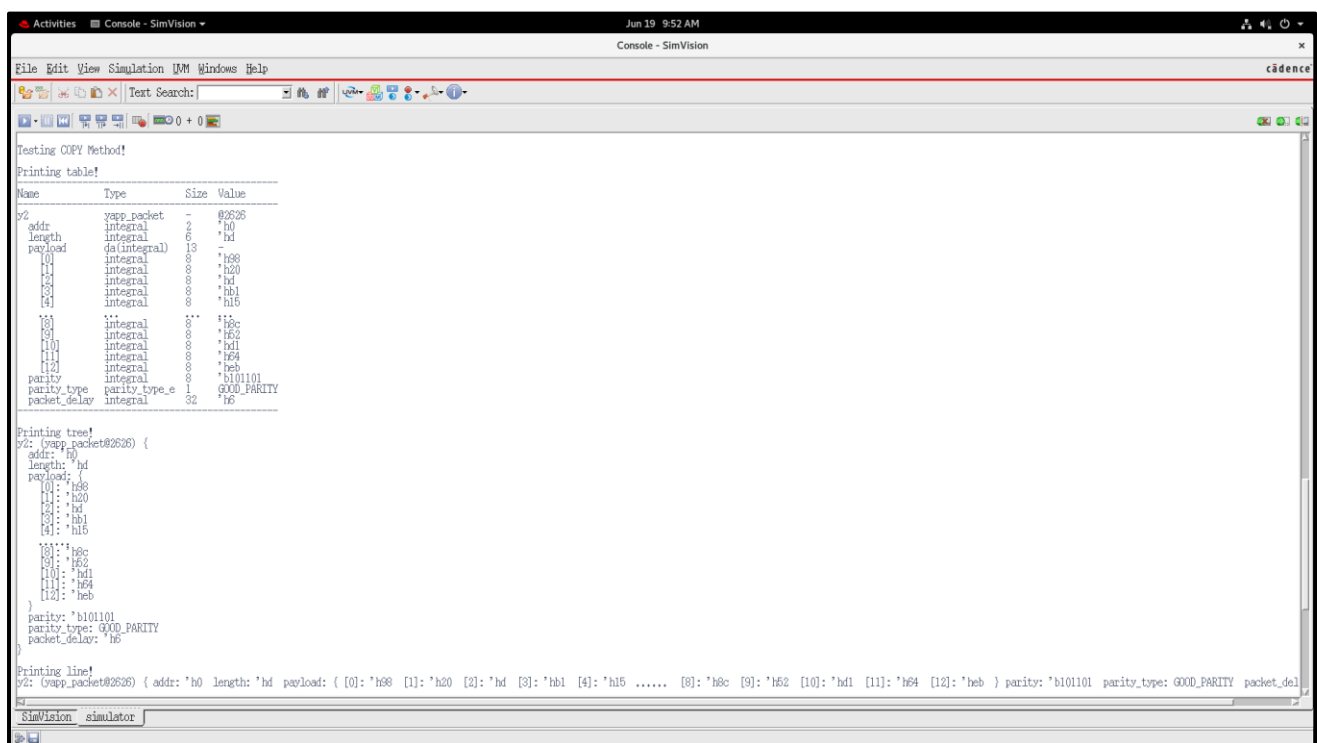
```
Name      Type      Size  Value
-----
Packet-1  yapp_packet  -    02675
addr      integral    2     'h2
length    integral    6     'hb
payload   da(integral) 11    -
[0]       integral    8     'h71
[1]       integral    8     'h10
[2]       integral    8     'h6d
[3]       integral    8     'h68
[4]       integral    8     'h1
[5]       ...
[6]       integral    8     'h3
[7]       integral    8     'h6b
[8]       integral    8     'hbe
[9]       integral    8     'h62
[10]      integral    8     'h36
parity    integral    8     b111
parity_type parity_type_e 1     GOOD_PARITY
packet_delay integral    32    'h2

Name      Type      Size  Value
-----
Packet-2  yapp_packet  -    02694
addr      integral    2     'h2
length    integral    6     'h3
payload   da(integral) 30    -
[0]       integral    8     'h24
[1]       integral    8     'h4
[2]       integral    8     'h94
[3]       integral    8     'h6
[4]       integral    8     'h33
[5]       ...
[6]       integral    8     'h2
[7]       integral    8     'h30

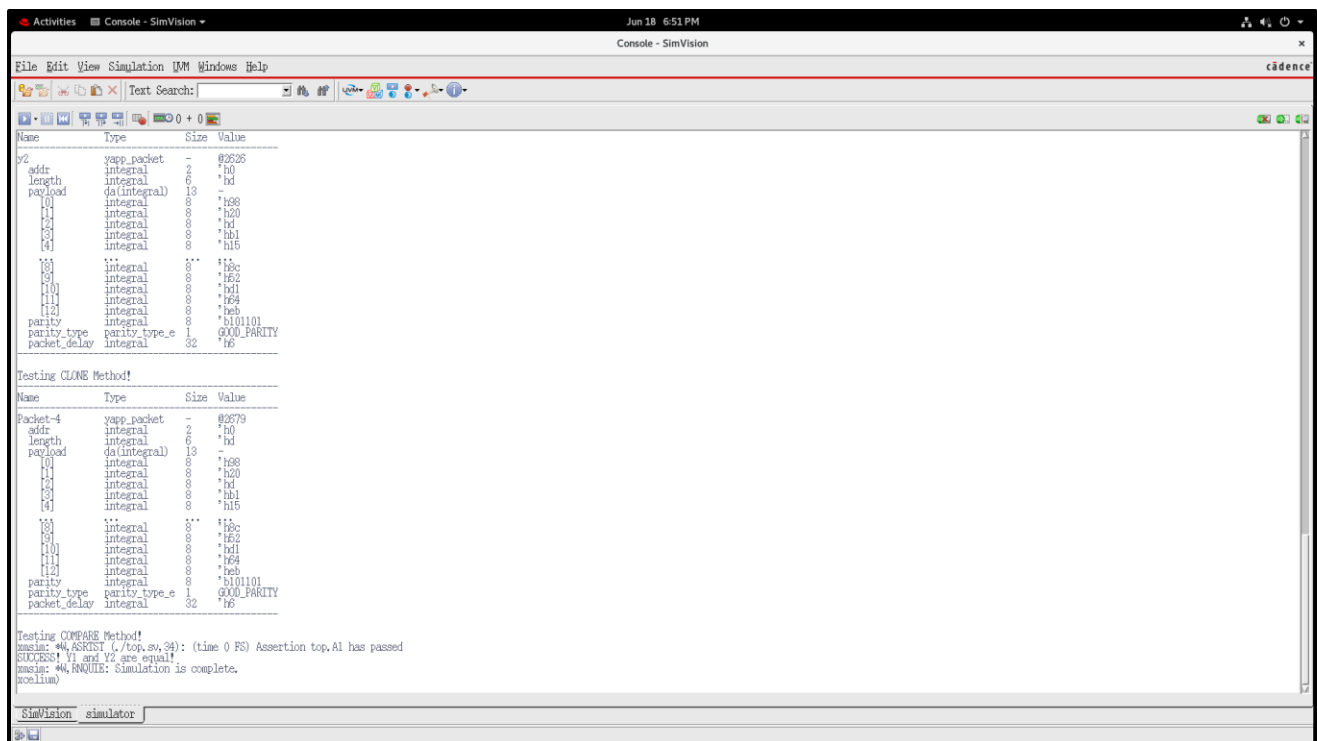
Name      Type      Size  Value
-----
Packet-3  yapp_packet  -    02639
addr      integral    2     'h2
length    integral    6     'h14
payload   da(integral) 20    -
[0]       integral    8     'h50
[1]       integral    8     'h67
[2]       integral    8     'h66
[3]       integral    8     'h63
[4]       integral    8     'h33
[5]       ...
[6]       integral    8     'h2
[7]       integral    8     'h30
```



- **Testing Copy Method with uvm_default_tree, uvm_default_table and uvm_default_line:**



- **Testing Clone and Compare Method:**



Task 2: Creating Test and Testbench Components

- Does the printed topology match your expectations for the UVM hierarchy?

Yes.

- Which test class is being executed?

Base test

- Do you see build phase reports from both test and testbench?

Yes.

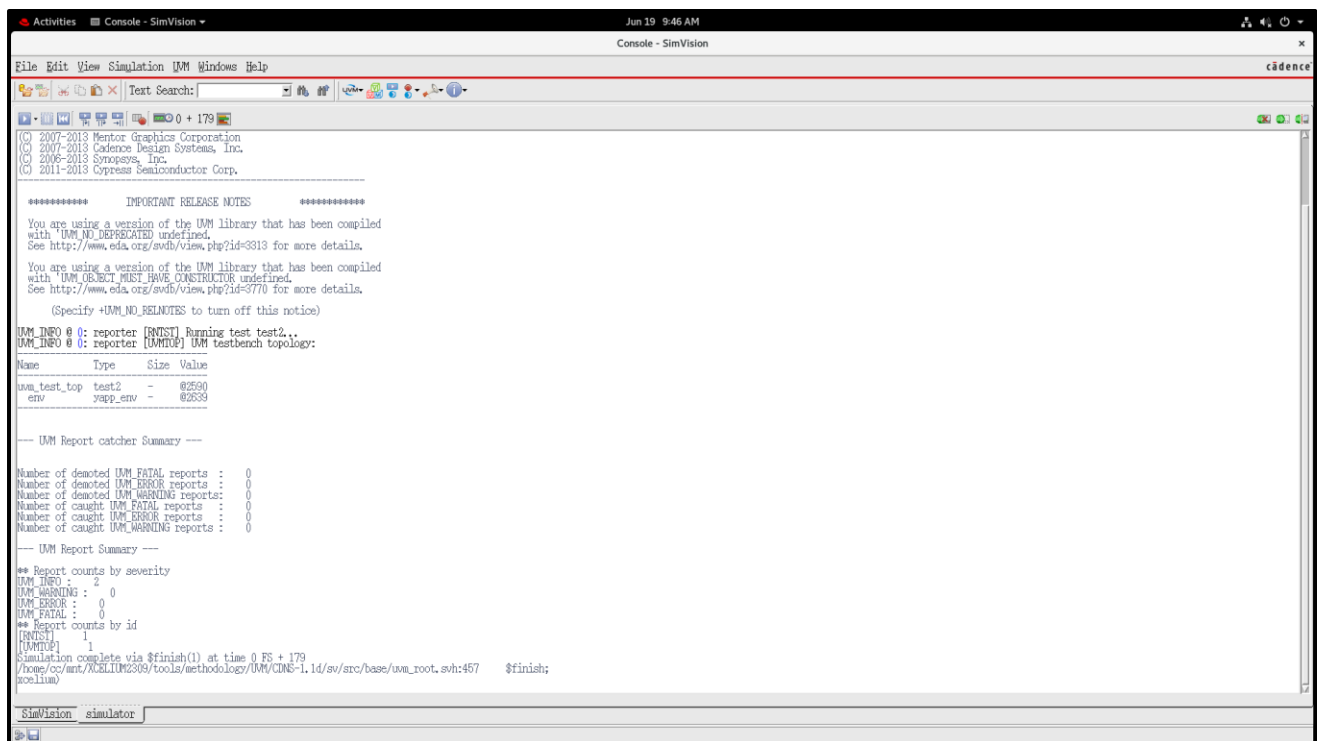
- Testing UVM_VERBOSITY=UVM_HIGH for base_test:

```
Jun 18 7:34 PM
Console - SimVision
File Edit View Simulation UVM Windows Help
Text Search:
0 + 179
You are using a version of the UVM library that has been compiled
with 'UVM_NO_DEPRECATED' undefined.
See http://www.eda.org/svdb/view.php?id=3313 for more details.
You are using a version of the UVM library that has been compiled
with 'UVM_8.BE.CI.MUST_HAVE_CONSTRUCTOR' undefined.
See http://www.eda.org/svdb/view.php?id=3770 for more details.
(Specify +UVM_NO_RELEASENOTES to turn off this notice)
UVM_INFO # 0: reporter [RNTST] Running test base_test...
UVM_INFO router_test_lib.sv(12) # 0: uvm_test_top [base_test] [Test] BUILD PHASE
EXECUTING!
UVM_INFO router_th.sv(10) # 0: uvm_test_top.env [yapp_env] [Environment] BUILD PHASE
EXECUTING!
UVM_INFO # 0: reporter [UMTOP] UVM testbench topology:
Name      Type      Size  Value
uvm_test_top base_test -    82587
env        yapp_env  -    82636
--- UVM Report catcher Summary ---
Number of desotet UVM_FATAL reports : 0
Number of desotet UVM_ERROR reports : 0
Number of desotet UVM_WARNING reports : 0
Number of caught UVM_FATAL reports : 0
Number of caught UVM_ERROR reports : 0
Number of caught UVM_WARNING reports : 0
--- UVM Report Summary ---
** Report counts by severity
UVM_INFO : 4
UVM_WARNING : 0
UVM_ERROR : 0
UVM_FATAL : 0
** Report counts by id
[RNTST] 1
[UMTOP] 1
[base_test] 1
[yapp_env] 1
Simulation complete via $finish(1) at time 0 FS + 179
/home/cc/mnt/X06LUM2309/tools/methodology/UVM/CIN5-1.1d/sv/src/base/uvm_root.svh:457 $finish;
(see live)
SimVision simulator
```

- Testing UVM_VERBOSITY=UVM_LOW for base_test:

```
Jun 18 7:35 PM
Console - SimVision
File Edit View Simulation UVM Windows Help
Text Search:
0 + 179
(C) 2007-2013 Mentor Graphics Corporation
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(C) 2006-2013 Synopsys, Inc.
(C) 2011-2013 Cypress Semiconductor Corp.
***** IMPORTANT RELEASE NOTES *****
You are using a version of the UVM library that has been compiled
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See http://www.eda.org/svdb/view.php?id=3313 for more details.
You are using a version of the UVM library that has been compiled
with 'UVM_8.BE.CI.MUST_HAVE_CONSTRUCTOR' undefined.
See http://www.eda.org/svdb/view.php?id=3770 for more details.
(Specify +UVM_NO_RELEASENOTES to turn off this notice)
UVM_INFO # 0: reporter [RNTST] Running test base_test...
UVM_INFO # 0: reporter [UMTOP] UVM testbench topology:
Name      Type      Size  Value
uvm_test_top base_test -    82587
env        yapp_env  -    82636
--- UVM Report catcher Summary ---
Number of desotet UVM_FATAL reports : 0
Number of desotet UVM_ERROR reports : 0
Number of desotet UVM_WARNING reports : 0
Number of caught UVM_FATAL reports : 0
Number of caught UVM_ERROR reports : 0
Number of caught UVM_WARNING reports : 0
--- UVM Report Summary ---
** Report counts by severity
UVM_INFO : 2
UVM_WARNING : 0
UVM_ERROR : 0
UVM_FATAL : 0
** Report counts by id
[RNTST] 1
[UMTOP] 1
Simulation complete via $finish(1) at time 0 FS + 179
/home/cc/mnt/X06LUM2309/tools/methodology/UVM/CIN5-1.1d/sv/src/base/uvm_root.svh:457 $finish;
(see live)
SimVision simulator
```

- Testing test2:



The screenshot shows the Cadence SimVision console window. The title bar indicates the date and time as 'Jun 19 9:46 AM'. The menu bar includes 'File', 'Edit', 'View', 'Simulation', 'UVM', 'Windows', and 'Help'. The toolbar contains various icons for file operations and simulation control. The main text area displays the following output:

```
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(C) 2006-2013 Synopsys, Inc.
(C) 2011-2013 Cypress Semiconductor Corp.

***** IMPORTANT RELEASE NOTES *****

You are using a version of the UVM library that has been compiled
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See http://www.eda.org/svdb/view.php?id=3313 for more details.

You are using a version of the UVM library that has been compiled
with 'UVM_OBJECT_MUST_HAVE_CONSTRUCTOR' undefined.
See http://www.eda.org/svdb/view.php?id=3770 for more details.

(Specify +UVM_NO_RELEASENOTES to turn off this notice)

UVM_INFO # 0: reporter [RUST] Running test test2..
UVM_INFO # 0: reporter [UVMTOP] UVM testbench topology:

Name      Type      Size Value
---
uvm_test_top test2    -    02590
env        yapp_env -    02539

--- UVM Report catcher Summary ---

Number of deasserted UVM_FATAL reports : 0
Number of deasserted UVM_ERROR reports : 0
Number of deasserted UVM_WARNING reports: 0
Number of caught UVM_FATAL reports : 0
Number of caught UVM_ERROR reports : 0
Number of caught UVM_WARNING reports : 0

--- UVM Report Summary ---

** Report counts by severity
UVM_INFO : 2
UVM_WARNING : 0
UVM_ERROR : 0
UVM_FATAL : 0

** Report counts by id
[RUST] 1
[UVMTOP] 1
Simulation complete via $finish(1) at time 0 FS + 179
/home/cc/mnt/XC6L/U02309/tools/methodology/UVM/CMS-1.1d/sv/src/base/uvm_root.svh:457 $finish;
20110619

SimVision simulator
```

- What is the minimum amount of code for test2, given that we are inheriting from base_test?

The class needs to be registered in factory using uvm_component_utils and a constructor needs to be declared.

THE END