Design of Sequential Circuits

This example is taken from M. M. Mano, *Digital Design*, Prentice Hall, 1984, p.235.

Example 1.3 We wish to design a synchronous sequential circuit whose state diagram is shown in Figure 13. The type of flip-flop to be use is J-K.

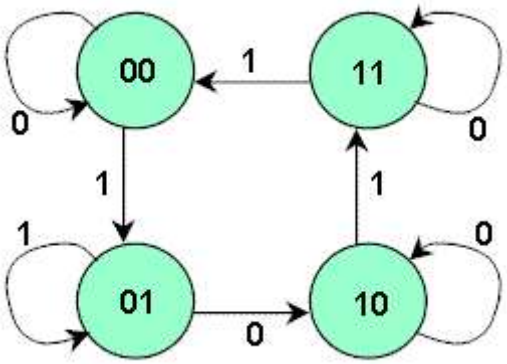

Figure 13. State diagram

From the state diagram, we can generate the state table shown in Table 9. Note that there is no output section for this circuit. Two flip-flops are needed to represent the four states and are designated Q_0Q_1. The input variable is labeled x.

Present State Q_0 Q_1	Next State x = 0	Next State x = 1
0 0	0 0	0 1
0 1	1 0	0 1
1 0	1 0	1 1
1 1	1 1	0 0

Table 9. State table.

We shall now derive the excitation table and the combinational structure. The table is now arranged in a different form shown in Table 11, where the present state and input variables are arranged in the form of a truth table. Remember, the excitable for the JK flip-flop was derive in Table 1.

Table 10. Excitation table for JK flip-flop

Output Transitions Q →Q(next)	Flip-flop inputs J K
0 → 0	0 X
0 → 1	1 X
1 → 0	X 1

1 → 1	X 0

Table 11. Excitation table of the circuit

Present State Q_0 Q_1	Next State Q_0 Q_1	Input x	Flip-flop Inputs J_0K_0	J_1K_1
0 0	0 0	0	0 X	0 X
0 0	0 1	1	0 X	1 X
0 1	1 0	0	1 X	X 1
0 1	0 1	1	0 X	X 0
1 0	1 0	0	X 0	0 X
1 0	1 1	1	X 0	1 X
1 1	1 1	0	X 0	X 0
1 1	0 0	1	X 1	X 1

In the first row of Table 11, we have a transition for flip-flop Q_0 from 0 in the present state to 0 in the next state. In Table 10 we find that a transition of states from 0 to 0 requires that input J = 0 and input K = X. So 0 and X are copied in the first row under J_0 and K_0 respectively. Since the first row also shows a transition for the flip-flop Q_1 from 0 in the present state to 0 in the next state, 0 and X are copied in the first row under J_1 and K_1. This process is continued for each row of the table and for each flip-flop, with the input conditions as specified in Table 10.

The simplified Boolean functions for the combinational circuit can now be derived. The input variables are Q_0, Q_1, and x; the output are the variables J_0, K_0, J_1 and K_1. The information from the truth table is plotted on the Karnaugh maps shown in Figure 14.

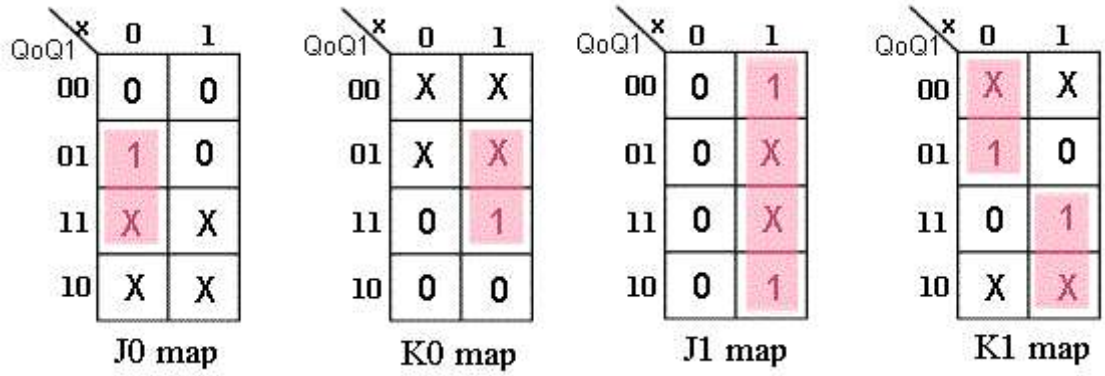

Figure 14. Karnaugh Maps

The flip-flop input functions are derived:

$J_0 = Q_1 * x'$ $K_0 = Q_1 * x$

$J_1 = x$ $K_1 = Q_0' * x' + Q_0 * x = Q_0 \odot x$

Note: the symbol ⊙ is exclusive-NOR.

The logic diagram is drawn in Figure 15.

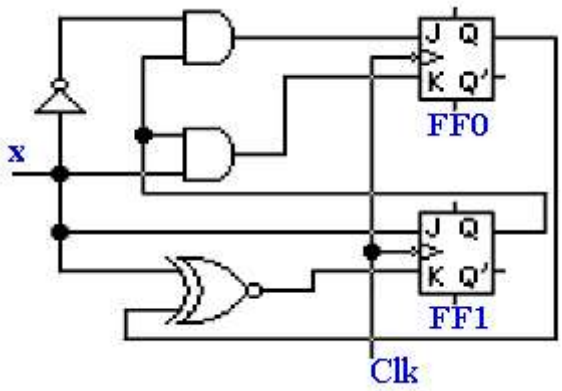

Figure 15. Logic diagram of the sequential circuit.

Example 1.4