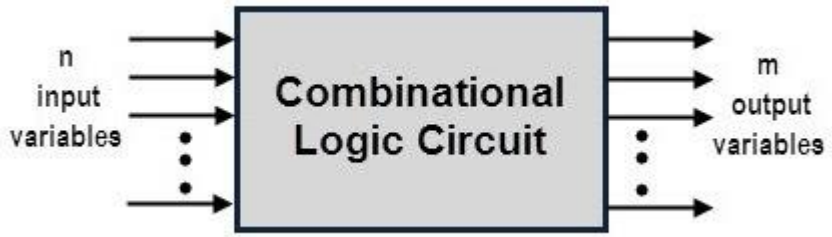
Chapter 5

SYNCHRONOUS SEQUENTIAL LOGIC

Sequential Logic

- In combinational digital circuits, the outputs at any instant of time are entirely dependent upon the inputs present at that time.



- There are many applications in which digital outputs are required to be generated in accordance with the sequence in which the input signals are received. This requirement can not be satisfied using a combinational logic system. These applications require outputs to be generated that are not only dependent on the present input conditions but they also depend upon the past history of these inputs. The past history is provided by feedback from the output back to the input.

Sequential circuit

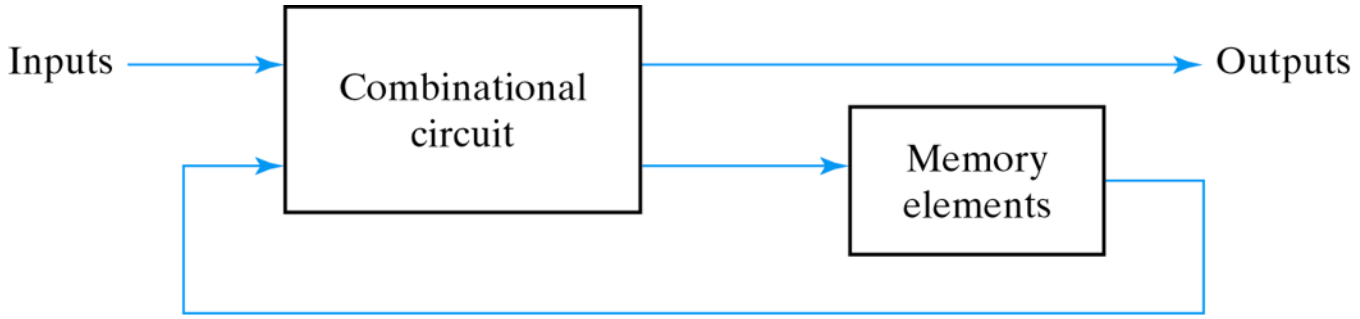


Fig. 5-1 Block Diagram of Sequential Circuit

Sequential circuit consists of a combinational circuit to which memory elements are connected to form a feedback path. The memory elements are devices capable of storing binary information within them. The binary information stored in the memory elements at any given time defines the state of the sequential circuit. The sequential circuit receives binary information from external inputs. These inputs, together with the present state of the memory elements, determine the binary value at the output terminals. They also determine the condition for changing the state in the memory elements.

The block diagram demonstrates that the external outputs in a sequential circuit are a function not only of external inputs but also of the present state of the memory elements. The next state of the memory elements is also a function of external inputs and the present state. Thus, a sequential circuit is specified by a time sequence of inputs, outputs and internal states.

For sequential circuit:

Present output= f(input, previous output)

Classification of sequential circuits:

❑Asynchronous sequential circuit:

A sequential circuit whose behavior depends upon the sequence in which the input signals change is referred to as an asynchronous sequential circuit. The outputs will be affected whenever the inputs change.

❑Synchronous sequential circuit:

A sequential circuit whose behavior can be defined from the knowledge of its signal at discrete instants of time is referred to as a synchronous sequential circuit. In these systems, the memory elements are affected only at discrete instants of time. The outputs are affected only with the application of a clock pulse.

Synchronous sequential circuits that use clock pulses in the inputs of memory elements are called clocked sequential circuits.

Flip-flops:

- The memory elements in a sequential circuit are called flip-flops (FFs).
- A Flip-flop(FF) circuit has two outputs. One for the normal value and one for the complement value of the stored bit.
- Binary information can enter a flip flop in a variety of ways and gives rise to different types of flip-flops:

i. SR Flip-flop

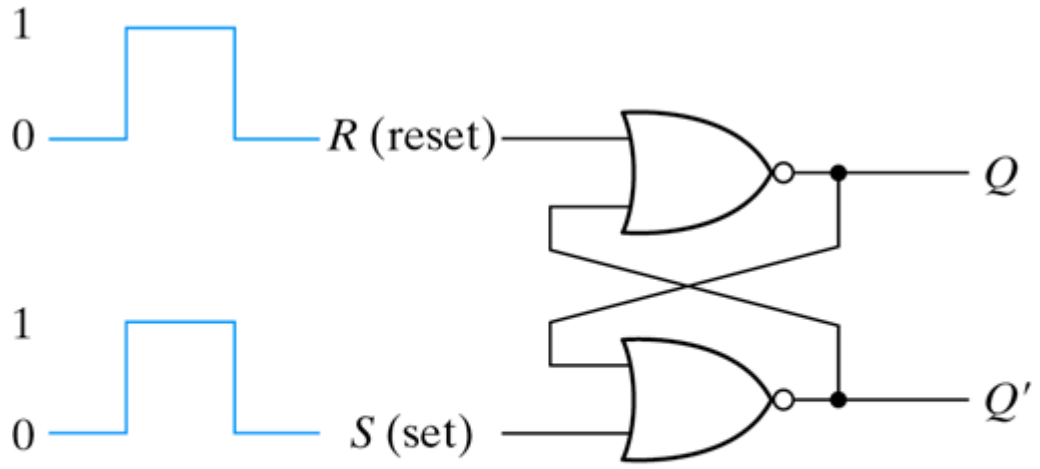
ii. JK Flip-flop

iii. T Flip-flop

iv. D Flip-flop etc.

Basic Flip-flop circuit:

- A Flip-flop circuit can be constructed from two NAND gates or two NOR gates. These flip-flops are shown in figure 1 and figure 2. Each FF has two outputs, Q and Q′, and two inputs, SET (S) and RESET(R). This type of FF is referred to as an SR FF or SR Latch.



(a) Logic diagram

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	

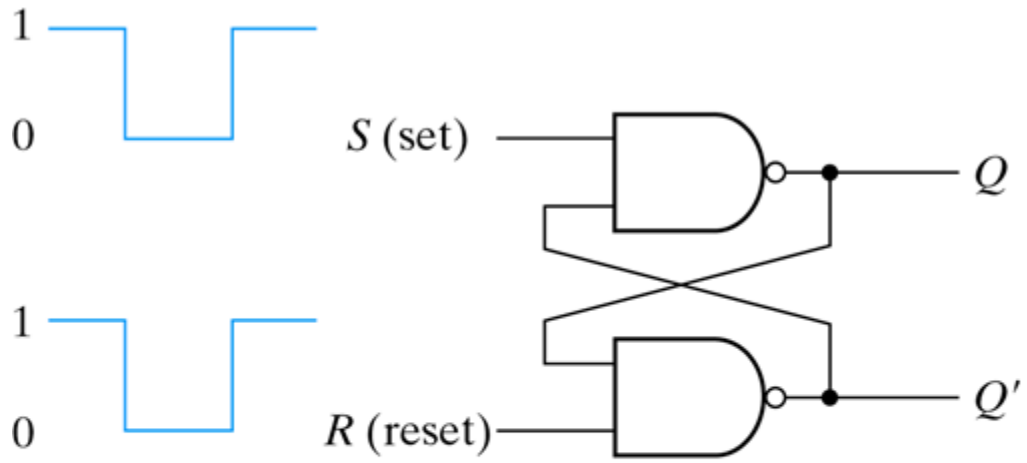
(b) Function table

Fig 1: Basic FF circuit with NOR gates

The FF in Fig 1 has two useful states. When Q= 1 and Q′= 0, it is in the set state (or 1-state).

When Q=0 and Q′= 1, it is in the clear state (or 0-state). The outputs Q and Q′ are complements of each other and are referred to as the normal and complement outputs, respectively. The binary state of the FF is taken to be the value of the normal output. When a 1 is applied to both the SET and RESET inputs of the FF in Fig.1, both Q and Q′ outputs go to 0. This condition violates the fact that both outputs are complement of each other. In normal operation this condition must be avoided by making sure that 1's are not applied to both inputs simultaneously.

The NAND basic FF circuit in Fig 2 operates with inputs normally at 1 unless the state of the flip flop has to be changed. A 0 applied momentarily to the set input causes Q to go to 1 and Q′ to go to 0, putting the FF in the set state. When both inputs go to 0, both outputs go to 1. This condition should be avoided in normal operation.



(a) Logic diagram

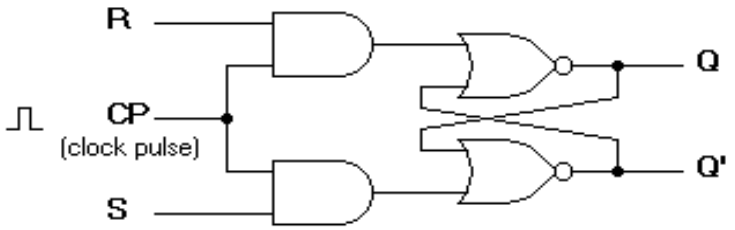
S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	

(b) Function table

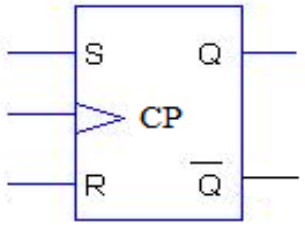
Fig 2. Basic FF circuit with NAND gates

i. Clocked SR Flip-flop

- The clocked SR flip-flop in following figure 3 consists of a basic NOR flip flop and two AND gates.



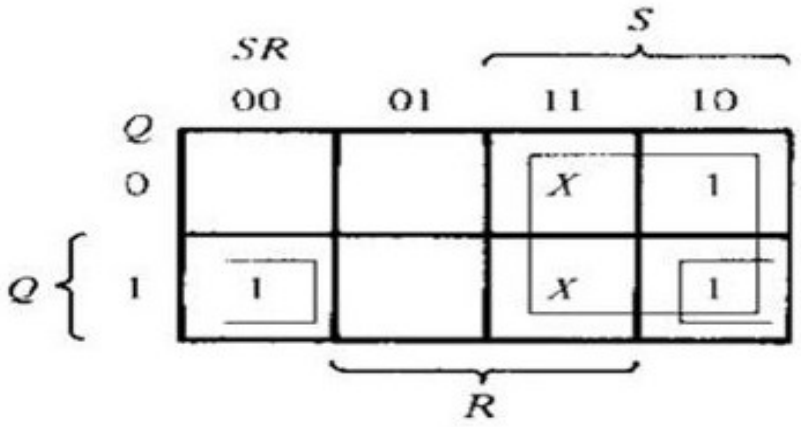
a) Logic diagram



b) Graphic Symbol

Q	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	indeterminate

c) Characteristic Table



$$Q(t+1) = S + R'Q$$

d) Characteristic equation

S	R	$Q_{(t+1)}$
0	0	Q
0	1	0
1	0	1
1	1	X

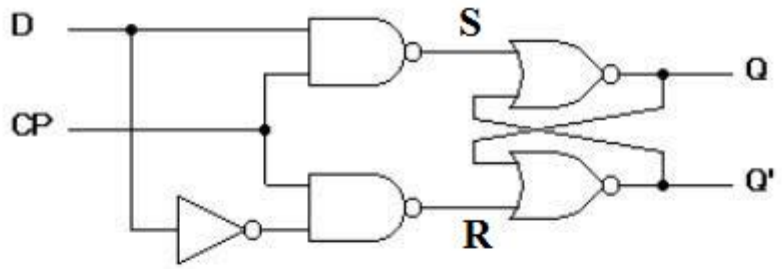
e) Truth table

Fig 3: Clocked SR Flip-flop

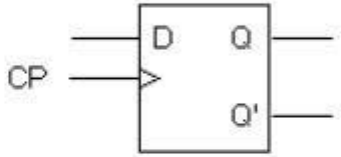
- The outputs of the two AND gates remain at 0 as long as the clock pulse (CP) is 0, regardless of the S and R input values. When the clock pulse goes to 1, information from the S and R inputs is allowed to reach the basic flip flop.
- The set state is reached with S=1, R=0 and CP=1.
- To change to the clear state, the inputs must be S=0, R=1 and CP=1.
- With both S=1and R=1, the occurrence of a clock pulse causes both outputs to momentarily go to 0. When the pulse is removed, the state of the flip flop is intermediate, i.e. either state may result.

ii. Clocked D Flip-flop

- The D flip flop shown in fig 4 is a modification of the clocked SR flip flop. The D input goes directly to the S input, and its complement is applied to the R input.



(a) Logic diagram



(b) Graphical symbol

Q D	Q(t+1)
0 0	0
0 1	1
1 0	0
1 1	1

(c) Truth table

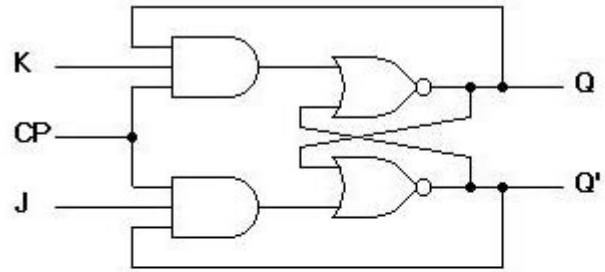
Characteristic Equation: Q (t+1) = D

Fig 4: Clocked D Flip-flop

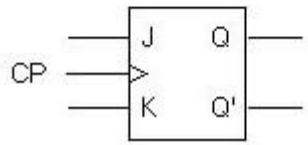
iii. Clocked JK Flip-flop

- A JK Flip flop is a refinement of the SR Flip flop in that the indeterminate state of the SR type is defined in the JK type. Inputs J and K behave like inputs S and R to set and clear the flip flop. When logic 1 inputs are applied to both J and K simultaneously, the flip flop switches to its complement state, i.e. if Q=1, it switches to Q=0 and vice versa.

- A clocked JK flip flop is shown in fig 5. Output Q is ANDed with K and CP inputs so that the flip flop is cleared during a CP only if Q=1, previously. Similarly, output Q′ is ANDed with J and CP input so that the flip flop is set with a CP only if Q′=1, previously.



(a) Logic diagram



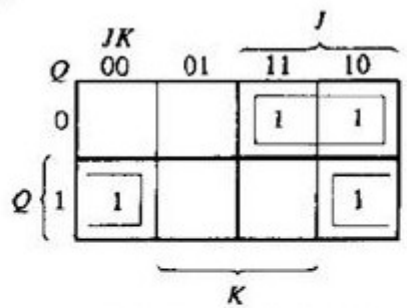
(b) Graphical symbol

Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

(c) Characteristic table

J	K	$Q_{(t+1)}$	
0	0	$Q_{(t)}$	*unchanged*
0	1	0	*reset*
1	0	1	*set*
1	1	$\overline{Q}_{(t)}$	*output inversion* *[Toggle]*

d) Truth table



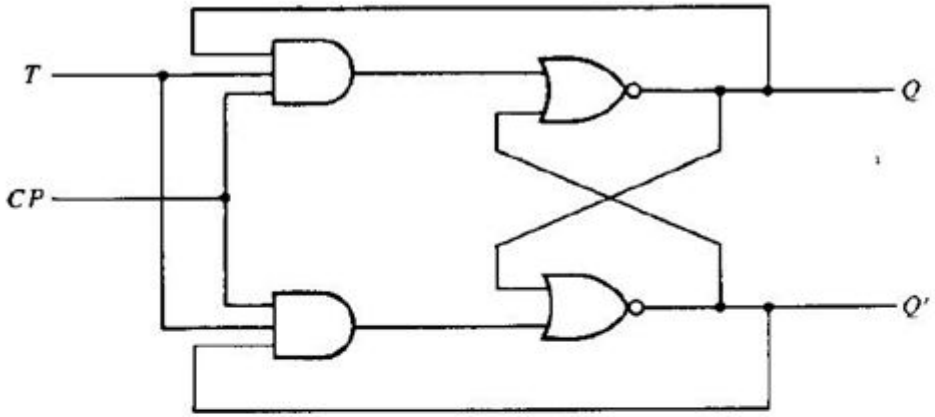
$$Q(t+1) = JQ' + K'Q$$

(e) Characteristic Equation

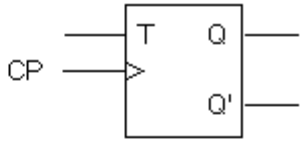
Fig 5: Clocked JK Flip flop

iv. **Clocked T Flip flop**

The T Flip flop is a single input version of the JK Flip flop. The T flip flop is obtained from the JK type if both inputs are tied together. The output of the T flip flop 'toggles' with each clock pulse.



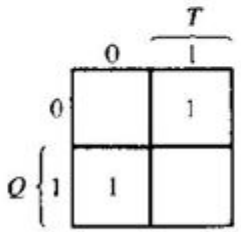
(a) Logic diagram



(d) Graphic Symbol

Q	T	Q(t + 1)
0	0	0
0	1	1
1	0	1
1	1	0

(b) Characteristic table



$Q(t+1) = TQ' + T'Q$

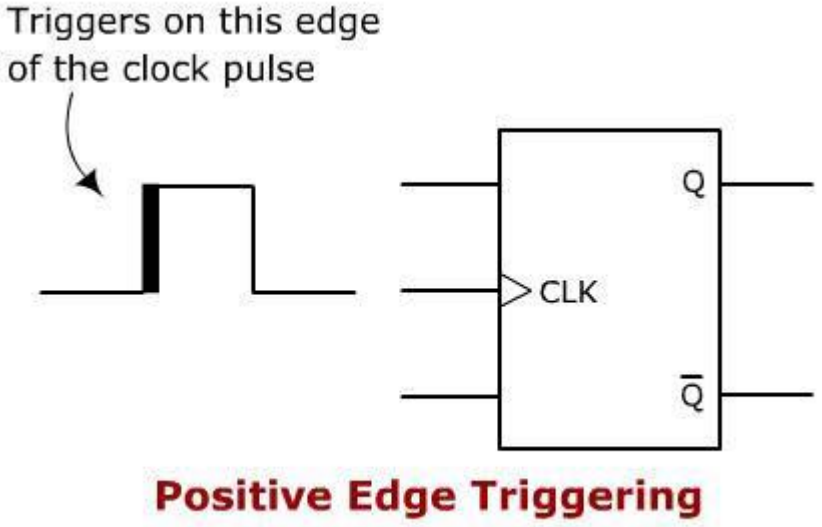
(c) Characteristic equation

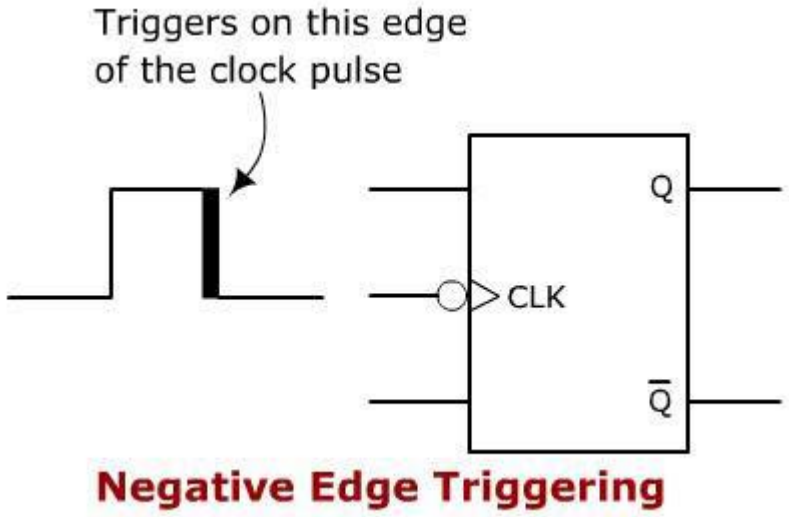
$Q(t+1) = T \oplus Q$

Fig 6: Clocked T Flip flop

Triggering of flip flops

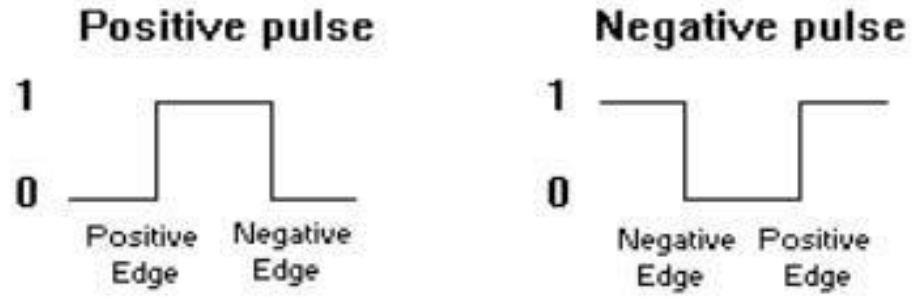
- The state of a flip flop is changed by a momentary (quick) change in the input signal. This change is called a trigger and the transition it causes is said to trigger the flip flop.
- **Positive Edge Triggering:** When a flip flop is required to respond at a LOW to HIGH transition state, POSITIVE edge triggering method is used. It is mainly identified from the clock input lead along with a triangle.
- **Negative Edge Triggering:** When a flip flop is required to respond during the HIGH to LOW transition state, a NEGATIVE edge triggering method is used. It is mainly identified from the clock input lead along with a low-state indicator and a triangle.
- Take a look at the symbolic representation shown below:





Clock Pulse Transition

- The movement of a trigger pulse is always from a 0 to 1 and then 1 to 0 of a signal. Thus it takes two transitions in a single signal. When it moves from 0 to 1 it is called a positive transition and when it moves from 1 to 0 it is called a negative transition.
- To understand more take a look at the images below.



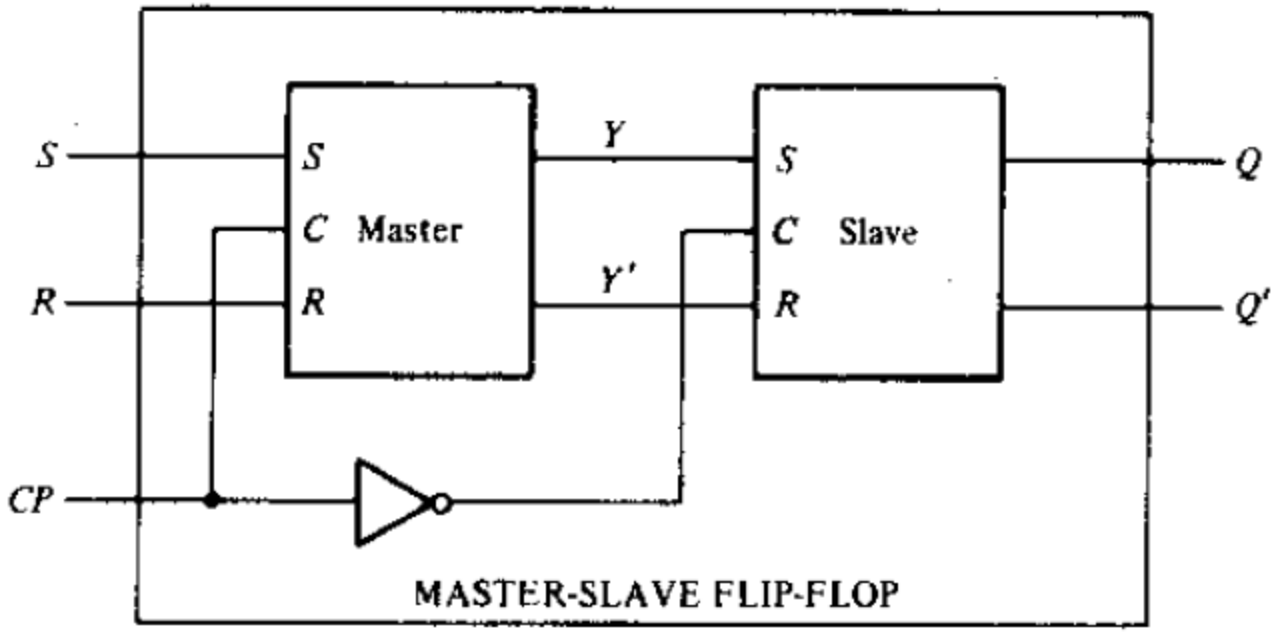
Definition of clock pulse transition

Master-Slave Flip-flop: [Self Study: See the book for details]

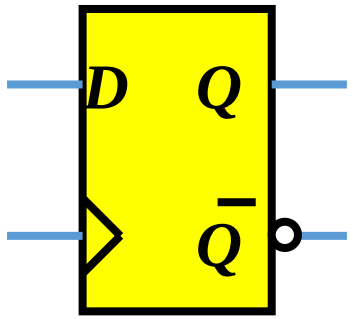
- A master slave flip flop is normally constructed from two flip flops, one is the master flip flop and the other is the slave. In addition to these two flip flops, the circuit also includes an inverter. The inverter is connected to clock pulse in such a way that the inverted CP is given to the slave flip flop i.e if CP=0 for a master flip flop, then CP=1 for a slave flip flop and vice versa.
- The master slave combination can be constructed for any type of flip flop by adding a clocked SR flip flop with an inverted clock to form the slave.

Master-Slave Flip-Flops

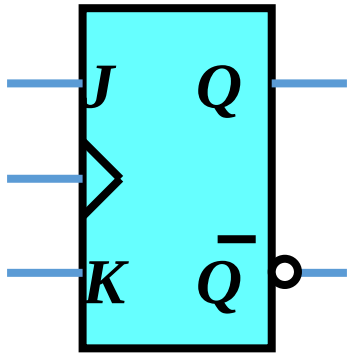
- *Master Slave SR* Flip-Flop (negative edge triggered)



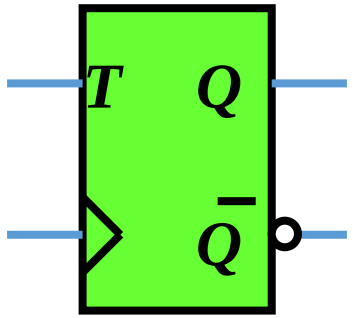
Flip-Flop Characteristic Tables



D	Q(t+1)	
0	0	Reset
1	1	Set

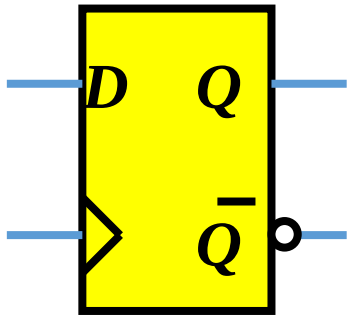


J	K	Q(t+1)	
0	0	Q(t)	No change
0	1	0	Reset
1	0	1	Set
1	1	Q'(t)	Toggle



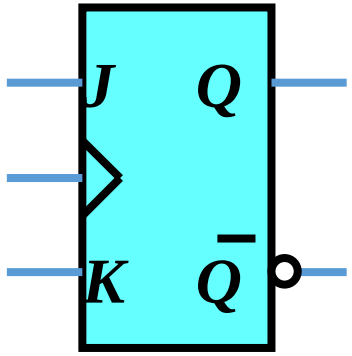
T	Q(t+1)	
0	Q(t)	No change
1	Q'(t)	Toggle

Flip-Flop Characteristic Equations



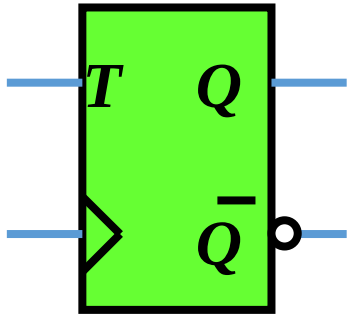
D	Q(t+1)
0	0
1	1

$$Q(t+1) = D$$



J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

$$Q(t+1) = JQ' + K'Q$$



T	Q(t+1)
0	Q(t)
1	Q'(t)

$$Q(t+1) = T \oplus Q$$

Excitation Table

- During the design process we usually know the transition from present state to next state and wish to find the flip flop input conditions that will cause the required transition. For this reason, we need a table that lists the required inputs for a given change of state. Such a list is called an excitation table.

SR Flip-flop

Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

D Flip-flop

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

JK flip-flop

Q(t)	Q(t+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

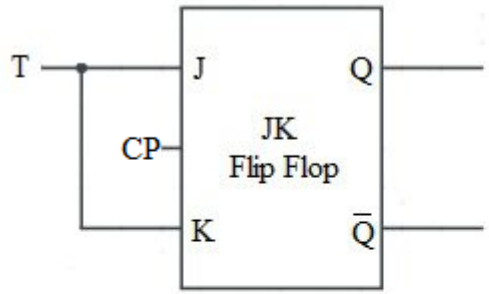
T flip-flop

Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

Excitation tables for all flip flops

Conversions:

- **From JK FF to T FF:**



JK:

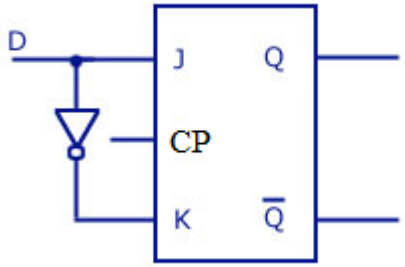
$Q(t+1) = JQ'+K'Q = JQ'+ J'Q$

$= J \oplus Q$

T:

$Q(t+1)= T \oplus Q$

From JK FF to D FF:



JK:

$Q(t+1) = JQ'+K'Q$

$= JQ'+ (J')'Q$

$= JQ'+ JQ$

$= J (Q'+ Q)$

$= J$

D:

$Q(t+1)= D$