# Register

- Clocked sequential circuits
  - A group of flip-flops and combinational gates.
  - Flip-flops + Combinational gates
    (essential) (optional)
- Register
  - A group of flip-flops.
  - Gates that determine how the information is transferred into the register.

# Registers

- A *n*-bit register
  - *n* flip-flops capable of storing *n* bits of binary information.
  - 4-bit register is shown in Fig. 6.1.

Clear =0 (active low); $A_x = 0$
Clock= ↑; $A_x=I_x$
Normal Operation; Clear =1

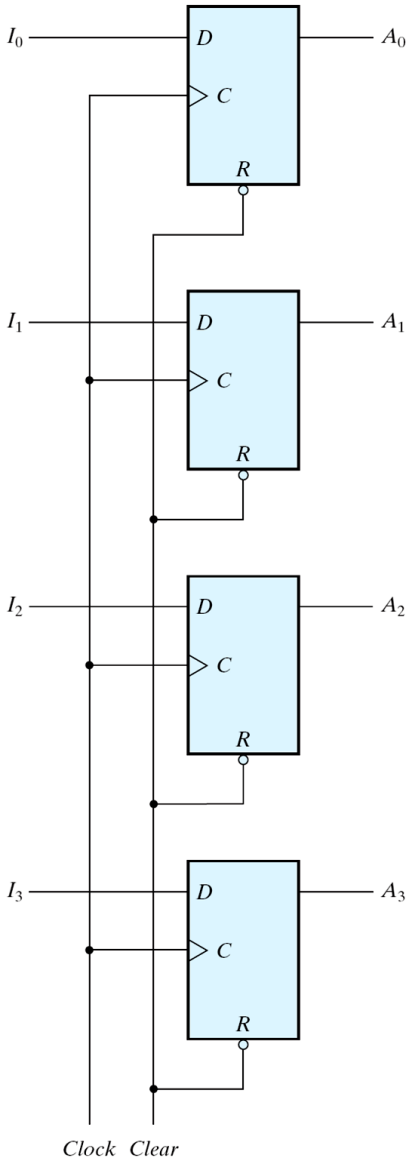



Fig. 6.1 Four-bit register

# REGISTERS

- *loading / updating the register:* The transfer of new information into a register
- *Parallel loading:* When all the bits of the register are loaded simultaneously with a common clock pulse

**Register with Parallel load [Self Study]**

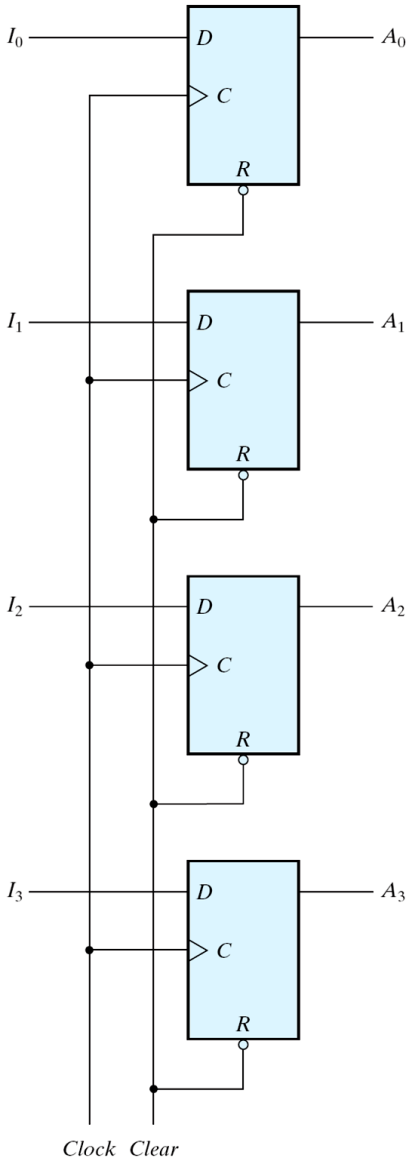
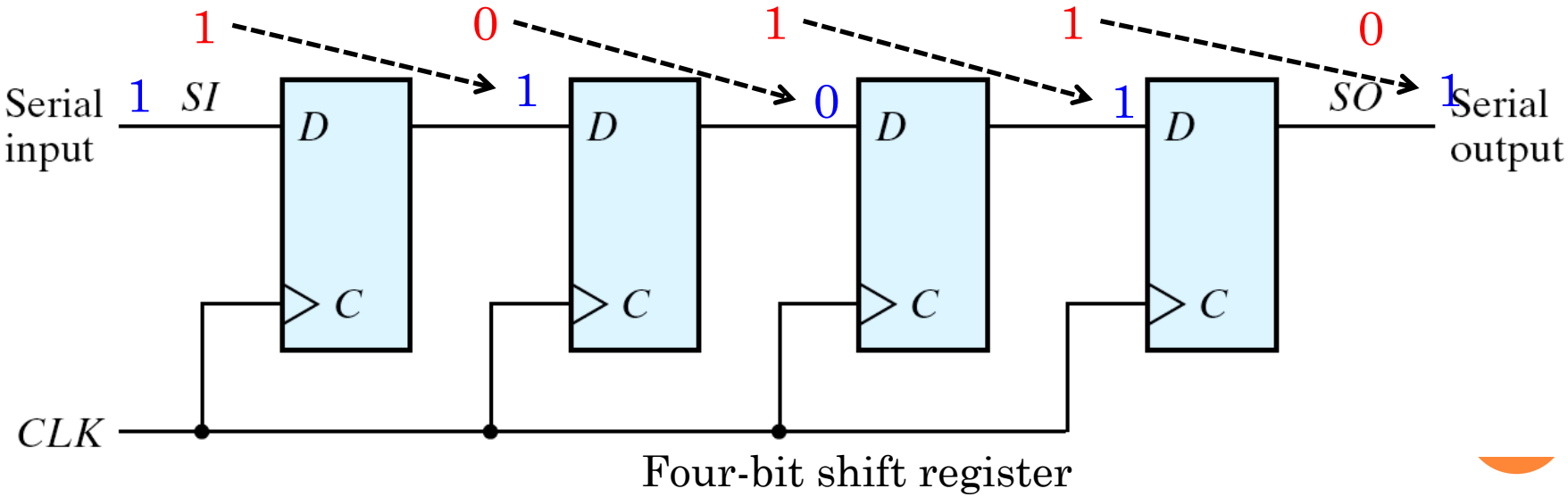



Fig. 6.1 Four-bit register

# Shift Registers

- A register capable of **shifting the binary information** held in each cell to its neighbouring cell, in a selected direction is called a **shift register.**
  - Clock controls the shift operation




Four-bit shift register

# Universal Shift Register

- Three types of shift register
  - Unidirectional shift register
    - A register capable of shifting in one direction.
  - Bidirectional shift register
    - A register can shift in both directions.
  - Universal shift register
    - Has both direction shifts & parallel load/out capabilities.

# Universal Shift Register (1/4)

- Capability of a universal shift register:
  1. A clear control to clear the register to 0;
  2. A clock input to synchronize the operations;
  3. A shift-right control to enable the shift right operation and the serial input and output lines associated w/ the shift right;
  4. A shift-left control to enable the shift left operation and the serial input and output lines associated w/ the shift left;
  5. A parallel-load control to enable a parallel transfer and the *n* parallel input lines associated w/ the parallel transfer;
  6. *n* parallel output lines;
  7. A control state that leaves the information in the register unchanged in the presence of the clock;

# Universal Shift Register

| Mode Control | | |
|---|---|---|
| $s_1$ | $s_0$ | Register operation |
| 0 | 0 | No change |
| 0 | 1 | Shift right |
| 1 | 0 | Shift left |
| 1 | 1 | Parallel load |

# Universal Shift Register

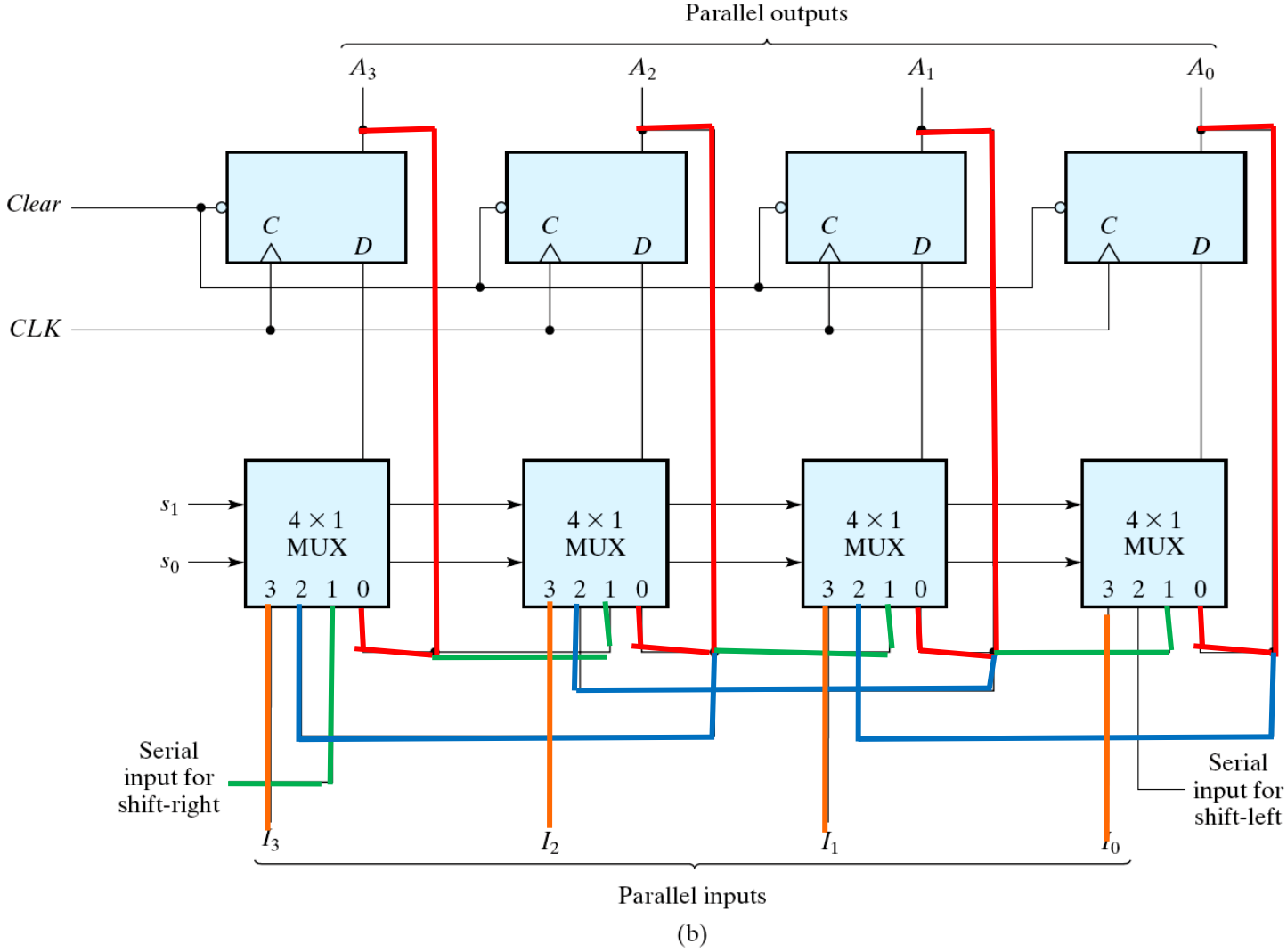
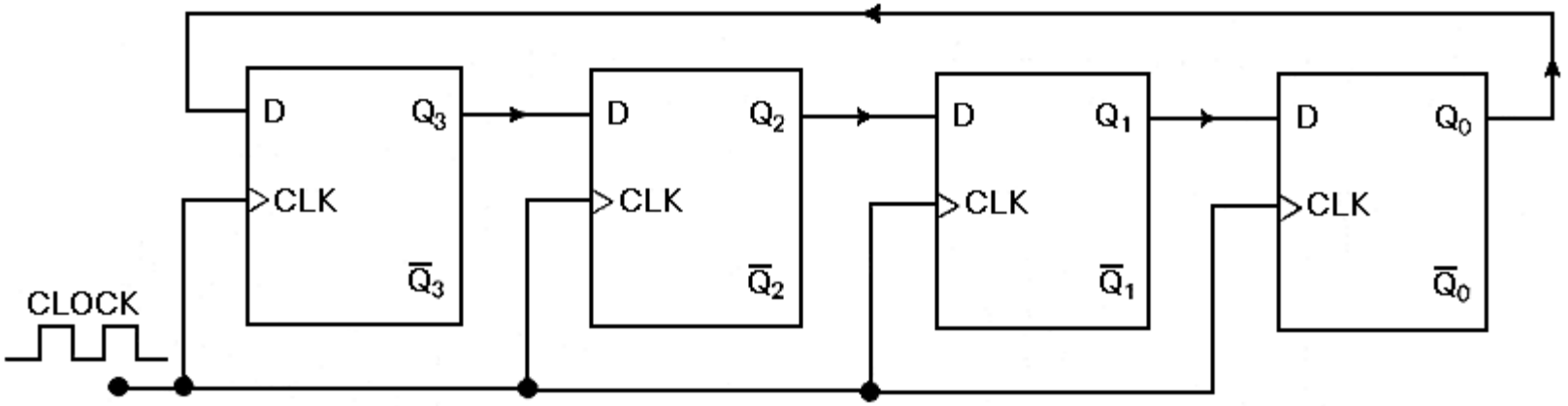
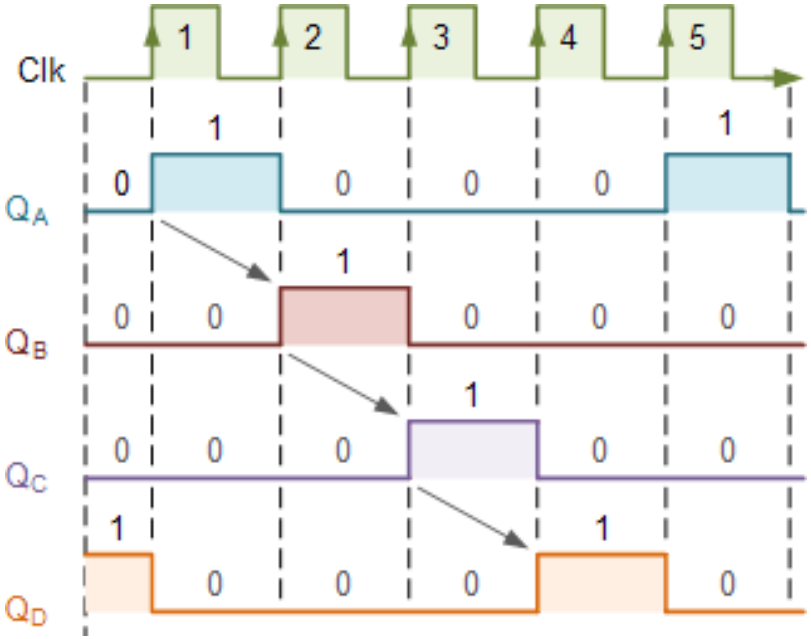



Fig. 6.7 Four-bit universal shift register

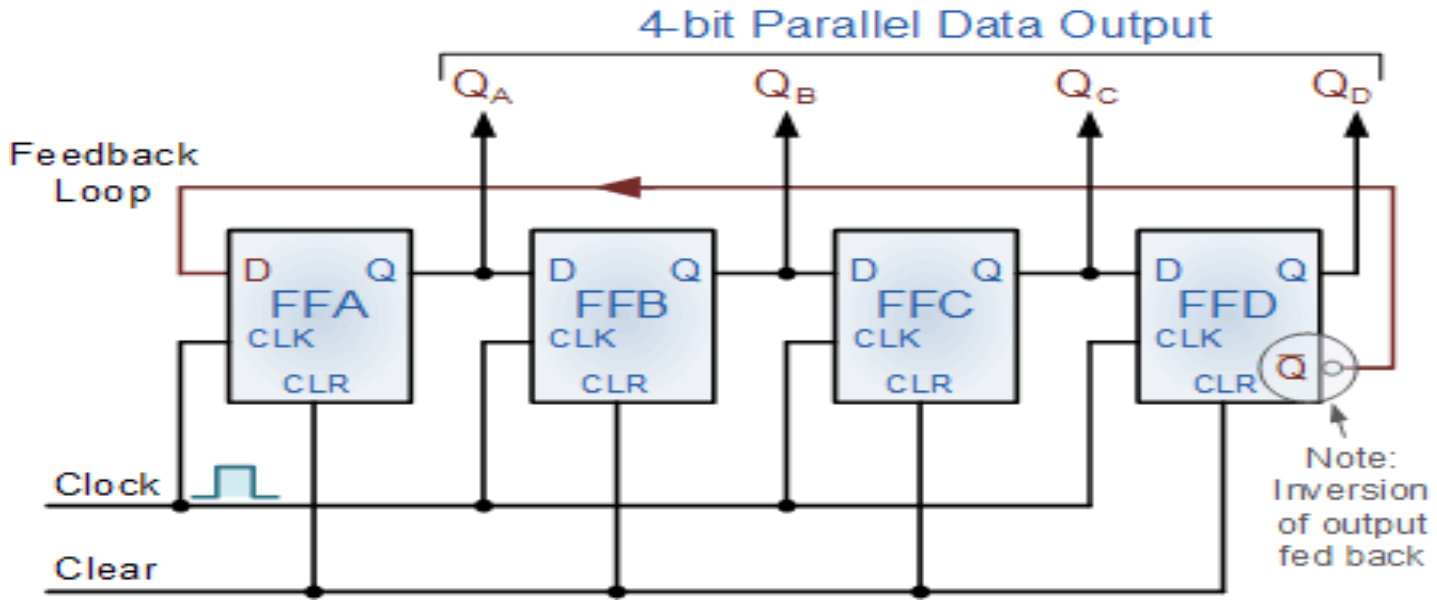
## Ring Counter




RING COUNTERS ARE IMPLEMENTED USING SHIFT REGISTERS. IT IS ESSENTIALLY A CIRCULATING SHIFT REGISTER CONNECTED SO THAT THE LAST FLIP-FLOP SHIFTS ITS VALUE INTO THE FIRST FLIP-FLOP. THERE IS USUALLY ONLY A SINGLE 1 CIRCULATING IN THE REGISTER, AS LONG AS CLOCK PULSES ARE APPLIED. (STARTS 1000->0100->0010->0001 REPEAT)


Clk
1
2
3
4
5
$Q_A$
$Q_B$
$Q_C$
$Q_D$

- Johnson Counter




The Johnson counter, also known as the twisted-ring counter, is exactly the same as the ring counter except that the inverted output of the last flip-flop is connected to the input of the first flip-flop.

**Truth Table for a 4-bit Johnson Ring Counter**

| Clock Pulse No | FFA | FFB | FFC | FFD |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 2 | 1 | 1 | 0 | 0 |
| 3 | 1 | 1 | 1 | 0 |
| 4 | 1 | 1 | 1 | 1 |
| 5 | 0 | 1 | 1 | 1 |
| 6 | 0 | 0 | 1 | 1 |
| 7 | 0 | 0 | 0 | 1 |

As well as counting or rotating data around a continuous loop, ring counters can also be used to detect or recognize various patterns or number values within a set of data. By connecting simple logic gates such as the *AND* or the *OR* gates to the outputs of the flip-flops the circuit can be made to detect a set number or value. Standard 2, 3 or 4-stage Johnson ring counters can also be used to divide the frequency of the clock signal by varying their feedback connections and divide-by-3 or divide-by-5 outputs are also available.

## Sources :


- Digital Logic ,Stephen Brown
- http://www.doc.ic.ac.uk/~nd/surprise_96/journal/vol4/cwl3/report.html#bcd
- http://people.wallawalla.edu/~curt.nelson/engr354/lecture/brown/chapter7_reg_counters.pdf
- http://www.electronics-tutorials.ws