BINARY UP/DOWN COUNTER

UP/DOWN COUNTER

- **Up Counter:** It counts from small to large number.
- **Example:** The 3 bit up counter counts binary form 0 to7 i.e.(000 to 111).
- **Down Counter:** It counts from large to small number.
- **Example:** The 3 bit down counter counts binary from 7-0 i.e.(111-000).
- Design a switch controlled UP/Down Synchronous Counter using JK Flip-flops. For M = 0, it acts as an Up counter and for M =1 as an Down counter.

State Table for 3 bit Up-Down Synchronous Counter:

Control input M	Present State			Next State			Input for Flip-flop					
	Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	0	1	0	X	0	X	1	X
0	0	0	1	0	1	0	0	X	1	X	X	1
0	0	1	0	0	1	1	0	X	X	0	1	X
0	0	1	1	1	0	0	1	X	X	1	X	1
0	1	0	0	1	0	1	X	0	0	X	1	X
0	1	0	1	1	1	0	X	0	1	X	X	1
0	1	1	0	1	1	1	X	0	X	0	1	X
0	1	1	1	0	0	0	X	1	X	1	X	1
1	0	0	0	1	1	1	1	X	1	X	X	1
1	0	0	1	0	0	0	0	X	0	X	1	X
1	0	1	0	0	0	1	0	X	X	1	X	1
1	0	1	1	0	1	0	0	X	X	0	1	X
1	1	0	0	0	1	1	X	1	1	X	X	1
1	1	0	1	1	0	0	X	0	0	X	1	X
1	1	1	0	1	0	1	X	0	X	1	X	1
1	1	1	1	1	1	0	X	0	X	0	1	X

K- map Simplification:

MQC \ QBQA	00	01	11	10
00	1	X	X	1
01	1	X	X	1
11	1	X	X	1
10	1	X	X	1

JA = 1

MQC \ QBQA	00	01	11	10
00	X	1	1	X
01	X	1	1	X
11	X	1	1	X
10	X	1	1	X

KA = 1

MQC \ QBQA	00	01	11	10
00	0	1	X	X
01	0	1	X	X
11	1	0	X	X
10	1	0	X	X

$JB = M\,\overline{QA} + \overline{M}\,QA$

MQC \ QBQA	00	01	11	10
00	X	X	1	0
01	X	X	1	0
11	X	X	0	1
10	X	X	0	1

$KB = M\,\overline{QA} + \overline{M}\,QA$

MQC \ QBQA	00	01	11	10
00	0	0	1	0
01	X	X	X	X
11	X	X	X	X
10	1	X	0	0

$JC = M\,\overline{QA}\,\overline{QB} + \overline{M}\,QA\,QB$

MQC \ QBQA	00	01	11	10
00	X	X	X	X
01	0	0	1	0
11	1	0	0	0
10	X	X	X	X

$KC = \overline{M}\,QA\,QB + M\,\overline{QA}\,\overline{QB}$

Logic Diagram

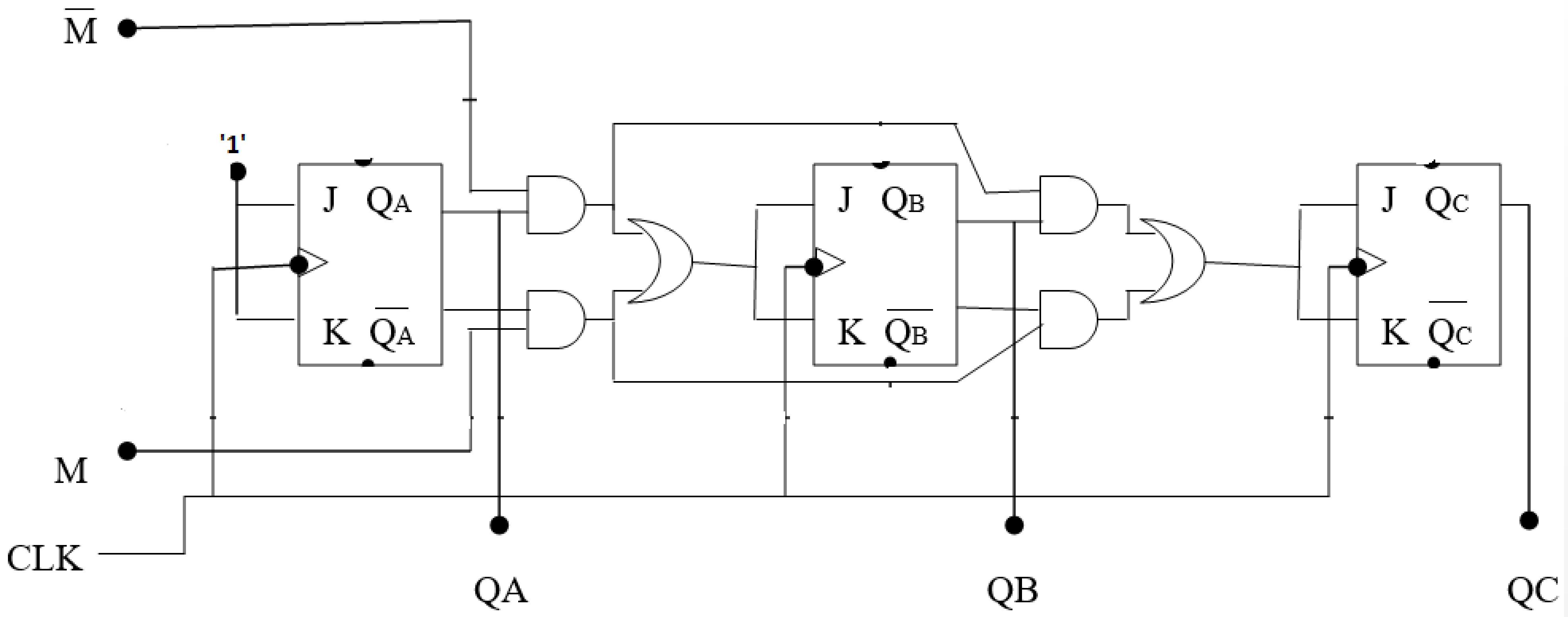


Fig : Logic Diagram of Up down counter using JK Flip Flop

MODULO N COUNTER
(MOD COUNTER)

WHAT IS MODULUS N COUNTER ?

- THE NUMBER OF STATES OR COUNTING SEQUENCES THROUGH WHICH A PARTICULAR COUNTER ADVANCES BEFORE RETURNING ONCE AGAIN BACK TO ITS ORIGINAL FIRST STATE IS CALLED THE MODULUS (MOD). IN OTHER WORDS, THE MODULUS (OR JUST MODULO) IS THE NUMBER OF STATES THE COUNTER COUNTS.
- MOD COUNTERS ARE DEFINED BASED ON THE NUMBER OF STATES THAT THE COUNTER WILL SEQUENCE THROUGH BEFORE RETURNING BACK TO ITS ORIGINAL VALUE

• FOR EXAMPLE, A 2-BIT COUNTER THAT COUNTS FROM 00 TO 11 IN BINARY,HAS A MODULUS VALUE OF 4 (00 → 01 → 10 → 11 , RETURN BACK TO 00) SO WOULD THEREFORE BE CALLED A MODULO-4,. NOTE ALSO THAT IT HAS TAKEN 4 CLOCK PULSES TO GET FROM 00 TO 11.

• THE MAXIMUM NUMBER OF POSSIBLE OUTPUT STATES (MAXIMUM MODULUS) FOR THE COUNTER IS: 2^N • THEREFORE, A “MOD-N” COUNTER WILL REQUIRE “N” NUMBER OF FLIP-FLOPS CONNECTED TOGETHER TO COUNT A SINGLE DATA BIT WHILE PROVIDING 2^N DIFFERENT OUTPUT STATES. A “MOD-N” COUNTER COUNTS FROM 0 TO N-1.

- MODULUS OF A COUNTER INDICATES THE NUMBER OF STATES THROUGH WHICH COUNTER PASSES DURING ITS OPERATION.
- 2-BIT BINARY COUNTER : MOD 4 COUNTER
- 3-BIT BINARY COUNTER: MOD 8 COUNTER
- MOD-N COUNTER IS ALSO CALLED AS MODULO COUNTER.

Example: Design a MOD-6 Ripple Counter using JK FFs.

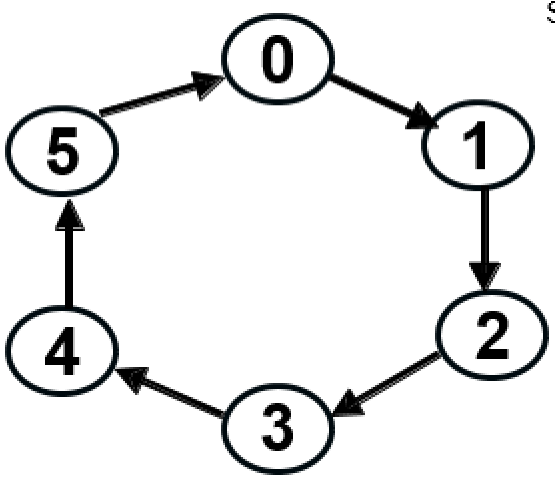
Solution: MOD 6 asynchronous counter will require 3 flip flops and will count from 000 to 101. Rest of the states are invalid.

MOD-6 ripple up-counter

Present St.	Next St.
CBA	CBA
000	001
001	010
010	011
011	100
100	101
101	000(110)

State Table

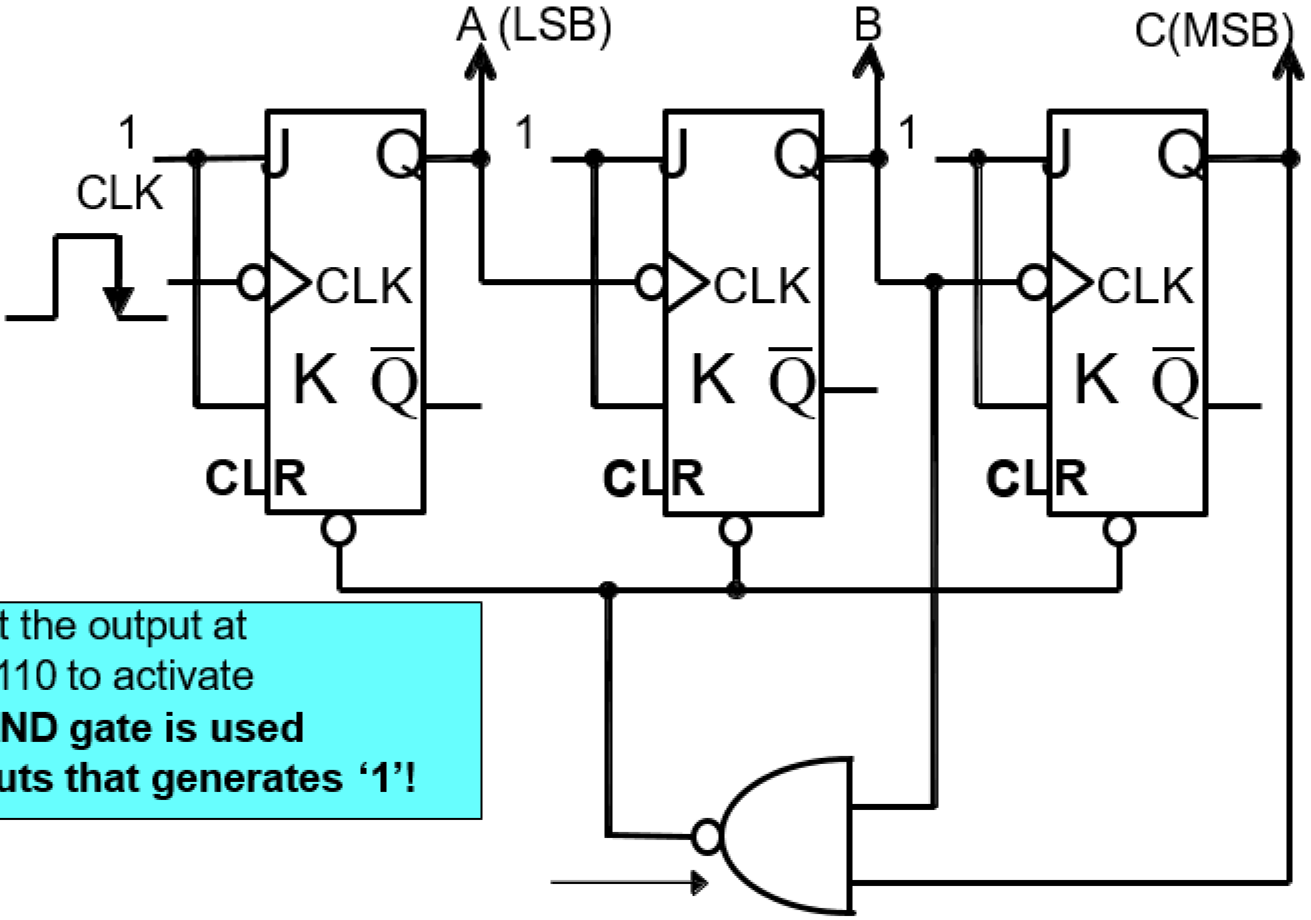
State Diagram



Reset the state to 000_2 when 110_2 is detected

Circuit diagram for MOD-6 ripple counter

Present St.	Next St.
CBA	CBA
000	001
001	010
010	011
011	100
100	101
101	000(110)



Detect the output at CBA=110 to activate CLR. **NAND gate is used to detect outputs that generates ‘1’!**

Self Study

- BCD Ripple counter
- Decade Counter
- MOD 75 Counter using decade counter
- MOD 100 Counter using decade counter