Ahsanullah University of Science and Technology
Bangladesh

COURSE OUTLINE

Part A

1. Course No./Course Code: ***CSE 2105 (BNQF 061)***

2. Course Title: ***Digital Logic Design***

3. **Course Type (GEd/Core Course/Elective):** ***Core Course***

4. Year/Level/Semester/Term: ***Level 2 Term 1***

5. Academic Session: ***Spring 2022***

6. Course Teacher/Instructor: ***Syeda Shabnam Hasan***

7. Pre-requisite(s) (if any): ***Nil***

8. Credit Value: ***3***

9. Credit Hours: ***3***

10. Total Marks: ***100***

11. Rationale of the Course: ***SDG 4 (Ensure Technical Level Education) and SDG 8 (Reduce Unemployment Rate).***

12. Faculty: Engineering

13. Department: Computer Science and Engineering (CSE)

14. Programme: Bachelor of Science in Computer Science and Engineering (B.Sc. in CSE)

15: Course Objectives:

Boolean Algebra: Basic theorems and properties, Boolean Functions and their simplification; Digital Logic Gates; Combinational Logic: Adder, Subtractor, Multiplexer and Demultiplexer, Encoder and Decoder, Comparator; Parity generator and checker; Synchronous Sequential Logic: Flip-Flops, Analysis and Design of sequential circuits; Registers; Synchronous and Asynchronous counters; Basic Memory cell.

16. Mapping of Course Outcomes with Bloom's Taxonomy and Programme Outcomes

Sl. No.	COs	POs	Bloom's Taxonomy		
			C	A	P
1	Explain the basic properties of Boolean algebra to simplify simple Boolean functions, the fundamental number system and error detection codes	1	2		
2	Apply the tabulation and Karnaugh map methods for simplifying combinational and sequential circuits	2	3		
3	Design different combinational and sequential digital logic systems and memory cell	3	3		

17. Mapping of COs with Knowledge Profiles, Complex Engineering Problem Solving and Complex Engineering Activities

Course Outcome	Knowledge Profile	Complex Problem Solving	Complex Engineering Activities
CO1	K4		
CO2	K4		
CO3	K8		

Part B

18. Week-wise Course Plan

Week	Topics	Teaching-Learning Strategy	Assessment Strategy	Corresponding COs
1	Introduction to digital logic (analog and digital signal, advantage of digital signal, logic level), Number System, Basic logic operations, truth tables, logic gates, implementing basic logic operations using NAND and NOR gate, Implementing NOT gate using X-NOR or X-OR gate.	- Lecture	- *Class Performance*	1
2	BCD/8421 code, Excess-3 code,2-4-2-1 code,8,4,-2,-1code,reflected/ gray code, odd/even parity, Boolean Algebra & logic simplification (commutative, associative, distributive law, rules of Boolean algebra, duality principle, de Morgan's theorems, different examples using the rules of Boolean algebra, simplification using Boolean algebra, Boolean function, implementation of Boolean function with gates).	- Lecture	- *Class Performance*	1
3	Standard forms of Boolean expressions (SOP, POS), Canonical forms (minterm, maxterm), determining standard expression from a truth table, Conversion between Canonical forms.	- Lecture -	- *Class Performance* - Quiz 1	1
4	2,3,4,5,6 variable K Maps, K-Map SOP minimization, K-Map POS minimization, don't care condition,	- Lecture - Think – Pair - Share (TPS)	- *Class Performance*	2,3

	Introduction to combinational logic, design procedure of combinational logic, 3-bit square gate, BCD to excess-3 code conversion.			
5	Half adder, full adder, half subtractor, full subtractor, implementation of a full adder using two half adders, binary parallel adder, CLA adder, BCD adder, comparator circuit.	- Lecture - Brain Storming Session - Think – Pair - Share (TPS)	- *Class Performance* - Quiz 2	2, 3
6	Multiplexer (2X1, 4X1, 8X1, 16X1 MUX), Design a 16 X1 MUX using two 8X1 MUXs, Boolean function implementation using MUX, Decoder (3X8,4X16 decoder), design a 4X16 decoder using two 3X8 decoders, Boolean function implementation using decoder, Encoder, Priority encoder, Demultiplexer.	- Lecture - Brain Storming Session - Think – Pair - Share (TPS)	- *Class Performance*	3
7	Sequential logic, sequential circuit, asynchronous and synchronous sequential circuits, Flip-flops (Basic flip-flop circuit, SR, D, JK, T flip-flops, triggering of flip-flops, Master slave flip-flop, excitation table, Conversion of JK flip-flop to T and D flip-flop.	- Lecture - Brain Storming Session - Think – Pair - Share (TPS)	- *Class Performance*	3
	Mid Break			
8	Design procedure of sequential circuit, timing diagram, design of counters (Synchronous counter: 2 bit & 3 bit binary counter, binary up-down counter).	- Lecture	- *Class Performance*	2, 3
9	Ripple counter (binary ripple counter), Random counter (2-3-5-7-2-…	- Lecture	- *Class Performance* - Quiz 3	3

	counter), register, register with parallel load, shift registers, bi-directional shift register with parallel load.			
10	BCD ripple counter, Ring counter, Johnson ring counter, Mod counter.	- Lecture - Brain Storming Session - Think – Pair - Share (TPS)	- *Class Performance*	3
11	problem solving regarding counters.	- Lecture - Brain Storming Session - Think – Pair - Share (TPS)	- *Class Performance*	3
12	Error detection and correction codes, Tabulation Method or Quine-MaCluskey method.	- Lecture	- *Class Performance* - Quiz 4	1, 2
13	Sequence detectors.	- Lecture - Brain Storming Session	- *Class Performance*	3
14	Review classes.			

Part C

19. Assessment and Evaluation

1) Assessment Strategy: ***Class Performance, Quizzes/Assignments, and Final Examination***

2) Marks distribution:

a) Continuous Assessment: ***Class Performance (10), Quizzes/Assignments (20)***

b) Summative: ***Final Examination (70)***

3) Make-up Procedures: ***Carryover/Clearance/Improvement Examination***

Part D

20. Learning Materials

20.1. Required (if any)

1. ***"Digital Design With An Introduction to the Verilog HDL" By M. Morris Mano, Michael D. Ciletti (5th edition).***
2. ***"Digital Fundamentals" By Floyd (11th edition).***
3. ***Course Website – https://classroom.google.com***
   Fall 2022: CSE 2105_Digital Logic Design
   Class Code: dh3pmth

20.2. Recommended (if any)

20.1. Others (if any)

Prepared by:	Checked by:	Approved by:
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Annex-1: PEO of CSE

PEO1 - Professionalism
Graduates will demonstrate sound professionalism in computer science and engineering or related fields.

PEO2 – Continuous Personal Development
Graduates will engage in life-long learning in multi-disciplinary fields for industrial and academic careers.

PEO3 – Sustainable Development
Graduates will promote sustainable development at local and international levels.

Annex-2: Mapping of PEO-PO

	PEO1	PEO2	PEO3
PO1 - Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals and an engineering specialization to the solution of complex engineering problems.	√		
PO2 - Problem analysis: Identify, formulate, research and analyze complex engineering problems and reach substantiated conclusions using the principles of mathematics, the natural sciences and the engineering sciences.	√		
PO3 - Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for public health and safety as well as cultural, societal and environmental concerns.	√		
PO4 – Investigation: Conduct investigations of complex problems, considering design of experiments, analysis and interpretation of data and synthesis of information to provide valid conclusions.	√		
PO5 - Modern tool usage: Create, select and apply appropriate techniques, resources and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.	√		
PO6 - The engineer and society: Apply reasoning informed by contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to professional engineering practice.	√		√
PO7 - Environment and sustainability: Understand the impact of professional engineering solutions in societal and environmental contexts and demonstrate the knowledge of, and need for sustainable development.	√		√
PO8 – Ethics: Apply ethical principles and commit to professional ethics, responsibilities and the norms of engineering practice.	√		

PO9 - Individual work and teamwork: Function effectively as an individual and as a member or leader of diverse teams as well as in multidisciplinary settings.	√	√	
PO10 – Communication: Communicate effectively about complex engineering activities with the engineering community and with society at large. Be able to comprehend and write effective reports, design documentation, make effective presentations and give and receive clear instructions.	√		
PO11 - Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work as a member or a leader of a team to manage projects in multidisciplinary environments.	√		
PO12 - Life-long learning: Recognize the need for and have the preparation and ability to engage in independent, life-long learning in the broadest context of technological change.		√	

Annex-3: Blooms Taxonomy *

Level	Cognitive Domain – Revised Version	Affective Domain	Psychomotor Domain
1	Remember (1)	Receiving Phenomena (1)	Perception (1)
2	Comprehend (2)	Responding to Phenomena (2)	Set (2)
3	Apply (3)	Valuing (3)	Guided Response (3)
4	Analyse (4)	Organizing Values (4)	Mechanism (4)
5	Evaluate (5)	Internalising Values (5)	Complex Overt Response (5)
6	Create (6)		Adaption (6)
			Origination (7)

* Based on "REVISED BLOOM'S TAXONOMY INDICATOR v3.31" , available athttp://adept.mmu.edu.my/wp-content/uploads/2018/09/Blooms-Taxonomy-Indicator-v3.31.xls