"MID 1"

(1) Given, Memory size = $1MB = 2^{20}B$

Block size = 16B

Cache size = $64KB = 2^6 \times 2^{10}B = 2^{16}B$

So, memory address has 20 bits

$\therefore$ Block size $= 2^w \Rightarrow 16 = 2^w \Rightarrow 2^4 = 2^w \therefore w = 4$ bits

Total Line, $m = \frac{64KB}{16B} = \frac{2^{16}B}{2^4B} = 2^{12}B = 4096$

(a) $\therefore m = 2^L \Rightarrow 2^{12} = 2^L \therefore L = 12$ bits

$\therefore$ Tag $= (20 - 4 - 12) = 4$ bits

FA010 =

Tag	Line	Word
1111	1010 0000 0001	0000

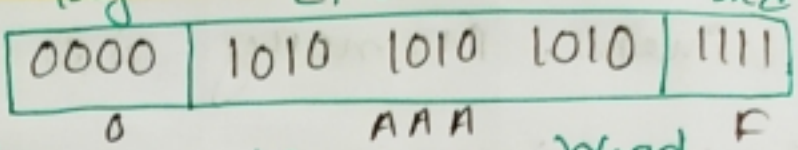
B1234 =

Tag	Line	Word
1011	0001 0010 0011	0100

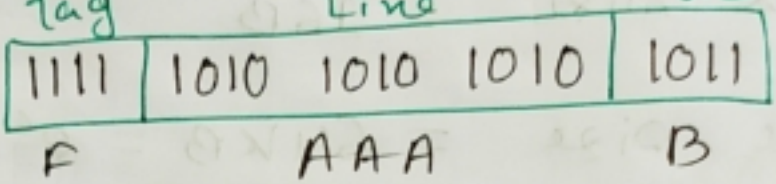
CAB0E =

Tag	Line	Word
1100	1010 1011 0000	1110

(b) Address 1:



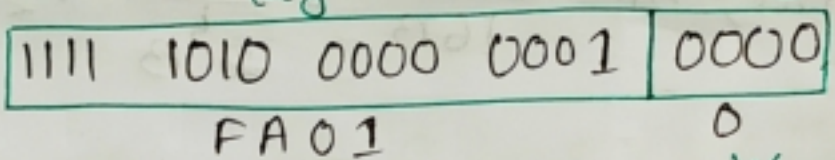
Address 2:



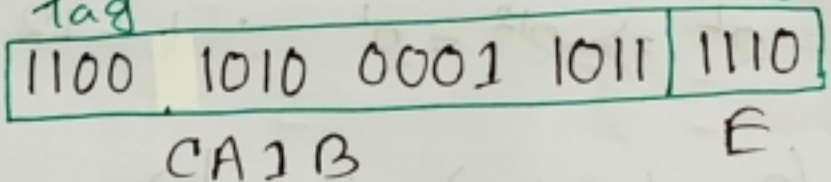
(c) For fully Associative: $w = 4$ bits

$\therefore$ Tag $= (20-4) = 16$ bits

FA010 =



CA1BE =



(d) $K = 2$, $SET = \frac{m}{K} = \frac{4096}{2} = 2048 = 2^{11}$

$w = 4$ bits

So, $2^s = SET \Rightarrow 2^s = 2^{11}$ $\therefore S = 11$ bits

$\therefore$ Tag $= (20-11-4) = 5$ bits

	Tag	Set	Word
FA010:	1 1111	010 0000 0001	0000
	1F	201	0

	Tag	Set	Word
CA1BE:	1 1001	010 0001 1011	1110
	19	21B	E

(2) Given, Memory address = 16 bits

$m = 32$ Line size = 4B

So, Line size $= 2^w \Rightarrow 4 = 2^w \Rightarrow 2^2 = 2^w \therefore w = 2$ bits

$m = 2^L \Rightarrow 32 = 2^L \Rightarrow 2^5 = 2^L \quad \therefore L = 5$ bits

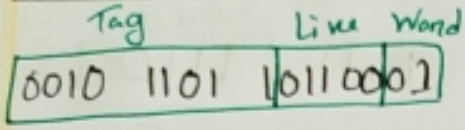
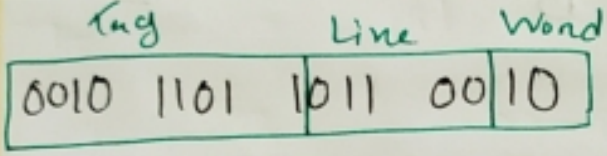
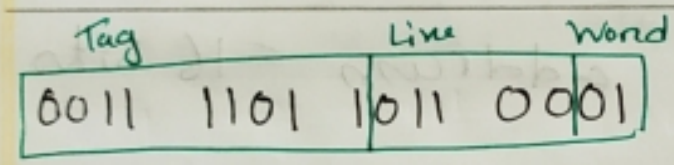
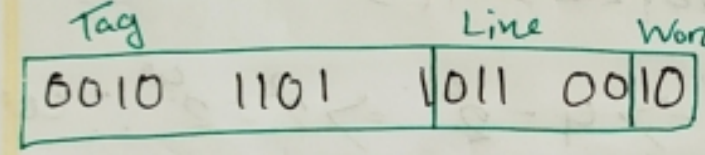
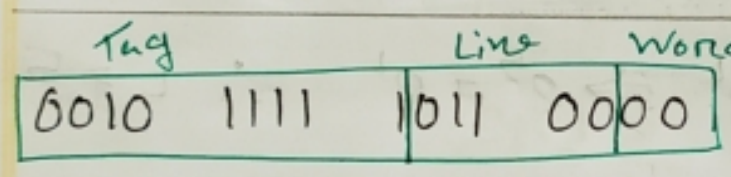
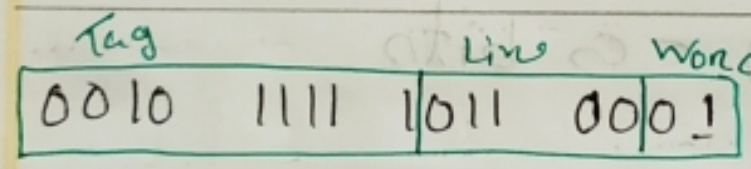
$\therefore$ Tag $= (16 - 2 - 5) = 9$ bits

(ii)

$$\therefore \text{Ratio} = \frac{32 \times 4 \times 8}{(32 \times 4 \times 8) + (32 \times 9)}$$

$$= \frac{1024}{1312} = 0.78 \text{ Ans}$$

iii)

Memory Address	Hit / Miss
	Cache Miss
	Cache Hit
	Cache Miss
	Cache Miss
	Cache Miss
	Cache Hit

$$\therefore \text{Hit ratio} = \frac{\text{Instruction/data read from cache}}{\text{Total accessed address}}$$

$$= \frac{2}{6} \times 100 = 33.33\%$$ Ans

(3) $m = 16$, line size $= 8B$

Address	Block # = quotient (address / Block size)	Hit / Miss	Consequences
20	$\frac{20}{8} = 2$	Miss	Block-2 is transferred in a free line of cache, say line-1.
21-23	2	Hit (3 Addresses)	CPU reads from cache.
24	3	Miss	Block-3 is transferred in a free line of cache, say line-2
25-31	3	Hit (7 addresses)	CPU reads from cache.
32	4	Miss	Block-4 is transferred in a free line of cache, say line-3
33-39	4	Hit (7 addresses)	CPU reads from cache.
40	5	Miss	Block-5 is transferred in a free line of cache, say line-4
41-45	5	Hit (5 Addresses)	CPU reads from cache.
28-31	3	Hit (4 Addresses)	CPU reads from cache.
32-39	4	Hit (8) addresses	CPU reads from cache
40-45	5	Hit (6 Addresses)	CPU reads from cache
26-31	3	Hit (4)	CPU reads from cache
32-39	4	Hit (8)	CPU reads from cache
40-45	5	Hit (6)	CPU reads from cache

Here, total scanned Address = 62

total instruction/data read from cache = 58

$\therefore$ Hit ratio $= \frac{58}{62} \times 100 = 93.54\%$ Ans

Here, No blocks were replaced.

(4) Cache size = 64KB = $64 \times 2^{10} = 2^6 \times 2^{10} = 2^{16}$B

K = 4, line size = 32B

$\therefore m = \frac{2^{16}B}{32B} = 2048$

$\therefore SET = \frac{m}{K} = \frac{2048}{4} = 512$

We know, S = j MOD SET

if	j = 5	then	S = 5
	j = 517		S = 5
	j = 1029		S = 5
	j = 1541		S = 5
	j = 2043		S = 5

So, block addresses 5, 517, 1029, 1541, 2043 are mapped to set number 5.