NORTH SOUTH UNIVERSITY

Department of Electrical & Computer Engineering

LAB REPORT

Course Name: Computer Organization & Architecture

Course Code: CSE332L

Experiment Number: 04

Experiment Name: Design of a 4-bit Binary Up-Down counter.

Submitted By

Name: MD. ABU AMMAR

Id: 1821944642

Section: 05

Submitted To

Instructor: Md. Saidur Rahman

Experiment Date: 05-12-2020	Submission Date: 06-12-2020

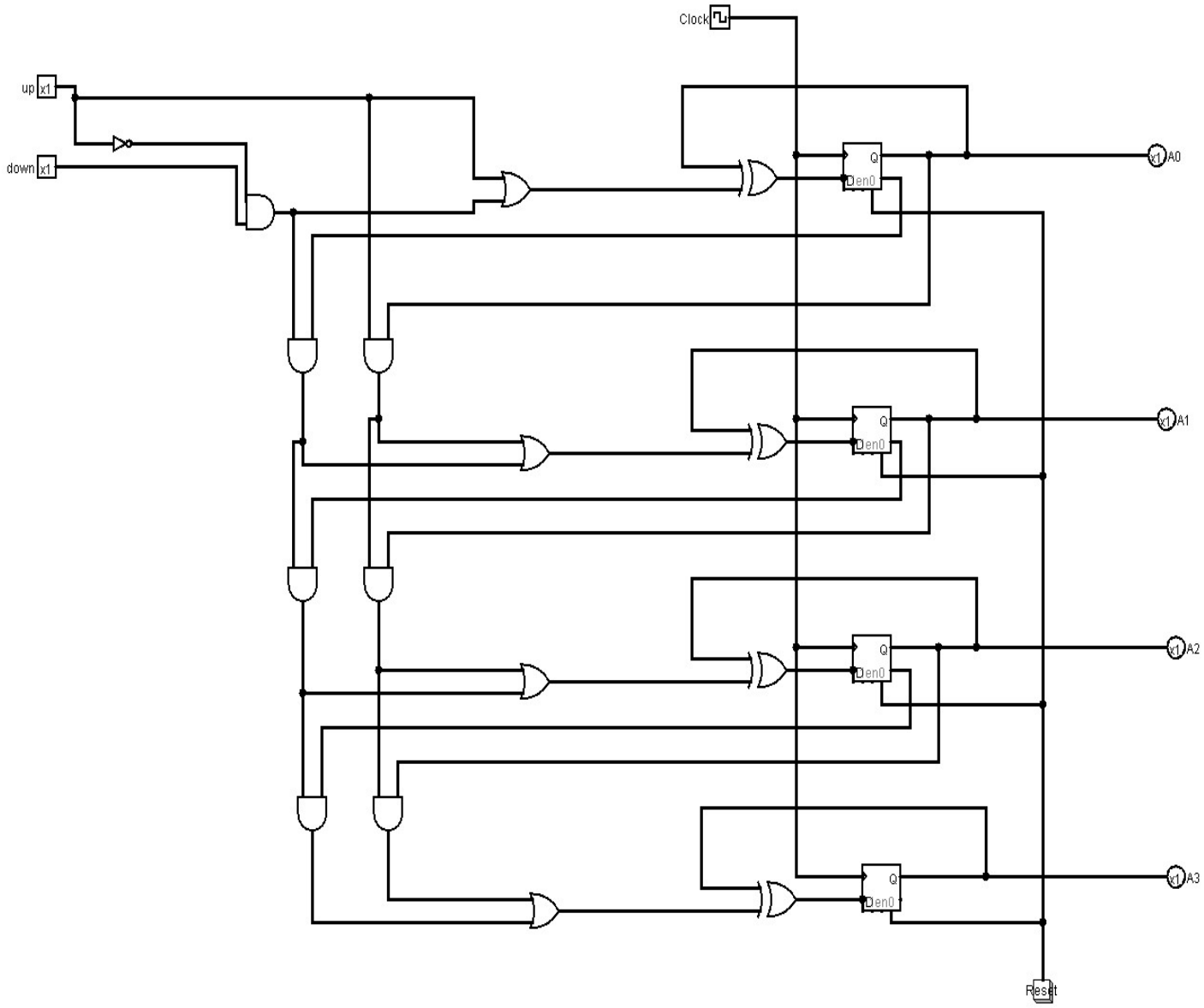
Experiment Name:

Design of a 4-bit Binary Up-Down counter.

Objectives:

- Learn how to design a -bit Binary Up-Down counter.
- Learn the difference between asynchronous and synchronous counter.
- Learn to implement a T flipflop using a D flipflop and a XOR gate.

Circuit Diagram:



Truth Table:

For Up Counter:

Clock Pulse	A3	A2	A1	A0
P0	0	0	0	0
P1	0	0	0	1
P2	0	0	1	0
P3	0	0	1	1
P4	0	1	0	0
P5	0	1	0	1
P6	0	1	1	0
P7	0	1	1	1
P8	1	0	0	0
P9	1	0	0	1
P10	1	0	1	0
P11	1	0	1	1
P12	1	1	0	0
P13	1	1	0	1
P14	1	1	1	0
P15	1	1	1	1

For Down Counter:

Clock Pulse	A3	A2	A1	A0
P0	1	1	1	1
P1	1	1	1	0
P2	1	1	0	1
P3	1	1	0	0
P4	1	0	1	1
P5	1	0	1	0
P6	1	0	0	1
P7	1	0	0	0
P8	0	1	1	1
P9	0	1	1	0
P10	0	1	0	1
P11	0	1	0	0
P12	0	0	1	1
P13	0	0	1	0
P14	0	0	0	1
P15	0	0	0	0

Discussion:

After completing the lab, we got a clear idea to build a 4-bit Binary Up-Down counter and get the clear conception of its function. In the lab we built a 4-bit up down counter where up counter count initially from 0 to 15 and down counter count initially from 15 to 0. By up and down input, we select the operation such as for 00 the operation is No Change, for 01 operation is Down Counter, for 10 and 11 the operation is Up Counter.

During this experiment we faced two interesting questions. Describing those questions below.

The first question came on our mind that is, when up and down is on why only up counter is working. The reason of up counter is working while both up and down pin is on is that the left side's AND gates are always off when Up and Down bit both are on or only Up bit is on, as the down the counter is activated only when any of the left side's 4 AND gates is active so when we put up = 1 the NOT gate convert it to 0 and it goes to the first input of 1st left AND gate and the output comes 0 so the 3 other left AND gates are also off during this time but right side's 3 AND gate working simultaneously at the same time which is the reason of Up Counter being activated.

Now the 2nd question came on our mind, In Up counter after 1111 why and how 0000 comes in output and in Down Counter after 0000 why and how 1111 comes in output.

- For Up Counter: In Up counter we count towards forward as our limit is 4-bit it means we can only count from 0 to maximum 15 , so after 15 we will restart the count from 0 that's why after 1111 = 15 the next output is 0000 = 0, but how this thing works in the circuit, we will unfold this now. If we see all the XOR gate's input after getting 1111 is in the output, we can clearly see that 2 inputs of each XOR gates are 1 or we can say same and the output of all XOR gate will be 0 as per the XOR gate's truth table, so after the next clock cycle this zeros will be updated in four D flipflops so basically we will get 0000 in the final output.

- For Down Counter: In Down counter we count towards backward as our limit is 4-bit we can only count from 15 to 0 in backward direction , so after 0 we will restart the count from 15 that's why after 0000 = 0 the next output is 1111 = 15, but how this thing works in the circuit, we will unfold this now. If we see all the XOR gate's input after getting 0000 is in the output, we can clearly see that 2 inputs of each XOR gates are 0 and 1 or we can say both are different and the output of all XOR gate will be 1 as per the XOR gate's truth table, so after the next clock cycle these 1 will be updated in four D flipflops so basically we will get 1111 in the final output.

As the global pandemic still going on, we are conducting online classes so all the experiments are doing in online using the desired software so there is no scope of getting error or any obstacle to do the experiment which we used to get in the physical lab classes. So, we get all the output accurately and finished the experiment without any problem.