Ano. to the Question NO.1"
011100t0 DATOMME ONOS
+11000011
11100110101
avry: Three in a carry in the result.
So, carry flag = 1  Pero: Result #0, So Rero flag = 0
Reput #0, So Rero flug =01
Even Parity: Result contains even number 1 So, Even parity plag = 1
So, Even parity thang =1
Sign: Result is positive. So, sign
Half-Corny: There was no covery from with bit
So, Half-carry flag = 00099 and

PART DISPLACEMENT. 2, P2

HAO . WA

Am. to the Quentlon No. 2"

$$6 = 0110$$
,  $5 = 0101$  And  $8 \times 14118$ 

$$1' = 1010$$

$$1' = 1011 = -5$$

	0/	moulos	have bear		
	A	a	Q-1	M	initial values
	0000	1011	DOW	01109	
	1010	1011	lordo b.	0110	A - A-M & First
	1101	0101		0110	Shift ) Cycle
	1110	1010	as steel	0110	Shift } Second
	0100	1010		0110	A = A+m > Third
	0010	0101	0	0110	A = A+m ? Phind Shift } cycle
		0101		0110	A = A-M ) Fourth
The second second	1110	0010	Decoduc !	6110	Shift Gyde
The state of the s	1110	0010	Decodur !	6110	Shift Jegele

Nampel

world A

100100111

(a) LOAD IMMEDIATE 20H 110000114

Amo: 20 H

6 LOAD DIRECT 20H

Am: 24 H

[] = 13019 | From 1 00 @ LOAD INDIRECT 20H

is no i Repult +0, so here they Ams: 21 H

@ LOAD INOIRECT 24H Sus Even points than

Am: 25H

eniting and in ponitive. e LOAD R1

Am: 23 Ho P LOAD REGISTER INDIRECT RI So, Haff-coord

Am: 2BH

(9) LOAD DISPLACEMENT 2, R2

Amo: 2AH

LOAD DISPLACEMENT 2, P] Am: 23H

Am. to the Question No. 4" 69M x8 bits 20 x 26 = 226 :Address line for now and column =  $\frac{26}{2}$ PASIGAS WE OF 1131 Timing and Contral organized cos 8 Defresh square arrays of Counter 8102 by 8102 elemends M Memony Address Albuno 1 ( Row 8192×8102 Address Buffer Column Data Imput Address Bullen Refrush Buffen cinevitay Data output Column Buffen Decoder

to write to a memory cell, the now and column address for the cell must be selected and data must be presented. The data input pins. The presented the data input pins. The chip's on-bouted logic either charges the memory cell's capaciton on discharges it, depending on whether a 1 or 0 is to be storted:

- The now address must be applied to the address input pin on the memory device for the prescribed amount of time before RAS goes low and be held for a period of time.
- @ FAS must go from ligy to low.
- 6 A column address must be applied to the address input pins on the

memony device fon the prescrible amount of time often RAS goes low and before CAS goes low and fuld for the prescribed time 9 WE munt be net low for a centain time for a write operation to occur. Rue timing of the transitions are determined by CAS going low. (5) Data mont be applied to the data input pin the prescribed amount of time before CAS goes low and held. 6 CAS mont switch from high, to low. Before the write cycle can be comidured complete. CAS and PAS most return to their inactive states. to - fla