Sample Questions
CSE-332/ Fall2020

1. Consider two different implementations of the same instruction set architecture. There are four classes of instructions, A, B, C, and D. The clock rate and CPI of each implementation are given in the following table.
2.

	CLOCK RATE	CPI class A	CPI class B	CPI class C	CPI class D
P1	2.5 GHz	1	2	3	3
P2	3 GHz	2	2	2	2

   a) Given a program with 106 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?
   b) What is the global CPI for each implementation?
   c) Find the clock cycles required in both cases.

3. The following table shows the number of instructions for a program.

	ARITH	STORE	LOAD	BRANCH	TOTAL
A.	650	100	600	50	1400
B.	750	250	500	500	2000

   a) Assuming that arith instructions take 1 cycle, load and store 5 cycles, and branches 2 cycles, what is the execution time of the program in a 2 GHz processor?
   b) Find the CPI for the program.
   c) If the number of load instructions can be reduced by one half, what is the speedup and the CPI?

4. A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count:

INSTRUCTION TYPE	INSTRUCTION COUNT IN MILLIONS	CYCLES PER INSTRUCTIONS
ARITHMETIC	45000	1
DATA TRANSFER	32000	2
FLOATING POINT	15000	2
CONTROL TRANSFER	8000	2

Determine the effective CPI, MIPS rate, and execution time for this program.

5. Consider two different machines, with two different instruction sets, both of which have a clock rate of 200 MHz. The following measurements are recorded on the two machines running a given set of benchmark programs:

MACHINE - A	INSTRUCTION TYPE	INSTRUCTION COUNT	CYCLES PER INSTRUCTIONS
	ARITHMETIC	8	1
	LOAD and STORE	4	3
	BRANCH	2	4
	OTHERS	4	3

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MACHINE - B	INSTRUCTION TYPE	INSTRUCTION COUNT	CYCLES PER INSTRUCTIONS
	ARITHMETIC	10	1
	LOAD and STORE	8	2
	BRANCH	2	4
	OTHERS	4	3

Determine the effective CPI, MIPS rate, and execution time for each machine.

6. Assuming the following assembly instructions are executed in the order that they are found in the table below, fill out the chart indicating the stage of the standard 5-stage pipeline that the instruction will be in during the clock cycles. If an instruction is not in any stage during a cycle, simply leave that box blank. Indicate the stages of the pipeline using: IF, ID, MEM, EX, and WR. If there is gap in stages due to a data hazard, make sure to indicate the data hazard using d*.

Instruction\ cycle	1	2	3	4	5	6	7	8	9
ADD R10, R2, R3									
SUB R4, R1, R5									
AND R6, R4, R7									
OR R8, R12, R9									
XOR R10, R1, R11									

7. Assume a machine using Five-stage pipelining runs a program. Instruction-3 is a conditional branch instruction. If the condition is TRUE, CPU skips next three instructions. Instruction-8 is also a conditional branch instruction and if it is FALSE, program control returns to Instruction-4. Show the time steps of pipelining stages assuming that both Instructions 3 and 8 are evaluated evaluated TRUE.

Instructions	Time Steps																
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

8.

Consider two different machines, with two different instruction sets, using two compilers runs a program having following distribution of instructions.

Instruction Type	Machine-A (Clock rate 250MHz)		Machine-B (Clock rate 300MHz)	
	Instruction Count in Millions	CPI	Instruction Count in Millions	CPI
ARITHMETIC	8	1	7	1
LOAD	6	5	8	4
BRANCH	2	4	2	5
STORE	4	2	3	3

Determine the effective CPI, MIPS rate, and execution time for each machine. Do MIPS ratings reflect the true relative performances of Machines A & B, justify your answer with reference to other values and performance measures.

9. A computer M_2 has the following CPIs for instruction types A thru D, and a program P_3 has the following mix of instructions.

   M_2: Type A $CPI_A = 1.7$ Type B $CPI_B = 2.1$ Type C $CPI_C = 2.7$ Type D $CPI_D = 2.4$

   P_3: Type A = 22% Type B = 29% Type C = 17% Type D = remaining %

   a) Calculate the average CPI of Machine M_2

   b) Calculate the runtime of P_3 on M_2 if IC = 22,311 and clock rate is 3.3 GHz

10. You are on the design team for a new processor. The clock of the processor runs at 200 MHz. The following table gives instruction frequencies for Benchmark program, as well as how many cycles the instructions take, for the different classes of instructions. For this problem, we assume that (unlike many of today's computers) the processor only executes one instruction at a time.

Instruction Type	Frequency	CPI
Loads & Stores	30%	6
Arithmetic Instructions	50%	4
All Others	20%	3

   a) Calculate the CPI for Benchmark program.

   b) What is the MIPS rating of the processor speed?

   c) The hardware expert says that if you double the number of registers, the cycle time must be increased by 20%. What would the new clock speed be (in MHz)?

   d) The compiler expert says that if you double the number of registers, then the compiler will generate code that requires only half the number of Loads & Stores. What would the new CPI be on the benchmark?

e) How many CPU seconds will the benchmark take if we double the number of registers (taking into account both changes described above)?

Solution

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Assignment# 1

CSE-332/Summer 2020 (Due date: Friday, July 31, 6pm)

11. Consider two different implementations of the same instruction set architecture. There are four classes of instructions, A, B, C, and D. The clock rate and CPI of each implementation are given in the following table.
12.

	CLOCK RATE	CPI class A	CPI class B	CPI class C	CPI class D
P1	2.5 GHz	1	2	3	3
P2	3 GHz	2	2	2	2

d) Given a program with 106 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?

e) What is the global CPI for each implementation?

f) Find the clock cycles required in both cases.

Solution:

Class A: 10%

Class B: 20%

Class C: 50%

Class D: 20%

For P1: CPI = 0.1× 1+ 0.2× 2 + 0.5 × 3 + 0.2 × 3 = 2.6

Execution Time: $106 \times 2.6 \times (1/2.5 \times 10^9)$ second = $275.6 \times 0.4 \times 10^{-9}$ sec = 110.24×10^{-9} sec

Clock cycles: 2.6 × 106 = 275.6

For P2: CPI = 0.1× 2+ 0.2× 2 + 0.5 × 2 + 0.2 × 2 = 2.0

Execution Time: $106 \times 2.0 \times (1/3 \times 10^9)$ second = $212 \times 0.33 \times 10^{-9}$ sec = 69.96×10^{-9} sec

Clock cycles: 2.0× 106 = 212

a) P2 implementation is faster
b) For P1: Global CPI = 2.6
   For P2: Global CPI = 2.0
c) For P1: Clock cycles: 275.6
   For P2: Clock cycles: 212

13. The following table shows the number of instructions for a program.

	ARITH	STORE	LOAD	BRANCH	TOTAL
A.	650	100	600	50	1400
B.	750	250	500	500	2000

d) Assuming that arith instructions take 1 cycle, load and store 5 cycles, and branches 2 cycles, what is the execution time of the program in a 2 GHz processor?
e) Find the CPI for the program.
f) If the number of load instructions can be reduced by one half, what is the speedup and the CPI?

Solution:

	ARITH	STORE	LOAD	BRANCH	TOTAL
A.	650	100	600	50	1400
B.	750	250	500	500	2000

	CPI=1	CPI=5	CPI=5	CPI=2	

For A:

Average CPI for A: $(650 \times 1 + 100 \times 5 + 600 \times 5 + 50 \times 2)/1400 = 4200/1400 = 3$

Execution time for A: $1400 \times 3 \times 1/(2 \times 10^9) = 4200 \times 0.5 \times 10^{-9}$ sec = 2100 ns

If the number of load instructions can be reduced by one half,

Average CPI for A: $(650 \times 1 + 100 \times 5 + 300 \times 5 + 50 \times 2)/1400 = 2700/1100 = 2.45$

Speed up = $(1400 \times 3 \times 1/(2 \times 10^9))/ (1100 \times 2.45 \times 1/(2 \times 10^9)) = 4200/2695 = 1.55$

For B:

Average CPI for B: $(750 \times 1 + 250 \times 5 + 500 \times 5 + 500 \times 2)/2000 = 5500/2000 = 2.75$

Execution time for A: $2000 \times 2.75 \times 1/(2 \times 10^9) = 2750$ ns

If the number of load instructions can be reduced by one half,

Average CPI for B: $(750 \times 1 + 250 \times 5 + 250 \times 5 + 500 \times 2)/1750 = 4250/1750 = 2.42$

Speed up = $(2000 \times 2.75 \times 1/(2 \times 10^9))/ (1750 \times 2.42 \times 1/(2 \times 10^9)) = 5500/4235 = 1.30$

14. A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count:

INSTRUCTION TYPE	INSTRUCTION COUNT IN MILLIONS	CYCLES PER INSTRUCTIONS
ARITHMETIC	45000	1
DATA TRANSFER	32000	2
FLOATING POINT	15000	2
CONTROL TRANSFER	8000	2

Determine the effective CPI, MIPS rate, and execution time for this program.

Solution:

CPI = $(45000 \times 1 + 32000 \times 2 + 15000 \times 2 + 8000 \times 2)/100000 = 1.55$

Execution time = $100000 \times 1.55 \times (1/40 \times 10^6) = 0.003875$ sec = 3.875 ms

MIPS = $(100000 \times 40 \times 10^6)/(100000 \times 1.55 \times 10^6) = 25.80$

15. Consider two different machines, with two different instruction sets, both of which have a clock rate of 200 MHz. The following measurements are recorded on the two machines running a given set of benchmark programs:

MACHINE - A	INSTRUCTION TYPE	INSTRUCTION COUNT	CYCLES PER INSTRUCTIONS
	ARITHMETIC	8	1
	LOAD and STORE	4	3
	BRANCH	2	4
	OTHERS	4	3

.....

MACHINE - B	INSTRUCTION TYPE	INSTRUCTION COUNT	CYCLES PER INSTRUCTIONS
	ARITHMETIC	10	1
	LOAD and STORE	8	2
	BRANCH	2	4
	OTHERS	4	3

Determine the effective CPI, MIPS rate, and execution time for each machine.

Machine-A

Effective CPI: $(8\times1+4\times3+2\times4+4\times3)/18 = 40/18 = 2.22$

Execution time: $18 \times 2.22 \times (1/200 \times 10^6) = 0.198 \times 10^{-6}$ sec

MIPS = $f /(CPI \times 10^6) = (200 \times 10^6)/(2.22 \times 10^6) = 90.09$

Machine-B

Effective CPI: $(10\times1+8\times2+2\times4+4\times3)/18 = 46/24 = 1.92$

Execution time: $24 \times 1.92 \times (1/200 \times 10^6) = 0.23 \times 10^{-6}$ sec

MIPS = $f /(CPI \times 10^6) = (200 \times 10^6)/(1.92 \times 10^6) = 104.16$

16. Assuming the following assembly instructions are executed in the order that they are found in the table below, fill out the chart indicating the stage of the standard 5-stage pipeline that the instruction

will be in during the clock cycles. If an instruction is not in any stage during a cycle, simply leave that box blank. Indicate the stages of the pipeline using: IF, ID, MEM, EX, and WR. If there is gap in stages due to a data hazard, make sure to indicate the data hazard using d*.

Solution:

Instruction\ cycle	1	2	3	4	5	6	7	8	9
ADD R10, R2, R3	IF	ID	MEM	EX	WR				
SUB R4, R1, R5		IF	ID	MEM	EX	WR			
AND R6, R4, R7			IF	ID	MEM	d*	EX	WR	
OR R8, R12, R9				IF	ID		MEM	EX	WR
XOR R10, R1, R11					IF		ID	MEM	EX

Note: Sum of R1 and R5 must be stored in R4 first (instruction: SUB R4, R1, R5) and then the updated value of R4 can be used in following instruction (instruction: AND R6, R4, R7). So there will be a data hazard marked by d*. As a result, following instructions will be delayed by one time step.

17. Assume a machine using Five-stage pipelining runs a program. Instruction-3 is a conditional branch instruction. If the condition is TRUE, CPU skips next three instructions. Instruction-8 is also a conditional branch instruction and if it is FALSE, program control returns to Instruction-4. Show the time steps of pipelining stages assuming that both Instructions 3 and 8 are evaluated evaluated TRUE.

Instructions	**Time Steps**																
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**
Inst-1	IF	ID	MEM	EX	WR												
Inst-2		IF	ID	MEM	EX	WR											
Inst-3			IF	ID	MEM	EX	WR										

Inst-4				IF	ID	MEM	cleared											
Inst-5					IF	ID												
Inst-6						IF												
Inst-7							IF	ID	MEM	EX	WR							
Inst-8								IF	ID	MEM	EX	WR						
Inst-9									IF	ID	MEM	EX	WR					
Inst-10										IF	ID	MEM	EX					
Inst-11											IF	ID	MEM					
Inst-12												IF	ID					
Inst-13													IF					

18.

Consider two different machines, with two different instruction sets, using two compilers runs a program having following distribution of instructions.

Instruction Type	Machine-A (Clock rate 250MHz)		Machine-B (Clock rate 300MHz)	
	Instruction Count in Millions	CPI	Instruction Count in Millions	CPI
ARITHMETIC	8	1	7	1
LOAD	6	5	8	4
BRANCH	2	4	2	5
STORE	4	2	3	3

Determine the effective CPI, MIPS rate, and execution time for each machine. Do MIPS ratings reflect the true relative performances of Machines A & B, justify your answer with reference to other values and performance measures.

Solution:

Machine-A

Effective CPI: $(8\times1+6\times5+2\times4+4\times2)/20 = 54/20 = 2.7$

Execution time: $20 \times10^6\times 2.7 \times (1/250 \times 10^6) = 0.216$ sec

MIPS = $f /(CPI \times 10^6) = (250 \times 10^6)/(2.7 \times 10^6) = 92.59$

Machine-B

Effective CPI: $(7\times1+8\times4+2\times5+3\times3)/20 = 58/20 = 2.9$

Execution time: $20 \times10^6\times 2.9 \times (1/300 \times 10^6) = 0.193$ sec

MIPS = $f /(CPI \times 10^6) = (300 \times 10^6)/(2.9 \times 10^6) = 103.44$

Here, MIPS ratings reflect the true relative performances of Machines A & B. Machine-B is faster since execution time is lower.

19. A computer M_2 has the following CPIs for instruction types A thru D, and a program P_3 has the following mix of instructions.

M_2: Type A $CPI_A = 1.7$ Type B $CPI_B = 2.1$ Type C $CPI_C = 2.7$ Type D $CPI_D = 2.4$

P_3: Type A = 22% Type B = 29% Type C = 17% Type D = remaining %

c) Calculate the average CPI of Machine M_2

d) Calculate the runtime of P_3 on M_2 if IC = 22,311 and clock rate is 3.3 GHz

Solution:

a) Average CPI: $0.22 \times 1.7 + 0.29 \times 2.1 + 0.17 \times 2.7 + 0.32 \times 2.4 = 0.374 + 0.609 + 0.459 + 0.768 = 2.21$

b) Run time: $22311 \times 2.21 \times (1/3.3 \times 10^9) = 14.94 \times 10^{-6}$ sec

20. You are on the design team for a new processor. The clock of the processor runs at 200 MHz. The following table gives instruction frequencies for Benchmark program, as well as how many cycles the instructions take, for the different classes of instructions. For this problem, we assume that (unlike many of today's computers) the processor only executes one instruction at a time.

Instruction Type	Frequency	CPI
Loads & Stores	30%	6
Arithmetic Instructions	50%	4
All Others	20%	3

f) Calculate the CPI for Benchmark program.

g) What is the MIPS rating of the processor speed?

h) The hardware expert says that if you double the number of registers, the cycle time must be increased by 20%. What would the new clock speed be (in MHz)?

i) The compiler expert says that if you double the number of registers, then the compiler will generate code that requires only half the number of Loads & Stores. What would the new CPI be on the benchmark?

j) How many CPU seconds will the benchmark take if we double the number of registers (taking into account both changes described above)?

Solution:

a) CPI: $0.3 \times 6 + 0.5 \times 4 + 0.2 \times 3 = 4.4$

b) MIPS = $(200 \times 10^6)/(4.4 \times 10^6) = 45.45$

c) Old Cycle time : $1/(200 \times 10^6) = 0.005 \times 10^{-6}$sec

New Cycle time: 0.005×10^{-6}sec + 0.001×10^{-6}sec = 0.006×10^{-6}sec

New clock speed, f = $1/(0.006 \times 10^{-6}\text{sec})$ Hz = 166.66×10^6 Hz = 166.66 MHz

d) Let us assume that, initially total number of instructions was = 100 (Loads & Stores = 30, Arithmetic = 50 and Others = 20).

Half the number of Loads & Stores = 30/2 = 15

New CPI: $(15 \times 6 + 50 \times 4 + 20 \times 3)/85 = (90+200+60)/85 = 350/85 = 4.11$

e) Taking c (New clock speed = 166.66 MHz and d (New CPI = 4.11) into consideration,

Execution time: $85 \times 4.11 \times 1/(166.66 \times 10^6)$ sec $= 2.10 \times 10^{-6}$ sec

More questions:

1. A program containing 2 Million instructions with the following instruction mix is run on a RISC machine having following CPI values:

Op	Freq	CPI
ALU	20%	2
Load	40%	6
Store	30%	5
Branch	10%	2

If the CPU runs at 200MHz, calculate the execution time of the program.

If a CPU design enhancement reduces the CPI of Load and Store instructions by 2 and 3 respectively. Calculate the resulting performance improvement from this enhancement using Amdahl's law. Also calculate the execution time with enhancement.

2. The following table shows the execution time of five routines of a program running on different numbers of processors.

No of Processor	Routine-A	Routine-B	Routine-C	Routine-D	Routine-E
16	4ms	14ms	2ms	12ms	2ms

Find the total execution time, and how much it is reduced if the time of routines A, C, & E is improved by 15%.

By how much is the total time reduced if routine B is improved by 10%?

By how much is the total time reduced if routine D is improved by 10%?

3. Given a computer *M*4 with clock rate = 3.1 GHz and a hardware accelerator that can make Type A instructions go 7 times faster, answer the following:

   If a program *P*4 has 29% Type A instructions and the remainder are Type B instructions, and its Instruction Count = 35,450 – will the accelerator make *P*4 run at least 2 times faster on *M*4 than it would without an accelerator?

Use Amdahl's Law to determine how much faster the accelerator needs to go to make *P*4 run 5.5 times faster on *M*4 (with accelerator) than it did without an accelerator.

4. You are on the design team for a new processor. The clock of the processor runs at 200 MHz. The following table gives instruction frequencies for Benchmark B, as well as how many cycles the instructions take, for the different classes of instructions. For this problem, we assume that (unlike many of today's computers) the processor only executes one instruction at a time.

Instruction Type	Frequency	Cycles
Loads & Stores	30%	6 cycles
Arithmetic Instructions	50%	4 cycles
All Others	20%	3 cycles

   Calculate the CPI for Benchmark B.

   What is the MIPS rating of the processor speed?

   The hardware expert says that if you double the number of registers, the cycle time must be increased by 20%. What would the new clock speed be (in MHz)?

   The compiler expert says that if you double the number of registers, then the compiler will generate code that requires only half the number of Loads & Stores. What would the new CPI be on the benchmark?

How many CPU seconds will the benchmark take if we double the number of registers (taking into account both changes described above)?

Memory operations currently take 30% of execution time. A new gadget called a "cache" speeds up 80% of memory operations by a factor of 4. A second new gadget called a "L2 cache" speeds up 1/2 the remaining 20% by a factor or 2. What is the total speed up?