North South University

Department of Electrical & Computer Engineering

Lab Report

Experiment No:	04
Experiment Title:	Design of a register file
Course Code:	**CSE332L**
Course Name:	**Computer Organization & Architecture Lab**
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Date of Experiment:	1-12-2020
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Equipment list: Logisim tool.

Block diagram:

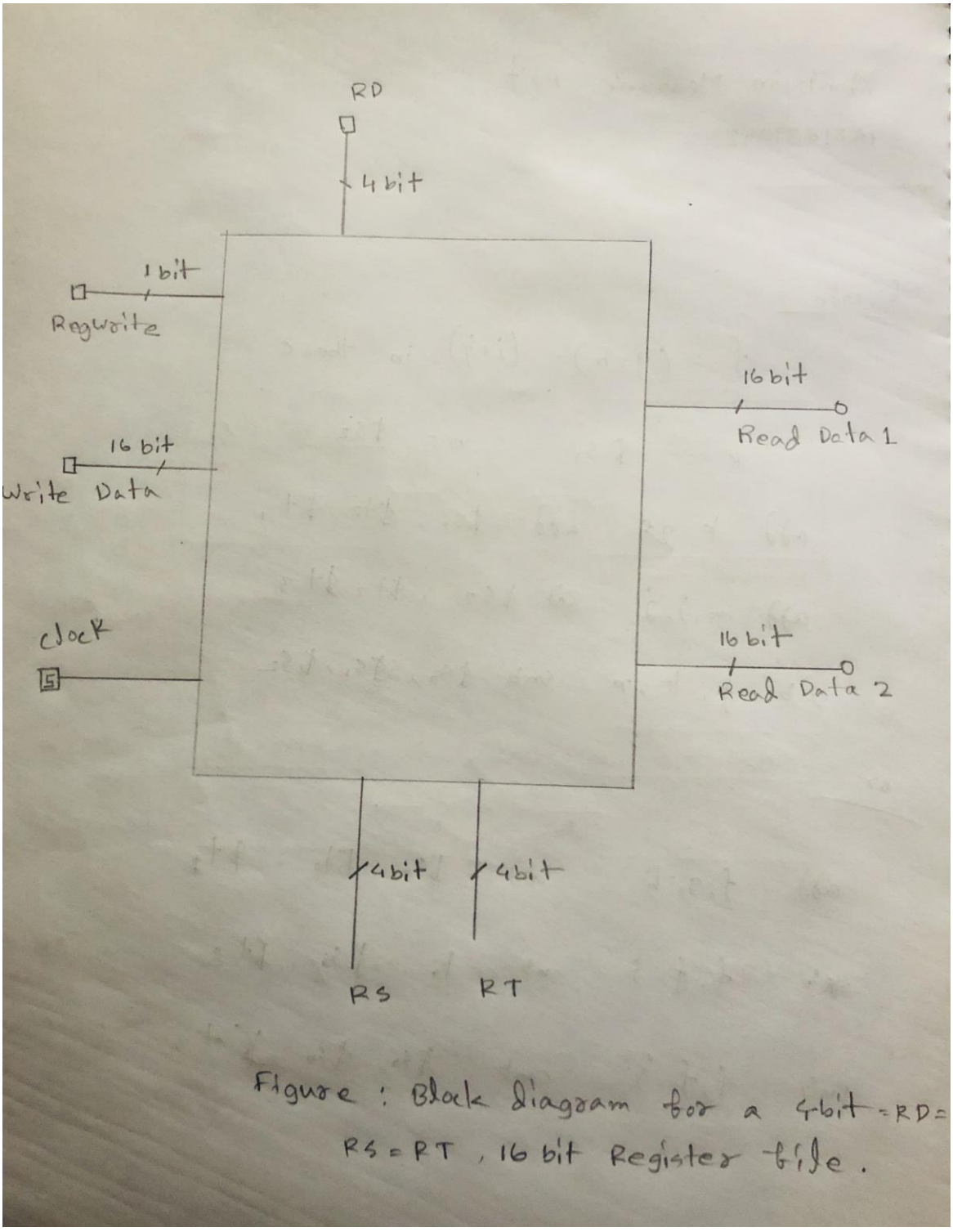

Figure : Block diagram for a 4bit =RD= RS = RT , 16 bit Register file.

Circuit diagram:

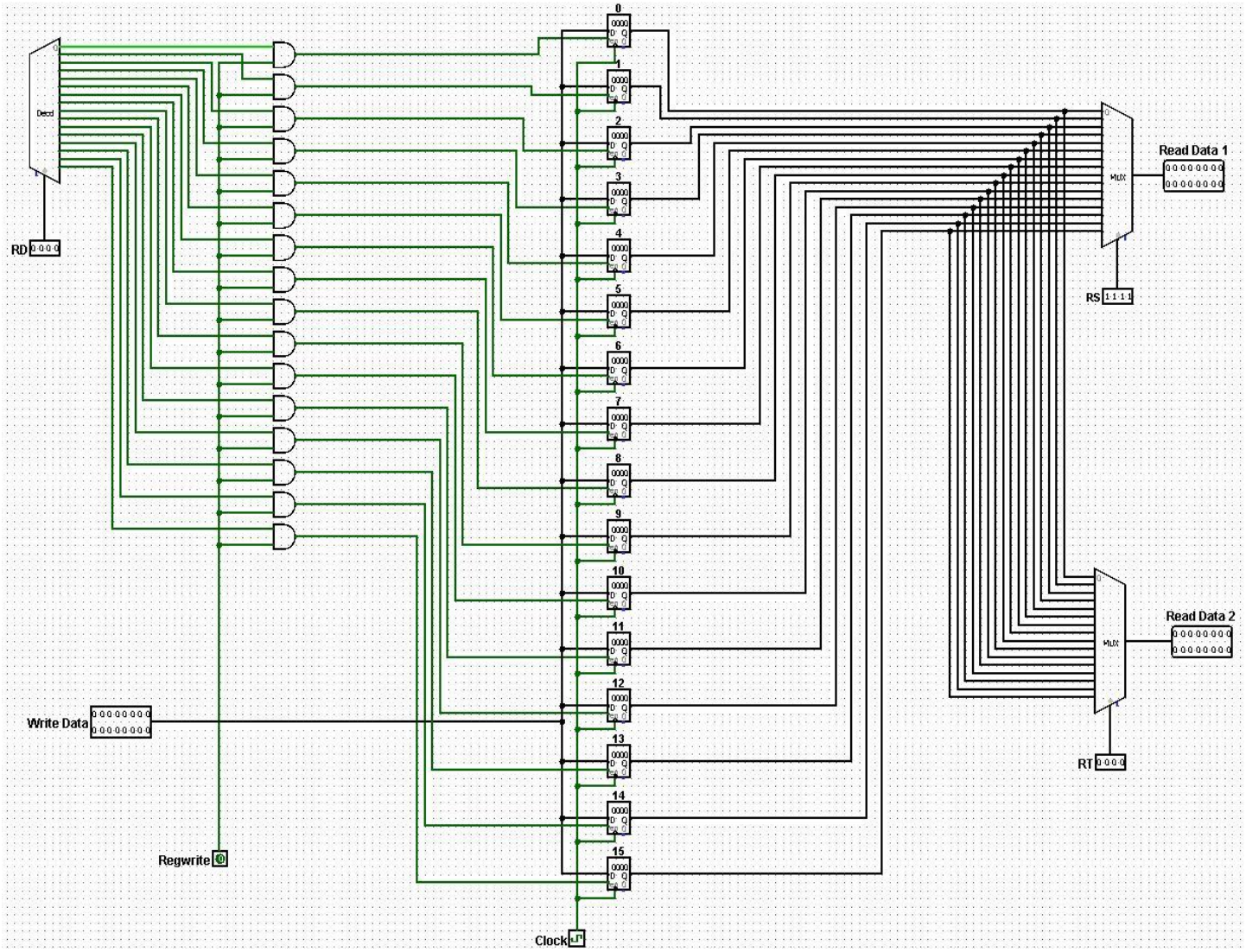

Figure: Circuit diagram of a 4-bit RD=RS=RT, 16-bit register file.

Discussion: Firstly, in Logisim, we take a 16-bit input labeled as ‘Write Data’. We take a decoder of 4-bit selection pin, with that we have 16 outputs of 1-bit data. We adda 4-bit selection pin in the decoder labeled as ‘RD’. We take 16 AND gates of 2 input numbers and add the 16 outputs respectively from the decoder in the first input of the AND gates, the other input of the AND gates will be connected with another 1-bit input labeled as ‘Regwrite’. Then we take 16 registers of 16-bit respectively labeled as 0-15(decimal). The first input of the registers will be connected with the 16-bit input labeled as ‘Write Data’. The other input of the registers will be connected respectively with the 16 outputs from the AND gates. Then we take a clock and connect it to the clock ports of the registers. Finally, we take two multiplexers of 4-bit selection pin respectively labeled as ‘RS’ and ‘RT’. The outputs from the registers will be connected to the respective ports in both of the multiplexers. From the multiplexers we will get two outputs of 16-bit respectively labeled as ‘Read Data 1’ and ‘Read Data 2’.