

North South University

Department of Electrical & Computer Engineering

Lab Report

Experiment No: 04

Experiment Title: Design of a Register File(16 Bit)

Course Code: CSE332L

Course Name: Computer Organization & Architecture Lab

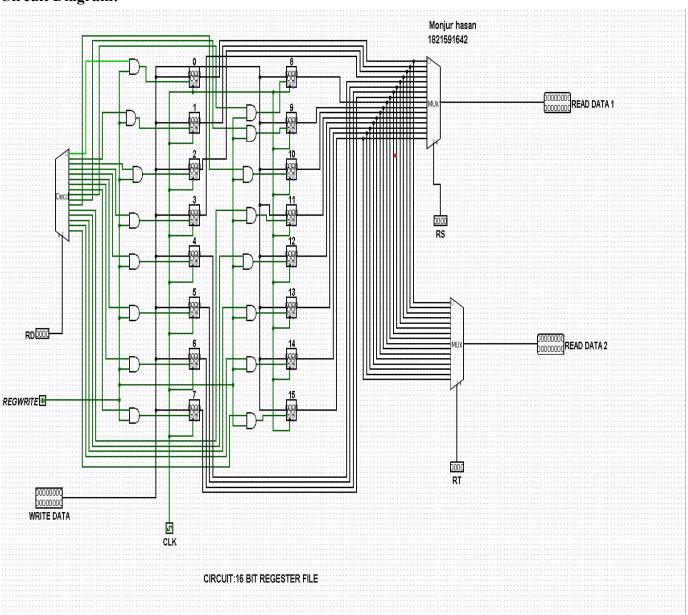
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Date of Experiment: 1/12/2020

Date of Submission: 1/12/2020

Experiment name: 16 bit Regaster Pile. Equipment list: 10 logisim tolls. Block diagram !-RT + R type 16 bit Rb - Register File write Read data 2 bata Reguerite ITU CLK Block biagram: - 16 bit Register File

Circuit Diagram:



Discussion . - By doing this lab Nous we can built 16- bit Register Bile, we built a circuit in the logisim. sinstly we take 16 bit input to werite in Resister. And we use a fecoder to select which register should work. And we connect a input with secoden each output and soing AND FOR AS a control signal. tor 166it Register me neet 4216 becoder we named it as RD'. We short all register clock for up somen data. And Finally we take 2 4x16 multiplexer tor output and named the mux or 'RS' And 'RT', And then I connect the output of Register

MADERA THE MUX input respectably. And
mux and that are 166it output.
And I named this as Read
bata I and Read Data & And
I check my circuit and this
working properly, and my Expersiment wers successfull.