Ans-1

Given,

RAM = 64 KB ; Block size = 4 bytes

cache size = 128B

∴ Total Number of lines = $\frac{128}{4} = 32$

Total Number of set = $\frac{32}{2} = 16$

Memory Address	Block, j	Set No s = j mod 16	Hit/ Miss	Line no	Consequence
3	0	0	Miss	1	Blak-0 move to line-1 of set-0
5	1	1	miss	1	Block-1 move to line-1 of set-1
10	2	2	Miss	1	Block-2 move to line-1 of set-2
65	16	0	miss	2	Block-2 move to line-2 of set-0
66	16	0	Hit	2	Read from cache
129	32	0	miss	1	Block-32 replace Block-0 in line-1 of set0
130	32	0	Hit	1	Read from cache
69	17	1	miss	2	Block-17 move to line-2 of set-1
7	1	1	Hit	1	Read from cache
133	33	1	miss	2	Block-33 replace Block-17 in line-2 of set-1
72	18	2	miss	2	Block-18 move to line-2 of set-2.
74	18	2	Hit	2	Read from cache
75	18	2	Hit	2	Read from cache

Memory Address	Block ID	Set no S=7 mod 16	Hit/Miss	Line no	consequence
11	2	2	Hit	1	Read from cache
137	34	2	Miss	2	Block-34 replace Block -18 in line-2 of set-2
1024	256	0	Miss	2	Block-256 replace Block -16 in line-2 of set-0,

$\therefore$ Hit ratio $= \frac{6}{16} \times 100$

$= 37.5\%$

Number of block replaced $= 4$

point to be noted here used LRU algorithm as replacement algorithm to replace Block in line of cache.

Ans

Ans:-2

a

In the above problem ; if we use 4 way- set associative mapping then there would shows some merits and demeritsas given below.

Demerits: (I) If we increase the value of K then the line number in every set will increas so that will take more time to match the tag of memory with tag of cache.

(II) There will be lower set number then before. so for a large number of instruction it will be problem.

Merits: (I) As there have more lines in every set so we have to use less replacement in the cache.

(II) Hit ration will be greater than before as we can store more instruction in sets with less replacement.

Average access time:

~~As the~~

we know if hit ration is greater then average access time will be lower.

means hit ratio $\propto \frac{1}{\text{Average Access time}}$

As 4-way has more hit ration than before so it will less average access time than 2-way.

$\therefore$ Average access time of 2-way > Average access time of 4-way.

Ans

b

Merits: (i) As there is no restriction to access cache in full associative mapping intially, so the more instruction can store at cache.

(ii) Cach will be use more then before.

(iii) Hit ratio will be greater than before.

Demerits:

(i) It will take more time to check the tag of RAM with tag of each than before.

(ii) We cant decide earlier where a ~~Memory~~ instruction will be store in cache.

Average Access time:

As mantioned in part a,

$$\text{hit ratio} \propto \frac{1}{\text{Average Access time}}$$

In full associtive mapping hit ratio will be greater than before for the given problem.

So Averag access time will much lower than befor for instruction/data for the given problem.

Ans

Ans:-3

Here,

Data bit = 8 bits

Parity bit = 4bits

Bits Position	12	11	10	9	8	7	6	5	4	3	2	1
Position Number	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001
Data & check bit	D_8	D_7	D_6	D_5	C_8	D_4	D_3	D_2	C_4	D_1	C_2	C_1
word read out	1	0	0	0	1	0	1	1	1	1	0	1

Data Read : 1 0 0 0 0 1 1 1

Error code Read : 1 1 0 1

Generating Error code:

$C_1 = D_1 \oplus D_2 \oplus D_4 \oplus D_5 \oplus D_7$

$= 1 \oplus 1 \oplus 0 \oplus 0 \oplus 0 = 0$

$C_2 = D_1 \oplus D_3 \oplus D_4 \oplus D_6 \oplus D_7$

$= 1 \oplus 1 \oplus 0 \oplus 0 \oplus 0 = 0$

$C_4 = D_2 \oplus D_3 \oplus D_4 \oplus D_8 = 1 \oplus 1 \oplus 0 \oplus 1 = 1$

$C_8 = D_5 \oplus D_6 \oplus D_7 \oplus D_8 = 0 \oplus 0 \oplus 0 \oplus 1 = 1$

∴ Error code = 1100

Now,

XOR of Error codes

```
  1101
  1100
------
  0001
```

Error is in 1st position

Here No data is error but there has an error in parity bit

Ans

=

Ans: 4

a

Given, -0.0000125

Now, $(0.0000125)_{10} = (0.0000000000000001101)_2$

So the Normalized form is,

$$1.101 \times 2^{-17}$$

here,

Exponent $= -17 + 127 = (110)_{10} = (01101110)_2$

significant $= (1010000\ldots)_2$

sign bit = 1 as the decimal number is negative.

∴ IEEE-32 bit format:

Sign	Exponent	Significance
1	01101110	10100000000000000000000
1bit	8 bit	23 bit

(b) Given,

sign bit = 1 so the number is Negative

Exponent with bias = $(00001110)_2 = (14)_{10}$

∴ actual Exponent = 14 - 127 = -113

Significant = $(1.0001001000100000\ldots)_2$

~~$= (1.59392010)$~~

$= (1.07080078125)_{10}$

∴ The decimal form,

$-1.07080078125 \times 2^{-113}$

$= -1.03114364545 \times 10^{-34}$

Ans