Answer to the Q. N. - 01

```
  1 0 1 1 0 0 1 0
  1 1 0 0 0 0 1 1
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1 0 1 1 1 0 1 0 1
```

$\therefore$ Carr Flag (CF) = 1

$\therefore$ Zero Flag (ZF) = 0 [result non zero]

$\therefore$ Sign Flag (SF) = 0 [MSB = 0]

$\therefore$ Even Parity = 0

$\therefore$ Half carry = 0

Answer to the Q. N. - 02

Here, 6 = $(0110)_2$

   $-5 = (1011)_2$

   m = 6 (0110)

   $\overline{m} + 1 = 1010$

   9 = -5 = ~~$\cancel{868}$~~ (1011)

$5 = 0101$

$1's a = 1010$

$2's = \dfrac{+1}{1011}$

Operation	A	Q	Q_{n+1}	m	$\bar{m}+1$	Cout
Initially	0000	1011	0			
				0110	1010	4
$Q_n Q_{n+1} = 10$	1010	1011	0	0110	1010	4
shift	1101	0101	1	0110	1010	3
shift	1110	1010	1	0110	1010	2
$Q_n Q_{n+1} = 01$	0100	1010	1	0110	1010	2
shift	0010	0101	0	0110	1010	1
$Q_n Q_{n+1} = 10$	1100	0101	0	0110	1010	1
shift	1110	0010	1	0110	1010	0

AQ = 11100010 = (-30)

2's complement:

$\overline{AQ} + 1 = 00011110$

$[16 + 8 + 4 + 2] = 30$

ⓐ Load immediate 20h → loads 20H into accumulator.

ⓑ Load direct 20h → loads 24H into accumulator.

ⓒ Load indirect 20h → loads 21H into accumulator.

ⓓ Load indirect 24H → load 25H into accumulator.

ⓔ Load R1 → load 23H into accumulator.

ⓕ Load register indirect R1 → loads 2BH into the accumulator.

ⓖ Load displacement 2, R2 → loads 2AH into accumulator.

ⓗ Load displacement 2, R1 → loads 23H into accumulator.

RAS   CAS   WE   OE

Timing and Control

Refresh Counter

MUX

Row Decoder

memory Array (4096 × 4096 × 8)

Row Adder Buffer

Column Adder Buffer

A_0

A_{11}

Refresh Circuit

column Decoder

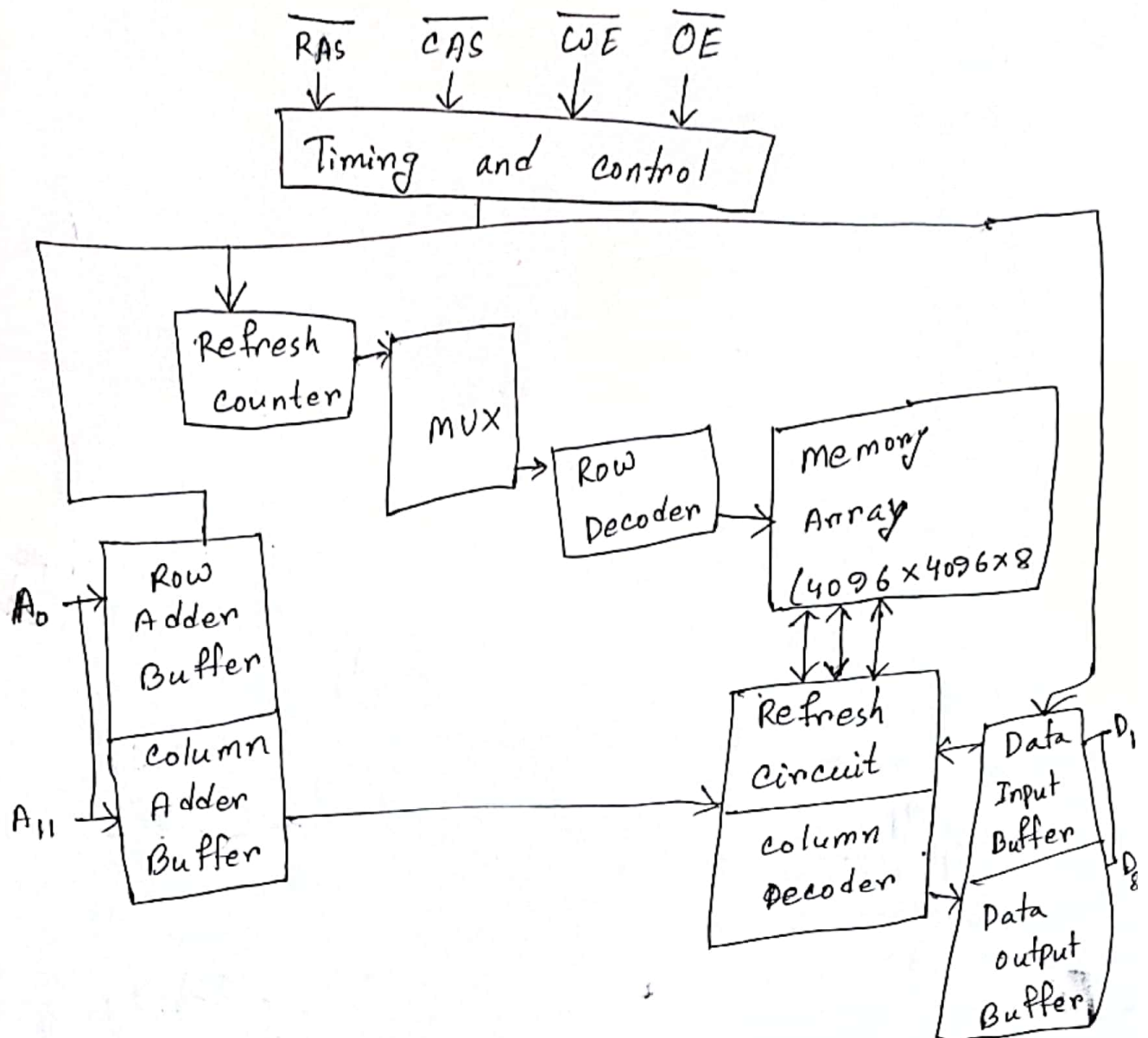Data Input Buffer

D_1

D_8

Data output Buffer

Figure - 64 M × 8 bits

Horizontal line connects to the select terminal of each cell in its row.

Vertical line connects to the Data In 1 sence terminal of each cell in its column.