



## NORTH SOUTH UNIVERSITY

Department of Electrical & Computer Engineering

### LAB REPORT

Course Name: Computer Organization & Architecture

Course Code: CSE332L

Experiment Number: 07

Experiment Name:

Build a Single Cycle Datapath.

Submitted By

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Experiment Date: 09-01-2021

Submission Date: 09-01-2021

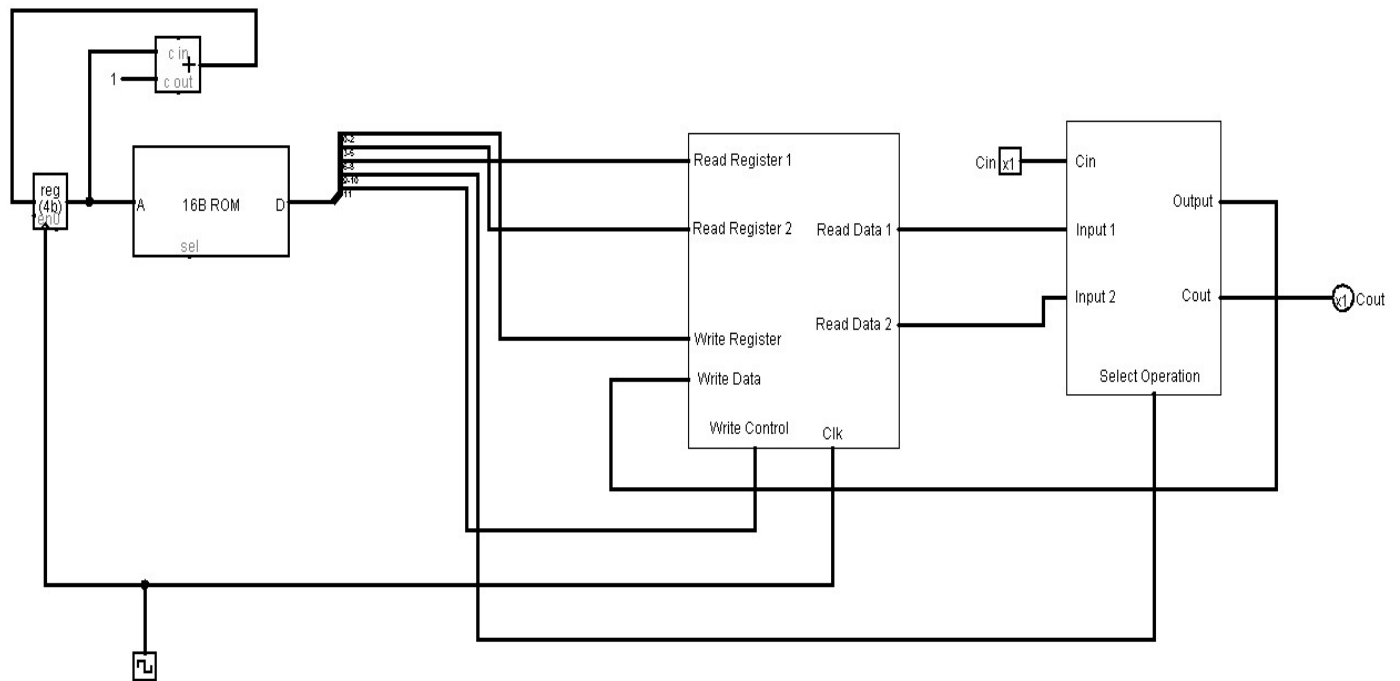
**Experiment Name:**

## Build a Single Cycle Datapath.

**Objectives:**

- We have to build an Instruction Fetch Unit of the Datapath.
- We have to implement an R-format and Load/Store Datapath.
- We have to compose the Datapath segments designed above to yield a complete single cycle Datapath.

**Circuit Diagram:**



**Figure:** Circuit diagram of a single cycle Datapath.

**Table: Instructions Decode**

Write Control	OP Code	Read Register 1	Read Register 2	Write Register	Hexa Code
1	11	000	001	010	E0A
1	10	011	100	101	CE5
1	01	010	101	110	AAE
1	00	101	110	111	977

**Discussion:**

After completing the lab, we got a clear idea to build a single cycle Datapath. As the full lab 6task, we did in Logisim software so we did not get any error. Here in this lab, we have implemented R-Type instruction only in our single cycle Datapath. We take a ROM to store our instructions. As discussed in the lab we store total 12 instruction in the ROM that's why we needed 4-bit input to address the instructions and we control the instruction traversing in the ROM by using a 4-bit Register with a 4-bit Adder. Then we got 12-bit data from the ROM which is actually our instruction that we saved in the ROM by decoding it from the written instruction to binary code then in hexa code like mentioned in the table Instruction Decode. This 12-bit data got split by the splitter where 0-2 bit went to Write Register, 3-5 bit went to Read Register 2, 6-8 bit went to Read Register 1, 9-10 bit went to Select Operation as OP-Code and the rest 1-bit went to Write Control of the 4-bit register file. At last, the final output stored in the 4-bit Register File and for every clock cycle the Datapath execute different instruction.