" Ans. to the Question No.1 "

$$\begin{array}{r} 01110010 \\ +11000011 \\ \hline \boxed{1}00110101 \end{array}$$

Carry: There is a carry in the result.

So, carry flag = 1

Zero: Result ≠ 0, So Zero flag = 0

Even Parity: Result contains even number 1

So, Even parity flag = 1

Sign: Result is positive. So, Sign flag = 0

Half-Carry: There was no carry from 4th bit.

So, Half-carry flag = 0

"Ans. to the Question No. 2"

$6 = 0110$, $5 = 0101$

$1's = 1010$

$+1$

$2's = 1011 = -5$

A	Q	Q_{-1}	M	initial values	
0000	1011	0	0110		
1010	1011	0	0110	A ← A-M	First Cycle
1101	0101	1	0110	Shift	
1110	1010	1	0110	Shift	Second cycle
0100	1010	1	0110	A ← A+M	Third Cycle
0010	0101	0	0110	Shift	
1100	0101	0	0110	A ← A-M	Fourth Cycle
1110	0010	1	0110	Shift	

"Ans. to the Question No. 3"

(a) LOAD IMMEDIATE 20H

Ans: 20H

(b) LOAD DIRECT 20H

Ans: 24H

(c) LOAD INDIRECT 20H

Ans: 21H

(d) LOAD INDIRECT 24H

Ans: 25H

(e) LOAD R1

Ans: 23H

(f) LOAD REGISTER INDIRECT R1

Ans: 2BH

(g) LOAD DISPLACEMENT 2, R_2

Ans: 2AH

(h) LOAD DISPLACEMENT 2, R1 Ans: 23H

"Ans. to the Question No. 4"

64M x 8 bits

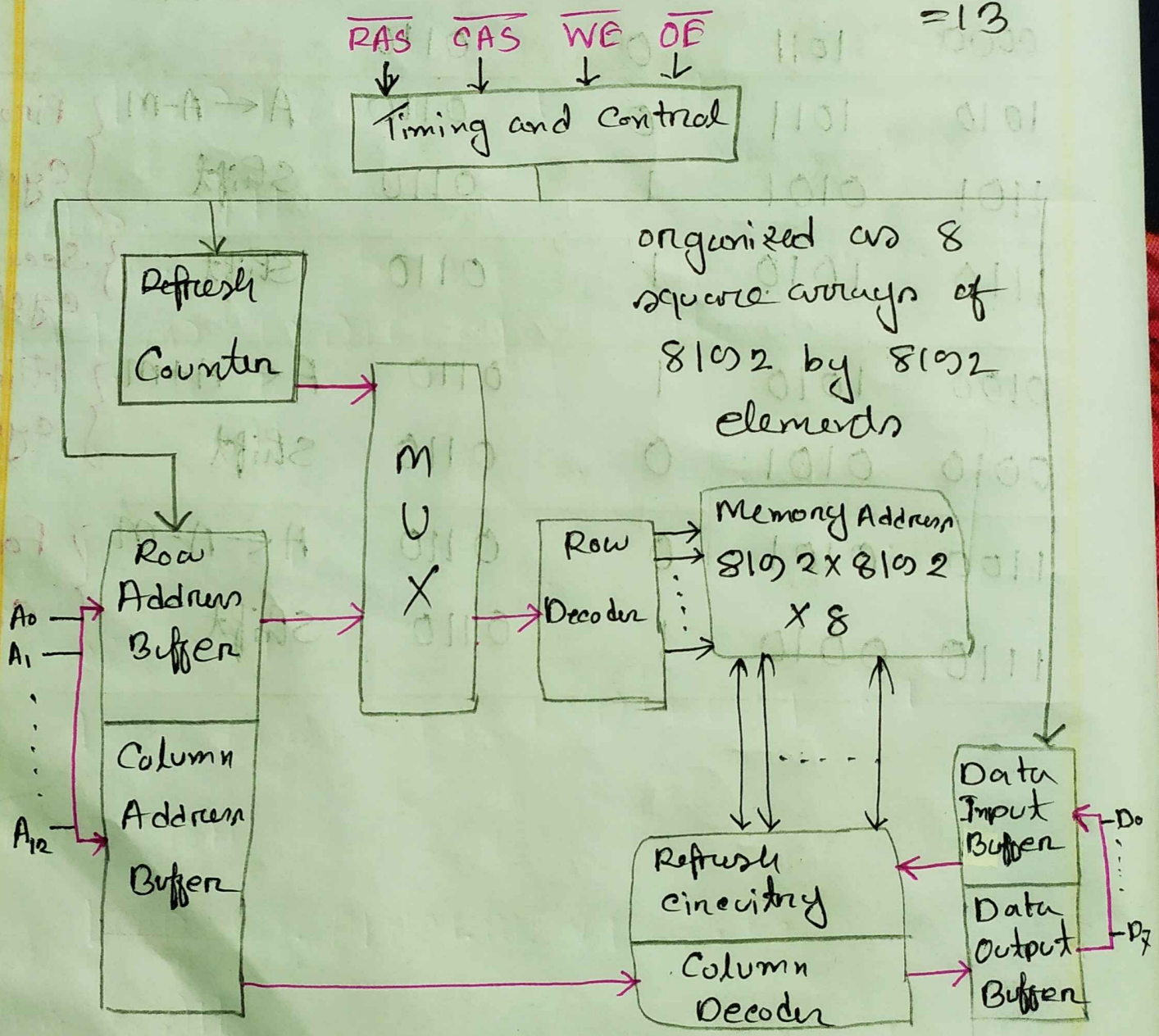
↓

$2^{20} \times 2^6$

$= 2^{26}$

∴ Address line for row and column $= \frac{26}{2}$

$= 13$



To write to a memory cell, the row and column address for the cell must be selected and data must be presented at the data input pins. The chip's on-board logic either charges the memory cell's capacitor or discharges it, depending on whether a 1 or 0 is to be stored:

(1) The row address must be applied to the address input pin on the memory device for the prescribed amount of time before $\overline{RAS}$ goes low and be held for a period of time.

(2) $\overline{RAS}$ must go from high to low.

(3) A column address must be applied to the address input pin on the

memory device for the prescribed amount of time after $\overline{RAS}$ goes low and before $\overline{CAS}$ goes low and held for the prescribed time.

(4) $\overline{WE}$ must be set low for a certain time for a write operation to occur. The timing of the transitions are determined by $\overline{CAS}$ going low.

(5) Data must be applied to the data input pin the prescribed amount of time before $\overline{CAS}$ goes low and held.

(6) $\overline{CAS}$ must switch from high to low.

(7) Before the write cycle can be considered complete, $\overline{CAS}$ and $\overline{RAS}$ must return to their inactive states.