

Assignment 2 | CSE 332

(To be submitted on 21/01/2021)

Question 1

(10 marks)

Consider the following MIPS loop:

```
LOOP: slt $t2, $0, $t1
      beq $t2, $0, DONE
      subi $t1, $t1, 1
      addi $s2, $s2, 2
      j LOOP
```

DONE:

- a) Assume that the register \$t1 is initialized to the value 10. What is the value in register \$s2 assuming \$s2 is initially zero?
- b) For the loop written in MIPS assembly above, assume that the register \$t1 is initialized to the value N. How many MIPS instructions are executed?

Question 2

(10 marks)

a) Translate the following C code to MIPS assembly code. Use the minimum number of instructions. Assume that the values of a, b, i, and j are in registers \$s0, \$s1, \$t0, and \$t1, respectively. Also, assume that register \$s2 holds the base address of the array D.

```
for(i=0; i<a; i++)
  for(j=0; j<b; j++)
    D[4*j] = i + j;
```

b) Using registers mentioned in 2(a) translate the following C code to MIPS assembly code.

```
while (a<10){
  D[a] = b + a
  a+=1
}
```

Question 3

(20 marks)

Implement the following C code in MIPS assembly using appropriate registers. Your solution does not need to be time efficient.

```
int fib(int n){
  if (n==0)
    return 0;
  else if (n == 1)
    return 1;
  else
    return fib(n-1) + fib(n-2);
}
```

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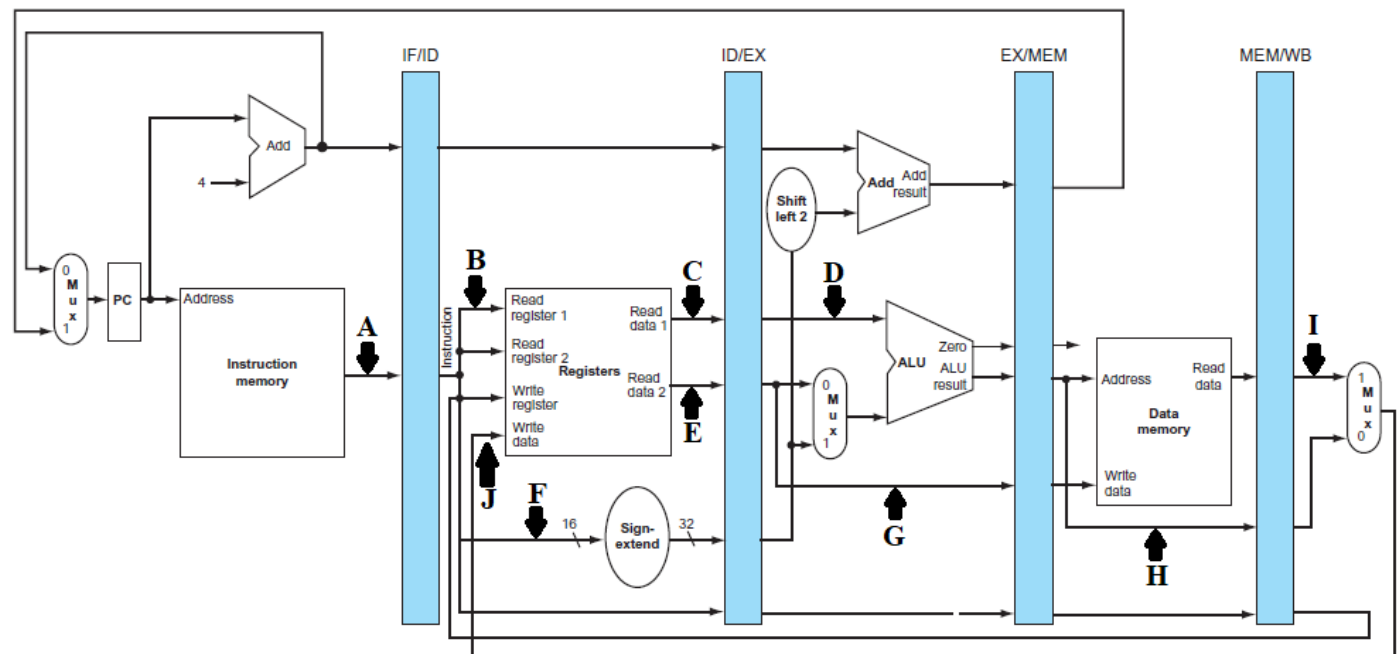
Question 4

(10 marks)

Datapath below shows a pipelined MIPS implementation. Given registers \$1 = 4, \$2 = 8, \$3 = 12, \$4 = 16, \$5 = 20, \$6 = 24, \$10 = 28, \$11 = 32, \$12 = 36, \$13 = 40 and \$14 = 44, and memory locations [24] = 50 and [28] = 100, what are sizes and values of the data in the indicated locations? If any value is unknown, put an "X".

	Size (or Number of bits)	Value
A		
B		
C		
D		
E		
F		
G		
H		
I		
J		

add \$14, \$5, \$6	lw \$13, 24(\$1)	add \$12, \$3, \$4	sub \$11, \$2, \$3	lw \$10, 20(\$1)
Instruction fetch	Instruction decode	Execution	Memory	Write-back



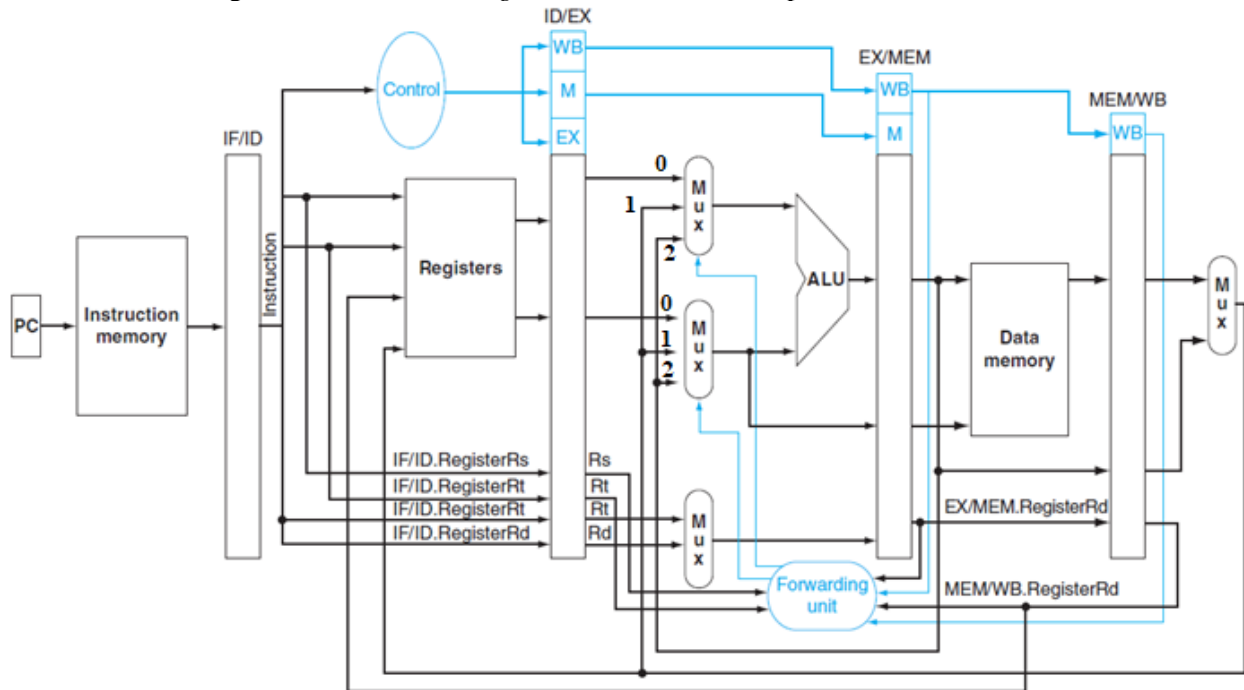
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Question 5

(10 marks)

The pipelined MIPS implementation in *Question 4* can be modified to resolve data hazards through *Forwarding*. Draw a possible internal circuit diagram of the *Forwarding Unit* shown in the datapath below.



Question 6

(10 marks)

Consider the same datapath in *Question 5*, how can the register file be modified to resolve the data dependence between the first and fourth instructions in the following program? To demonstrate this modification, design a register file containing four two-bit registers.

