Name: MD. ABU AMMAR
Id: 1821944642

Ans: 1

Given that,

RAM = 64 KB

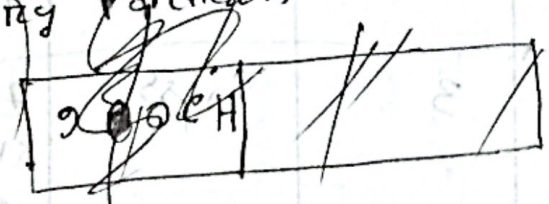
Block size, j = 4 Bytes

cache size = 64 Bytes

$\therefore$ set = $\frac{64}{4 \times 2} = 8$

For 90 C4 H in decimal 37060

Memory Format,



Address	Block, j	S	Hit/miss	comment consequence
90C4H=37060	J= 9265	s= j mod set = 9265 % 8 = 1	miss	Block - 9265 is transferred into set 1
9B1A=39706	9926	6	miss	Block 9926 transfer to set 6.
41EA 3H	4218	2	miss	4218 block transfer into set 2.
3BB8 H	8822	6	hit	CPU read from cach
F445H	15633	1	miss	15633 will be replace inset 1
6ECFH	7091	3	miss	7091 block shift to set 3
E7F1H	14844	4	hit	read from cach
5EEB H	6074	2	hit	read from cache
5EEBH	6074	2	hit	read from cache
5743H	5584	0	hit	(1)
CF7C	13279	7	hit	4

Ans: 3

Given, m = 12 bit

$D_{12}\ D_{11}\ D_{10}\ D_9\ D_8\ D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1$
1 1 0 0 1 0 1 1 1 0 0 1

Now, $2^K \geq m + K$

$2^4 \geq 12 + 4$

$\therefore 16 \geq 16$

$\therefore K = 4$

Now, parity bits are 1, 2, 4, 8

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
10000	01111	01110	01101	01100	01011	01010	01001	01000	00111	00110	00101	00100	00011	00010	00001
D_{12}	D_{11}	D_{10}	D_9	D_8	D_{87}	D_6	D_{65}	C_8	D_4	D_3	D_2	C_4	D_1	C_2	C_1

$C_1 = D_1 \oplus D_2 \oplus D_4 \oplus D_5 \oplus D_7 \oplus D_9 \oplus D_{11}$

$= 1 \oplus 0 \oplus 1 \oplus 1 \oplus 0 \oplus 0 \oplus 1 = 0$

$C_2 = D_1 \oplus D_3 \oplus D_4 \oplus D_6 \oplus D_7 \oplus D_{10} \oplus D_{11}$

$= 1 \oplus 0 \oplus 1 \oplus 1 \oplus 0 \oplus 0 \oplus 1 = 0$

$C_4 = D_2 \oplus D_4 \oplus D_8 \oplus D_9 \oplus D_{10} \oplus D_{11}$

$= 0 \oplus 1 \oplus 1 \oplus 0 \oplus 0 \oplus 1 = 1$

$C_8 = D_5 \oplus D_6 \oplus D_7 \oplus D_8 \oplus D_9 \oplus D_{10} \oplus D_{11}$

$= 1 \oplus 1 \oplus 0 \oplus 1 \oplus 0 \oplus 0 \oplus 1 = 0$

So, $C_8 C_4 C_2 C_1 = 0100$, Thus 4 number bit has an error

∴ correct data bit $= D_4 = 0$, here the code is error.

So the correct data bits are $= (3, 5, 6, 7, 9, 10, 11, 12)$

Ans

Ans:-4

(a) Given,

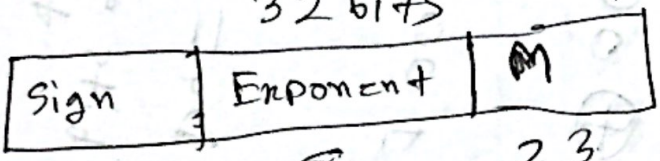
387.625

$(387)_{10} = (110000011)_2$

$(0.625)_{10} = (0.101)_2$

we ~~know~~, ~~for~~

32 bits



$\therefore (387.625)_{10} = (110000011.101)_2$

$= 1.10000011101 \times 2^8$

M = 10000011101 (23 bits)

e = 8

E = 8 + 127 = 135 = $(10000111)_2$

0	10000111	10000111101000000000000

(b)

Here,

$E = 10001110 = 142$

$M = 00110000000000000000000$

$Value = (-1)^S \times 1.M \times 2^{E-bias}$

$= (-1)^1 \times 1.0011 \times 2^{142-127}$

$= (-1) \times 1.11 \times 2^{-2} \times 2^{15}$

$= (-1) \times 1.11 \times 2^{13}$

$= (-1)\ 11100000000000 = -14336$

Ans

~~Ans) 2 (6)~~

(b) here

Sign bit	Exponent	Significant.
1	10001110	00.11000000....

decimal of significant, 0011000...

$= 0 \times 2^{-1} \Rightarrow 0$

$= 0 \times 2^{-1} \Rightarrow 0$

$= 1 \times 2^{-3} \Rightarrow 0.125$

$= 1 \times 2^{-4} = 0.0625$

$= 1 \times 2^{-5} \Rightarrow 0$

0.1875...

Normalized form $= 1.1875$

Decimal of exponent, $(10001110)_2 = (142)_{10}$

$\therefore$ Exponent $= 142 - 127$

$= 15$

$\therefore$ Decimal value is 1.1875×10^{15}

Ans

Ans:-2

here,

0003 - hit

0004 - hit

0005 - miss

0006 - hit

0007 - miss

0008 - hit

0009 - hit

$$\text{hit ratio} = \frac{5}{7} \times 100\%$$

$$= 71.43\%$$

Ans

Quiz 4

Quiz-4

Firstly we try to make 4M x64 bit module from 4M x4 bit module.

Now, $\frac{64}{4} = 16$

So it requires 16, 4M x4 bit chips for one module.

Let data bus be D 63 - D0

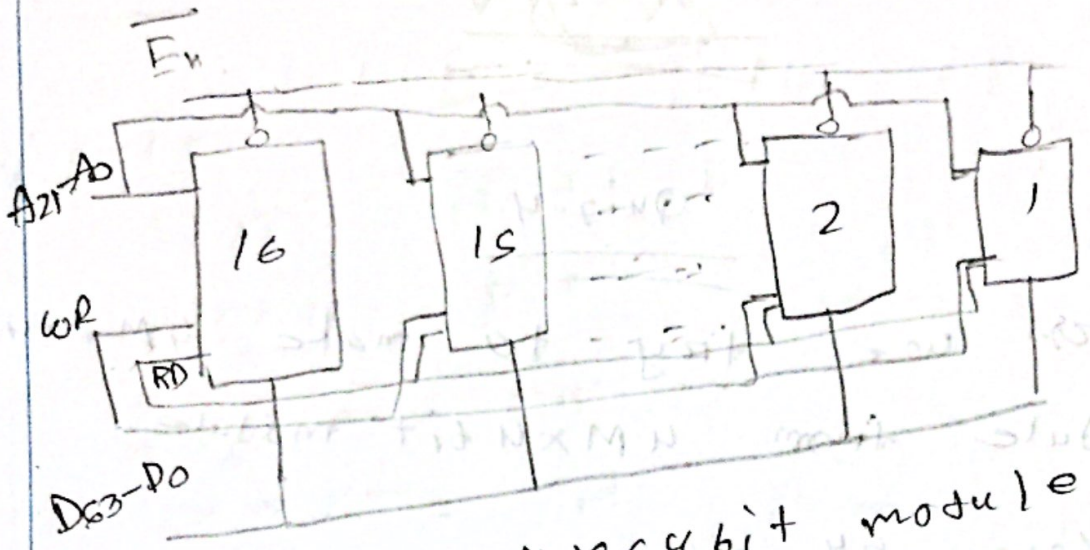
∴ For all these 16 chips, address bus, chip enable, read, write are connected together individually.

but for data bus.

D3 D2 D1 D0 is connected to chip 1

and so on, so that

D63 D62 D61 D60 is connecte to chip 16.



4 M×64 bit module

Now, $CAM = 2^6 \times 2^{20} = 2^{26}$

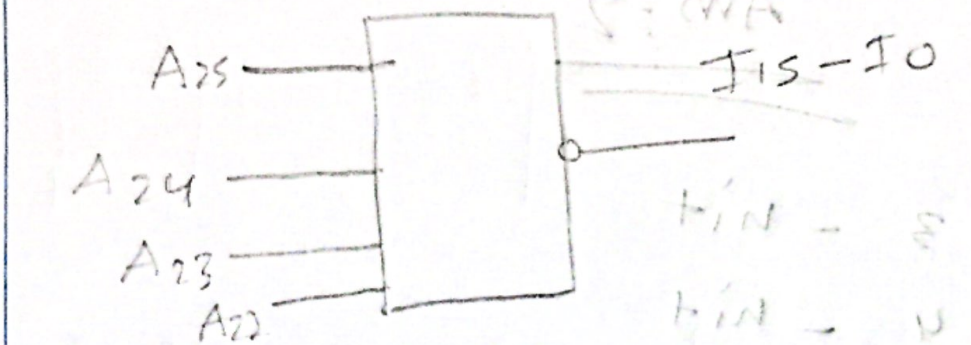
So, it has 26 address line

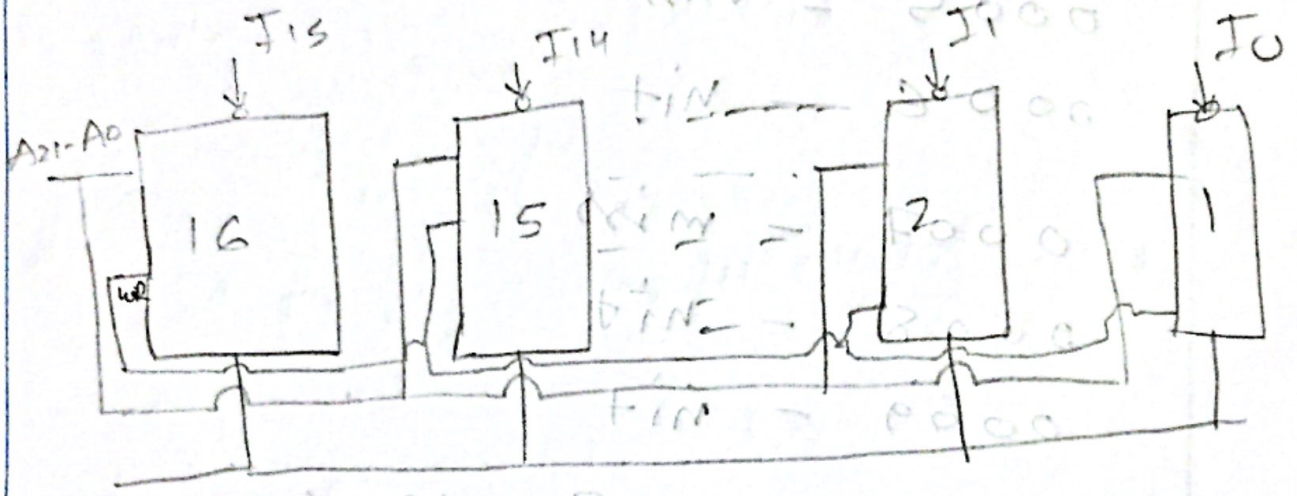
~~and we~~ ab

So A25 A24 A23 A22 will be used by decoder of $2^4 = 16$ select lines

~~For~~. So it requires 16 4M×64 bit modules

For these 16 modules, address & data bus read, write lines are common, but enable will be different.





Ans