North South University
Department of Electrical and Computer Engineering
CSE 332 Computer Organization & Architecture Fall 2020
Final Term Examination Set A
Total Marks: 40 | Duration: Two hours

Answer ALL Questions. Good Luck!

Question 1 **(1+1+2)**

The world of Computer Architecture is quite interesting! A lot can be unraveled about a computer just by looking at its instruction set architecture. So, a group of interns were asked to answer some questions about a certain computer Y, just by having a look at the pattern of one of its instructions types. This computer contained a processor that can be thought of as a smaller version of 32 bit MIPS. Following is the R-type instruction of Y's processor.

op	rs	rt	rd	shamt	func
4 bits	3 bits	3 bits	3 bits	3 bits	4 bits

Let's see if you can answer the questions that the interns were asked!

a) What is the size of any of Y's instructions?
b) How many registers were present in Y's processor?
c) How many different R-type instructions are possible?

Question 2 ***(Choose the right answer or fill in the blanks)*** **(4)**

i) Processor having Clock cycle of 0.5ns will have clock rate of

a) 2GHz b) 3GHz c) 4GHz d) 8GHz

ii) If computer A executes a program in 5 seconds and computer B runs the same program in 15 seconds, what is the relative performance of computer A compared to computer B?

a) 1.4 b) 1.5 c) 0.67 d) 3

iii) The situation when the data of operands are not available is called __________.

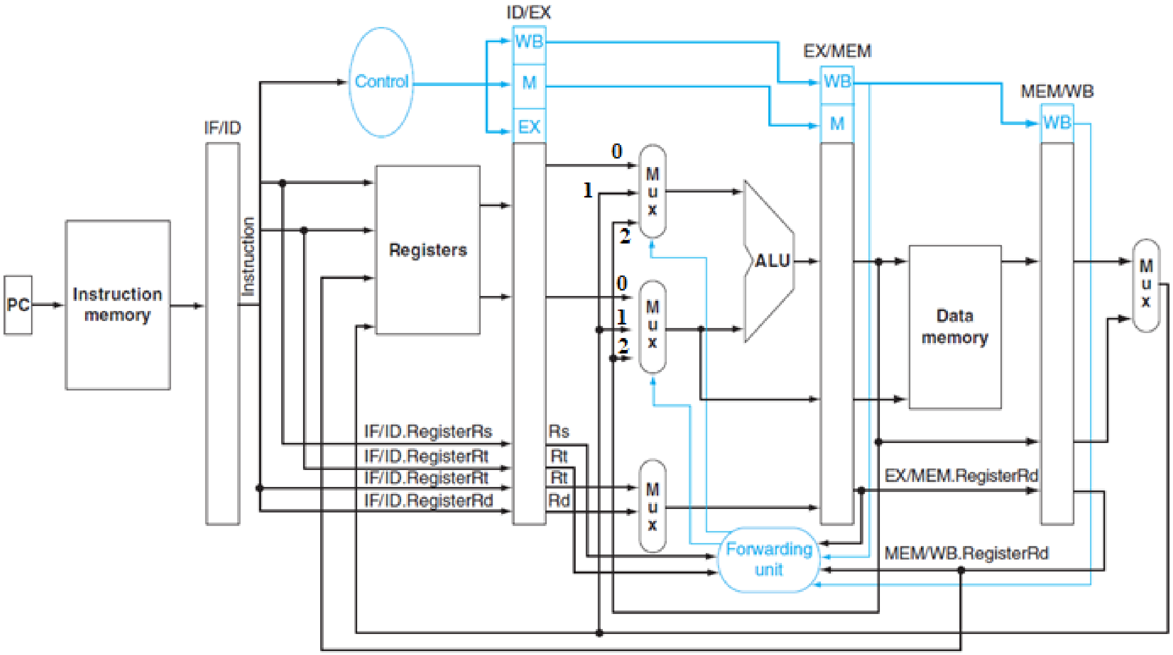
a) Data hazard b) Stall c) Deadlock d) Structural hazard

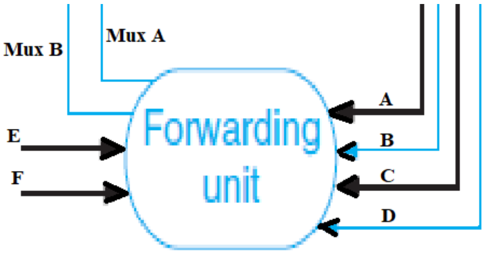
iv) Each stage in pipelining should be completed within ____ cycle.

a) 1 b) 2 c) 3 d) 4

Question 3 (6+6+2+2+8)

i. Following figure shows a pipelined datapath, which includes hardware required for forwarding. You need to fill up the table below.





Inputs	Name	Size	Values	Values	Values
A			9	22	14
B			1	1	1
C			11	22	14
D			1	0	0
E			12	14	14
F			9	15	14
Outputs					
Mux A		2			
Mux B		2			

ii) Translate the following high level code into MIPS Assembly code.

High Level code

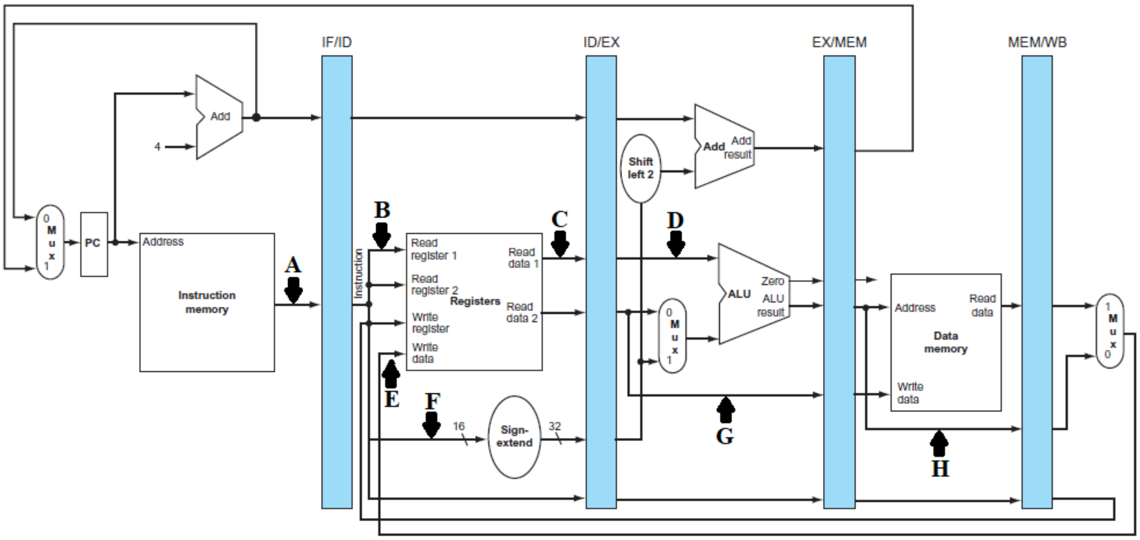
```
…
int main(){
   int i,y, fib[10];
   int n0 = 0;
   int n1 = 1;
      for(i=0;i<10;i++){
      if(i<2){
         fib[i]=i;
         }
      else{
         fib[i]=n0+n1;
         n0 = n1;
         n1 = fib[i];
         }
      y = doubleFib(fib[i]);
      }
   …
}

…

int doubleFib(int x){
   return 2*x;
}
```

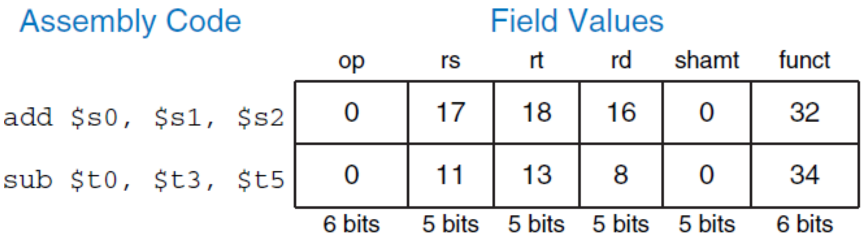
iii) How many instructions are executed to run the above program?

iv) Figure in **page number 2** shows a pipelined MIPS implementation. If all stages require 200 ns to complete its work, how much time will be taken to execute the above program in a five stage pipelined MIPS processor?

v) In the following pipelined datapath, $1 = 5, $2 = 8, $3 = 12, $4 = 16, $5 = 20, $6 = 24, $10 = 28, $11 =32, $12 = 36, $13 = 40 and $14 = 44, and memory locations [24] = 50 and [28] = 100. Using these values and some additional information given below, fill the table? If any value is unknown, put an "**X**".

sub $11, $2, $3	lw $13, 24 ($1)	add $12, $3, $4	lw $10, 20($1)	add $14, $5, $6
Instruction fetch	Instruction decode	Execution	Memory	Write-back





Assembly Code

Field Values

	op	rs	rt	rd	shamt	funct
add $s0, $s1, $s2	0	17	18	16	0	32
sub $t0, $t3, $t5	0	11	13	8	0	34
	6 bits	5 bits	5 bits	5 bits	5 bits	6 bits

	Size (or Number of bits)	Value
A		
B		
C		
D		
E		
F		
G		
H		

Question 4 **(2+2+4)**

Back in the days, main memory modules used to be quite small in size. One such a module was of size 4 MB, which was connected to a processor with a direct mapped cache that could hold 64 KB of data. Both the main memory had a block size of 16 bytes.

a) If both the main memory and the cache were byte addressable, what could have been the minimum size of the physical memory address used for addressing both the main memory and the cache?

b) What could have been the size of "tag" for addressing cache?

c) Based on you answers to parts **a** and **b**, what should have been the **total** size of the direct mapped cache if each cache block contained an additional valid bit?