**Makeup-MT: CSE 332/Sections: 4 & 5**

**Marks = 40 Time = 1 Hour 30 mins**

**NSU-Fall 2020**

**Answer all questions**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. | For a system, RAM = 64KB, Block size = 4 bytes, Cache size = 128 bytes, 2-way Set Associative cache. CPU requires to access following memory locations while running a program “Test\_Cache”.  3, 5, 10, 65, 66, 129, 130, 69, 7, 133, 72, 74, 75, 11, 137, 1024 (for convenience, addresses are given in decimal).  Calculate the Hit ratio assuming the cache is empty at the beginning. Also count the number of blocks replaced in cache memory if LRU (least Recently Used) is used as replacement algorithm.  Please construct a table as follows and calculate/provide info for each address.   |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Memory address | Block of RAM | Set no  Checked  (to be assigned in case of Miss) | Hit/  Miss | Consequence | Comments, if any | State of cache | | 3 | 0 | 0 | M | Block-0 is transferred into Line-1 of Set-0 | Line-1 is chosen randomly | |  |  |  |  | | --- | --- | --- | --- | | Set-0 | Line-1 | ~~B-0~~ | B-32 | |  | Line-2 | ~~B-16~~ | B-256 | | Set-1 | Line-1 | B-1 |  | |  | Line-2 | ~~B-17~~ | B-33 | | Set-2 | Line-1 | B-2 |  | |  | Line-2 | ~~B-18~~ | B-34 | | Set-3 | Line-1 |  |  | |  | Line-2 |  |  | | -- |  |  |  | | -- |  |  |  | | Set-15 | Line-1 |  |  | |  | Line-2 |  |  | | | 5 | 1 | 1 | M | Block-1 is transferred into Line-1 of Set-1 | Line-1 is chosen randomly | | 10 | 2 | 2 | M | Block-2 is transferred into Line-1 of Set-2 | Line-1 is chosen randomly | | 65 | 16 | 0 | M | Block-16 is transferred into Line-2 of Set-0 | Line-2 is found free | | 66 | 16 | 0 | H | CPU reads from Line-2 of Set-0 |  | | 129 | 32 | 0 | M | Block-32 is transferred into Line-1 of Set-0 | B-0 of Line-1 is replaced since B-16 of Line-2 has been accessed recently and Least Recently used (LRU) algorithm is used | | 130 | 32 | 0 | H | CPU reads from Line-1 of Set-0 |  | | 69 | 17 | 1 | M | Block-17 is transferred into Line-2 of Set-1 | Line-2 is found free | | 7 | 1 | 1 | H | CPU reads from Line-1 of Set-1 |  | | 133 | 33 | 1 | M | Block-33 is transferred into Line-2 of Set-1 | B-17 of Line-2 is replaced since B-1 of Line-1 has been accessed recently and Least Recently used (LRU) algorithm is used | | 72 | 18 | 2 | M | Block-18 is transferred into Line-2 of Set-2 | Line-2 is found FREE | | 74 | 18 | 2 | H | CPU reads from Line-2 of Set-2 |  | | 75 | 18 | 2 | H | CPU reads from Line-2 of Set-2 |  | | 11 | 2 | 2 | H | CPU reads from Line-1 of Set-2 |  | | 137 | 34 | 2 | M | Block-34 is transferred into Line-2 of Set-2 | B-18 of Line-2 is replaced since B-2 of Line-1 has been accessed recently and Least Recently used (LRU) algorithm is used | | 1024 | 256 | 0 | M | Block-256 is transferred into Line-2 of Set-0 | B-16 of Line-2 is replaced since B-32 of Line-1 has been accessed recently and Least Recently used (LRU) algorithm is used |   ----- | **15** |
| 2. | 1. Briefly discuss relative merits and demerits if 4-way set associative cache is used in above problem. Also compare the average access time for instruction/data. 2. Briefly discuss relative merits and demerits if fully- associative cache is used in above problem. Also compare the average access time for instruction/data. | **5** |
| 3. | A 12-bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written into memory if the 12-bit word read out is 100010111101 | **5** |
| 4. | a) Convert -0.0000125 to IEEE 32-bit floating point format.  b) Convert the following IEEE 32 bit into decimal.  Please show the calculations for both the questions.   |  |  |  | | --- | --- | --- | | Sign bit | exponent | significant | | 1 | 00001110 | 00010010001000000000000 | | **10** |