**Quiz-5/Marks = 5/ Time= 20 mins**

A superscalar processor, shown below, is running a program given below. Show the execution sequence using “in-order-issue-in-order-completion” policy. Also calculate the run time. Calculate the uses 1GHz clock.

Fetch

Unit-1

Fetch

Unit-2

Decode

Unit-1

Decode

Unit-2

Integer ALU

Floating Point

Unit

Write-back

Unit-1

Write-back

Unit-2

Inst-1: floating point operation and requires 3 clock cycles

Inst-2: integer operation and requires one clock cycle

Inst-3: floating point operation, requires two clock cycles and depends on output of Inst-2.

Inst-4: Integer operation, requires two clock cycles

Inst-5: Integer operation, requires one clock cycle but depends on output of Inst-4

Inst-5 and Inst-6 are integer operations, require one clock cycle each but conflict for a register within CPU

Please note that Integer operations may use any ALU but floating point operations require floating point ALU only.

**Quiz-6/Marks = 5/ Time= 10 mins**

1. What do you understand by Register Renaming? 1
2. What types of data dependencies could be removed by this? Give examples. 3
3. Also comment what type of instruction issuing policy prefer this technique. 1