
**Department of Electrical and Computer Engineering**

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**CSE435**

***Group-3***

# Project Name: 4 Bit Subtractor

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**Submitted to**

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## Abstract:

4-bit subtractor is a combinational digital circuit that performs 4 bit subtraction with borrow-in. The Main objective of this project is to design 4-bit Subtractor by using electricBinary and ModelSim software with reduced number of transistors without any error. Two types of simulation or test bench will be performed in order to ensure that the implementation is fully functional. First, a schematic simulation will be performed by means of the "elctricBinary" software. Second, the 4-bit subtractor layout model will be emulated by the "ModelSim software". Performing the simulation mainly consists of evaluating the output of 4-bit subtractor.


## Introduction:

Arithmetic circuits are important part of Digital circuits. In the digital circuits, subtractor is one of the most critical components used in the processor of portable devices. Here we are going to build 4-bit subtractor by using 4 parallel full adder. We are designing two parts of this circuit:

- Schematic design of 4-bit subtractor by using CMOS transistor.
- Layout design of 4-bit subtractor by using nMOS and pMOS.

For this project we are using two software one is "electricBinary" and another one is "ModelSim" where one is to design and another one is to use the testbench for check the output. Also several steps are taken, subtractor using adder that is how can subtract by adding between bits. Logic diagram of full adder and also the schematic diagram of full adder circuit. After that, we have used "logisim" software for the purpose to check the output and so on. Step by step we design schematic and layout design and check for the error. Errorless output is our expected output.

## FULL ADDER:


Fig. 1 bit full adder circuit

So let's *add* two numbers,

A=12 & B=7, so A+B=19

In binary, 12=1100

\+ 7=0111

Sum, 19=1|0011

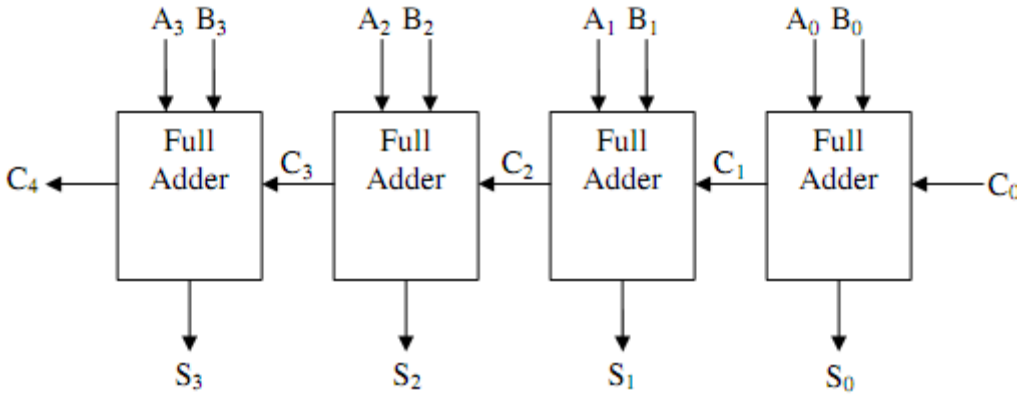



Fig. 4 bit Full adder circuit

Now we are going to implement our main project based on the footprints of a full adder circuit with some slight changes. Basically, in case of subtractor circuit we are going to Invert (NOT) the input of B and the Count which we will get in the final part of our 4 bit circuit. The reason of doing this inversions are discussed below in details.

## 4 bit subtractor using full adder:

Now let's subtract two numbers, let A=12 & B=7

So A-B = A+ (-B)
=A+ (2s Complement of B)
=A+ (1s complement of B)

That is, A= 1100
And B=0111
=1000(1s complement of B) [this inversion is getting from the NOT gate of B]
=1001(2s complement of B) [this '1' is from the input Cin, which we are providing]

Now A=12=1100
\- B=7 =1001
Diff +5 =1|0101

Again let's say A=7 whereas B=12, so by subtracting, we will get Difference, DF= -5

For this reason, the final Borrow (B) will be inverted to show that the zero will be inverted to one, which will represent that the answer is a positive number and the output one will represent that the answer is a negative number.

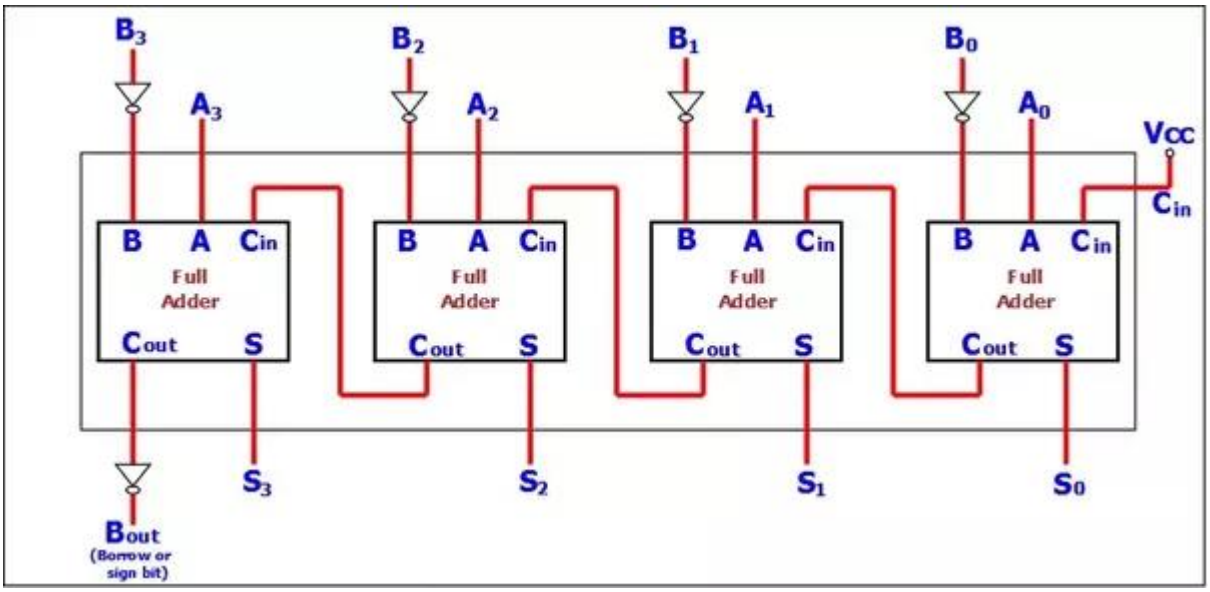



Fig. 4 bit subtractor circuit using full adder

## Two important equation:

S=A.B.Cin + Cout' (A+B+Cin)

Cout=A.B+ (A+B).Cin

## 4-Bit subtractor circuit (logisim):

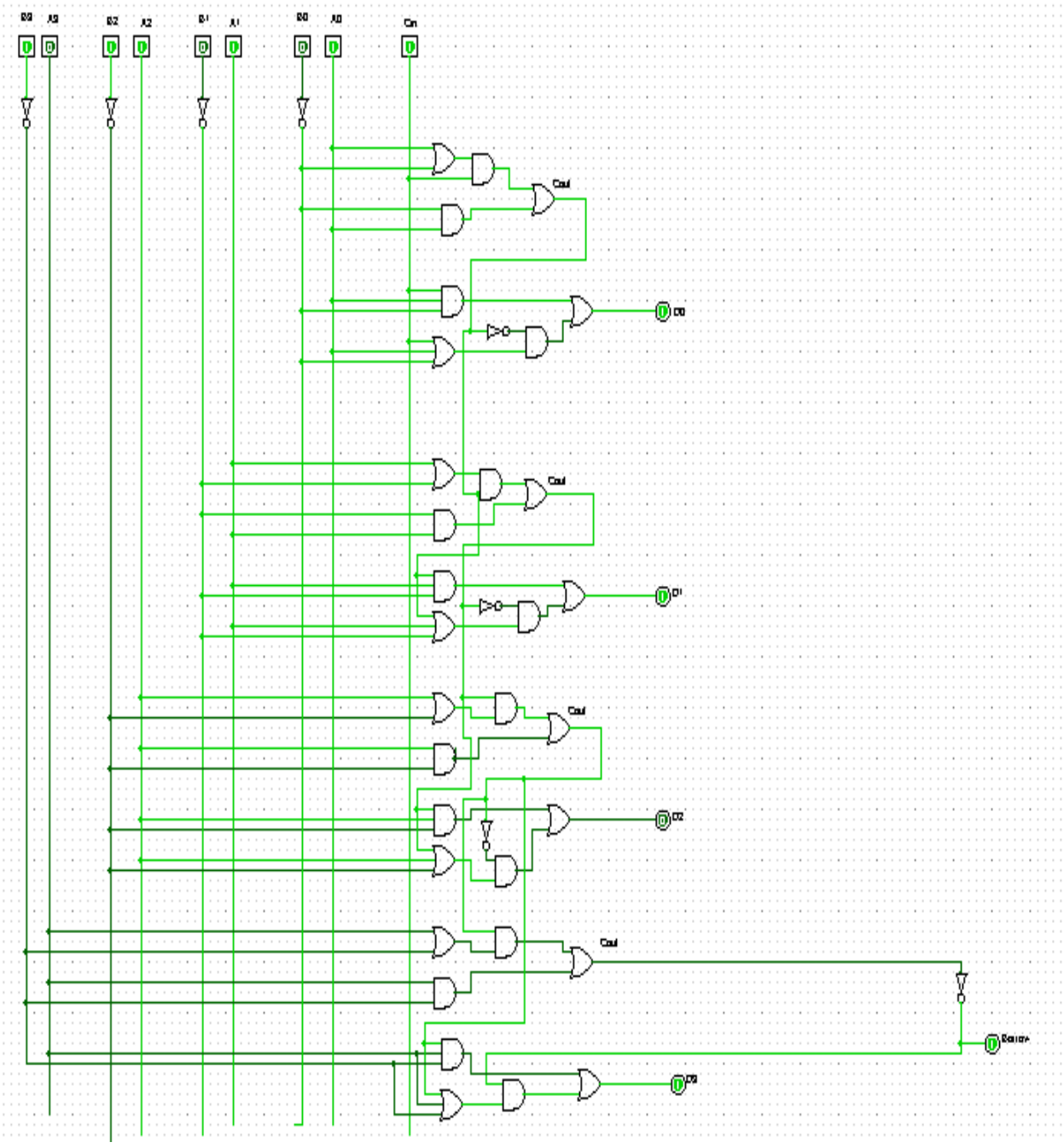
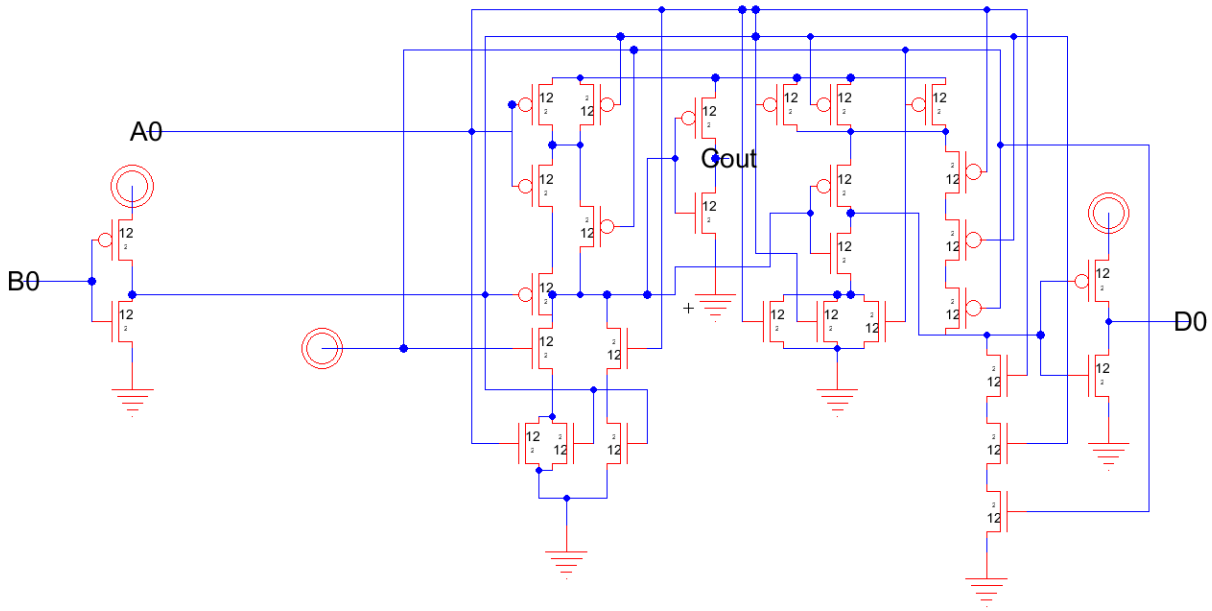
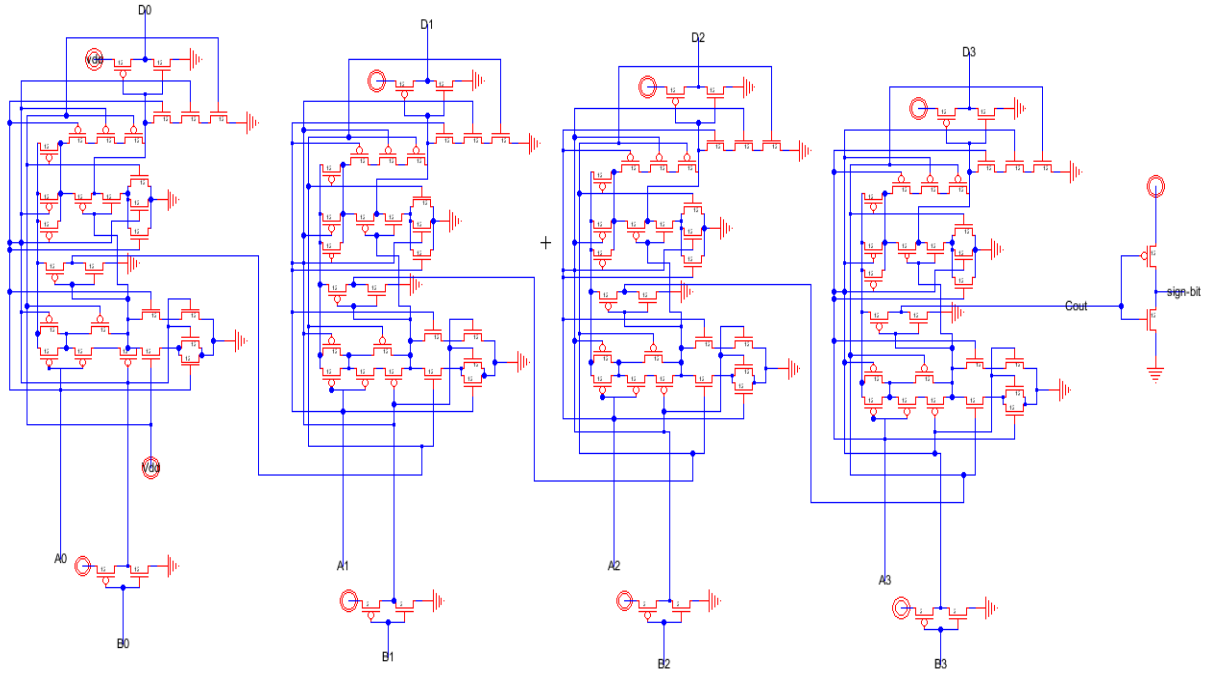


Fig. logisim of 4 bit subtractor

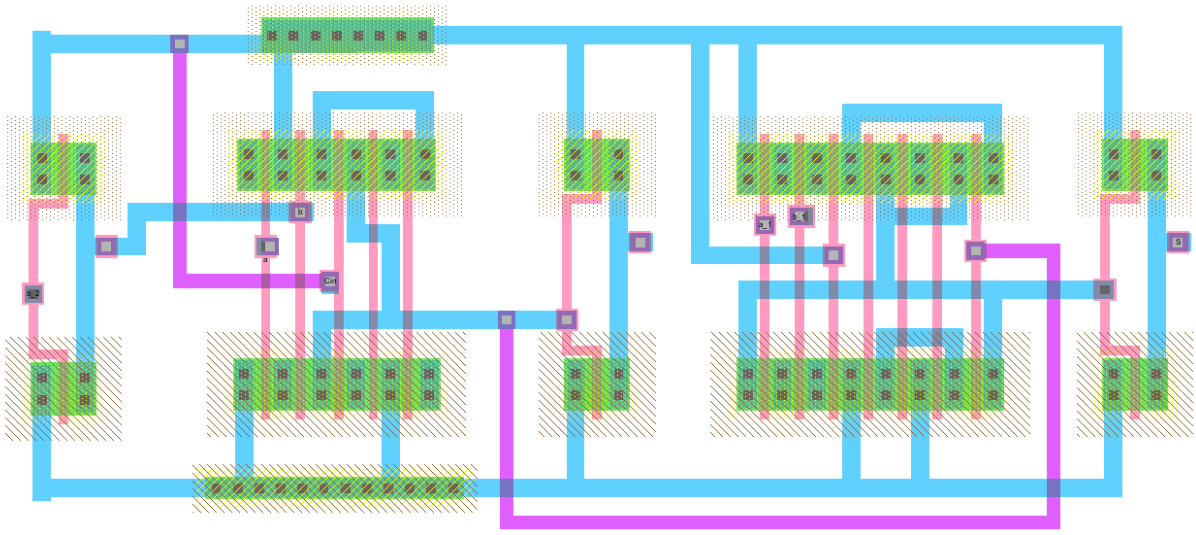
## 1 bit subtractor circuit (schematic):



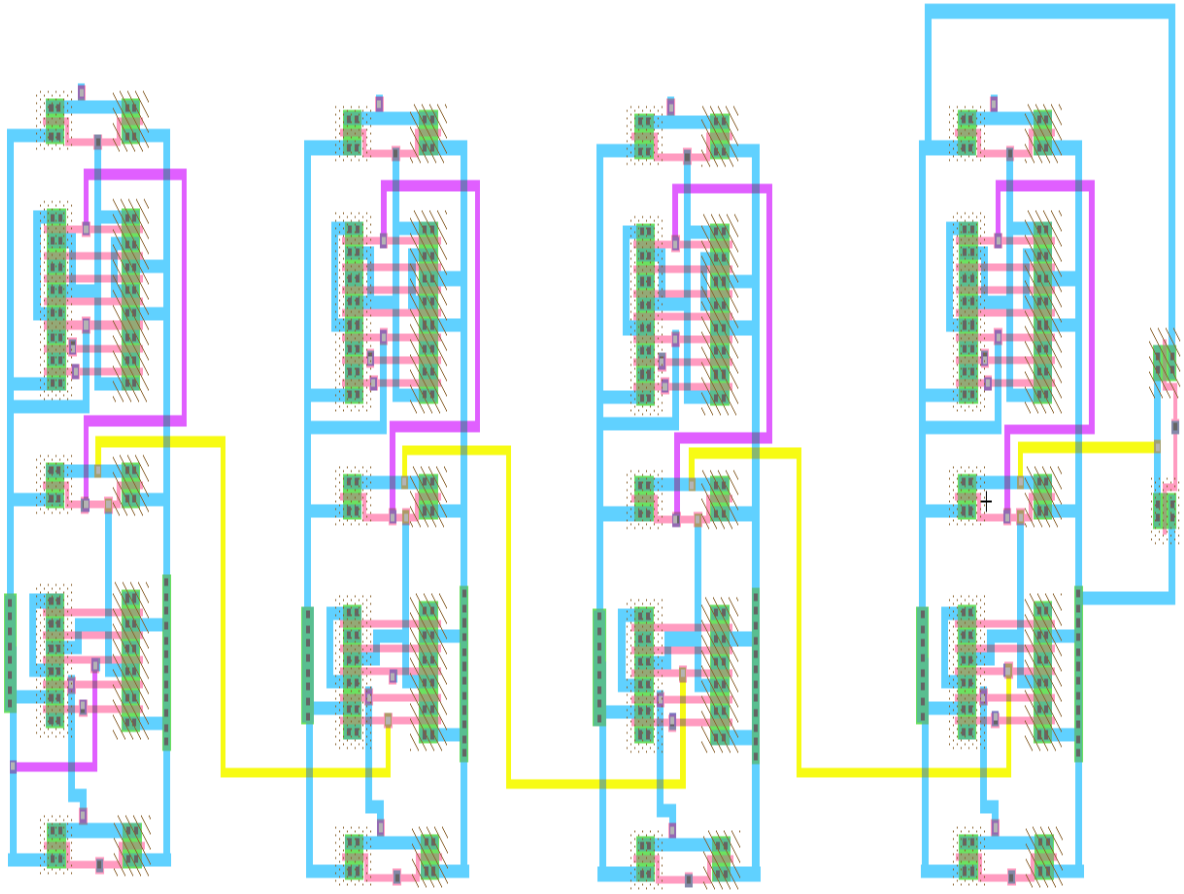

## 4 bit subtractor circuit (schematic):



1 bit subtractor circuit (layout):

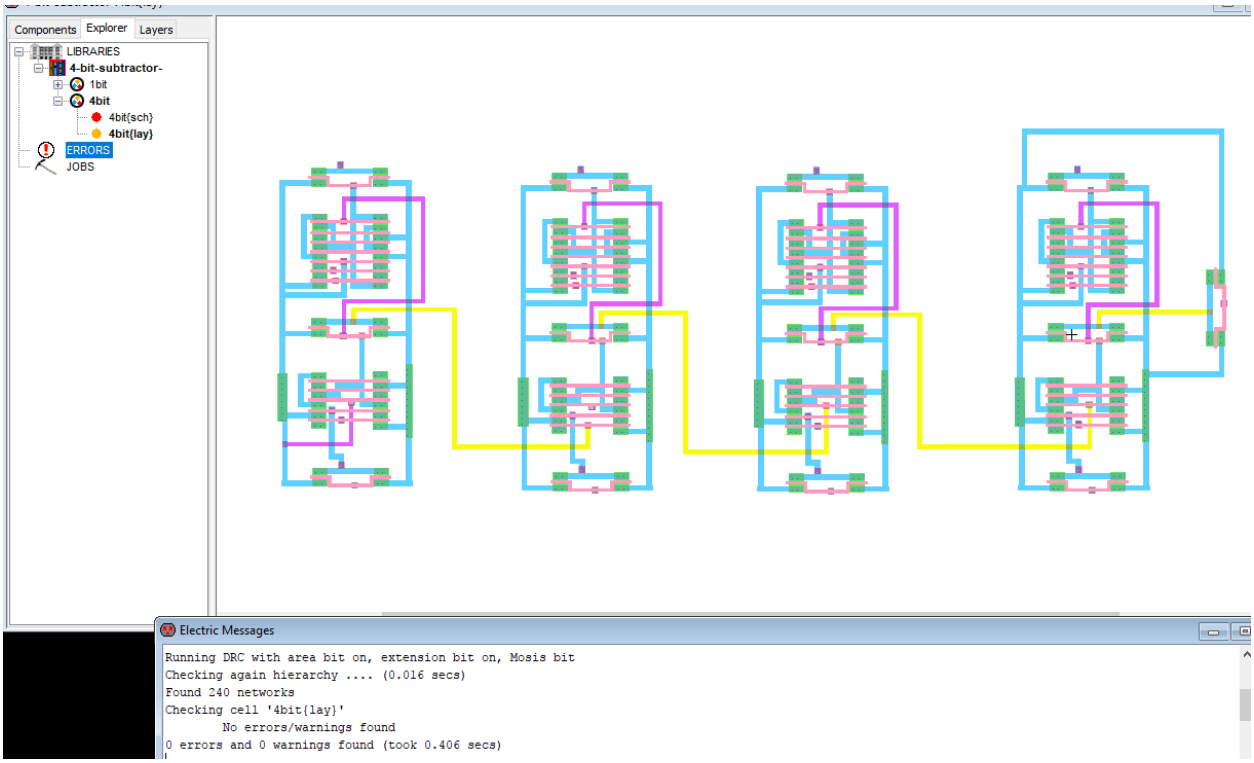


4 bit subtractor circuit (layout):

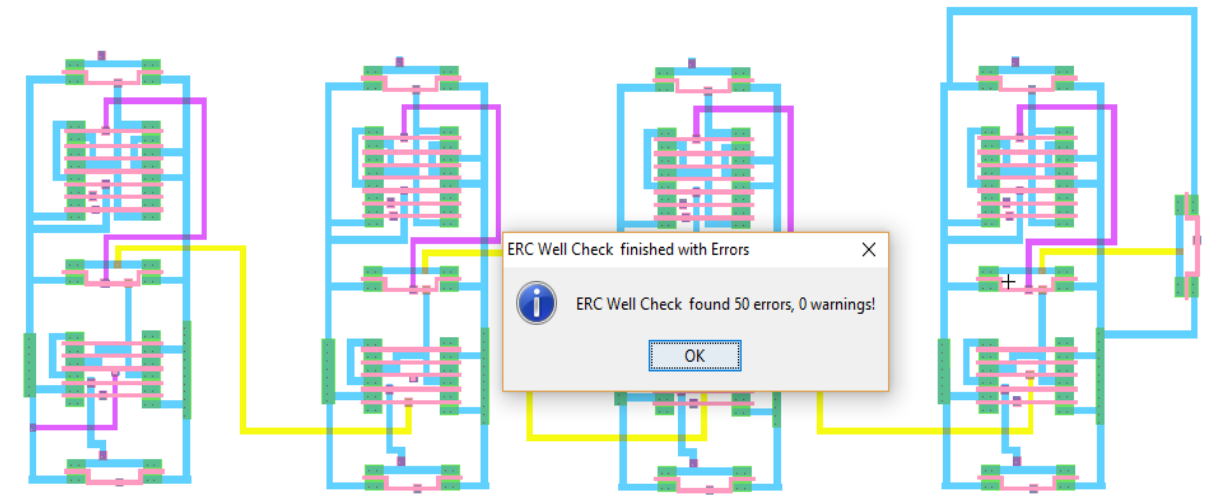


# ERROR CHECKINGS:

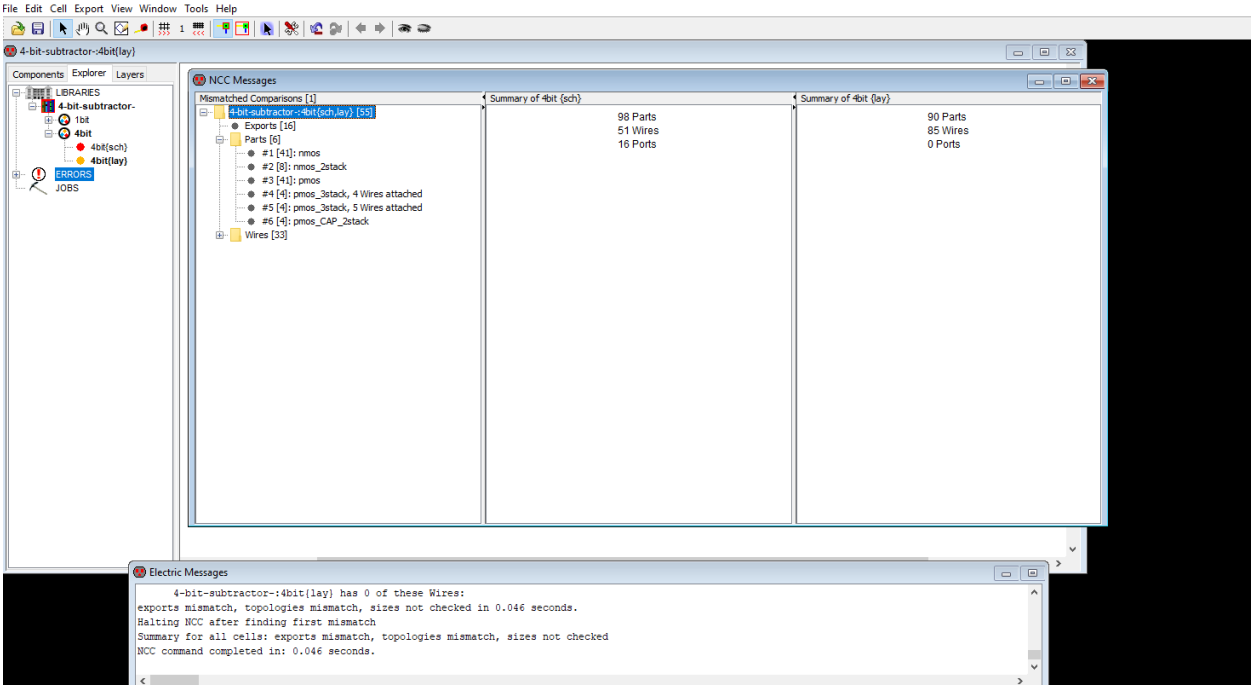
## DRC




## ERC



## NCC




## Conclusion:

At last we get our desire output where there is no error as we check for DCC. Both schematic and layout are working well. We have faced many problem and we have also overcome them and get our desire design. First, there was problem of drawing schematic design from logic gate design and then we design it and simplify the design with minimum number of transistors. Then draw it with the help of the software. After schematic part is done we move to the layout part and to design the layout part we draw a stick diagram for the schematic design. Then following the stick diagram we draw the layout. To draw it we have faces may problem like, there was showing spacing error between pMOS and nAct which causing error. Then we have change the space between them and make it error less and connect is step by step. After that we have face another problem with taking metal-2 and metal-3 though at the end we come up to take metal-2 and metal-3 and by using them we build our design. Another issue is that when we are taking carry out from first subtractor that time we saw EM problem and by taking differen metal we solve this problem. To take the metal we use metal via.