National University of Computer and Emerging Sciences, Lahore Campus

CS-2006 Operating system

Quiz: 6 Total-Marks:10

Sample: A

Q:1- **marks:5**

Use following page replacement algorithm and find out number of page faults for the following page reference string.

Consider 3 frames. 9, 5, 4, 2, 5, 8, 9, 1, 2, 4, 5, 5, 3, 8, 2, 5, 3, 2, 0

a. LRU (past)
b. FIFO
c. Optimal (future)
d. FIFO with frame size:4 (if there is any **beladay's anomly** exists? Explain your answer).

(a) LRU:

9 5 4 2 5 8 9 1 2 4 5 5 3 8 2 5 3 2 0

9 2 2 9 9 9 4 4 4 4 8 8 8 3 3
5 5 5 5 1 1 1 5 5 5 5 2 2 2 2
4 4 8 8 8 2 2 2 2 3 3 3 5 5 0

Page faults:- 34 = (16)

(b) FIFO:-

9 5 4 2 5 8 9 1 2 4 5 5 3 8 2 5 3 2 0

9 2 2 2 2 1 1 1 5 5 5 2 2 2 2 0
5 5 5 8 8 8 2 2 2 3 3 3 5 5 5 5
4 4 4 4 9 9 9 4 4 4 8 8 8 3 3 3

Page faults:- 3 = (16)

(c) Optimal:-

9 5 4 2 5 8 9 1 2 4 5 5 3 8 2 5 3 2 0

9 9 9 9 9 4 5 3 3 3 3 0
5 5 5 8 8 8 8 8 5 5 5 5
4 2 2 2 2 2 2 2 2 2 2 2 2

Page faults: 3 = (11)

(d) FIFO:
frame size = 4

9	5	4	2	5	8	9	1	2	4	5	5	3	8	2	5	3	2	0
9	8	8	8	8	8	5	5	5	5	5	0	0						
5	5	9	9	9	9	9	3	3	3	3								
4	4	4	1	1	1	1	1	8	8	8								
2	2	2	2	2	4	4	4	4	2	2								

Page faults :- 4 = (13)

Belady's anomaly states that if increasing in frame size of memory, there will be no decrement of page faults,

then more page faults
if more Free frame

In this Question with frame size = 3 page faults were 16 and by increasing frame size with = 4 page faults decrease with (13)

so there will not exist any Belady's anamoly.

Q:2- **marks:5**

Consider a process running on a system with a 52-bit CPU (i.e., virtual addresses are 52 bits in size). The system has a physical memory of 8GB. The page size in the system is 4KB, and the size of a page table entry is 4 bytes. The OS uses hierarchical paging. Which of the following statements is/are true? You can assume 2 10 = 1K, 2 20 = 1M, and so on.

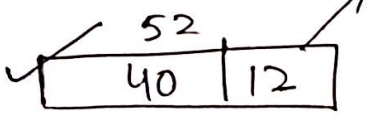
(a) We require a 4-level page table to keep track of the virtual address space of a process.

(b) We require a 5-level page table to keep track of the virtual address space of a process.

(c) The most significant 9 bits are used to index into the outermost page directory by the MMU during address translation.

(d) The most significant 40 bits of a virtual address denote the page number, and the least significant 12 bits denote the offset within a page.

Justify your answer by giving suitable explaination.

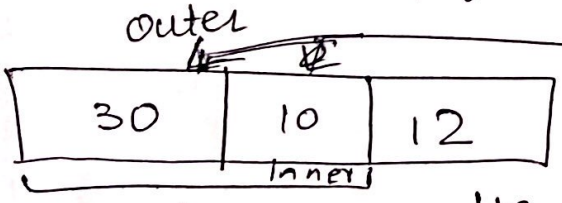


Page size = 4KB = $2^{2+10} = 2^{12}$

Page Table size = NP * PTES.

$2^{40} * 4$ bytes => 4TB.

outer level Page size = Page Table size / Page size = 4TB / 4KB = $\frac{2^{2+40}}{2^{12}} = 2^{42-12} = 2^{30}$



40 - 30 = inner Bits.