SCREAM I: a single mask, single-crystal silicon, reactive ion etching process for microelectromechanical structures

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Abstract

A single-crystal silicon, high aspect ratio, low-temperature process sequence for the fabrication of suspended microelectromechanical structures (MEMS) using a single lithography step and reactive ion etching (RIE) is presented The process is called SCREAM I (single-crystal reactive etching and metallization) SCREAM I is a bulk micromachining process that uses RIE of a silicon substrate to fabricate suspended movable single-crystal silicon (SCS) beam structures Beam elements with aspect ratios of 10 to 1 and widths ranging from 0 5 to 4 0 μm have been fabricated All process steps are low temperature (<300 °C), and only conventional silicon fabrication tools are used photolithography, RIE, MIE, plasma-enhanced chemical-vapor deposition (PECVD) and sputter deposition SCREAM I is a self-aligned process and uses a single lithography step to define beams and structures simultaneously as well as all necessary contact pads, electrical interconnects and lateral capacitors SCREAM I has been specifically designed for integration with standard integrated circuit (IC) processes, so MEM devices can be fabricated adjacent to prefabricated analog and digital circuitry In this paper we present process parameters for the fabrication of discrete SCREAM I devices We also discuss mask design rules and show micrographs of fabricated devices

Introduction

Silicon micromechanical structures are generally fabricated using two approaches surface micromachining and bulk micromachining In surface micromachining, the silicon substrate is used as a foundation and alternating layers of polycrystalline silicon (polysilicon) and SiO_2 (oxide) are deposited, the oxide is selectively removed and the remaining patterned polysilicon is the mechanical structure In bulk micromachining, the single-crystal silicon (SCS) substrate is etched away to leave the structure Bulk micromachining has typically been done using wet chemistry This paper discusses bulk micromachining using reactive ion etching (RIE) processes

Initial research into surface micromachining showed the viability of microelectromechanical (MEM) systems MEM structures, including moving motors, gears and accelerometers, have been fabricated and tested [1–5] Surface micromachining relies on chemical-vapor deposition (CVD) to form the alternating layers of oxide and polysilicon Significant freedom in device design is allowed using this technology However, it is difficult to produce thick films, polysilicon film thicknesses reported in the literature are typically 2 0 μm [1–3] This limited structure thickness results in three constraints (1) lower lateral capacitance, (2) increased proportion of lateral fringing capacitance, and (3) increased out-of-plane motion

The wet chemistry needed to remove the interleaved oxide layers can be problematical, as well. The structures are made of polycrystalline silicon with inherently poorer electronic and mechanical properties than single-crystalline silicon, including reduced carrier mobility and interface properties, higher defect densities, reduced mechanical strength, etc The high temperature ($\approx$950 °C), needed to anneal stress properly from the polysilicon and oxide layers complicates the integration of these devices with standard CMOS fabrication, where post-metallization temperatures greater than $\approx$400 °C are generally inacceptable

Bulk micromachining has generally been achieved through anisotropic wet chemical etches [4, 5] These chemistries etch faster in certain crystallographic planes of silicon [6–8] The structural shapes can be controlled by biasing the mask design, by choice of wafer orientation, and by heavy dopant implantation (which is an etch-stop) [6] Such etches are difficult to control for submicron dimensions or for vertical high-aspect-ratio devices, they are instead used for through-wafer etches Bulk micromachining using wet chemistry is

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currently applied to through-wafer etches for commercial accelerometers and pressure sensors

SCREAM and SCREAM I processes are dry bulk micromachining processes, using reactive ion etching (RIE) to pattern and release structures [9,10] SCREAM I is an enhancement of SCREAM [11,12] SCREAM requires two masks to fabricate suspended and movable structures With SCREAM I, we have increased the structural depth (10–20 μm), and removed the second lithography step This simplification was made possible by use of a self-aligned-metallization approach where a single layer of patterned oxide is used to pattern all etches and depositions, up to and including metallization

Applications

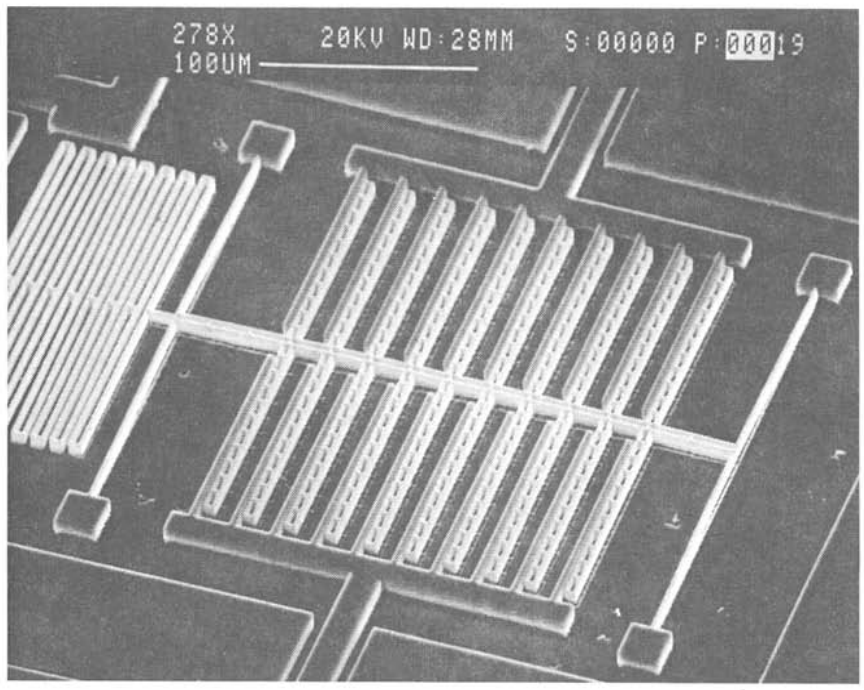
SCREAM I is ideally suited for the fabrication of high-aspect-ratio single-crystal silicon beams Nominal dimensions for SCREAM I beams are listed in Table 1

A simple application of the SCREAM I process is the fabrication of a lateral accelerometer, as shown in Fig 1 [13] Simple fixed–fixed restoring springs are used to suspend a released mass The mass is a set of released beams The sidewalls of the beam structures are nearly vertical with less than 2 5% widening from top to bottom A 1 μm separation between sidewall capacitor plates can be achieved The large laterally opposed surface areas between fixed and released beams result in relatively large capacitances ($\approx$3 pF) and relatively large forces ($\approx$35 μN at 5 V and 1 μm separation) Motion of the mass is detected by measuring the variation in lateral capacitance Acceleration of the device along the axis of measurement causes (to the first order) a linear displacement scaled only by the ratio of the released mass to the lateral spring constant This accelerometer device is typical of the MEM devices that can be fabricated with SCREAM I

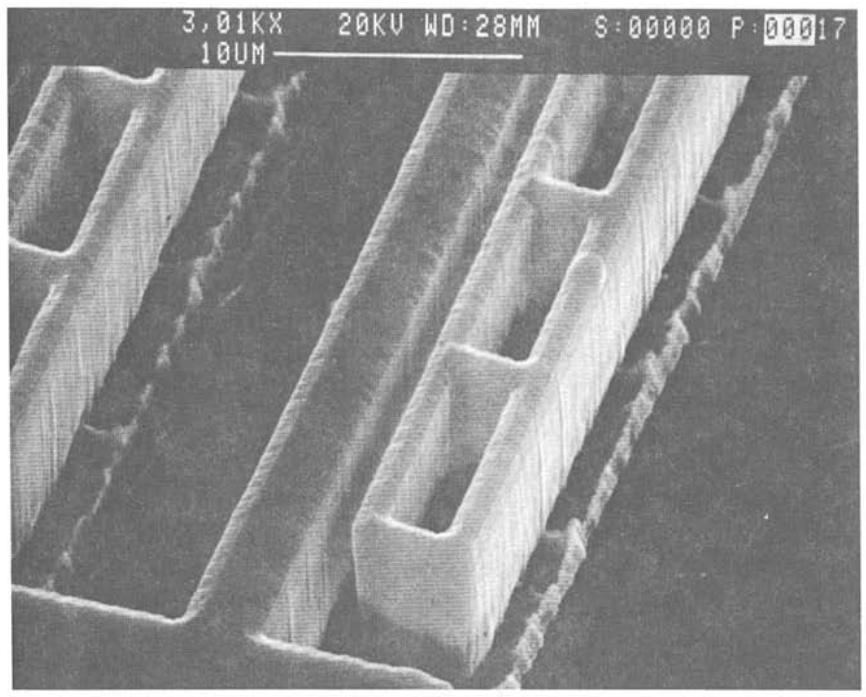
The high aspect ratio of SCREAM I devices allows increased isolation from out-of-plane modes of vibration For the accelerometer device, we want to measure the acceleration along a single measurement axis Any out-of-plane motion would also cause a change in capacitance, and produce an acceleration error The amount

TABLE 1 Typical SCREAM I beam-structure dimensions

	Maximum	Minimum	Typical
Beam height (μm)	20	2	10
Silicon beam width (μm)	5	0 5	0 5
Total beam width (μm)	6	1 0	1 5
Aspect ratio	10 1	0 5 1	6 6 1



(a)



(b)

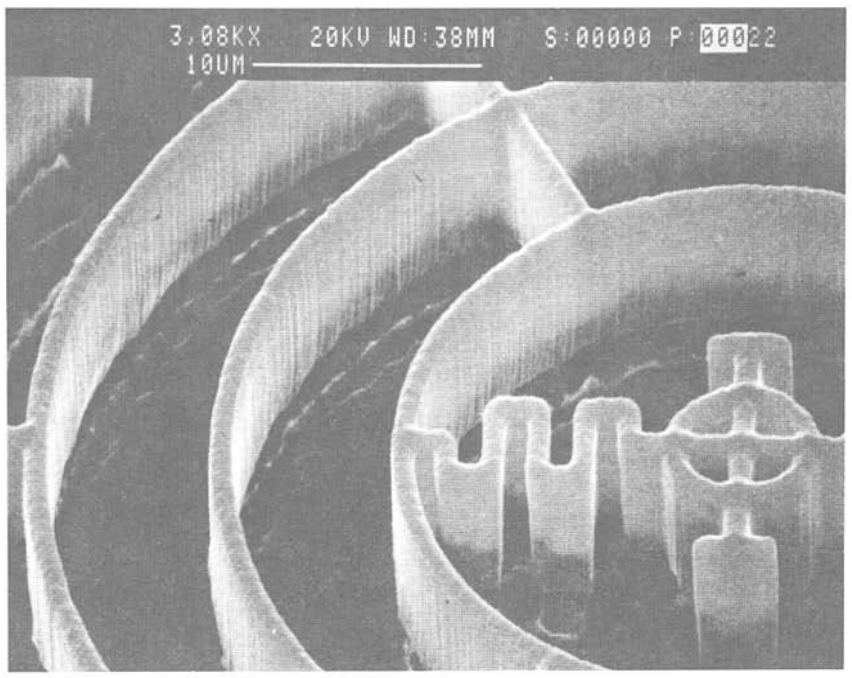
Fig 1 Scanning electron micrograph (SEM) of SCREAM I lateral accelerometer (b) is a close up of (a)

of in-plane and out-of-plane motion is controlled by the spring constant, which is proportional to the third power of the beam width in the direction of motion (for small displacements) The ratio of the out-of-plane spring constant to the in-plane spring constant for a beam with a 10 1 aspect ratio would be 1 1000

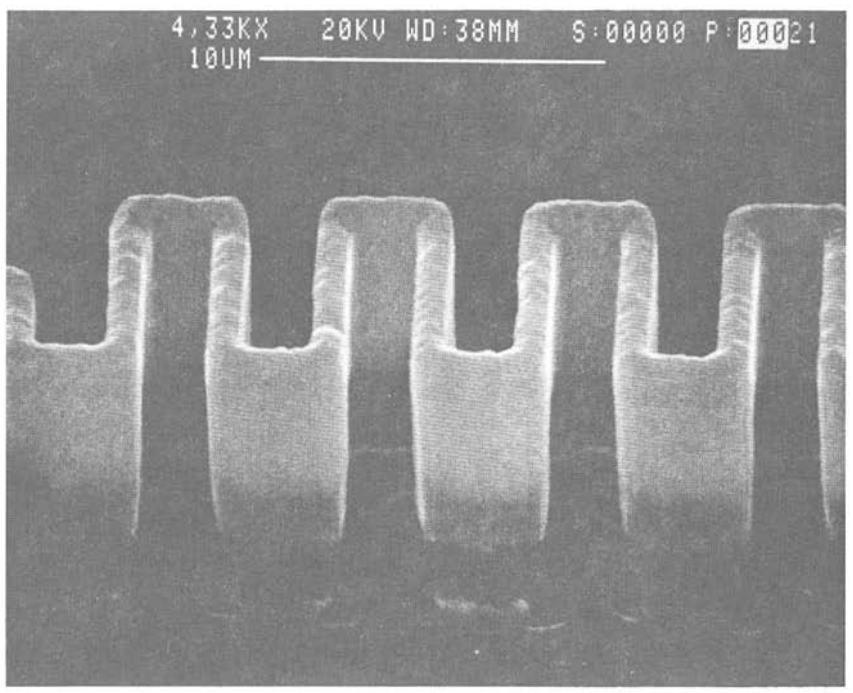
SCREAM I process outline

Sample structures produced using the SCREAM I process are shown in Fig 2 The process is outlined in Table 2 and Fig 3

We start with a clean silicon wafer of arbitrary orientation We used both ⟨100⟩ and ⟨111⟩ wafers and highly doped n-type arsenic and moderately doped p-type boron wafers The SCREAM I process is inde-



(a)



(b)

Fig 2 SEM of SCREAM I fabricated structures (a) shows circular x–y resonator and (b) shows folded springs Note vertical sidewalls and conformal aluminum sputter deposition

TABLE 2 Outline of SCREAM I process flow

Step number		Description
1	Mask oxide	PECVD (1–2 μm)
2	Photolithography	Transfer pattern
3	Pattern transfer	CHF_3MIE
4	Resist removal	O_2 plasma
5	Trench etch #1	Cl_2 RIE
6	Sidewall oxide deposition	PECVD (0 3 μm)
7	Clear floor oxide	CF_4 RIE
8	Trench etch #2	Cl_2 RIE
9	Release	SF_6 RIE
10	Sputter metal	Aluminum
11	Wire bond	

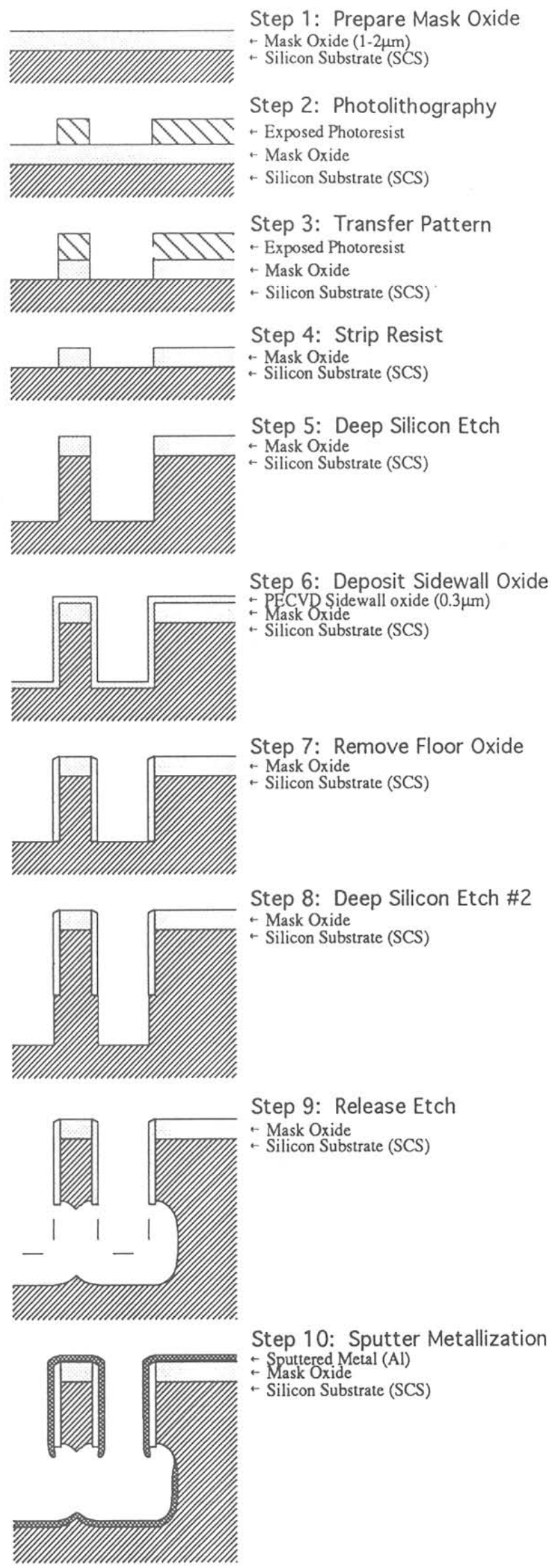


Fig 3 SCREAM I process outline Cross section of a typical beam made using the SCREAM I process These Figures show a beam and the associated capacitor plate The released beam moves laterally, while the plate on the right is static and can be used to measure the motion of the beam

pendent of crystal orientation, doping level and doping type for these samples

Step 1 deposit mask oxide

We deposit a layer of oxide that will serve as the mask throughout the process sequence PECVD oxide is used because of the high deposition rate and low deposition temperature A standard PECVD oxide recipe runs at 240 °C (IPE System 1000 PECVD)

Step 2 photolithography

Optical resist is spun, exposed and developed (KTI 8951 16 5cs positive photoresist with KTI 875 photoresist developer, GCA/Mann DSW 6100B photolithographic stepper, numerical aperture of 0 42 and minimum resolution of 0 5 μm)

Step 3 pattern transfer

The pattern is transferred from the resist to the mask oxide using CHF_3 magnetron ion etching (MIE) at ≈ 3 mTorr (MRC-720 Magnetron Ion Etcher)

Step 4 resist strip

A standard O_2 plasma strip is used

Step 5 deep silicon etch

The mask oxide is then used to transfer the pattern into the substrate A deep, vertical (anisotropic) BCl_3/Cl_2 RIE is used (Table 3) [9] Depending on the structure height, the trench may be from 4 to 20 μm deep Typical etch time is 45 min

The deep silicon trench etch is the most critical step in the process Experimental results have indicated this trench etch step to be stable and reliable with fairly wide process windows It has been found, however, that chamber cleanliness is important, since residual materials (from other users) have been found to deposit on the sidewalls of the trench during the etch process

TABLE 3 Process parameters for silicon trench etches (Steps 5 and 8)

Parameter	Step 1	Step 2	Step 3
Power	200 V	300 V	475 V
Pressure	20 mTorr	20 mTorr	40 mTorr
Time	1 min	1 min	(user defined)
Chemistry			
Cl_2	0 sccm	2 sccm	50 sccm
BCl_3	14 sccm	14 sccm	5 sccm
H_2	7 sccm	7 sccm	0 sccm
Etch rate Si	1900 Å/min = 11 4 μm/h		
Etch rate SiO_2	96 Å/min = 0 576 μm/h		
Selectivity	20 1 for silicon oxide		
Tool	PlasmaTherm PK-1250 parallel plate RIE		

Step 6 sidewall oxide deposition

A conformal layer of PECVD oxide is applied The oxide protects the sidewall during release and is $\approx 0\,3$ μm thick A thinner sidewall oxide may be used if improved aspect ratio is needed

The purpose of Steps 6–9 is to protect the top and sides of the silicon beams, to expose the substrate floor around the beam, to remove the silicon from under the beam and to produce beams released and suspended over the substrate Figure 3, Step 9 shows a cross section of the released beam The dashed lines in the Figure show the extent of the trench floor before the release etch

Thus, Step 6 forms the sidewall layer and deposits oxide in the trench bottom The trench bottom must be cleared for the release and the sidewall oxide must be left intact, we use an anisotropic oxide etch

Step 7 remove floor oxide

We use a CF_4/O_2 RIE at 10 mT (Table 4) This etch will remove 0 3 μm of oxide from the mesa top and from the trench bottom The etch will leave the sidewall oxide largely undisturbed, except for faceting of the mask oxide corners

Step 8 deep silicon etch #2

Before the release, we use a deep silicon RIE to etch down another 3–5 μm below the lower edge of the sidewall oxide This etch exposes 3–5 μm of silicon underneath and on each side of the beams The exposed silicon under the beams is to be removed during the release Refer to Table 3 for parameters Typical etch time is 15 min

Step 9 isotropic release etch

The release is an isotropic SF_6 RIE at 90 mT (Table 5) The etch removes the silicon under the beams, leaving them suspended over the substrate The SF_6 chemistry is highly selective to oxide, several microns

TABLE 4 CF_4 RIE parameters (Step 7)

Parameter	Value
Tool	PlasmaTherm System 72 parallel plate RIE
Power	75 W
Pressure	10 mTorr
Chemistry	
CF_4	21 sccm
O_2	5 sccm
Power density	0 128 W/cm^2
Time	16 min
Etch rate	160 Å/min

TABLE 5 SF_6 RIE parameters (Step 9)

Parameter	Value
Power	50 W
Pressure	90 mTorr
Chemistry	
SF_6	100 sccm
O_2	8 sccm
Power density	0 085 W/cm^2
Time	20 min
Etch rate Si	1130 Å/min = 6 8 μm/h
Etch rate SiO_2	3 Å/min
Selectivity	≈300 1

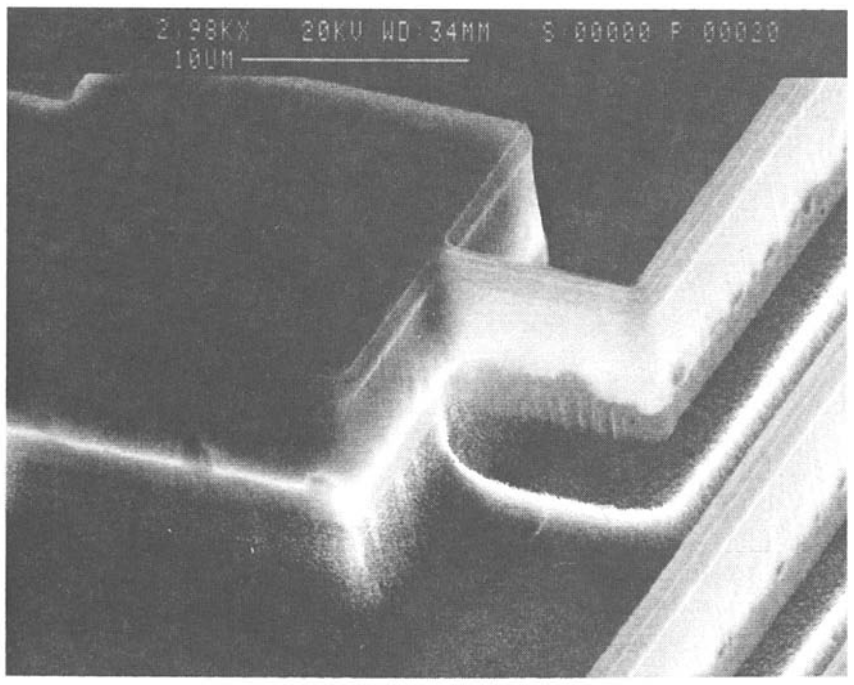


Fig 4 SEM of SCREAM I cantilevered beam after the release etch (Step 9) and before metallization

TABLE 6 Aluminum sputter deposition parameters (Step 10)

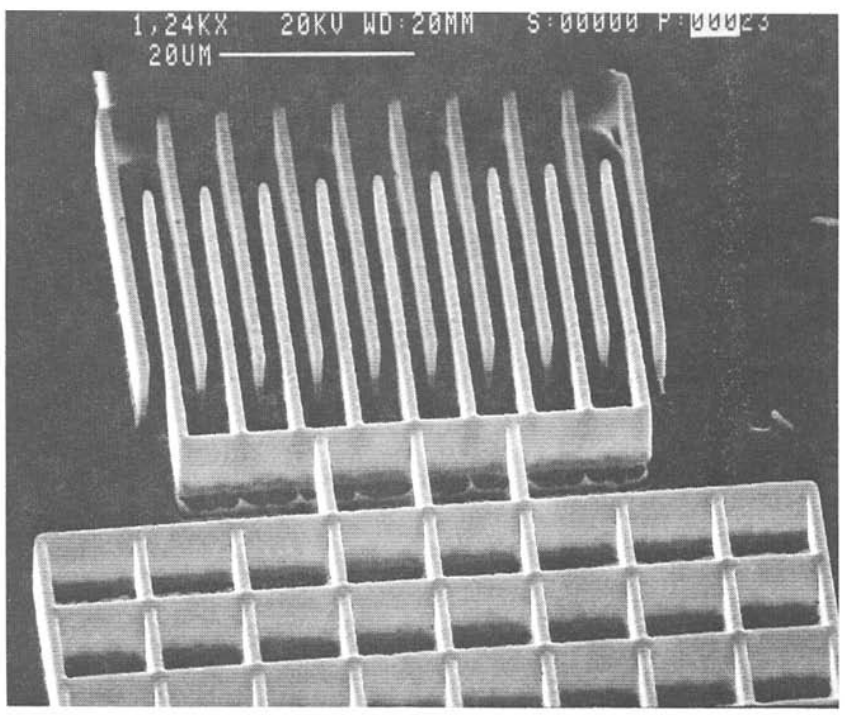
Parameter	Value
Deposition pressure	25 mTorr
Chemistry	
Ar	40 sccm
Regulation	current controlled
Required current	5 A
Rotation	yes
Nominal voltage	312 V
Nominal power	1 51 kW
Deposition rate	70 Å/min
Pre-sputter time	20 min
Sputter time	40 min
Nominal film thickness	3000 Å
Target type	8 in aluminum

of silicon are etched with only nominal erosion of the protective oxide coating Figure 4 shows a serpentine beam, anchored by a fixed pad, after the release etch and before the metallization step Note the undercut of the oxide sidewall, this overhang will support the metallization layer and prevent it from electrically shorting to the exposed silicon underneath the beam

The released structure has a core of SCS and a conformal oxide coating surrounding it The structural elements are suspended at the corners and are free-floating in the center The beams are next covered with an isolated metal layer to form the capacitor drive electrodes

Step 10 metal sputter deposition

We sputter deposit an aluminum layer (Table 6) See Fig 5 for an SEM of two completed SCREAM I structures Note that aluminum sputter metallization appears to be very uniform on the sidewalls, this may allow the use of thinner sidewall metal films (1000 Å) than are listed in Table 6 (3000 Å)



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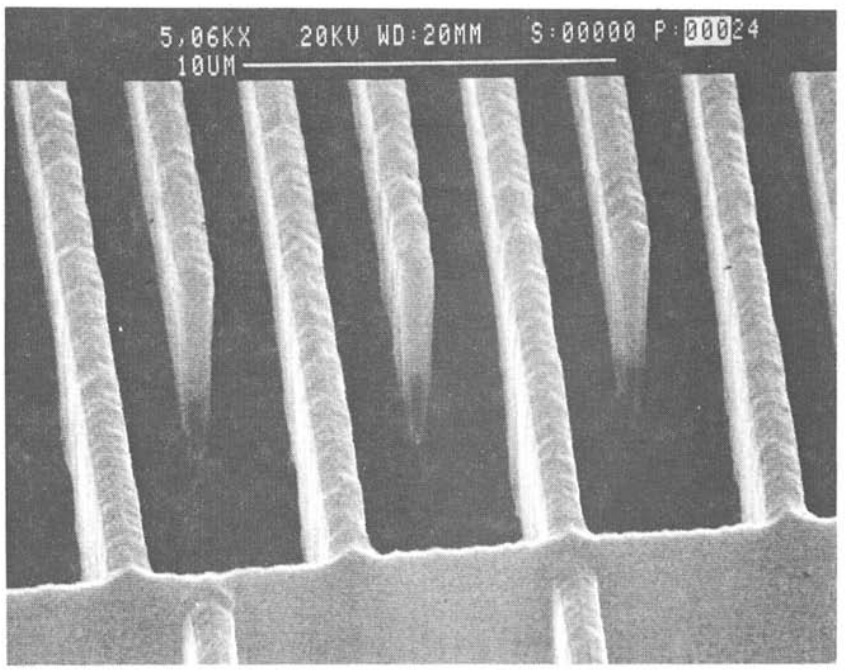

(b)

Fig 5 SEM of SCREAM I interdigitated finger capacitors (a) is an overview of finger capacitors structures and (b) is close-up of (a)

The structures are now completed and may be wire-bonded for testing and measurement It may be desirable to add a thin passivation oxide layer (50 nm) to prevent shorting between moving electrodes The CF_4 anisotropic RIE (Step 7) could be used to remove anisotropically only the oxide on the mesa top (and trench bottom) while leaving the sidewall oxide intact This allows us to wire bond to the contact pads (now cleared of oxide) and to retain the dielectric insulation of the capacitor plates (still covered with oxide) Silicon nitride could equally well be used for capacitor plate isolation

SCREAM I: mask design rules

To design a single-mask MEM device with the SCREAM I process, some design rules should be followed

Mask oxide thickness is a critical parameter, it protects the silicon beams throughout the process A typical recommended initial thickness is 2 5 μm for 10 μm tall beams Note that faceting will occur on the mask edges as a result of the high d c bias from the Cl_2 RIE (Steps 5 and 8) If a sufficiently thick mask oxide is *not* prepared, this faceting will thin the mask oxide at the edges and may cause beam damage during release

We have limited ourselves to a single layer of metal Process outlines for multi-level design have been published [11]

Every isolated set of electrical interconnects, contact pads and capacitive plates must be surrounded by a trench This trench serves simultaneously to isolate the individual conductors and to pattern the self-aligned metal The recessed sidewall undercut of the trench disconnects the semi-conformal deposited metal from structure to structure and from structure to substrate This isolation allows us to define multiple interconnects without additional masks

Released beams in a device should generally be of the same width Narrow beams may release faster and the underside may continue to etch during the time needed for thicker beams to release The second Cl_2 RIE (Step 8) was added specifically to minimize this effect, by increasing the exposed sidewall silicon during the release etch and shortening release times see ref 11 for a more complete discussion

Released beams should be narrow (generally less than 5 μm) and should be narrower than the beams not intended for release Mechanical interconnects, the beams used to support electrical interconnects, are generally not released and can be made 10 μm wide Anchors used to support the ends of the fixed–fixed restoring springs should also be a minimum of 10 μm $\times$ 10 μm in size

Note, however, that where die area must be minimized (such as the fixed capacitive fingers shown in Fig 1) beams may be narrowed further, provided there is some anchor point that will hold them firm An example of this is shown in Fig 1(b), where the fixed solid beam (on the left) is made only 3 μm wide and may have released from the substrate, however, since the beam is short (100 μm) and is held firmly in place by an anchor, lateral motion of this fixed beam is limited

Figure 6 is the top view of a cell for a simple single-beam cantilevered MEM device There are three contact pads, three electrical interconnects and two side-drive electrodes Note the trench, the hatched lines in the Figure, around each of the three isolated interconnects, this trench isolates each electrical interconnect and is in fact the only part exposed while patterning the device (Step 2)

In Fig 7, the cross section for one of the interconnects is illustrated (i e , the cross section marked AA′ in Fig 6) The SCREAM I process defines and isolates the metal layers without the need for etch back Thus, photolithography is normally not required to etch back metal and define interconnects in the SCREAM I

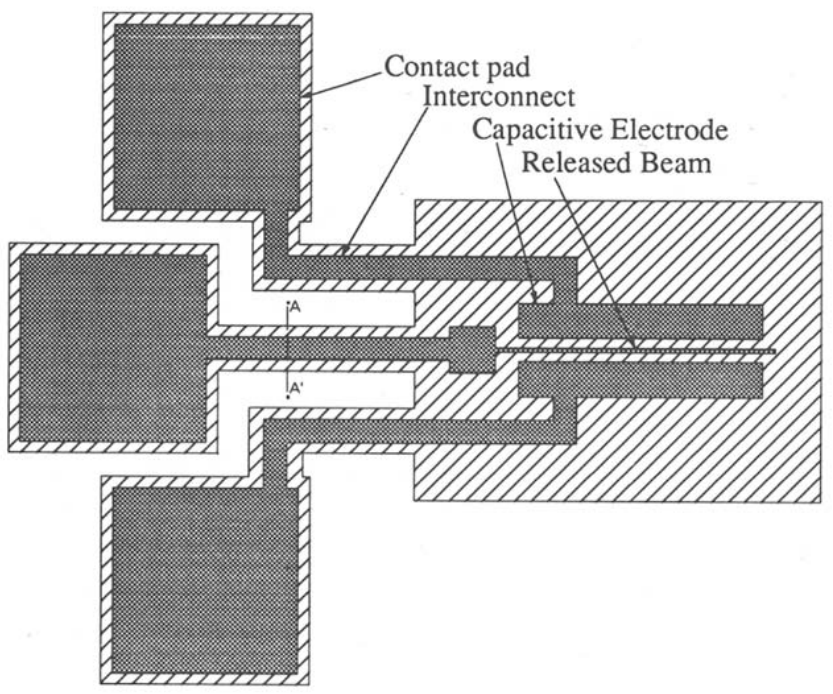

Fig 6 Top view of a simple MEM device The cantilevered beam is the thin beam between the two capacitive electrodes The upper and lower electrodes allow one to either drive or sense the motion of the beam The gray areas represent the contacts, interconnects and beams, while the hatched area represents the trench that surrounds and isolates the MEM device

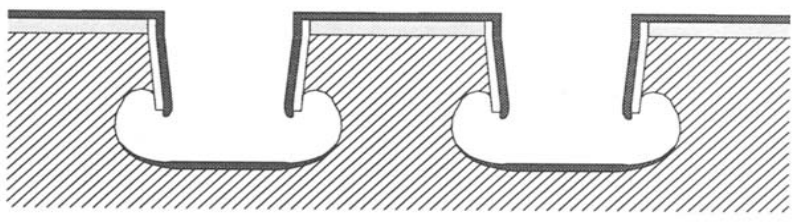

Fig 7 Cross section of an interconnect, i e , the line AA′ in Fig 6 The interconnect is the gray metal layer on the mushroom-shaped object in the center of the picture The white layer under the metal is an insulating layer of silicon dioxide

process The oxide layer under the metal isolates the metal from the substrate, and the overhanging oxide prevents the sidewall metal on the beams from contacting with the substrate

SCREAM I results and discussion

Structural elements have been fabricated that are several microns tall (4–20 μm), have approximately vertical sides and have a thin ($\approx$0 3 μm) layer of metal covering the top and sides of the structures The oxide layer between the metal and substrate is an insulating dielectric and supports applied voltages up to 80 V without metal-to-substrate oxide failure

We use sputter-deposited metal on the sidewall of parallel beams as parallel-plate capacitors Sidewall capacitors can be made 4–20 μm tall, with 1–2 μm of interplate spacing, and several millimetres in length, as a result, large capacitances can be generated We have built suspended structures with a lateral capacitance of $\approx$3 pF Figure 1 shows a lateral capacitor device where the gap spacing is approximately 1 μm and the beam length is 100 μm, there are 20 beams [13]

One of the significant benefits of the SCREAM I process is the sidewall height Surface micromachining processes are generally limited to polysilicon thicknesses $\approx$2 μm SCREAM I allows 10–20 μm of structure height This increased sidewall height has important implications for lateral sensor and actuator devices Three points are listed

(1) Larger capacitance Capacitance scales linearly with capacitor plate height, i e , sidewall height Capacitance is generally the scaling factor used to determine displacement (for a given voltage) in actuators, and to determine sensitivity (for a given plate separation) in sensors Larger sidewall capacitance facilitates operation of both devices SCREAM I devices will have five to ten times the lateral capacitance of surface micromachined devices with similar cell size This increased capacitance per unit beam length can be used either for improved device parameters, or to make the SCREAM I device five to ten times smaller than a surface micromachined device of equivalent capacitance

(2) Non-linear capacitance The ratio of fringing capacitance to parallel-plate capacitance is determined by the ratio of sidewall height to interplate distance The larger the ratio, the less influence fringing capacitance has in determining the total capacitance Fringing capacitance is non-linear and as such complicates device design, operation and measurement [9] Surface micromachined devices typically have height-to-separation ratios of 1–2 to 1, SCREAM I devices have height-to-separation ratios of 5–10 to 1

(3) Out-of-plane mode attenuation Out-of-plane motion will be perceived by lateral sensors as a change in lateral capacitance If the sensor is meant to be sensitive only to lateral motion, this out-of-plane motion will cause measurement errors High-aspect-ratio beams provide an attractive solution, they inhibit out-of-plane motion while permitting lateral motion SCREAM I devices have vertical-to-lateral spring-constant ratios of 1000 to 1

With regard to metal deposition, we use an 8 inch diameter metal target for sputter deposition of the sidewall metal for these capacitor plates Sputter deposition is semi-conformal and will deposit laterally on the sidewalls, but will not deposit underneath the beams on the exposed underside silicon of the structures (see Fig 3, step 10) Thus, we find that the metal hangs down at the bottom edge of the beams This overhang is beneficial because it ensures that the metal on top of the structures does not electrically contact with the silicon substrate, which is left bare under the structure by the isotropic release etch This overhanging metal and the isolation of it from the substrate facilitates integration with VLSI

Conclusions

SCREAM I is the core process sequence of a larger family of dry bulk micromachining processes Other related processes have been published concerning increased device mass, decreased lateral spring constant, multi-level metallization, and IC integration [13]

We have presented a low-temperature process for fabricating single-crystal silicon micromechanical structures The process, called SCREAM I (single-crystal reactive etching and metallization), uses conventional fabrication tools Using optical lithography with a single mask, all mechanical beam structures, electrical interconnects and bonding pads are defined All subsequent steps are self aligned and require only a single metallization layer Each step is low temperature ($<$300 °C) and can therefore be carried out adjacent to prefabricated analog and digital circuitry SCREAM I beams are 0 5–4 μm wide with aspect ratios greater than 10

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