EE 501 Analog IC Design

- **Instructor Contact Information**
  - **Name: Degang Chen**
  - **Office: 2134 Coover Hall**
  - **Email: djchen@iastate.edu**
  - **Phone: 294-6277**
  - **Office Hour: MW 3:30 – 5:00 pm**
    Or any other time convenient to you
  - Please include "EE501" in the subject line in all email communications to avoid auto-deleting or junk-filtering

EE 501 Analog IC Design

- **TA Contact Information**
  - **TA:**
    - **Name: Mr. Yulong Shi**
    - **Office: 3102 Coover Hall**
    - **Phone:** 701 306 5095
    - **Email: yulong@iastate.edu**
    - **Office hour to be announced**
  - **Yulong will help you with the Lab and the projects**
  - **Senior graduate students in Coover 3102 and 3104 may also offer help with your Cadence simulation.**

EE 501 Analog IC Design

- **Student Introduction**
  - **Email TA and me your contact information**
    - **For us to contact you if necessary**
  - **Brief intro**
    - **Name**
    - **Advisor**
    - **Area**
    - **Interest**
    - **IC design experience**
    - **Cadence experience**
  - **Study / lab / project partners**

Class Webpage

- http://class.ece.iastate.edu/djchen/ee501/2011
- Blackboard for video recordings
- Please check the page for
  - Any announcement
  - Class notes
  - HW assignments
  - Lab assignments
  - Project requirements
  - Class policy and other info

Student behavior expectations

- Full attendance except with prior-notified excuses
- On-time arrival
- Active participation
  - Ask questions
  - Answer questions from instructor or students
- Be cordial/considerate to other students and TA
- Help each other
- Promptly report/share problems/issues
  - Email csg@iastate.edu, cc TA and me, stating you are working on a lab, and describing the issue

Prohibited behaviors

- Any foul language or gesture
- Comments to other students that are discriminatory in any form
- Any harassments as defined by the university
- Academic dishonesty

- No alcohol, drugs, or any other illegal / improper substances

Accommodation/Assistance

- Please let me know if you
  - Have any special needs
  - Have disability in any form
  - Have any medical/mental/emergency conditions
  - Have field trips / interviews
  - Have special requests
  - Want me to adjust lecture contents/pace
- Can also consult me if you
  - Would like to seek advice on any professional or personal issues
  - Would like to have certain confidential discussions

Course Description

- Design techniques for analog and mixed-signal VLSI circuits.
- Amplifiers: operational amplifiers, transconductance amplifiers, finite gain amplifiers and current amplifiers.
- Linear building block: differential amplifiers, current mirrors, references, cascoding and buffering.
- Performance characterization of linear integrated circuits: offset, noise, sensitivity and stability.
- Layout considerations, simulation, yield and modeling for high-performance linear integrated circuits.
- CAD tools: Cadence.

Course Objectives

- Understand fundamental concepts related to sources of non-idealities, matching, noise, nonlinearities, and stability.
- Design and analyze key building blocks.
- Design and analyze multistage op amps for low voltage, low power, high gain, and high speed applications.
- Experience floor planning, analog layout, corner simulation, yield assessment, design for test, and test planning.

Prerequisite by topics

- Proficiency and fluency in using Cadence, Synopsis, and other IC design and simulation tools
- Knowledge of basic amplifier structures, their large signal and small signal analysis, and computation of their gain, bandwidth, impedance and so on.
- Knowledge of how transistors work, including various operation regions.
- Knowledge of signals and systems, including poles, zeros, transfer functions, frequency response, transient response, stability, phase margins, and so on.
- Knowledge of semiconductor fabrication and how transistors, resistors, capacitors, diodes, etc. are made.
- Knowledge of probability, random variable, pdf’s, noise, signal to noise ratio, noise transfer, and so on.

Final Grade Weighting

- Laboratory: 25%
- Design projects: 20% each
- Homework: 15%
- One or two Exams: 20% total
- Bonus for
  - Classroom participation: 5%
  - Original creative work (publishable/patentable work)

Final Grade Scale

- A: 95%+
- A – : 90 – 95%
- B+: 85 – 90%
- B: 80 – 85%
- NR: <80%, unless requested
  - » If requested, the same trend follows: 5% for each grade notch

Fabrication Privilege

- Circuit fabrication is not required for the course
- It is offered free as a privilege
- Requirements for this privilege
  - Detailed simulation results demonstrating that circuit is highly likely to work
  - Sufficient testing plan (what to measure and how)
  - Promise to test (availability and commitment of time)
  - Register in ee599CD and submit a report to MOSIS
- Benefits:
  - Valuable experience
  - Increased marketability
  - Get one or two credits for fabrication and testing
- Limits: max two submissions per student

Two Alternative Ways to Get A

- Successful design of both projects
  - Both show A-level performance in schematic and post layout simulation, as well as well-thought-out layout
  - At least one project successfully fabricated and satisfactorily tested
- Nontrivial originally contribution
  - Accepted technical paper to a decent conference and/or journal
  - Paper deemed at similar level by Instructor

Collaboration and helping each other

- For tasks intended for group work, you are expected to find a partner and share the tasks among the group members. In a group project, effective teamwork is critical to maximize the productivity of the whole group. In the submitted work, identify components and indicate percentage contribution by each member to each component.
- For tasks not intended for group work, individual submission is required. In this case, you are encouraged to discuss among your friends on how to attack problems. However, you should write your own solution. Copying other people’s work is strictly prohibited.

Academic dishonesty

- Cheating is a very serious offense. It will be dealt with in the most severe manner allowable under University regulations. If caught cheating, you can expect a failing grade and initiation of a cheating case in the University system.
- Basically, it’s an insult to the instructor, the department and major program, and most importantly, to the person doing the cheating. Just don't.
- If in doubt about what might constitute cheating, send e-mail to your instructor describing the situation. If you notice anyone cheating, please report it to the instructor or the TA. Do not deal with it yourself.

Discrimination

- State and Federal laws as well as Iowa State University policies prohibit any form of discrimination on the basis of race, color, age, religion, national origin, sexual orientation, gender identity, sex, marital status, disability, or status as a U.S. veteran. Language or gestures of discriminatory nature will not be tolerated. Severe cases will be reported to appropriate offices. See ISU policies at http://www.hrs.iastate.edu/hrs/files/reaffirmation.pdf
- Let us make every effort to work together and create a positive, collegial, caring, and all-supportive learning environment in our classroom, laboratory, TA office, and instructor office.

Disability accommodation

- Individuals with physical or mental impairments who are otherwise qualified to perform their work or pursue their studies may request reasonable accommodations to enable them to work or continue their studies.
- If you believe you have learning disability, you must contact Student Disability Resources at the Academic Success Center to initiate the accommodation process.

Religion based conflict

- Iowa State University welcomes diversity of religious beliefs and practices, recognizing the contributions differing experiences and viewpoints can bring to the community. Students with religion based conflict should talk to the instructor and appropriate university offices to request accommodations at the earliest possible time.

Text Book

- Allen and Holberg, *CMOS Analog Circuit Design,* 3nd Edition, Oxford, 2011
- Hastings, *The Art of Analog Layout,* Prentice Hall, 2nd ed
- Available at Amazon
  - Significant discounts vs bookstore
- International editions from Taiwan or Singapore

References

- Gray, *et al, Analysis and Design of Analog Integrated Circuits,* 5th Ed., Wiley, 2009
- William Liu, *Mosfet Models for Spice Simulation, Including BSIM3v3 and BSIM4*, Wiley-IEEE, 2001
- Daniel P. Foty, *MOSFET Modeling With SPICE: Principles and Practice,* Prentice Hall, 1996
- Yannis Tsividis, *Operation and Modeling of the MOS Transistor,* Oxford University Press; 2nd edition (May 1, 2003)
- Laker and Sansen, *Design of Analog Integrated Circuits,* McGraw Hill, 1994
- David Johns & Ken Martin , *Analog Integrated Circuit Design*, John Wiley & Sons, Inc. 1997
- Behzad Razavi, *Design of Analog CMOS Integrated,* CircuitsMcGraw-Hill, 1999
- Geiger, *et al, VLSI Design Techniques for Analog and Digital Circuit*, McGraw Hill, 1990

- Baker, *CMOS Circuit Design, Layout and Simulation,* IEEE Press, 1997
- Alan B. Grebene, *Bipolar and MOS Analog Integrated Circuit Design* (Wiley Classics Library), 2001

MOSIS links

- MOSIS web site
- FAQ from comp.lsi.cad
- MOSIS scalable design rules
- MOSIS Pads directory.
- Process description: TSMC 0.18, ON 0.5
- SPICE model parameters: TSMC 0.18, ON 0.5

Links for information sources

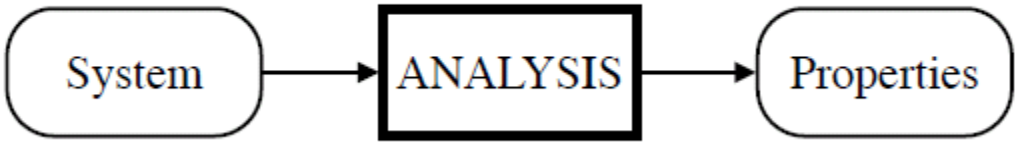
- IEEE IEL
- Science Citation Index / ISI Web of Science
- U.S. Patent Office
- International Technology Roadmap for Semiconductors
- Semiconductor Research Corporation

Links for technical writing

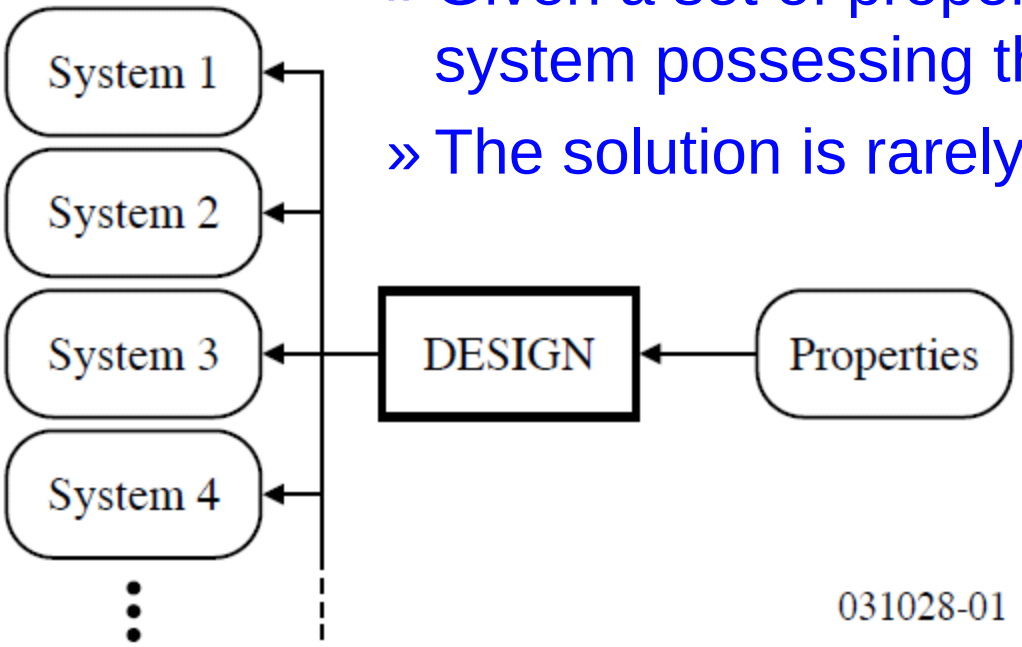
- Things to think about while writing papers
- A nuts and bolts guide to college writing
- The Barleby refence site
- William Shrunk's "Elements of Style"
- Dictionary.com
- Answers.com
- Visual Thesaurus
- Latex style files for IEEE journals

Analysis versus design

- Analysis:



  - Given a system, find its properties.
  - The solution is unique.
- Design:
  - » Given a set of properties, come up with a system possessing them.
  - » The solution is rarely unique.



The Analog IC Design Process

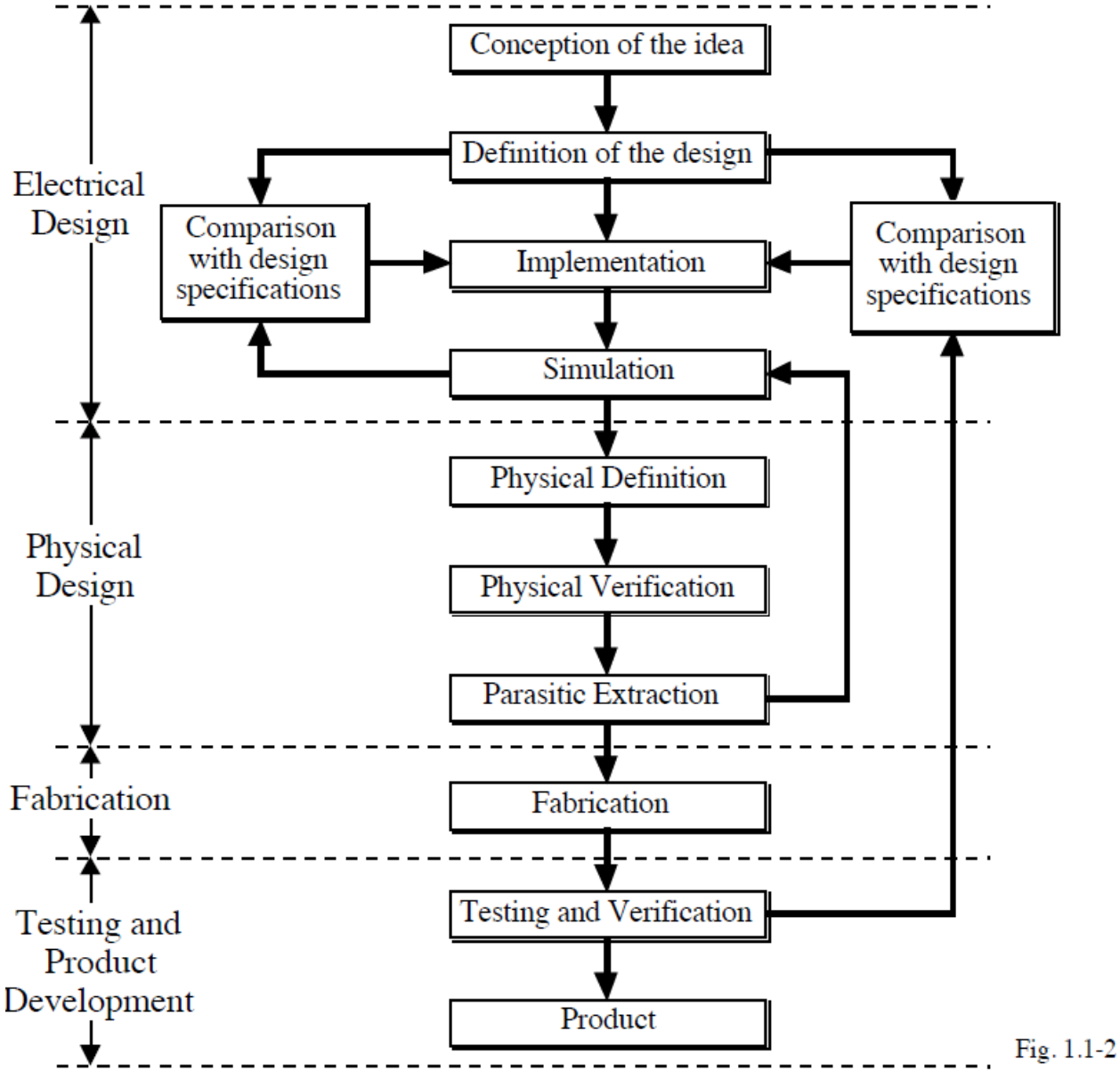
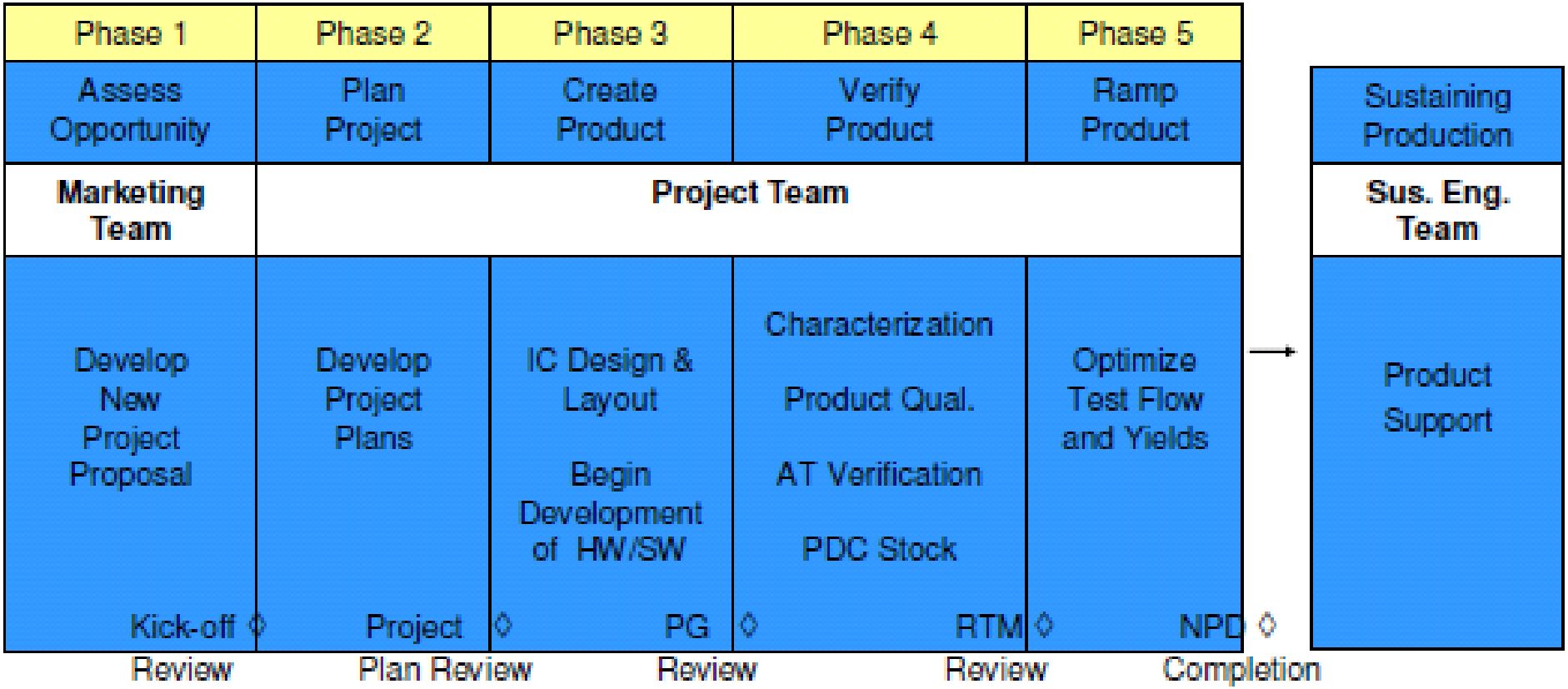
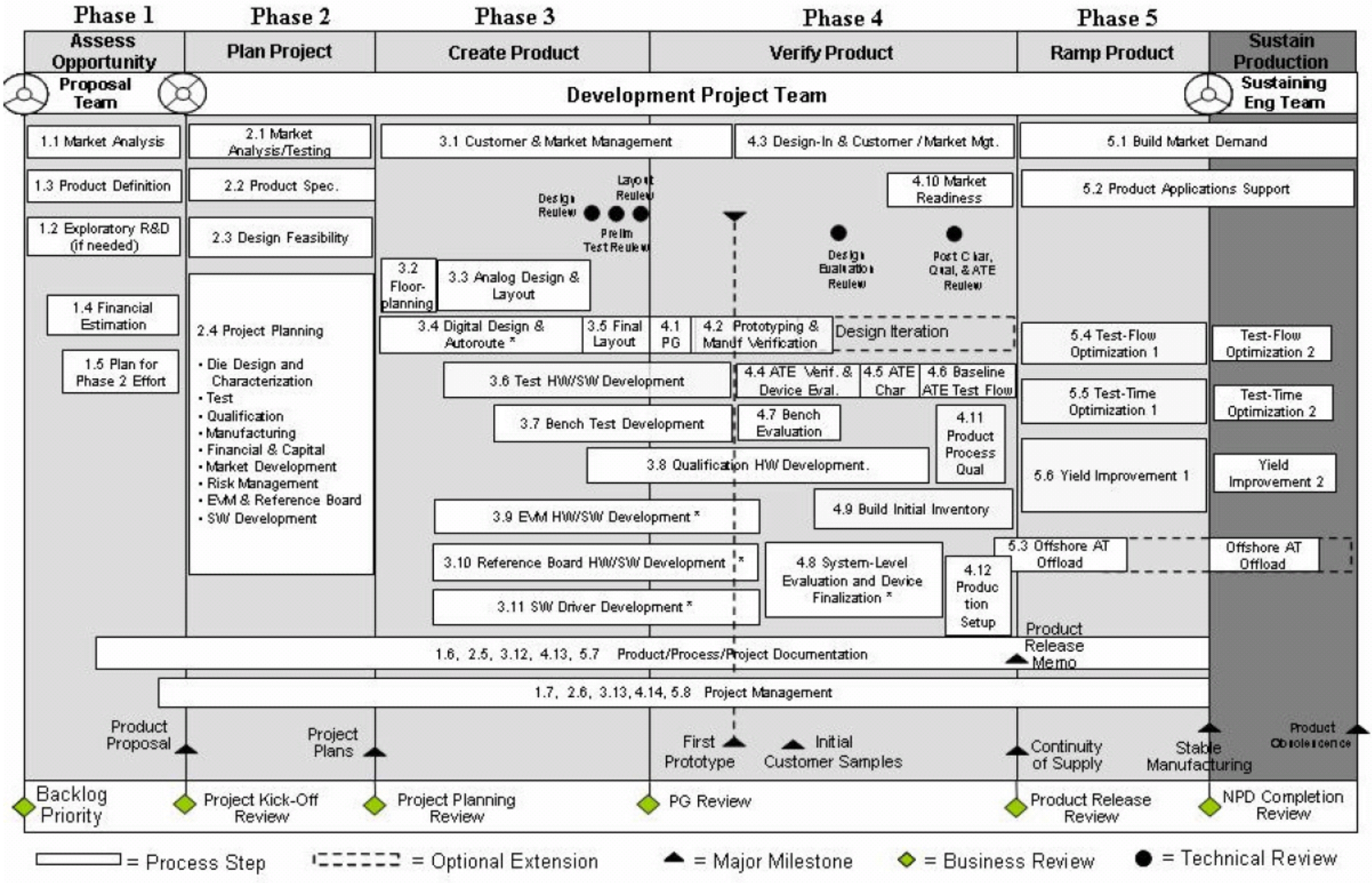


Fig. 1.1-2



Texas Instruments version



Texas Instruments

Electrical Design

- the process from the specifications to a circuit solution

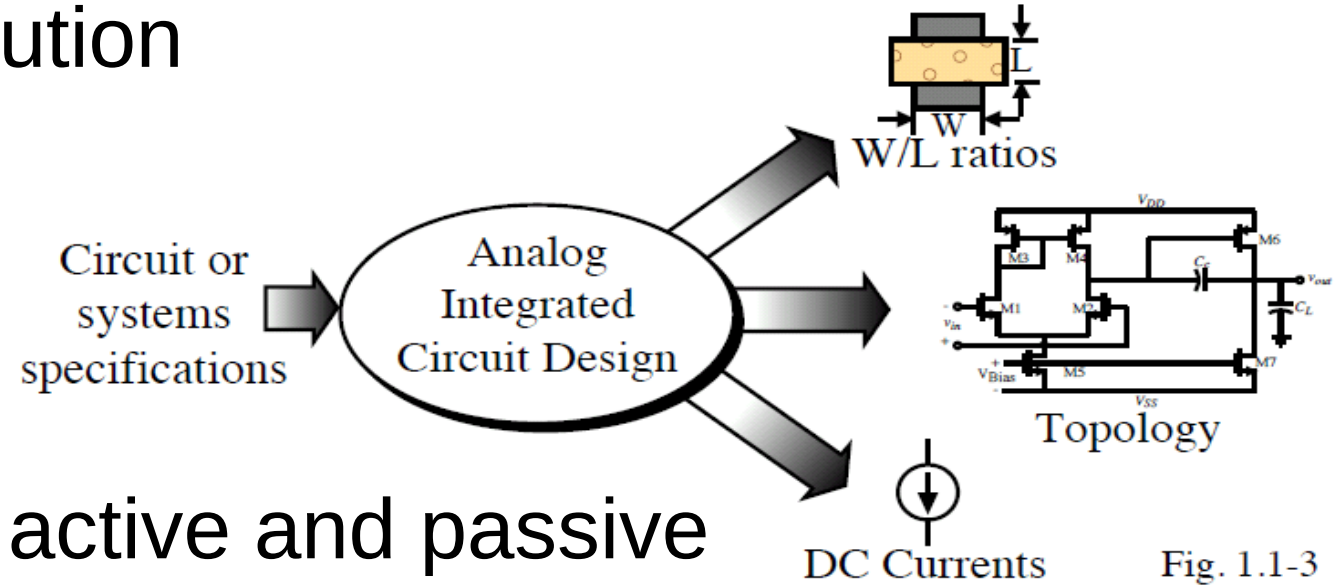
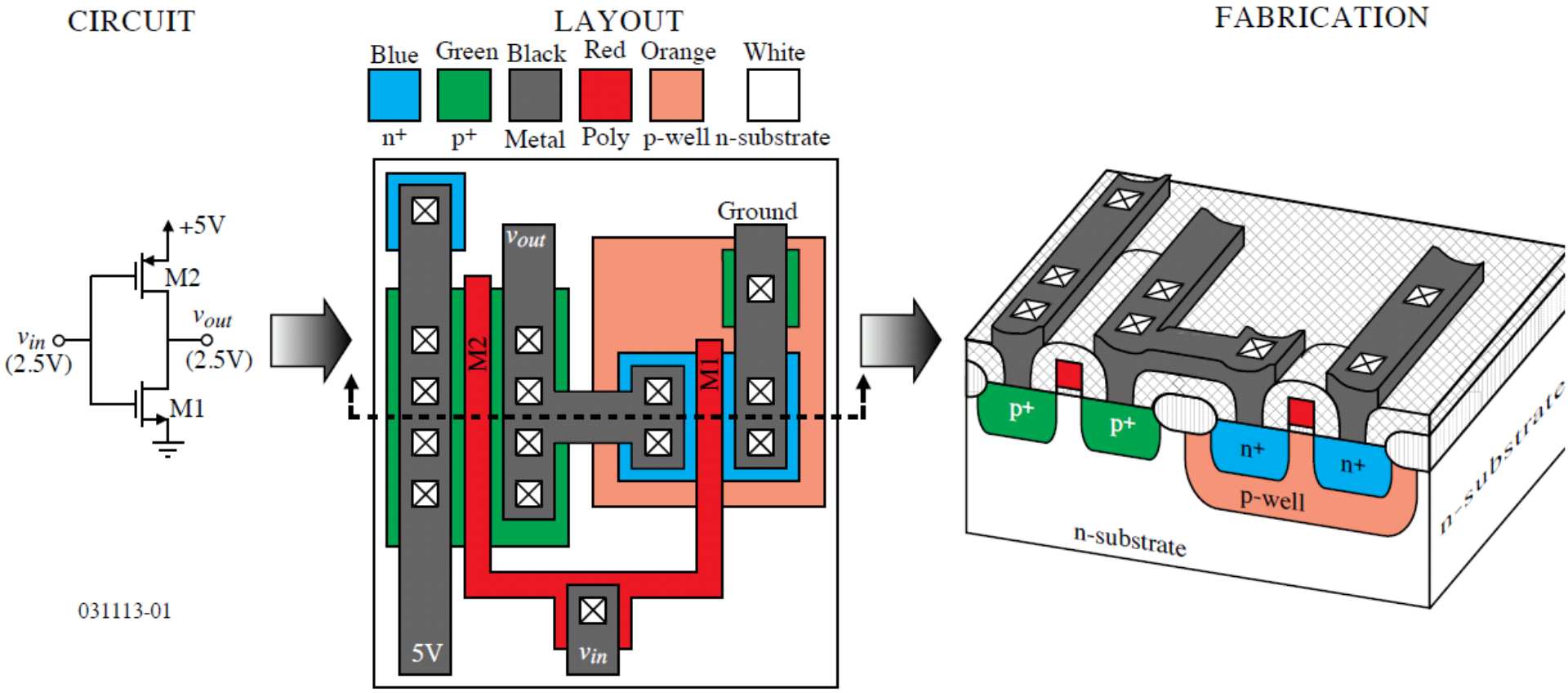


Fig. 1.1-3

- Requires active and passive device electrical models for
  - Creating the design
  - Verifying the design
  - Determining the robustness of the design

Physical Design

- From electrical design to a layout pattern



Test

- To verify that fabricated circuit meet specifications
- To characterize additional “behavior”
- To trouble-shoot design
- To fine tune certain parameters
- To trim certain parameters

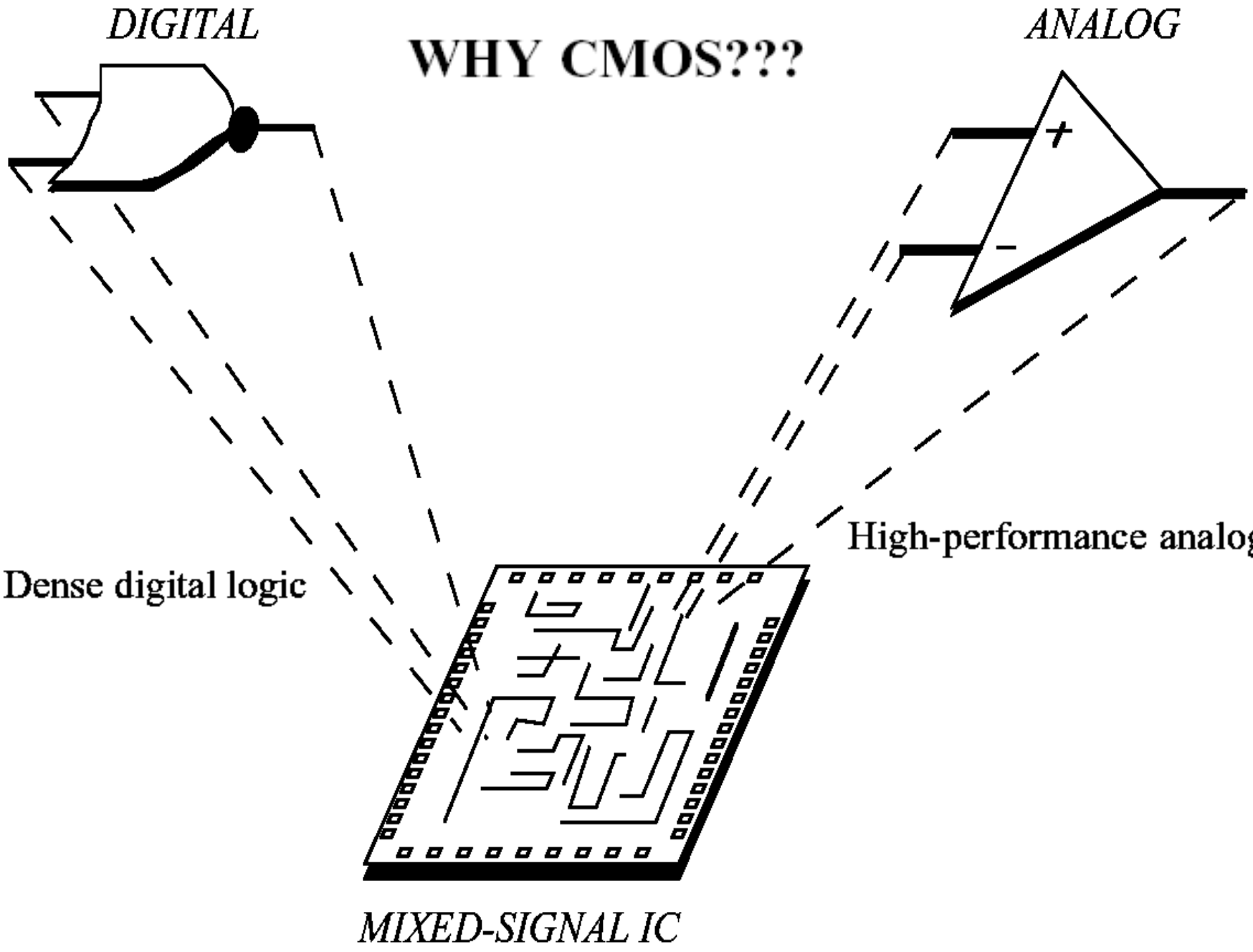
- Top designers are top test engineers

Skill-set for Analog IC design

- Good physics background
- Decent math skills
- Skilled in measurements
- Good understanding of principles, concepts, and assumptions
- Skilled in simulation
- Grasp of technology and modeling
- Intuition for reasonable simplifications
- Audacity to try new things, but guided by theory and physics
- Not afraid of failure, but methodical learning from failures/mistakes
- Wide range of knowledge

Technology scaling

- The good:
  - Smaller geometries
  - Smaller parasitics
  - Higher transconductance
  - Higher bandwidths
- The bad:
  - Reduced voltages
  - Smaller channel resistances (lower gain)
  - More nonlinearity
  - Deviation from square-law behavior
- The challenging:
  - Increased substrate noise in mixed signal applications
  - Threshold voltages are not scaling with power supply
  - Reduced dynamic range
  - Poor matching at minimum channel length


DIGITAL
WHY CMOS???
ANALOG
+
–
High-performance analog
Dense digital logic
MIXED-SIGNAL IC

Classification of Integrated Circuits by Device Count

Nomenclature	Active Device Count	Typical Functions
SSI	1-100	Gates, OpAmps, Many linear applications
MSI	100-1000	Registers, Filters, etc.
LSI	1000-100,000	Microprocessors, data converters, etc.
VLSI	>100,000	Memories, Computers, Signal Processors
SoC (System on Chip)	???	Large digital systems with embedded analog, mixed-signal, RF function, such as transceivers

Technology nodes

- Typically referred to by minimum feature size
  - Smallest geometry size that can be made in the horizontal direction
  - But vertical direction length (oxide thickness) can be much smaller
- Feature size are scaled by roughly $1/\sqrt{2}$, but rounded to some pre-agreed upon numbers
- Examples: 0.5μm, 0.35μm, 0.25μm, 0.18μm, 0.13μm, 90nm, 65nm, 45nm, …

Signal naming conventions

Signal Definition	Quantity	Subscript	Example
Total instantaneous value of the signal	Lowercase	Uppercase	q_A
DC value of the signal	Uppercase	Uppercase	Q_A
AC value of the signal	Lowercase	Lowercase	q_a
Complex variable, phasor, or rms value of the signal	Uppercase	Lowercase	Q_a

Example:

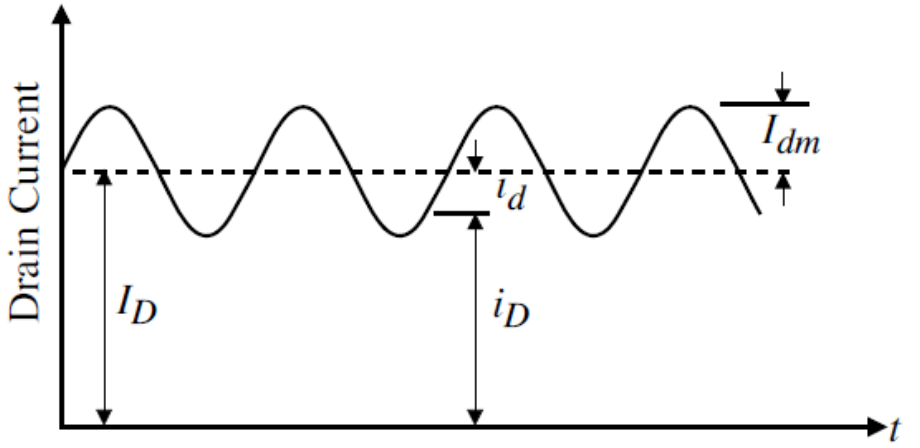
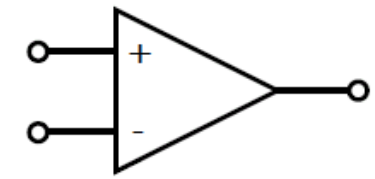
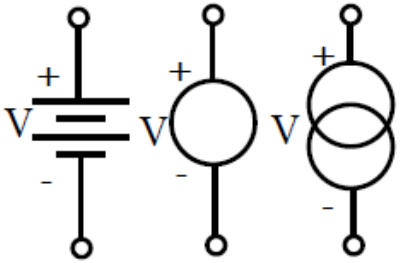


Fig. 1.4-1

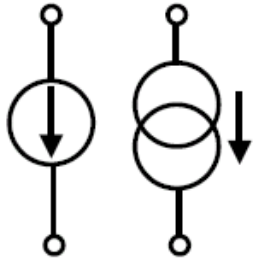
Schematic Symbols



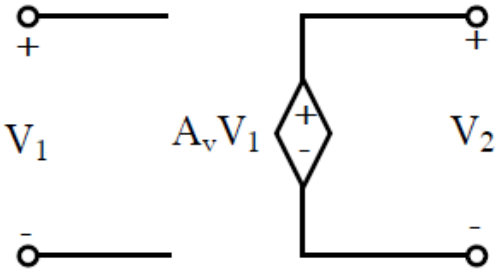
Differential amplifier,
op amp, or comparator



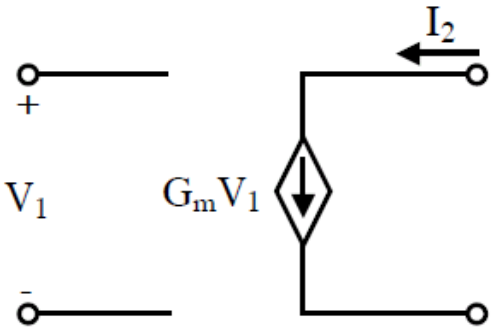
Independent
voltage sources



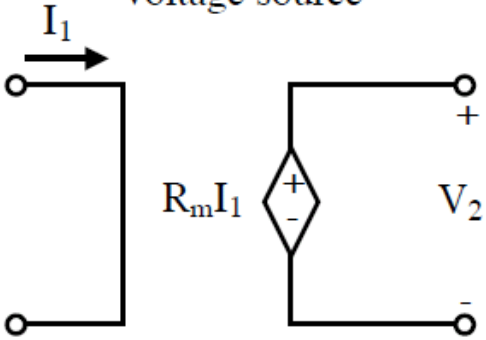
Independent
current source



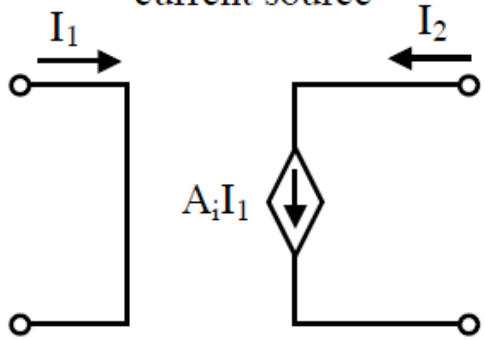
Voltage-controlled,
voltage source



Voltage-controlled,
current source

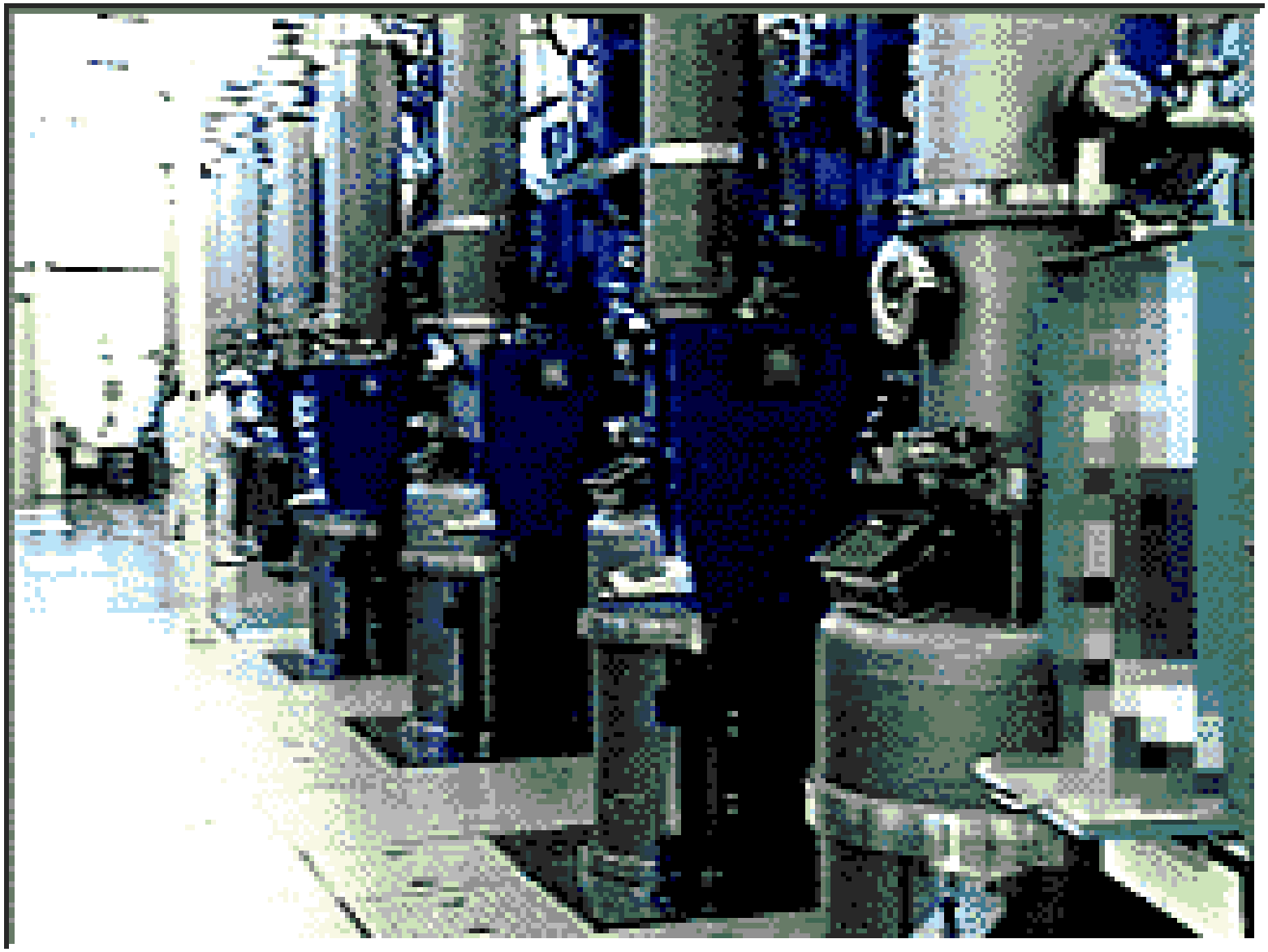


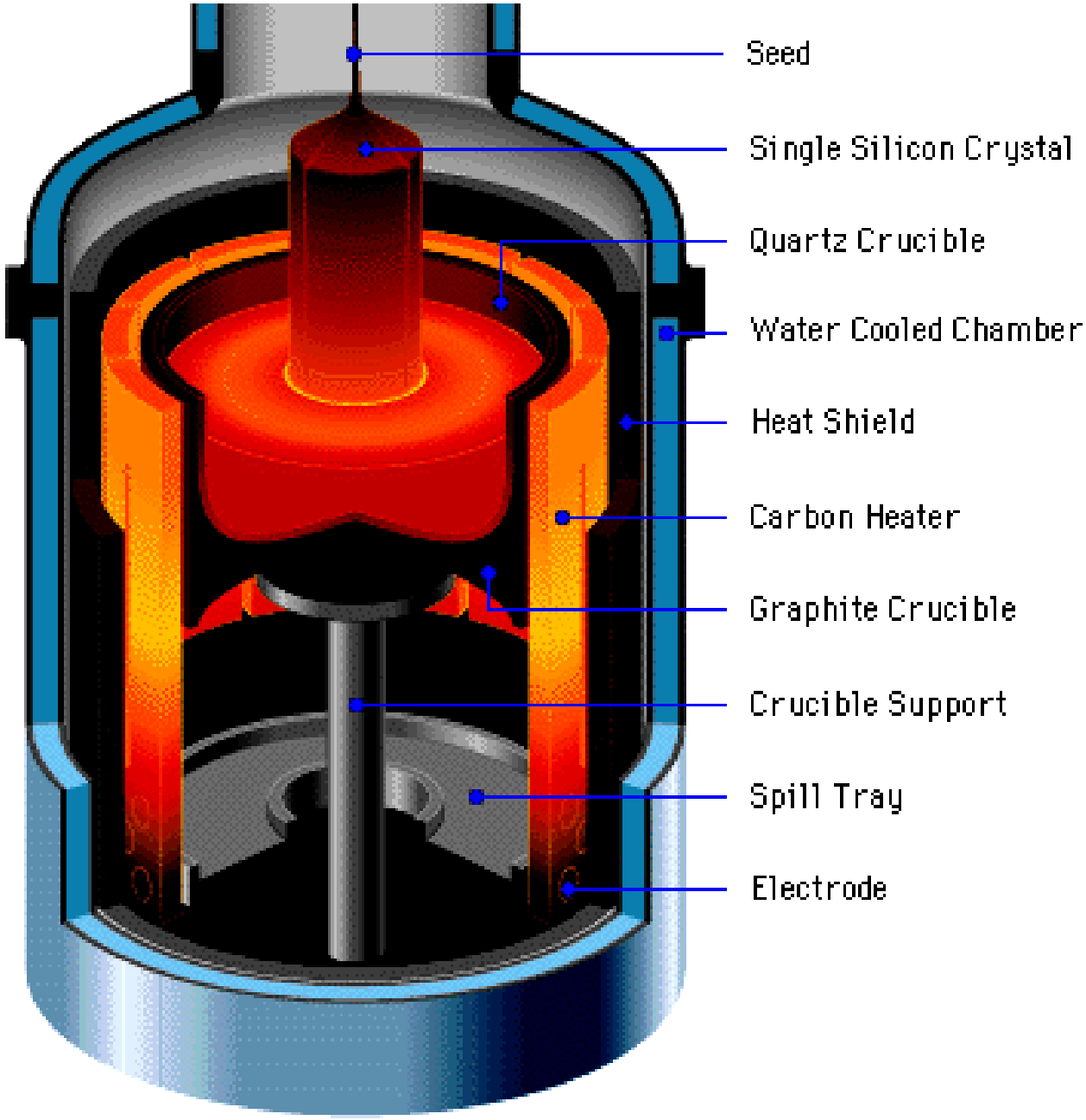
Current-controlled,
voltage source

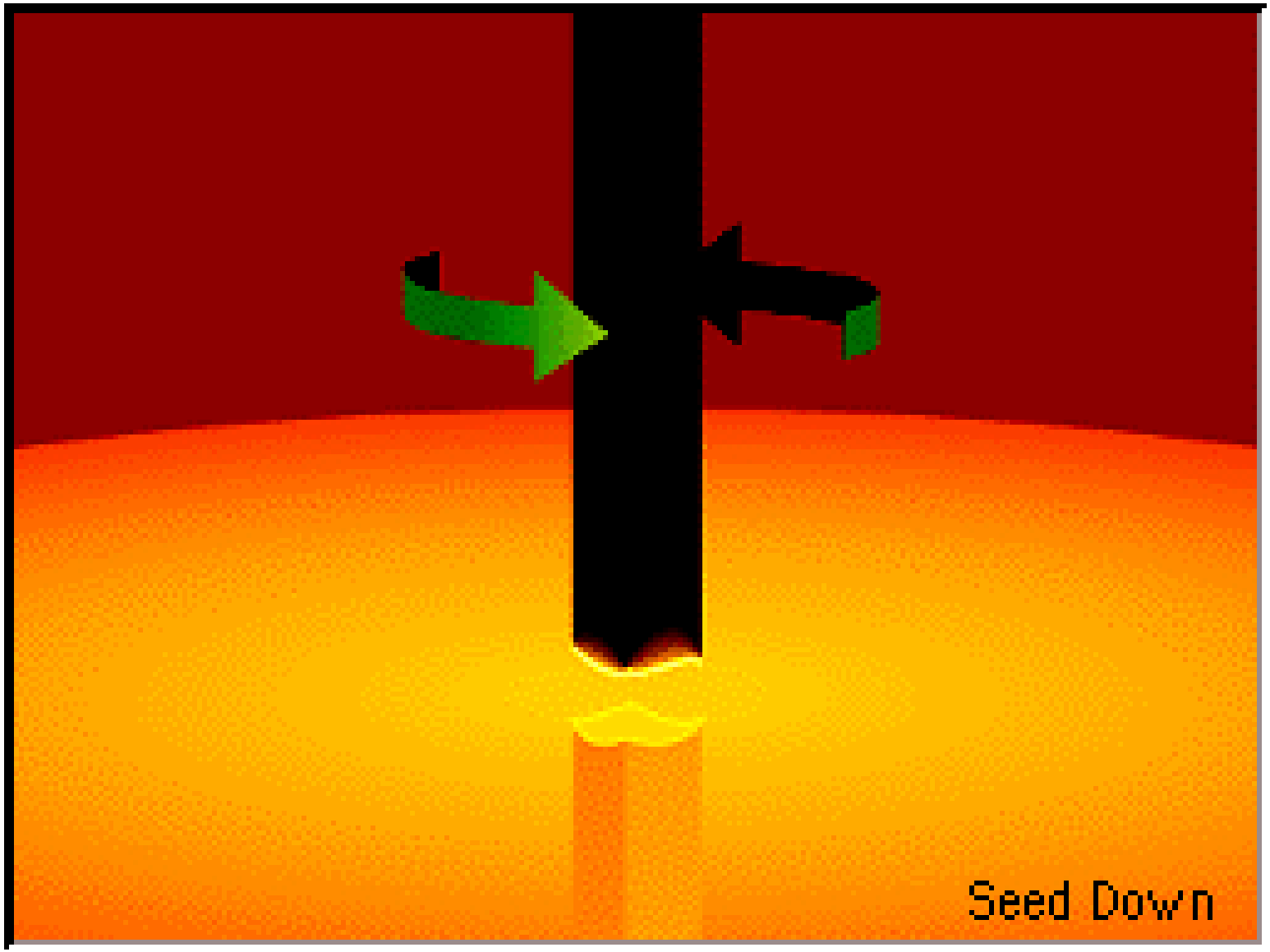


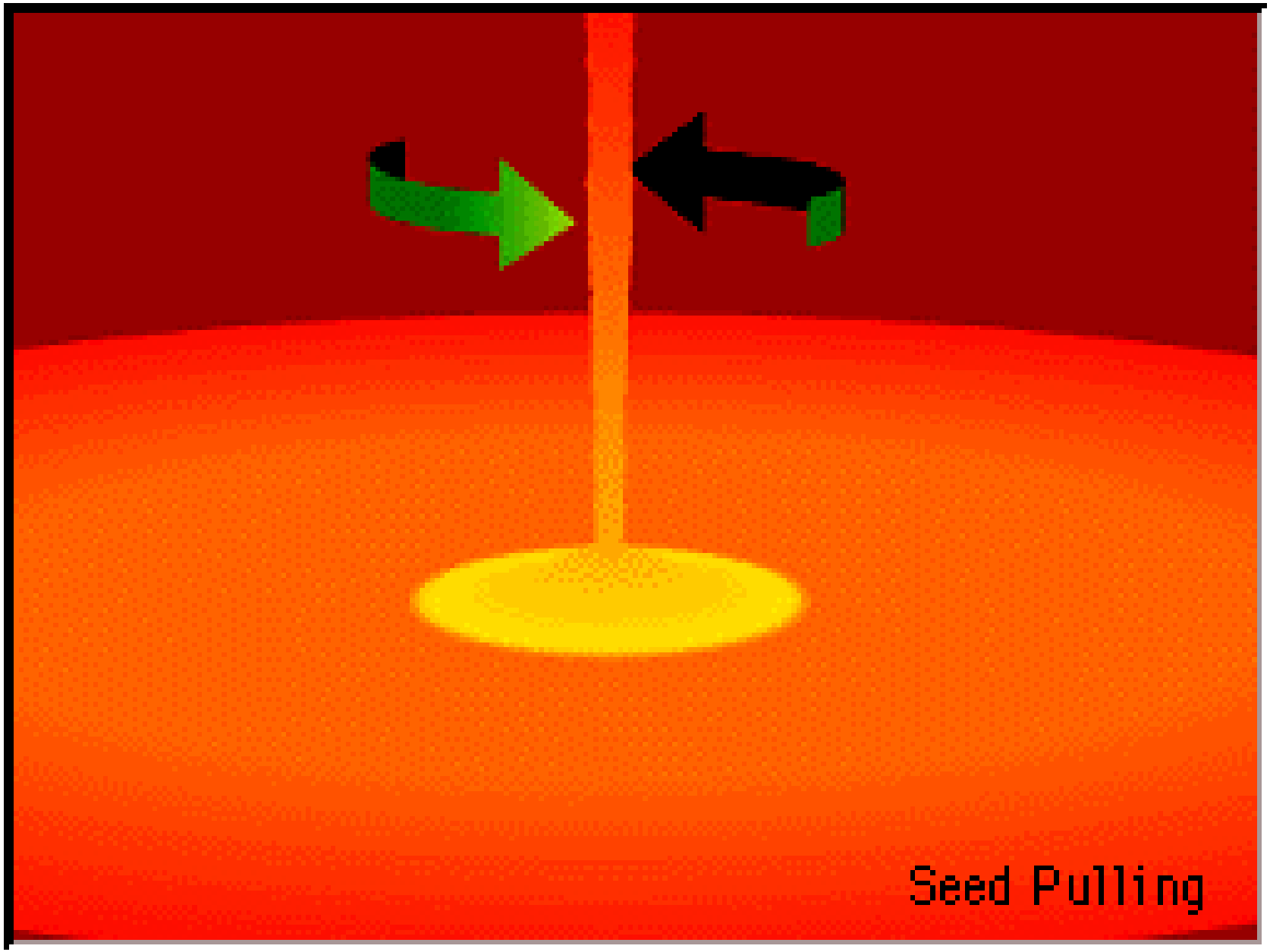
Current-controlled,
current source

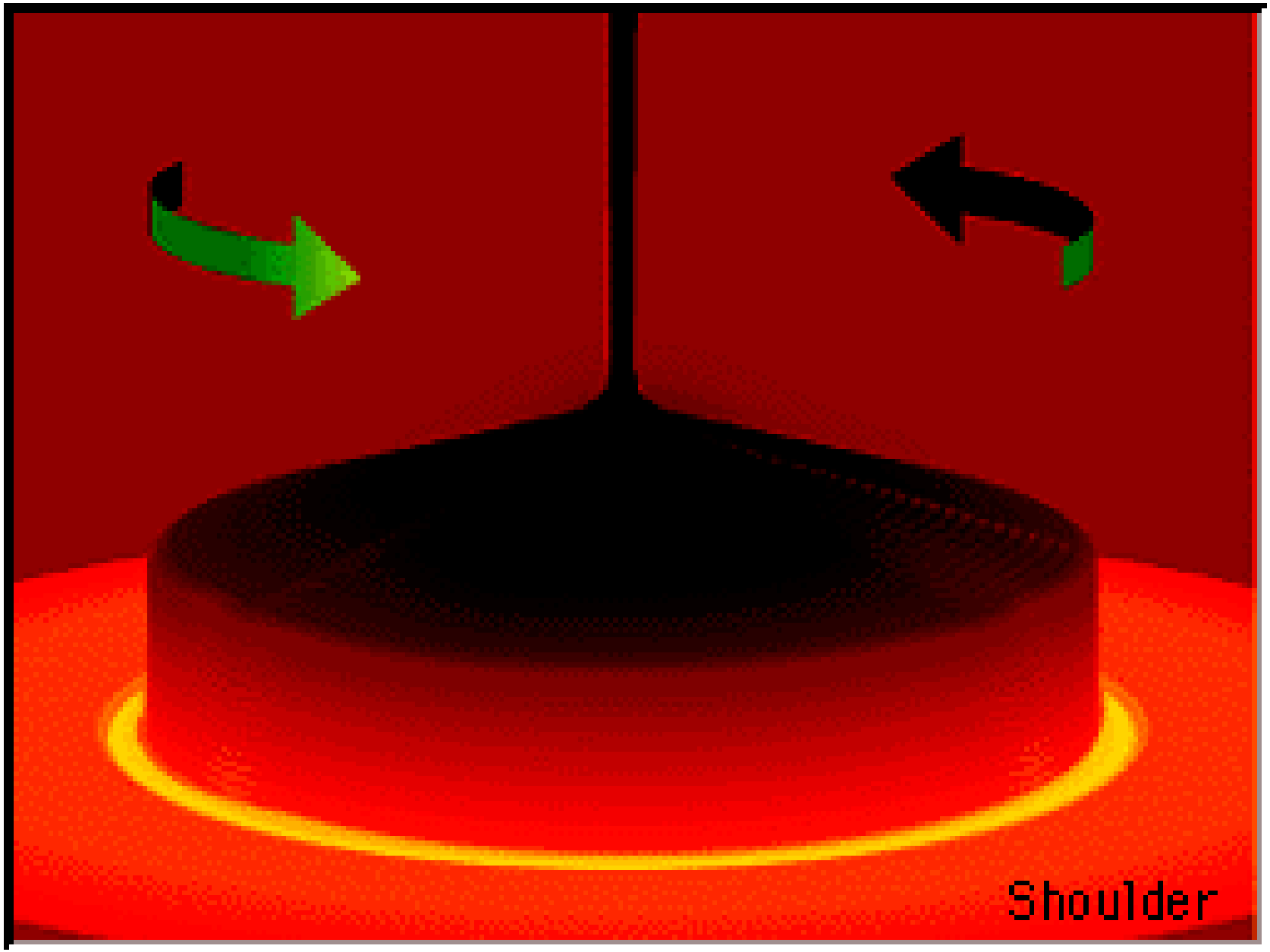
From Rocks to Wafer, to chips

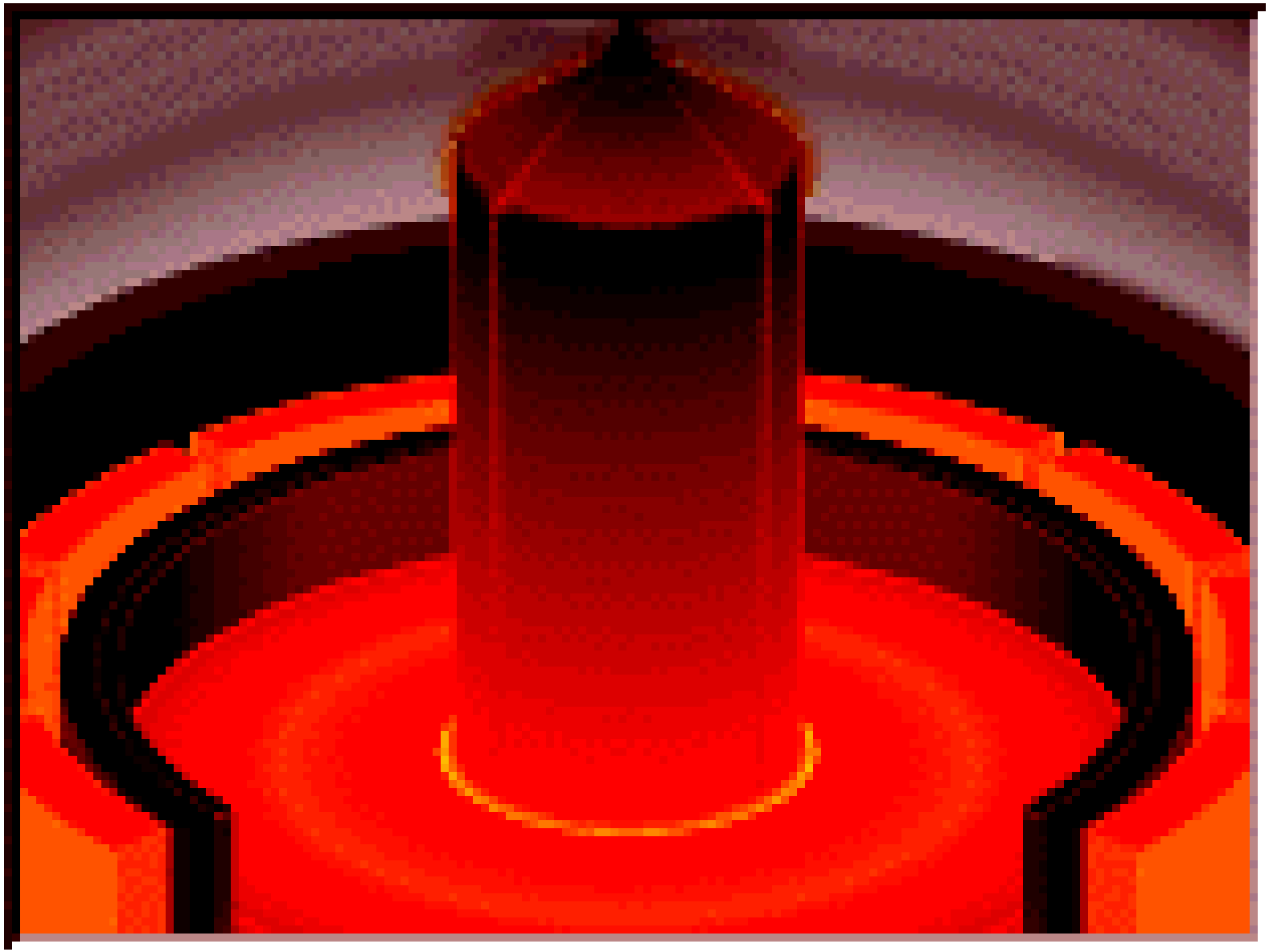


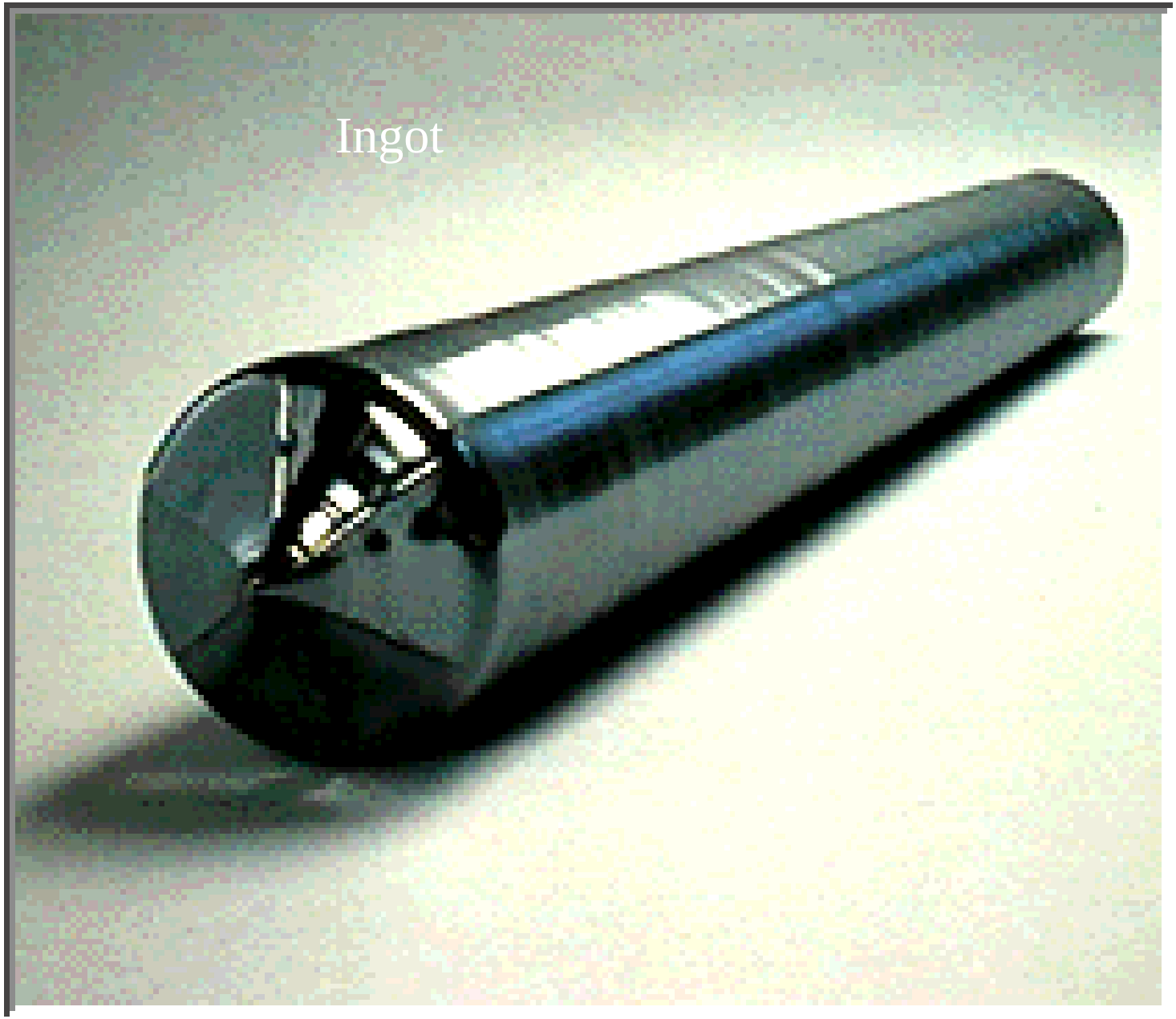

Seed
Single Silicon Crystal
Quartz Crucible
Water Cooled Chamber
Heat Shield
Carbon Heater
Graphite Crucible
Crucible Support
Spill Tray
Electrode

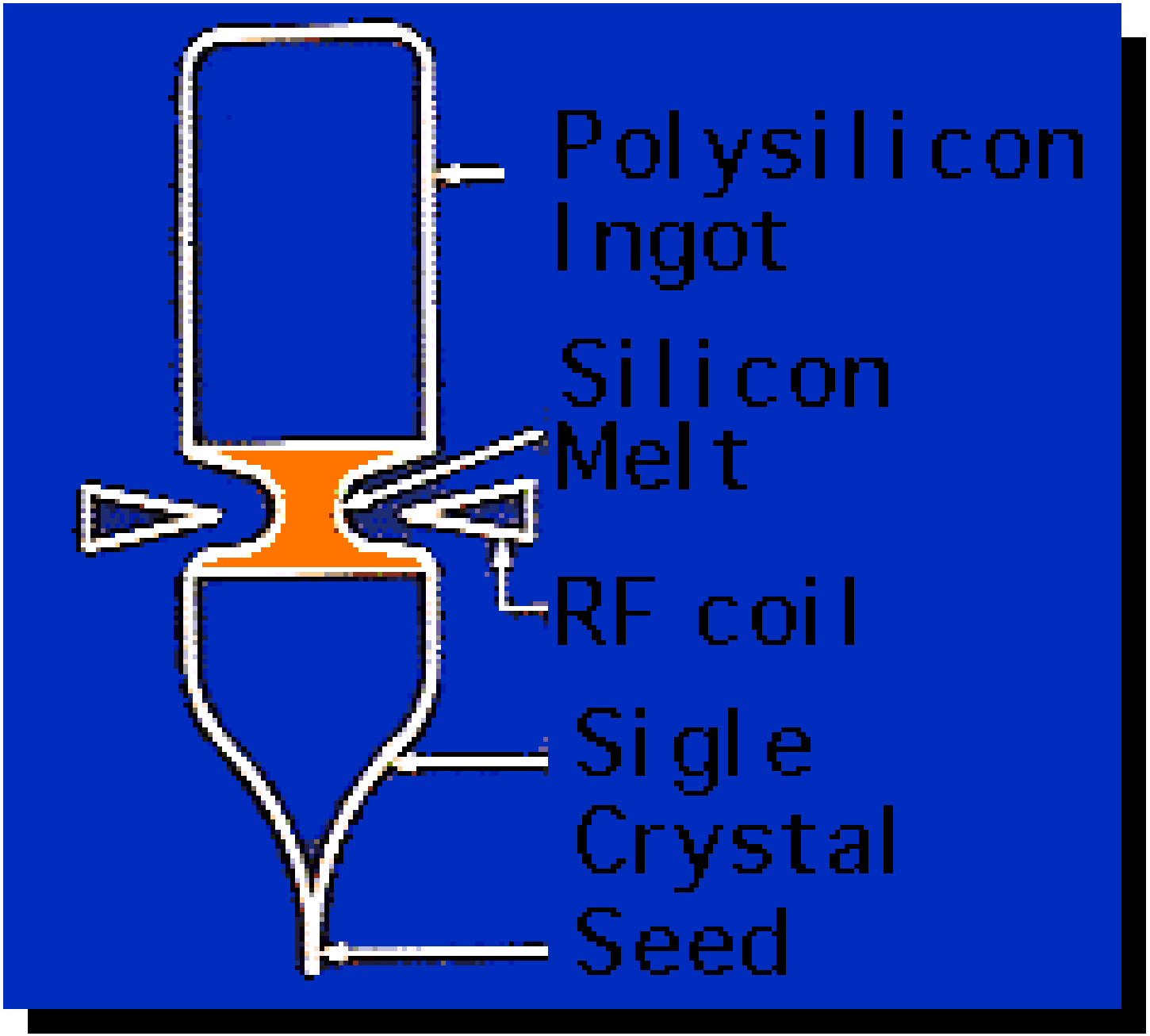

Seed Down


Seed Pulling

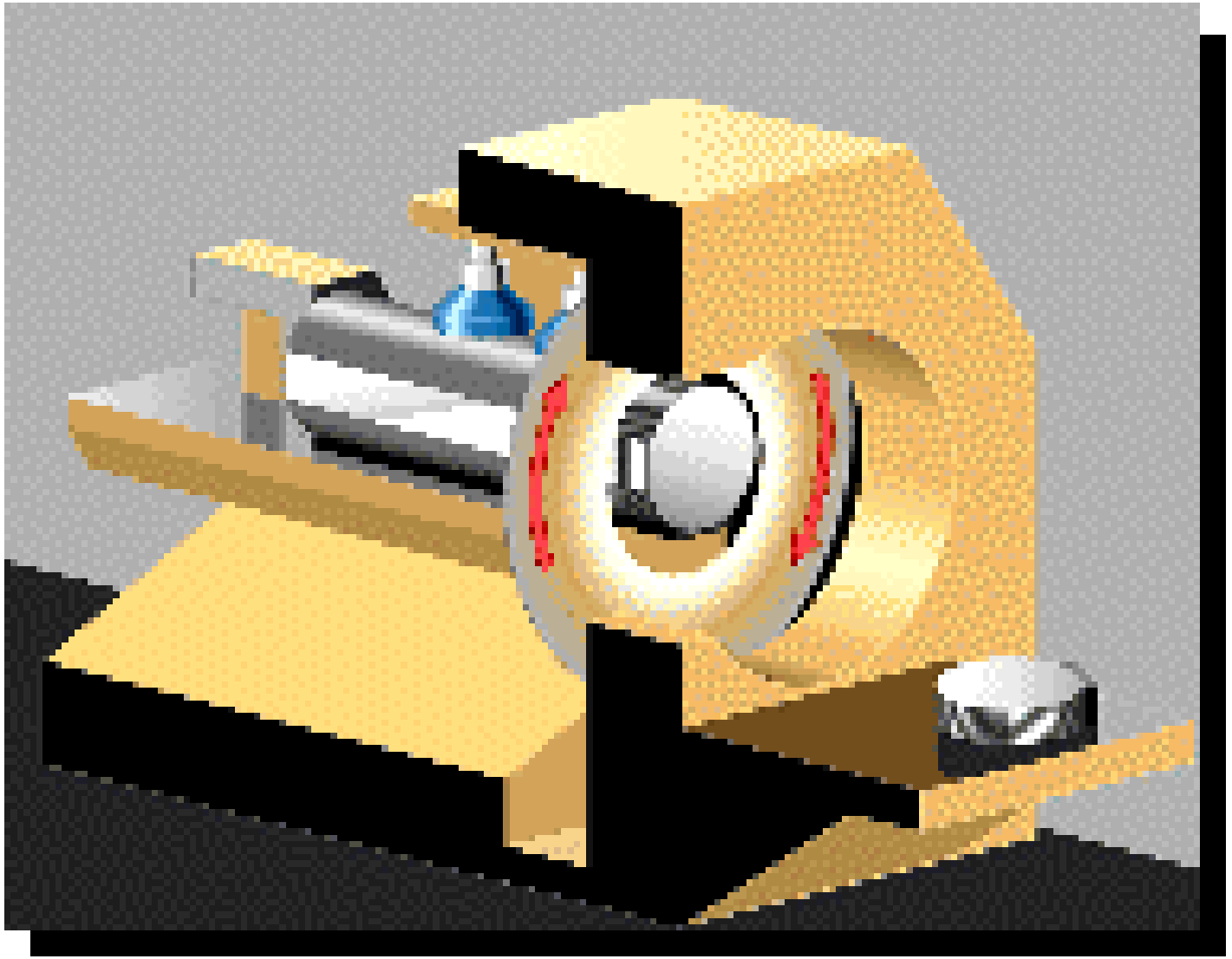

Shoulder



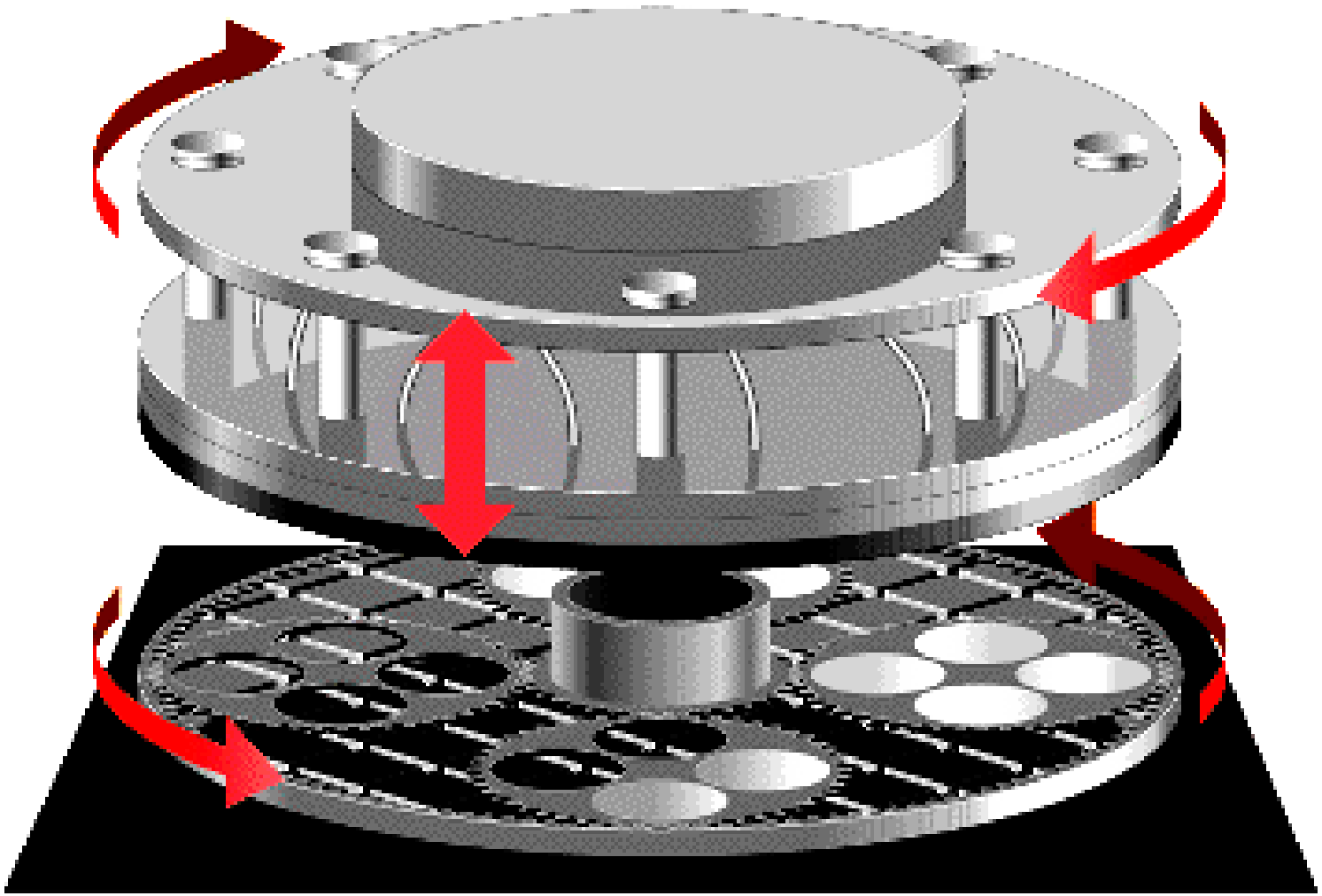

Ingot


Polysilicon
Ingot
Silicon
Melt
RF coil
Sigle
Crystal
Seed

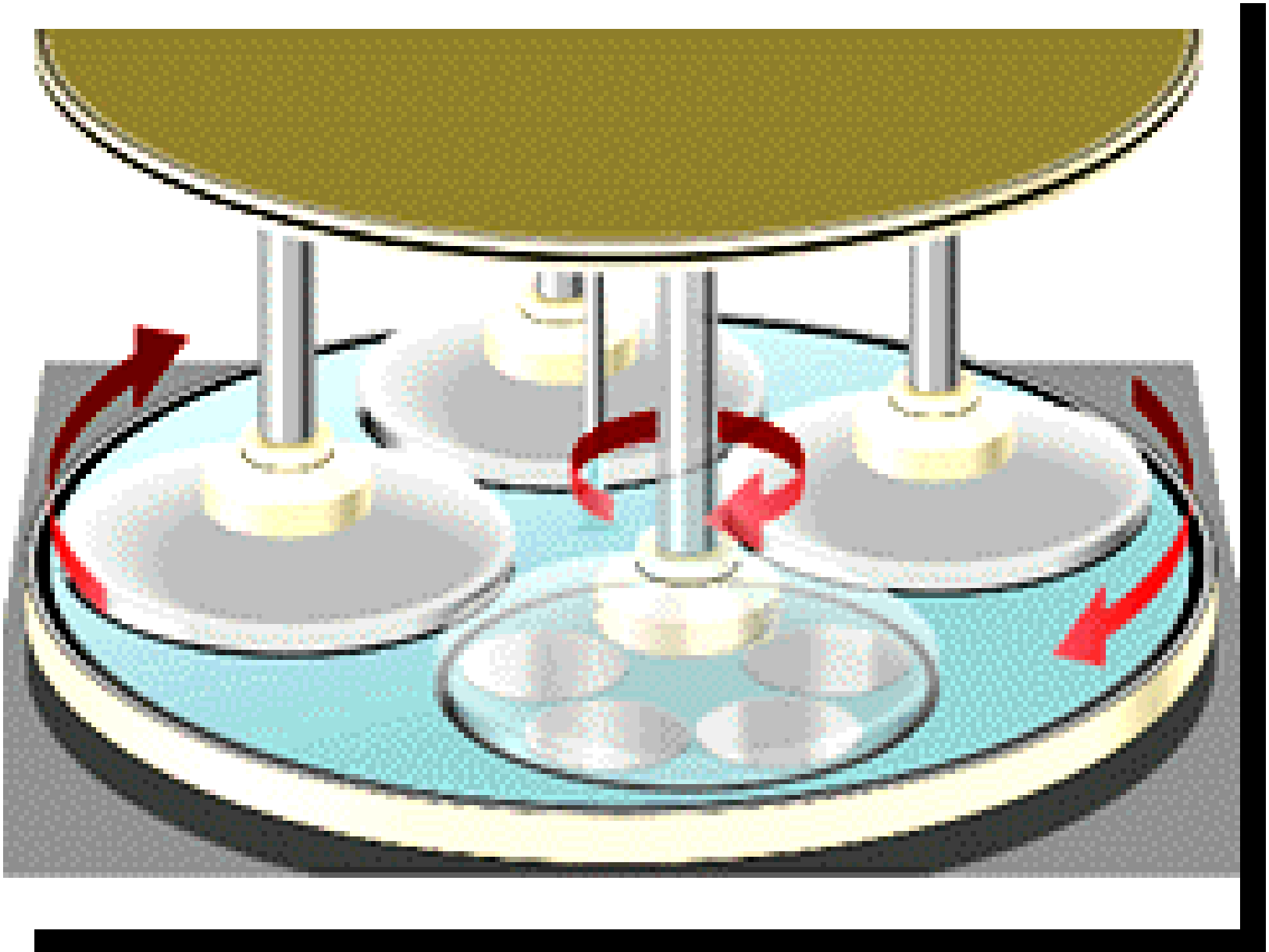
Slicing



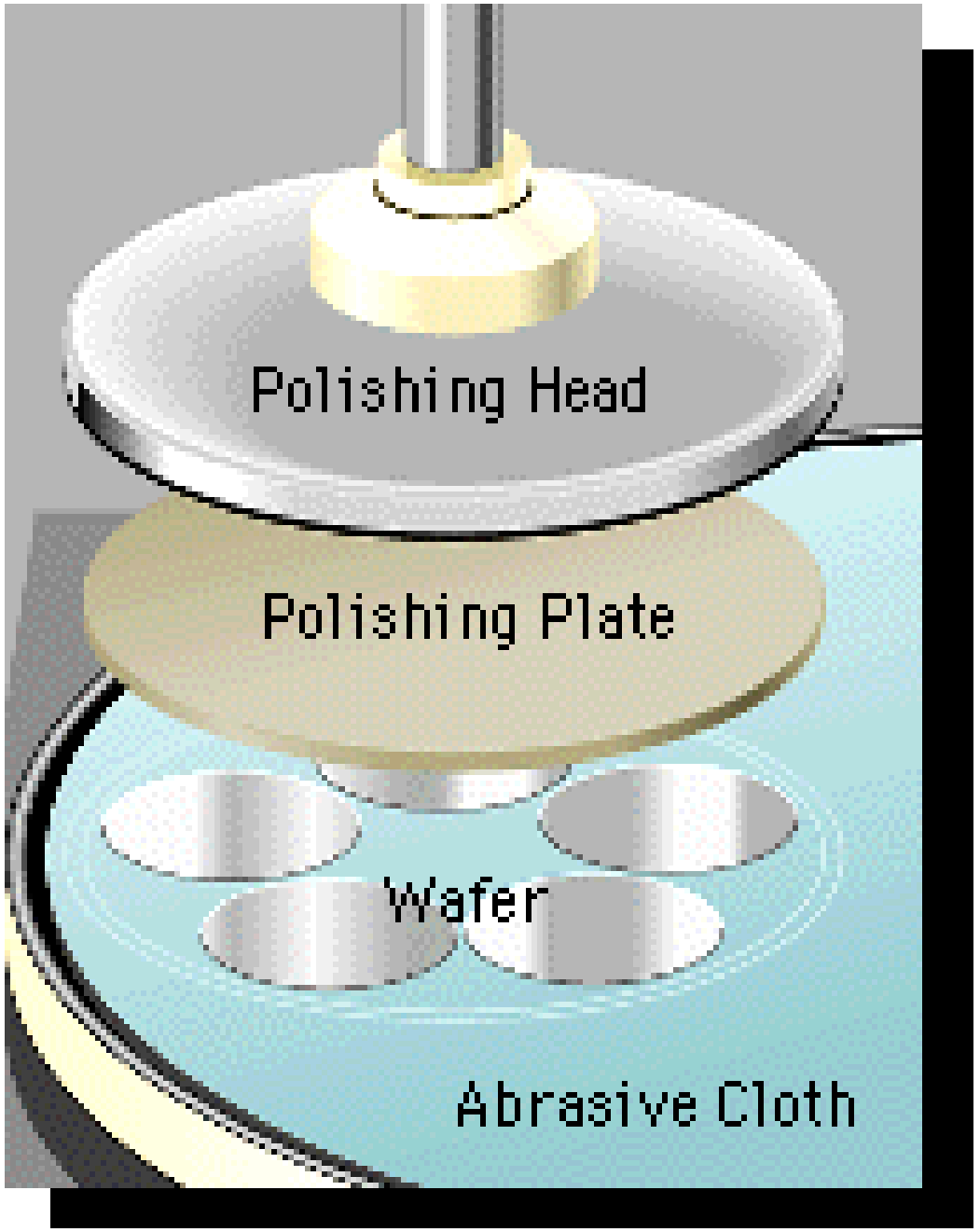
Lapping

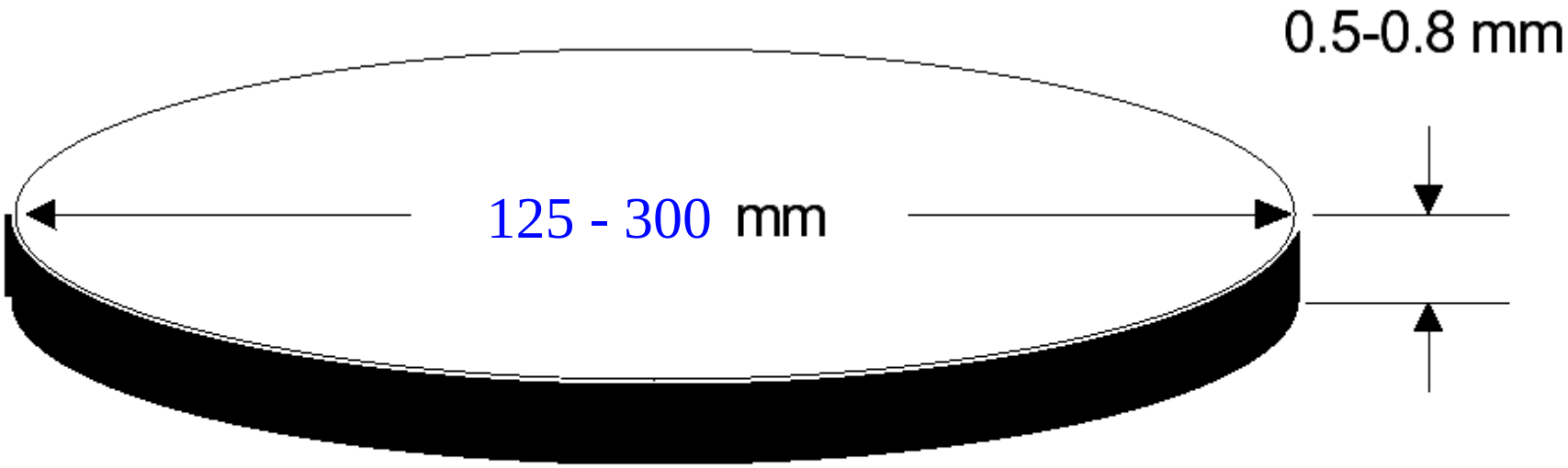


Polishing



Closer View Of Polishing





n-type: 3-5 Ω-cm

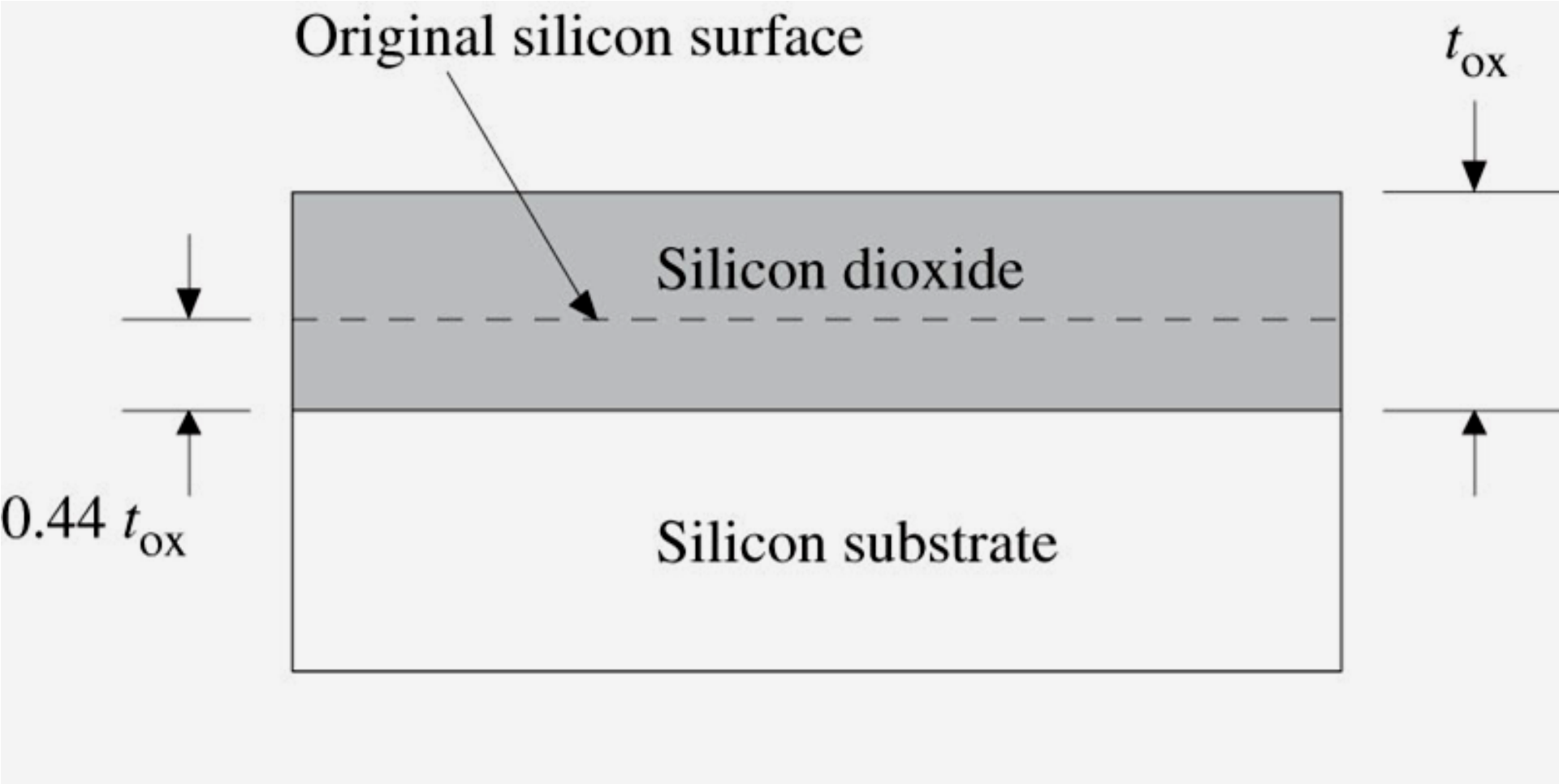
p-type: 14-16 Ω-cm

BASIC FABRTICATION PROCESSES

- Oxide growth
- Thermal diffusion
- Ion implantation
- Deposition
- Etching
- Shallow trench isolation
- Epitaxy
- Photolithography

Oxidation

- **The process of growing a layer of silicon dioxide (SiO2)on the surface of a silicon wafer.**
- **Uses:**
  - ✓ **Provide isolation between two layers**
  - ✓ **Protect underlying material from contamination**
  - ✓ **Very thin oxides (100 to 1000 Å) are grown using dry-oxidation techniques.**
  - ✓ **Thicker oxides (>1000 Å) are grown using wet oxidation techniques.**

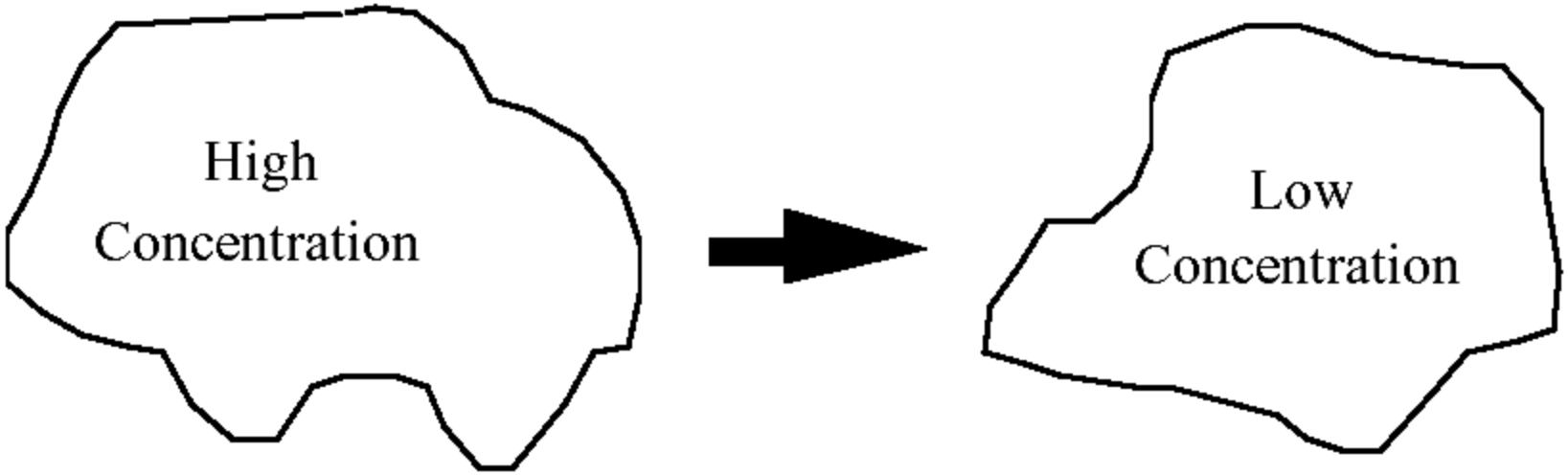


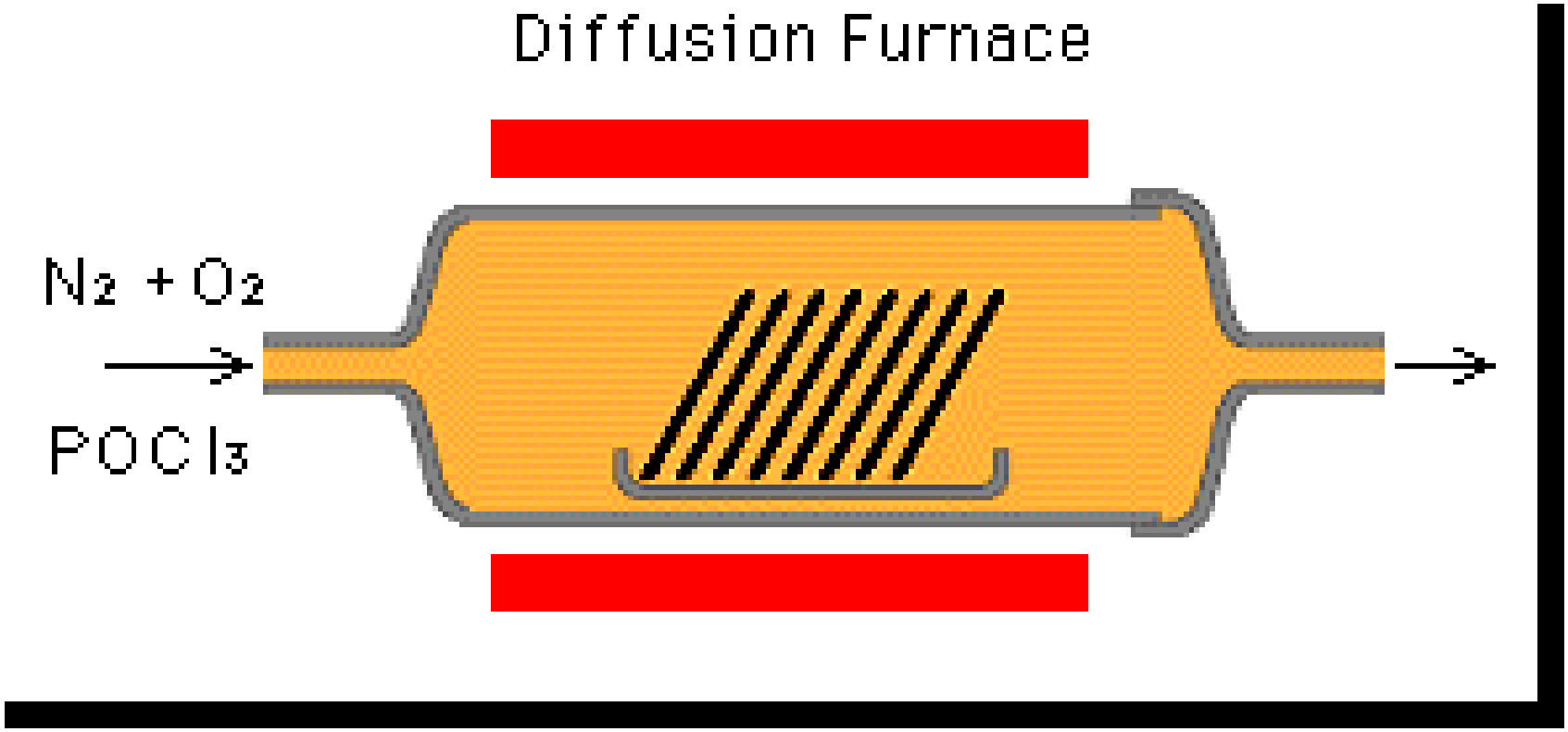
(Thickness of SiO_2 grossly exaggerated.)

Diffusion

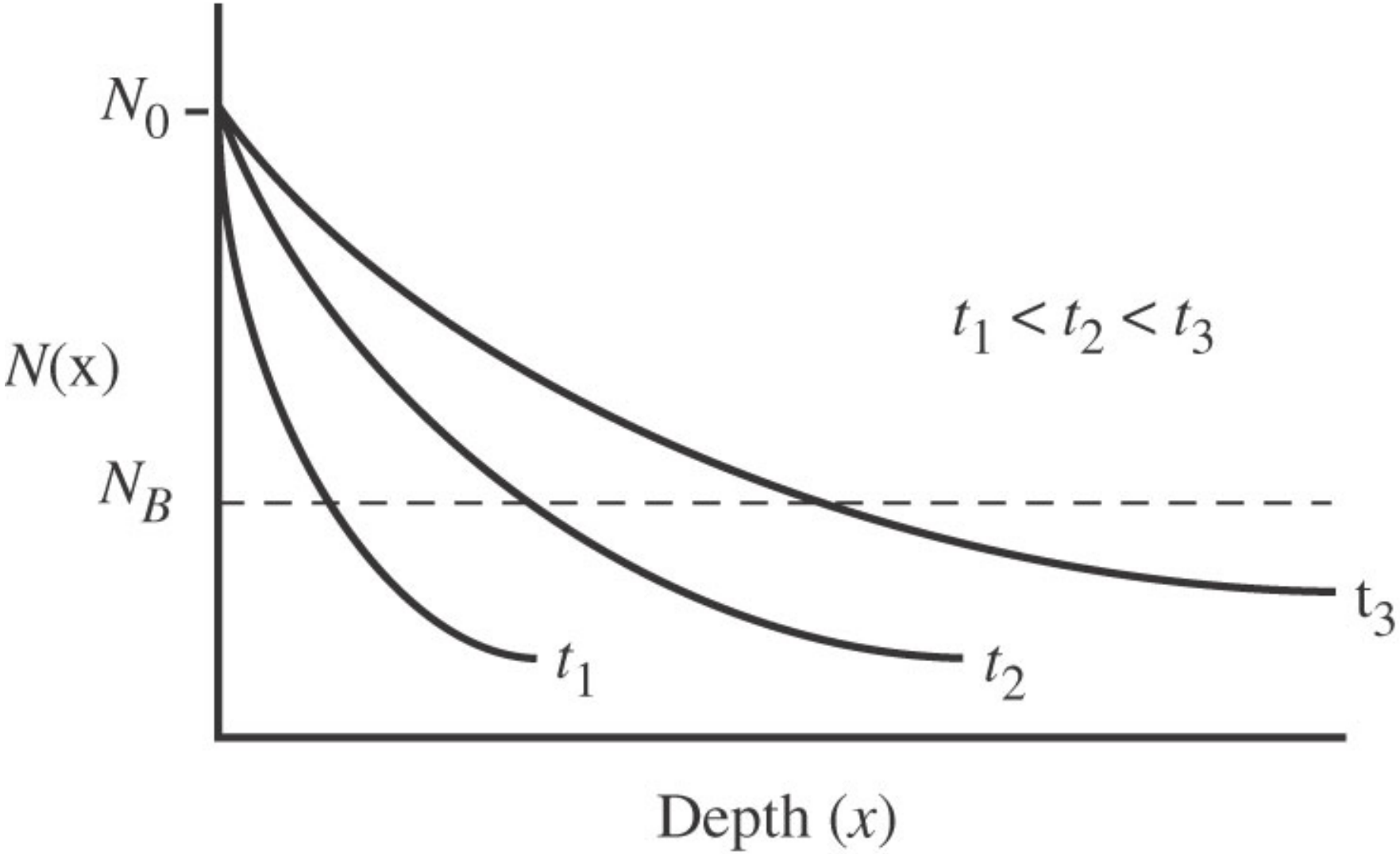
Movement of impurity atoms at the surface of the silicon into the bulk of the silicon

- **From higher concentration to lower concentration.**
- **Done at high temperatures: 800 to 1400 °C.**

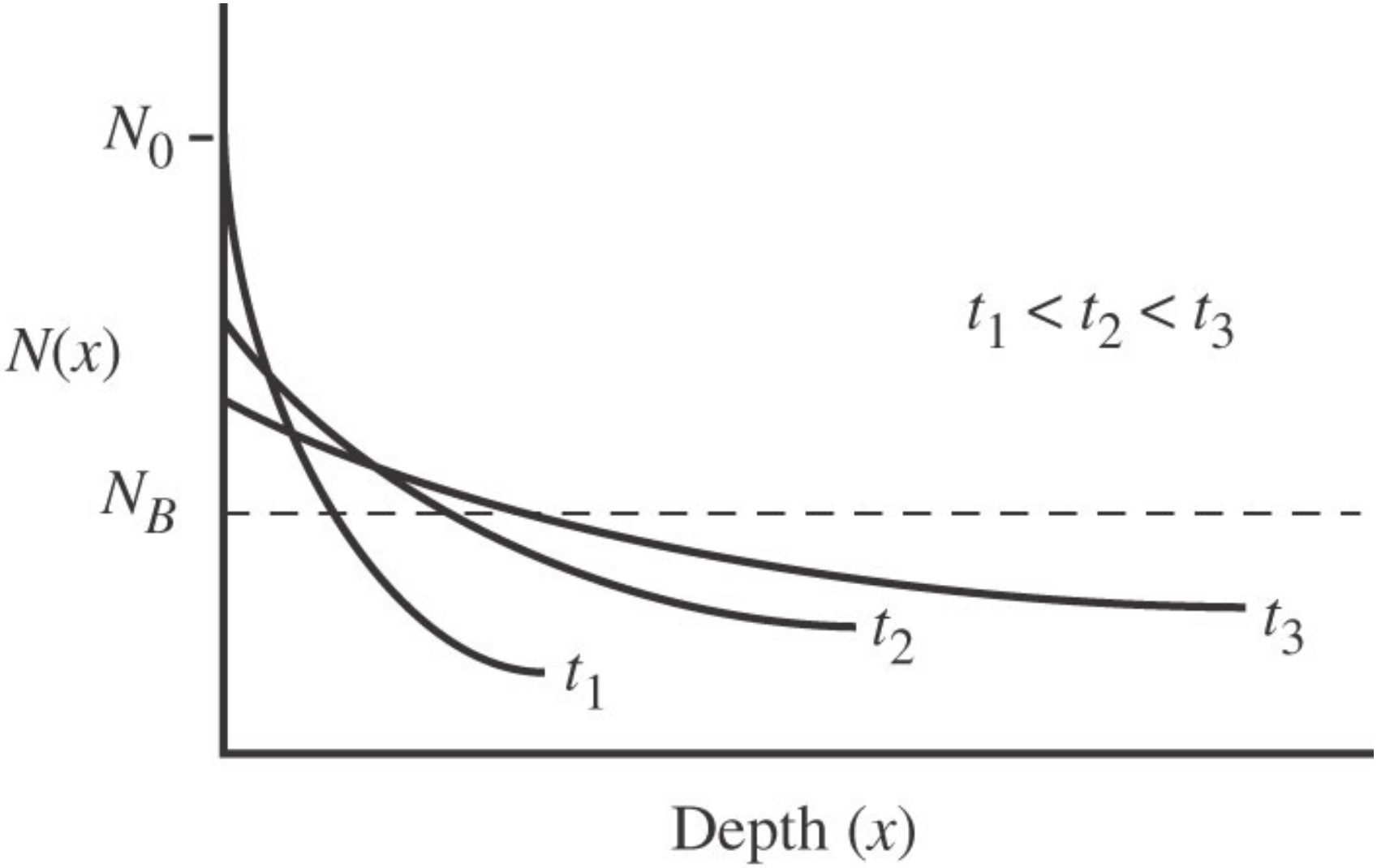



Diffusion Furnace
N2 + O2
POCl3

Infinite-source diffusion

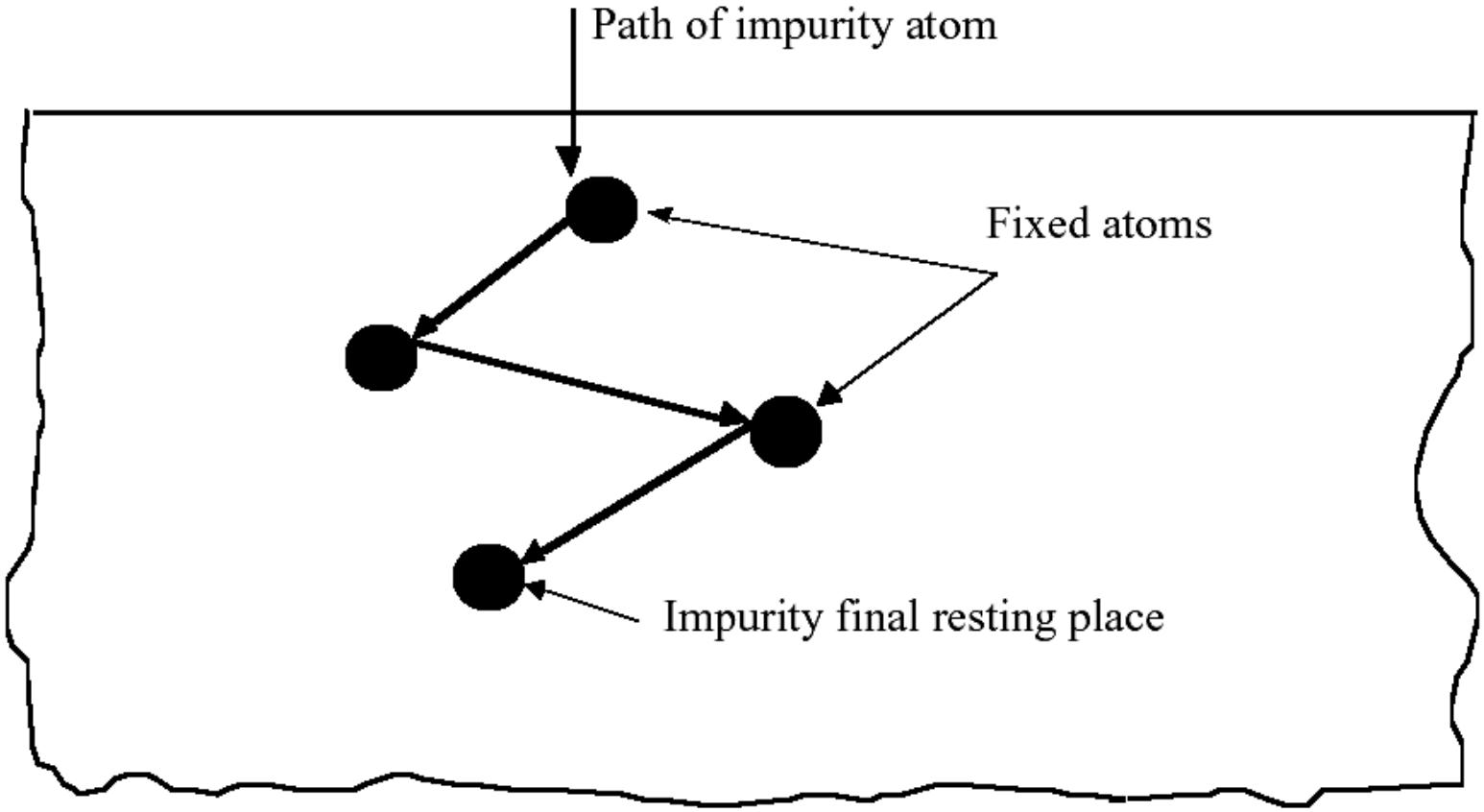


Finite-source diffusion

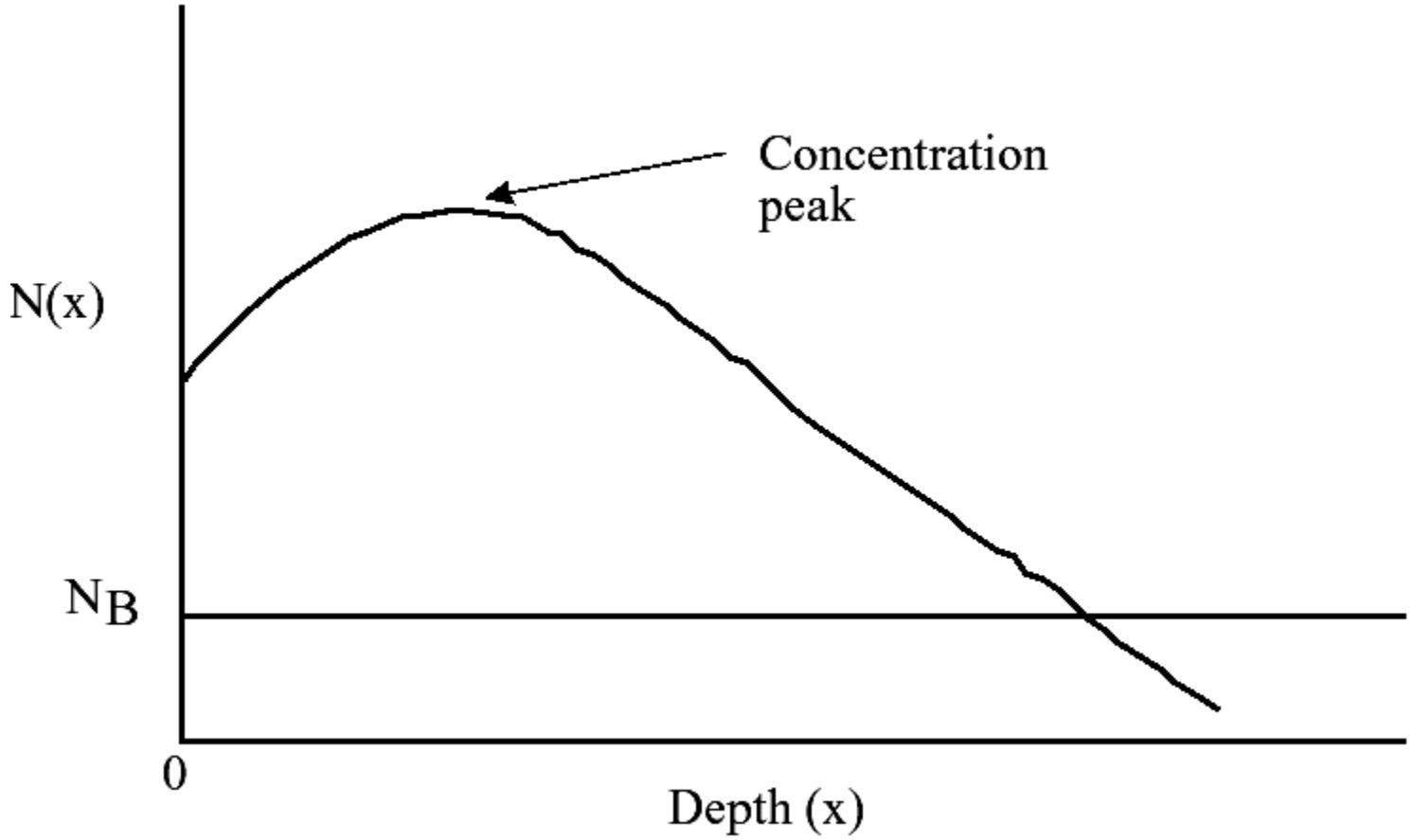


Ion Implantation

The process by which impurity ions are accelerated to a high velocity and physically lodged into the target.



- **Require anneal to repair damage**
- **Can implant through surface layers**
- **Can achieve unique doping profile**



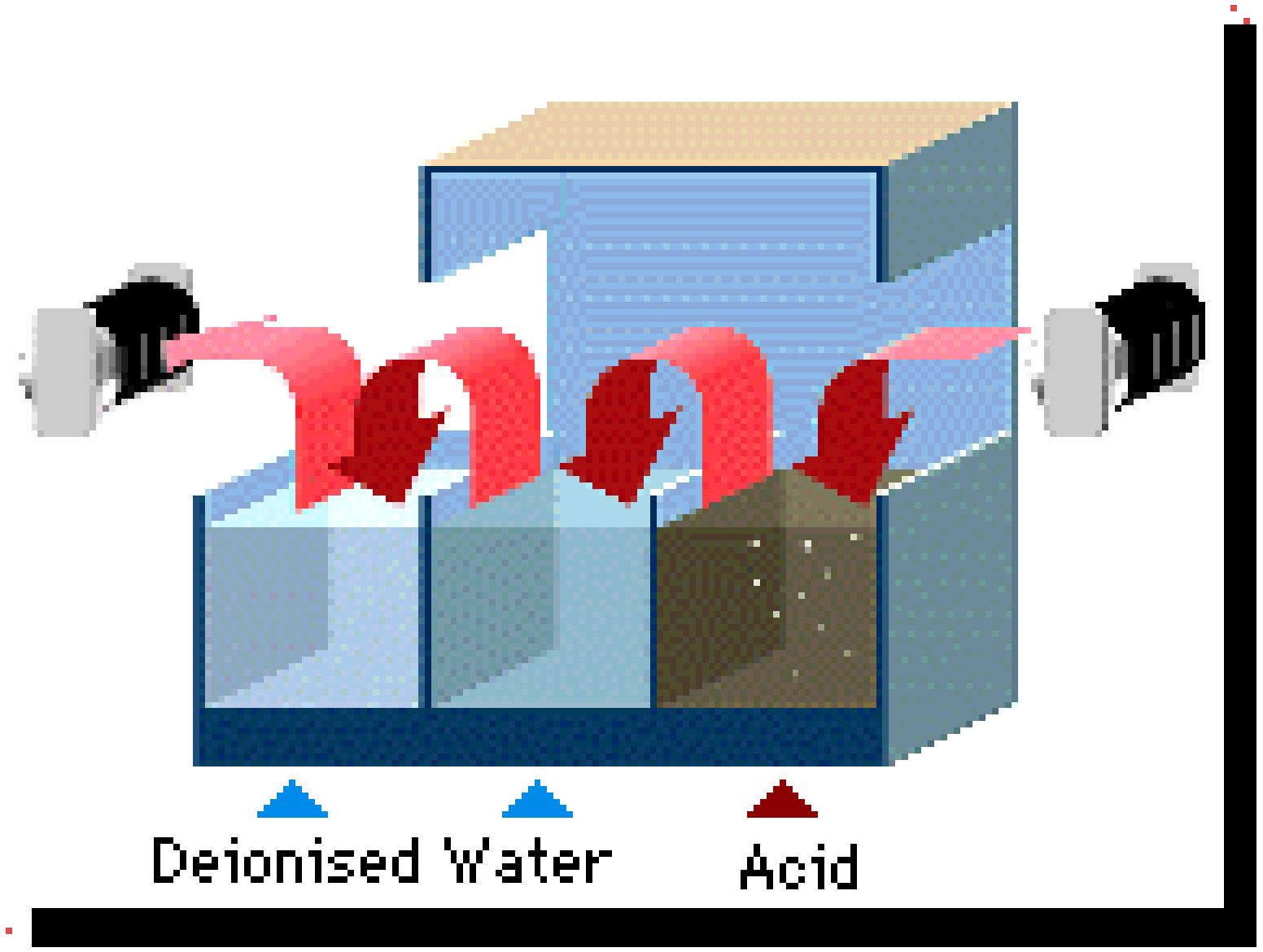
Deposition

- Chemical-vapor deposition (CVD)
- Low-pressure chemical-vapor deposition
- Plasma-assisted chemical-vapor deposition
- Sputter deposition

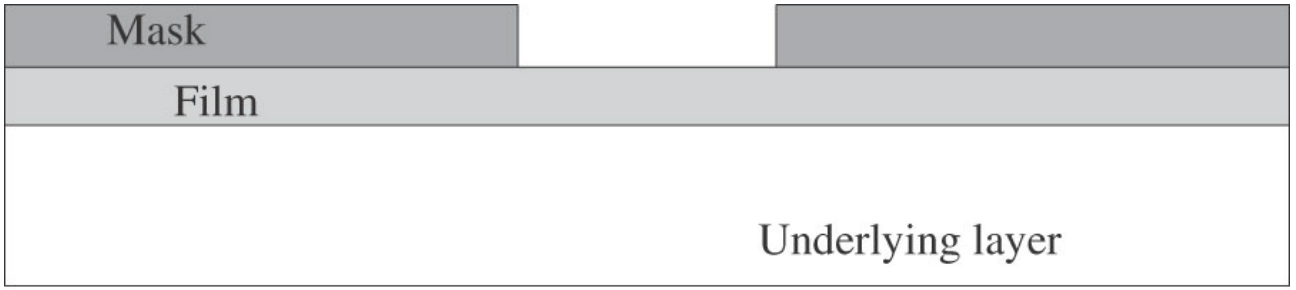
- Materials deposited
  - Silicon nitride (Si_3N_4)
  - Silicon dioxide (SiO_2)
  - Aluminum
  - Polysilicon

Etching

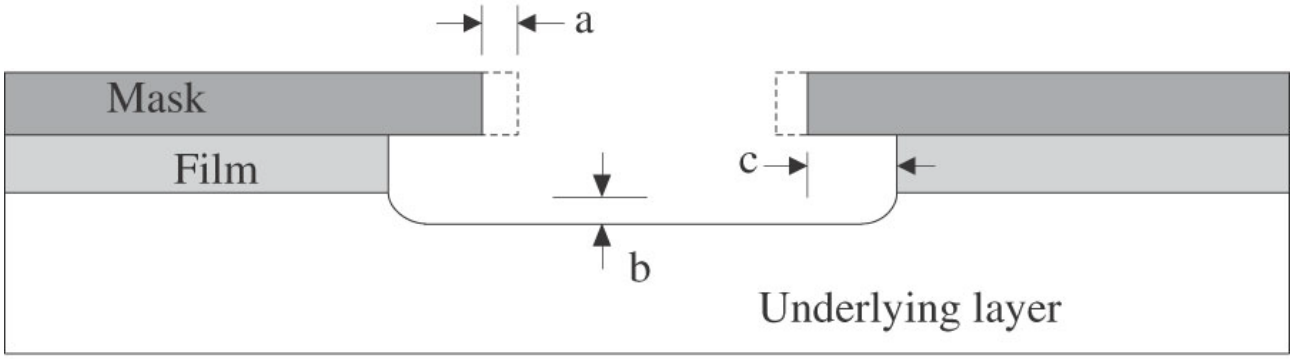
- To selectively remove a layer of material
- But may remove portions or all of
  - The desired material
  - The underlying layer
  - The masking layer
- Two basic types of etches:
  - Wet etch, uses chemicals
  - Dry etch, uses chemically active ionized gasses.


Deionised Water
Acid

- **Selectivity:** $$S = \frac{\text{Desired layer etch rate}}{\text{Undesired layer etch rate}}$$
- **Anisotropy:** $$A = 1 - \frac{\text{lateral etch rate}}{\text{vertical etch rate}}$$



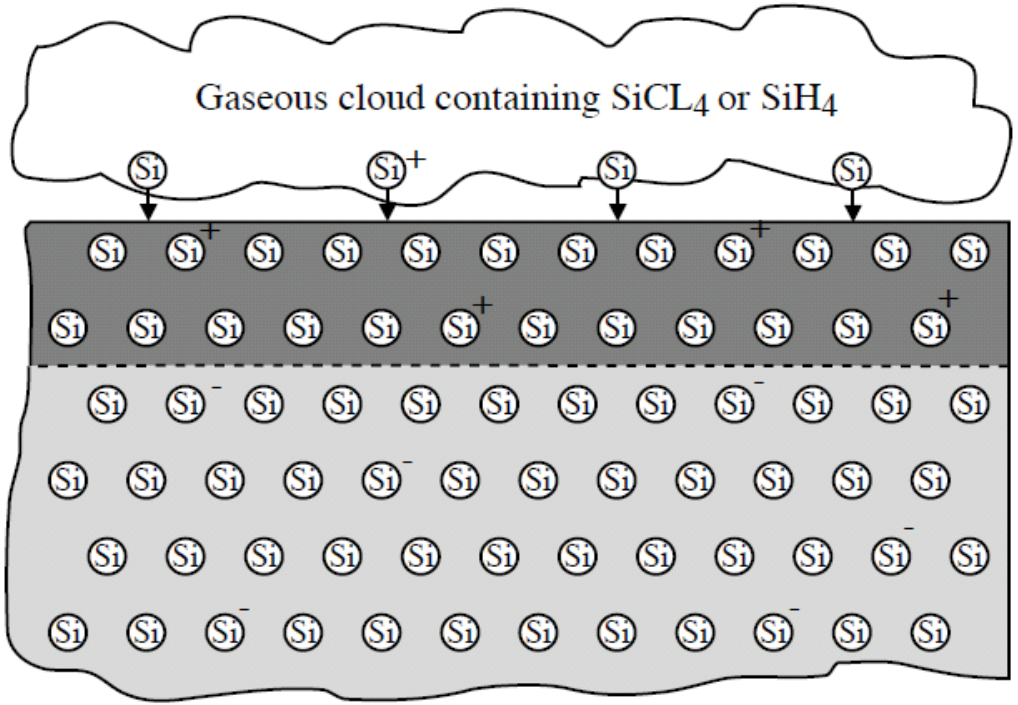
(a)



(b)

Epitaxy

- Epitaxial growth consists of the formation of a layer of single-crystal silicon on the surface of the silicon material so that the crystal structure of the silicon is continuous across the interfaces.
  - It is done externally to the material as opposed to diffusion which is internal
  - The epitaxial layer (epi) can be doped differently, even opposite to the material on which it is grown
  - It is accomplished at high temperatures using a chemical reaction at the surface
  - The epi layer can be any thickness, typically 1-20 microns



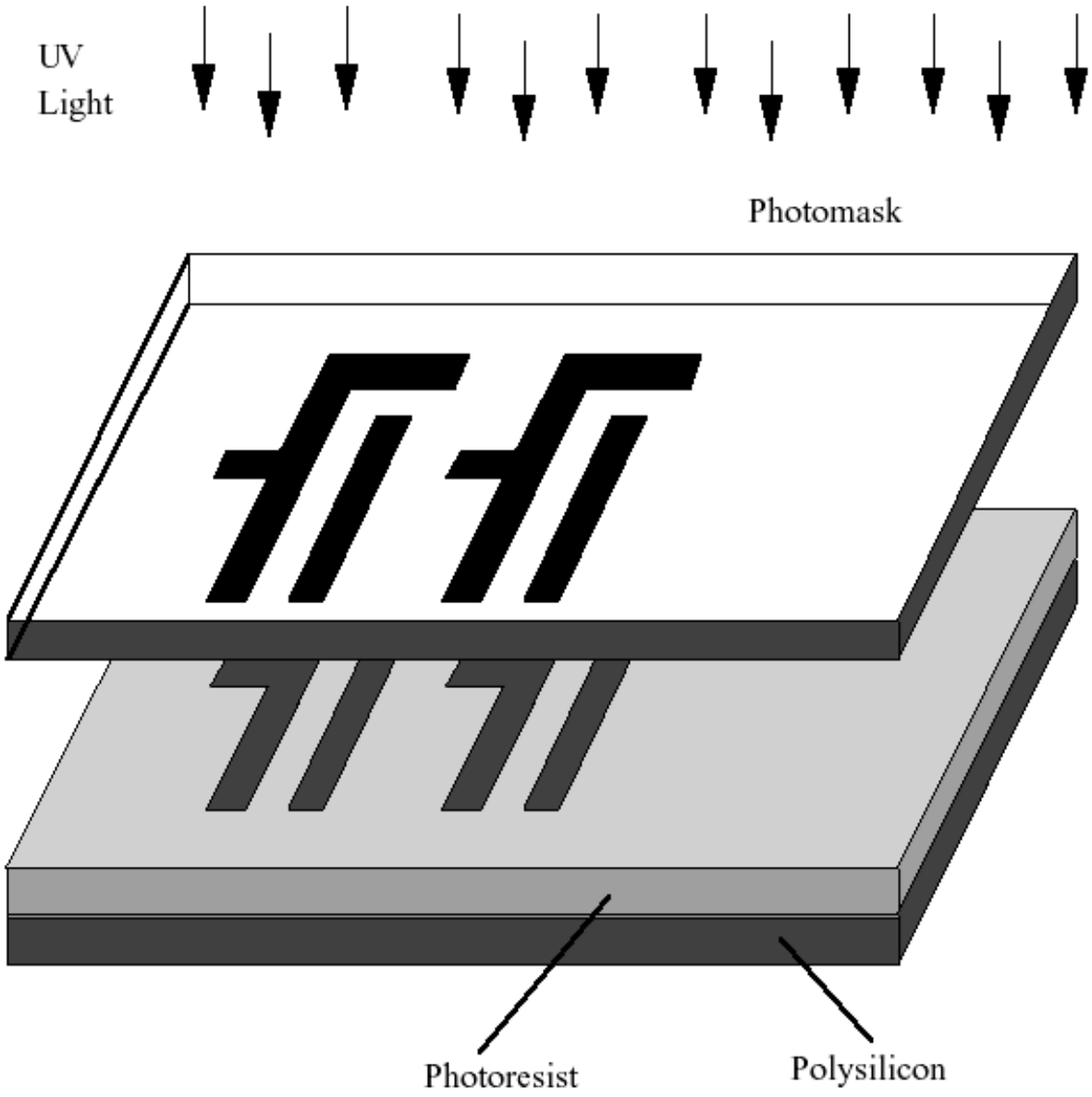
Photolithography

- **Components**
  - **Photoresist material**
  - **Photomask**
  - **Material to be patterned (e.g., SiO_2)**
- **Positive photoresist-**
  - **Areas exposed to UV light are soluble in the developer**
- **Negative photoresist-**
  - **Areas not exposed to UV light are soluble in the developer**

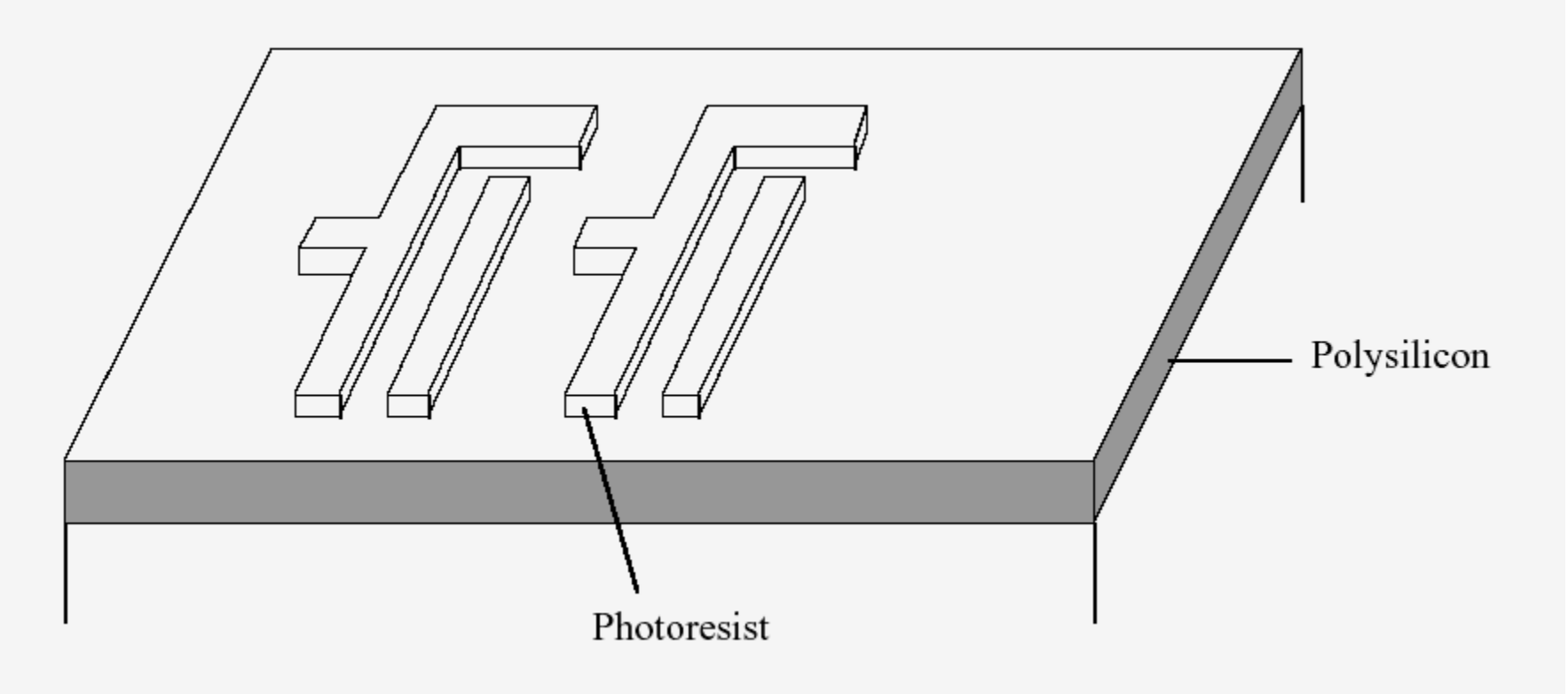
Steps:

1. Apply photoresist
2. Soft bake
3. Expose the photoresist to UV light through photomask
4. Develop (remove unwanted photoresist)
5. Hard bake
6. Etch the exposed layer
7. Remove photoresist

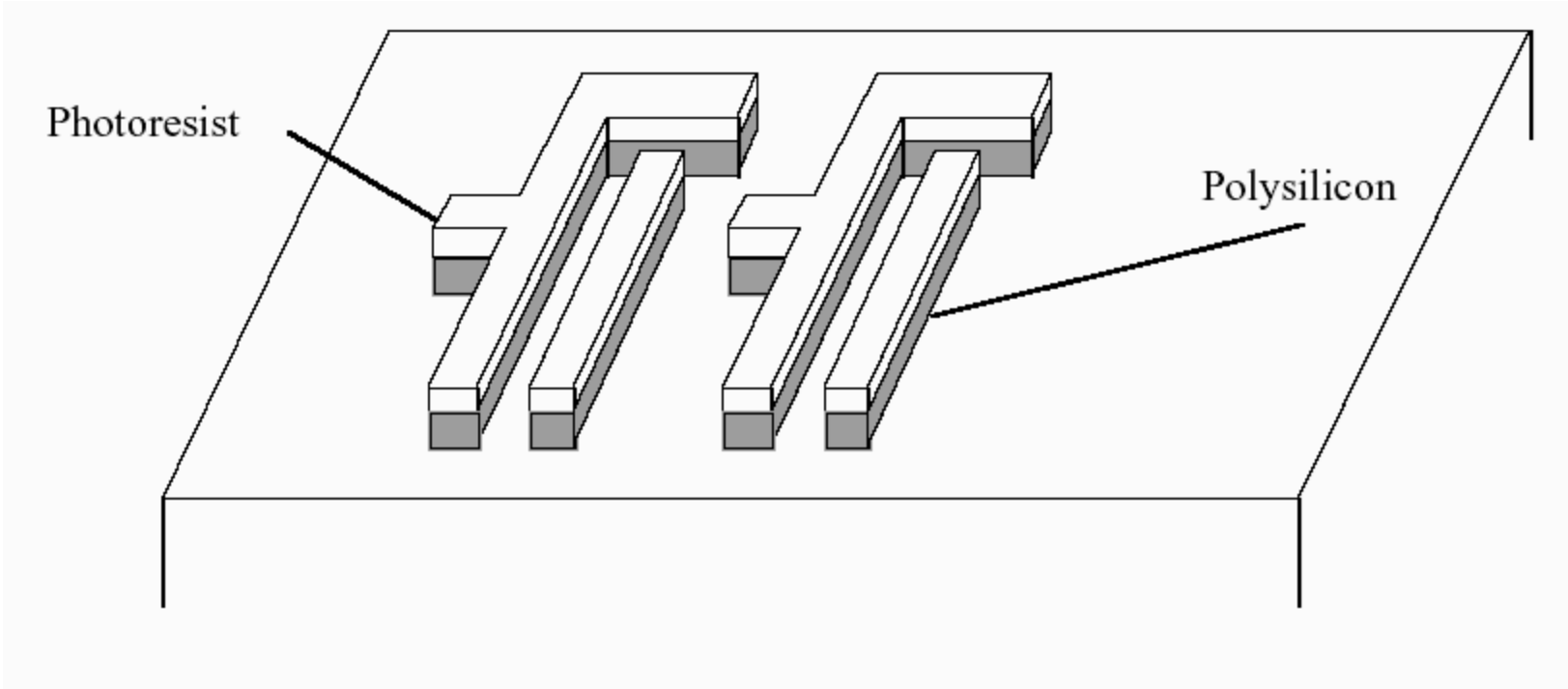
Expose:



After Developing



After Etching



After Removing Photoresist