University of Nevada, Reno

CPE 301 MICROPROCESSOR SYSTEMS DESIGN
FINAL EXAM, Fall 2017

1. The Intel 82C55 Programmable Peripheral Interface chip is designed to be connected to a microprocessor as a memory mapped I/O device which provides 3 additional 8-bit GPIO ports for connecting to external devices. The ports are referred to as PA, PB, and PC in the data sheet.

   Design the address decoding circuit for this 82C55 chip to interface it to an Atmega 2560 processor mapped as external data memory with a start address of 0xC800.

Use **ABSOLUTE** decoding with no fold-back for the external **DATA** memory.

For **CPE406** HW use **PARTIAL** decoding as specified in the HW assignment.

Show your work and include the following items:

a. **MEMORY MAP**
b. **MEMORY ADDRESS TABLE**
c. **BOOLEAN EQUATIONS** for chip select signal
d. Full schematic logic diagram of your **DECODING CIRCUIT**

2. Write an **Atmega2560** *C language function* which will take the an unsigned char variable and output it to the 82C55 (as mapped in Question 1) port PC is connected to a standard 8-bit printer with the **following characteristics**.

Note that this function will output only one character each time it is called.

Be sure to define all the necessary global pointers.

The output of port PC is connected to the **input data lines** of a standard 8-bit printer. Two control signals are used for handshaking. First, the active high BUSY signal from the printer tells the computer that it must wait before sending another character to the printer - when BUSY goes low then it is OK to send the next character. Second, the active low /STROBE signal is sent from the computer to the printer telling the printer that the data lines contain valid data. The sequence of events is shown in the timing diagram below. Thus, the function must accomplish the following: 1) wait for the BUSY signal to go low, 2) output the data to port PC, 3) set the /STROBE signal low, and 4) set the /STROBE signal back high.

ASSUME: 82C55 is already initialized and PA and PC are set for output, and PB is set for input.

The input BUSY signal is connected to the 82C55 PB bit 7.

The output /STROBE signal is connected to the 82C55 PA bit 3.

Printer Timing Diagram

The timing diagram below illustrates the data and handshake lines during transfer of one data byte to the computer. DATA 1 through DATA 8 and the Strobe line are driven by the computer.

Printer Timing

Interval	Description	Minimum Value	Typical Value
T_{ds}	Delay from DATA written to data Strobe.	0.5 µs	
T_{str}	Data Strobe width.	1 µs	
T_{dh}	Duration of valid data after Strobe.	0.5 µs	
T_{sb}	Delay from falling edge of Strobe to rising edge of Busy.	0.5 µs (max)