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EE 421: Digital Electronics

LED Blink

For the LED blink project I used the code from the assignment and implemented the 32 bit clock (figure 1). I then set different bits of the clock to correspond to different LED's, the last bit blinking at 50MHz (every 85 seconds) and the 25th bit blinking about every 1.3 seconds. The register transfer level (RTL) diagram is shown in figure 2, the DE1 LED port map is shown in figure 3, and the simulation result is shown in figure 4.

```

1  LIBRARY IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  use IEEE.STD_LOGIC_ARITH.ALL;
4  use IEEE.STD_LOGIC_UNSIGNED.ALL;
5
6  ENTITY blink IS
7  PORT(
8      clk : IN STD_LOGIC;
9      dir : IN STD_LOGIC;
10     count_out : OUT STD_LOGIC_VECTOR(31 DOWNTO 0)
11 );
12 END blink;
13
14 ARCHITECTURE behavioral OF blink IS
15     SIGNAL count_int : STD_LOGIC_VECTOR(31 DOWNTO 0) := "00000000000000000000000000000000";
16
17 BEGIN
18     PROCESS(clk)
19     BEGIN
20         IF clk = '1' AND clk'EVENT THEN      --if rising edge
21             if dir = '1' THEN                  --clock direction
22                 count_int <= count_int + 1;
23             ELSE
24                 count_int <= count_int - 1;
25             END IF;
26         END IF;
27     END PROCESS;
28
29     count_out <= count_int;
30 END behavioral;

```

Figure 1: VHDL LED Blink Code

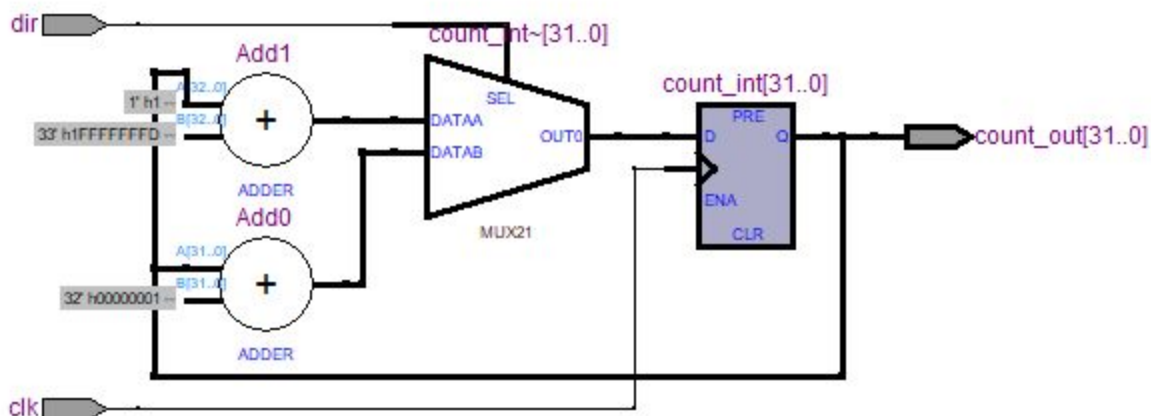


Figure 2: RTL of the Counter Circuit

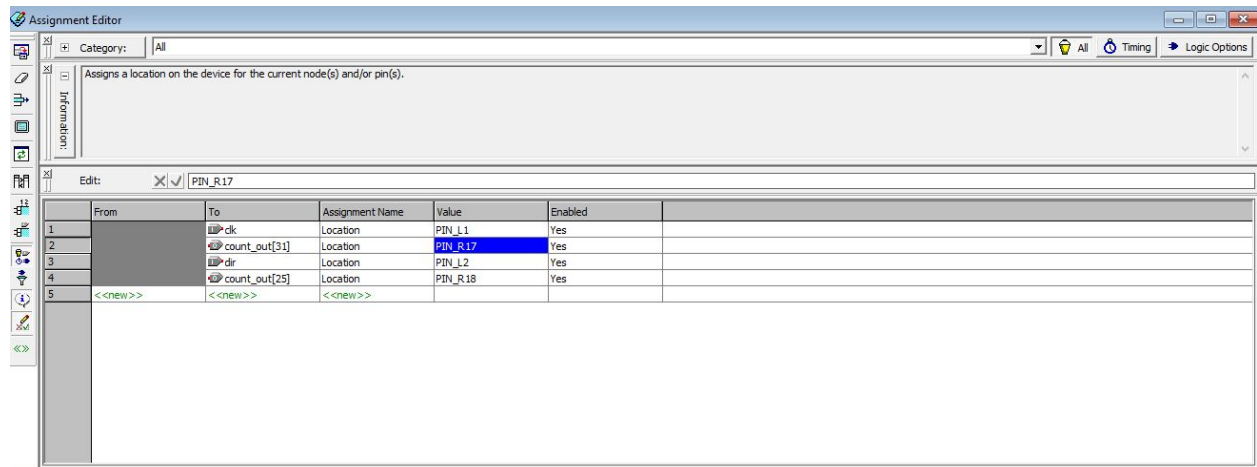


Figure 3: The DE1 LED Port Map

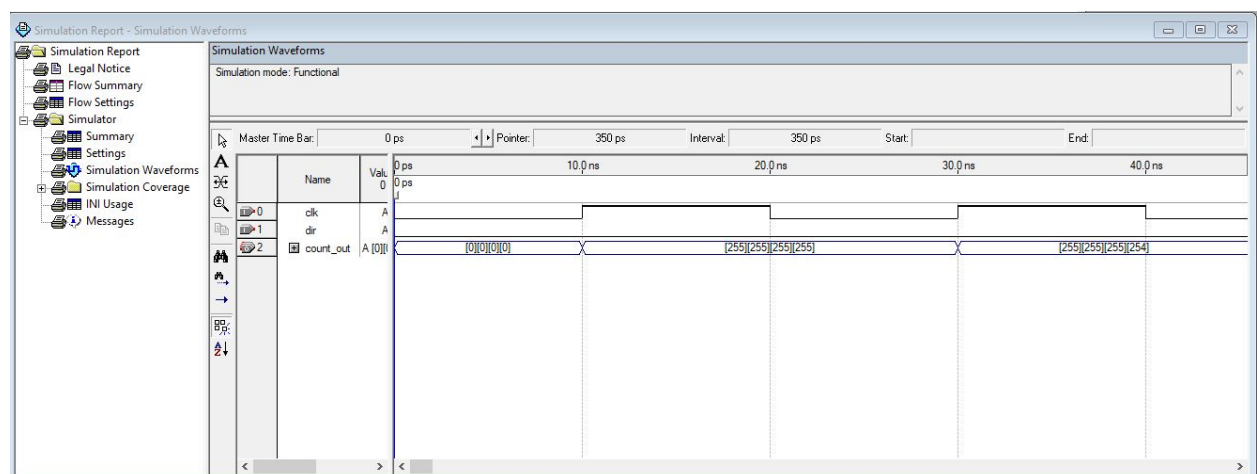


Figure 4: Simulation Results