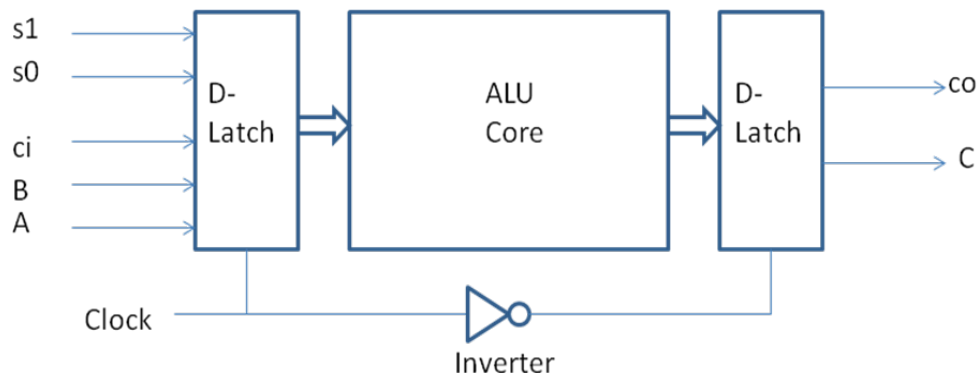


EE421/621 Digital Electronics
Department of Electrical and Biomedical Engineering
University of Nevada, Reno

Project1 – ALU Design:

In this project, a 4-bit Arithmetic Logic Unit (ALU) is required to be designed. This ALU takes as inputs two 4-bit words (A and B in 2's complements), a 2-bit instruction (s0 and s1) and a carry in bit (ci) and produces as outputs a 4-bit result (work C) and a carry out bit (co). To synchronize the flow of data through the ALU, a system clock (Clock) is used to indicate when the inputs/outputs are valid. (An anticipated structure is illustrated as below but you can design your own using DFFs)



The ALU is able to perform the following operations:

Instruction (s ₁ ,s ₀)	Carry-in Bit (c _i)	Function	Resulting Operation
0,0	0	Transfer A	C=A
0,0	1	Increment A	C=A+1
0,1	0	Add A to B	C=A+B
0,1	1	Add A to B+1	C=A+B+1
1,0	0	Subtract B from A-1	C=A-B-1
1,0	1	Subtract B from A	C=A-B
1,1	X	Bitwise XOR A and B	C=A XOR B

Basic requirements on the project:

- (1) Design the circuit using VHDL codes
- (2) VHDL code for this circuit should be at register transfer or gate level. In other words, various modules talked in the class are expected to be used for build the ALU circuit. In your code, these modules can be described in behavior or RTL level. PORT MAP structures are encouraged in the VHDL coding, and you can breakdown 4bit-addition to the gate level.
- (3) Your project report should clearly present
 - a. the design procedures of your circuit (what modules did you use, how did you use the modules to realize the circuit functions, how did you design the control logic for the instructions, etc)
 - b. VHDL codes