**BUG 1:**

**Source Day 1/Two\_Wire\_SPI**

A screenshot of a social media post

Description automatically generatedA screen shot of a video game

Description automatically generated

Looking at pictures of bug 1 when the bottom half of getting errors generating bitstream error is “[Synth 8-27] else clause after check for clock not supported”

A screen shot of a video game

Description automatically generated

A screenshot of a social media post

Description automatically generated

The code was fixed by removing the elseif clause and replacing it with an if. This didn’t break simulation and can now generate bitstream 😊

**BUG 2:**

**Source Day 1/LED Control**

A screenshot of a social media post

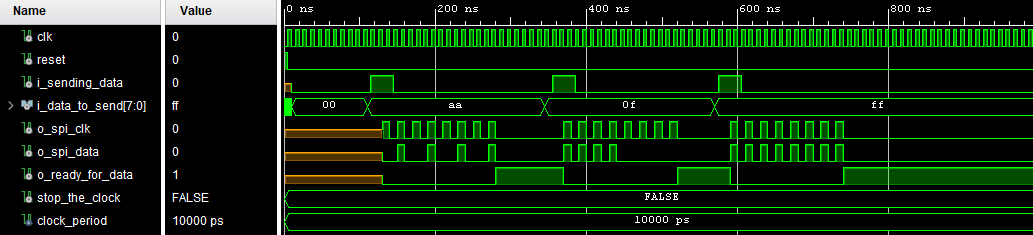
Description automatically generated

This code is suppose to use the two\_wire\_spi source to send some pixel data. It should be sending “00000000” for the first 4 transmissions but this doesn’t work. The outputs are just U I suspect this is due to the actual two\_wire\_spi code. You can see here we are waiting for ready\_for\_data to be high before sending anything. I think that the code is not initializing the o\_ready\_for\_data from the two\_wire\_spi source to be 1 initially. The testbench is shown below for led\_control.

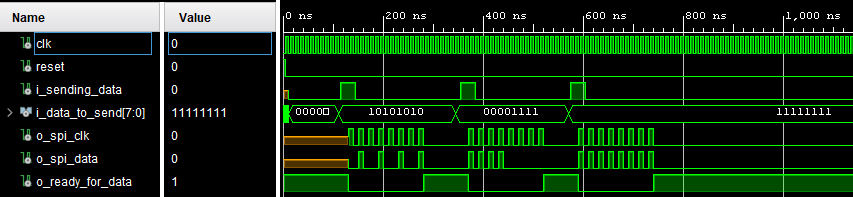
A screenshot of a computer

Description automatically generated

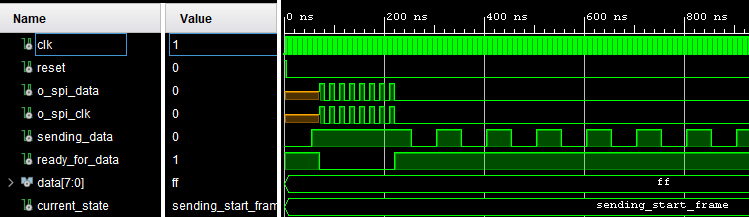
Below is the testbench of the two\_wire\_spi source which verifies my suspicions.



Below is the test bench for two\_wire\_spi fixed



Retesting the led\_control reveals a successful testbench now I just need to complete the code



**BUG 3:**

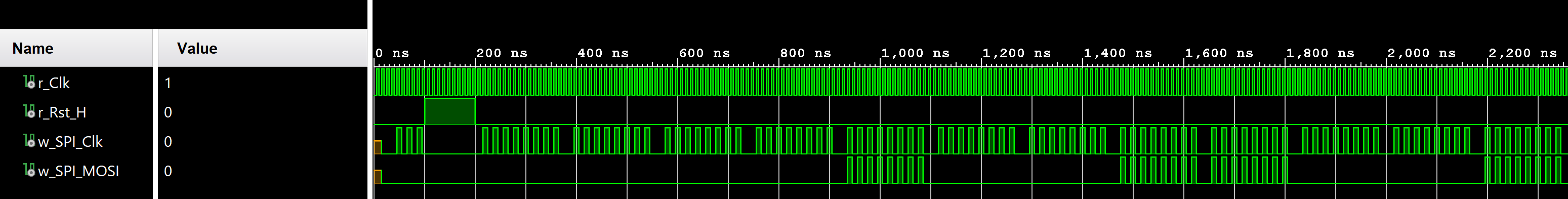
**Source Day 1/Two Wire Spi**

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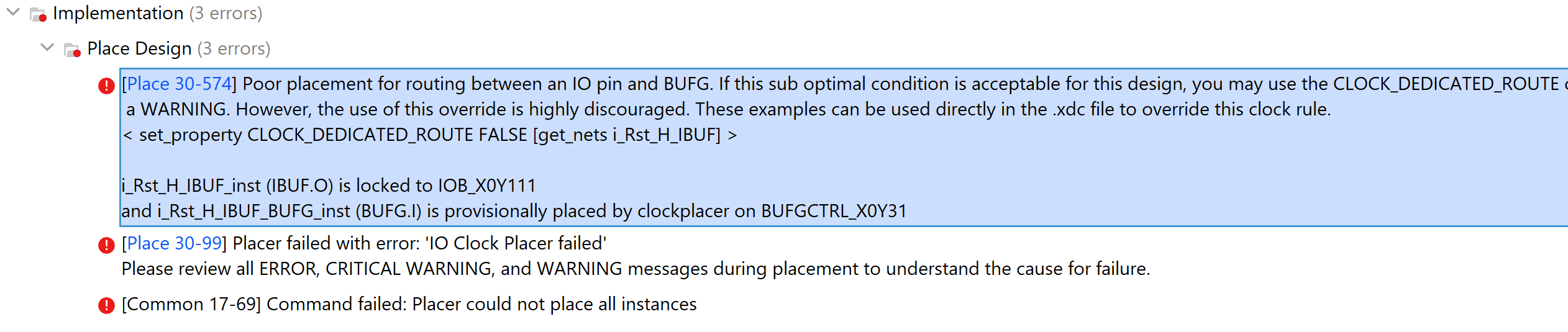
**Bug 4:**

**Source Day 2/Addresable\_Strips**

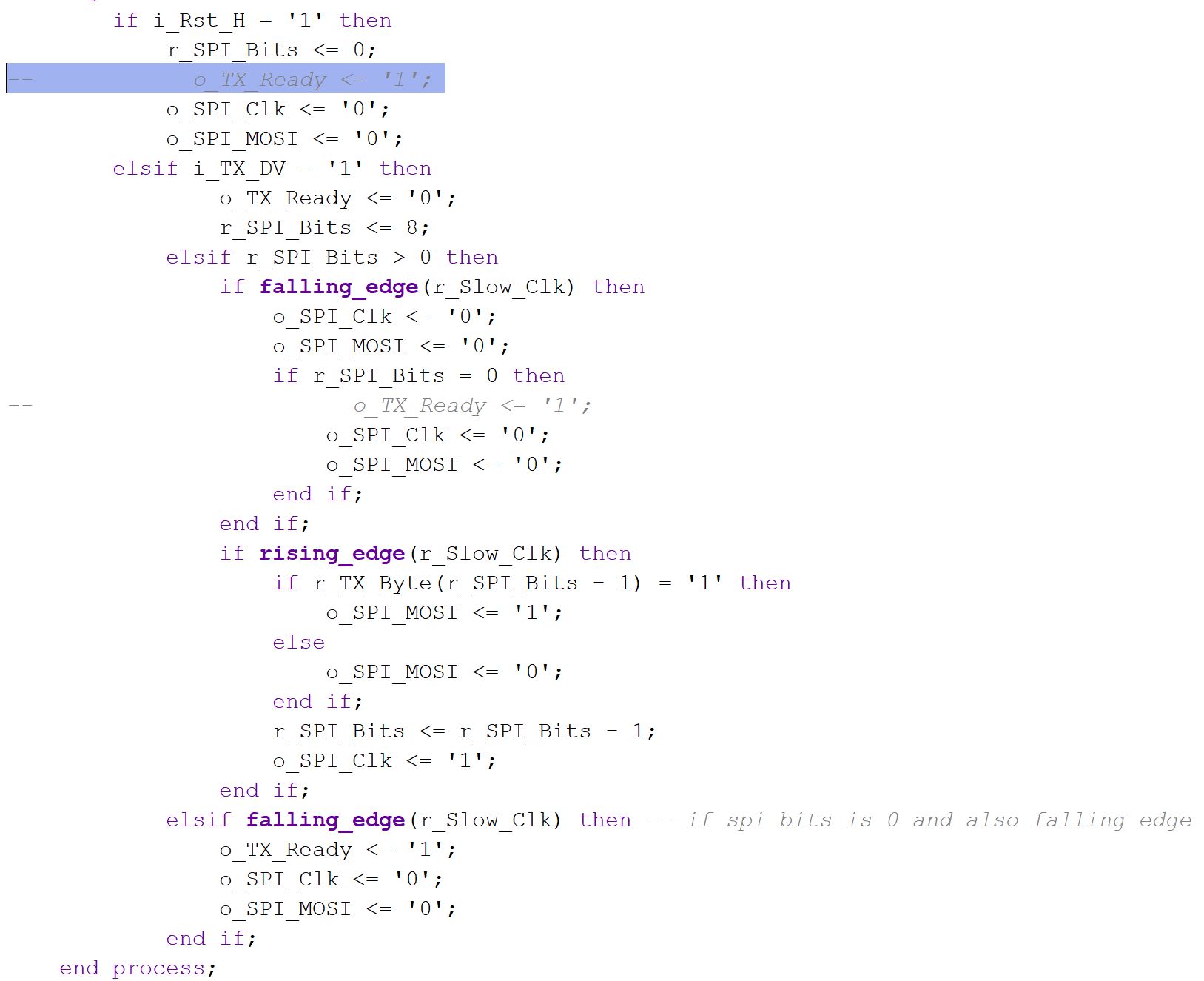
I decided to completely rewrite all the code I made and although I lost some time I managed to do everything eventually simulation below for just the start frame and the first two leds.



However even though I have no errors in the code and the simulation nworks fine now I can’t generate bitstream because of this error….



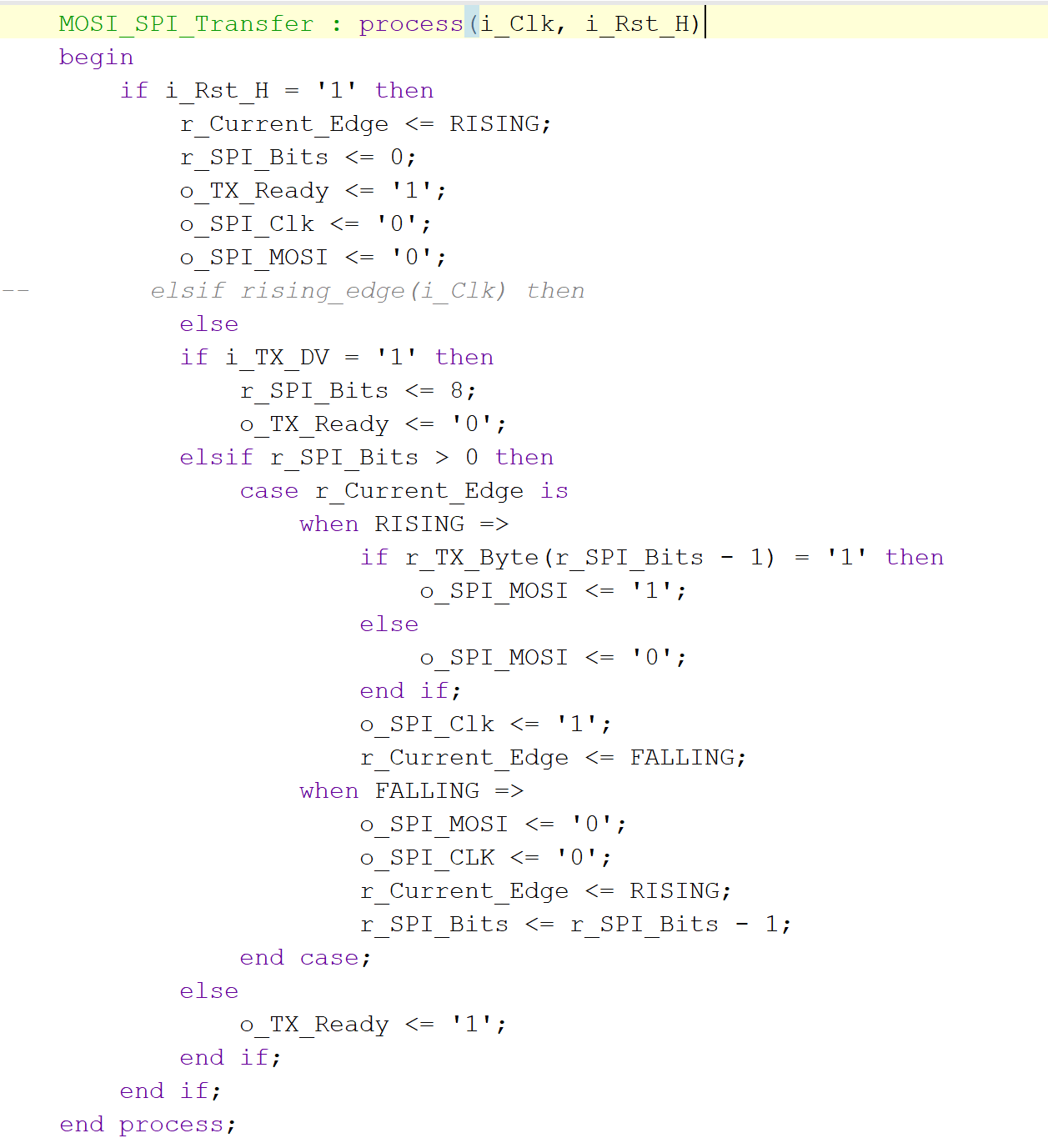
After like 2 hours of debugging I found the issue……. The highlighted line when uncommented caused the error. I have no idea why this isn’t a clock.

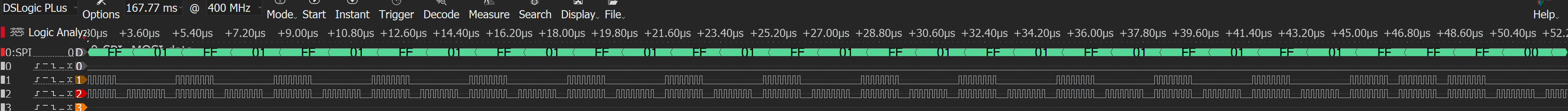


**Bug 5: Day 3**

No pictures for this but even though my simulation is working every time I upload my code nothing is coming up on the FPGA when I probe with my logic analyser. I have confirmed that it’s not the issue with the logic analyser as I have tested other codes on the same pins and they worked. I even drove the spi pins with a clock directly and that worked but when I try to display the spi output it just stays low. I am pretty sure the spi code needs to be improved so I guess I’m going to rewrite it for the third time.

I fixed the problem with no output showing I suspect its to do with the fact that I was doing stuff on rising and falling edges before. Now I only do stuff on rising edges





Success!! I just have an issue where the o\_tx\_ready which signifies that the spi bus is no longer busy is hanging for too long which accepts multiple spi transactions while actually only proessing one.