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# **LLC resonant converters: an overview of modeling, control and design methods and challenges.**

Claudio Adragna

November 2022

*Dedicated to Anna and Alberto*

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## ABSTRACT

The LLC resonant converter is perhaps today's most popular resonant conversion topology. Yet, though in existence for many years, only relatively recently has it gained the popularity it certainly deserves. Since its first appearance in the literature in 1988, it has been confined for a long time to niche applications: high-voltage power supplies or high-end audio systems, to name a few.

Its significant industrial usage started in mid 2000s with the boom of flat screen TVs, whose power supply requirements found in the LLC resonant converter their best answer, and was fueled by the introduction of new regulations, both voluntary and mandatory, concerning an efficient use of energy. This combination of events pushed power designers to find more and more efficient ac-dc conversion systems.

Since then, several other mass-produced electronic devices, such as All-In-One and small form factor PCs, high-power ac-dc adapters and LED drivers, have made a massive usage of this topology, especially in its half-bridge version. Higher power systems, such as server and telecom power supplies and, more recently, charging stations for electric vehicles, have adopted mainly the full-bridge version.

Over these last three decades, there has been a lot of progress on both theoretical and practical aspects related to the LLC resonant converter. Lots of papers and application notes deal with it, and many IC manufacturers have dedicated driver ICs in their portfolio. Despite that, its design is still considered a challenging task in Power Conversion. Thus, a guided tour through its intricacies may be beneficial to both the neophyte and the experienced engineer.

The paper will cover from the basics (operating modes, soft switching mechanism, first-harmonic approximation, etc.) to some advanced topics (design optimization, control methods, synchronous rectification, interleaving, etc.) using a hands-on, design-oriented approach.

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# PART I

## INTRODUCTION TO RESONANT CONVERSION

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### Chapter 1

#### Background

Since the beginning of the electronics era, users' needs have dictated a clear trend towards size and weight reduction of electronic equipment. Of course, this trend has affected power supply systems as well, as essential sub-systems for the proper operation of the equipment.

Essentially all electric equipment may benefit from size and weight reduction of their power supply. In mobile applications such as transportation, this directly translates into fuel saving or increased operating range. For portable equipment, being smaller, lighter, yet more powerful, is perceived by users as an added value. Stationary applications take advantage of a lower size and weight of power supplies as well: this makes more space available for the primary function of the installation and cuts the total cost of ownership by making installation and maintenance easier and quicker.

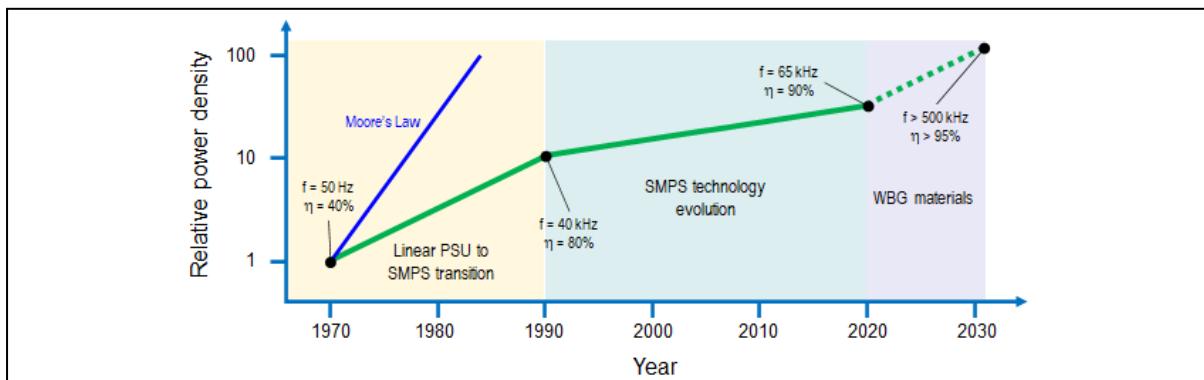
In power supplies this trend is expressed by a constant demand of higher *efficiency* and *power density*, two quantities that always go hand in hand.

Efficiency is the ratio of the power output by a power supply unit (PSU) to the power that the PSU draws from the input source, being their difference (power loss) converted into heat.

Power density is a Figure of Merit (FOM) that measures the degree of compactness of a PSU. Depending on the key design goal, it can be defined in different ways, typically as the ratio of its rated power to its volume ( $\text{W/cm}^3$ ) or its weight ( $\text{W/kg}$ ) or scaled equivalent units. Whichever definition we consider, either volumetric or gravimetric, the power density trend can be synthesized in “packing more power in less space”.

While the progress in circuit integration technology has substantially reduced the size and weight of all electronic devices, in general the miniaturization rate of power supplies has not been keeping the same pace.

**Figure 1. Power density trajectory in typical commercial offline power supplies.**



Different types of power converters (ac-dc, dc-dc, point-of-load, voltage regulator modules, etc.) show different miniaturization rates. In this context we will focus on ac-dc converters, i.e., those used in power supplies operated off the ac power distribution line, the so-called *offline power supplies*.

As shown in figure 1, while integrated circuit technology evolves following Moore's Law, doubling the density of transistors every approximately two years, in the last fifty years on average it takes about one decade to offline power supplies to double their power density [1]. The reasons for this slower speed will be briefly reviewed in the continuation of this discussion.

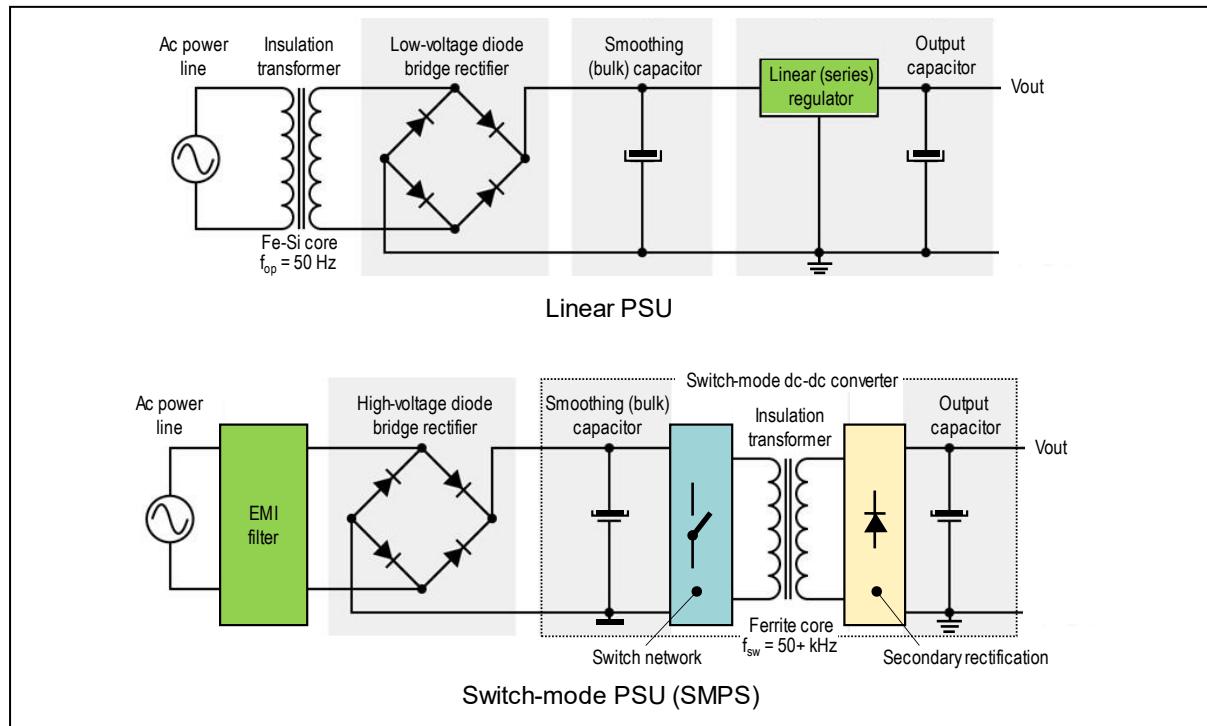
This race for higher power density started with the epochal transition from linear to switch-mode power supplies, which took place at the end of the sixties of the past century, enabled by the advent of high-voltage bipolar junction power transistors (BJT) and the development of low-loss ferrites.

Linear power supplies (see figure 2) do not offer much opportunity for power density increase because size and weight are essentially dictated by the bulky line-frequency insulation transformer based on silicon iron laminations, and the heatsink. As to the heatsink, there are limited chances to reduce its size because the efficiency of linear power supplies is low and related to the input and output voltages only.

On the contrary, switch-mode technology does not need a line-frequency transformer (see fig. 2) and requires smaller heatsinks (or no heatsink at all in some cases) due to their higher efficiency and consequent lower amount of heat generated.

After the initial fast increase due to the linear to switch-mode transition, which represented a groundbreaking moment, in the last thirty years power density in offline power supplies has slowly increased at a rate lower than 10%/yr, despite important technology milestones such as the introduction of high-voltage power MOSFETs, which replaced BJTs, and the advancements in power magnetics.

**Figure 2. Transition from linear to switch-mode technology marked a quantum leap in size and weight reduction of offline power supplies.**



This slower progress in power density, can be explained also with a change of focus: in the early nineties, the rapid diffusion of consumer electronics and an increased attention to environmental concerns prompted the introduction of requirements and regulations concerning light-load efficiency and standby consumption. This oriented R&D efforts towards complying with these new specifications that demanded an efficiency improvement over the entire load range and not just at full load as required by the power density targets.

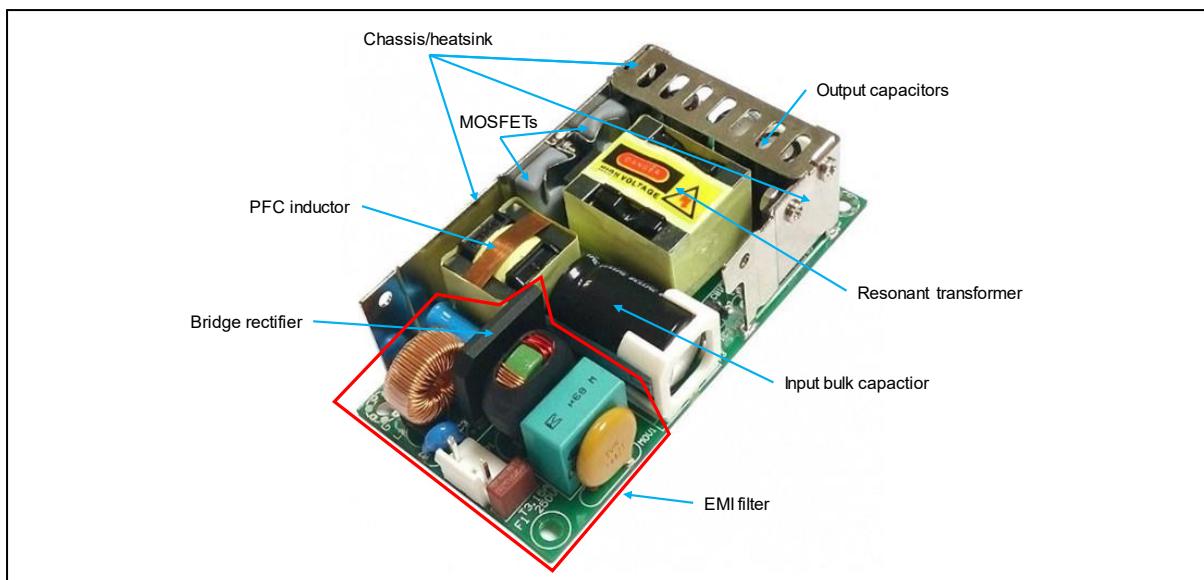
Today, the tremendous growth of portable equipment has put power density again under the spotlight. With the advent of wide-bandgap materials, namely SiC and GaN, power supply industry seems to be on the verge of another fast growth period for power density, even for offline power supplies.

Why are offline power supplies (an example is shown in figure 3) so difficult to miniaturize? Safety isolation (to prevent electric shock hazard), the holdup time (we need energy reservoir to keep the supplied equipment operating even during short interruptions of the ac line voltage), and the electromagnetic compatibility (EMC) requirements (not to adversely affect the operation of other electronic equipment, nor to be adversely affected by other equipment or other electric phenomena) as well as the high voltages that they are required to switch, pose quite severe obstacles in their path to miniaturization.

Though the objective is to make PSUs smaller and lighter, the ultimate technical requirement is to make them more efficient. The reason is straightforward: if we handle a given power in a smaller volume, there will be less surface area for cooling and less room for heatsinks.

It is true that this issue can be tackled also from a different angle: improving the thermal design to facilitate heat removal. However, this strategy can be pursued just to some extent. Fans can be used in some applications only (e.g., telecom or server power, ATX/PS2 PC) and are out of consideration in others (e.g., ac-dc adapters and chargers for mobile equipment) for obvious reasons of user experience. Encapsulated power supplies can benefit from filler materials and other mechanical provisions that facilitate heat exchange but there are regulatory limits on the touch temperature, i.e., on the maximum surface temperature of the enclosure. In the end if we want to increase power density we must generate as little heat as possible, which is another way to say that we need to aim at high efficiency.

**Figure 3. An offline power supply with its bulky parts.**



Switch-mode technology is based on storing and/or transferring energy through magnetic (inductive) components, so that increasing the switching frequency brings lower inductance values and, as a general consequence, a size reduction of these devices and in some cases also of the capacitive energy reservoirs. Increasing switching frequency, therefore, is a mainstream towards smaller size PSUs. Unfortunately, also this is true only to some extent and conflicts with the requirement of high efficiency.

Switching losses and electromagnetic interference (EMI) both increase with switching frequency and any attempt to reduce switching losses by switching faster will cause more EMI that will need a bulkier filter or other provisions to be kept within the limits. Of course, slowing down switching to reduce EMI causes higher losses and impairs efficiency. This points out the need for conversion systems characterized by a low rate of rise of switching losses with frequency and, on the other hand, by a low level of EMI emissions, so that these can be kept below the regulatory limits without bulky filters (which is essential to increase power density).

Hard-switched PWM converters (intended as the classical switch-mode power processors such as buck, boost, etc. and their isolated versions flyback, forward, etc., converters that are typically controlled with a form of pulse-width modulation), can run very efficiently but not at a high switching frequency. The term “hard-switched” stems from the way switching occurs in the power devices (power switches and rectifiers) of these converters. This is commonly referred to as hard switching because it involves significant peaks of power dissipation due to voltage and current being simultaneously high during the transition from one state to the other. These peaks are repeated at the switching frequency, so the higher the frequency is, the larger the average power dissipation will be. These concepts will be expanded in Part II, chapter 2.

A careful design and component selection may resolve part of the efficiency-EMI compromise but simply raising the switching frequency and carefully designing the converter is not sufficient: the entire process of power conversion needs to be reconsidered for high efficiency and low EMI to increase power density via higher switching frequencies.

The reason for the keen interest that resonant converters have always attracted is that they apparently solve all the issues related to conventional hard-switched PWM converters, offering significant advantages as summarized in the following list:

- Soft switching (zero-voltage switching, ZVS, and/or zero-current switching, ZCS) significantly reduces switching losses and the energy needed to drive power switches.
- Smooth waveforms, with relatively low  $dv/dt$  or  $di/dt$  stress, which relieves the strain on power components.
- Parasitic elements are part of the power processing circuit: they work *for*, not *against* the just cause of an efficient power conversion; therefore, there is no need for snubber and clamp circuits to limit unwanted and dangerous voltage and current spikes that inevitably bring additional power losses.
- Low EMI, because of both the smooth waveforms and the less noise produced by the parasitic elements; filtering requirements are less demanding.
- As a result of all the above merits, high-efficiency, high switching frequency and high power density are more easily attainable.

However, dealing with resonant converters is not exactly a bed of roses:

- Resonant converters work in a completely different manner as compared to PWM converters. They may present multiple operating modes, so they are more complicated and difficult to analyze. Both the static and the dynamic transfer functions are usually strongly nonlinear, often beyond the area of simple mathematical descriptions. This,

along with the enormous diversity in the resonant converter world, may force power designers to carry out a detailed design study before selecting a topology and its modes of operation to meet a particular set of requirements.

- In most cases their nice properties are obscured by significant drawbacks (e.g., large peak voltages or rms currents, or too wide range of operating frequency).
- Resonant converters can be designed to be highly efficient in a narrow range of operating conditions. Obtaining good performance over a wide range of load currents and input voltages is difficult, in some cases practically impossible.
- Significant reactive currents may circulate in the tank circuit even when the load is removed, leading to poor part-load efficiency
- Simulations tools (e.g., Spice, PSIM, Simetrix, ...) are helpful as a verification means but do not give much insight in overall behavior and do not provide a fast and effective way of optimization.

Additionally, there are limiting factors preventing higher frequency and power density that resonant converters attenuate just slightly or do not remove at all:

- Eddy currents in ferrite cores, skin and proximity effects in copper conductors are a major source of losses in power transformers that tend to rise significantly with the switching frequency. The smooth waveforms of resonant converters do not help much.
- For converters operated directly from the power line, resonant operation does not loosen isolation requirements nor enables any size reduction in the ac-dc front-end (input bridge plus bulk capacitor).
- Though resonant converters are more EMI-friendly, the parasitic elements in the components of the filter (essentially the equivalent series resistance, ESR, and equivalent series inductance, ESL, of capacitors, and the end-to-end capacitance of inductors and chokes) make the EMI filter ineffective at higher frequencies anyhow.
- The higher the switching frequency, the more the noise generated by the power switches makes the layout particularly critical to converter's performance.
- Conduction and driving losses in switching devices. These losses cannot be eliminated but the emerging technologies of SiC and GaN switching devices, which approach ideal switches better than silicon, are making this limiting factor less and less important.

Among the crowded multitude of resonant topologies appeared in the literature and industry in the semicentennial history of resonant conversion, in the last decade one topology has emerged and conquered a dominant position: the LLC resonant converter.

Nowadays, this converter is at the heart of the power supply in a wide range of electronic equipment powered from the ac line (see figure 4). This includes consumer applications (Desktop and AIO PCs, TVs, high-power ac-dc adapters and chargers for laptop PCs), lighting applications (street lighting and industrial lighting luminaires, high power LED drivers), telecom, server and cloud computing power, medical equipment, EV chargers and even open frame power supplies.

Whenever the power level approaches hundred watts, so that it cannot be adequately served by flyback converters, or even at lower power levels when there are special requirements on efficiency or form factor constraints, the LLC resonant converter is prevalent.

At lower power levels (say, up to 500W) the half-bridge implementation is the most common, at higher power levels designers prefer the full-bridge implementation. Of course, there is no clear boundary: as usual it all depends on the specifications and requirements of the system as well as on cost targets.

**Figure 4. Typical applications and power supplies using the LLC resonant converter.**



In some cases, the LLC converter has enabled to build the equipment as we see it today (for example, flat screen TVs with the internal power supply); in other cases, it has dethroned other topologies, like in the case of the desktop PC power supply, where it has almost replaced the forward converter, or the telecom power supply where it has significantly undermined the supremacy of the phase-shift full-bridge converter.

There are other resonant conversion topologies offering the favorable characteristics that we mentioned earlier, so what are the reasons of the success of the LLC converter?

In author's view the most sensible short answer is that the LLC resonant converter provides these benefits at the lowest level of design compromise. In other words, it offers nice properties without heavy drawbacks: it can operate both as a step-up and a step-down converter (this concept will be clarified in the following) with limited voltage stress across the semiconductor devices and an rms-to-dc ratio of primary and secondary currents only slightly larger than unity. Additionally, a wide range of output power (including no-load conditions) can be controlled with a relatively narrow variation of the operating frequency and always maintaining soft switching operation for all the semiconductor devices. To put the icing on the cake, all these benign properties can be obtained almost for free: as we will see, the LLC converter can be obtained by adding an inductor to the traditional series-resonant LC converter and this additional inductor can be realized simply by introducing an air gap in the power transformer.

With this picture in mind, it appears quite weird that it took so long time for the industry to accept and adopt it: its first appearance in the literature dates to 1988, whereas its massive industrial usage started in the mid-2000s. Definitely, there are several reasons for that, and it is not in the scope of the present discussion to look for them. In author's opinion it was probably not that obvious that a significant magnetizing current in the power transformer could bring so many benefits at such low cost, hence the topology was overlooked for a long time.

To conclude this introductory picture, it is worth highlighting that the LLC resonant converter, though considered still today the ultimate resonant conversion solution, still shares some unfavorable characteristics with the other resonant topologies. Complexity is one of them: there are at least six different useful operating modes plus others that are either of no practical use or must be avoided at all. It is a strongly nonlinear system, and its dynamic properties are particularly challenging to be accurately described. After a “paper-design” a substantial simulation campaign needs to be done if one wants to really get the most out of it. However, the promises of the LLC resonant converter were so alluring that power engineers were not discouraged by that and struggled to go along its learning curve to finally dominate its intricacies.

## Chapter 2

### Historical outline

In 1826 the experiments of Félix Savary, a French scientist, showed the ability of an inductor-capacitor circuit to produce electrical oscillations [2]. The mathematical description of this circuit and its oscillation frequency were first determined by Lord Kelvin in 1853. In 1886 James Clerk Maxwell showed that the response of an inductor-capacitor circuit to an alternating current was at its maximum when the frequency of the alternating current and the natural oscillation frequency of the circuit were the same.

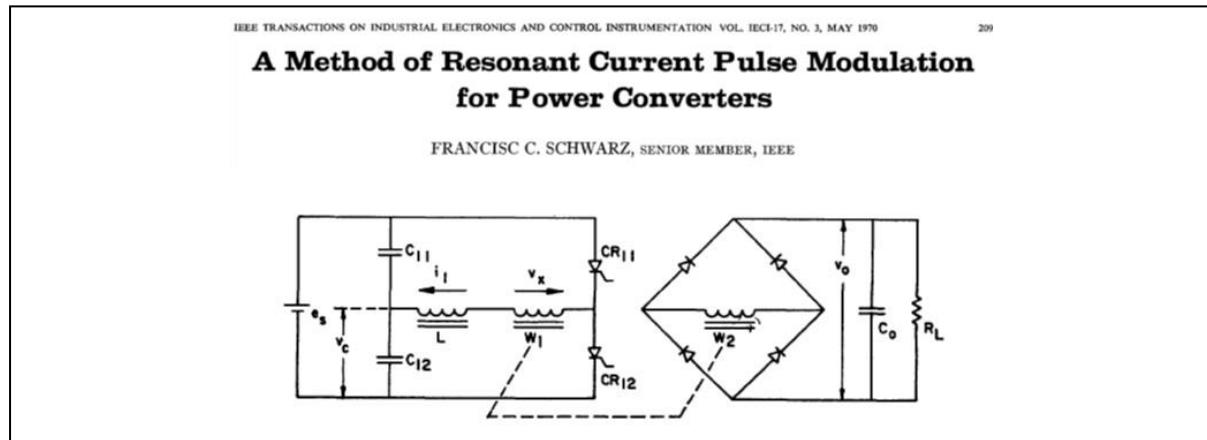
The first practical application of inductor-capacitor circuits can be found in the 1890s in the spark-gap radio transmitters, where they allowed the transmitter and receiver to be tuned to the same frequency. Heinrich Hertz, who associated the term resonance to the characteristics of those circuits, and Guglielmo Marconi are probably to be credited as those who most contributed to make their use in radio communications practical.

To find the first application of resonant circuits (also termed tank circuits or tuned circuits) having to do with power conversion we need to jump to 1959, when Peter Baxandall [3] invented what today is called the class-D dc-ac resonant inverter (or amplifier), a system capable of converting dc power into ac power and that is the basic building block of most of today's resonant converters.

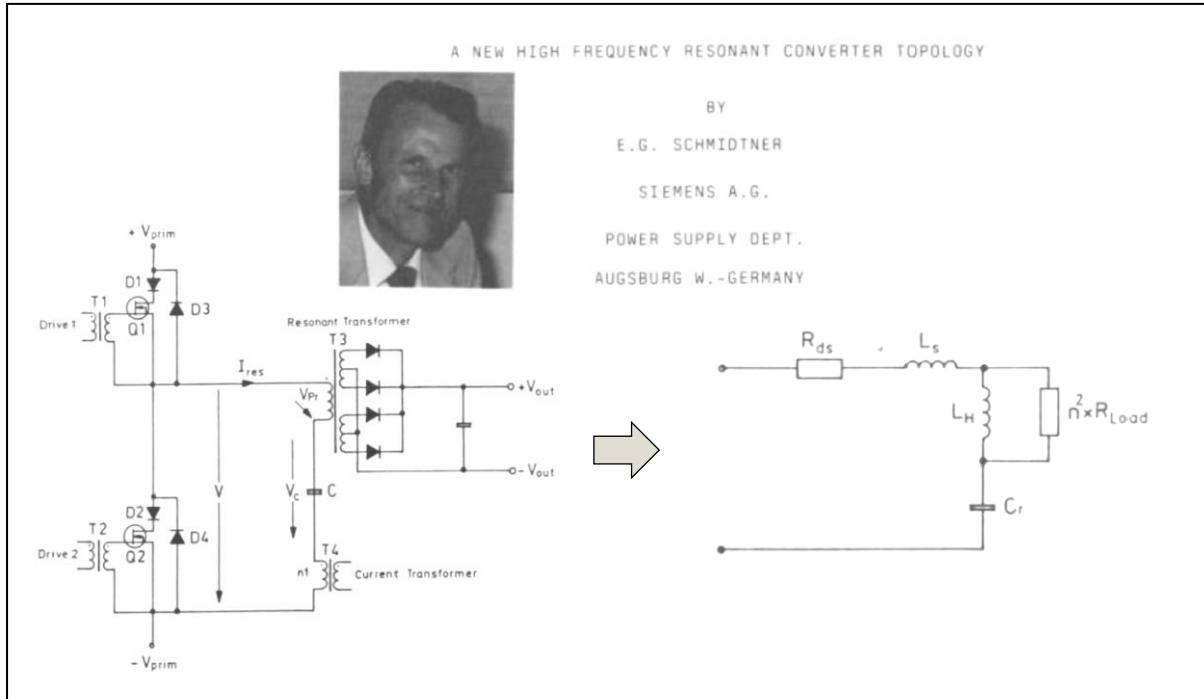
To author's knowledge, the pioneer of resonant dc-dc power converters is Francisc Schwartz, who in 1970 published his work on a "load-insensitive series inverter-converter" [4] (figure 5). With that he built a 95% efficient, 2 kW LC resonant converter operated at 10 kHz with silicon-controlled rectifiers (SCRs) as the power switches, achieving a power density of 0.4 kW/kg. This converter was intended for being used in an ion propulsion engine for spacecraft. In a paper of 1976 [5] he improved his previous work introducing the concept of controlling the power flow by adjustment of the phase angle between the excitation voltage and the resonant current.

The 1980s marked significant advances in the theory. Worth noticing are the work from Vatché Vorperian [6], where he provided a complete analysis of the series and parallel LC resonant converter, those of Ramesh Oruganti and Fred Lee [7]-[8] and that of Robert Steigerwald [9], which laid the foundations of the first-harmonic approximation (FHA) analysis.

**Figure 5. Probably the first resonant converter appeared in the technical literature [4].**



**Figure 6. First appearance of LLC resonant converter in the technical literature [10].**



In addition to the LC series resonant converter, the parallel resonant converter and the series-parallel resonant converter came onto the stage, and in a paper of Erich Schmidtner [10] (figure 6) in 1988 there was the first appearance of the LLC resonant converter, though the name LLC arrived later, initially attributed to a slightly different resonant topology too.

In those years there was no noticeable industrial usage, just niche applications (e.g., high-voltage PSUs in X-ray machines), though the interest in resonant conversion in the community of power engineers was growing dramatically. In the second half of the decade the first resonant control ICs appeared in the market: the LD405 and GP605 from Gennum Corp. and the CS3805 from Cherry Semiconductors were likely the first ones, soon followed by the UC3860 from Unitrode, the MC34066 from Motorola, the CS360 from Cherry Semiconductors and many others [11]. They all were low voltage ICs with ground-referenced drivers, intended to drive different types of resonant and quasi-resonant converters. To use these ICs in half-bridge topologies, gate-drive transformers were necessary to drive the high-side switch of the half-bridge leg. Noticeably, at that time high-voltage bipolar transistors (BJTs) had replaced SCRs as the power switches, and the transition from BJTs to MOSFETs had already started.

The first significant industrial usage started astride the end of 1990s and the beginning of 2000s. Two examples: Runo Nielsen pioneered resonant power supplies in high-end audio equipment (inventing the control method [12] that today with different flavors can be found in some of the most advanced resonant controllers commercially available) and Mike Archer at EOS pioneered resonant ac-dc adapters for notebook PCs. Production volumes were not big, but resonant converters had left their niche and made their debut in the mass market.

There were two significant technology transitions and a technology development occurred in early 90s that ignited the start of massive industrial usage.

The first transition was that of the electronic ballast for fluorescent lamps that was quickly replacing the old-fashioned magnetic ballast. The electronic ballast required inverters based on the half-bridge topology and initially lamp makers had no other solution than using gate-drive transformers and the associated discrete circuitry to drive the half-bridge.

The second transition concerned the power switches: the MOSFET, which appeared in the market in the 1980s, at that time was progressively replacing bipolar transistors in almost all applications, due to its superior switching performance. Higher switching frequencies and power density were possible by transitioning to MOSFETs.

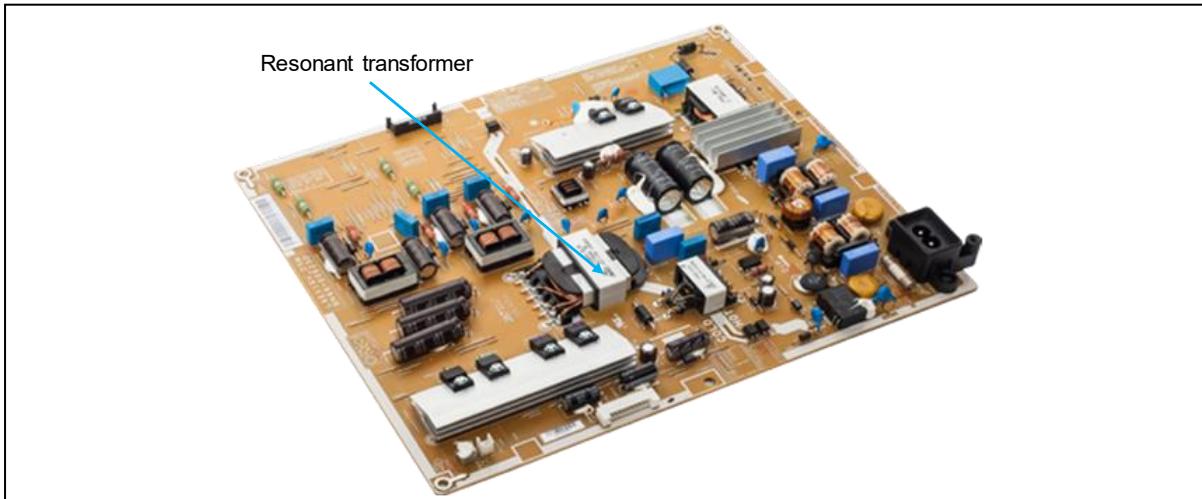
Realizing the big potential of these changes in the lighting market, Philips Semiconductors and STMicroelectronics jointly developed a high-voltage (600 V) Si technology, followed soon by International Rectifier. With that technology it was possible to build a high-voltage driver in a silicon chip able to drive a floating switch directly. This kit part was at the heart of the numerous high-voltage half-bridge drivers that were launched in those years and that tremendously simplified the driving circuitry of the inverter.

Soon the control functions for the lamp were integrated along with the half-bridge driver, to simplify the entire BOM of the inverter. These high-voltage control ICs, which were launched in the market in the second half of 1990s, paved the way to the high-voltage resonant controllers that were released at the end of 1990s (ca 1998) and boomed in the next decade. The L6598 from STMicroelectronics, the TEA1610 from Philips (now NXP) and Motorola's MC33068 were probably the first high-voltage resonant controllers to be launched.

At the beginning of 2000s there were some interesting studies that highlighted the benefits of the LLC converter over the other resonant topologies [13]-[15] and maybe this growing awareness of its value triggered the real explosion of industrial usage that started amid the first and the second half of 2000s. The killer application was the flat screen TV (LCD and Plasma at that time), where the major makers intended migrate the power supply from the external small trunk used at that time to inside the chassis (thanks also to a progressive reduction of the power demanded by the TV set). A very flat design was needed, like that shown in figure 7: the LLC converter appeared as the perfect answer and soon became dominant. Its usage was progressively extended to many other applications supported also by the proliferation of energy saving initiatives (e.g., 80+ program, EU Code of Conduct, DOE, etc.) and by market requirements getting more and more demanding.

The growing industrial usage of the LLC converter, in turn, brought a proliferation of research by both industry and academia; as of today (June 2022), while another technology transition is progressively replacing the Si-based MOSFET with the GaN HEMT (High-Electron-Mobility-Transistor), searching for “LLC converter” on IEEE Xplore provides more than 2400 results.

**Figure 7. Flat screen TV SMPS using an LLC resonant converter.**



# Chapter 3

## Definition and classification of resonant converters

Resonant converters are switch-mode converters that include a tank circuit that actively participates in determining the input-to-output power flow. They should not be confused with quasi-resonant converters, where there is a tank circuit too, but its role is to just create the conditions for soft switching (ZVS or ZCS), with no involvement in the power transfer process.

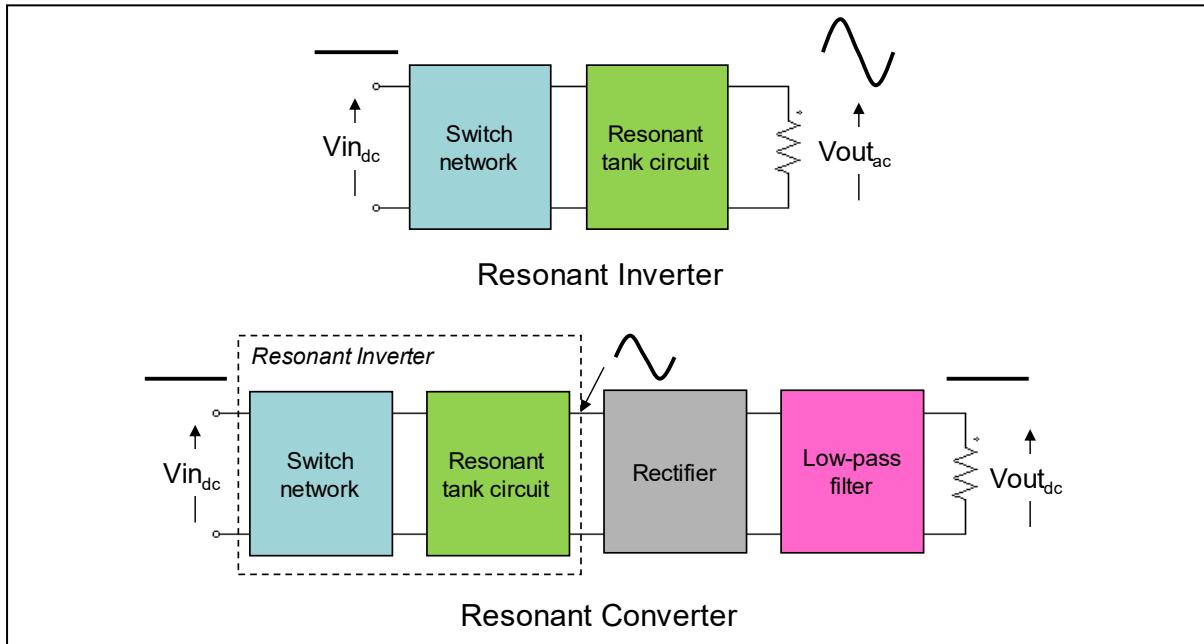
In other words, in resonant converters the selective properties of a tank circuit (i.e., the fact that it responds primarily to stimuli having a frequency close to its resonant frequency and negligibly to other frequencies) are used to control the amplitude of currents/voltages in the converter and, ultimately, how much power transits from the input source to the output load.

As a result, resonant converters are characterized by currents or voltages that are essentially sinusoidal or piecewise sinusoidal. The low higher harmonics content of its waveforms, along with the ability of achieving soft switching for all the switching devices, explains why they are truly EMI-friendly and excellent candidates for high power density designs.

That of resonant converters is an extremely broad family and providing a comprehensive picture is not an easy task. To help get one's bearings, it is possible to consider a property shared by most of, if not all, the members of the family: they are based on a “resonant inverter”, i.e., a system that converts a dc voltage into an ac voltage with low harmonic content and provides ac power to a load, with the addition of a rectifier and a low pass filter. This is illustrated in figure 8.

Different types of inverters can be built, depending on the switch network and the characteristics of the tank circuit, i.e., the number of reactive elements it includes and their configuration [16]. Some assumptions will be done to restrict the analysis within the limits of the practical usage.

**Figure 8. General block diagram of a resonant inverter, and a resonant converter.**



A fundamental one is that the switch network is connected to a voltage source and the load seen by the tank circuit can be either a voltage sink or a current sink. Additionally, the switch network drives the tank circuit symmetrically in voltage and time, to produce an ac square wave voltage. Power flow will be controlled by frequency modulation, that is, by changing the frequency of the square wave closer to or further from the tank circuit's resonant frequency.

It is worth noticing that in some cases the switch network must be coupled to the tank circuit through a dc blocking capacitor to maintain the volt-second balance across the inductive components of the tank and prevent their saturation. In other cases, one capacitor of the tank circuit may double its function as dc blocking capacitor.

These assumptions restrict the switch networks to essentially the half-bridge and the full bridge. In power amplifier terminology, switching inverters using this kind of switch network are termed class-D resonant inverters.

The order and the configuration of the tank circuit defines inverter's/converter's static and dynamic properties. The order of the tank circuit is the number of reactive elements it includes. It is worth mentioning that during a switching cycle the order of the tank circuit may change under some specific operating conditions. This is commonly referred to as multi-resonance and, ultimately, results in a so-called multi-resonant inverter/converter. In case this does not happen, the converter is defined as a single resonant inverter/converter.

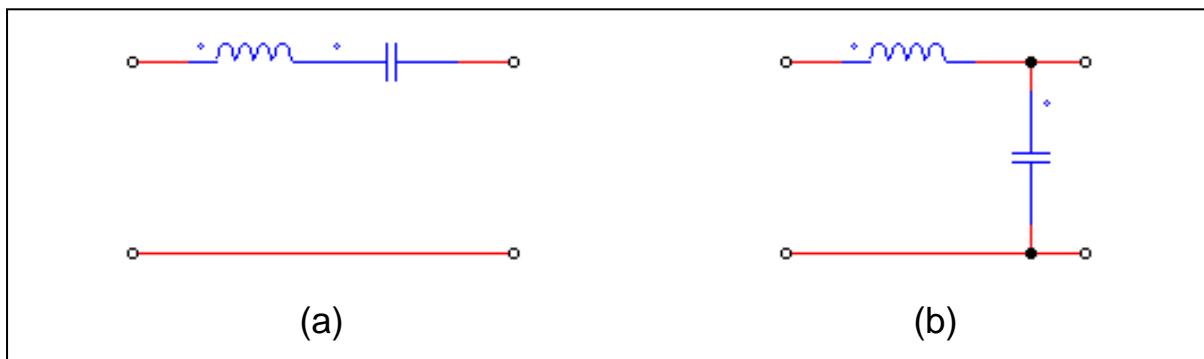
It is intuitive that the higher the order of the tank circuit is, the larger the number of possible configurations will be. However, not all these possible configurations are usable, and those that are practically used are even fewer.

With two reactive elements (2nd order tank circuits) there are eight theoretically possible configurations but only four of them are workable with a voltage source input. Two of them, shown in figure 9, are commonly used: the LC series resonant tank (a) and the LC parallel resonant tank (b).

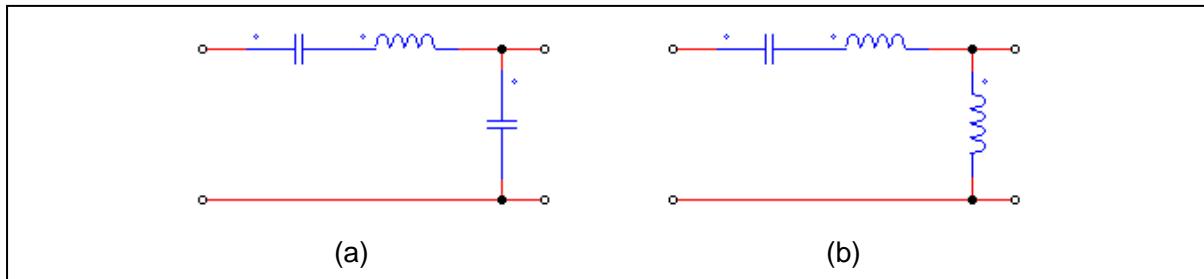
With three reactive elements (3rd order tank circuits) the number of different configurations is thirty-six, but only fifteen can be used in practice with a voltage source input. Figure 10 shows the two most used tank circuits: the so-called *LCC* because it uses one inductor and two capacitors with the output port in parallel to one C (a), and its dual configuration, the *LLC*, using two inductors and one capacitor, with the output port in parallel to one L.

To be noticed: the LCC tank circuit of figure 10a is the core of the inverter commonly used in electronic lamp ballast for gas-discharge lamps.

**Figure 9. LC Series (a) and LC parallel (b) 2-element tank circuits.**



**Figure 10. LCC (a) and LLC (b) 3-element tank circuits.**



With four reactive elements (4th order tank circuits) there are 182 possible configurations but those theoretically usable are less than sixty. The examples of usage of fourth order tank circuits are quite rare and limited to very few of the usable configurations. Their practical meaning is, above all else, that 3rd order tanks may become 4th order when parasitic elements (junction capacitance, intrawinding capacitance, etc.) are considered. Therefore, the effect of parasitic elements on the behavior of 3rd order systems may be understood through the analysis of the 4th order system they generate.

As previously stated, for any resonant inverter there is one associated dc-dc resonant converter, obtained by rectification and filtering of the inverter output. Predictably, the above-mentioned inverters based on half or full bridge switch networks will originate the class-D resonant converters.

Considering offline applications, the rectifier block will be coupled to the resonant inverter through a transformer to guarantee the isolation required by safety regulations. The rectifier block can be configured as either a full-wave rectifier, which needs a center tap arrangement of transformer's secondary winding, or a bridge rectifier, in which case tapping is not needed. The first option is preferable with a low voltage / high current output; the second option with a high voltage / low current output. In the latter case the rectifier block may be configured as a voltage doubler as well.

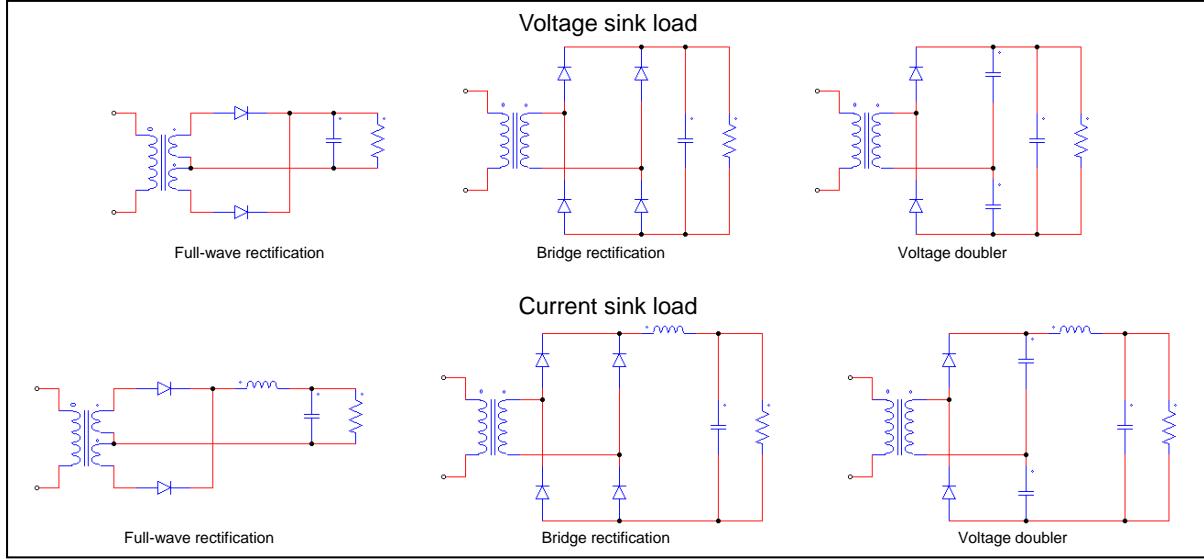
As to the low-pass filter, depending on the configuration of the tank circuit, it will be made by capacitors only (voltage sink load) or by an L-C type smoothing filter (current sink load). All these combinations of rectifier plus low-pass filter are illustrated in figure 11.

Diodes are shown as rectifiers for the sake of simplicity but in real applications they are often replaced by other MOSFETs controlled to emulate the behavior of diodes (synchronous rectification). In this way conduction losses associated to rectification can be significantly reduced and efficiency increased.

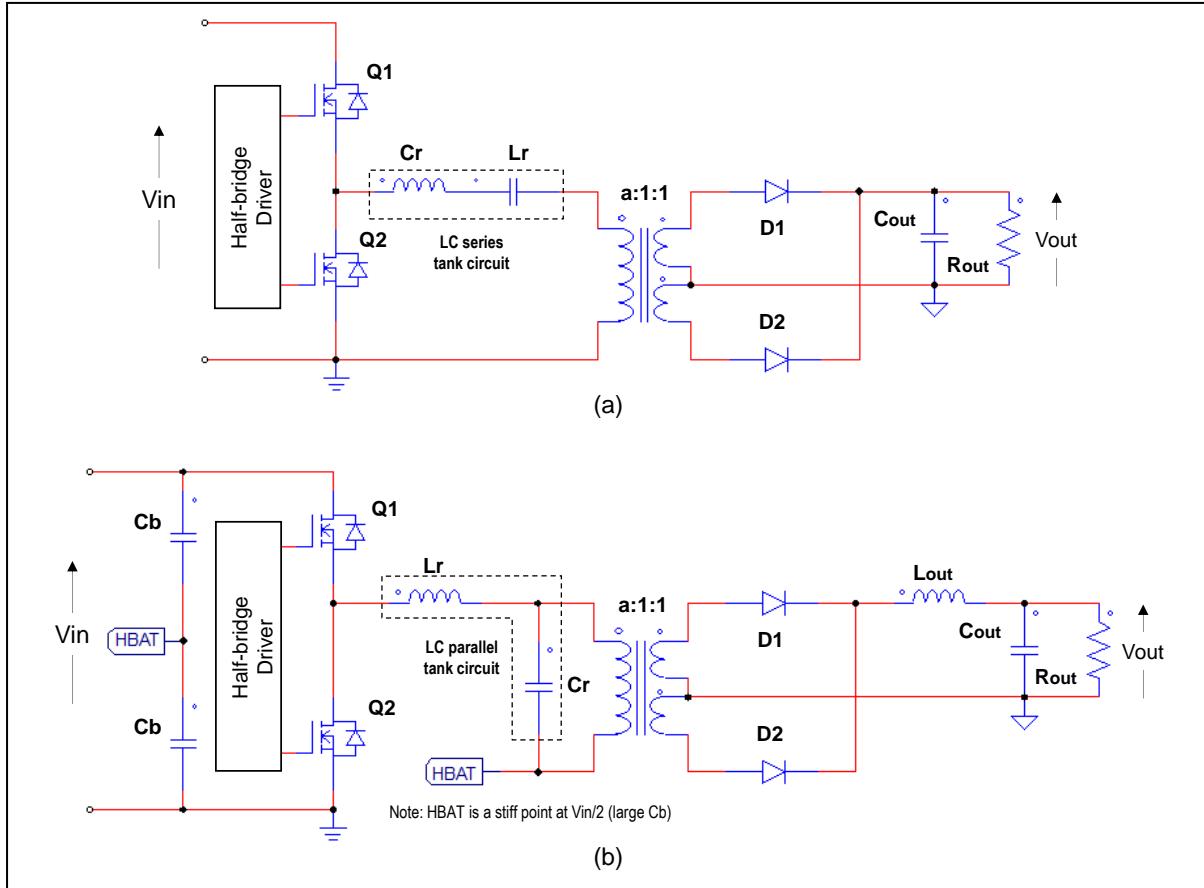
Synchronous rectification (SR), which will be discussed more in details in Part VI, Chapter 1 brings in several issues but also opens the door to more opportunities because with an appropriate timing of the SR MOSFET it is possible to use phase-shift control to enhance some feature of the converter or even provide bi-directional power flow capability.

The LC series and parallel resonant tanks of figure 9 are at the heart of the homonym 2<sup>nd</sup> order resonant converters, which are illustrated in figure 12 in their half-bridge version and thoroughly treated in the literature [7]-[10]. Notice that in the LC series resonant converter the resonant capacitor  $C_r$  acts also as dc blocking capacitor, whereas in the LC parallel resonant converter the two input capacitors  $C_b$  are large so that they create a stiff point (HBAT) whose voltage equals  $V_{in}/2$ . In the end, they block the dc component of the square wave generated by the half-bridge and the voltage across  $C_r$  is pure ac.

**Figure 11. Transformer-coupled rectifier plus low-pass filter combinations.**



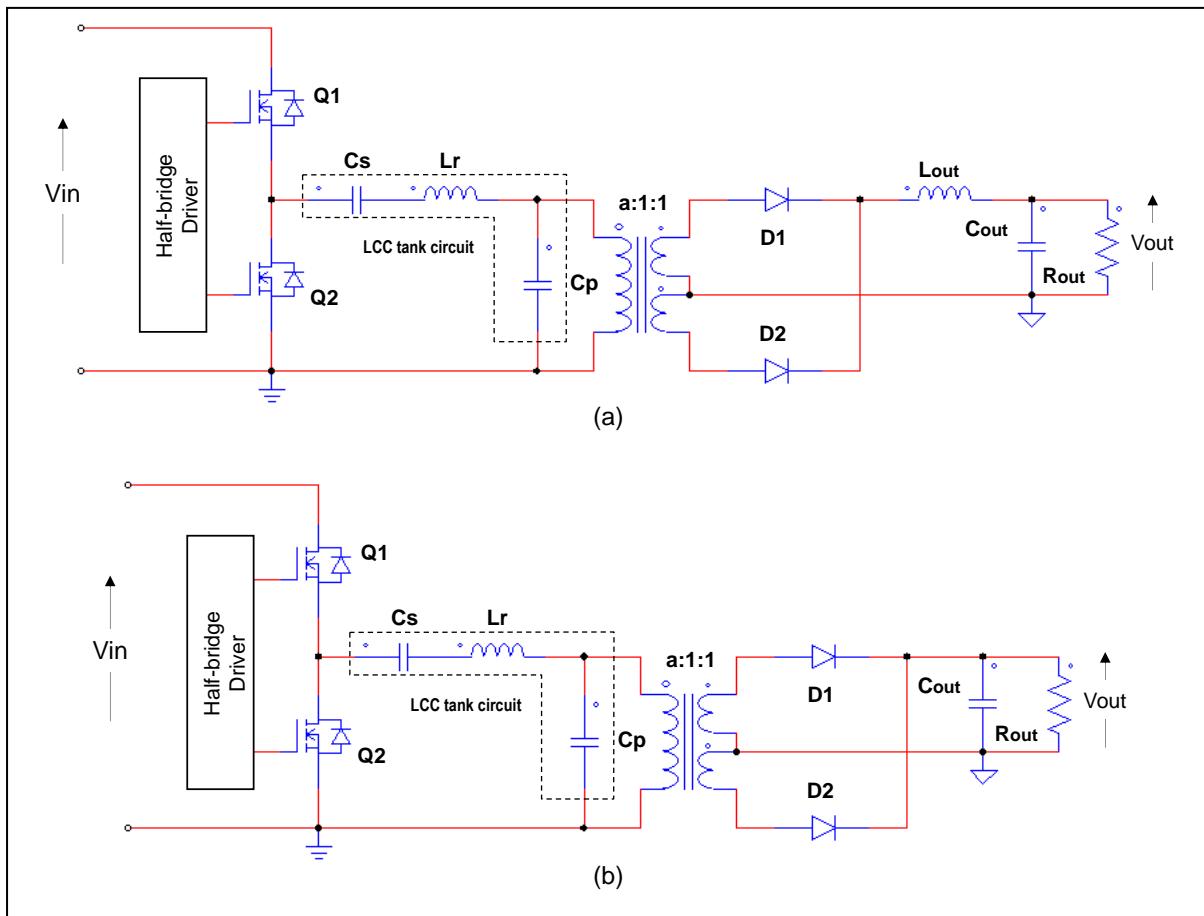
**Figure 12. 2<sup>nd</sup> order resonant converters: (a) LC series; (b) LC parallel.**



The LCC tank circuit of figure 10 is the core of the homonym resonant converter when coupled to a voltage sink load [12] and of the series-parallel resonant converter [9] when it is coupled to a current sink load. They are both illustrated in figure 13. Notice that in both the series capacitor  $C_s$  acts also as dc blocking capacitor.

The LLC tank circuit is the core of the homonym converter that will be the subject of the following discussion.

**Figure 13. 3<sup>rd</sup> order resonant converters: (a) series-parallel converter; (b) LCC converter.**



## PART II

### LLC CONVERTER GENERAL OVERVIEW

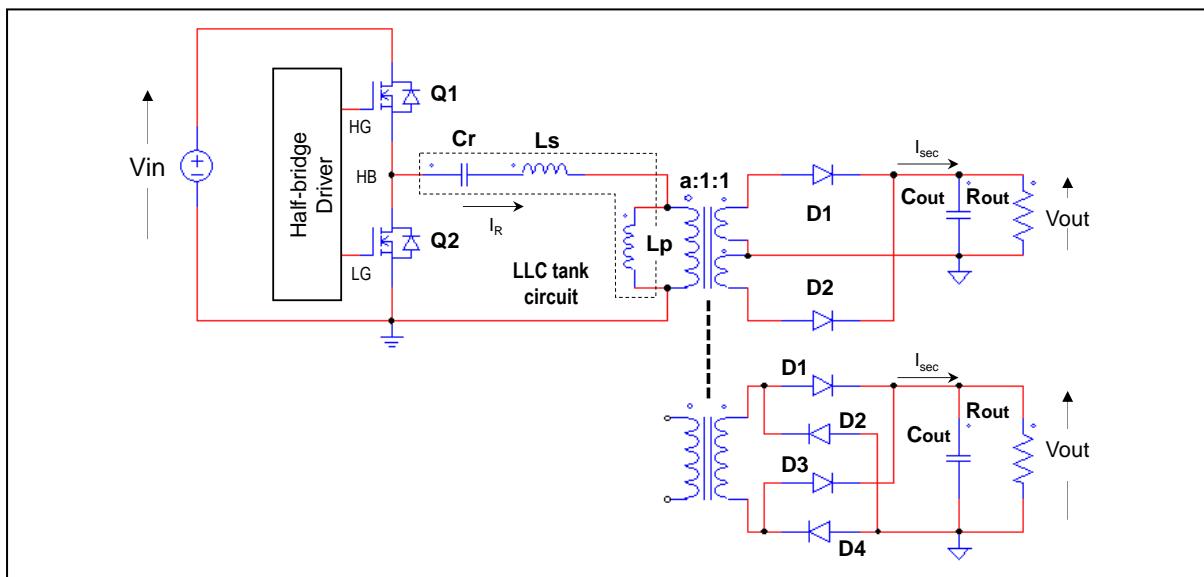
#### Chapter 1

#### Introduction

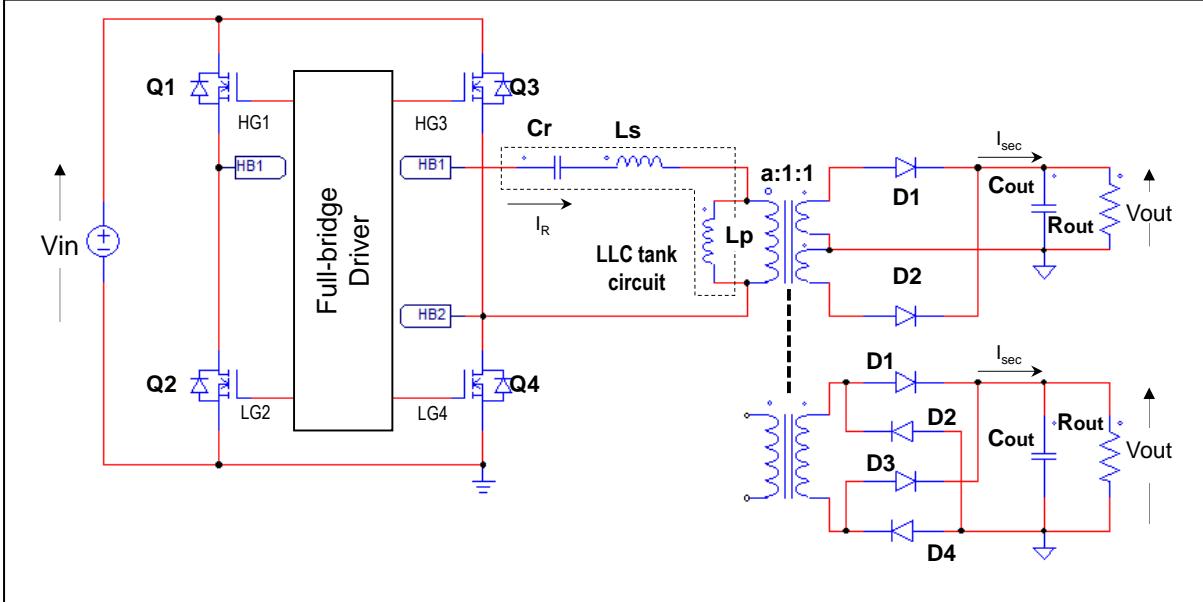
Figure 14 shows an LLC resonant converter in its half-bridge implementation, with the dual option of output rectification: center-tap full-wave (upper scheme) for low voltage, high current output, and single-ended bridge rectification (lower scheme) for a higher voltage output. Figure 15 shows an LLC resonant converter in its full-bridge implementation, suitable for larger power levels, again with the dual option of output rectification.

The two power MOSFETs Q1 and Q2 are driven on and off to generate a 50% duty cycle square wave  $V_{HB}$ . A small dead-time  $T_D$  is inserted between the turn-off of either switch and the turn-on of the other one. This dead-time not only ensures that Q1 and Q2 do not cross-conduct: for reasons that will be explained afterward, in normal operation the edges of  $V_{HB}$  occur when Q1 or Q2 are switched off and it takes some time for  $V_{HB}$  to swing rail-to-rail. Therefore, this dead-time allows the transitions of  $V_{HB}$  to be completed before turning on the other switch, so that Q1 and Q2 are turned on with zero drain-source voltage (ZVS). During part of the time interval when both Q1 and Q2 are off, the continuity of the circuit is ensured by the body diodes of Q1 (after Q2 turns off) and Q2 (after Q1 turns off), which have therefore a crucial role in the operation of the converter. In case one uses switches without an intrinsic anti-parallel diode like MOSFETs (e.g., BJTs or IGBTs), the diodes must be added externally.

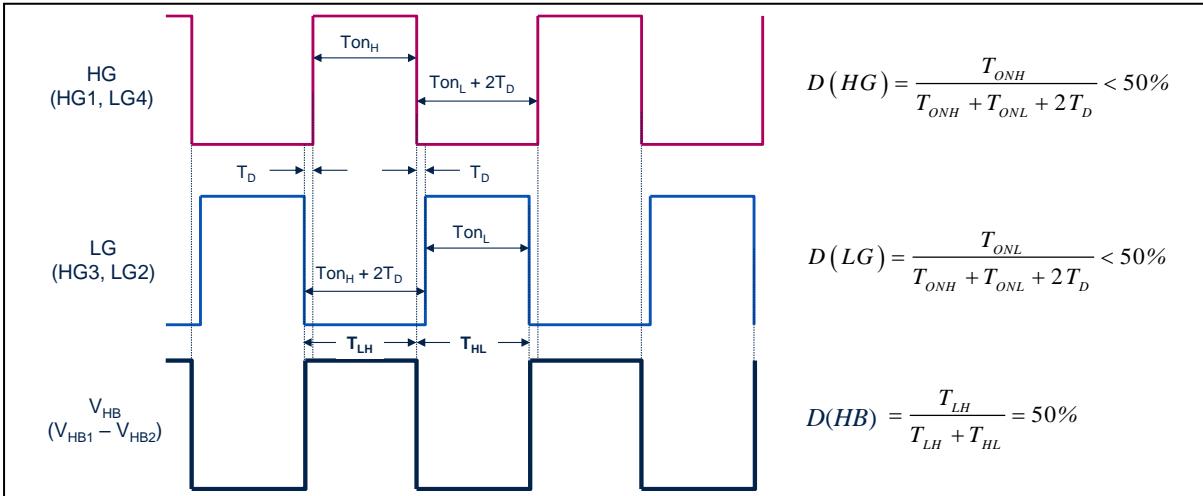
**Figure 14. LLC half-bridge resonant converter with its two basic options of secondary rectification.**



**Figure 15. LLC full-bridge resonant converter with its two basic options of secondary rectification.**



**Figure 16. Switch network operation (in parentheses that relevant to the full bridge).**



In the present discussion we will be essentially concerned with offline converters, hence with input voltages in the hundred volts, so that the voltage drop across the body diode ( $\approx 1$  V) can be neglected and assumed to be zero.

As illustrated in the diagrams of figure 16, to generate a 50% duty cycle square wave the driver must ensure equal distance in time between the falling edges of the driving signals. Note that the duty cycle of each driving signal will be lower than 50% because of the dead-time  $T_D$ .

Considering the half-bridge version, this square wave swings all the way from zero to  $V_{in}$ , top- and bottom-clamped by the body diodes of Q1 and Q2, thus it has an average value (i.e., a dc component) of  $V_{in}/2$  and an amplitude of  $\pm V_{in}/2$ . In the LLC tank circuit, the resonant capacitor  $C_r$  is in series to the half-bridge switch network and under steady-state conditions the average voltage across inductors must be zero, so the dc component  $V_{in}/2$  of the input voltage must drop across  $C_r$ . Therefore,  $C_r$  acts as both resonant capacitor and dc blocking capacitor.

It is worth noticing that the input source delivers current to the converter only during the half-cycle when Q1 is on (not exactly equal to the on-time of Q1 but for the moment we can assume they are the same), while during the other half-cycle (when Q2 is on) the tank current recirculates internally, and no energy is taken from the input source. It is then expected that the input current of the LLC resonant half-bridge be discontinuous with essentially 50% conduction duty cycle.

In the LLC full-bridge converter of figure 15, the switches Q1, Q2, Q3 and Q4 always work in diagonal: Q1 and Q4 are turned on and off simultaneously and so do Q2 and Q3. Different modulation schemes where either Q1 and Q3 or Q2 and Q4 are on simultaneously are possible but they are outside the perimeter we have set at the beginning of this discussion. In this case too, a small dead-time  $T_D$  is inserted between the turn-off of one diagonal and the turn-on of the other one. The purpose and the effect of  $T_D$  are the same as in the half-bridge.

This square wave generated by the full-bridge swings all the way from  $-V_{in}$  to  $V_{in}$ , thus it has zero average value and twice the amplitude of the square wave generated in the half-bridge.

The resonant capacitor  $C_r$  will have only ac voltage across its terminals; thus, it does not act in principle as a dc blocking capacitor. In the real-world operation, there are unavoidable asymmetries in the switch network that make the duty cycle of the generated square wave not exactly equal to 50%.  $C_r$  will absorb them by having a small dc voltage component and ensuring that the average voltage developed across the inductors be zero.

In this case the input source delivers current to the tank circuit during the conduction of both the diagonals so that, unlike in the half-bridge, the input current flows continuously in both half-cycles. With the same dc input current in the full bridge the input current amplitude in each half-cycle is half of that in the half-bridge. Therefore, its peak and squared rms values are cut in half as well, and the rms currents through the power switches too. Note that this is consistent with the fact that the amplitude of the square wave voltage is double.

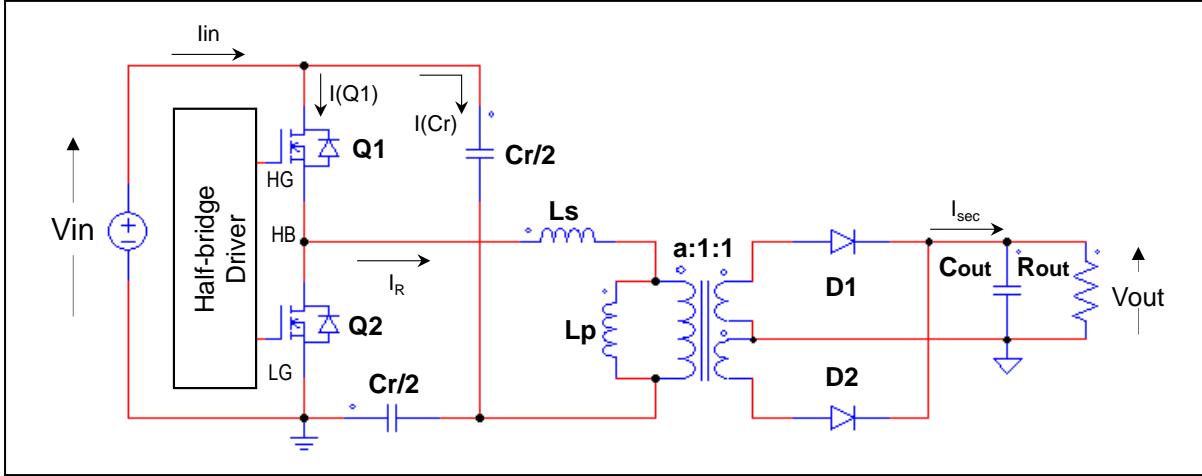
Before going on with a more detailed analysis of the properties of the LLC tank, it is worth mentioning a variant of the half-bridge topology, shown in figure 17 (for simplicity, only the version with center-tap full-wave output rectification).

The resonant capacitor  $C_r$  is split in two  $C_r/2$  parts, one connected to ground and the other to the input voltage bus. It is immediate to recognize that they are dynamically in parallel and act a single capacitor  $C_r$ . Sometimes this comes free of charge, i.e., when one needs to parallel capacitors not to exceed their ac current rating: it's just a matter of a different connection.

Unlike the single capacitor version, where the input current  $I_{in}$  equals the current through the high-side switch Q1,  $I(Q1)$ , all the time, in this case  $I_{in}$  is given by the superposition of  $I(Q1)$  and  $I(C_r)$ , the current in the high-side resonant capacitor. The current  $I(C_r)$  with the direction defined in figure 17 is in phase opposition to  $I(Q1)$  and to the current through the series resonant inductor  $I_R$ ; also, its instantaneous amplitude is half that of  $I_R$  since it is equally split between the two resonant capacitors. As a result, when Q1 is on,  $I(C_r)$  is negative and  $I_{in}$  equals  $I(Q1) - I(C_r)$ ; when Q1 is off and  $I(Q1) = 0$ ,  $I_{in} = I(C_r)$  is positive, so that there is a continuous input current flow like in a full-bridge converter, with the consequent reduction of peak and rms values compared to the single capacitor version.

Note, however, that unlike the bridge converter, here the currents  $I(Q1)$  and  $I(Q2)$  have the same rms value as in the single capacitor version of the half-bridge.

**Figure 17. LLC half-bridge resonant converter with split resonant capacitors.**



It is advantageous to use this configuration to reduce not only the ac current requirements on the resonant capacitors and the ac input current but also the differential-mode conducted noise. This solution is recommended at higher power levels or when the converter is powered directly from the rectified mains voltage. In this case, in fact, the differential-mode noise generated by the resonant converter that the input EMI filter is required to mitigate is lower and thus it is possible to use a lighter and possibly smaller filter.

The LLC resonant converter is a class-D resonant converter belonging to the family of multi-resonant converters because there are two resonance frequencies that may or may not appear in a switching cycle. One appears when the secondary rectifiers are conducting: the inductance  $L_p$  is dynamically shorted out by the low-pass filter and the load (there is a constant voltage,  $a(V_{out} + V_{Rect})$ , across it, with a primary-to-secondary turns ratio and  $V_{Rect}$  average forward drop of secondary rectification, equal to a forward drop  $V_F$  in case of center-tap full-wave rectification or  $2V_F$  in case of single-ended bridge rectification). Essentially,  $L_p$  acts as a reactive load to the remaining LC circuit, so:

$$f_{R1} = \frac{1}{2\pi\sqrt{L_s C_r}}, \quad (1)$$

The second resonance frequency is relevant to the condition of nonconductive secondary rectifiers, so that the secondary winding(s) is/are open, where the tank circuit turns from LLC to LC because  $L_s$  and  $L_p$  are de facto in series and work as a single inductor. Therefore:

$$f_{R2} = \frac{1}{2\pi\sqrt{(L_s+L_p) C_r}}. \quad (2)$$

It will be of course  $f_{R1} > f_{R2}$ . Normally, we will refer to  $f_{R1}$  as the *main* or *upper* or *series* resonance frequency of the LLC tank, while  $f_{R2}$  is sometimes called the *secondary* or *lower* or *parallel* resonance frequency. The separation between  $f_{R1}$  and  $f_{R2}$  depends on the ratio  $L_p / L_s$ :

$$\frac{f_{R1}}{f_{R2}} = \sqrt{1 + \frac{L_p}{L_s}}; \quad (3)$$

the larger this ratio is the further the two frequencies will be and vice versa. As we will see, the value of  $L_p / L_s$  (typically  $> 1$ ), often denoted with  $k$ , is an important design parameter.

When in a switching cycle the secondary current never goes to zero (except for single points in time), so that the tank circuit responds to the square wave generated by the switch network with a resonant current made up only of sinusoids at  $f = f_{R1}$ , the LLC is said to operate in Continuous Conduction Mode (CCM). When in a switching cycle there are finite time

intervals during which neither of the secondary rectifiers is conducting, so that the resonant current includes portions of a sinusoid at  $f = f_{R2}$ , the LLC converter is said to operate in Discontinuous Conduction Mode (DCM).

The tank circuit looks quite bulky, with its three magnetic components  $L_s$ ,  $L_p$  and the transformer. However, one of the good properties of the LLC resonant converter is that  $L_s$  and  $L_p$  can be realized within the transformer, so that there can be just a single physical magnetic device. This is called magnetic integration and will be discussed in a dedicated section (see “Magnetic Integration in the LLC Resonant Converter”, chapter 6).

The symmetric operation of the LLC resonant converters equalizes the stress of secondary rectifiers both in terms of reverse voltage and forward conduction current.

As to the reverse voltage, in case of center-tap full-wave rectification, when one rectifier is reverse-biased, its voltage is, to a first approximation,  $2 \cdot V_{out} + V_F$ . In fact, when one half-winding (e.g., that of D1) is conducting the voltage externally applied to that half-winding is  $V_{out} + V_F$ ; assuming an ideal transformer, this voltage is coupled one-to-one to the non-conducting half-winding, providing a negative voltage to the anode of D2 because of the dot positions. Since the cathode of D2 is connected to the  $V_{out}$  bus, the reverse voltage applied to D2 is  $2 \cdot V_{out} + V_F$ . The transformer, however, is not ideal, and a leakage inductance is associated to the secondary windings to account for their imperfect coupling. This leakage inductance,  $L_{Lsec}$ , causes a voltage drop  $V_{Lsec} = L_{Lsec} \cdot di(D1) / dt$  that adds up to  $V_{out} + V_F$  and is reflected to the other half-winding as well. As a result, the reverse voltage applied to the non-conducting rectifier will be  $2V_{out} + V_F + V_{Lsec}$ .

In case of single-ended secondary with bridge rectification, the voltage applied to reverse-biased diodes of the bridge is only  $V_{out} + V_F$  and is not affected by the leakage inductance  $L_{Lsec}$ . The reason is that the negative voltage of the secondary winding is fixed at  $-V_F$  externally and is not determined by internal coupling like in the case of the tapped secondary.

If we compare the LLC converter to similar PWM converters (such as the ZVS Asymmetrical Half-bridge, or the Forward converter), the equal reverse voltage typically allows the use of common cathode diodes housed in a single package with lower blocking voltage. A lower blocking voltage means also a lower forward drop for the same current rating, and then lower losses. A similar benefit can be found also when using synchronous rectification: a lower voltage rating means a lower  $R_{DS(on)}$  for a given die size.

The forward conduction current  $I_{sec}(t)$  is proportional (a times) to the difference between the primary resonant current  $I_R(t)$  flowing through  $C_r$  and  $L_s$  and the current  $I_M(t)$  flowing through the parallel inductor  $L_p$ :  $I_{sec}(t) = a [I_R(t) - I_M(t)]$ . Therefore, current flows on the secondary side if  $|I_R(t)| > |I_M(t)|$ .

In case of perfect symmetry of the power circuit and of the operation of the switch network each rectifier (in case of center-tap full-wave rectification) or each leg of the bridge (in case of bridge rectification) carries half the total forward conduction current under all operating conditions. In the real-world operation the two secondary half currents may be slightly different, but if this does not bring significant thermal differences or increase in the output voltage ripple it is not an issue. One of the major sources of asymmetry in the secondary currents in case of center tap is the asymmetry of the two half-windings; the single winding arrangement with bridge rectification is less prone to cause differences in the forward currents of the two legs of the output bridge.

It must be noted that in the LLC resonant converter the output current form factor is worse as compared to the previously mentioned PWM topologies that have an L-C output low-pass

filter. This implies that the output capacitor bank is more stressed, which is one of the few real drawbacks of the topology, although the stress level is considerably lower than that in a flyback converter. Table 1 shows the typical shape of the secondary current in the LLC resonant converter and other popular PWM converters, along with a numerical comparison.

To complete the general picture on the LLC resonant converter, it is worth briefly mentioning the parasitic components that most affect its behavior.

A first parasitic component to consider is the capacitance of the midpoint of the half-bridge structures, the node HB in the schematic of figure 14, the nodes HB1 and HB2 in the schematic of figure 15. Its net effect is that the transitions of the half-bridge midpoint(s) will require some energy and take a finite time to complete. This relates to the previously mentioned dead-time  $T_D$  and will be discussed more in detail in the next chapter.

Another parasitic element to consider is the distributed capacitance of transformer's windings. This capacitance exists for both the primary and the secondary windings and, in combination with windings' inductance, originates the so-called self-resonance of the transformer.

Another parasitic capacitance that needs to be taken into consideration is the junction capacitance of the secondary rectifiers, which adds up to that of the transformer windings. Their combined effect can be modeled with a single capacitor parasitic in parallel to  $L_p$ , thus turning the 3<sup>rd</sup>-order LLC tank into a 4<sup>th</sup>-order LLCC tank circuit. The effects of this change will be discussed in detail in Part IV, chapter 5

**Table 1. Output stress for LLC resonant converter vs PWM topologies @ 50% duty cycle.**

<i>Output current form factors</i>	<i>LLC resonant</i>	<i>Forward, ZVS Asymm. HB</i>	<i>Flyback (CCM-DCM boundary)</i>
Peak-to-dc ratio	$\approx \pi/2 = 1.57$	< 1.2 typ.	4
Rms-to-dc ratio	$\approx \pi/2\sqrt{2} = 1.11$	$\approx 1$	$\sqrt{8/3} \approx 1.63$
Ac-to-dc ratio	$\approx \sqrt{\pi^2/8 - 1} = 0.48$	< 0.1	$\sqrt{8/3 - 1} \approx 1.29$

# Chapter 2

## The switching mechanism

A major benefit of resonant converters in general and, in particular, of the LLC converter is their ability to achieve soft switching. This ability stems from the combined action of the switch network and the properties of the tank circuit. Before diving into the details of this matter, it is worth going for a moment back to the basics and recall the concepts of hard switching, soft switching, and their characteristics.

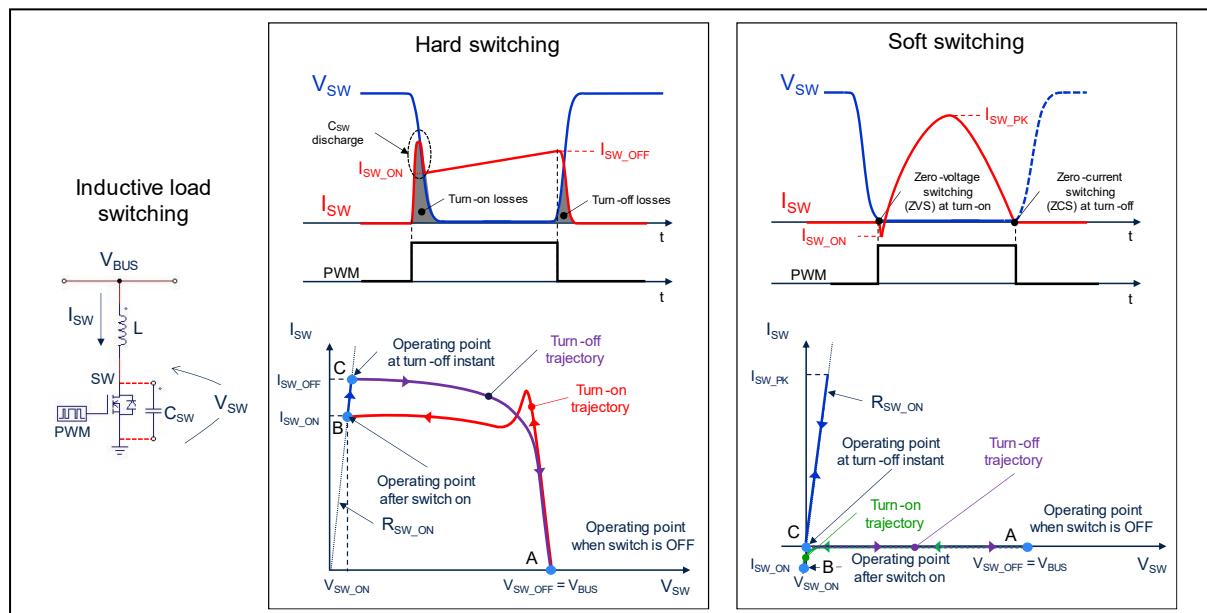
### *Soft switching: ZVS and ZCS*

With reference to the diagrams in figure 18, with hard switching the operating point of the power switches goes from A to B when it is turned on by the PWM signal going high, from B to C during the on-time, and from C to A when it is turned off by the PWM signal going low. During the transitions A to B and C to A, the instantaneous operating point crosses the active region where  $V_{SW}$  and  $I_{SW}$  are simultaneously high, resulting in a peak of power dissipation.

This peak is repeated at the switching frequency, thus the higher the frequency is, the larger the average power dissipation will be. At a given switching frequency, the average dissipation can be reduced by crossing the active region more rapidly (i.e., by switching faster), which will reduce the voltage-current overlap (the gray-shaded area). The initial peak in the turn-on trajectory is due to the parasitic capacitance  $C_{SW}$  associated to the swinging node of the power switch (lumping together many contributors such as the capacitance of the switch itself and that of all the components connected directly or indirectly to that node) that just before the turn-on instant of the switch is charged at a certain voltage ( $V_{BUS}$  in the example of figure 18).

So, every time the switch is turned on, the energy inside this parasitic capacitance (proportional to the squared voltage at the turn-on instant) is discharged inside the switch, causing an additional current spike and, consequently, additional power losses.

**Figure 18. Inductive load switching: hard vs soft switching.**



With soft switching the turn-on command to the switch (i.e., the PWM signal going high) is given when the voltage  $V_{SW}$  across its terminals is zero or almost zero (zero-voltage switching, ZVS). Of course, we need to assume that VSW drops because of the action of the external circuit because the switch cannot do this by itself. Therefore, the operating point moves from A to B along the horizontal axis and B can be theoretically located at the origin of the axes ( $V_{SW} = 0$ ,  $I_{SW} = 0$ ); in the real-world operation B will be at a negative voltage very close to zero (in a MOSFET, the drop across the body diode) with a slightly negative current, so that the switch works in the 3rd quadrant for a short while. During the on-time the operating point moves up from B along the line whose slope represents the on-resistance of the switch, reaches the peak, and then goes down to C, which is essentially located at the origin of the axes. At this point the PWM signal goes low; since no current is flowing in the switch, we have zero-current switching (ZCS), and the operating point may go back to A moving along the horizontal axis, again under the action of the external circuit.

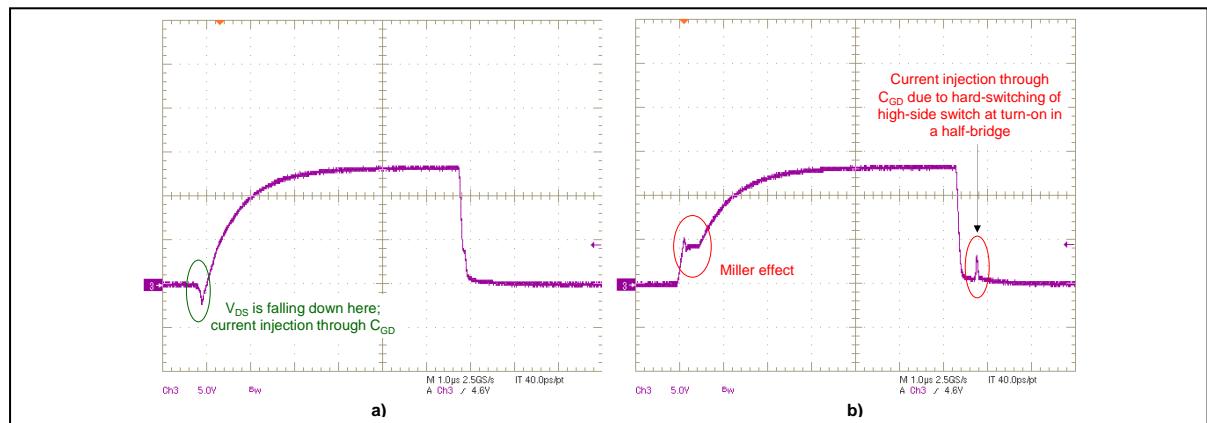
In this way, every time the switch is turned on or off the voltage-current overlap is extremely low and this results in negligible power dissipated during the transitions. It is important to point out once more that this behavior cannot be achieved without the aid of the external circuit that creates the conditions for ZVS and/or ZCS to occur.

ZVS is the preferred switching technique when there are high voltages involved, especially for MOSFETs, because it eliminates capacitive losses and is enabled by body diode. ZCS is the preferred switching technique for diodes, BJTs and IGBTs because it eliminates reverse recovery and storage related losses. As usual, nothing comes for free: ZVS and ZCS eliminate switching losses but usually increase conduction losses due to higher RMS circulating currents and, in some cases, require switches with a higher blocking voltage rating. Further, the same switch can normally achieve either ZVS or ZCS, not both.

ZVS has an additional positive side-effect: the absence of the Miller effect, normally present in MOSFETs at turn-on when hard switched. In fact, being the drain-source voltage already zero when the gate is driven high, the drain-gate capacitance  $C_{GD}$  is essentially in parallel to the gate-source capacitance  $C_{GS}$  and cannot “steal” the charge provided to the gate. The so-called “Miller plateau”, the flat portion in the gate voltage waveform, as well as the associated gate charge, is here missing and less driving energy is therefore required.

Note that this property provides a method to check if the converter is running with ZVS or not by looking at the gate waveform of Q2 (which is more convenient to probe because it is source-grounded), as shown in figure 19.

**Figure 19. Low-side MOSFET gate voltage at turn-on: a) with ZVS; b) without ZVS (hard switching).**



### Analysis of switching mechanism - preliminary considerations.

Let us now examine this behavior in the context of class-D resonant converters in general and the LLC resonant converter specifically. We will consider the half-bridge implementation first and then extend the analysis to the full bridge.

Class-D resonant converters may be included in the family of *resonant-transition converters*, i.e., those converters where power switches are driven in such a way that a resonant tank circuit is stimulated to create ZVS at turn-on.

To understand how this can be achieved, let us consider the circuits a) and b) illustrated in figure 20 where the switches Q1 and Q2 that generate the square wave input voltage to the resonant tank are power MOSFETs. Their body diodes DQ1, DQ2 are pointed out because, as mentioned earlier, they play an important role since they determine the low ( $\approx 0$ ) and high ( $V_{in}$ ) levels of the generated square wave voltage  $V_{HB}$ . In circuit a), the drain-to-source parasitic capacitances  $C_{oss1}$ ,  $C_{oss2}$  are pointed out as well: in fact, as regards the voltage changes of the node HB, the parasitic capacitances  $C_{GD}$  and  $C_{DS}$  are effectively in parallel, then  $C_{GD} + C_{DS} = C_{oss}$  must be considered.

There are other contributors to the capacitance of the node HB: parasitic contributors (e.g., the capacitance formed between the case of the MOSFETs and the heat sink, the intrawinding capacitance of the resonant inductor, etc.) and, in case, an intentional contributor: an external capacitor connected between the node HB and ground to slow down the slope of the edges of  $V_{HB}$  for EMI reasons. They are all lumped together in the capacitor  $C_{Stray}$ .

Note that both  $C_{oss1}$  and  $C_{oss2}$  are connected between the node HB and a node having a fixed voltage ( $V_{in}$  for  $C_{oss1}$ , ground for  $C_{oss2}$ ). Then,  $C_{oss1}$  is effectively connected in parallel to  $C_{oss2}$  and  $C_{Stray}$ , and it is convenient to lump all of them together in a single capacitor  $C_{HB}$  from the node HB to ground, as shown in the circuit b) of figure 20:

$$C_{HB} = C_{oss1} + C_{oss2} + C_{Stray}, \quad (4)$$

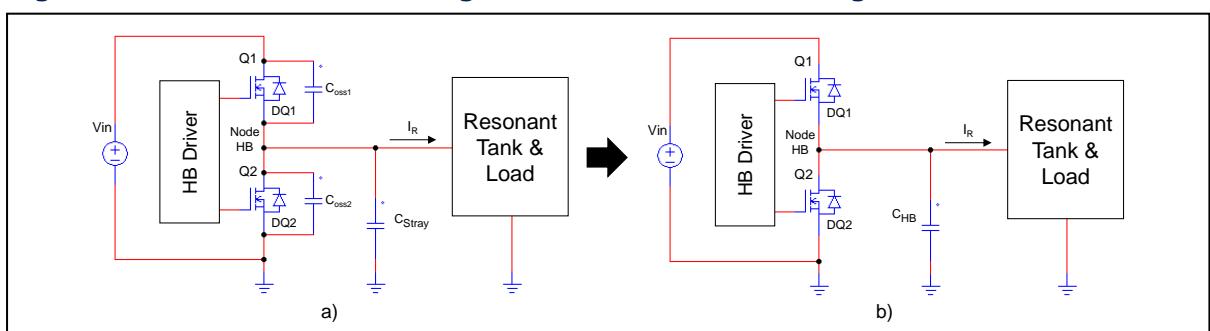
which we will refer to in the following discussion.

Unlike  $C_{Stray}$ , which is essentially a linear capacitance (i.e., its value little or not at all depends on the drain-source voltage  $V_{DS}$ ),  $C_{oss1}$  and  $C_{oss2}$  are nonlinear capacitors: their value is a function of  $V_{DS}$  that is smaller for high  $V_{DS}$  values and significantly increases at low  $V_{DS}$  values.

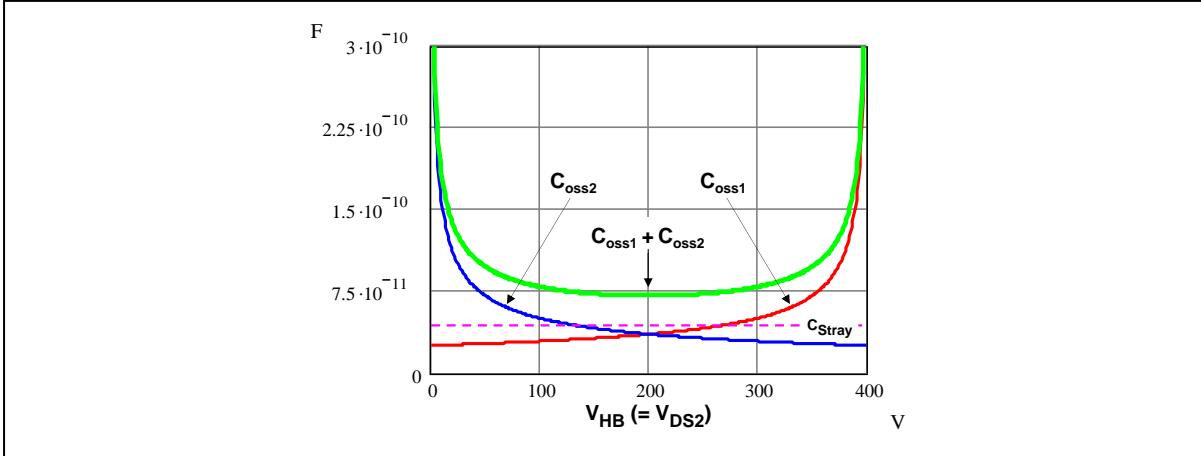
Figure 21 shows how  $C_{oss1}$ ,  $C_{oss2}$  and  $C_{Stray}$  vary with  $V_{DS}$  under the simplifying assumptions that both  $C_{oss}$ 's are the same and change with  $V_{DS}$  following the law of a step-graded junction capacitance:

$$C_{ossx} = \frac{C_{oss0}}{\sqrt{1 + \frac{V_{DS}}{V_B}}}, \quad (5)$$

**Figure 20. Switch network driving a tank circuit in a half-bridge converter.**



**Figure 21. Node HB capacitances vs. node HB voltage  $V_{HB}$  (qualitative plot).**



where  $C_{oss0}$  is the junction capacitance at  $V_{DS} = 0$  and  $V_B$  is the barrier potential (we can typically assume  $V_B \approx 0.6$  V for silicon at room temperature). It is worth reminding that when  $V_{HB}$  is swept from 0 to  $V_{in}$ , the  $V_{DS}$  of Q2 equals  $V_{HB}$ , while that of Q1 changes in the opposite direction ( $V_{DS}(Q1) = V_{in} - V_{DS}(Q2)$ ).

Considering this nonlinearity is a tremendous complication, though a necessary step for an accurate analysis of the resonant transitions of the node HB. This is particularly true for the latest generations of Superjunction MOSFETs, where the change in  $C_{oss}$  when  $V_{DS}$  is swept from zero to their rated voltage has a complex strong nonlinearity and can exceed two orders of magnitude. Additionally,  $C_{oss}$  is affected by hysteresis phenomena too [16].

In this context, to simplify the analysis we will consider an equivalent linear capacitance  $C_{ex}$  in place of the real  $C_{oss}$ , as taught in [18]. There is not a single capacitance value able to model all the characteristics of interest simultaneously, we need to choose the appropriate capacitance when addressing a certain aspect of the transition: the time-equivalent linear capacitance  $C_{eT}$  for the transition times, the Z-equivalent capacitance  $C_{eZ}$  for determining the current at the end of the transition, the energy-equivalent capacitance  $C_{eE}$  for the energy stored in the capacitor, and the charge-equivalent capacitance  $C_{eQ}$  for its charge.

#### *Analysis of the switching mechanism.*

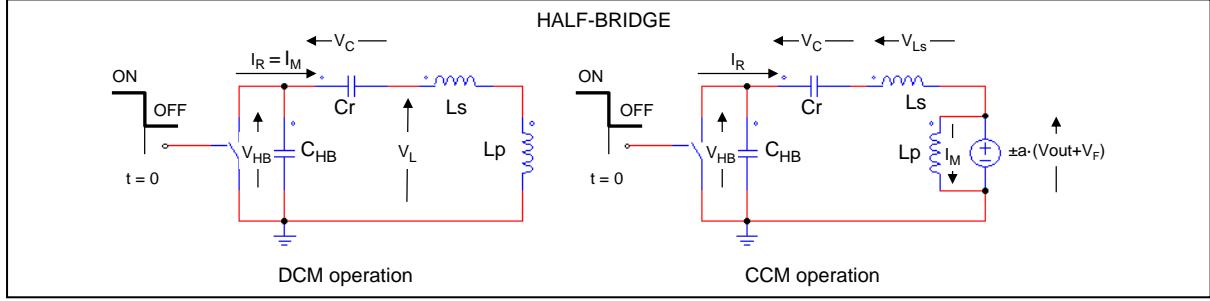
As previously mentioned, there is no overlap between the conduction of Q1 and Q2, rather there is a dead-time  $T_D$  between the turn-off of one switch and the turn-on of the other one where they are both open; in normal operation the edges of  $V_{HB}$  occur when Q1 or Q2 are switched off and it takes some time for  $V_{HB}$  to swing rail-to-rail.

So, we are now interested in determining the transition times of the half-bridge midpoint node HB when Q1 and Q2 are turned off. This is important to completely characterize the square wave  $V_{HB}$  and, what is more, to determine the conditions for the edges of  $V_{HB}$  to occur when Q1 or Q2 are switched off or, in other words, the conditions for Q1 and Q2 to be turned on with ZVS.

To do so, it is necessary to consider the equivalent circuit during the transition. For simplicity we will consider only the turn-off of Q2, corresponding to the positive-going edge of  $V_{HB}$ , because the turn-off of Q1 is exactly mirror-symmetric.

Depending on whether the transition starts while there is current circulating on the secondary side (CCM operation) or not (DCM operation), different equivalent circuits must be considered, as depicted in figure 22. Direction of currents and voltages is as shown.

**Figure 22. Equivalent circuits for the analysis of the transitions of  $V_{HB}$  at Q2 turn-off.**



As previously seen, when the secondary rectifiers do not conduct,  $L_p$  and  $L_s$  form a single inductor  $L_s + L_p$ , so the tank current  $I_R(t)$  that flows through  $L_s$  and the current  $I_M(t)$  flowing through  $L_p$  are the same. When the secondary rectifiers are conducting the currents  $I_R(t)$  and  $I_M(t)$  are different (the secondary current is  $a$  times their difference) and there is a constant voltage equal to  $\pm a \cdot (V_{out} + V_{Rect})$  across  $L_p$ , so that  $L_p$  can be replaced by a voltage generator for the purpose of the analysis. The sign of this generator depends on the difference  $I_R(t) - I_M(t)$ , i.e., on the direction of the current in the secondary winding: if  $I_R(t) > I_M(t)$  it has the “+” sign and the “-“ sign if  $I_R(t) < I_M(t)$ .

In both circuits, Q2 is replaced by an ideal switch that opens at  $t = 0$ . As we can see, a tank circuit is involved during the transitions, whence the denomination *resonant transitions* given to the swings of the node HB.

The initial conditions of the circuit are:  $V_{HB}(0) = 0$ ,  $V_C(0) = V_{C0}$ ,  $I_R(0) = I_{R0}$ ,  $dV_{HB}/dt(0) = -I_{R0}/C_{HB}$ . Both  $V_{C0}$  and  $I_{R0}$  depend on the design of the LLC tank and the operating conditions of the converter and are assumed to be known quantities.

During the transient  $C_r$  and  $C_{HB}$  are effectively in series; it is normally  $C_r \gg C_{HB}$  (typically, two orders of magnitude), so that the changes of the  $V_C$  voltage during the transient can be neglected. Therefore, it is possible to assume  $V_C = V_{C0}$  during the transient and replace  $C_r$  with a constant voltage generator  $V_{C0}$ .

The equations governing the operation of the circuits in figure 22 are:

$$\begin{cases} \frac{d^2V_{HB}}{dt} + \frac{1}{(L_s+L_p)C_{HB}} V_{HB} = \frac{V_{C0}}{(L_s+L_p)C_{HB}} & (\text{DCM}) \\ \frac{d^2V_{HB}}{dt} + \frac{1}{L_s C_{HB}} V_{HB} = \frac{V_{C0} \pm a(V_{out}+V_{Rect})}{L_s C_{HB}} & (\text{CCM}) \end{cases} \quad (6)$$

The solutions of these equations are:

$$V_{HB}(t) = \begin{cases} V_{C0} + \frac{V_{C0}}{\sin \varphi_O} \sin(\omega_O t - \varphi_O) & (\text{DCM}) \\ V_{C0} \pm a(V_{out} + V_{Rect}) + \frac{V_{C0} \pm a(V_{out}+V_{Rect})}{\sin \varphi_C} \sin(\omega_C t - \varphi_C) & (\text{CCM}) \end{cases}, \quad (7)$$

with:

$$\omega_O = \frac{1}{\sqrt{(L_s+L_p)C_{HB}}} = 2\pi \sqrt{\frac{C_r}{C_{HB}}} f_{R2}; \quad \varphi_O = \tan^{-1} \left( -\frac{V_{C0}}{I_{R0}} \sqrt{\frac{C_{HB}}{L_s+L_p}} \right). \quad (8a)$$

$$\omega_C = \frac{1}{\sqrt{L_s C_{HB}}} = 2\pi \sqrt{\frac{C_r}{C_{HB}}} f_{R1}; \quad \varphi_C = \tan^{-1} \left( -\frac{V_{C0} \pm a(V_{out}+V_{Rect})}{I_{R0}} \sqrt{\frac{C_{HB}}{L_s}} \right). \quad (8b)$$

The expression of the tank current is:

$$I_R(t) = -C_{HB} \frac{dV_{HB}(t)}{dt} = \begin{cases} \frac{I_{R0}}{\cos \varphi_O} \cos(\omega_O t - \varphi_O) & (\text{DCM}) \\ \frac{I_{R0}}{\cos \varphi_C} \cos(\omega_C t - \varphi_C) & (\text{CCM}) \end{cases}. \quad (9)$$

Equations (6) to (9) apply in the time interval  $(0, T_T)$ , where  $T_T$  is the time needed for the voltage  $V_{HB}$  to reach  $V_{in}$ .  $T_T$  can be calculated from (7) imposing that  $V_{HB}(T_T) = V_{in}$ :

$$T_T = \begin{cases} \frac{1}{\omega_O} \left[ \varphi_O + \sin^{-1} \left( \frac{V_{in} - V_{C0}}{V_{C0}} \sin \varphi_O \right) \right] & (\text{DCM}) \\ \frac{1}{\omega_C} \left\{ \varphi_C + \sin^{-1} \left[ \frac{V_{in} - V_{C0} \mp a(V_{out} + V_{Rect})}{V_{C0} \pm a(V_{out} + V_{Rect})} \sin \varphi_C \right] \right\} & (\text{CCM}) \end{cases} \quad (10)$$

In (10) the value of  $C_{HB}$  used to calculate  $\varphi_C$  and  $\varphi_O$  with (8a), (8b) will include the time-equivalent linear capacitance  $C_{eT}$  of Q1 and Q2.

We find the value of the resonant current at the end of the transition by substituting (10) in (9):

$$I_R(T_T) = \begin{cases} \frac{I_{R0}}{\cos \varphi_O} \sqrt{1 - \left( \frac{V_{in} - V_{C0}}{V_{C0}} \right)^2 \sin^2 \varphi_O} & (\text{DCM}) \\ \frac{I_{R0}}{\cos \varphi_C} \sqrt{1 - \left( \frac{V_{in} - V_{C0} \mp a(V_{out} + V_{Rect})}{V_{C0} \pm a(V_{out} + V_{Rect})} \right)^2 \sin^2 \varphi_C} & (\text{CCM}) \end{cases} \quad (11)$$

In (11) the value of  $C_{HB}$  used to calculate  $\varphi_C$  and  $\varphi_O$  with (8a), (8b) will include the Z-equivalent linear capacitance  $C_{eZ}$  of Q1 and Q2.

Equations (6) to (9) are applicable in the time interval  $(0, T_T)$  with  $T_T$  given by (10), provided the initial condition, DCM/CCM, is maintained in that interval. Specifically:

- in case of DCM transition at  $t = 0$  the relevant equations are applicable until  $T_T$  or until the tank current  $I_R(t)$ , under the action of the positive-going edge of  $V_{HB}$ , becomes greater than the current  $I_M(t)$  flowing through  $L_p$  (i.e., current starts flowing on the secondary side), whichever condition occurs first.
- In case of CCM transition at  $t = 0$  the relevant equations are applicable until  $T_T$  or until  $I_R(t) = I_M(t)$  (i.e., the secondary current zeroes), whichever condition occurs first. Note that in (6) the  $a \cdot (V_{out} + V_{Rect})$  generator has the “-” sign because  $I_R(t)$  is increasing under the action of the positive-going edge of  $V_{HB}$ ; if it equals  $I_M(t)$  at  $t = t_Z$ , it was necessarily  $I_R(t) < I_M(t)$  at  $t = 0$ .

In case of DCM transition, if the condition  $I_R(t) > I_M(t)$  occurs at a time instant  $t_Z \in (0, T_T)$  with  $T_T$  given by (10), the transition will be described by the DCM equation (6) in the time interval  $(0, t_Z)$  and then by the CCM equation (6) in the time interval  $(t_Z, T_T)$ , where  $T_T$  is the resulting transition time.  $T_T$  is found starting from the CCM equation 6 where the  $a \cdot (V_{out} + V_{Rect})$  generator has the “+” sign, with the initial conditions given by the DCM equations (7) and (9) at  $t = t_Z$ .

The time instant  $t_Z$  can be found considering that in order for  $I_R(t)$  to be greater than  $I_M(t)$  and have current on the secondary side, the voltage across the parallel inductance  $L_p$  must equal  $a \cdot (V_{out} + V_{Rect})$ . With reference to the DCM circuit of figure 22, this occurs when

$$V_L \frac{L_p}{L_s + L_p} = (V_{HB} - V_{C0}) \frac{L_p}{L_s + L_p} = a(V_{out} + V_{Rect}), \quad (12)$$

that is, when:

$$V_{HB} = V_{C0} + a(V_{out} + V_{Rect}) \left( 1 + \frac{L_s}{L_p} \right). \quad (13)$$

Therefore:

$$t_Z = \frac{1}{\omega_O} \left\{ \varphi_O + \sin^{-1} \left[ \frac{a(V_{out} + V_{Rect})}{V_{C0}} \left( 1 + \frac{L_s}{L_p} \right) \sin \varphi_O \right] \right\}. \quad (14)$$

Of course, the condition for a DCM-CCM transition to occur is that  $V_{HB}$  given by (13) is less than  $V_{in}$ , otherwise the transition will be entirely DCM.

In case of CCM transition, if the condition  $I_R(t) = I_M(t)$  occurs at  $t = t_Z \in (0, T_T)$  with  $T_T$  given by (10), in most cases the transition becomes DCM after  $t_Z$ , thus it will be described by the CCM equation (6), in  $(0, t_Z)$  and then by the DCM equation (6) in  $(t_Z, T_T)$ .  $T_{T^*}$  is derived from the DCM equation (6) with the initial conditions given by the CCM equations (7) and (9) at  $t = t_Z$ .

For completeness it is worth mentioning that it is possible to observe CCM-CCM transitions in a very limited range of operation, where the condition  $I_R(t) = I_M(t)$ , i.e., zero secondary current, occurs in a single point in time. The equations (6) describing these transitions differ by the sign of the generator  $a \cdot (V_{out} + V_{Rect})$  that changes from “-” to “+”. These are normally of no concern for the design of the LLC tank.

All these “hybrid” transitions occur in a large range of operating conditions; if we exclude some extreme operating conditions, the resulting values of  $T_T$  do not significantly differ from those calculated with (10), thus we will consider  $T_T$  only.

Figure 23 shows the equivalent circuits for the analysis of the transitions of the voltages  $V_{HB1}$  and  $V_{HB2}$  of a full bridge LLC resonant converter when the diagonal Q2-Q3 is turned off.

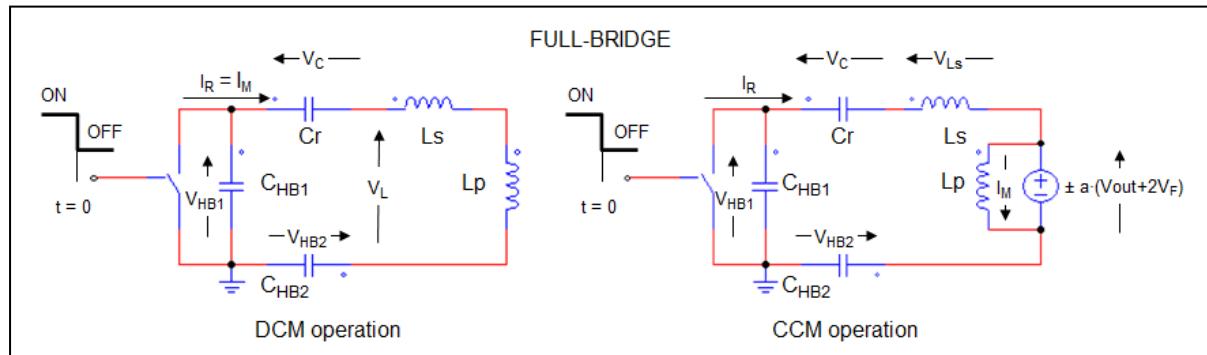
The initial conditions of the circuits are:  $V_{HB1}(0) = 0$ ,  $V_{HB2}(0) = Vin$ ,  $V_C(0) = V_{C0}$ ,  $I_R(0) = I_{R0}$ ,  $dV_{HB1}/dt(0) = -I_{R0}/C_{HB1}$ ,  $dV_{HB2}/dt(0) = I_{R0}/C_{HB2}$ .

Notice that the two nodes HB1 and HB2 move in a complementary way, so that along the transition it is  $V_{HB1}(t) + V_{HB2}(t) = Vin$ .

Notice also that  $C_{HB1}$  and  $C_{HB2}$  are dynamically in series, so that they can be unified in a single capacitor of the appropriate value. Assuming for simplicity that they are equal, they can be replaced by a single capacitor  $C_{HB} = C_{HB1}/2 = C_{HB2}/2$ .

It is convenient to consider this single capacitor in place of  $C_{HB1}$  to analyze the transition of  $V_{HB1}$ ; that of  $V_{HB2}$  will be simply given by  $Vin - V_{HB1}$ . With this choice it is possible to reuse the same formulas (6) to (14) for  $V_{HB1}$  and easily derive those for  $V_{HB2}$ .

**Figure 23. Equivalent circuits for analyzing the transitions of  $V_{HB1}$ ,  $V_{HB2}$  at Q2-Q3 turn-off.**



## Chapter 3

### ZVS conditions analysis

The previous analysis provided us with all the elements to find what conditions must be met to have the primary switches operated with ZVS under steady-state conditions. In a correctly designed converter these conditions must be met throughout the entire operating range, with some margin too to account for the tolerances of the LLC tank and the other components. Again, for simplicity during the discussion we will refer to the half-bridge version only because, to extend what we plan to say to the full-bridge version, the changes are obvious.

As previously said, to achieve ZVS the value of  $T_T$  given by (10) must not exceed the dead time  $T_D$  to make sure that Q1 and Q2 are turned on with zero  $V_{DS}$  and not while the node HB is still flying and their  $V_{DS}$  is still greater than zero. Note, however, that this condition is only necessary. To ensure ZVS other conditions must be fulfilled.

From the previous analysis it is also possible to derive sufficient conditions. To have the expected positive-going edge of  $V_{HB}$  when Q2 is turned off (negative-going edge of  $V_{HB}$  when Q1 is turned off), the resonant  $I_R(t)$  current must be able to charge (discharge) the capacitor  $C_{HB}$  until  $V_{HB} = V_{in}$  ( $V_{HB} = 0$ ). Therefore, not only  $I_{R0}$  must be negative (positive), but also  $I_R(t)$  must remain negative (positive) during the transition of the HB node. In fact, if  $I_{R0}$  was positive (negative) the capacitance  $C_{HB}$  would be discharged (charged) and  $V_{HB}$  will not rise (fall) but go negative (over  $V_{in}$ ). In the actual circuit  $V_{HB}$  will be clamped at a slightly negative voltage by the body diode of Q2 DQ2 (slightly over  $V_{in}$  by the body diode of Q1, DQ1). Further, should  $I_{R0}$  be negative (positive) and  $I_R(t)$  change sign before  $V_{HB}$  reaches  $V_{in}$  or zero, the transition of  $V_{HB}$  would reverse direction along the way, thus ZVS would be lost. Notice, therefore, that saying that the resonant current must not change sign during the transition is equivalent to saying that the amplitude of the transition must be larger than  $V_{in}$ .

In a system where the dead-time  $T_D$  between the turn-off of a switch and the turn-on of the other one tracks the duration of the transition time  $T_T$ , the combination of the two conditions:

- a)  $T_T \leq T_D$  (which is intrinsic in this case).
- b) During the low-to-high transition of  $V_{HB}$  the resonant current must be negative, during the high-to-low transition of  $V_{HB}$  the resonant current must be positive.

represents a necessary and sufficient condition to ensure ZVS of the primary switches (Q1, Q2 in the half bridge, Q1, ..., Q4 in the full bridge).

In a system where  $T_D > T_T$  is fixed somehow, it is necessary that the tank current  $I_R(t)$  keeps its sign unchanged during the entire time interval  $(0, T_D)$ . Should the current become zero in a time instant between  $T_T$  and  $T_D$ , DQ2 (DQ1) would not be forward biased any more, and the voltage  $V_{HB}$ , no more constrained to zero ( $V_{in}$ ), would experience oscillations at an angular frequency equal to either  $\omega_0$  or  $\omega_c$ . Q1 (Q2) would then be turned on at  $t = T_D$  with a drain-source voltage in general greater than zero.

Once the transition is completed at  $t = T_T$  and the voltage  $V_{HB}$  is clamped at essentially  $V_{in}$  by the body diode of Q1 DQ1, the tank current  $I_R(t)$  and the resonant capacitor voltage  $V_C(t)$  evolve according to the equations that describe the operation of the LLC tank during each half switching cycle. If also during the time interval  $(T_T, T_D)$   $V_C$  can be still considered equal to  $V_\infty$ , we can consider again the equivalent circuit of figure 22 where the switch is open

and the capacitor  $C_{HB}$  is replaced by a voltage source  $V_{in}$ . With this assumption, there is a constant voltage  $V_{in} - V_{C0}$  across  $L_s + L_p$  in case of DCM transitions and a constant voltage  $V_{in} - V_{C0} \mp a(V_{out} + V_{Rect})$  across  $L_s$  in case of CCM transitions, and the resonant current  $I_R(t)$  evolves linearly. If  $T_D$  exceeds  $T_T$  by more than:

$$T_{zz} = \begin{cases} \frac{L_s + L_p}{V_{in} - V_{C0}} I_R(T_T) & (\text{DCM}) \\ \frac{L_s}{V_{in} - V_{C0} \mp a(V_{out} + V_{Rect})} I_R(T_T) & (\text{CCM}) \end{cases}, \quad (15)$$

then the resonant current zeroes and  $V_{HB}$  starts oscillating and at the end of the dead-time the  $V_{DS}$  of Q1 will be larger than zero and ZVS will be lost. In this case the necessary and sufficient condition for ZVS of primary switches is:

- a)  $T_T \leq T_D \leq T_T + T_{zz}$ , with  $T_{zz}$  given by (15).
- b) During the low-to-high transition of  $V_{HB}$  the resonant current must be negative, during the high-to-low transition of  $V_{HB}$  the resonant current must be positive.

or alternatively:

- a)  $T_T \leq T_D$ .
- b) The resonant current must be negative during the dead-time relevant to the low-to-high transition of  $V_{HB}$ , it must be positive during the dead-time relevant to the high-to-low transition of  $V_{HB}$ .

This can be visualized in figure 24, which refers to  $\text{Q2} \Rightarrow \text{OFF}$ ,  $\text{Q1} \Rightarrow \text{ON}$  transition and where the condition  $T_T \leq T_D$  is clearly fulfilled. The current  $I_R(t)$  represented by the solid line is negative throughout the dead-time  $T_D$ , i.e., it fulfills the condition  $T_T + T_{zz} \geq T_D$ , and then ensures ZVS. In contrast, the current  $I_R(t)$  represented by the dotted line is negative only in the first part of the dead-time  $T_D$ , so it does not fulfill the condition  $T_T + T_{zz} \geq T_D$  and ZVS does not occur.

Notice that here we find again that when switches work with ZVS their initial operating point is in their 3<sup>rd</sup> quadrant of operation.

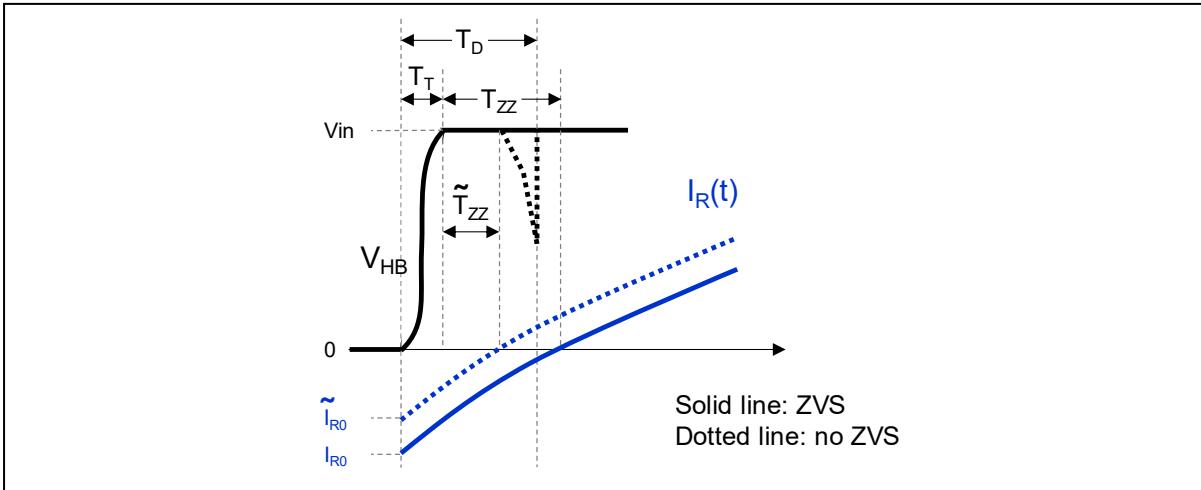
It is instructive to review the switching mechanism and the conditions for ZVS in the timing diagram of figure 25. Q2 opens in the instant  $t_0$  and its current falls quickly and zeroes at  $t = t_1$ . The voltage  $V_{HB}$  then falls until  $t = T_T$ , when it hits the input bus voltage and the body diode of Q1, DQ1, becomes forward biased, thus clamping the voltage at a diode forward drop  $V_F$  over  $V_{in}$ .  $I_R(t)$  will go on flowing through DQ1 for the remaining part of the dead-time  $T_D$  until  $t = t_2$  when Q1 turns on and its  $R_{DS(on)}$  shunts DQ1. When this occurs, the voltage across Q1 is  $-V_F$ , a value negligible as compared to the input voltage  $V_{in}$ . In the end, the turn-on transition of Q1 is done with negligible dissipation due to voltage-current overlap and with its  $C_{oss}$  already discharged, so that there will be no significant capacitive loss either. This is ZVS.

Note that during the turn-off of Q2 there is some voltage-current overlap during the time interval  $(t_0 - t_1)$ . There is some power loss associated to that but if the time interval  $(t_0 - t_1)$  is significantly shorter than the transition time  $(t_0 - T_T)$  this loss is relatively low. This happens if the capacitance  $C_{HB}$ , which acts as a snubber, is large enough. The good news is that we can artificially increase  $C_{HB}$  (by adding an external capacitor) to reduce the turn-off losses of Q1 and Q2 with no penalty at turn-on as long as they are switched on with ZVS.

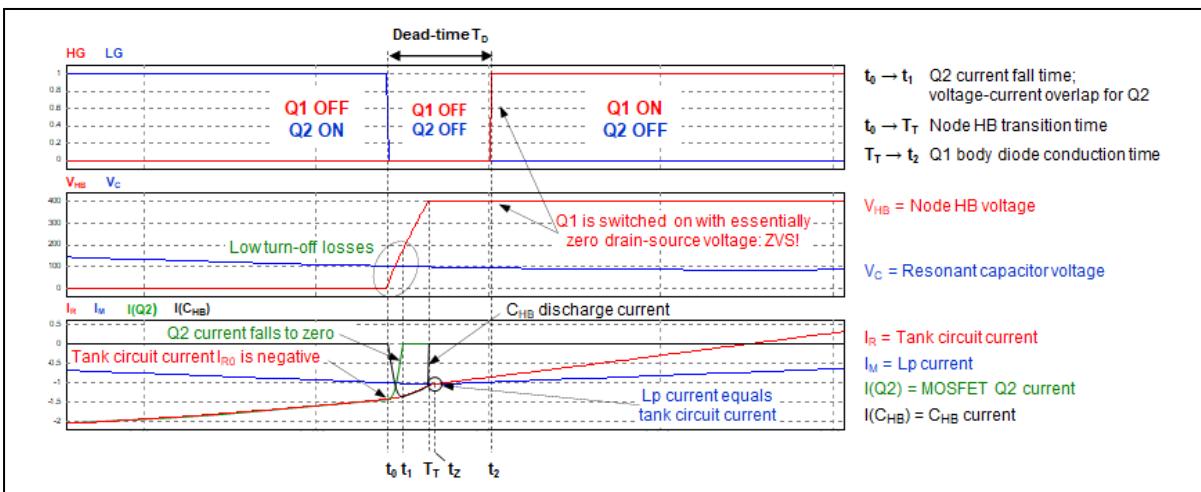
Now we want to relate the ZVS conditions to the operating frequency of the switch network.

In the end, if the tank current at the end of  $V_{HB}$  transitions has a sign opposite to that of  $V_{HB}$ , both switches may work with ZVS at turn-on (remember that this condition alone is not sufficient).

**Figure 24. Schematic description of  $V_{HB}$  and  $I_R(t)$  zero-crossings; ZVS conditions.**



**Figure 25. Detail of Q2 ON-OFF & Q1 OFF-ON CCM transition with ZVS for Q1.**



The resonant current is sinusoidal or piecewise sinusoidal, so that applying a high  $V_{HB}$  level (positive by definition) the initially negative tank current will become positive after some time; similarly, applying a low  $V_{HB}$  level (negative by definition), the initially positive tank current will become negative after some time. This happens if the tank current lags behind  $V_{HB}$ , in other words if the zero-crossings of the tank current occur after the zero-crossings of the applied voltage.

Inductors behave in this way: when subject to an ac voltage, their ac current lags the voltage. Therefore, a necessary condition for ZVS to occur is that the LLC tank behaves as an inductor overall. This happens in a certain region of the operating frequency that is called therefore the *inductive region*.

It is intuitive that to make the LLC tank circuit behave like an inductor, that is, have the zero-crossings of the tank current lag the zero-crossings of the applied voltage  $V_{HB}$ , the frequency of  $V_{HB}$  must be larger than a certain value. This is something natural in circuits under sinusoidal excitation (at high frequencies the inductive impedance dominates over capacitive impedance); here we have a square wave excitation and for the moment we can provide a physical explanation without invoking impedance concepts that will be introduced later in the discussion.

Let us consider again an initial condition where Q2 is closed, Q1 open and the tank current is negative (flowing out of the LLC tank). The necessary condition for ZVS is fulfilled. As Q2 is switched off,  $V_{HB}$  goes positive and Q1 is switched on after the dead-time, as shown in figure 25. After some more time also the tank current becomes positive. Now, if we want to have ZVS for Q2 in the next turn-on, in that instant the tank current must be still positive to meet the necessary condition for ZVS. This will occur if Q1 is switched off (and Q2 on after the dead-time) before the tank current naturally reverses its sign, that is, before a certain reversal time  $T_R$  elapses from Q2 switch-off.

This sets a lower limit to the frequency  $f_{sw}$  of  $V_{HB}$  where ZVS can be achieved. Considering that there will be at least a  $2T_R$  time interval between one turn-off of, say, Q1 and the next one, this limit can be expressed as:

$$f_{sw} > \frac{1}{2T_R}. \quad (16)$$

The inductive region for the LLC converter extends above this minimum switching frequency; in the region below this minimum frequency ZVS cannot occur.

Before going further, it is important to observe that operating in the inductive region (where impedance, intended in a broad sense, increases with frequency) implies that power flow can be controlled in closed-loop operation by changing the frequency of  $V_{HB}$  in such a way that a reduced power demand from the load produces a frequency rise, while an increased power demand causes a frequency reduction.

To assess  $T_R$  the most unfavorable case is when the tank current is made up of a single sinusoid at  $f = f_{R1}$ . In this case the tank current will be again negative half the resonance period  $1/f_{R1}$  after it has become positive, then after a time larger than  $1/2f_{R1}$  from the turn-off of Q2.

The previous analysis can be summarized in the following points:

- At frequencies  $f_{sw} \geq f_{R1}$  the necessary condition for ZVS is met.
- A frequency  $f_{CM} = 1/2T_R$ , with  $f_{R2} < f_{CM} < f_{R1}$ , exists where the resonant current  $I_R(t)$  and the applied voltage  $V_{HB}$  are in-phase ( $I_R(t)$  crosses zero as  $V_{HB}$  transitions from one level to the other, both in the same direction); we will show that  $f_{CM}$  is a function of the output load and that as the load goes from open circuit to short circuit  $f_{CM}$  goes from  $f_{R2}$  to  $f_{R1}$ .
- The necessary condition for ZVS is met at frequencies  $f_{sw} > f_{CM}$ , it is not for  $f_{sw} \leq f_{CM}$ .

When  $f_{sw} < f_{CM}$ ,  $I_R(t)$  leads  $V_{HB}$  (the zero-crossings of the tank current occur before the zero-crossings of  $V_{HB}$ ), thus the tank circuit behaves like a capacitor, whence the term *capacitive mode operation* when the LLC converter works in that frequency region (*capacitive region*).

It is worth mentioning that under steady-state conditions the ZVS necessary condition are met in some frequency intervals in the region  $f_{sw} \leq f_{R2}$  named *pseudo-inductive regions*. It is possible to observe LLC converters operated in these regions in case of anomalous operating conditions with some protection schemes.

As previously stated, working in the inductive region is not a sufficient condition for ZVS to occur: the duration of the dead-time  $T_D$  must fulfill the previously mentioned conditions a), that is, in general,  $T_T \leq T_D \leq T_T + T_{zz}$ , with  $T_T$  given by (10) and  $T_{zz}$  given by (15).

There is a frequency range in the inductive region, bordering the boundary with the capacitive region ( $f_{sw} \geq f_{CM}$ ), where the zero crossing of the tank current, though lagging, is so close to the zero crossing of  $V_{HB}$  that the tank current zeroes within the dead-time or even

before completing the transition so that the node HB cannot swing “rail-to-rail” and ZVS cannot be achieved. When  $f_{sw} = f_{CM}$  Q1 or Q2 are turned off with a tank current that is initially zero and during the dead-time has the wrong direction (negative when Q1 turns off, positive when Q2 turns off). This means that  $V_{HB}$  is not forced to transition, rather it is forced to keep its level, and  $V_{HB}$  transitions when the other switch is turned on after the dead-time.

It is interesting to have a closer look at this border region close to the inductive-capacitive boundary and examine the types of behavior shown in figure 26. They refer to the  $Q2 \Rightarrow OFF$ ,  $Q1 \Rightarrow ON$  transition; those related to the opposite transition are obviously turned upside down.

Going from a) to d), the switching frequency is progressively reduced so that converter’s operation is moved closer and closer to the capacitive-inductive boundary and there is a progressive behavior change from soft switching to hard switching.

Case a) is in the inductive region, away enough from the capacitive-inductive boundary so that  $I_R(t)$  crosses zero nearly at the end of the dead-time  $T_D$ ; Q1 turns on nearly with ZVS with no significant losses. This is essentially the upper limit of the border region, and the lower limit of the region where ZVS is achieved. We indicate with  $f_{ZVS}$ , the corresponding operating frequency.

Case b) is closer to the boundary and  $I_R(t)$  crosses zero well within the dead-time  $T_D$ ;  $V_{HB}$  starts its swing with an amplitude that is still larger than  $V_{in}$ ; as  $I_R(t)$  reverses,  $V_{HB}$  goes down again so Q1 will experience capacitive losses at turn-on; notice that at the end of the dead time the voltage does not reach zero, hence the body diode of Q2 DQ2 is not conducting; this type of hard switching is termed *type-1 hard switching*. Here ZVS would have been still possible with a shorter dead-time.

Case c) is slightly closer to the boundary and  $I_R(t)$  still crosses zero within the dead-time but a bit earlier compared to case b); the swing of the node HB becomes smaller than  $V_{in}$ , so that  $V_{HB}$  does not reach  $V_{in}$  and a shorter dead-time might result in *peak switching* but not in ZVS; after reaching the peak as  $I_R(t)$  crosses zero,  $V_{HB}$  goes down but does not yet reach zero, thus there is again a type-1 hard switching with associated capacitive losses.

Case d) is extremely close to the inductive-capacitive boundary: the tank current reverses closer to Q2 turn-off and the  $V_{HB}$  ringing appears as a small voltage bump;  $V_{HB}$  falls below zero within the dead-time, forward biasing DQ2 so that it conducts for the remainder of the dead-time; when Q1 turns on and pulls  $V_{HB}$  to  $V_{in}$ , its reverse recovery is invoked; this type of hard switching for Q1 where DQ2 is reverse-recovered is termed *type-2 hard switching*.

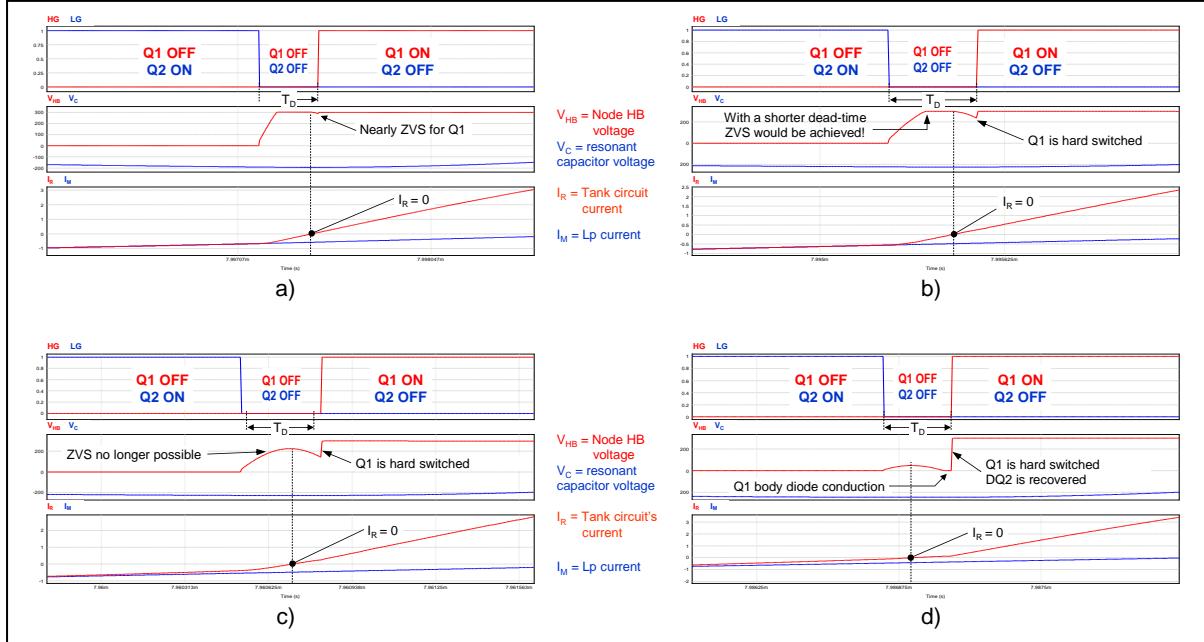
If we further reduce the switching frequency,  $I_R(t)$  will cross zero before Q2 turns off, thus it is easy to predict that the small bump in  $V_{HB}$  disappears and  $V_{HB}$  stays flat until pulled to  $V_{in}$  as Q1 is turned on, with no significant change in behavior compared to case d).

It is interesting to notice that in cases a) and b) the transition starts as DCM ( $|I_R(t)| = |I_M(t)|$ , then no secondary current when Q2 is turned off) and becomes CCM ( $|I_R(t)| > |I_M(t)|$ , secondary current starts flowing) before the transition is completed.

Approaching the capacitive-inductive boundary (cases c) and d)), when Q2 is turned off it is already  $|I_R(t)| > |I_M(t)|$  (secondary current is already flowing), thus the transition is entirely CCM.

Finally, it is worth pointing out that in case of a control system with a fixed dead-time, the LLC converter must be designed not to exceed the case a) situation in the worst-case. With a control system that adaptively changes the dead-time  $T_D$  to track the transition time  $T_T$ , the LLC converter could be designed to work until the boundary between case b) and case c).

**Figure 26. Bridge leg transitions in the vicinity of inductive-capacitive regions boundary.**



The discussion on the switching mechanism has been focused on the primary-side switches so far, and the conditions in order for them to achieve ZVS at turn-on have been found. One important merit of the LLC resonant converter is that also the rectifiers on the secondary side are soft-switched: they feature zero-current-switching (ZCS) at both turn-on and turn-off.

In fact, the secondary current is proportional to the difference  $|I_R(t)| - |I_M(t)|$  so it starts flowing when, during the evolution of the primary currents in a switching cycle, it is  $|I_R(t)| > |I_M(t)|$ . The onset of this condition is determined by the voltage across  $L_p$  equaling  $\pm a \cdot (V_{out} + V_{Rect})$ , which forward biases the secondary rectifiers. Therefore, the two events, forward bias and current becoming greater than zero are simultaneous. This is a fortunate coincidence of ZVS and ZCS at turn-on. This is true to a first approximation: we will see in the following (Part III, Chapter 1) that considering some real-world parasitic elements of the power switches this simultaneity does not occur. It will not be exactly ZCS but for the moment let us assume it is.

The secondary current ceases to flow when  $|I_R(t)| = |I_M(t)|$ . As long as current flows on the secondary side the voltage across  $L_p$  equals  $\pm a \cdot (V_{out} + V_{Rect})$  thus forward biasing the secondary rectifiers. The voltage on  $L_p$  may reverse only when the secondary current zeroes, so that it is no more constrained. Therefore, at turn-off they become reverse biased when their forward current is zero (ZCS at turn-off), and their reverse recovery is not invoked.

It is therefore possible to state that ZCS at turn-on and turn-off for the secondary rectifiers is a structural property of the LLC converter: it always happens no matter how the LLC tank is designed, irrespective of its operating conditions.

## Chapter 4

### Hard switching in the LLC resonant converter

Let us have now a closer look at the operation of the LLC converter when its primary switches work with type-1 and type-2 hard switching and at their consequences.

As previously stated, we have type-1 hard switching when the primary switches are turned on with nonzero  $V_{DS}$  and with the body diode of the just off switches nonconducting. We have seen (case b) of figure 26) that this occurs when  $f_{sw}$  is slightly less than  $f_{ZVS}$  but it may occur also when  $f_{sw} > f_{R1}$  if the initial current  $I_{R0}$  is too small to complete transitions within the dead-time. This case is illustrated in figure 27, which shows the operation at the maximum switching frequency where ZVS is not achieved because of a too slow transition of the node HB.

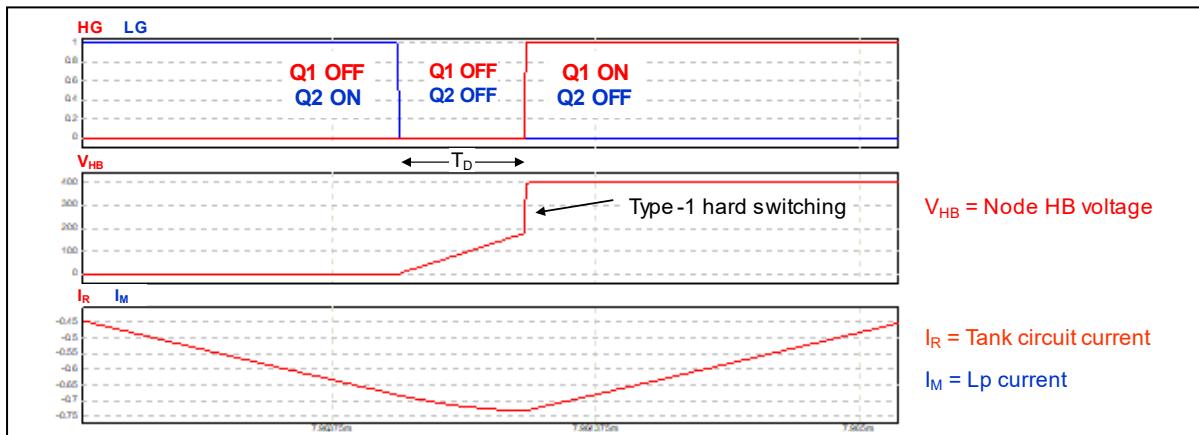
Note that in this case  $I_M(t)$  is just superimposed on  $I_R(t)$ , then no current is flowing on the secondary side: this means that  $C_{HB}$  is resonating with the total inductance  $L_s + L_p$  (DCM transition). Also, note that the resonant current peaks at the end of the  $V_{HB}$  transition, thus the condition  $T_D \leq T_T + T_{ZS}$  for ZVS does not generally matter and in this special case the condition  $T_T < T_D$  is necessary and sufficient for ZVS.

With type-1 hard switching one major consequence is that the switch undergoes considerable capacitive losses at turn-on. Few type-1 hard switching cycles are thermally insignificant, but continuous operation may cause MOSFETs to overheat and fail.

At heavy load, these losses might not be that high because the switching frequency is close to the minimum. However, they will add up to already significant conduction losses and the risk of overheating is not that improbable. Under no-load conditions, although the turn-on voltage is lower than  $V_{in}$  hence the associated energy of  $C_{HB}$  is lower, the operating frequency is usually considerably higher than close to the capacitive region. These power losses may be even considerably higher than total power normally dissipated under ZVS conditions, with consequent overheating.

Turn-on switching losses (voltage-current overlap) are insignificant at heavy load (i.e., close to the capacitive region) because turn-on is close to ZCS, and the operating frequency is low. At no-load these losses might not be negligible because switching frequency is high; it depends on the  $L_p$  current at the transition instants.

**Figure 27. Half bridge leg transition with type-1 hard switching under no-load conditions.**



Another negative consequence of type-1 hard switching is the generation of large common-mode EMI that adversely affects EMC compatibility. Finally, the slope of  $V_{HB}$  is much larger than with ZVS operation and there is the risk of  $dv/dt$  induced turn-on for the MOSFET just turned off if the gate-drive circuitry is not properly designed. This parasitic turn-on is caused by the current injected through its  $C_{GD}$  and flowing through the gate driver's pull down that holds the gate low, if large enough to raise the gate voltage up to the turn-on threshold. This would cause a lethal shoot-through condition for half bridge leg. In figure 19b it is possible to see the sign of this current injection as the small spike that follows the negative-going edge of the gate voltage. In this case the spike is too small to cause problems.

It is worth noticing that in these conditions the primary switches are almost soft switched at turn-off: if the case shown in figure 26 b) turn-off is almost with ZCS; in the case of figure 27 there is almost no voltage-current overlap at turn off due to the snubbing effect of  $C_{HB}$ .

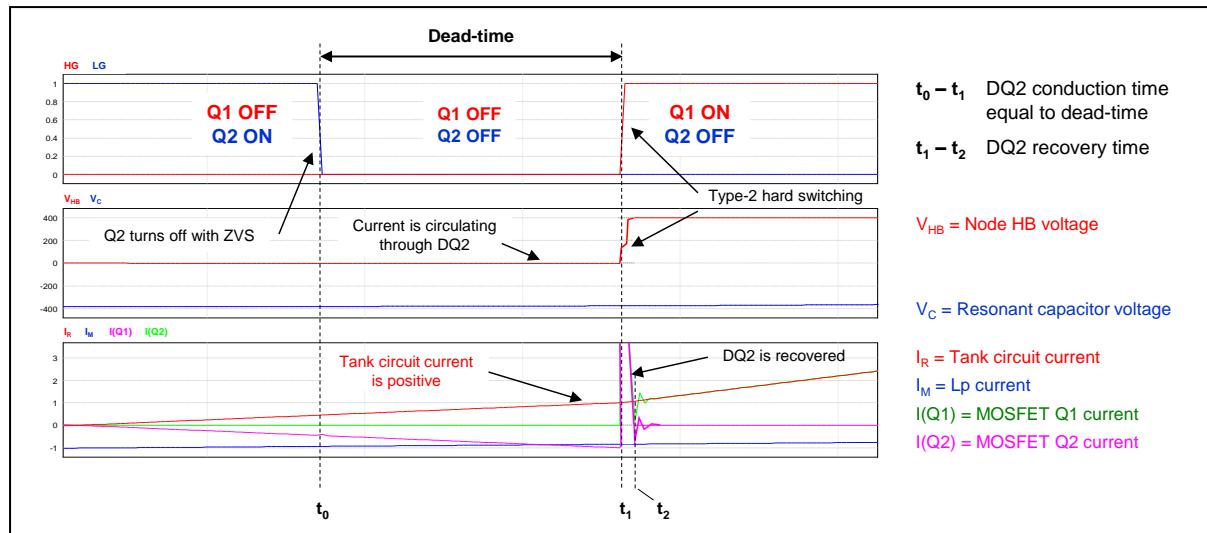
To analyze the type-2 hard switching, it is convenient to refer to the diagrams in figure 28, which show a hard transition starting from the state when Q2 is closed and Q1 open. In the time instant  $t_0$  when Q2 opens, the tank current is positive i.e., it is flowing into the LLC tank. With Q2 now open the current will go on flowing through DQ2 throughout the dead-time and will be switched to Q1 only when Q1 closes at  $t = t_1$ , the end of the dead-time.

As to Q2, it undergoes a true ZVS at turn-off because the voltage across it does not change significantly. Therefore, there will be no loss associated to turn-off, like what happens at turn-on when the converter works in the inductive region.

Q1, instead, will experience a totally different situation. Being DQ2 conducting during the entire dead-time, the voltage across Q1 at  $t = t_1$  equals  $V_{in} + V_F$  so that there will be a considerable voltage-current overlap with a corresponding peak of power loss in addition to the capacitive losses. In this respect, it is a condition identical to that of hard switched converters operated in CCM at turn-on.

In addition to that, however, the abrupt voltage reversal of  $V_{HB}$  occurring at  $t = t_1$  while the body diode DQ2 is conducting cannot be instantly blocked: DQ2 needs to be reverse recovered (i.e., the electrical charges in its forward-biased junction must be totally evacuated) before being able to block a reverse voltage. Hence, DQ2 will keep its low impedance and there will be a condition equivalent to a shoot-through between Q1 and Q2 until it recovers (at  $t = t_2$ ).

**Figure 28. Half bridge leg transition with type-2 hard switching.**



Of course, the same series of events described so far happens to Q1 and Q2 with exchanged roles when Q1 is turned off if  $I_R(t)$  is flowing out of the resonant tank circuit (negative current).

Even considering MOSFETs with ultra-fast and low reverse recovery charge body diode, DQ1 and DQ2 may easily undergo a reverse current spike with an amplitude much larger than the forward current it was carrying and relatively long in duration (in the hundred ns). This current spike will flow almost entirely through both switches because the resonant inductor  $L_S$  does not allow so abrupt current changes.

There is considerable peak of power dissipation in both Q1 and Q2 associated to this current spike because it occurs with a high  $V_{DS}$  for both. This power loss at turn-on, combined with the other turn-on losses, may easily result in overheating, since heat sinking is not usually sized to handle this abnormal condition.

This temporary shoot-through of the half-bridge leg during the reverse recovery of DQ1 and DQ2 is a potentially destructive condition. Not only is it because of the associated power dissipation or because one or more of the SOA boundaries of Q1 and Q2 are exceeded. In fact, as the body diode is recovering with its intrinsic  $dI/dt$ , the MOSFET experiences an extremely high  $dv/dt$  (many tens of V/ns!), due to the unavoidable parasitic inductances of the package, the PCB, etc. This  $dv/dt$  may exceed the critical value for the reverse recovery of its body diode (this critical value lowers when the MOSFET is hot). This would lead to an immediate failure because of the second breakdown of the parasitic bipolar transistor intrinsic in MOSFET structure.

The adverse effects of the reverse recovery of DQ1 and DQ2 do not end here. The risk of  $dv/dt$  induced turn-on for the MOSFET just turned off is in this case much higher than with type-1 hard switching because of the higher  $dv/dt$  involved; the common-mode noise generated by type-2 hard switching is much larger than that of type-1 hard switching; finally, the voltage spikes generated by the  $dI/dt$  of the reverse recovery on the stray inductances of the power circuit may damage any control IC coupled to the half-bridge leg by taking its pins violently below ground.

To summarize, type-1 hard switching may occur all over the operating frequency range, from the region bordering the capacitive region upwards, type-2 hard switching occurs only in the capacitive region, from the capacitive-inductive boundary downwards.

There is, however, an exception to this general rule, as reported in [19], that is worth mentioning for completeness.

When a MOSFET is turned on with ZVS, the current flowing through its body diode is mostly diverted into the channel and flows from source to drain; as current becomes positive (flowing from drain to source), the body diode is subject to a low reverse voltage, essentially the voltage drop across the  $R_{DS(on)}$ . The residual current through the body diode combined to its slow recovery and the low reverse voltage, further slowed down by the low reverse voltage, may cause the body diode to be still conductive as the MOSFET is turned off, thus preventing  $V_{HB}$  transition. If this condition lasts until the end of the dead-time and beyond, a type-2 hard switching will occur.

With present day MOSFET technologies normally this occurs at frequencies well over 1 MHz, even higher for MOSFETs with fast-recovery body diode. Since the issue shows up as a seeming longer MOSFET turn-off delay, the previously mentioned control system where the dead-time tracks the duration of the transition time can effectively prevent it.

In the end, operating the primary switches with ZVS brings the following benefits:

- 1) Low switching losses: either very high efficiency can be achieved if the half-bridge is operated at a not too high switching frequency or high switching frequency operation is possible with still acceptably high efficiency.
- 2) Reduction of the energy needed to drive the primary switches, thanks to the absence of Miller effect at turn-on: turn-on speed becomes unimportant because there is no voltage-current overlap but also gate charge is reduced, then a gate driver with a small source capability is viable.
- 3) Low noise and EMI generation minimize filtering requirements and make this converter extremely attractive in noise-sensitive applications.
- 4) The above-mentioned adverse effects of hard switching, which impair efficiency and jeopardize the converter, are prevented.

Therefore, working away from the capacitive region and operating the primary switches with ZVS is a must for the LLC converter both from the performance and the reliability point of view.

# Chapter 5

## Design-oriented ZVS conditions

The takeaway of the analysis of the ZVS conditions is that the converter must be operated in the inductive region of switching frequencies, but ZVS is not guaranteed throughout this region. Making the specified range of operating conditions for a converter entirely included within the region where ZVS is guaranteed is the result of an appropriate design of the LLC tank. In view of setting up a procedure to check if a design meets this goal, it is convenient to link the ZVS conditions we have examined so far to the operating conditions of the converter.

Summarizing the results of the previous analysis, on the one hand, the switching frequency must be kept at a safe distance from the capacitive-inductive boundary, i.e.,  $f_{sw} > f_{ZVS}$ , to prevent type-1 and type-2 hard switching. On the other hand, a minimum current  $I_{R0}$  at the beginning of the  $V_{HB}$  transitions must be ensured along the entire operating frequency range, to prevent type-1 hard switching also with  $f_{sw} > f_{R1}$ .

The condition  $f_{sw} > f_{ZVS}$  can be expressed also in terms of a minimum current  $I_{R0}$  needed at the beginning of the  $V_{HB}$  transitions as one MOSFET (in the half bridge) or a diagonal of MOSFETs (in the full bridge) is switched off. In fact, imposing that  $f_{sw} > f_{ZVS}$  means imposing that the distance in time between the zero crossing of the square wave voltage  $V_{HB}$  and the zero crossing of the tank current is larger than a certain value. If we know the slope of the tank current between the two zero-crossings, this distance in time can be expressed in terms of the initial value of the tank current.

As previously stated, once the transition of  $V_{HB}$  is completed at  $t = T_T$  and the voltage  $V_{HB}$  is clamped at essentially  $V_{in}$  by the body diode of Q1 DQ1, the tank current  $I_R(t)$  and the resonant capacitor voltage  $V_C(t)$  evolve according to the equations that describe the operation of the LLC tank during each half switching cycle. In particular, the tank current will be a sinusoidal arc that can be described by the following equation:

$$I_R(t) = \frac{|I_R(T_T)|}{\sin \theta} \sin(\omega t - \theta), \quad (17)$$

where  $\omega$  equals either  $2\pi f_{R1}$  or to  $2\pi f_{R2}$  depending on whether it is a CCM or DCM transition. We have observed that in the frequency region close to  $f_{ZVS}$  transitions are part or entirely CCM, so we will consider this case (then,  $\omega = \omega_{R1} = 2\pi f_{R1}$ ).

This sinusoid crosses zero at  $t = \theta / \omega_{R1}$  but this condition does not give us any information on the magnitude of  $I_R(T_T)$  needed to cross zero after  $t = T_D$ . Note, however, that at this moment we are just interested in the initial portion of  $I_R(t)$  that develops within  $T_D$ . Therefore, we can assume that during the time interval  $(T_T, T_D)$   $V_C$  can be still considered equal to  $V_{C0}$ , so that CCM equation (15) still applies. In the end the condition for ZVS,  $T_T + T_{zz} \geq T_D$ , becomes:

$$I_R(T_T) \geq \frac{V_{in} - V_{C0} - a(V_{out} + V_{Rect})}{L_S} (T_D - T_T). \quad (18)$$

With a similar reasoning we can derive the condition for ZVS on the other extreme where the transition is entirely DCM:

$$I_R(T_T) \geq \frac{V_{in} - V_{C0}}{L_S + L_p} (T_D - T_T). \quad (19)$$

In (18) and (19)  $T_T$  and  $I_R(T_T)$  are calculated with (10) and (11), respectively and finally the minimum  $I_{R0}$  can be calculated:

$$I_{R0} \geq \begin{cases} \frac{\cos \varphi_O}{\sqrt{1 - \left(\frac{V_{in} - V_{C0}}{V_{C0}}\right)^2}} \frac{V_{in} - V_{C0}}{L_s + L_p} (T_D - T_T) & (\text{DCM}) \\ \frac{\cos \varphi_C}{\sqrt{1 - \left(\frac{V_{in} - V_{C0} - a(V_{out} + V_{Rect})}{V_{C0} + a(V_{out} + V_{Rect})}\right)^2}} \frac{V_{in} - V_{C0} - a(V_{out} + V_{Rect})}{L_s} (T_D - T_T) & (\text{CCM}) \end{cases}, \quad (20)$$

where  $T_T$  is still given by (10).

It is possible to provide simpler formulas if one does not consider operating conditions that are too close to the inductive-capacitive boundary.

With the usual values of the quantities in (8a), (8b), the phase angles  $\varphi_C$  and  $\varphi_O$  are both considerably less than unity. Therefore, it is possible to consider the expansion of (10) and (11) to Maclaurin series truncated to the first terms. They are respectively:

$$T_T \approx \begin{cases} \frac{\varphi_O V_{in}}{\omega_O V_{C0}} & (\text{DCM}) \\ \frac{\varphi_C V_{in}}{\omega_C V_{C0} + a(V_{out} + V_{Rect})} & (\text{CCM}) \end{cases}. \quad (21)$$

$$I_R(T_T) \approx \begin{cases} I_{R0} \left\{ 1 - \frac{1}{2} \left[ \left( \frac{V_{in} - V_{C0}}{V_{C0}} \right)^2 - 1 \right] \varphi_0^2 \right\} & (\text{DCM}) \\ I_{R0} \left\{ 1 - \frac{1}{2} \left[ \left( \frac{V_{in} - V_{C0} - a(V_{out} + V_{Rect})}{V_{C0} + a(V_{out} + V_{Rect})} \right)^2 - 1 \right] \varphi_C^2 \right\} & (\text{CCM}) \end{cases}. \quad (22)$$

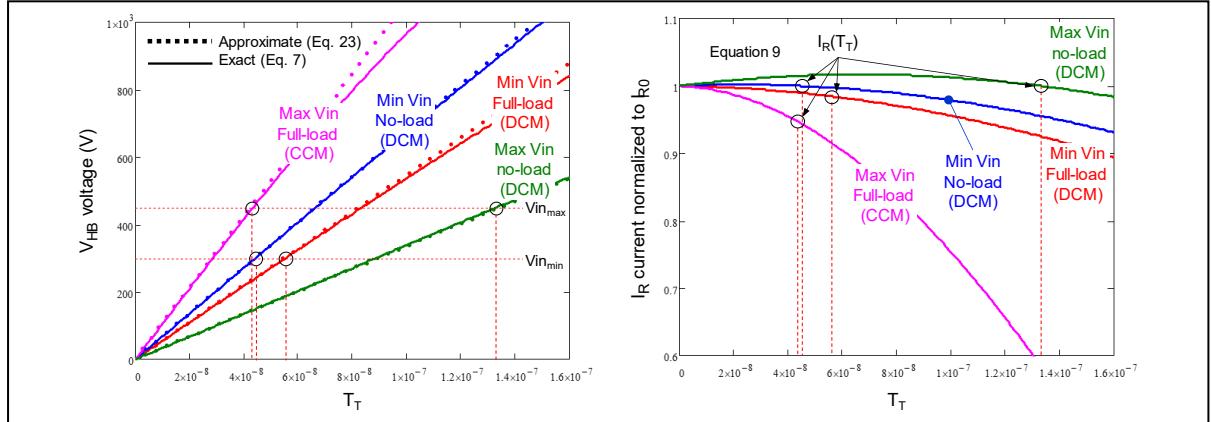
Note that in (22) there are not first-order terms for  $\varphi_C$  and  $\varphi_O$ : with a further slight loss of accuracy, it is therefore possible to assume  $I_R(T_T) \approx I_{R0}$ . With this approximation (7) and (10) can be simplified in:

$$V_{HB}(t) = -\frac{I_{R0}}{C_{HB}} t; \quad T_T = C_{HB} \frac{V_{in}}{|I_{R0}|} \quad (\text{DCM, CCM}). \quad (23)$$

These approximate relationships are accurate enough for design purposes under a large range of operating conditions, as shown in the left-hand diagram of figure 29 that refers to the four corner operating conditions in a typical LLC tank design whose operating range does not get too close to the region bordering the capacitive-inductive boundary.

Looking at the right-hand side plot of figure 29, which shows the plots of (9) normalized to  $I_{R0}$ , in this design the condition where accuracy is worst is at the maximum input voltage and full load, where the change of  $I_R(t)$  during the  $(0, T_T)$  interval is the largest. Anyway, the difference  $I_R(T_T) - I_{R0}$  is limited to less than 10%, so that the error on the average charge current in the  $(0, T_T)$  interval is less than 5%. In the other three corners the change in  $I_R(t)$  is much smaller.

**Figure 29. Assessment of accuracy of (23) and plot of (9) in a typical LLC tank design.**



The condition where accuracy is best is at the maximum input voltage and no load. In those conditions (23) is accurate and can be definitely used for checking ZVS.

Notice that in the design which the plots of figure 29 refer to, the transition at minimum  $V_{in}$  and maximum load where the switching frequency is at a minimum is a DCM type. In a more aggressive design that aims to get closer to the border region, the transition in those conditions would be a mixed DCM-CCM or a CCM type. In this case, the accuracy of (23) might not be acceptable and the more accurate formulae (7), (10) and (11) should be used.

To find a simple criterion to assess whether the accuracy of (23) might not be acceptable when the operating frequency is at a minimum it is possible to observe in figure 26 that the  $V_{C0}$  voltage is strongly negative, so that the quantity  $V_{C0} \pm a(V_{out} + V_{Rect})$  that appears in the amplitude of  $V_{HB}(t)$  swing (7) is small, so that they essentially disappear from the CCM circuits in figures 22 and 23. At this point it is possible to estimate the minimum current  $I_{R0}$  that ensures a full rail-to-rail  $V_{HB}$  swing with a simple energy balance:

$$\frac{1}{2} L_s I_{R0}^2 \geq \frac{1}{2} C_{HB} V_{in}^2, \quad (24)$$

which provides:

$$|I_{R0}| \geq \sqrt{\frac{C_{HB}}{L_s}} V_{in}. \quad (25)$$

Therefore, if the current  $I_{R0}$  is sufficiently greater than the critical value given by (25), say, at least 30%, then (23) is sufficiently accurate to assess  $T_T$  and ZVS. Otherwise, the more accurate formulae should be used.

To complete the picture, we need to assess the voltage across the resonant capacitor at the instant of transition,  $V_{C0}$ , which appears in many of the relationships found so far. Its value is related to the operating conditions of the converter.

It is worth noticing that the resonant capacitor voltage  $V_C(t)$  is the integral of the resonant tank current  $I_R(t)$ . Therefore, being  $T_{sw} = 1/f_{sw}$  the period of the square wave  $V_{HB}$ , the change  $\Delta V_C$  in  $V_C(t)$  from the instant 0 when Q2 turns off to the instant  $T_{sw}/2$  when Q1 turns off is given by:

$$\Delta V_C = \frac{1}{Cr} \int_0^{T_{sw}/2} I_R(t) dt. \quad (26)$$

Notice that the integral in (26), neglecting the electric charge exchanged between the input source and  $C_{HB}$ , is the electric charge  $Q_{in}$  that the input source provides to the half bridge in a switching cycle; in a full bridge it is half that value ( $Q_{in}/2$ ). The dc input current to the converter is the per-cycle electric charge  $Q_{in}$  multiplied by the switching frequency  $f_{sw}$ , hence:

$$\Delta V_C = \begin{cases} \frac{Q_{in}}{Cr} = \frac{I_{in}}{Cr f_{sw}} & (\text{HB}) \\ \frac{Q_{in}}{2 Cr} = \frac{I_{in}}{2 Cr f_{sw}} & (\text{FB}) \end{cases}. \quad (27)$$

In the half bridge, where  $V_C(t)$  has a dc value equal to  $V_{in}/2$ , by symmetry the initial value  $V_C(0) = V_{C0}$  and the final value  $V_C(T_{sw}/2)$  must be on opposite sides of  $V_{in}/2$  and equidistant, whereas in the full bridge  $V_C(t)$  is symmetric to zero, then:

$$V_{C0} = \begin{cases} \frac{1}{2} \left( V_{in} - \frac{I_{in}}{Cr f_{sw}} \right) & (\text{HB}) \\ -\frac{I_{in}}{4 Cr f_{sw}} & (\text{FB}) \end{cases}. \quad (28)$$

$$V_C(T_{sw}/2) = \begin{cases} \frac{1}{2} \left( Vin + \frac{I_{in}}{Cr f_{sw}} \right) & (\text{HB}) \\ \frac{I_{in}}{4 Cr f_{sw}} & (\text{FB}) \end{cases} \quad (29)$$

As previously mentioned, in (26) - (29) the contribution of the electric charge exchanged between the input source and  $C_{HB}$ , which is proportional to the  $C_{HB}/Cr$  ratio and the input voltage  $Vin$ , has been neglected. This is acceptable because this contribution is significant at light load, where the switching frequency is close to its upper end, whereas we are interested in calculating  $V_{CO}$  when the switching frequency is close to the lower end, which occurs at heavy load.

The suggested step-by-step procedure to check if the design of an LLC tank achieves ZVS under all operating conditions depends on whether the control implements an adaptive  $T_D$  that tracks  $T_T$  in a certain time interval ( $T_{Dmin}, T_{Dmax}$ ) or a fixed  $T_D$ .

- In case of adaptive  $T_D$ , it is possible to:
  1. Determine  $I_{R0}$  when the converter operates at its maximum frequency and check that the condition  $T_T < T_{Dmax}$  is fulfilled using (23).
  2. Determine  $I_{R0}$  when the converter operates at its minimum frequency, check that it has the right sign and check if the condition  $T_T < T_{Dmax}$  is fulfilled. To calculate  $T_T$ :
    - a. use (23) if  $|I_{R0}|$  is at least 30% larger than the minimum value provided by (25).
    - b. use (10) if  $|I_{R0}|$  is less than 30% larger.
    - c. ZVS is not achieved if  $|I_{R0}|$  is lower than the minimum value provided by (25).
- In case of fixed  $T_D$ , it is possible to:
  1. Determine  $I_{R0}$  when the converter operates at its maximum frequency and check that the condition  $T_T < T_D$  is fulfilled using (23).
  2. Determine  $I_{R0}$  when the converter operates at the minimum switching frequency, check that it has the right sign and check that the sign is maintained until  $T_D$  ends by using (18). To compute (18):
    - a. use (23) to calculate  $T_T$  and consider  $I_R(T_T) = I_{R0}$  if  $|I_{R0}|$  is at least 30% larger than the minimum value provided by (25).
    - b. use (10) to calculate  $T_T$  and (11) to calculate  $I_R(T_T)$  if  $|I_{R0}|$  is less than 30% larger.
    - c. ZVS is not achieved if  $|I_{R0}|$  is lower than the minimum value provided by (25).

Notice that even with an adaptive  $T_D$ , if  $T_T < T_{Dmin}$  the situation is similar to that of a fixed  $T_D$ , and a check that  $T_T + T_{zz} \geq T_{Dmin}$  with the relevant procedure might be necessary.

If  $T_T \ll T_D$  the tank current flows through the body diode (in case of MOSFET switch) or in reverse conduction (in case of GaN HEMT switch) during most of the dead-time: in case of low input voltage there could be a detrimental impact on efficiency, especially with GaN HEMT switches, which have a large voltage drop when reverse conducting, significantly larger than that on MOSFET body diode ( $\approx 3\text{-}4 \text{ V}$  vs.  $\approx 0.7 \text{ V}$ ).

When the ZVS conditions are not met or are met marginally, consider modifying the design of the LLC tank, especially if the tolerance of the components has not been taken into account.

Finally, it is worth reminding that all the derivations related to the switching transients have been developed assuming an instantaneous turn-off of the power switches. If, instead, the fall time of the switch current,  $T_f$ , is known and it is, as it should reasonably be  $T_f < 2T_T$  calculated with either (23) or (10), the actual  $T_T$  can be obtained by adding  $T_f/2$ .

## Chapter 6

### Magnetic integration in the LLC resonant converter

Magnetic integration combines multiple magnetic devices in a single physical device, with the objective of reducing the overall physical size and the parts count, usually with little or no handicap in converter's performance, sometimes even enhancing its operation. The inevitable price to pay for that is a more complex design process, often with several trial-and-error steps.

The LLC resonant converter with its two inductors and transformer is particularly suitable for magnetic integration: they all can be realized in a single magnetic device [20]-[22]. This opportunity becomes apparent by observing the topological similitude between the electrical magnetic structure of the LLC converter and transformer's physical model, whose simplified schematic (without parasitic resistances and capacitances) is shown in figure 30.

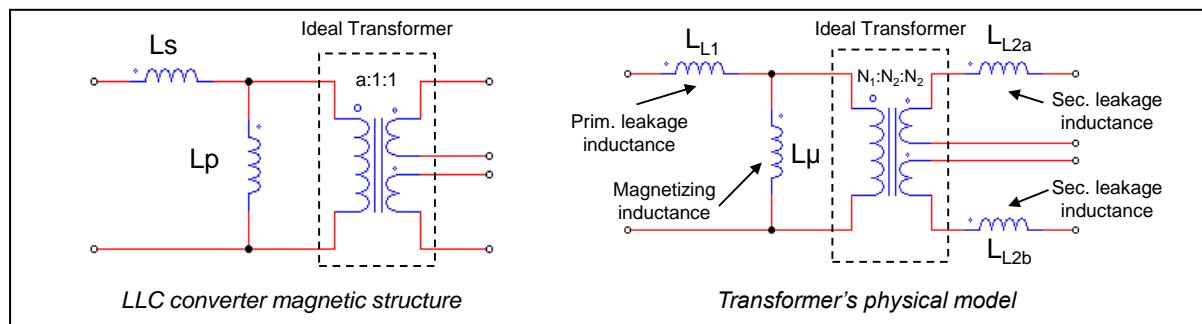
$L_p$  is in the same place as the magnetizing inductance  $L_p$ ,  $L_s$  in the same place as the primary leakage inductance  $L_{L1}$ . Then,  $L_p$  can be realized as the transformer's magnetizing inductance by adding an air gap to the magnetic circuit, and the leakage inductance can be used for  $L_s$ .

In the electrical magnetic structure of an LLC tank,  $L_s$  is a non-negligible fraction of the total primary inductance  $L_s + L_p$  therefore, to make  $L_s$  with the leakage inductance a leaky physical magnetic structure is needed.

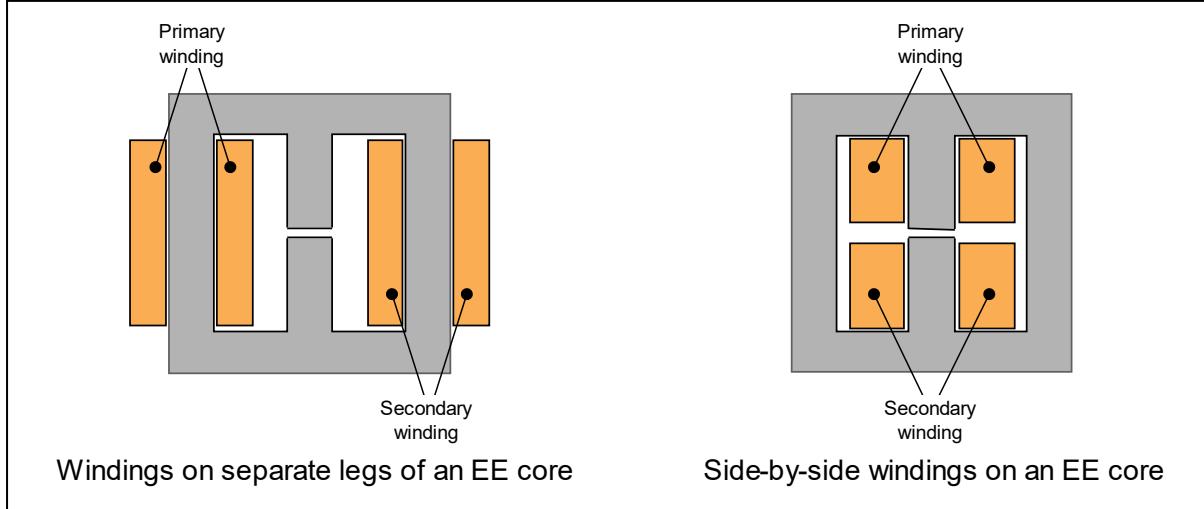
Considering a ferrite core plus bobbin assembly, the most common approach in industry, the usual concentric winding arrangement used in flyback transformers is not recommended. Increasing the space between the windings can provide higher leakage inductance values but the range of  $L_s$  values obtainable in this way is quite narrow. Also, it is difficult to achieve a good reproducibility of the result because it depends on parameters (such as winding surface irregularities or spacer thickness) difficult to control in production. Other winding arrangements are recommended, such as placing the windings on separate core legs or side-by-side on the same leg, as shown in figure 31. Of course, shapes other than EE cores can be used (U cores, other types of E cores, pot cores etc.).

The variety of possible winding arrangements to achieve a well-controlled leakage inductance is much larger, especially in case of planar magnetics. In this context, however, we will stick to the most common approach in industry: since slotted bobbins for side-by-side windings like that shown in figure 32 are readily available in countless shapes and sizes, we will assume that this kind of configuration will be used. Noteworthy, this solution makes it easy to meet safety isolation requirements.

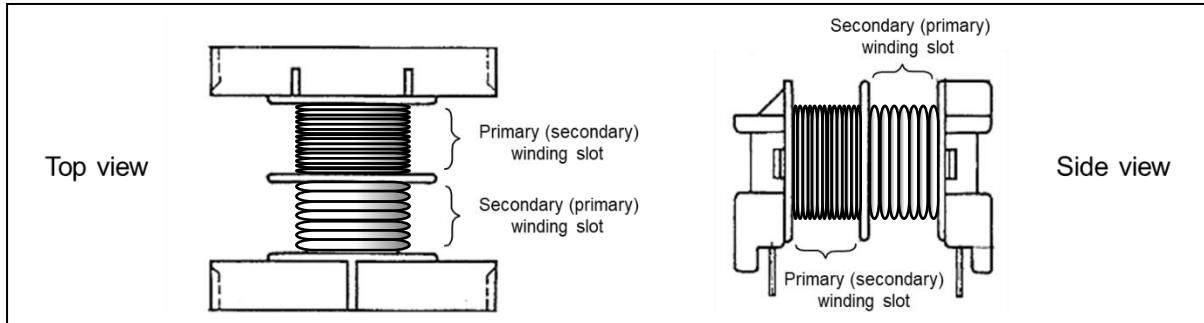
**Figure 30. Comparison of LLC magnetic structure and transformer's model (center-tap).**



**Figure 31. Examples of leaky magnetic structures.**



**Figure 32. Slotted bobbin for EE core and side-by-side windings arrangement.**



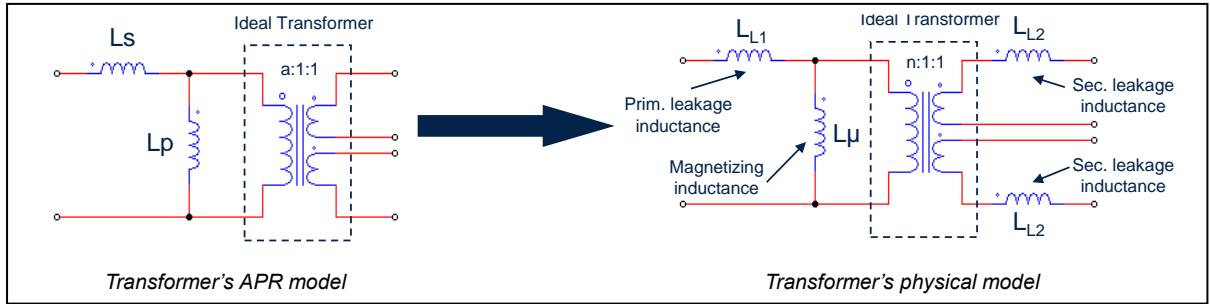
The physical model of figure 30 results from the analysis of the magnetic structure (carried out, for example, with the reluctance model approach):  $n = N_1/N_2$  is the actual primary-to-secondary turns ratio;  $L_\mu$  models the magnetizing flux linking all windings;  $L_{L1}$  models the flux generated by the primary winding and not linked to the secondary windings;  $L_{L2a}$  and  $L_{L2b}$  model the flux generated by the secondary windings and not linked to the primary winding. For simplicity we will assume that the secondary windings are symmetric so that  $L_{L2a} = L_{L2b} = L_{L2}$ .

In the LLC electrical magnetic structure there is no leakage in the secondary windings. This is not a problem from the modeling point of view because the transformer's model can be manipulated so that  $L_{L2}$  disappears. In fact, there are infinite electrically equivalent models of a given transformer (i.e., described by the same equations at the input and output terminals but with different internal parameters) that depend on the choice of the turns ratio of the ideal transformer in the model. With an appropriate choice of this *equivalent turns ratio*  $a$  (obviously different from the physical turns ratio  $n = N_1/N_2$ ) all the elements related to the leakage flux can be relocated on the primary side. This is the APR (All-Primary-Referred) model, which is the same as the electrical magnetic structure of the LLC converter in figure 30. It is possible to show that the APR model is obtained with the following choice of  $a$ :

$$a = k_c \sqrt{\frac{L_1}{L_2}}, \quad (30)$$

with  $k_c$  transformer's coupling coefficient,  $L_1$  inductance of the primary winding and  $L_2$  inductance of each secondary winding (assumed to be equal).

**Figure 33. Design strategy of integrated magnetics in LLC converters.**



Then, it is important to highlight that  $L_s$  and  $L_p$  are not real physical inductances ( $L_{L1}$ ,  $L_\mu$  and  $L_{L2}$  are) and their numerical values are different ( $L_s \neq L_{L1}$ ,  $L_p \neq L_\mu$ ), like the turns ratios  $a$  and  $n = N_1/N_2$ .  $L_s$  and  $L_p$ , however, can be given a physical interpretation, which means that their value can be measured on a physical sample.

Since the equation terminals must be the same for the physical model and the APR model, the primary inductance  $L_1$ , which is measurable keeping the secondaries open, must be unchanged and the following equality holds:

$$L_1 = L_s + L_p = L_{L1} + L_\mu . \quad (31)$$

Additionally, from the APR model it is apparent that shorting the secondaries,  $L_s$  can be measured directly.  $L_p$  can then be derived as the difference between  $L_1$  and  $L_s$ .

Therefore, as sketched in figure 33, the design of the LLC tank with magnetic integration can be carried out based on APR model and then, the parameters of the APR model ( $a$ ,  $L_s$ ,  $L_p$ ) will be translated into those of the physical model for the specifications to be given to the transformer manufacturer.

The problem is mathematically undetermined: there are 4 unknowns in the physical model ( $L_{L1}$ ,  $L_\mu$ ,  $n$ , and  $L_{L2}$ ) and only three parameters in the APR model.

Again, we need a simplifying assumption to overcome this issue: it is that of magnetic circuit symmetry, that is, the flux linkage is assumed to be the same for both the primary and the secondary winding(s). This provides the missing condition:  $L_{L2} = L_{L1}/n^2$ . In the end:

$$n = a \sqrt{1 + \frac{L_s}{L_p}}; \quad L_\mu = \sqrt{L_p L_1}; \quad L_{L1} = L_1 - L_\mu; \quad L_{L2} = \frac{L_{L1}}{n^2} . \quad (32)$$

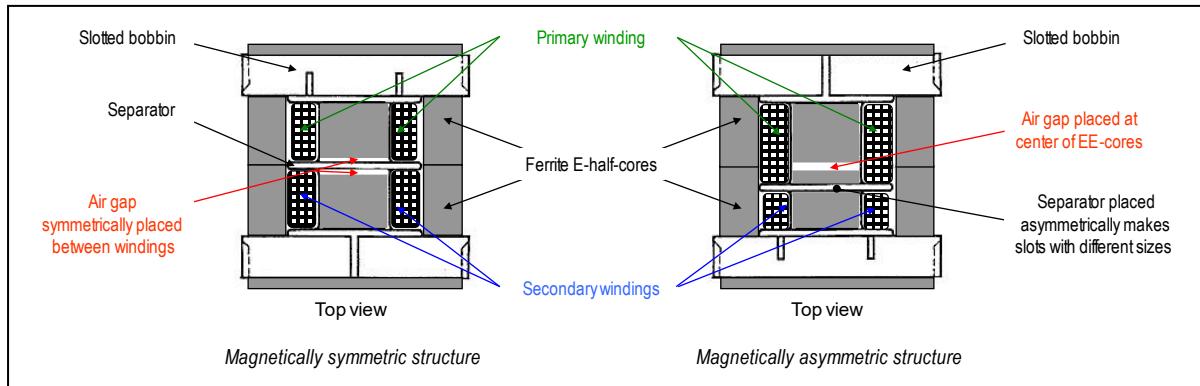
Being the transformer model defined, the next step is to pass from the parameters of the model to those of the transformer construction: number of primary turns  $N_1$ , number of secondary turns  $N_2$  and air gap thickness  $l_G$ . Once the ferrite core and bobbin are chosen, these three parameters are those to be managed to get the desired integrated transformer.

A detailed discussion of this step is beyond the scope of the present work, and we refer to [22] for that; here we just present the basic concepts, some more details are given in Part IV, chapter 9.

With reference to the leaky magnetic structures of figure 31, if the position of the air gap is symmetric between the windings the assumption of magnetic circuit symmetry that has led to the relationships (30) is not that far from reality. Otherwise (30) are not applicable.

In case of symmetric position of the air gap, like in any ferrite core plus bobbin assembly it is possible to define a specific inductance factor  $A_L$  (which depends on air gap thickness) such that  $L_1 = N_1^2 \cdot A_L$ . It is also possible to define a specific leakage inductance factor  $A_{LIK}$  such that  $L_{L1} = N_1^2 \cdot A_{LIK}$ .  $A_{LIK}$  is a function of bobbin's geometry, independent of the air gap thickness.

**Figure 34. Magnetically symmetric and asymmetric high-leakage magnetic structures.**



The main issue with this symmetric arrangement is that there is a considerable stray flux that scatters around the air gap and that adds up to the leakage flux between the windings; both concur to generate significant proximity losses in the facing wires of the windings and radiated EMI. A thicker separator between the slots eases isolation and increases  $A_{Llk}$  but also exacerbates these issues.

The position of the air gap may not be symmetrically located between the primary and secondary windings, as shown in the magnetically asymmetric structure of figure 34; in many practical cases it is placed below the primary winding, which reduces the stray flux and the radiated EMI. The air gap position affects both  $L_p$  and  $L_{L1}$  (then the resulting  $L_p$  and  $L_s$  too) and  $L_{L2}$ , then how leakage inductance is apportioned between primary and secondary side.

In the end, the optimal air gap position is a trade-off between eddy current loss in wires near the gap, generation of magnetizing energy ( $L_p$ ) and secondary rectifier reverse voltage extra stress due to  $L_{L2}$ . In case of magnetic asymmetric structure, the specific inductance factor  $A_L$  and specific leakage inductance factor  $A_{Llk}$  are different for the primary and the secondary side and need to be derived by characterization.

**Table 2. Magnetic integration vs. discrete magnetics in LLC converters: summary of pros and cons.**

INTEGRATED MAGNETICS	DISCRETE MAGNETICS
<p>Benefits:</p> <ul style="list-style-type: none"> <li>• Low-cost (single magnetic device)</li> <li>• Smaller footprint</li> <li>• Easy primary-to-secondary isolation</li> <li>• Lower core losses, higher light load efficiency</li> </ul>	<p>Benefits:</p> <ul style="list-style-type: none"> <li>• Conventional magnetic design</li> <li>• Lower radiated EMI</li> <li>• Lower ac resistance and conduction losses</li> <li>• Greater design flexibility (any <math>L_s</math>, <math>L_p</math> combination achievable)</li> </ul>
<p>Drawbacks:</p> <ul style="list-style-type: none"> <li>• Limited range of <math>L_s</math> achievable</li> <li>• Fringing flux causes proximity effect in windings and higher radiated EMI</li> <li>• More complex magnetic design</li> <li>• Higher reverse voltage across secondary rectifiers due to leakage</li> </ul>	<p>Drawbacks:</p> <ul style="list-style-type: none"> <li>• More complex primary-to-secondary isolation</li> <li>• Higher component count, larger footprint</li> <li>• Parasitic capacitance of inductor may create additional ringing</li> </ul>

Magnetic integration is a very convenient technique to minimize the size and the parts count of an LLC converter but has its own limitations and is not the only possible option for a power designer. Of course, it is also possible to follow a “discrete” approach, using separate physical magnetic devices to build the series inductor  $L_s$  and the set  $L_p + \text{transformer}$  (it makes little sense to keep  $L_p$  too as a separate physical device). Table 2 summarizes pros and cons of the two approaches.

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# PART III

## LLC CONVERTER OPERATION

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### Chapter 1

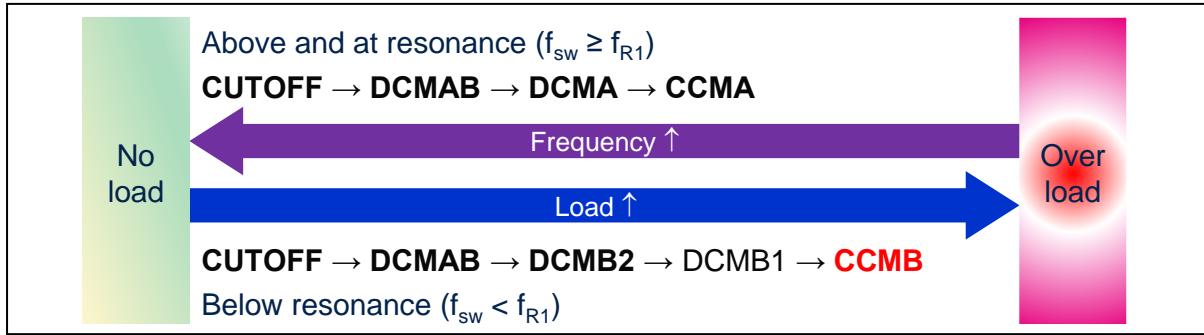
#### Fundamental steady-state operating modes

Due to its multi-resonant nature, the LLC resonant converter features a considerable number of different operating modes. In fact, the presence of two resonance frequencies associated to the conductive or nonconductive status of the secondary rectifiers originates different combinations of time intervals in which the secondary rectifiers are conductive with time intervals in which they are not. These time intervals may alternate in different ways in a switching cycle, producing a variety of CCM and DCM modes that depend on the input-to-output voltage ratio, the output load and the characteristics of the tank circuit

Not all of these CCM and DCM modes can be seen in a given converter; some are not even recommended, like those associated to capacitive mode operation. In the following we will consider the fundamental steady-state operating modes illustrated in figure 35 and use the nomenclature defined in [14]:

1. Operation at resonance, when the converter works exactly at  $f_{sw} = f_{R1}$ ;
2. Above-resonance (or superresonant) operation, when the converter works at a frequency  $f_{sw} > f_{R1}$ ; moving along the frequency arrow:
  - 2a) CCMA operation at heavy load;
  - 2b) DCMA operation at medium load;
  - 2c) DCMAB operation at light load;
3. Below-resonance (or subresonant) operation, when the converter works at a frequency  $f_{CM} < f_{sw} < f_{R1}$ ; following the load arrow, we will consider two sub-modes:
  - 3a) DCMAB operation at medium-light load;
  - 3b) DCMB2 operation at heavy load;
- DCMB1 occurs just before CCMB, where ZVS is likely to be lost already. It does not significantly differ from DCMB2 and will not be considered.
4. Below-resonance operation, when the converter works at a frequency  $f_{R2} < f_{sw} < f_{CM}$  corresponding to the CCMB operating mode.
5. No-load operation (CUTOFF), both above and below resonance

**Figure 35. LLC Resonant converter fundamental steady-state operating modes.**



Notice that, unlike PWM converters where DCM operation is invariably associated to light load operation and CCM to heavy load operation, in the LLC resonant converter this connection holds only when operating above the upper resonance frequency  $f_{R1}$ , DCM operation occurs also at heavy load below  $f_{R1}$ .

The discussion will start from the inspection of the main waveforms in a switching cycle, highlighting each subinterval where the circuit assumes a topological state and deducing the properties of the converter when operated in that mode from those waveforms. The half bridge leg transitions are considered instantaneous, their features have been discussed already.

The waveforms shown in the time diagrams that follow refer to the half bridge in figure 8 with center-tap full-wave rectification; it is understood that what will be said about the semiconductor switches can be simply extended to the full bridge version and the single-ended output bridge configuration. What is said about the switch Q1 in the half bridge applies to the Q1-Q4 diagonal in the full bridge; similarly, what is said about the switch Q2 of the half bridge applies to the Q2-Q3 diagonal of the full bridge. On the secondary side, what is said about D1 in the center-tap full wave rectification applies to the leg D1-D4 in the single-ended bridge rectification and D2 corresponds to D2-D4.

A final note on notation: in this context the  $I_R(t)$  and  $I_M(t)$  will be simply indicated with  $I_R$  and  $I_M$ , the dependence on time is implicit.

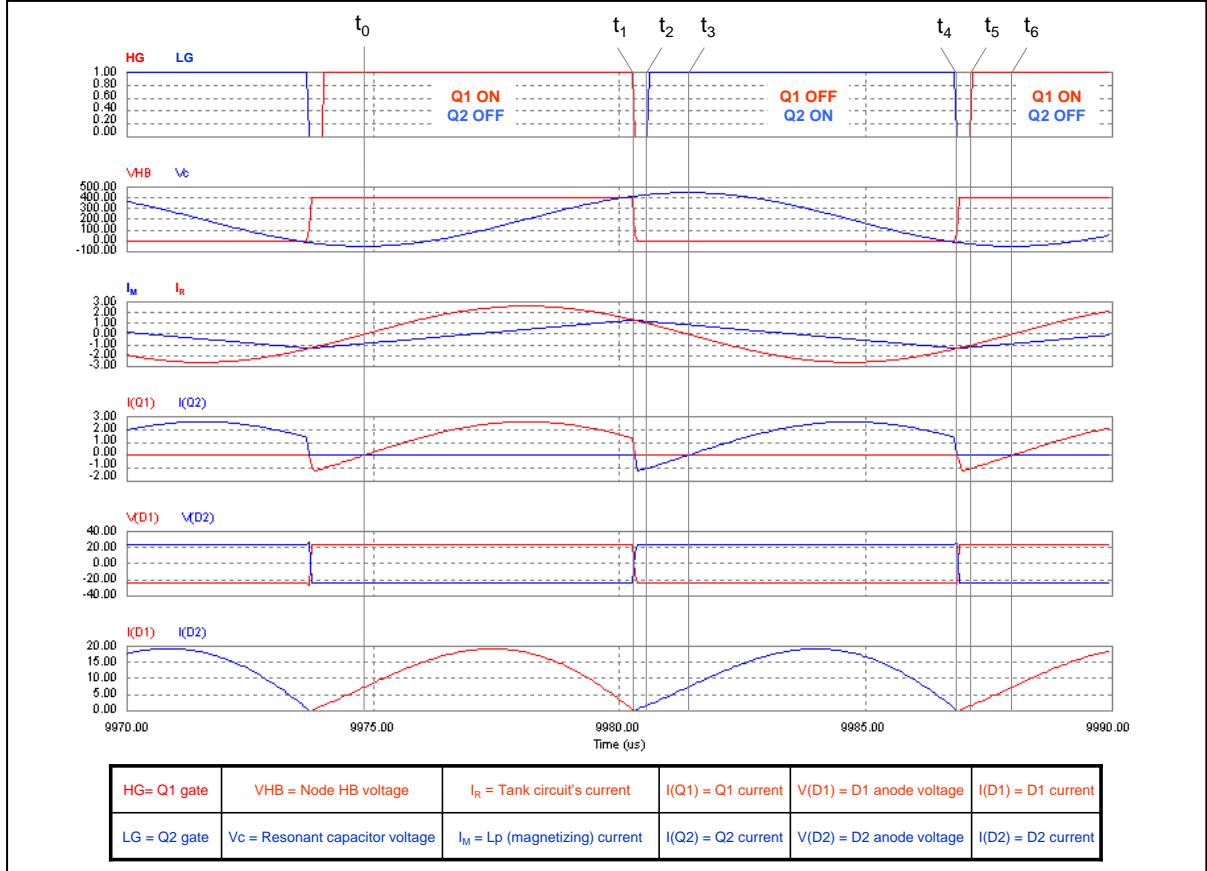
#### *Operation at resonance ( $f_{sw} = f_{R1}$ ).*

In this operating mode it is possible to distinguish six fundamental time sub-intervals within a switching cycle, as illustrated in figure 36. Figure 37 shows the relevant sequence of topological states.

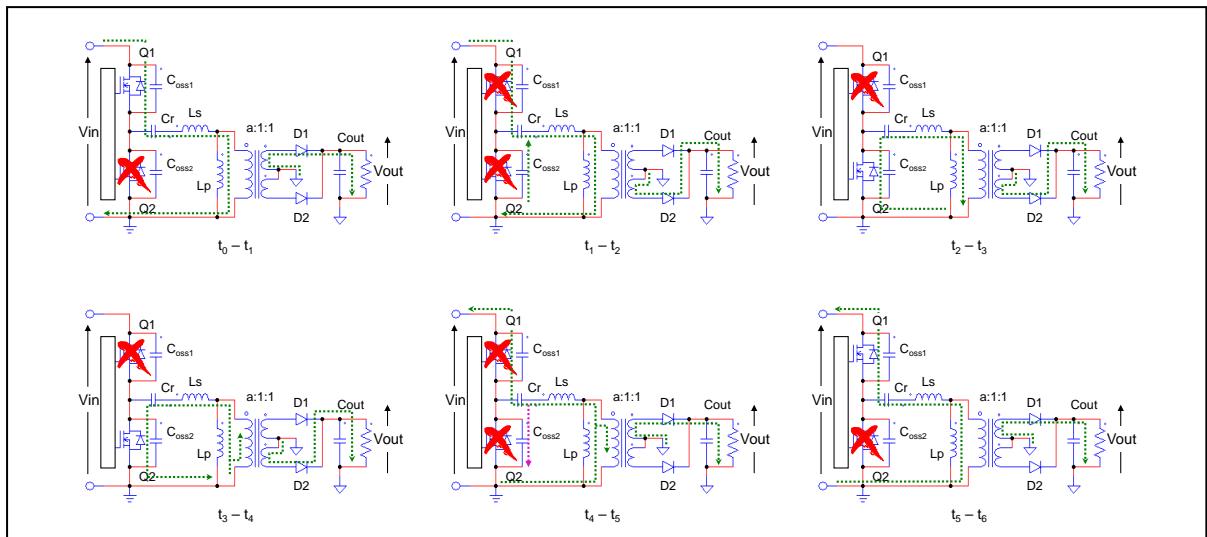
The instant  $t_0$  and then the first sub-interval can be chosen arbitrarily; we fix  $t_0$  as the instant when, with Q1 conducting and Q2 open, the tank current  $I_R$  has a positive-going zero-crossing.

- $t_0 \rightarrow t_1$ . Q1 is ON and Q2 is OFF; in the half bridge this is the sole “energy delivery” phase (the first of two in the full bridge), the time interval when energy is delivered by the input source:  $V_{HB}$  is positive, current flows from the input source to the tank circuit, so that it both refills the resonant tank and supplies the load; the operating point of Q1 is in the first quadrant (current is flowing from drain to source); D2 is reverse-biased while D1 is conducting, so  $L_p$  is shorted by the output load reflected back to the primary side and the voltage across it is fixed at  $a(V_{out} + V_{Rect})$ ;  $L_p$ , then, is not participating in resonance and  $C_r$  is resonating with  $L_s$  only;  $I_R$  is a portion of a sinusoid with a frequency  $f = f_{R1}$ ; during this phase  $I_R$  rises, peaks and starts decaying; this phase ends when Q1 is switched off at  $t = t_1$ ; note that at  $t = t_1$   $I_R = I_M$  and then  $I(D1) = 0$ .

**Figure 36. Operation at resonance ( $f_{sw} = f_{R1}$ ): main waveforms.**

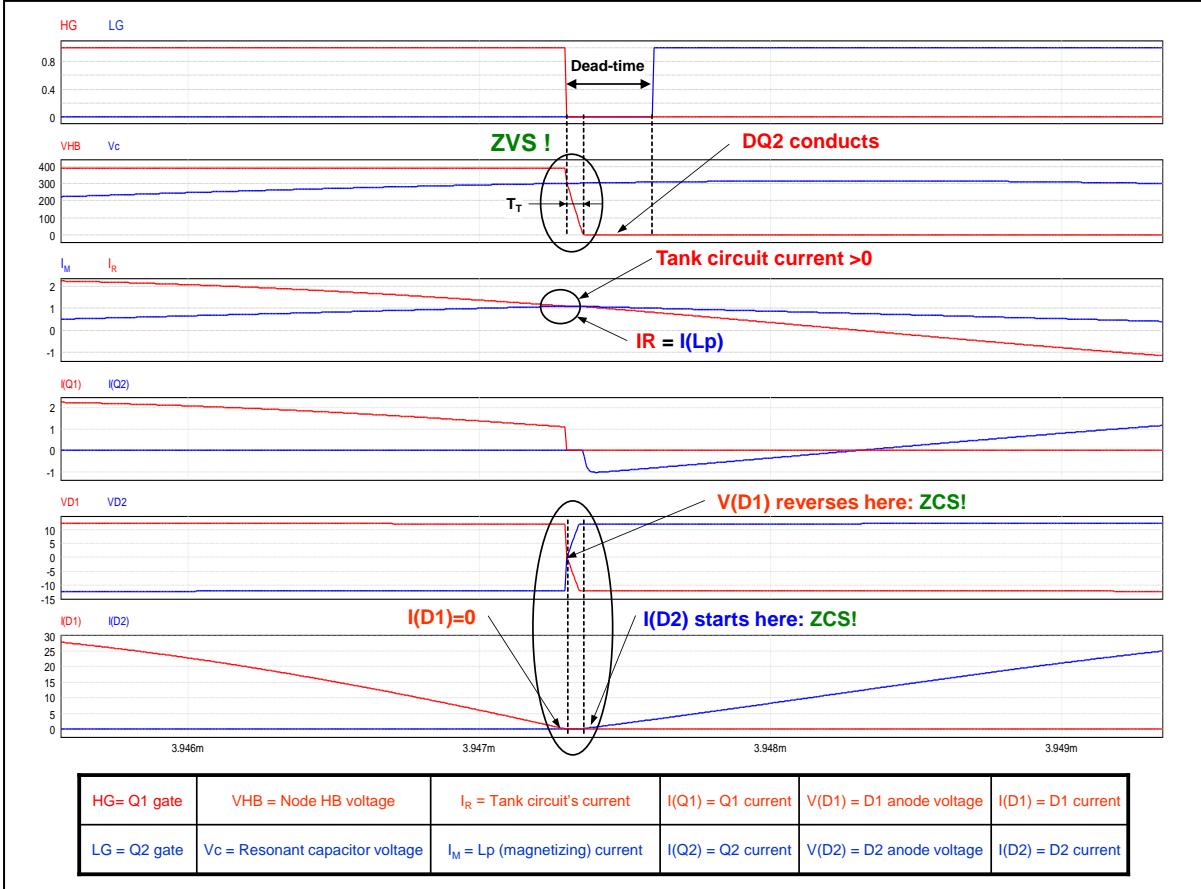


**Figure 37. Operation at resonance ( $f_{sw} = f_{R1}$ ): topological states.**



- b)  $t_1 \rightarrow t_2$ . This is the dead-time during which both Q1 and Q2 are OFF; at  $t = t_1$  the current  $I(Q1) = I_M = I_R$  is greater than zero and provides the energy to let the node HB swing from  $V_{in}$  to 0 at  $t = t_1 + T_T$ ; during this interval current flow through the  $C_{oss}$  of Q1 and Q2; at  $t = t_1 + T_T$  the body diode of Q2, DQ2, is injected; this allows  $I_R$  to flow; the voltage across  $L_p$  reverses to  $-a \cdot (V_{out} + V_{Rect})$  and the slope of its current changes sign; D2 starts conducting while D1 is reverse biased; this phase ends when Q2 is switched on at  $t = t_2$ . This interval is shown in detail in figure 38.

**Figure 38. Operation at resonance ( $f_{sw} = f_{R1}$ ): switching details in  $(t_1, t_2)$ .**



- c)  $t_2 \rightarrow t_3$ . Q1 is OFF and Q2 is ON; at  $t = t_2$   $I_R$  is diverted from DQ2 to the  $R_{DS(on)}$  of Q2, then no significant energy is lost during the turn-on transient (ZVS); note that now the operating point of Q2 is in the third quadrant, current is flowing from the source to drain; D2 keeps on conducting and the voltage across  $L_p$  is  $-a \cdot (V_{out} + V_{Rect})$ , so that  $L_p$  is not participating in resonance and  $C_r$  is resonating with  $L_s$  only;  $I_R$  is a portion of a sinusoid having a frequency  $f = f_{R1}$ ; this phase ends when  $I_R = 0$  at  $t = t_3$ .
- d)  $t_3 \rightarrow t_4$ . Q1 is OFF and Q2 is ON; in the half bridge this is the recirculation phase (the second energy delivery phase in the full bridge), specular to phase a); tank circuit current, which is zero at  $t = t_3$  becomes negative; D1 is non-conducting;  $L_p$ 's current has a negative slope, so the voltage across  $L_p$  must be negative; since the diode D2 is conducting, this voltage will be equal to  $-a \cdot (V_{out} + V_{Rect})$ ;  $L_p$ , then, is not participating in resonance,  $C_r$  is resonating with  $L_s$  only and  $I_R$  is a portion of a sinusoid having a frequency  $f = f_{R1}$ ; during this phase, which ends when Q2 is switched off at  $t = t_4$ ,  $I_R$  reaches its minimum value, after that it starts increasing; note that at  $t = t_4$   $I_R = I_M$  and then  $I(D2) = 0$ .
- e)  $t_4 \rightarrow t_5$ . This is the dead-time during which both Q1 and Q2 are OFF; at  $t = t_4$  the current  $I(Q2) = -I_M = -I_R$  is greater than zero and provides the energy to let the node HB swing from 0 to  $V_{in}$  at  $t = t_4 + T_T$ ; during this interval current flow through the  $C_{oss}$  of Q1 and Q2; at  $t = t_4 + T_T$  the body diode of Q1, DQ1, is injected; this allows  $I_R$  to flow back to the input source; the voltage across  $L_p$  reverses to  $a \cdot (V_{out} + V_{Rect})$  and its current slope changes sign; D1 starts conducting while D2 is reverse biased; this phase, which is specular to phase b), ends when Q1 is switched on at  $t = t_5$ .

- f)  $t_5 \rightarrow t_6$ . Q1 is ON and Q2 is OFF; at  $t = t_5$   $I_R$  is diverted from DQ1 to the  $R_{DS(on)}$  of Q1, so that no significant energy is lost during the turn-on transient (ZVS); note that now the operating point of Q1 is in the third quadrant, current is flowing from the source to drain; in this phase, specular to phase c), the tank current is negative (coming out of the input terminal) despite the impressed voltage  $V_{HB}$  is positive so that the input energy is negative, i.e., it is returned to the input source; D1 keeps on conducting and the voltage across  $L_p$  is  $a \cdot (V_{out} + V_{Rect})$ , so that  $L_p$  is not participating in resonance and  $C_r$  is resonating with  $L_s$  only;  $I_R$  is a portion of a sinusoid with a frequency  $f = f_{R1}$ ; this phase ends when  $I_R = 0$  at  $t = t_6$  and another switching cycle starts.

#### Remarks

1. The parallel inductor  $L_p$  never resonates, and its current is essentially triangular. The LLC converter, then, can be regarded as a series LC resonant half-bridge (composed by  $L_s$  and  $C_r$ ) that supplies a reactive RL load (composed by  $L_p$  and the equivalent resistor loading the converter). This standpoint provides considerable insight into the operation of the converter, as shown in some of the following remarks.
2. In a resistively loaded series LC tank operating at resonance the impressed voltage  $V_{HB}$  and the tank current are exactly in phase, hence the switched current is zero and, thereby, ZVS cannot be achieved; the effect of adding an inductor ( $L_p$ ) in parallel to the resistive load is to provide the tank current with the phase shift (lagging) necessary to switch a current greater than zero, so that ZVS becomes now possible at resonance.
3. As shown in the diagrams of figure 36, the tank circuit current is a sinusoid with a frequency  $f = f_{R1}$  the lags the impressed voltage by an angle  $\varphi$  equal to:

$$\varphi = 2\pi \frac{t_6 - t_4}{t_6 - t_0} = 2\pi \frac{t_3 - t_1}{t_6 - t_0}. \quad (33)$$

so that they have the same sign at half-bridge leg transitions; furthermore, the switched currents  $I_R(t_1)$  and  $I_R(t_4)$  (corresponding to the current  $I_{R0}$  discussed in the previous sections) are large enough to complete the HB node swing well within the dead-times ( $t_1, t_2$ ) and ( $t_4, t_5$ ) respectively.

It is not difficult to recognize that the angle  $\varphi$  is the phase of the input impedance of the loaded resonant tank evaluated at  $f = f_{R1}$ ; additionally, since the impedance of a series LC tank at resonance is zero, in this condition the input impedance of the LLC resonant tank equals the impedance of the parallel RL load.

4. In a series LC tank operating at resonance the voltage drop across L is always equal in module and opposite in sign to the drop across C (this is why its impedance is zero). In our specific case the drop across the series  $L_s-C_r$  will be zero, so that it is possible to write the following voltage balance equations:

$$\begin{aligned} Vin - Vin/2 &= a \cdot (V_{out} + V_{Rect}) && \text{Q1 ON, Q2 OFF} \\ -Vin/2 &= -a \cdot (V_{out} + V_{Rect}) && \text{Q1 OFF, Q2 ON} \end{aligned} \quad (34)$$

for the half bridge and:

$$\begin{aligned} Vin &= a \cdot (V_{out} + V_{Rect}) && \text{Q1-Q4 ON, Q3-Q2 OFF} \\ -Vin &= -a \cdot (V_{out} + V_{Rect}) && \text{Q1-Q4 OFF, Q3-Q2 ON} \end{aligned} \quad (35)$$

for the full bridge. Both of (34) result in:

$$Vin = 2a \cdot (V_{out} + V_{Rect}) \quad (36)$$

for the half bridge, while both of (35) provide:

$$Vin = a \cdot (V_{out} + V_{Rect}). \quad (37)$$

This is a fundamental property of the LLC resonant half-bridge: operating at  $f = f_{R1}$  implies that input and output voltages fulfill (36) or (37) and, vice versa, if input and output voltages meet the condition (36) or (37) the converter is operating at  $f = f_{R1}$ .

Then, whether the LLC converter operates at resonance or not, for a given output voltage  $V_{out}$  and a given turn ratio  $a$ , depends on the input voltage only, not on the load and on the parameters of the tank. From the design point of view, since  $V_{in}$  and  $V_{out}$  are specified, one can decide the input voltage where to operate at resonance by choosing the turns ratio  $a$ .

Condition (36) is considered the 1:1 conversion ratio for the LLC resonant half bridge, (37) is that for the full bridge.

5. The logical consequence of LLC converter's ability to operate at resonance independently of the output load is that the LLC resonant half-bridge can deliver any power if operated at resonance.

This can be seen also in another way: being zero the impedance of the series  $Ls-Cr$ , the RL load "sees" the impressed voltage directly or, in other words, it is supplied by an ideal voltage source. This is a "singularity" in LLC converter's operation, referred to as the *load-independent* point, where the usual energy vs. frequency relationship does not hold. Actually, the inevitable voltage drops across the resistive elements of the real-world circuit (such as MOSFETs'  $R_{DS(on)}$ , winding resistance, secondary rectifier's dynamic resistance or  $R_{DS(on)}$ , etc.) cause a slight dependence of the frequency on the load.

Note that this is a situation comparable to that of CCM-operated PWM converters, where the duty cycle is ideally independent of the load, in reality slightly dependent because of losses.

6. In the half bridge energy is taken from the input source only during phase a) from  $t_0$  to  $t_1$ , then for less than half the switching period, while from  $t_1$  to  $t_4$  energy recirculates internally to allow energy flow into the load while Q1 is not conducting. This low "duty cycle" of the positive input current is a limiting factor in terms of power handling capability, especially if the input voltage is low. This consideration suggests the use of the half bridge topology in high input voltage applications (e.g., with a PFC front-end, which provides a 400V input rail). In the full bridge topology, phase d) from  $t_3$  to  $t_4$  becomes an energy delivery phase as well, then the duty cycle of the positive input current is larger, and the power handling capability is essentially doubled.
7. The lagging phase-shift  $\varphi$  of the tank circuit originates the energy return phases from  $t_4$  to  $t_6$  in the half bridge and from  $t_1$  to  $t_3$  and  $t_4$  to  $t_6$  in the full bridge; during these intervals energy flow is negative (impressed voltage and input current have opposite signs), so this energy subtracts to that drawn from the input during phase a) (and d) in the full bridge) and reduces the net energy flow from the input source to the load each cycle. This energy can be regarded as reactive energy and  $\cos \varphi$  as the input power factor. Making  $\varphi$  as small as possible (i.e., increasing  $Lp$ ) would shorten the duration of the external energy recirculation phase and reduce the amount of reactive energy, thus improving the energy transfer process. This, however, would also reduce  $I_R(t_1)$  and  $I_R(t_4)$ , hence  $\varphi$  can be reduced as long as the switched currents are large enough to ensure ZVS.
8. Recalling that the current switched at turn-off by Q1,  $I_R(t_1)$  and by Q2,  $I_R(t_4)$ , determine their switching losses, it is obvious that keeping  $\varphi$  to the minimum value that ensures

ZVS of Q1 and Q2 provides an optimum design. Of course, component tolerance and abnormal operating conditions must be adequately accounted for, thus  $\varphi$  must be larger than the minimum required, and the typical operation will be sub-optimal.

- The secondary rectifiers D1 and D2 start conducting as Q2 and Q1 turn off respectively. D1 and D2 cease to conduct exactly when Q1 and Q2 turn off, respectively. These are also the moments when the voltages across D1 and D2 reverse. As a result, neither D1 nor D2 experience a voltage reversal while conducting a forward current; reverse recovery, with all its adverse effects, does not occur (ZCS). Note that, in this respect, this is a situation identical to that of a PWM converter operating on the boundary between CCM and DCM.

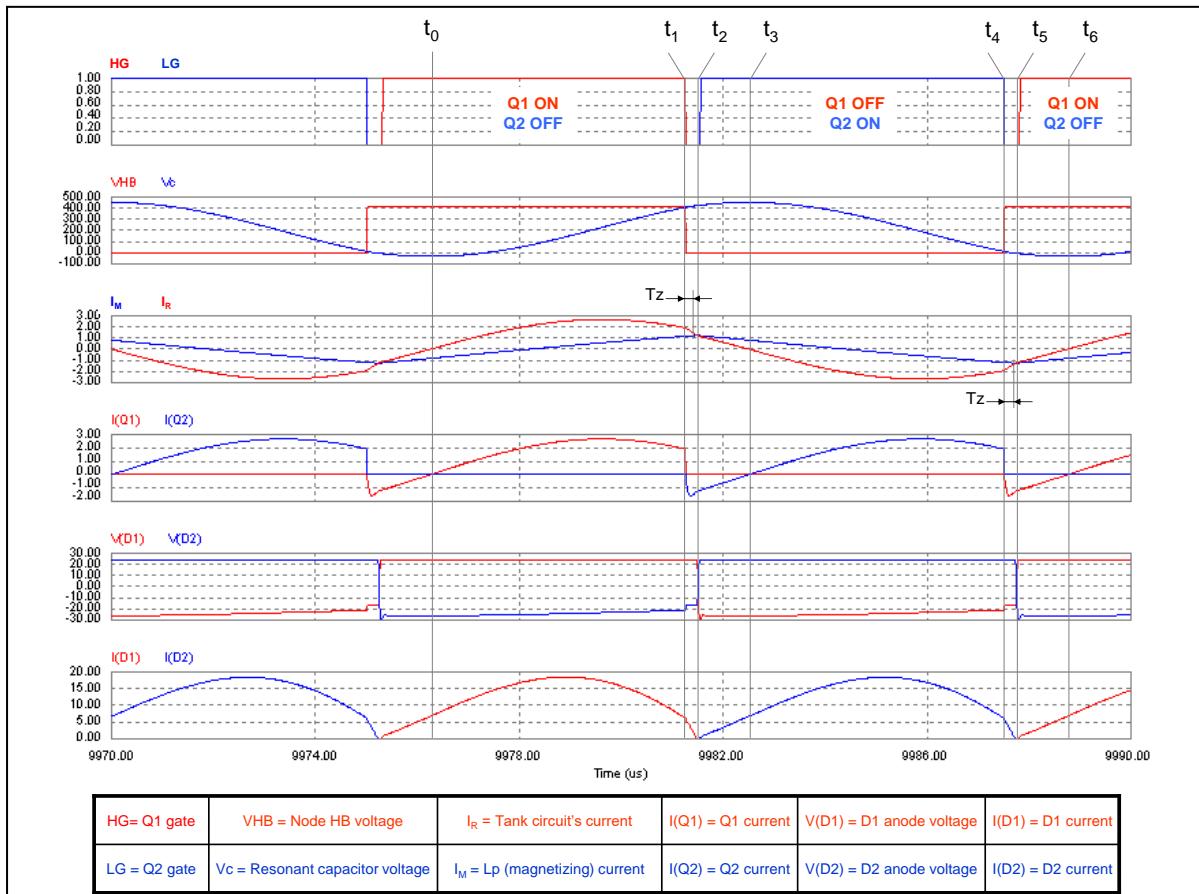
*Operation above resonance ( $f_{sw} > f_{R1}$ ).*

In this operating mode the converter exhibits its usual frequency vs. load characteristic. We will consider three sub-modes where, in a closed-loop regulated system, CCM operation progressively turns into DCM operation as the output load is reduced and frequency is moved away from resonance.

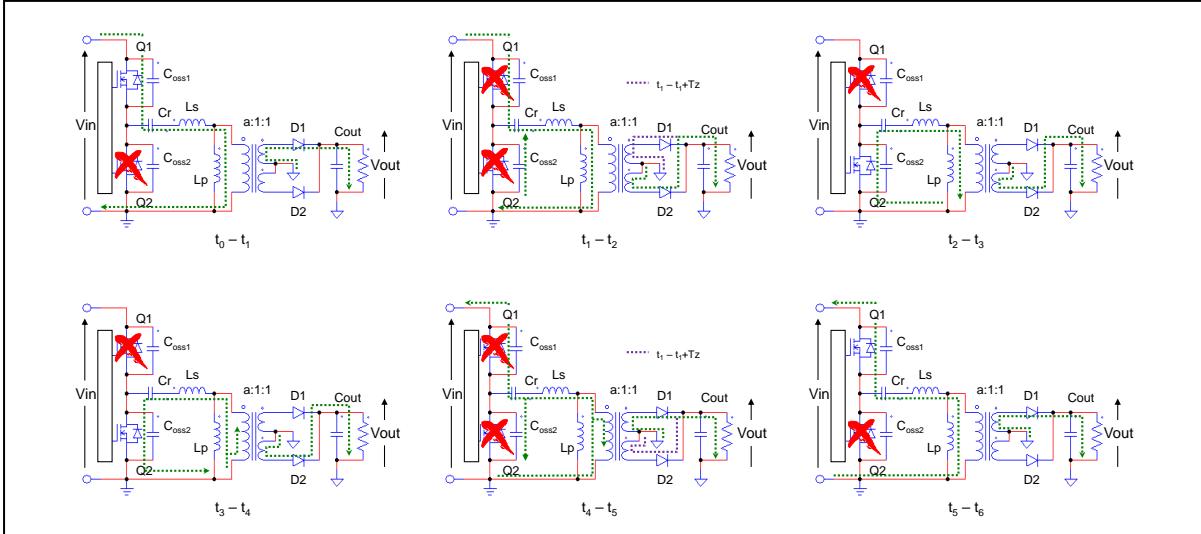
#### A. CCMA operation at heavy load.

In this case it is possible to identify six fundamentals sub-intervals as well; the relevant waveforms and sequence of topological states are illustrated in the timing diagram of figure 39 and in figure 40 respectively. Again,  $t_0$  is the instant when, with Q1 conducting and Q2 open,  $I_R$  has a positive-going zero-crossing.

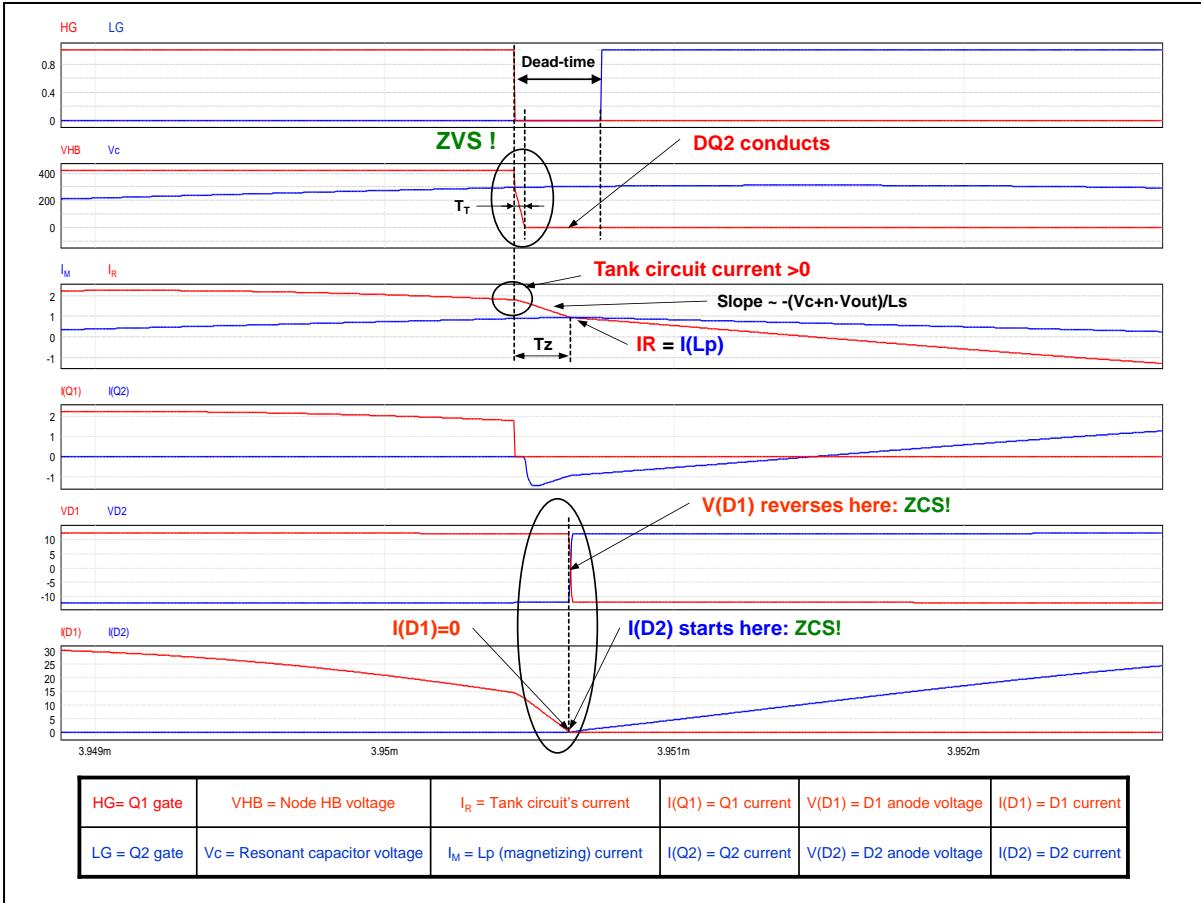
**Figure 39. Operation above resonance ( $f_{sw} > f_{R1}$ ): main waveforms in CCMA mode at heavy load.**



**Figure 40. CCMA mode above resonance ( $f_{sw} > f_{R1}$ ): topological states.**



**Figure 41. CCMA mode above resonance ( $f_{sw} > f_{R1}$ ): switching details in ( $t_1, t_2$ ).**



- $t_0 \rightarrow t_1$ . Q1 is ON and Q2 is OFF; this is an energy delivery phase identical to the corresponding phase seen in the operation at resonance, with the only difference that at the end of this phase, at  $t = t_1$ , it is still  $I_R > I_M$  and then  $I(D1) > 0$ .
- $t_1 \rightarrow t_2$ . This is the dead-time during which both Q1 and Q2 are OFF; at  $t = t_1$  the current  $I_R$  is greater than zero and provides the energy to let the node HB swing from  $V_{in}$  to 0 at  $t = t_1 + T_T$ ; during this interval current flow through the  $C_{oss}$  of Q1 and Q2; at  $t = t_1 + T_T$

the body diode of Q2, DQ2, is injected; this allows  $I_R$  to flow;  $I_R$  slope changes to a higher negative value, so that it quickly approaches  $I_M$ , which is still increasing with the same slope; the same change of slope concerns  $I(D1)$ , which falls quickly to zero until  $I_R$  equals  $I_M$  at  $t = t_1 + T_Z$ , after that D1 is reverse biased, the slope of  $I_M$  changes sign and D2 starts conducting; this phase ends when Q2 is switched on at  $t = t_2$ . Note that during  $T_Z$   $I_R$  is still a portion of a sinusoid at  $f = f_{R1}$  because it is still  $I_R > I_M$ . This interval is shown in detail in figure 41.

- c)  $t_2 \rightarrow t_3$ . Q1 is OFF and Q2 is ON; at  $t = t_2$   $I_R$  is diverted from DQ2 to the  $R_{DS(on)}$  of Q2, so that no significant energy is lost during the turn-on transient (ZVS); this phase, which ends when  $I_R = 0$  at  $t = t_3$ , is identical to the  $(t_2, t_3)$  phase of the operation at resonance.
- d)  $t_3 \rightarrow t_4$ . Q1 is OFF and Q2 is ON; it is specular to phase a) and identical to the phase  $(t_3, t_4)$  seen in the operation at resonance (recirculation phase of the half bridge, second energy delivery phase for the full bridge) with the only difference that at the end of this phase, at  $t = t_4$ , it is still  $I_R < I_M$  and then  $I(D2) > 0$ .
- e)  $t_4 \rightarrow t_5$ . This is the dead-time during which both Q1 and Q2 are OFF; at  $t = t_4$  the current  $I(Q2) = -I_R$  is greater than zero and provides the energy to let the node HB swing from 0 to  $V_{in}$  at  $t = t_4 + T_T$ ; during this interval current flow through the  $C_{oss}$  of Q1 and Q2; at  $t = t_4 + T_T$  the body diode of Q1, DQ1, is injected; this allows  $I_R$  to flow back to the input source;  $I_R$  changes to a higher slope, so that it quickly approaches  $I_M$ , which is still decreasing with the same slope; D2 conducts until  $I_R$  equals  $I_M$  at  $t = t_4 + T_Z$ , after that it becomes reverse biased,  $I_M$  slope changes sign and D1 starts conducting; this phase, specular to phase b), ends when Q1 is switched on at  $t = t_5$ .
- f)  $t_5 \rightarrow t_6$ . Q1 is ON and Q2 is OFF; at  $t = t_5$   $I_R$  is diverted from DQ1 to the  $R_{DS(on)}$  of Q1, so that no significant energy is lost during the turn-on transient (ZVS); this phase, which ends when  $I_R = 0$  at  $t = t_6$ , is specular to phase c) and identical to the  $(t_5, t_6)$  phase of the operation at resonance.

### Remarks

1. In this “above-resonance” CCM sub-mode the parallel inductor  $L_p$  never resonates, and the LLC converter can be regarded as a series LC resonant half-bridge supplying a reactive RL load, like in the operation at resonance.
2. As shown in the diagrams of figure 39, the tank circuit current lags the impressed voltage by an angle  $\varphi$  equal to:

$$\varphi = 2\pi \frac{t_6 - t_4}{t_6 - t_0} = 2\pi \frac{t_3 - t_1}{t_6 - t_0}. \quad (38)$$

so that they have the same sign at half-bridge leg transitions; furthermore, the switched currents  $I_R(t_1)$  and  $I_R(t_4)$  are large enough to complete the HB node swing well within the dead-times  $(t_1, t_2)$  and  $(t_4, t_5)$  respectively.

3. The voltage drop across the series  $L_s$ - $C_r$  tank circuit operating above resonance is positive (the inductive reactance is larger in module than the capacitive reactance), i.e., the plus sign is located on the side of the node HB. Therefore:

$$\begin{aligned} a(V_{out} + V_{Rect}) &< \frac{V_{in}}{2} & (\text{HB}) \\ a(V_{out} + V_{Rect}) &< V_{in} & (\text{FB}) \end{aligned} \quad (39)$$

Then, when operating open-loop above resonance, for a given input voltage the LLC resonant converter will provide an output voltage lower than that available at

resonance; vice versa, in closed loop operation with a given output voltage the LLC resonant converter will operate above resonance when:

$$\begin{aligned} V_{in} &> 2a(V_{out} + V_{Rect}) \quad (\text{HB}) \\ V_{in} &> a(V_{out} + V_{Rect}) \quad (\text{FB}) \end{aligned} \quad (40)$$

In this case the conversion ratio, intended as previously mentioned, is  $< 1$  and the LLC converter is said to have a “step-down” or “buck” characteristic when operating above resonance.

4. When operating above resonance, the Thevenin-equivalent schematic of the LLC resonant tank as seen by the load has finite impedance (no more zero as when operating at resonance).

When the load current increases, for a given frequency (open-loop operation) the voltage conversion ratio diminishes; for a given  $V_{out}$  (closed-loop operation) operating frequency needs to get back closer to resonance.

5. The secondary rectifier D1 starts conducting as D2 cease to conduct and vice versa. They both stop conducting when the tank circuit's current  $I_R$  equals  $L_p$ 's current  $I_M$ , like when operating at resonance. However, this does not happen synchronously with the half-bridge leg transitions (it is  $I_R > I_M$  at  $t = t_1$  and  $I_R < I_M$  at  $t = t_4$ ): when this occurs  $I_R$  and  $I_M$  are “forced” to equalize so that the current of the conducting diode goes to zero.

The physical reason for that is the presence of  $L_s$ : when there is a transition of the half-bridge leg the resulting voltage change is not immediately directly impressed on the transformer (we have seen that  $C_r$  can be considered as a “dynamic” short circuit during transitions, i.e., its voltage can be considered constant) but falls across  $L_s$  that acts as a sort of “absorber”. This leaves  $I_M$  unchanged but pushes  $I_R$  towards  $I_M$ . Only when it is  $I_R = I_M$  and no current flows through the secondary rectifier that was previously conducting can the voltage across the primary winding of the transformer reverse and hence also the voltage across the secondary rectifiers.

In the end, also in this case they are reverse-biased only when their current has gone to zero, thus ensuring ZCS.

## B. DCMA at medium load

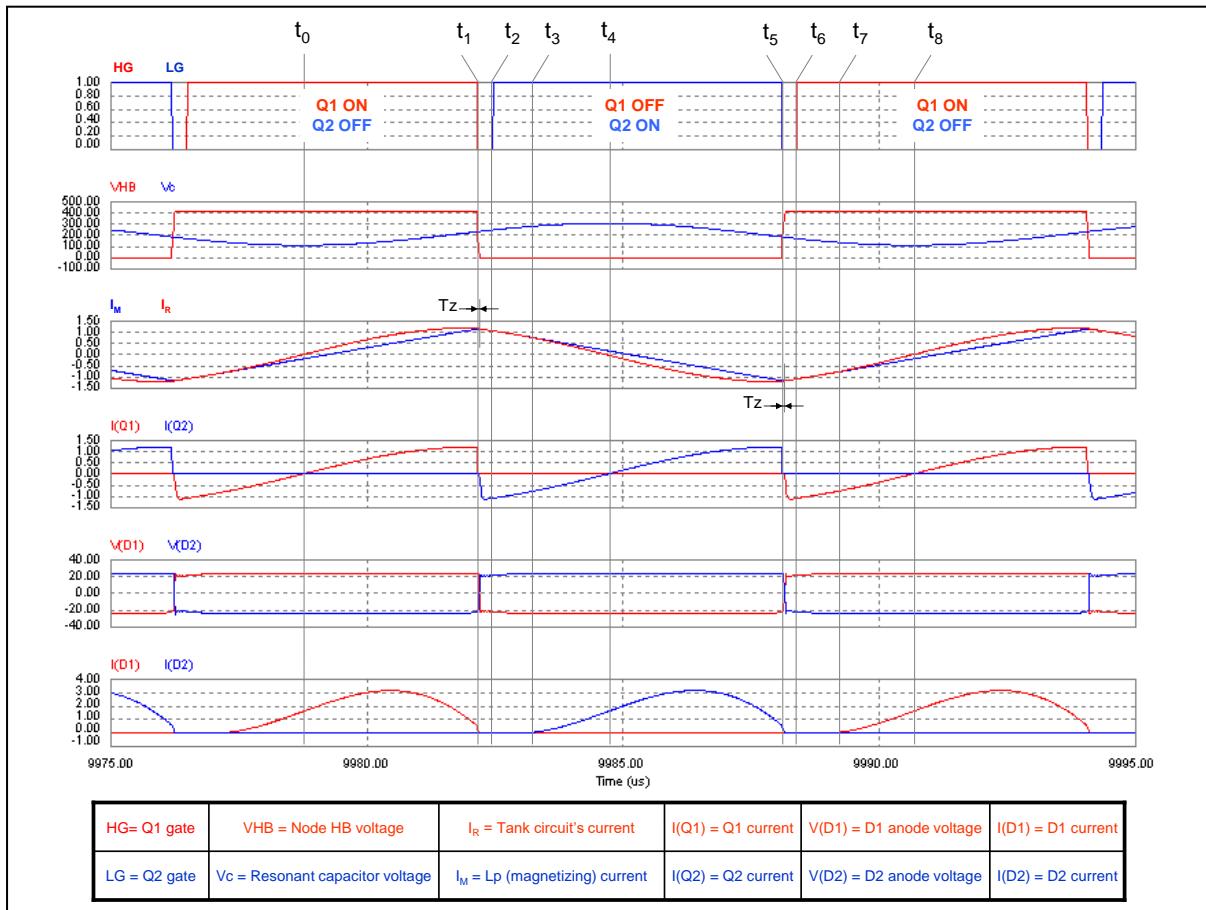
In this “above-resonance” DCM sub-mode it is possible to identify eight fundamentals sub-intervals; the relevant waveforms are illustrated in the timing diagram of figure 42.

The topological states are shown in figure 43. The switching details in the dead-time interval ( $t_1, t_2$ ) are shown in figure 44.

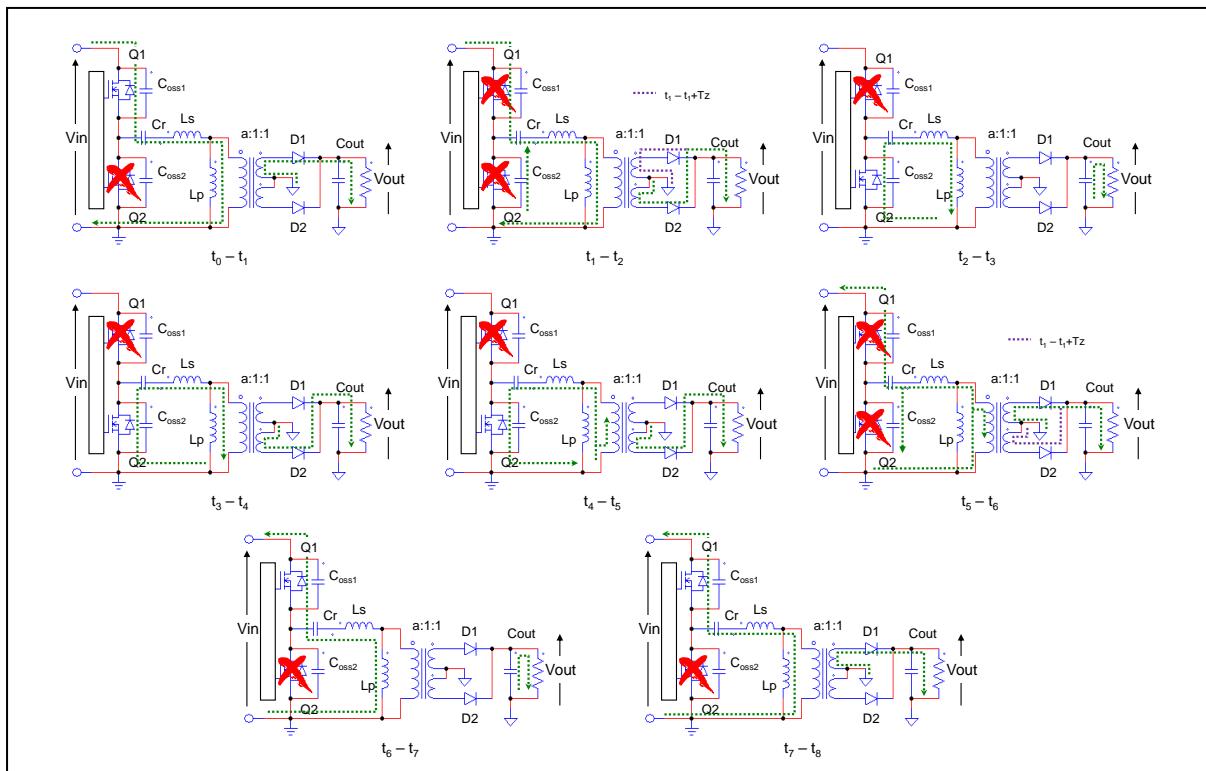
Two new sub-intervals, namely  $(t_2, t_3)$  and  $(t_6, t_7)$ , appear just after the dead-times of the half bridge leg transitions  $(t_1, t_2)$ ,  $(t_5, t_6)$ , respectively. The other six phases are identical to those of CCMA, thus only the new intervals will be described.

- a)  $t_2 \rightarrow t_3$ . Q1 is OFF and Q2 is ON; at  $t = t_2$   $I_R$  is diverted from DQ2 to the  $R_{DS(on)}$  of Q2, so that no significant energy is lost during the turn-on transient (ZVS); note that the operating point of Q2 is in the third quadrant, current is flowing from the source to drain; D1 is non conducting but the voltage across the secondary windings is still too low to let D2 conduct, then in this interval  $I_R = I_M$  is a portion of a sinusoid having a frequency  $f = f_{R2}$ ; this phase ends when D2 starts conducting at  $t = t_3$ .

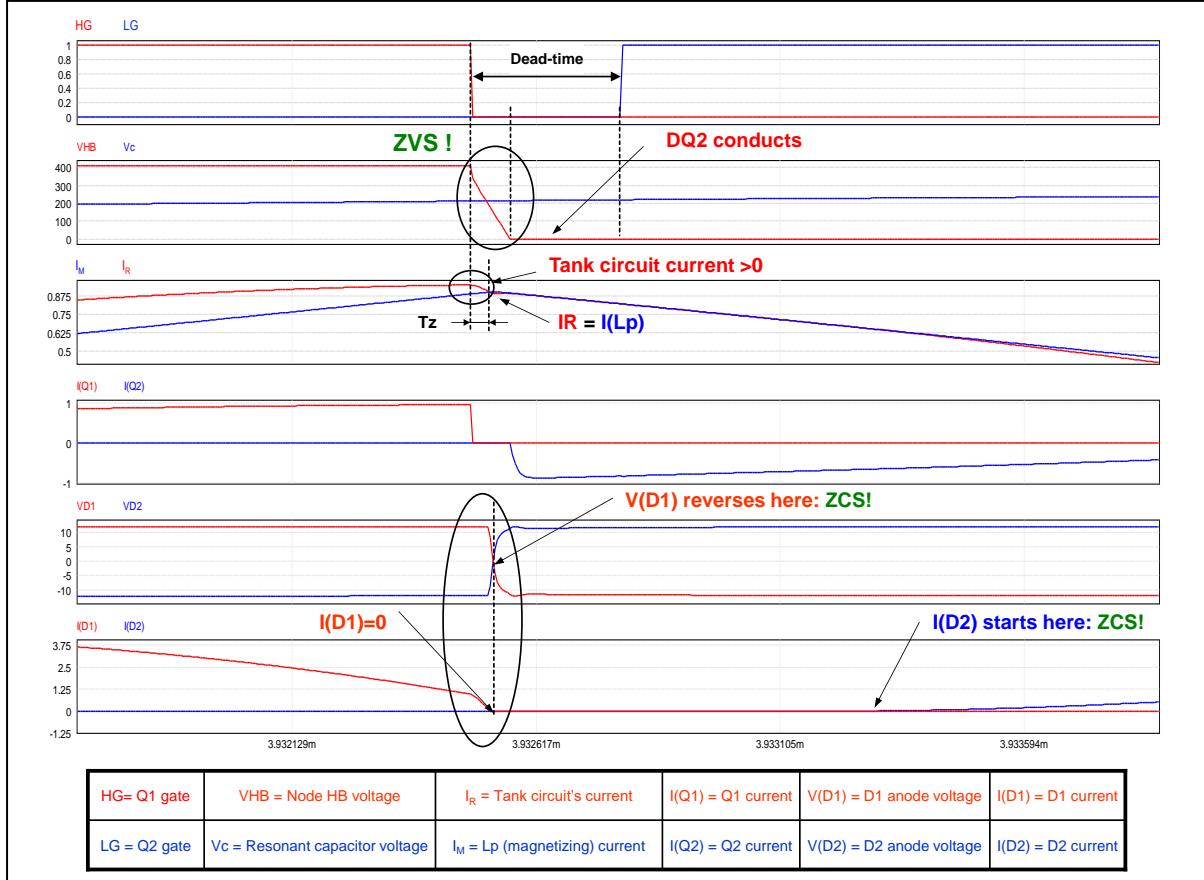
**Figure 42. Operation above resonance ( $f_{sw} > f_{R1}$ ): main waveforms in DCMA mode at medium load.**



**Figure 43. DCMA mode above resonance ( $f_{sw} > f_{R1}$ ): topological states.**



**Figure 44. DCMA mode above resonance ( $f_{sw} > f_{R1}$ ): switching details in ( $t_1, t_2$ ).**



- a)  $t_6 \rightarrow t_7$ . Q1 is ON and Q2 is OFF; at  $t = t_6$   $I_R$  is diverted from DQ1 to the  $R_{DS(on)}$  of Q1, so that no significant energy is lost during the turn-on transient (ZVS); note that the operating point of Q1 is in the third quadrant, current is flowing from the source to drain; D2 is non conducting but the voltage across the secondary windings is still too low to let D1 conduct, then still  $I_R = I_M$  is a portion of a sinusoid having a frequency  $f = f_{R2}$ ; this phase, which is specular to phase a), ends when D1 starts conducting at  $t = t_7$ .

#### Remarks

1. In this above-resonance DCM sub-mode the multi-resonant nature of the LLC converter shows up: in a switching cycle there are two time intervals just after bridge-leg transitions during which no current is flowing on the secondary side (whence this is DCM operation), then the entire transformer's primary inductance  $L_s + L_p$  resonates and the second resonance frequency  $f_{R2}$  appears.

As visible in figure 44, at the transitions of the half-bridge leg the resonant current  $I_R$  is still slightly greater than  $I_M$  in absolute value, so it takes a very small portion ( $T_z$ ) of the dead times for the two currents to equal each other (it can be considered as an example of a CCM-DCM mixed transition).

2. As shown in the diagrams of figure 42, the tank circuit current is still lagging the impressed voltage  $V_{HB}$ , so that they have the same sign at half-bridge leg transitions; furthermore, the switched currents  $I_R(t_1)$  and  $I_R(t_5)$  are large enough to complete the HB node swing well within the dead-times ( $t_1, t_2$ ) and ( $t_5, t_6$ ) respectively.

However, as compared to CCM mode, the energy delivery phases (i.e.,  $(t_0, t_1)$  in the half bridge,  $(t_0, t_1)$  and  $(t_4, t_5)$  in the full bridge) are shorter, the energy return phases (i.e.,  $(t_5, t_8)$  in the half bridge,  $(t_1, t_4)$  and  $(t_5, t_8)$  in the full bridge) are longer and the phase-shift  $\varphi$ :

$$\varphi = 2\pi \frac{t_8 - t_5}{t_8 - t_0} = 2\pi \frac{t_4 - t_1}{t_8 - t_0}. \quad (41)$$

increases moving towards  $\pi/2$ . Using ac terminology, the active energy is lower and the reactive energy is higher.

3. The secondary rectifiers D1 and D2 start conducting during the conduction period of Q1 and Q2, respectively. Both the initial current and also its  $dI/dt$  are zero, thus they have a soft turn-on. D1 and D2 cease to conduct when tank circuit's current  $I_R$  equals  $L_p$ 's current  $I_M$ .

In this case this is almost synchronous with either switch turn-off. Again, only when  $I_R$  equals  $I_M$  and no current is flowing through the secondary rectifier previously conducting can the voltage across the primary winding of the transformer reverse and hence also the voltage across the secondary rectifiers. In the end, also in this case they are reverse biased only when their current has gone to zero, thus ensuring ZCS.

4. Essentially, the reason why D2 does not conduct during  $(t_2, t_3)$  and D1 does not during  $(t_6, t_7)$  is that the voltage across the transformer is not large enough so that the voltage developed across  $L_p$  and reflected to the secondary side can forward-bias D2 or D1. In formulae, this is expressed as:

$$[V_{HB} - V_C(t)] \frac{L_p}{L_s + L_p} = \pm a(V_{out} + V_{Rect}), \quad (42)$$

where "+" applies when  $V_{HB} = Vin$ , "-" when  $V_{HB} = 0$ . This is the same condition seen for a DCM transition of  $V_{HB}$ , extended to the entire intervals  $(t_2, t_3)$ ,  $(t_6, t_7)$ .

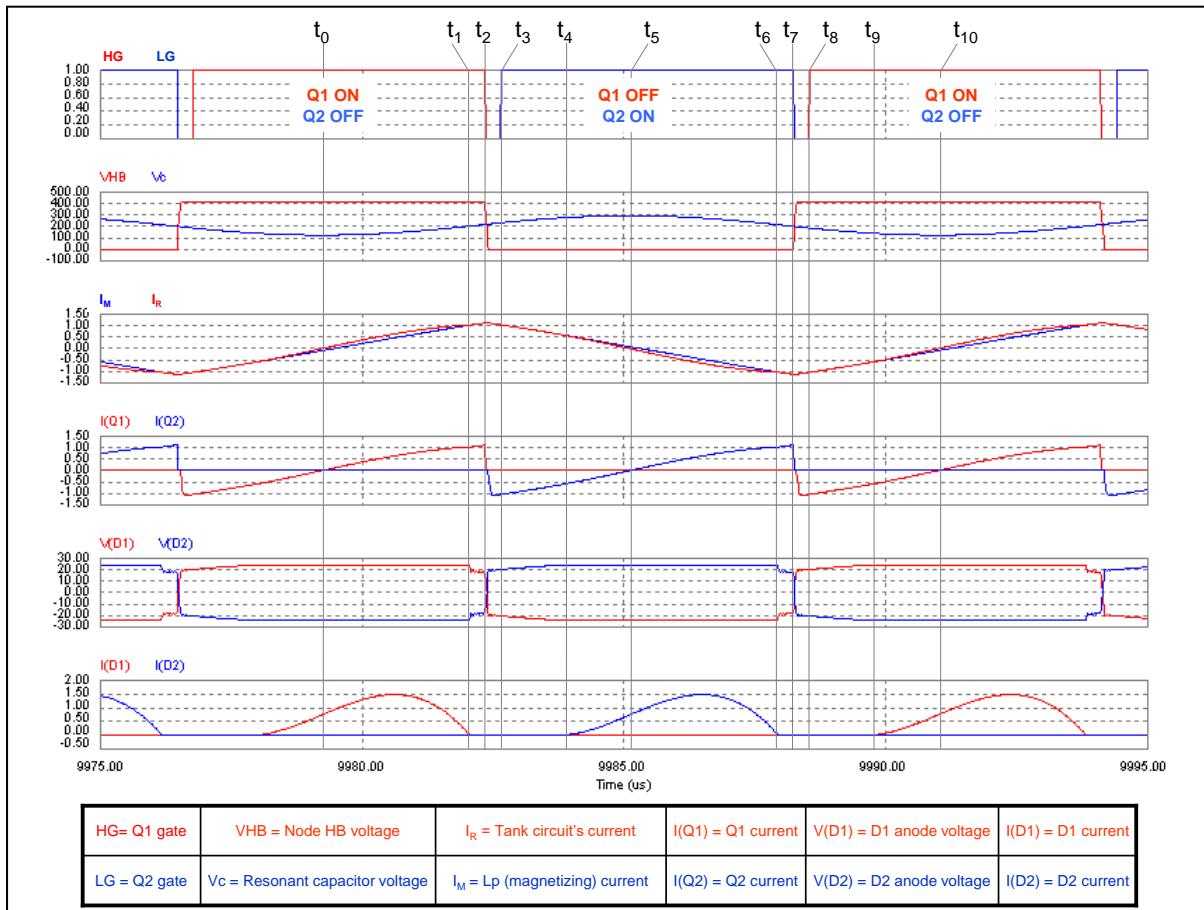
### C. DCMAB at light load

In this "above-resonance" DCM sub-mode it is possible to identify ten fundamentals sub-intervals; the relevant waveforms are illustrated in the timing diagram of figure 45 and the topological states in figure 46. Figure 47 shows the switching details in the dead-time interval  $(t_2, t_3)$ .

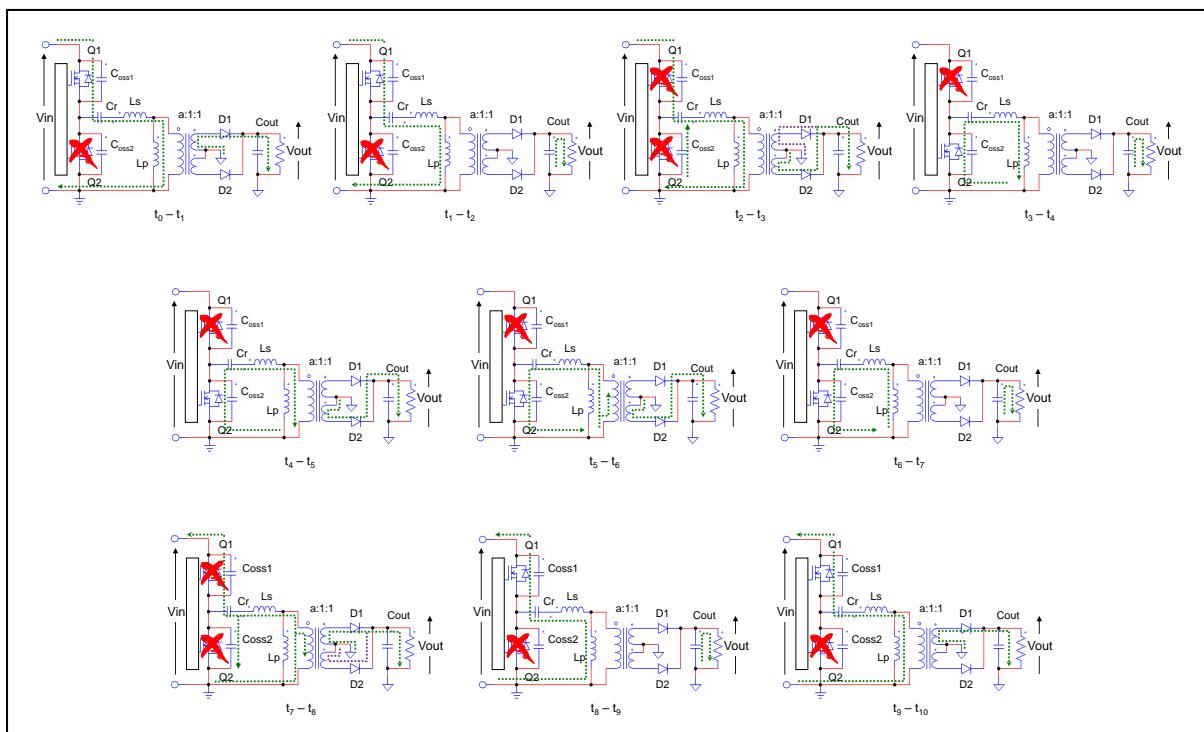
Two more new sub-intervals, namely  $(t_1, t_2)$ ,  $(t_6, t_7)$  appear just before the dead-times of the half-bridge leg transitions  $(t_2, t_3)$ ,  $(t_7, t_8)$ , respectively. The remaining eight phases are identical to those of the DCMA above-resonance mode, thus only the new intervals will be described.

- a)  $t_1 \rightarrow t_2$ . Q1 is ON and Q2 is OFF; at  $t = t_1$   $I_R$  equals  $I_M$  and then  $I(D1)$  becomes zero, before Q1 turns off at  $t = t_2$  and remains at zero until this phase ends at  $t = t_2$ . During this interval the condition (42) is met and the current  $I_R = I_M$  is a portion of a sinusoid having a frequency  $f = f_{R2}$ .
- b)  $t_6 \rightarrow t_7$ . Q1 is OFF and Q2 is ON; at  $t = t_6$   $I_R$  equals  $I_M$  and then  $I(D2)$  becomes zero before Q2 turns off at  $t = t_7$  and remains at zero until this phase ends at  $t = t_7$ . During this interval, specular to  $(t_1, t_2)$ , the condition (42) is met, thereby the current  $I_R = I_M$  is a portion of a sinusoid having a frequency  $f = f_{R2}$ .

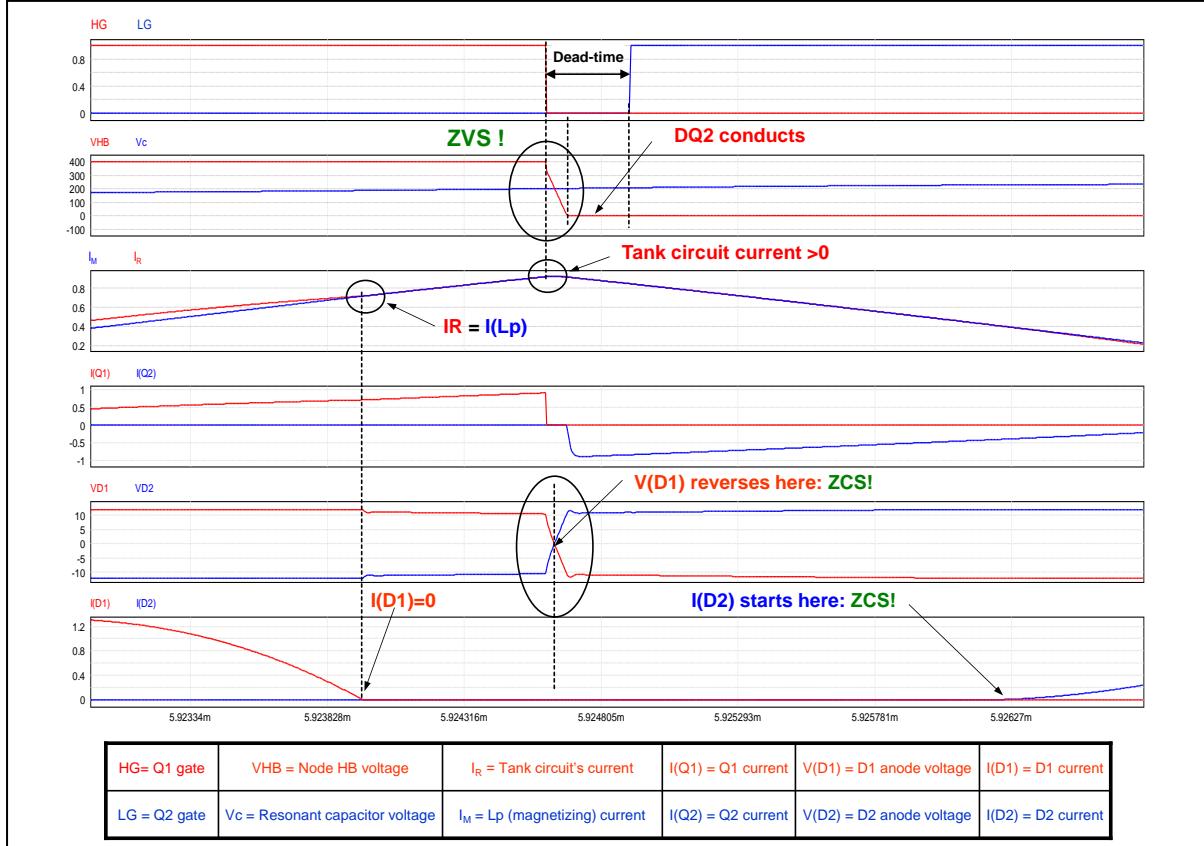
**Figure 45. Operation above resonance ( $f_{sw} > f_{R1}$ ): main waveforms in DCMAB mode at light load.**



**Figure 46. DCMAB mode above resonance ( $f_{sw} > f_{R1}$ ): topological states.**



**Figure 47. DCMAB mode above resonance ( $f_{sw} > f_{R1}$ ): switching details in  $(t_2, t_3)$ .**



### Remarks

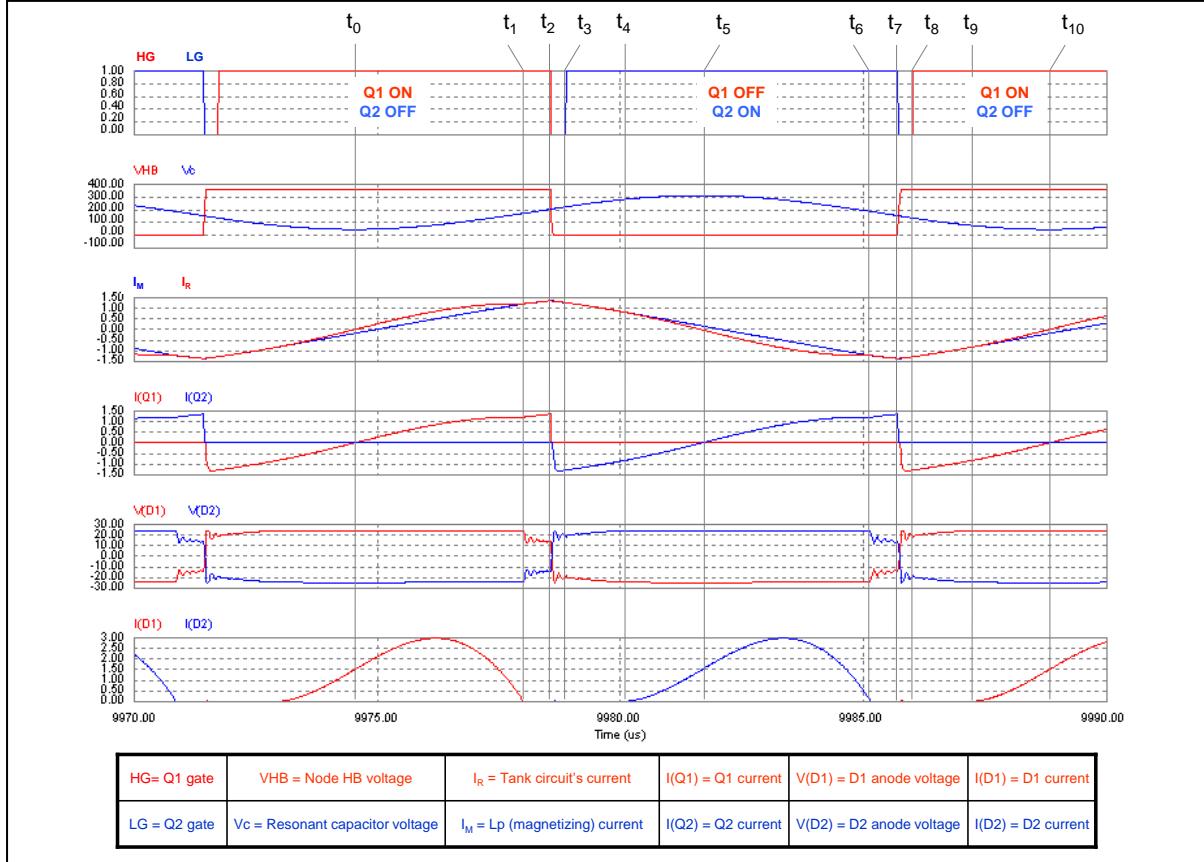
1. The transition between this DCMAB mode and the previous DCMA is marked by the  $I_R = I_M$  condition occurring exactly at  $t = t_1$ .
2. In this above-resonance DCM sub-mode, in a switching cycle there are two time intervals  $(t_1, t_4), (t_6, t_9)$  during which no current flows on the secondary side (whence this is DCM operation) and then the entire transformer's primary inductance  $L_s+L_p$  resonates and  $f_{R2}$  appears. Considering each half-cycle, non-conductive intervals appear at the beginning and the end.
3. As shown in the diagrams of figure 45, the tank circuit current is still lagging the impressed voltage, so that they have the same sign at half-bridge leg transitions; furthermore, the switched currents  $I_R(t_2)$  and  $I_R(t_6)$  are large enough to complete the HB node swing well within the dead-times  $(t_2, t_3)$  and  $(t_7, t_8)$  respectively (see figure 47). As compared to DCMA mode, the energy delivery phases (i.e.,  $(t_0, t_2)$  in the half bridge,  $(t_0, t_2)$  and  $(t_5, t_7)$  in the full bridge) even shorter, the energy return phases (i.e.,  $(t_7, t_{10})$  in the half bridge,  $(t_2, t_5)$  and  $(t_7, t_{10})$  in the full bridge) are longer the external recirculation phase is longer and the phase-shift  $\varphi$ :

$$\varphi = 2\pi \frac{t_{10}-t_7}{t_{10}-t_0} = 2\pi \frac{t_5-t_2}{t_{10}-t_0}. \quad (43)$$

gets closer to  $\pi/2$ . Most of the energy in the tank circuit is reactive.

4. As to the secondary rectifiers, they start conducting during the conduction period of Q1 and Q2, respectively. Both the initial current and also its  $dI/dt$  are zero, thus they have a soft turn-on. they cease to conduct before the transitions of the half-bridge; the operation is DCM, then ZCS occurs by definition.

**Figure 48. Operation below resonance ( $f_{CM} < f_{sw} < f_{R1}$ ): main waveforms in DCMAB mode.**



*Operation below resonance ( $f_{CM} < f_{sw} < f_{R1}$ ).*

In this operating mode the converter still exhibits its usual frequency vs. load characteristic. We will consider two sub-modes where, in a closed-loop regulated system, DCM operation gets deeper and deeper as the load increases and frequency moves away from resonance.

#### A. DCMAB at medium-light load

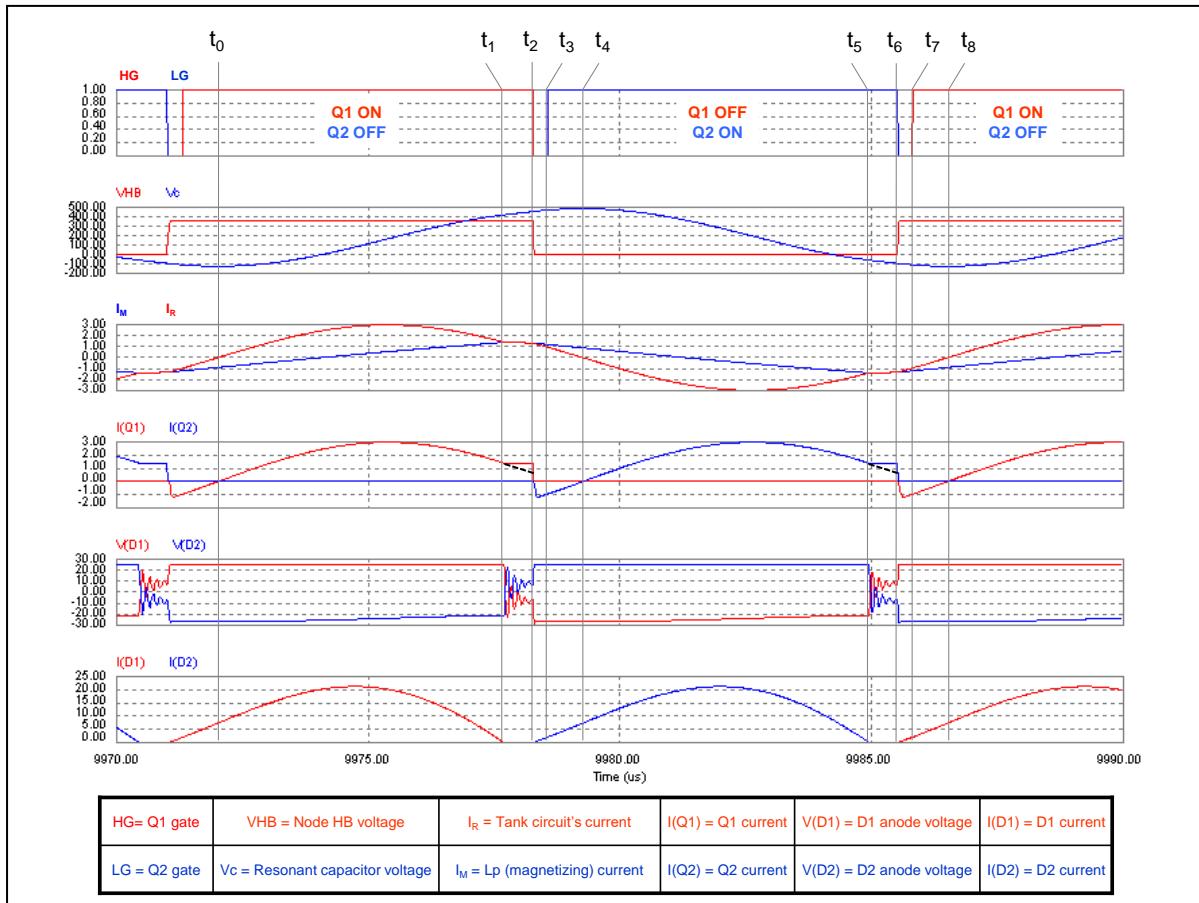
This below-resonance DCM sub-mode is exactly equal to the above-resonance DCMAB sub-mode previously considered. The waveforms are shown in figure 48 and it is possible to see that they match those shown in figure 45. Also the topological states and the switching details during the dead-time ( $t_2, t_3$ ) are the same as those shown in figures 46 and 47 respectively. To be noted only that in this case the condition  $I_R = I_M$  at  $t = t_1$  occurs at a considerably higher power level than in the case of the above-resonance DCMAB sub-mode (2:1 in the example shown).

#### B. DCMB at heavy load

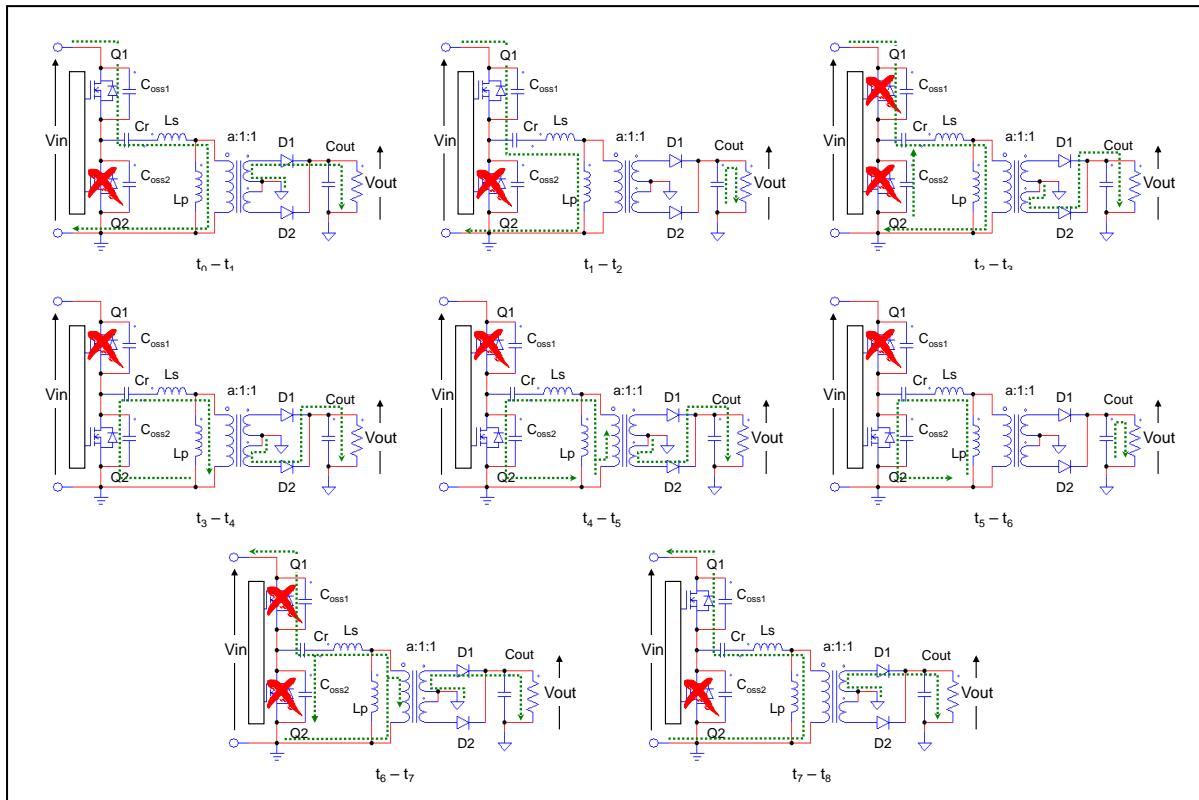
This “below-resonance” DCM sub-mode, which is unique to below resonance operation, actually comprises two sub-modes (DCMB2 & DCMB1) as frequency moves away from resonance. Their waveforms do not differ much, only those of DCMB2 (which occurs at a higher frequency) will be shown.

It is possible to identify eight fundamentals sub-intervals and the relevant waveforms are illustrated in the timing diagram of figure 49. Again,  $t_0$  is the instant when, with Q1 conducting and Q2 open, the tank current  $I_R$  has a positive-going zero-crossing. The topological states are shown in figure 50.

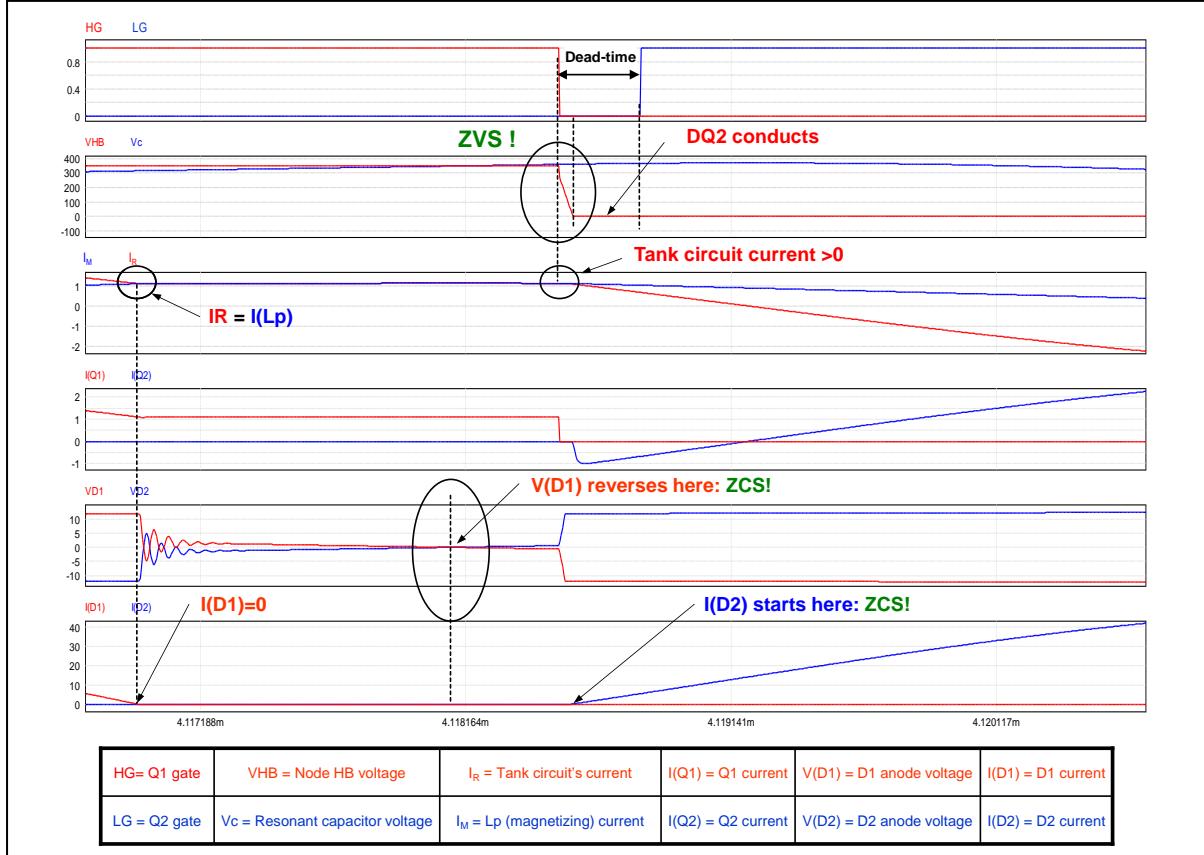
**Figure 49. Operation below resonance ( $f_{CM} < f_{sw} < f_{R1}$ ): main waveforms in DCMB2 mode.**



**Figure 50. DCMB2 mode below resonance ( $f_{CM} < f_{sw} < f_{R1}$ ): topological states.**



**Figure 51. DCMB2 mode below resonance ( $f_{CM} < f_{SW} < f_{R1}$ ): switching details in ( $t_2$ ,  $t_3$ ).**



- $t_0 \rightarrow t_1$ . Q1 is ON and Q2 is OFF; in the half bridge this is the sole energy delivery phase (the first of two in the full bridge), when current flows from the input source to the tank circuit; the operating point of Q1 is in the first quadrant (current is flowing from drain to source); D2 is reverse-biased while D1 is conducting, so  $L_p$  is shorted by the output load reflected back to the primary side and the voltage across it is fixed at  $a \cdot (V_{out} + V_{Rect})$ ;  $L_p$ , then, is not participating in resonance and  $C_r$  is resonating with  $L_s$  only;  $I_R$  is a portion of a sinusoid with a frequency  $f = f_{R1}$ ; during this phase, which ends when  $I_R$  equals  $I_M$  and, then,  $I(D1) = 0$  at  $t = t_1$ ,  $I_R$  reaches its maximum value, after that it starts decaying.
- $t_1 \rightarrow t_2$ . Q1 is ON and Q2 is OFF; at  $t = t_1$   $I(D1)$  becomes zero and  $I_R$  equals  $I_M$ , that is before the conduction time of Q2 ends; both D1 and D2 are non-conducting and  $L_p$ , no more shunted by the load reflected to the primary side, goes effectively in series to  $L_s$  and participates to resonance;  $I_R$  is a portion of a sinusoid having a frequency  $f = f_{R2}$ ; depending on tanks circuit's parameters and on the operating conditions, this portion can be similar to a straight line, as shown in the diagrams of figure 49; this phase ends when Q1 is switched off at  $t = t_2$ .
- $t_2 \rightarrow t_3$ . This is the dead-time during which both Q1 and Q2 are OFF; at  $t = t_2$  the current  $I(Q1) = I_M = I_R$  is greater than zero and provides the energy to let the node HB swing from  $V_{in}$  to ground, so that the body diode of Q2, DQ2, is injected; this allows  $I_R$  to flow; the voltage across  $L_p$  reverses to  $-a \cdot (V_{out} + V_{Rect})$ ; D2 starts conducting while D1 is reverse biased; this phase ends when Q2 is switched on at  $t = t_3$ . The detailed view of this interval is shown in figure 51.

- d)  $t_3 \rightarrow t_4$ . Q1 is OFF and Q2 is ON; at  $t = t_3$   $I_R$  is diverted from DQ2 to the  $R_{DS(on)}$  of Q2, so that no significant energy is lost during the turn-on transient (ZVS); note that the operating point of Q2 is in the third quadrant, current is flowing from the source to drain; D2 keeps on conducting and the voltage across  $L_p$  is  $-a \cdot (V_{out} + V_{Rect})$ , so that  $L_p$  is not participating in resonance and  $C_r$  is resonating with  $L_s$  only;  $I_R$  is a portion of a sinusoid having a frequency  $f = f_{R1}$ ; this phase ends when  $I_R = 0$  at  $t = t_4$ .
- e)  $t_4 \rightarrow t_5$ . Q1 is OFF and Q2 is ON; in the half bridge this is the recirculation phase (the second energy delivery phase in the full bridge), specular to phase a); the tank current  $I_R$ , which is zero at  $t = t_4$  becomes negative; D1 is non-conducting;  $I_M$  has a negative slope, so the voltage across  $L_p$  must be negative; since the diode D2 is conducting this voltage will be equal to  $-a \cdot (V_{out} + V_{Rect})$ ;  $L_p$  is not participating in resonance,  $C_r$  is resonating with  $L_s$  only and  $I_R$  is a portion of a sinusoid having a frequency  $f = f_{R1}$ ; during this phase, which ends when  $I_R$  equals  $I_M$  and, thereby,  $I(D2)$  is zero at  $t = t_5$ ,  $I_R$  reaches its minimum value, after that it starts increasing;
- f)  $t_5 \rightarrow t_6$ . This phase mirrors ( $t_1, t_2$ ): at  $t = t_5$   $I(D2)$  becomes zero and  $I_R$  equals  $I_M$ , that is, before the conduction time of Q1 ends; both D1 and D2 are non-conducting and  $L_p$ , no more shunted by the load reflected to the primary side, goes effectively in series to  $L_s$  and participates to resonance;  $I_R$  is now a portion of a sinusoid having a frequency  $f = f_{R2}$ ; this phase ends when Q2 is switched off at  $t = t_6$ .
- g)  $t_6 \rightarrow t_7$ . This is the dead-time during which both Q1 and Q2 are OFF; at  $t = t_6$  the current  $I(Q2) = I_M = -I_R$  is greater than zero and provides the energy to let the node HB swing from 0 to  $V_{in}$ , so that the body diode of Q1, DQ1, is injected; this allows  $I_R$  to flow back to the input source; the voltage across  $L_p$  reverses to  $a \cdot (V_{out} + V_{Rect})$ , D1 starts conducting while D2 is reverse; this phase ends when Q1 is switched on at  $t = t_7$ .
- h)  $t_7 \rightarrow t_8$ . Q1 is ON and Q2 is OFF; at  $t = t_7$   $I_R$  is diverted from DQ1 to the  $R_{DS(on)}$  of Q1, so that no significant energy is lost during the turn-on transient (ZVS); note that now the operating point of Q1 is in the third quadrant, current is flowing from the source to drain; this phase, along with the preceding one is the energy return phase: current is negative (coming out of the input terminal) despite the impressed voltage is positive so that the input energy is negative, i.e., it is returned to the input source; D1 is still conducting and the voltage across  $L_p$  is  $a \cdot (V_{out} + V_{Rect})$ , so that  $L_p$  is not participating in resonance anymore and  $C_r$  is resonating with  $L_s$  only;  $I_R$  is again a portion of a sinusoid having a frequency  $f = f_{R1}$ ; this phase ends at  $t = t_8$  when  $I_R = 0$  and another switching cycle begins.

#### Remarks

1. In this below-resonance DCM sub-mode the multi-resonant nature of the LLC converter is apparent too: from  $t_1$  to  $t_2$  and from  $t_5$  to  $t_6$  the secondary rectifiers are both open and the second resonance frequency  $f_{R2}$  appears. This is one of the fundamental advantages of the LLC resonant converter over the traditional LC series-resonant converter. In fact, it helps keep operation away from capacitive mode: although the tank circuit current  $I_R$  lags the impressed voltage  $V_{HB}$  (being  $f_{sw} > f_{CM}$  by assumption), the switching period is longer than the resonant period,  $1/f_{R1}$ . Then  $I_R$ , which is decaying (in absolute value), might come close to zero or even reverse if it still evolved according to the same sinusoid at frequency  $f = f_{R1}$  (see the extrapolated black dotted lines drawn in  $(t_1, t_2)$  and  $(t_5, t_6)$ ). This lower frequency

sinusoid “holds up” the tank current, delaying the instant when the switched currents  $I_R(t_2)$  and  $I_R(t_6)$  change sign and have amplitude large enough to complete the HB node swing well within the dead-times ( $t_2$ ,  $t_3$ ) and ( $t_6$ ,  $t_7$ ) respectively, i.e., that ZVS is achieved.

2. In the series LC tank  $L_s-C_r$  operating below resonance with  $f_{sw} > f_{CM}$  the voltage drop across the L-C series is negative (the capacitive reactance is larger in module than the inductive reactance), i.e., a minus sign is located at the node HB. Hence:

$$\begin{aligned} a(V_{out} + V_{Rect}) &> \frac{V_{in}}{2} \quad (\text{HB}) \\ a(V_{out} + V_{Rect}) &> V_{in} \quad (\text{FB}) \end{aligned} \quad (44)$$

Then, when operating open-loop below resonance, for a given input voltage the LLC resonant converter will provide an output voltage higher than that available at resonance; vice versa, in closed loop operation with a given output voltage the LLC resonant converter will operate above resonance when:

$$\begin{aligned} V_{in} &< 2a(V_{out} + V_{Rect}) \quad (\text{HB}) \\ V_{in} &< a(V_{out} + V_{Rect}) \quad (\text{FB}) \end{aligned} \quad (45)$$

In other words, the conversion ratio, intended as previously mentioned, is  $> 1$ ; then the LLC is said to have a “step-up” characteristic when operating below resonance.

3. The secondary rectifiers D1 and D2 start conducting when Q2 and Q1 are switched off, respectively. The initial current is zero and its  $dI/dt$  is low, thus they have a soft turn-on. They cease to conduct before the transitions of the half-bridge; the operation is DCM, then ZCS occurs by definition. Essentially, the reason why D2 does not conduct during  $(t_1, t_2)$  and D1 does not during  $(t_5, t_6)$  is that during these sub-intervals the condition (37) is met.
4. The waveforms in DCMB1 are very similar, only  $I_R$  detaches from  $I_M$  and the secondary rectifiers start conducting slightly before the primary switches are turned off. Therefore, while DCMB2 is characterized by the duration of the intervals  $(t_1, t_2)$  and  $(t_5, t_6)$  that gets longer as frequency is reduced, in DCMB1 the duration of these intervals starts decreasing quite rapidly with frequency, to reach zero when  $f_{sw} = f_{CM}$ , i.e., at the boundary with capacitive mode operation. DCMB1 occurs in the frequency region bordering the inductive-capacitive boundary, thus it can be a good design practice not to go below the DCMB1-DCMB2 boundary.

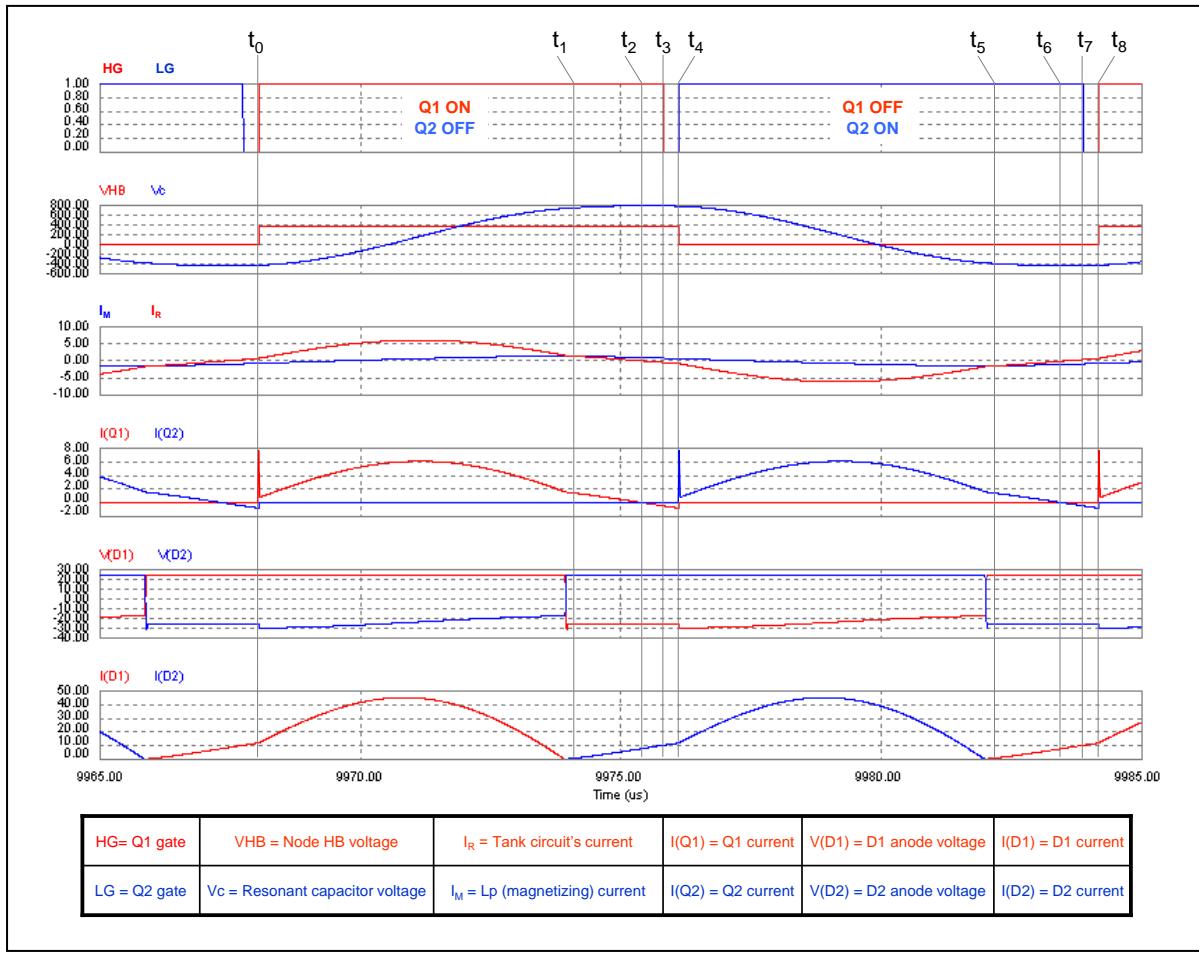
*Capacitive-mode operation below resonance ( $f_{R2} < f_{sw} < f_{CM}$ ).*

In this operating mode, unique to below-resonance operation and corresponding to the CCMB operating mode defined in [14], it is possible to distinguish eight fundamental time sub-intervals within a switching cycle, as illustrated in the timing diagrams of figure 52.

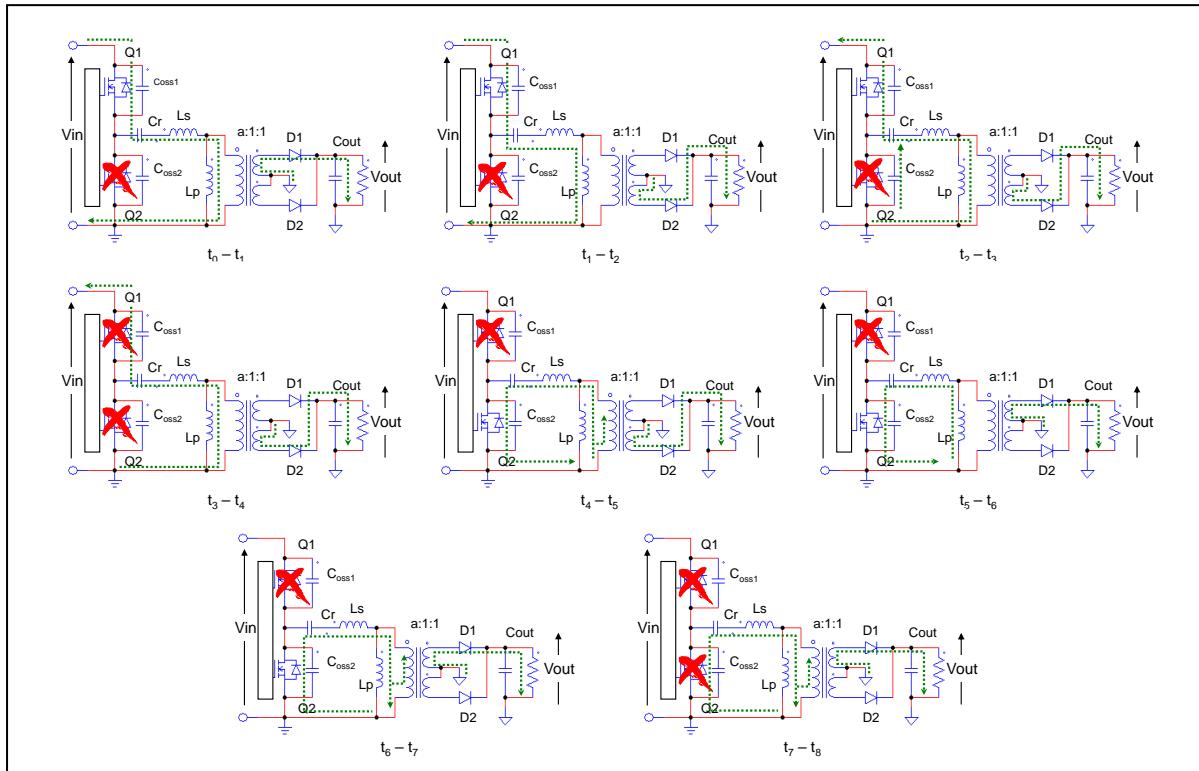
In this case it is convenient to define  $t_0$  as the instant when Q1 is switched on. The topological states are shown in figure 53.

- a)  $t_0 \rightarrow t_1$ . The tank current  $I_R(t_0)$  as Q1 is switched on is already positive: this means that in the just finished dead time it was flowing through the body diode of Q2, DQ2; and, actually, this is confirmed by the voltage  $V_{HB}$  of the half-bridge midpoint which was previously zero and is abruptly pulled up to  $V_{in}$  exactly at  $t = t_0$  with a large  $dv/dt$ ; the body diode DQ2 is then reverse-recovered and a large current spike flows through Q1 and DQ2 until the latter recovers completely. This is the so-called type-2 hard switching, functionally, similar to a cross-conduction of the half-bridge leg.

**Figure 52. Capacitive mode operation below resonance ( $f_{R2} < f_{sw} < f_{CM}$ ): main waveforms.**



**Figure 53. CCMB mode below resonance ( $f_{R2} < f_{sw} < f_{CM}$ ): topological states.**



Very high  $d/dt$  may occur and, as a result, large voltage spikes generated across the parasitic inductances experiencing this large  $d/dt$ ; the voltage  $V_{HB}$  may have large positive overshoots. During this phase energy is taken from the input source, the tank current reaches its maximum value and then decays; the phase ends when  $I_R = I_M$  and then,  $I(D1) = 0$  at  $t = t_1$ .

- b)  $t_1 \rightarrow t_2$ . Unlike what happens in the below-resonance DCMB2 sub-mode, where there was insufficient voltage across the resonant capacitor to forward-bias D2, here  $V_C$  is much larger and D2 starts conducting immediately at  $t = t_1$ ;  $I_R$  starts decreasing, becoming lower than  $I_M$  and eventually crosses zero before Q1 turns off, at  $t = t_2$ , which marks the end of this phase.
- c)  $t_2 \rightarrow t_3$ .  $I_R$ , which is negative and decreasing, is flowing through Q1 that is working in the third quadrant;  $I(D2)$  is positive and increasing; this phase ends at  $t = t_3$  when Q1 turns off.
- d)  $t_3 \rightarrow t_4$ . This is the dead-time during which both Q1 and Q2 are OFF; during this phase  $I_R$  is negative and further decreasing; since Q1 is off, it is flowing through DQ1; note that the voltage of the half-bridge midpoint  $V_{HB}$  does not change; this phase ends when Q2 turns on at  $t = t_4$ .
- e)  $t_4 \rightarrow t_5$ . The tank current  $I_R(t_4)$  as Q2 is switched on is already negative and flowing through the body diode of Q1, DQ1; the voltage of the half-bridge midpoint,  $V_{HB}$ , is abruptly pulled down to ground at  $t = t_4$  with a large  $dv/dt$ ; the body diode DQ1 is then reverse-recovered and a large current spike flows through Q2 and DQ1 until the latter recovers completely. Again, this is the so-called type-2 hard switching, described in Part II chapter 4, functionally, similar to a cross-conduction of the half-bridge leg.  
Very high  $d/dt$  may occur and, as a result, large voltage spikes generated across the parasitic inductances experiencing this large  $d/dt$ ; the voltage  $V_{HB}$  may have large negative undershoots. During this phase energy is internally recirculated, the tank current reaches its minimum value and then increases; the phase ends when  $I_R = I_M$  and then,  $I(D2) = 0$  at  $t = t_5$ .
- f)  $t_5 \rightarrow t_6$ . This phase mirrors exactly ( $t_1, t_2$ ): the voltage  $V_C$  across the resonant capacitor is so large that D1 is forward-biased and starts conducting immediately at  $t = t_5$ ;  $I_R$  starts increasing, becoming higher than  $I_M$  and eventually crosses zero before Q2 turns off, at  $t = t_6$ , which marks the end of this phase.
- g)  $t_6 \rightarrow t_7$ . This phase mirrors exactly ( $t_2, t_3$ ):  $I_R$ , which is positive and increasing, is flowing through Q2 that is working in the third quadrant;  $I(D1)$  is positive and increasing; this phase ends at  $t = t_7$  when Q2 turns off.
- h)  $t_7 \rightarrow t_8$ . This is the dead-time during which both Q1 and Q2 are OFF; during this phase  $I_R$  is positive and increasing; since Q2 is off, it is flowing through DQ2; note again that the voltage of the half-bridge midpoint  $V_{HB}$  does not change; this phase ends when Q2 turns on at  $t = t_8$  and another switching cycle begins. The detailed view of this interval has been shown already in figure 28 (where  $t_0$  corresponds to  $t_7$  and  $t_1$  to  $t_8$ ).

#### Remarks

1. In the below-resonance capacitive mode operation current is continuously flowing on the secondary side, except for single points in time ( $t = t_1, t = t_5$ ), then this is a CCM mode (as already said, it corresponds to the CCMB mode defined in [14]).

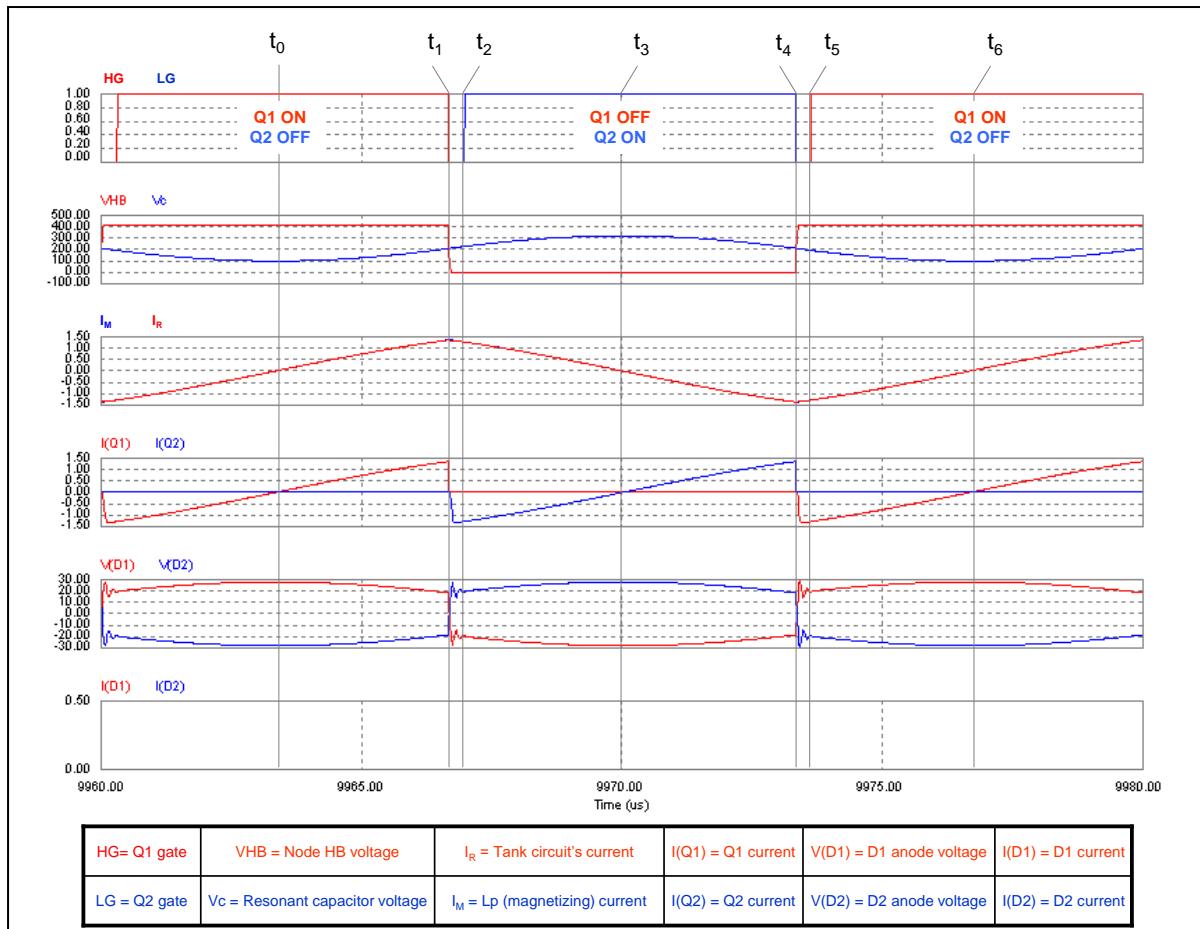
2. The physical reason of this CCMB operation is, as previously pointed out, the large voltage developed across the resonant capacitor. Then a large energy level must be circulating in the tank circuit in order for the capacitive mode to take place. Capacitive operating mode is then likely to occur under heavy load, overload or short circuit conditions and appropriate countermeasures must be taken to handle this.
3. Unlike the other modes, in capacitive mode the secondary rectifiers D1 and D2 start conducting during the conduction period of Q2 and Q1, respectively. The initial current is zero and its  $di/dt$  is low, thus they have a soft turn-on. Again, also in this case the voltage across the secondary rectifiers reverses as a result of their currents going to zero. Then, ZCS is maintained even under these conditions, and this confirms that the secondary rectifiers are soft switched at both turn-on and turn-off under all operating conditions as previously discussed.

#### No-load operation - cutoff

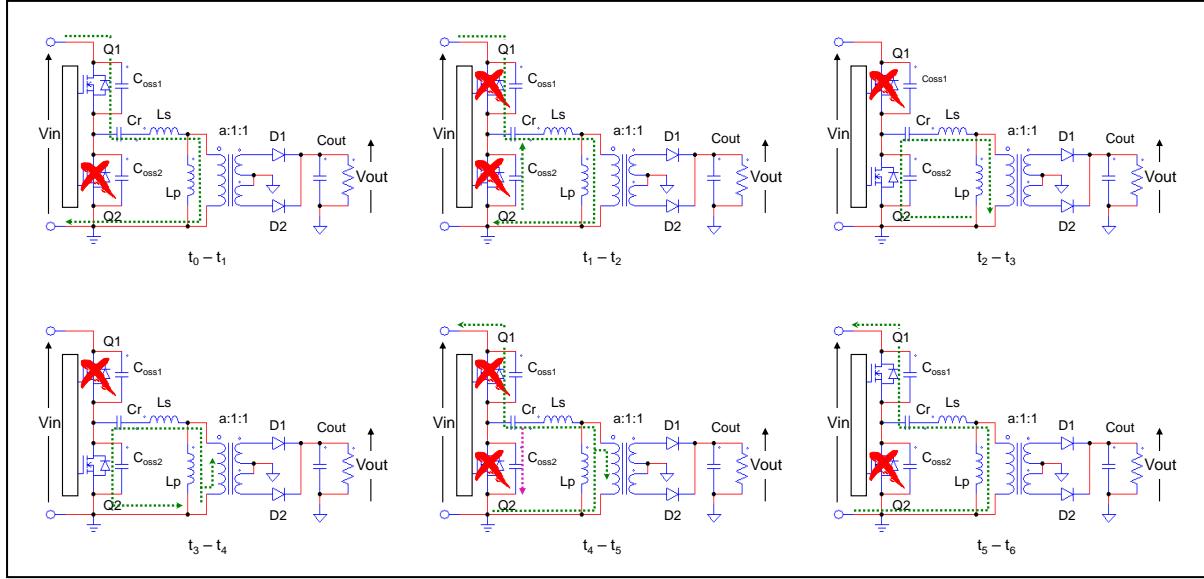
The ability to operate under no-load conditions is another peculiar characteristic of the LLC resonant converter. The typical waveforms in this operating mode, called also “cutoff” mode, which can occur at frequencies both above, below and at the resonant frequency  $f_{R1}$ , as demonstrated in [14], are illustrated in the timing diagrams of figure 54. The topological states are shown in figure 55.

Note that it is  $I_R = I_M$ , then  $I(D1) = I(D2) = 0$ , throughout the entire switching cycle;  $I_R$  is made by portions of sinusoid at  $f = f_{R2}$  but looks very much like a triangular waveform.

**Figure 54. No-load operation (cutoff): main waveforms.**



**Figure 55. No-load operation (cutoff): topological states.**



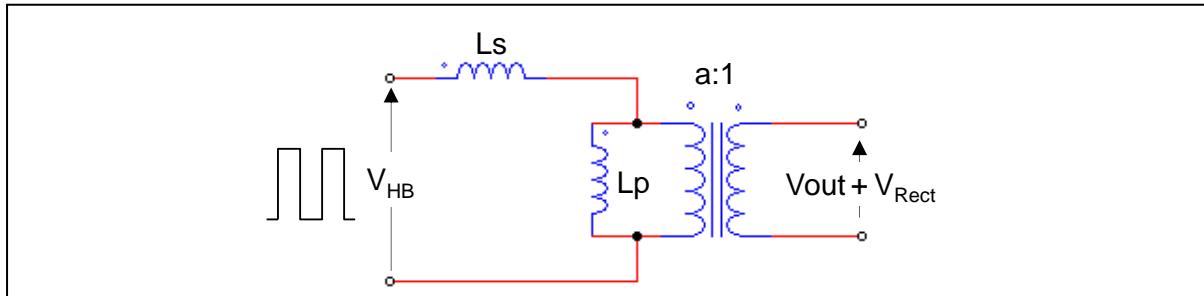
In order for this operation to occur, the voltage developed across  $L_p$  and reflected to the secondary side has to be lower than the output voltage throughout the entire switching cycle, so that either secondary rectifier cannot be forward-biased; in other words, the condition (39) has to be met for  $t \in (t_0, t_6)$ . Also, note that  $I_R$  is in quadrature with the impressed voltage  $V_{HB}$ , that is, the phase-shift  $\varphi$  equals  $\pi/2$ . This is consistent with the interpretation of  $\cos \varphi$  as the input power factor ( $\cos \pi/2 = 0$ ).

The ability of the converter to operate with no-load can be easily deduced by the condition (39) itself: however big the peak value of  $V_{in}(t) - V_C(t)$  is, if  $a \cdot (V_{out} + V_{Rect})$  is not zero, it is possible to find a value of  $L_p$  that meets condition (39). In the end: no-load operation capability is not an intrinsic property of the LLC resonant converter (like ZCS for the secondary rectifiers) but it can be achieved with an appropriate design of the tank circuit.

From a different standpoint, under no load conditions the resonant capacitor  $C_r$  “disappears” ( $V_C(t) \approx V_{in}/2$  in the half bridge,  $V_C(t) \approx 0$  in the full bridge) and the output voltage is given by the inductive divider made up by  $L_s$  and  $L_p$  as shown by the equivalent circuit of figure 56.

Then, if the output-to-input voltage conversion ratio is greater than the inductive divider ratio, regulation will be possible at some finite frequency, otherwise it will not. From (39), substituting  $V_{HB} = V_{in}$  and with the appropriate values of  $V_C(t)$  for the half bridge and the full bridge, it is possible to find a necessary condition in order for the converter to be able to regulate at zero load:

**Figure 56. LLC circuit equivalent schematic under no-load conditions.**



$$\begin{aligned} \frac{L_p}{L_s+L_p} &\leq 2 \frac{a(V_{out}+V_{Rect})}{V_{in}} \quad (\text{HB}) \\ \frac{L_p}{L_s+L_p} &\leq \frac{a(V_{out}+V_{Rect})}{V_{in}} \quad (\text{FB}) \end{aligned} \quad (46)$$

The difference with respect to the LC series resonant converter is apparent: if  $L_p \rightarrow \infty$  the LLC converter turns into the LC one; with no load no current can flow in the resonant tank and the only possible equilibrium condition is when input and output voltage (reflected to the primary side) are equal:  $V_{in} = 2a \cdot (V_{out} + V_{Rect})$  in the half bridge, or  $V_{in} = a \cdot (V_{out} + V_{Rect})$  in the full bridge. If the input and output voltage have a different ratio, output voltage regulation is impossible.

$L_p$ , then, plays a key role: it not only allows soft switching under no-load conditions as already discussed, but also makes no-load operation possible. The price to pay for that is the considerable tank current  $I_R = I_M$  circulating in the circuit as shown in figure 54. This circulation is not lossless: power is dissipated in MOSFETs, the resonant capacitor and the transformer. This, combined with the fact that under no-load condition the converter is usually running at its maximum frequency so that turn-off losses are significant, prevents the LLC resonant converter from achieving extremely low input power levels at no load. As a result, meeting the energy efficiency requirements that are specified in many applications (e.g., external power supplies) becomes unfeasible, unless appropriate countermeasures are taken.

Before exploring these possible countermeasures, it is worth mentioning another phenomenon that may heavily affect no-load operation. While normally the transferred power decreases as frequency increases (we remind that the converter is working in the inductive region), at light load from some frequency onward a frequency rise may cause a larger power to be transferred to the output. This reversal of the power-frequency connection is a showstopper for converter's operation because in a closed-loop regulated system the feedback loop turns from negative to positive causing the operating frequency to jump to the maximum programmed value and the output voltage to drift high until energy balance is found at some point.

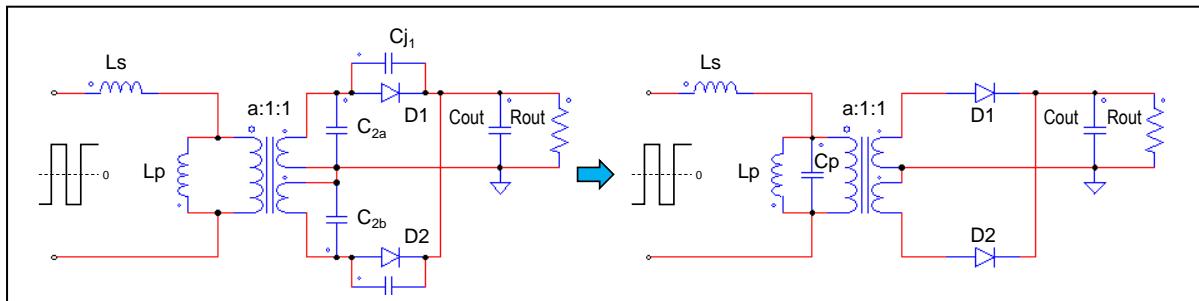
The root cause of this phenomenon, empirically defined as *feedback reversal*, is to be found in the parasitic components of the secondary side of the converter: specifically, the end-to-end capacitance of the transformer's secondary windings (the distributed capacitance existing between adjacent turns that appears in shunt with a winding) and the junction capacitance  $C_j$  (or the output capacitance  $C_{oss}$ ) of the secondary rectifiers.

These parasitic elements, illustrated in figure 57 (left-hand side) for the case of the center-tap full-wave rectification, have a limited impact at heavy and intermediate load, where they make secondary rectifier's turn-on no more exactly with ZCS, but may deeply affect the real-world converter's operation at light and very light load (DCMA, DCMAB and cutoff modes).

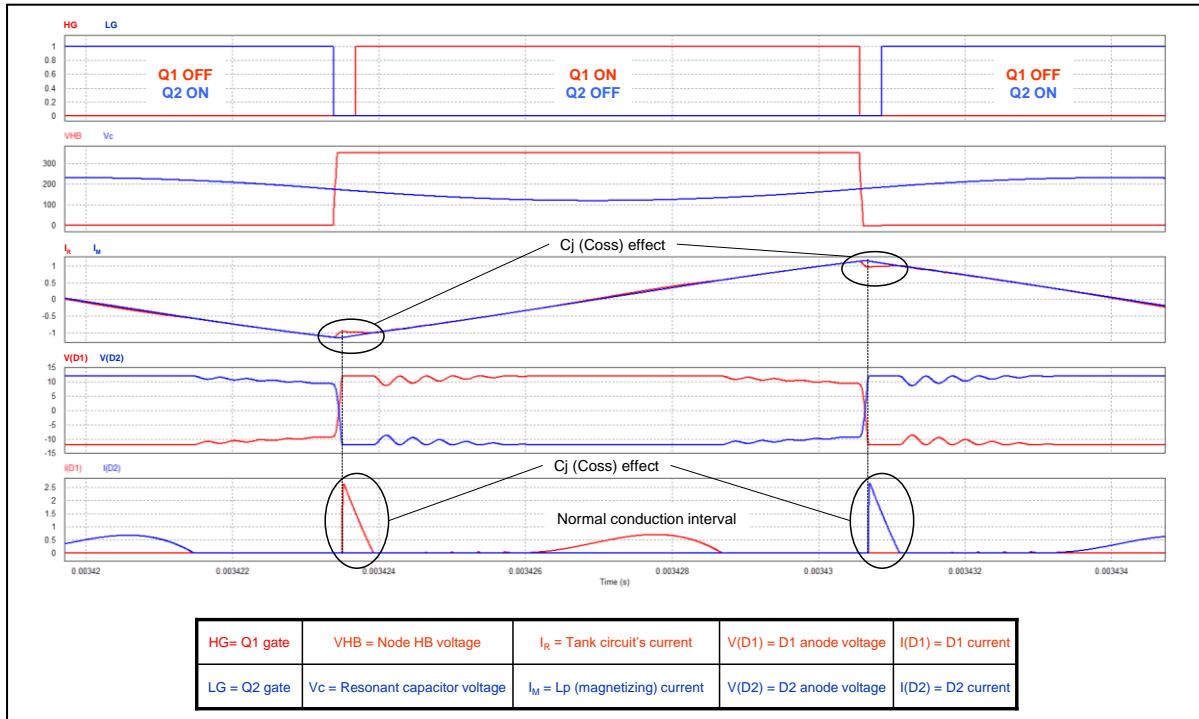
To facilitate the analysis, it is convenient to lump all the contributions into a single capacitor reflected to the primary side,  $C_p$ , that goes in parallel to  $L_p$ , as shown in figure 57 (right-hand side). Usually, unless the secondary windings have many turns (e.g. in high output voltage converters), the end-to-end capacitance of the secondary windings is much smaller than that of the rectifiers, therefore the characteristics of these components essentially determine the extent of the phenomenon.

Figure 58 shows the key waveforms of the converter operating below resonance in DCMAB mode at very light load. The effect of  $C_j$  ( $C_{oss}$ ) is pointed out on both the resonant tank current  $I_R$  and on the secondary currents  $I(D1)$  and  $I(D2)$ . The explanation of this effect can be described as follows.

**Figure 57. Transformer's and secondary rectifiers' parasitic capacitances lumped in a single capacitor  $C_p$  on the primary side.**



**Figure 58. Key waveforms showing  $C_j$  ( $C_{oss}$ ) effect in below resonance DCMAB mode.**



For example, considering the positive-going  $V_{HB}$  transition when Q2 turns off, the capacitor  $C_p$  in parallel to  $L_p$  delays the voltage change across  $L_p$  so that the  $V_{HB}$  transition initially falls mainly across  $L_s$ . Therefore, the current through  $L_p$ ,  $I_M$ , is little perturbed, while the current  $I_R$  rises quickly flowing through  $C_p$ .  $I_R$ , then, detaches from  $I_M$  and this goes on until  $C_p$  is charged to the point that the secondary voltage  $V(D1)$  - equal to  $1/a$  of the voltage across  $L_p$  - forward biases the secondary rectifier D1 and is clamped at  $V_{out} + V_{Rect}$ .

At this point, the voltage across  $L_p$  is fixed so that  $I_M$  ramps up with its slope  $a \cdot (V_{out} + V_{Rect}) / L_p$ , whereas  $I_R$  moves with a slope  $[V_{HB} - V_c - a \cdot (V_{out} + V_{Rect})] / L_s$ . In the example of figure 58 the slope of  $I_R$  is very small; thus  $I_R$  is almost constant and rejoins  $I_M$  after a short time (which is also marked by the oscillations on  $V(D1)$  due to the D1 no longer forward biased because the  $V(D1)$  generated by the normal energy transfer mechanism is still less than  $V_{out} + V_{Rect}$ ).

On the secondary side, the temporary detachment of  $I_R$  and  $I_M$  originated by the charge of  $C_p$  produces a sort of triangular current pulse that adds up to that produced by the normal energy transfer mechanism.

The same series of events, of course with everything mirrored, happen on the negative-going  $V_{HB}$  transition when Q1 turns off. As a result, in every switching half cycle there are two time intervals where current is output from the converter to the load. It is intuitive that even at cutoff, when the secondary current generated by the normal energy transfer mechanism disappears, these additional pulses are still there, carrying power from the input to the output proportionally to the switching frequency. This explains the feedback reversal phenomenon and makes real no-load operation impossible unless the residual load (e.g., the feedback circuitry, or a pre-load) consumes the power carried in this way, or some other countermeasure is provided.

An obvious possible way to mitigate the phenomenon is to reduce  $C_p$  (i.e.,  $C_i$  or  $C_{oss}$  contributions), but also slowing down the transitions of  $V_{HB}$  can help, because this reduces the current injection into  $C_p$  and the  $I_R - I_M$  detachment. This can be realized with the addition of an external capacitor connected between the node HB and ground. As a positive side effect, this will reduce the common-mode EMI emissions, but care must be taken not to lose ZVS.

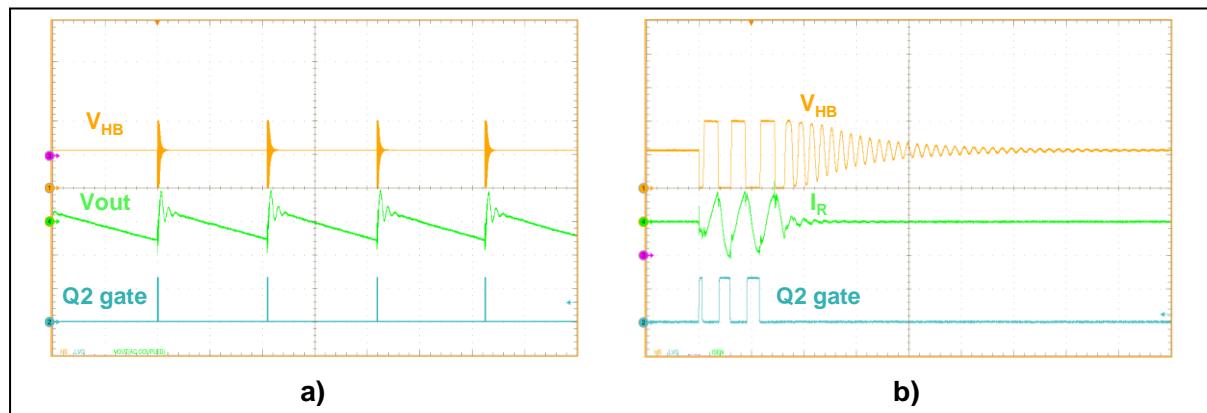
The feedback reversal phenomenon, here analyzed in the time domain, will be analyzed in the frequency domain in Part IV, Chapter 5.

The most effective way to reduce no-load consumption to a very low level as well as to prevent feedback reversal is to make the converter operate intermittently ("burst-mode" or "pulse-skipping" operation), with a series of a few switching cycles spaced out by long idle periods where both switches are OFF, as shown in the pictures of figure 59. In this way, the average switching frequency and associated losses are substantially reduced (down to few hundred hertz), and so do the average value of the residual tank current and associated losses.

Burst-mode operation can be realized in many ways. Whatever the implementation is, converter's stops and restarts must be done judiciously to prevent anomalous current peaks due to volt-second imbalance in transformer driving when switching restarts. By not doing so, since the repetition rate of bursts is well within the audible range, these current peaks might generate acoustic noise in the transformer, due to magnetostriction and electrodynamic forces in the windings and the core.

The other potential drawback of burst-mode operation is the increase of the output voltage ripple. In most cases, especially when the onset of burst-mode occurs at very light load, the resulting ripple is lower than the ripple at full load due in particular to the ESR of the output capacitors. For example, in the scope picture of figure 59 a) it is less than 40 mV peak-to-peak.

**Figure 59. Burst-mode operation: a) overall behavior; b) detail of a single burst.**



Normally, there is a trade-off between the various requirements: to minimize switching losses and conduction losses due to the residual tank current, the energy carried in each burst should be maximized so to have very few cycles in a burst and very long idle times between one burst and the other; however, this requires large peak currents during bursts, which causes a larger output voltage ripple and may easily result in unacceptable acoustic noise.

## Chapter 2

### Abnormal operating conditions and protection functions

The natural behavior of the LLC resonant converter under overload or short circuit conditions is intrinsically unsafe and so that the control must be complemented with adequate means to handle these conditions properly.

This jeopardy stems from two unfortunate facts. Firstly, as an overloaded LLC converter loses regulation and its output voltage drops, its power transfer capability increases. There is a lower voltage reflected across  $L_p$  so its current gets smaller and a larger portion of the primary current is transferred to the output. If operated at resonance, where the impedance of the  $L_s-C_r$  circuit is zero, the converter could theoretically provide even an infinite power. Secondly, the frequency  $f_{CM}$  that marks the boundary between capacitive and inductive mode increases with the load and may get very close to  $f_{R1}$  in case of short circuit. This makes type-2 hard switching nearly unavoidable if a converter designed to operate across  $f_{R1}$  is not equipped with appropriate protection functions.

This scenario can be analyzed with the equivalent schematic of the LLC converter under short circuit conditions shown in figure 60. The inductance  $L_p$  is actually shunted by an extremely low impedance, so it becomes “transparent”, and the LLC circuit reduces to a series LC circuit composed of  $C_r$  and  $L_s$ . The transformer will work as a “current transformer”, so that the output current will be  $\alpha$  times the entire primary (input) current  $i_{in}$ . It is intuitive that the impedance of the  $L_s-C_r$  resonant tank plays a key role.

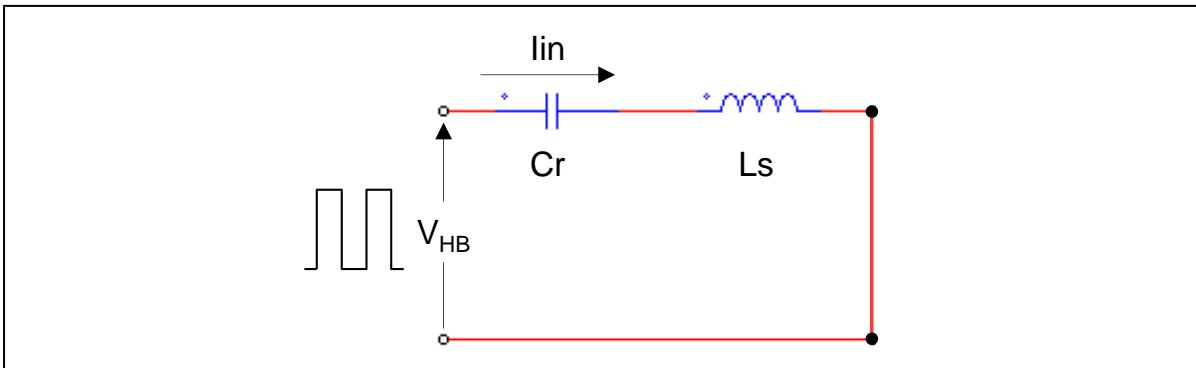
Two cases will be considered:

1. The converter always works above resonance (some means is provided by the control to bottom-limit the operating frequency at a value  $f_{min} > f_{R1}$ ). The control loop, in the attempt to keep the output voltage regulated will reduce the switching frequency down to the minimum value  $f_{min}$ . In this case the converter still operates in the inductive region (CCM sub-mode) and ZVS is ensured; however, the impedance of the  $L_s-C_r$  tank circuit can be very low and then the current  $i_{in}$  can reach very high values, the closer  $f_{min}$  to  $f_{R1}$  is, the lower the impedance and the higher the current will be.
2. The converter can operate below resonance (some means is provided to bottom-limit the operating frequency at a value  $f_{min}$  such that  $f_{CM} < f_{min} < f_{R1}$ ). Again, the control loop, in the attempt to keep the output voltage regulated will reduce the switching frequency to the minimum value  $f_{min}$ . In this case, the input current will be limited by the impedance of the  $L_s-C_r$  tank circuit.

However, increasing the load,  $f_{CM}$  increases and tends to  $f_{R1}$  under short circuit conditions, therefore the capacitive region is entered and ZVS is lost, with all the consequent troubles that were previously mentioned. The resulting waveforms will be similar to those shown in figure 52.

It is interesting to see what happens under short circuit if the converter is operating at resonance ( $f_{sw} = f_{R1}$ ). Theoretically, since tank circuit's impedance is zero, and then the short circuit is directly connected across the input source, the converter should be able to keep the output voltage unchanged whatever current the load demands (the system is working in the load-independent point).

**Figure 60. LLC circuit equivalent schematic under short circuit conditions.**



In real-world operation,  $I_{in}$ , though reaching very high values, will be limited by the parasitic resistance of the short-circuit mesh, the ESR of  $C_r$  and by transformer's non-idealities. Also, the input source will have a finite impedance and a finite power capability. Additionally, the drop across the secondary rectifiers does not reflect a true short circuit on the primary side. Because of the parasitic resistances, the output voltage will drop, and the control loop will react pushing the operating frequency to the minimum  $f_{min}$ , which must be lower than  $f_{R1}$  since we were assuming that the converter was operating at  $f_{R1}$ . In the end this will fall into case 2.

From the above analysis it is possible to draw the following conclusions:

1. Two major issues arise under overload or short circuit conditions: very high current levels, and capacitive mode operation with type-2 hard switching. This makes the operation of the LLC resonant converter under overload or short circuit inherently unsafe if no overload/short circuit protection (OL-SCP) is used, just like in conventional PWM-controlled converters. OL-SCP will have to prevent not only the tank current from exceeding unsafe values but also ZVS from being lost.
2. Limiting the minimum operating frequency of the converter is not always effective. It prevents from losing ZVS under overload or short circuit only if this minimum value is above the resonant frequency  $f_{R1}$ . Thereby, relying on just limiting the minimum operating frequency would force to give up the below-resonance operating region and its interesting properties, severely limiting the usability range of the converter. Further, the problem of having too high circulating current would be still unsolved.
3. Converters are often specified to have peak load demands that are considerably higher than the maximum continuous power, and whose duration is such that it cannot be averaged by the output capacitor bank. While these peak loads may be thermally irrelevant, from the electrical standpoint they must be considered as a steady state; then, the OL-SCP circuits must not be triggered but the converter must be designed so that the conditions for ZVS are not violated under these transient conditions as well.

Inspecting the waveforms under heavy load conditions one can realize that that, unlike PWM-controlled converters, the peak current in a switching cycle is not reached at the end of the conduction time of either MOSFET. This suggests that the usual cycle-by-cycle peak current limitation so widely used in PWM-controlled converters is not applicable to LLC resonant converters.

Additionally, peak current limitation would turn the converter into a peak-current-mode-controlled one, which is unstable at 50% duty cycle with any CCM operation.

The simplest and also most immediate action to take in response to the detection of an overload or short circuit condition is to increase the operating frequency. It is advantageous to push the frequency well above the resonance frequency  $f_{R1}$ , to ensure that the converter operates in the inductive region: ZVS is maintained, and the input current is under control by the inductive reactance of the tank circuit to a level just below the overload detection threshold.

However, this frequency rise is not typically sufficient to effectively limit the short-circuit output current at safe values. In fact, on the one hand, the input impedance of the tank circuit in the inductive region is essentially proportional to frequency; since there are practical limits on the maximum operating frequency (it rarely exceeds 3-4 times  $f_{R1}$ ), the short circuit tank current can still be considerably large.

On the other hand, as previously mentioned, when the output voltage drops because of the action of the OL-SCP circuits, more of the primary current is transferred to the output. As a consequence, the short circuit output current can be still much higher than the nominal full-load current and the resulting stress, especially for the secondary rectifiers, might be unacceptable.

The OL-SCP circuit, in addition to limiting the tank current should provide some timed shutdown protection that either forces the converter to operate intermittently with a low repetition rate to, drastically reduce the average output current to thermally insignificant values, or latches it off if the OL-SCP circuits are active for more than some time.

These countermeasures (overcurrent limitation through forced frequency rise and intermittent operation or latch off) provide a good coverage but still require a restrictive design of the LLC tank: they ensure ZVS during steady-state operation under overload or short circuit conditions but do not ensure that ZVS occurs during the transient following the application of the overload or short circuit. In other words: ZVS is ensured statically but not dynamically.

This can be clarified as follows. When an overload or a short circuit is applied to the converter its load has a sudden increase and the control loop will react reducing the switching frequency  $f_{sw}$  to keep the output voltage regulated. The OL-SCP circuits will be triggered once  $f_{sw}$  is at the point that the tank current is large enough for the overload to be detected. While  $f_{sw}$  is dropping  $f_{CM}$  is rising, and if they cross each other before the OL-SCP circuit detects the overload and pushes frequency up, for some time ZVS is lost and hard switching occurs.

Working for a limited time with type-1 hard switching might not be a problem but, unfortunately, the potential risks of type-2 hard switching are such that even few switching cycles (some claim even a single cycle [23]) can produce a catastrophic failure of the primary switches. This risk can be mitigated by using MOSFETs with fast-recovery body diodes, relying on their greater robustness [23].

Without a protection that specifically addresses this issue the only way to prevent this temporary loss of ZVS is to design the LLC tank so that in the worst case  $f_{sw}$  never gets too close to  $f_{CM}$ . From a different angle, this means that under normal operating conditions its phase-shift  $\phi$  must be large enough to never fall to zero even temporarily during a short circuit.

As a consequence, the design cannot be optimized in terms of per-cycle energy returned to the input source or, equivalently, reactive energy. This goes to the detriment of efficiency, especially at medium and light load, where reactive energy is comparable to active energy.

For these reasons it is recommended that the OL-SCP circuits monitor the tank current not only to detect an excessive tank current but also to make sure that its zero-crossings always occur after the  $V_{HB}$  transitions and after the dead-time is over. As just stated, the task of the OL-SCP circuits seems overspecified (if the tank current crosses zero after the dead-

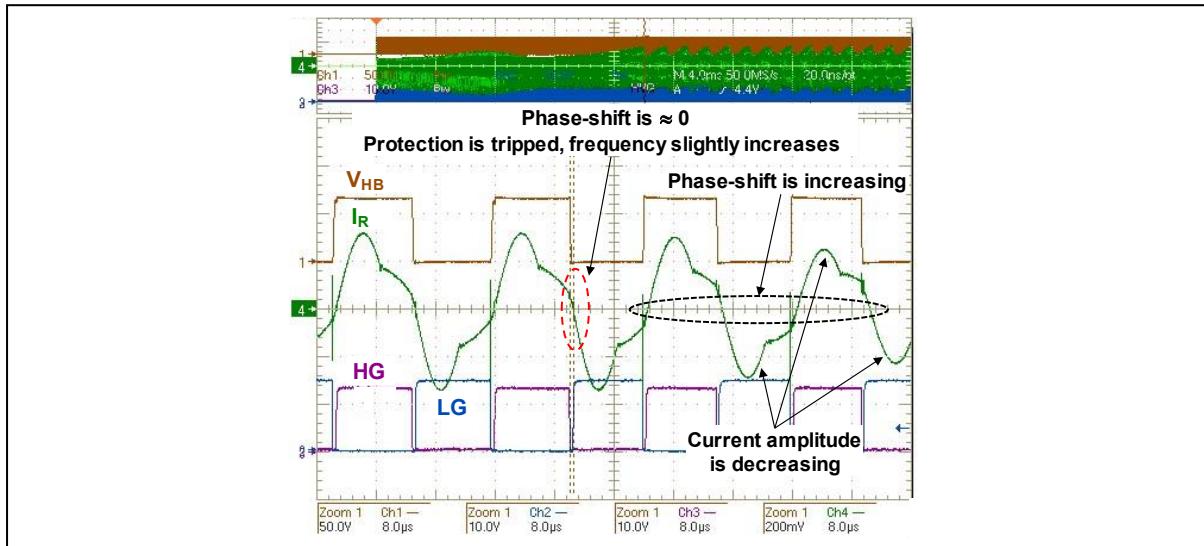
time it will occur after the  $V_{HB}$  transition...). Actually, it is not and to show that we will consider two different operating scenarios.

The first scenario includes peak loading, overload, or input undervoltage. In this case the phase-shift  $\varphi$  of the tank current normally takes a few switching cycles to reverse from positive (lagging) to negative (leading), i.e., the zero-crossings of the tank current gradually get nearer in time to the  $V_{HB}$  transitions until they overlap and then reverse their position.

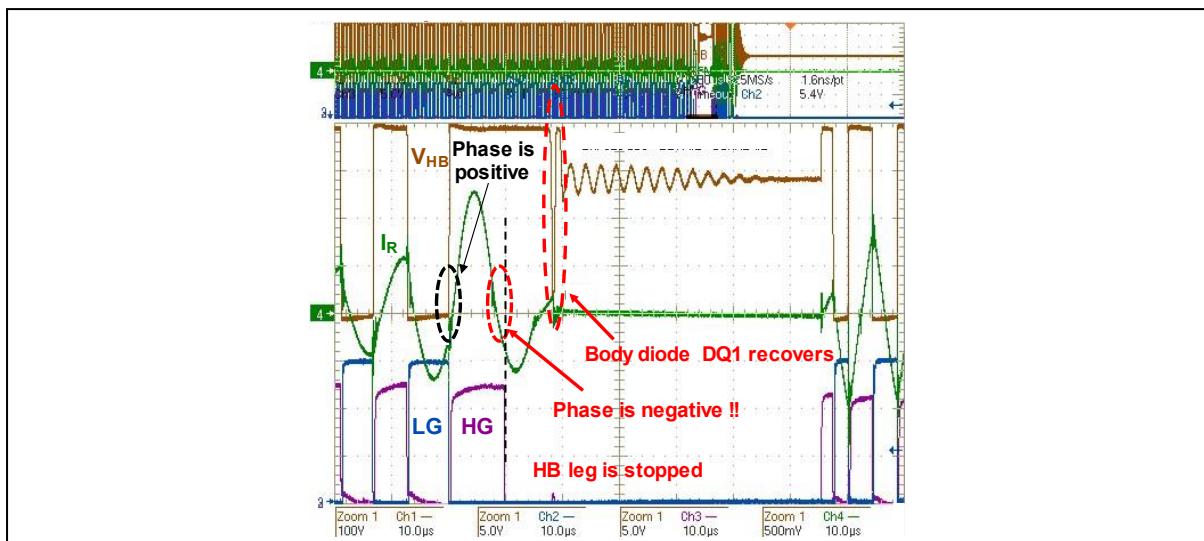
This situation can be detected, for example, by opening a time window after the turn-off of either MOSFET or after the dead-time end; if the tank current crosses zero within that window it is assumed that the phase-shift is getting too close to zero. The corrective action can be to force the operating frequency to increase, to push the phase-shift back to more positive values. This is shown in the picture of figure 61.

The second scenario includes output short-circuit or failure of one or both secondary rectifiers. In this case the perturbation induced in the tank current can be so large that the phase-shift reverses abruptly, even in the same switching half-cycle as shown in figure 62.

**Figure 61. Impending capacitive mode due to overload trips the relevant protection.**



**Figure 62. Abrupt capacitive mode due to short circuit: phase-shift reverses within the HG half-cycle.**



In figure 62 we can see that the tank current initially increases slightly during the LG half-cycle, and then during the subsequent HG half-cycle it crosses zero still after the  $V_{HB}$  transition (positive phase-shift) but after a high peak it crosses again zero and becomes negative before HG goes low (negative phase-shift). Of course, this behavior can easily bypass the detection method previously described (and maybe also the corrective action is inadequate), therefore it needs different detection method and corrective action.

Notice that the MOSFET that is currently on (Q1, since HG is high, in the case of figure 62) can be switched off with no issue: as previously observed, its turn-off occurs with ZVS. Type-2 hard switching is prevented by simply not turning on the other MOSFET in the half-cycle next to the detection, as shown in figure 62.

This abrupt phase reversal can be detected, for example, by monitoring the sign of the tank current at the beginning and the end of the dead-time (reminder: the tank current must cross zero after the end of the dead-time); in case either of the two checks results in a wrong sign, the MOSFET supposed to be turned on next stays off.

With this protection scheme the converter is also temporarily stopped as a precautionary measure to let the tank current decay to zero, and then restarted at a higher frequency to make sure that it works in the inductive region. This corrective action is quite sharp and a milder action, still able to prevent type-2 hard switching, might be preferred in some cases: for example, just stopping the converter until the tank current has the right sign. A type-1 hard switching would likely occur because the tank current becomes small, but a few cycles of type-1 hard switching are acceptable. The other functions of the OL-SCP would complete the job.

It is interesting to notice in figure 62 that after the negative portion of  $I_R$  following the turn-off of Q1 (HG going low), the tank current becomes positive while  $V_{HB}$  is still high and both MOSFET are off. This current is flowing through the body diode DQ1, from the cathode to the anode, and is wiping out its reverse recovery charge  $Q_{rr}$ . As DQ1 recovers and its current drops to zero with a  $dI/dt$  depending on its recovery characteristics,  $V_{HB}$  bounces and finally the half bridge leg exhibits a high impedance. It is clear that if Q2 had been turned on while DQ1 was recovering the half bridge leg would have been a low impedance connected across the input voltage until the recovery had been over (shoot-through).

This protection against type-2 hard switching is commonly referred to as *anti-capacitive protection* (ACP) or *hard switching prevention* (HSP) function.

As a conclusion, capacitive-mode operation and the resulting type-2 hard switching are avoided with a careful design of the LLC tank that also takes the tolerance of its components into consideration. If the OL-SCP function includes the ACP function the design can be carried out considering only the normal operating range (including, in case, peak loading). If the ACP function is not available, also input undervoltage, overload and short circuit conditions must be considered.

## Chapter 3

### Start-up of the LLC resonant converter

Like in all converters, start-up is quite a critical phase that needs to be properly handled. In fact, normally at start-up the output capacitors are discharged, so this phase can be regarded as a sort of virtual short circuit. When the converter is first switched on (or also while it is restarting, e.g., after being shut down temporarily by a protection) the energy flow should be progressively increased to allow a gradual buildup in output current and voltage. This is commonly realized via the so-called *soft-start* function.

In the LLC converter soft-start is realized by forcing an initial switching frequency higher than the resonance frequency  $f_{R1}$ , so that the converter operates in the inductive region and the input current is limited by the inductive reactance of the tank circuit. Then the frequency is allowed to progressively decay until the output voltage reaches the regulation setpoint and the control loop takes over.

In order for this approach to be effective the initial frequency needs to be at least 3-4 times higher than  $f_{R1}$ , which could be an issue in a high frequency design. The so-called PWM-PFM hybrid modulation method proposed in [24], where pulse-width modulation (PWM) is combined to frequency modulation (PFM), enables a start-up with an initial frequency less than 50% higher than  $f_{R1}$ , while keeping the initial current low.

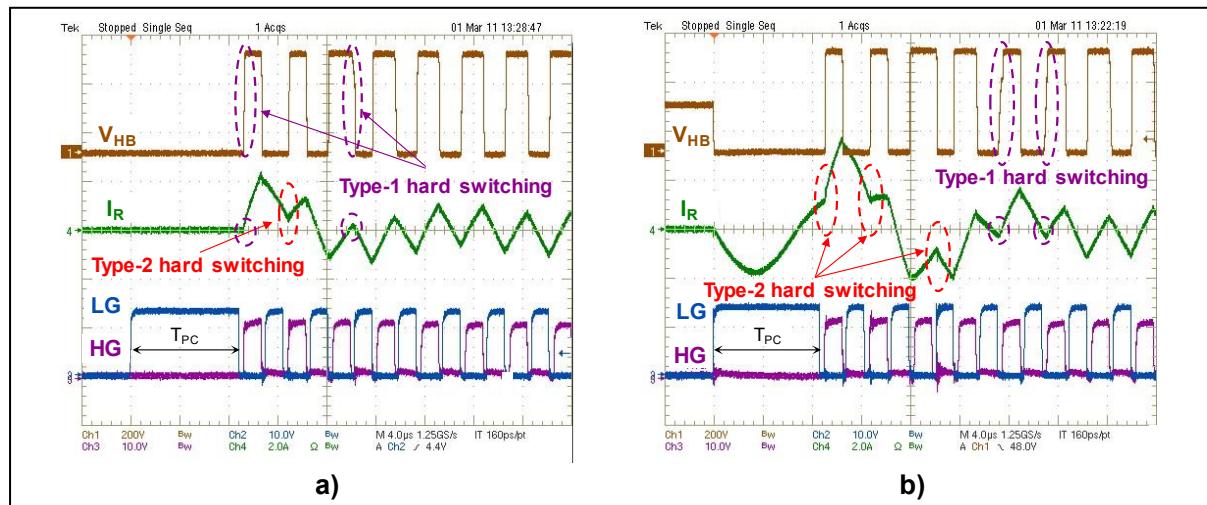
Coming back to the traditional PFM soft-start, figure 63 shows some typical waveforms at start-up of a half bridge converter under two different initial conditions:

- with the resonant capacitor  $C_r$  totally discharged (for example, in case of a cold start);
- with  $C_r$  initially charged (for example, in case of a fast off-on or a restart after a fault).

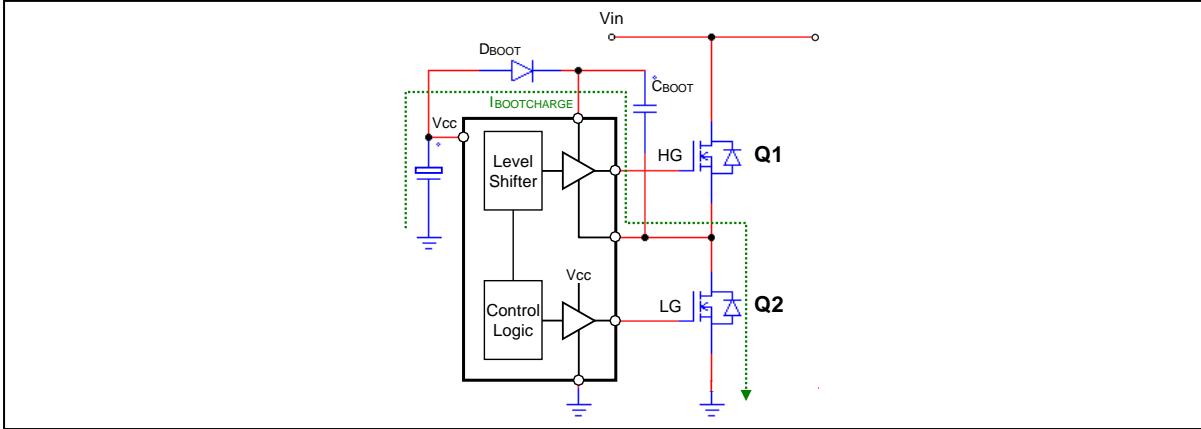
The voltage  $V_C$  across  $C_r$  is not shown but can be inferred from the initial value of  $V_{HB}$ , which equals  $V_C$  before the switching activity starts.

Before analyzing these two cases, it is worth pointing out a characteristic, visible in figure 63, that is common to essentially all high-voltage resonant controller ICs that use the bootstrap approach to supply the driver of the high-side MOSFET Q1 as illustrated in figure 64.

**Figure 63. Main waveforms of a half bridge converter at start-up: a) with  $C_r$  initially discharged, b) with  $C_r$  initially charged.**



**Figure 64. Bootstrap approach for high-side driving and  $C_{BOOT}$  charge path.**



These devices usually start switching by turning on the low-side MOSFET Q2 for a preset time  $T_{PC}$  (in the  $\mu\text{s}$ ) to pre-charge the bootstrap capacitor  $C_{BOOT}$  that supplies the floating driver of Q1 via the bootstrap diode  $D_{BOOT}$  and ensure proper driving of Q1 since the first cycle.

Considering case a), the very first turn-on of the high-side MOSFET Q1 is with type-1 hard switching. If the gate-drive circuitry is properly designed to prevent  $\text{dv}/\text{dt}$ -induced turn-on of Q2 this probably inevitable hard switching is of no concern. In the subsequent cycles it is possible to observe both a type-2 hard switching and another type-1 hard switching, despite the converter is definitely working in the inductive region, as testified by the triangular shape of the tank current once it stabilizes after the initial perturbation.

Once again, that of inductive region is a static concept i.e., related to steady-state operation, whereas start-up is a dynamic situation where the converter works under rapidly changing conditions that are far away from those of the steady state. Specifically, in steady state the voltage  $V_C$  across the resonant capacitor  $C_r$  has a dc component equal to  $V_{in}/2$  and the inductive section of the LLC tank is symmetrically driven ( $\pm V_{in}/2$ ). At start-up, it takes some time for the dc component of  $V_C$  to go from zero to  $V_{in}/2$  and, during this transient, the inductive section of the LLC tank is not driven symmetrically. The volt·second product in two consecutive half-cycles is imbalanced and if this imbalance is large enough, the current may not reverse in a half-cycle, as happens at the end of the first switching cycle in figure 63 a). As a result, one MOSFET (Q1) is turned on while the body diode of the other one (DQ2) is conducting and undergoes a type-2 hard switching.

This phenomenon is known as *transformer flux imbalance* or *flux doubling* and affects half-bridge and push-pull topologies. In LLC converters this start-up issue is the only negative consequence of flux doubling thanks to the series resonant inductor  $L_s$ ; in push-pull topologies or traditional PWM-controlled half-bridge converters, it represents a possible transformer saturation hazard that often leads to catastrophic failures.

The case b) in figure 63, related to an initially charged  $C_r$ , is even worse. After the initial turn-on of Q2 to pre-charge  $C_{BOOT}$ ,  $C_r$  gets discharged and  $V_C$  starts from zero like in case a) but, unlike case a) where the initial tank current was zero, here the initial current is nonzero and is ringing at a frequency  $f = f_{R1}$  because the energy initially stored in  $C_r$  is being exchanged with  $L_s$  ( $L_p$  is shunted, being zero the initial  $V_{out}$ ). If the pre-charge time  $T_{PC}$  is such that:

$$\frac{2k+1}{2f_{R1}} < T_{PC} < \frac{k+1}{f_{R1}}, \quad k = 0, 1, \dots, \quad (47)$$

like in case b), a nonzero initial voltage on  $C_r$  causes a type-2 hard switching the very first time the high-side MOSFET Q1 turns on and a perturbation so large that there are other cycles

with type-2 hard switching, followed by some cycles with type-1 hard switching when the perturbation is settling.

To have the first turn-on of Q2 with ZVS and prevent most of the subsequent hard switching cycles the pre-charge time should be such that:

$$\frac{k}{f_{R1}} < T_{PC} < \frac{2k+1}{2f_{R1}}, \quad k = 0, 1, \dots . \quad (48)$$

However, it is not always possible to meet this condition: the choice of  $f_{R1}$  is often dictated by other specifications or criteria and, on the other hand, normally  $T_{PC}$  is internally fixed and not tightly controlled.

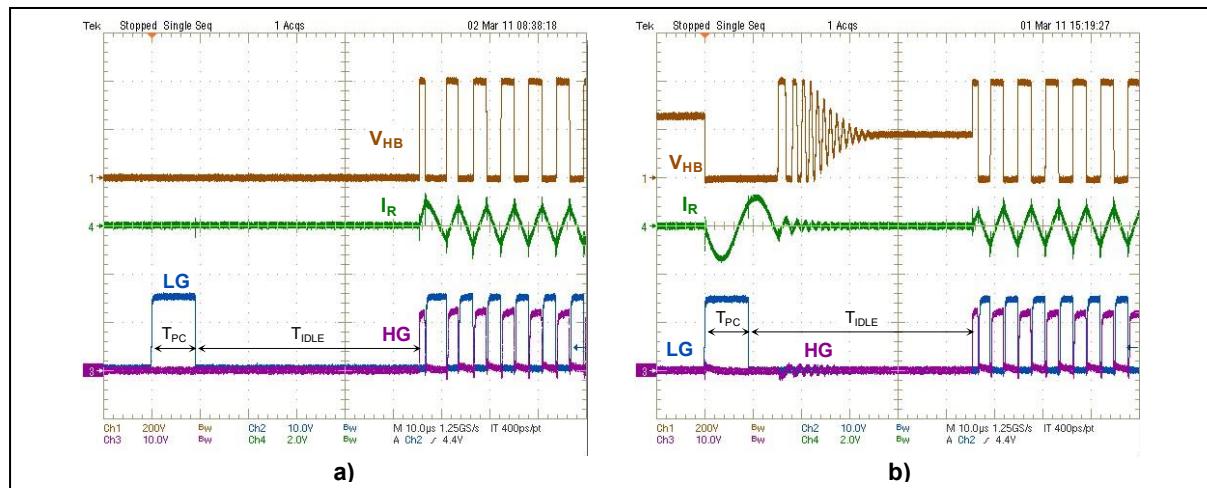
A possible solution to this issue is the *safe-start* procedure proposed in [25] and illustrated in the pictures of figure 65. It effectively complements soft-start, taking care of the initial cycles where soft-start is ineffective to prevent type-2 hard switching.

The cycles with type-2 hard switching occurring when the initial voltage on  $C_r$  differs from  $V_{in}/2$  can be prevented by synchronizing  $V_{HB}$  to the zero-crossings of the tank current during the initial cycles. In this way current reversal in every switching half-cycle and then ZVS are ensured as shown in figure 65a). Indirectly, the initial volt-second imbalance is nearly eliminated because this synchronization makes the initial duty cycle of  $V_{HB}$  less than 50%.

The type-2 hard switching consequent to a non-zero initial voltage on the resonant capacitor  $C_r$  and an unfortunate  $T_{PC}$  -  $f_{R1}$  combination can be prevented by keeping both MOSFETs off for a time  $T_{IDLE}$  immediately following  $T_{PC}$  before starting the normal switching activity as shown in figure 65 b). Normally an idle time  $T_{IDLE}$  in the ten  $\mu s$  is long enough to let the tank current fade out without significantly discharging the bootstrap capacitor.

The full bridge configuration is only slightly less problematic than the half bridge. In case of start-up with a discharged  $C_r$  the initial condition is equal to the steady-state condition thus there is little or no volt-second imbalance and type-2 hard switching does not occur. Type-1 hard switching is seldom observed too. A pre-charged  $C_r$ , instead, may generate the same issues seen in the half bridge depending on the direction of the ringing current when there is the first turn-on of the Q1-Q3 diagonal. The safe-start procedure shown in figure 65 can effectively eliminate any risk of type-2 hard switching also in the full bridge.

**Figure 65. Main waveforms of a half bridge converter at start-up with safe-start: a) with  $C_r$  initially discharged, b) with  $C_r$  initially charged.**



## LLC RESONANT CONVERTER OVERVIEW: SUMMARY

To conclude this part, it is useful to recap the takeaways of the discussion.

- The LLC resonant converter provides the following benefits:
  - Soft switching of all semiconductor devices (ZVS at turn-on for primary switches, ZCS at both turn-on and turn-off of secondary rectifiers)
  - Ability to accommodate 0-100% load range with a limited frequency range
  - Magnetic integration
    - Series inductor, parallel inductor and transformer can be combined into a single physical device
  - Smooth waveforms
    - Piecewise sinusoidal primary and secondary currents with no steep edges
    - Voltage square wave  $V_{HB}$  with not too high  $dv/dt$ 
      - The  $dv/dt$  of  $V_{HB}$  can be reduced by adding extra capacitance  $C_{HB}$  with essentially no impact on efficiency thanks to ZVS.
      - Low EMI emissions, relatively loose filtering requirements
  - Enables high-efficiency, high power density designs
- The LLC resonant converter features the following drawbacks:
  - High current ripple on secondary side requires low-ESR capacitors
    - Stress is however much lower than in flyback converters
  - Variable operating frequency might not be acceptable in some contexts
  - Works satisfactorily if input-to-output voltage conversion ratio is limited
    - In case of offline PSUs, in most cases it works with a PFC front-end; without PFC with a single mains input, rarely with a wide-range input because performance is severely degraded.
- The most significant facts concerning LLC resonant converter design are:
  - Operation at, above or below resonance depends essentially on input voltage, output voltage and transformer's turn ratio. Load dependence is weak, essentially due to the voltage drop across the resistive elements in the power circuit.
  - Operation at resonance looks to be the preferred operating point: it provides ideally perfect load regulation, sinusoidal current, optimum peak-to-dc ratio.
    - Sensible design strategy: design the converter to work at resonance at the nominal input voltage, use below resonance operation to handle the lower section of the input voltage range and above resonance operation to handle the upper section of the input voltage range.
  - No-load operation with ZVS is enabled by transformer magnetizing inductance
    - Its value is a trade-off between ZVS ability, switching losses at full-load, part-load efficiency, and input consumption at no-load.
  - Soft-start, overcurrent and short circuit protection must be provided
    - Avoiding excessive tank currents and capacitive-mode operation is a must.

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# **PART IV**

## **LLC CONVERTER LARGE-SIGNAL MODELING AND DESIGN**

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### **Chapter 1**

#### **Modeling approaches**

The purpose of the following discussion is to provide a detailed quantitative analysis of the steady-state operation of the LLC converter that can be easily translated into a design procedure able to meet, or get as close as possible to, the targets that here we recap for reader's convenience:

- The converter must work in the inductive region to ensure ZVS for the primary switches under all the specified operating conditions (that may include even no-load conditions).
- Depending on the available protection functions, one will need to consider also the abnormal operating conditions, such as overload, short circuit, or input undervoltage, as well as dynamic conditions, not only steady state.
- The above points should be addressed keeping the amount of reactive energy that circulates in the tank circuit at a minimum. This will minimize the associated conduction losses and help keep efficiency high as the load is reduced.

There are two fundamental approaches to the large-signal analysis and modeling of resonant converters:

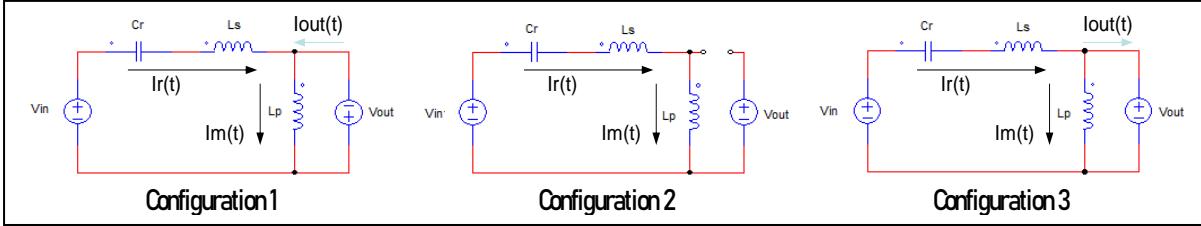
- Time domain analysis (TDA). It is based on finding the time domain solutions to the state equations of each of its possible circuital configurations, determining which sequence of configurations occur in a switching cycle for given input voltage, output voltage and load conditions and extracting the timing and electrical quantities.
- Frequency domain analysis (First-Harmonic Approximation, FHA). Based on the selective properties of resonant circuits, it assumes that the input-to-output power flow is essentially due to the fundamental components of currents and voltages. It enables the usage of the classical ac circuit analysis.

In the following discussion the TDA approach will be briefly reviewed, and the FHA approach treated in depth from a design-oriented angle. Finally, a simplified TDA-based design procedure will be provided to complement and compensate the shortcomings of the FHA approach.

##### *Brief review of TDA approach*

In the literature it is possible to find several works on the analysis of LLC converters based on various types TDA methodologies (state-variable, cycle-averaging, variable structure, etc.). References [26]-[32] are just some examples of a much broader production. They are all based on representing the system in the time domain.

**Figure 66. Possible circuital configurations of the LLC tank in a half switching cycle.**



The LLC converter has six possible circuital configurations in a switching cycle. Owing to symmetry, one can consider a half switching cycle and then only three of them are needed to completely characterize the steady-state operation, as shown in figure 66. Notice that not all these configurations necessarily appear in the operating sequence.

With a given set of ( $a$ ,  $L_s$ ,  $L_p$ ,  $C_r$ ) values and for given input voltage, output voltage and load conditions, a TDA algorithm determines which of the six (seven if we include capacitive-mode operation and CCMB) operating modes listed in figure 35 applies. Then it solves the differential equations related to the corresponding sequence of circuit configurations using an iterative method (not in all the operating modes a closed-form solution exists) and determines the boundaries that mark the transition from one configuration to the other.

Essentially, a TDA algorithm reconstructs the exact waveforms of voltages and currents in the power circuit. From these, it is possible to extract all the data of interest such as their dc, rms and peak values, the operating frequency, the current-voltage phase-shift, etc.

Repeating this process for different input and output voltages and loads, it is possible to build plots that show how these quantities of interest change with the operating conditions and assess what the worst-case conditions for the design are. Further, changing the set of ( $a$ ,  $L_s$ ,  $L_p$ ,  $C_r$ ) values it is possible to assess the effect of the tolerance in the component values and even compare different designs to find the optimum one for the assigned specifications.

Clearly, TDA is a CAD procedure: extensive calculations are involved, and appropriate SW and HW tools are needed. The return is anyway rewarding: TDA provides accurate results throughout all operating modes, the multi-resonant nature of the LLC tank appears clearly and its impact on converter operation is described faithfully. TDA, though, does not generally allow a handy design procedure that, starting from the electrical specification, leads to the definition of the values of the set ( $a$ ,  $L_s$ ,  $L_p$ ,  $C_r$ ). There is one exception to that, which will be discussed later.

#### Fundamentals of FHA approach

As previously stated, the physical justification for the FHA approach, first proposed by Steigerwald in [8] and thoroughly discussed in the literature (e.g. [33]-[35]), lies in the selective nature of tank circuits. It assumes that the power transfer from the source to the load through the resonant tank is almost completely associated to the fundamental harmonic of the Fourier expansion of the currents and voltages involved. The harmonics of the switching frequency are then neglected, and the tank waveforms are assumed to be purely sinusoidal at the fundamental frequency: this approach gives quite accurate results for operating points at and around the resonance frequency  $f_{R1}$  in CCM mode, while it is less accurate, but still enough to make some sensible design considerations, at frequencies below  $f_{R1}$  or at light load, when the system works in a DCM mode.

With FHA many details of circuit operation on a switching cycle time base are lost, like the dead-times and the  $V_{HB}$  transitions, or the multi-resonant nature of the LLC tank with its

implications in the below resonance region. However, since the standard ac analysis can be used and the involved calculations are by far fewer, a calculation tool, though convenient, is not essential. What is more, based on FHA it is possible to find a handy design procedure that, starting from electrical spec, leads to the definition of the tank's parameter ( $a$ ,  $L_s$ ,  $L_p$ ,  $C_r$ ).

Let us refer to the LLC resonant half bridge converter in figure 67 and consider the simple case of ideal components, both active and passive.

The CSN provides a square wave input voltage  $v_{HB}(t)$  at a frequency  $f_{sw}$  to the resonant tank, which can be expanded in Fourier series:

$$v_{HB}(t) = \begin{cases} \frac{V_{in}}{2} + \frac{2}{\pi} V_{in} \sum_{j=1,3,5,\dots} \frac{1}{j} \sin(j 2\pi f_{sw} t) & (\text{HB}) \\ \frac{4}{\pi} V_{in} \sum_{j=1,3,5,\dots} \frac{1}{j} \sin(j 2\pi f_{sw} t) & (\text{FB}) \end{cases}. \quad (49)$$

The fundamental component  $v_{HB1}(t)$ , in phase with the original square wave, is:

$$v_{HB1}(t) = \begin{cases} \frac{2}{\pi} V_{in} \sin 2\pi f_{sw} t & (\text{HB}) \\ \frac{4}{\pi} V_{in} \sin 2\pi f_{sw} t & (\text{FB}) \end{cases}, \quad (50)$$

whose peak value  $V_{HB1pk}$  and rms value  $V_{HB1}$  are respectively:

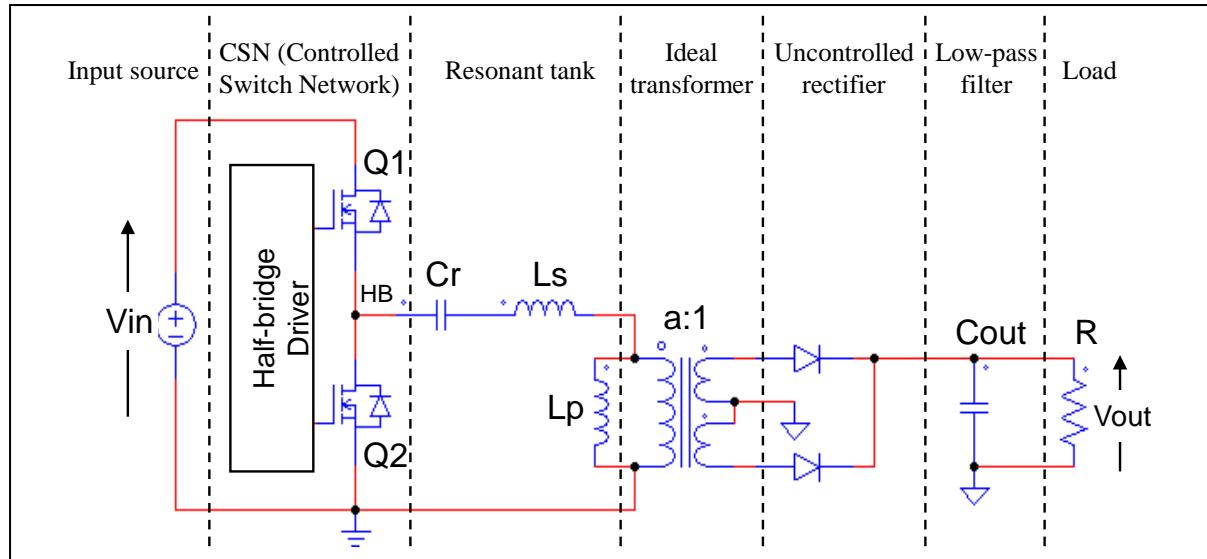
$$V_{HB1pk} = \begin{cases} \frac{2}{\pi} V_{in} & (\text{HB}) \\ \frac{4}{\pi} V_{in} & (\text{FB}) \end{cases}; \quad V_{HB1} = \begin{cases} \frac{\sqrt{2}}{\pi} V_{in} & (\text{HB}) \\ \frac{2\sqrt{2}}{\pi} V_{in} & (\text{FB}) \end{cases}. \quad (51)$$

As a consequence of the above-mentioned assumptions, the resonant tank current  $i_{R1}(t)$  will be also sinusoidal, with a certain rms value  $I_{R1}$  and a phase-shift  $\varphi$  with respect to the fundamental component of the input voltage:

$$i_{R1}(t) = \sqrt{2} I_{R1} \sin(2\pi f_{sw} t - \varphi) = \sqrt{2} I_{R1} [\cos \varphi \sin 2\pi f_{sw} t - \sin \varphi \cos 2\pi f_{sw} t]. \quad (52)$$

This current  $i_{R1}(t)$  lags ( $\varphi > 0$ ) or leads ( $\varphi < 0$ ) the voltage  $v_{HB1}(t)$ , depending on whether the inductive reactance or the capacitive reactance dominates in the behavior of the resonant tank at  $f = f_{sw}$ . Regardless of that,  $i_{R1}(t)$  can be expressed as the sum of two contributes, the first in phase with  $v_{HB1}(t)$ , the second in quadrature with  $v_{HB1}(t)$ .

**Figure 67. LLC resonant half bridge functional blocks.**



The dc input current  $I_{in dc}$  that the converter draws from the input source can be found as the average value over a switching period  $T_{sw} = 1/f_{sw}$  of the sinusoidal tank current flowing during the conduction period of the high side MOSFET in the half-bridge (i.e., when the dc input voltage is applied to the LLC tank); of course, in the full bridge the dc input current will be twice as much:

$$I_{in} = \begin{cases} \frac{1}{T_{sw}} \int_0^{T_{sw}/2} i_{R1}(t) dt = \frac{\sqrt{2}}{\pi} I_{R1} \cos \varphi & (\text{HB}) \\ \frac{2}{T_{sw}} \int_0^{T_{sw}/2} i_{R1}(t) dt = \frac{2\sqrt{2}}{\pi} I_{R1} \cos \varphi & (\text{FB}) \end{cases} . \quad (53)$$

The real power  $P_{in}$ , drawn from the input source can now be calculated as either the product of the input dc voltage  $V_{in}$  times the average input current  $I_{in}$  or, equivalently, the product of the rms values of voltage and current first harmonic, times  $\cos \varphi$ :

$$P_{in} = V_{in} I_{in} = V_{HB1} I_{R1} \cos \varphi = \begin{cases} \frac{\sqrt{2}}{\pi} V_{in} I_{R1} \cos \varphi & (\text{HB}) \\ \frac{2\sqrt{2}}{\pi} V_{in} I_{R1} \cos \varphi & (\text{FB}) \end{cases} . \quad (54)$$

Let now us consider the output rectifiers and the low-pass filter. In the real circuit, the rectifiers are driven by a quasi-sinusoidal current and the voltage reverses when this current becomes zero; therefore, the voltage at the input of the rectifier block is an alternate square wave  $v_{sec}(t)$  with an amplitude  $\pm(V_{out} + V_{Rect})$  in phase with the rectifier current.

The Fourier expansion of the square wave output voltage  $v_{sec}(t)$  is:

$$v_{sec}(t) = \frac{4}{\pi} (V_{out} + V_{Rect}) \sum_{j=1,3,5,\dots} \frac{1}{j} \sin(j 2\pi f_{sw} t - \psi) , \quad (55)$$

where  $\psi$  is the phase shift with respect to the input voltage. The fundamental component of  $v_{sec}(t)$  is:

$$v_{sec1}(t) = \frac{4}{\pi} (V_{out} + V_{Rect}) \sin(j 2\pi f_{sw} t - \psi) , \quad (56)$$

whose rms amplitude is:

$$V_{sec1} = \frac{2\sqrt{2}}{\pi} (V_{out} + V_{Rect}) . \quad (57)$$

Similarly, the fundamental component of the secondary current  $i_{sec}(t)$  will be:

$$i_{sec1}(t) = \sqrt{2} I_{sec1} \sin(j 2\pi f_{sw} t - \psi) , \quad (58)$$

where  $I_{sec1}$  is its rms value. Now we can relate the dc output current  $I_{out}$ , i.e., the average secondary-side current, to the load:

$$I_{out} = \frac{2}{T_{sw}} \int_0^{T_{sw}/2} |i_{sec1}(t)| dt = \frac{2\sqrt{2}}{\pi} I_{sec1} = \frac{P_{out}}{V_{out}} = \frac{V_{out}}{R_{out}} , \quad (59)$$

where  $P_{out}$  is the output power associated to the output load resistance  $R_{out}$ . It is also possible to derive the ac current  $I_{sec.ac}$  flowing into the output capacitor that makes up the low-pass filter:

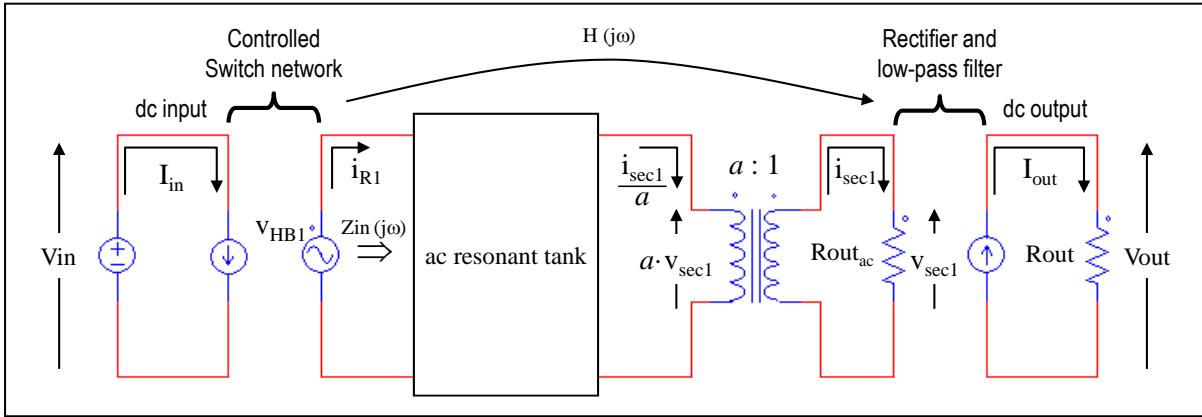
$$I_{sec.ac} = \sqrt{I_{sec1}^2 - I_{out}^2} . \quad (60)$$

Since  $v_{sec1}(t)$  and  $i_{sec1}(t)$  are in phase, the rectifier block exhibits an effective resistive load  $R_{out,ac}$  that is equal to the ratio of instantaneous voltage and current. Considering (57) and (59):

$$R_{out,ac} = \frac{v_{sec1}(t)}{i_{sec1}(t)} = \frac{V_{sec1}}{I_{sec1}} = \frac{8}{\pi^2} \frac{V_{out} + V_{Rect}}{I_{out}} = \frac{8}{\pi^2} (R_{out} + R_{Rect}) = \frac{8}{\pi^2} \frac{V_{out}^2}{P_{out}} \left( 1 + \frac{V_{Rect}}{V_{out}} \right) , \quad (61)$$

where it is clearly  $R_{Rect} = V_{Rect} / I_{out}$ .

**Figure 68. Resonant converters: transformation into equivalent linear circuit for FHA analysis.**



In the end, the nonlinear circuit of figure 67 can be transformed into the linear circuit of figure 68, where the ac resonant tank is excited by an effective sinusoidal input source and drives an effective resistive load. Notice that this transformation has been done with no assumption on the configuration of the tank circuit, the LLC circuit was used just as a concrete example.

This transformation allows the circuit to be studied with the complex ac-analysis method and, additionally, to pass from ac to dc voltages and currents, since the relationships between them are well-defined and fixed: refer to equations (51), (53), (54), (58) and (59).

The ac portion of the equivalent circuit in figure 68 can be characterized in the frequency domain by its forward transfer function  $H(j\omega)$  and input impedance  $Zin(j\omega)$ . In particular, considering the LLC equivalent circuit of figure 69, the expressions of  $H(j\omega)$  and  $Zin(j\omega)$  are:

$$H(j\omega) = \frac{V_{sec1}(j\omega)}{V_{HB1}(j\omega)} = \frac{1}{a} \frac{Re // j\omega Lp}{Zin(j\omega)}, \quad (62)$$

$$Zin(j\omega) = \frac{V_{HB1}(j\omega)}{I_{R1}(j\omega)} = \frac{1}{j\omega Cr} + j\omega Ls + Re // j\omega Lp. \quad (63)$$

In these expressions  $Re$  is  $Rout_{ac}$  reflected to the primary side of the transformer:

$$Re = a^2 Rout_{ac}. \quad (64)$$

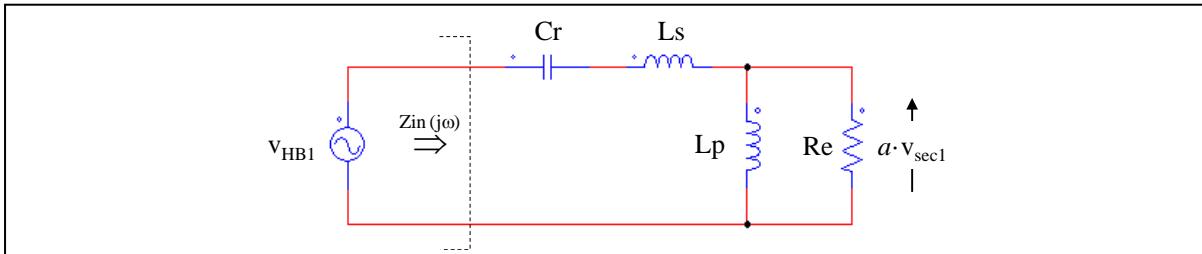
We now define the so-called *normalized voltage conversion ratio* or *voltage gain*  $M(f_{sw})$ :

$$M(f_{sw}) = a H(j 2\pi f_{sw}) = a \frac{V_{sec1}}{V_{HB1}}, \quad (65)$$

with  $V_{sec1}$  and  $V_{HB1}$  given by (57) and (51) respectively. Therefore, it is possible to write:

$$G_V = \frac{V_{out} + V_{Rect}}{Vin} = \begin{cases} \frac{1}{2a} |M(f_{sw})| & (\text{HB}) \\ \frac{1}{a} |M(f_{sw})| & (\text{FB}) \end{cases}. \quad (66)$$

**Figure 69. LLC resonant converters: equivalent linear circuit for FHA analysis.**



In other words, the voltage conversion ratio  $G_V = V_{out}/V_{in}$  in the half bridge is equal to half the module of the tank's forward transfer function  $H(j\omega)$  evaluated at the switching frequency and in the full bridge twice as much. It is worth highlighting that also this property does not depend on the configuration of the tank circuit.

For certain considerations it is of some interest the output impedance too. The equivalent circuit for its derivation is shown in figure 70. From that, considering the quantity referred to the primary side :

$$Z_{out}(j\omega) = a^2 \frac{V_{sec1}(j\omega)}{I_{sec1}(j\omega)} = \left( \frac{1}{j\omega C_r} + j\omega L_s \right) // j\omega L_p . \quad (67)$$

Finally, we define the following quantities:

Normalized frequency:  $x = \frac{f_{sw}}{f_{R1}}$ . (68)

Inductance ratio:  $k = \frac{L_p}{L_s}$ . (69)

Characteristic impedance:  $Z_0 = \sqrt{\frac{L_s}{C_r}} = 2\pi f_{R1} L_s = \frac{1}{2\pi f_{R1} C_r}$ . (70)

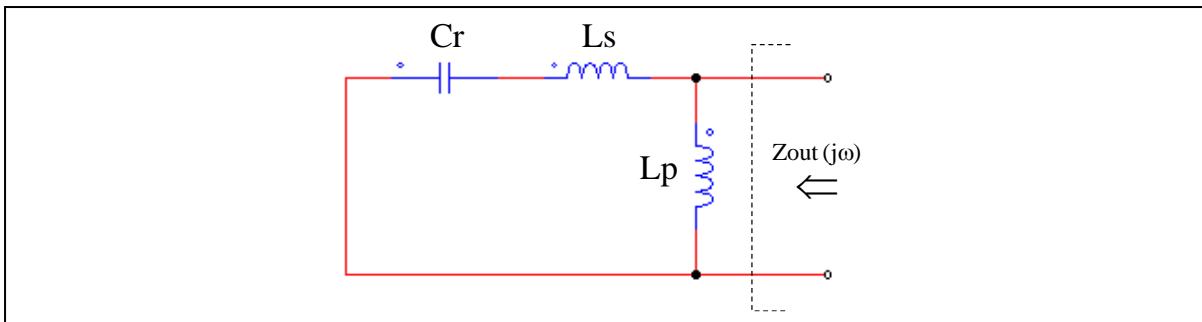
Quality factor:  $Q = \frac{Z_0}{R_e} = \frac{Z_0}{a^2 R_{out,ac}} = \frac{\pi^2}{8} \frac{Z_0}{a^2 (R_{out} + R_{Rect})} = \frac{\pi^2}{8} \frac{Z_0}{a^2} \frac{P_{out}}{V_{out}^2} \frac{1}{1 + \frac{V_{Rect}}{V_{out}}}$ . (71)

With these settings the normalized upper resonant frequency  $x_{R1}$  is obviously unity, the below resonance region is characterized by  $x < 1$  and the above resonance region by  $x > 1$ . The normalized lower resonant frequency  $x_{R2}$ , taking (3) and (69) into account, becomes:

$$x_{R2} = \sqrt{\frac{1}{1+k}} . \quad (72)$$

Note that in the typical case of a converter where the output voltage is regulated ( $V_{out} = \text{const.}$ ) the quality factor  $Q$  can be regarded as the converter load ( $Q \propto P_{out}$ ); therefore,  $Q = 0$  corresponds to no load,  $Q \rightarrow \infty$  when  $R_{out} = 0$  (short circuit).

**Figure 70. LLC resonant converters: equivalent linear circuit for FHA analysis of the output impedance.**



## Chapter 2

### FHA approach: input impedance analysis

Splitting (63) in its real and imaginary parts and considering (68)-(71), the expression of the input impedance of the LLC tank becomes:

$$Z_{in}(x, k, Q) = Z_0 \left\{ Q \frac{k^2 x^2}{1+Q^2 k^2 x^2} + j \left[ x \left( 1 + \frac{kx}{1+Q^2 k^2 x^2} \right) - \frac{1}{x} \right] \right\}. \quad (73)$$

It is convenient to analyze argument and magnitude of this complex function separately: they will provide different useful information on converters' operation and design.

*Analysis of  $\arg[Z_{in}(x, k, Q)]$ .*

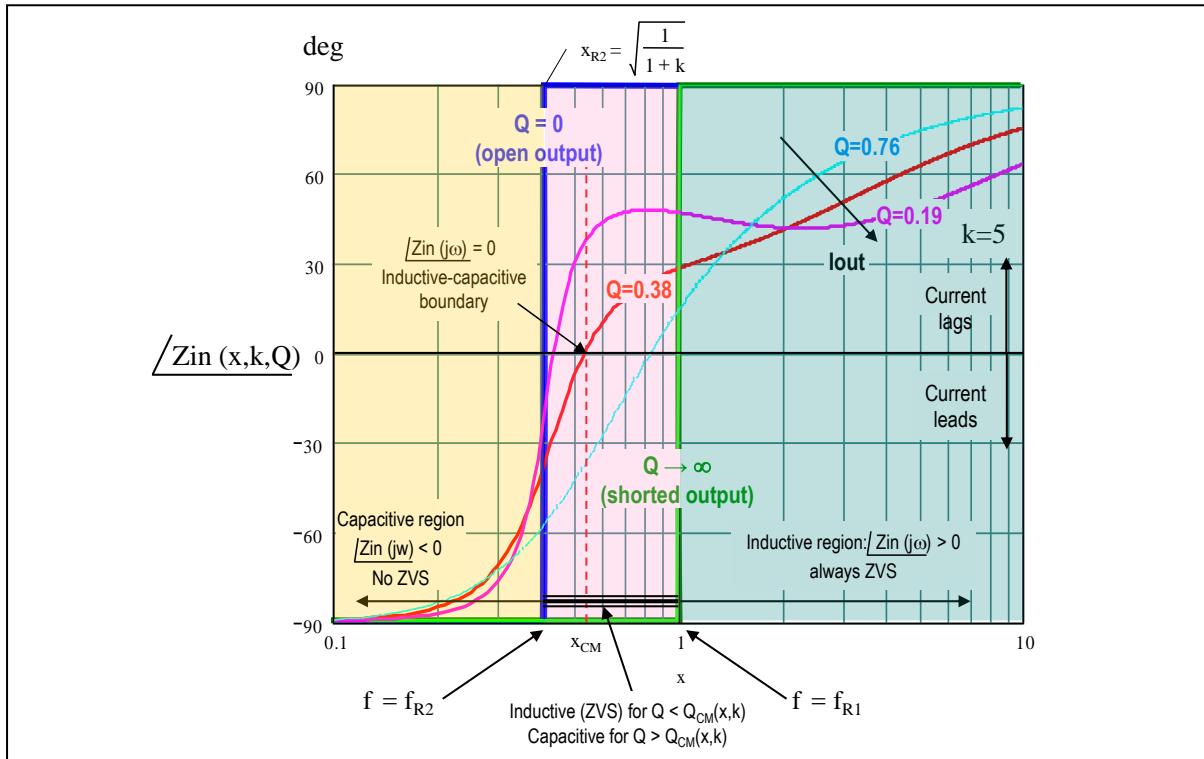
The complete expression of the argument of (73) is:

$$\arg[Z_{in}(x, k, Q)] = \tan^{-1} \frac{[1+k+Q^2 k^2(x^2-1)]x^2-1}{Qk^2x^3}, \quad (74)$$

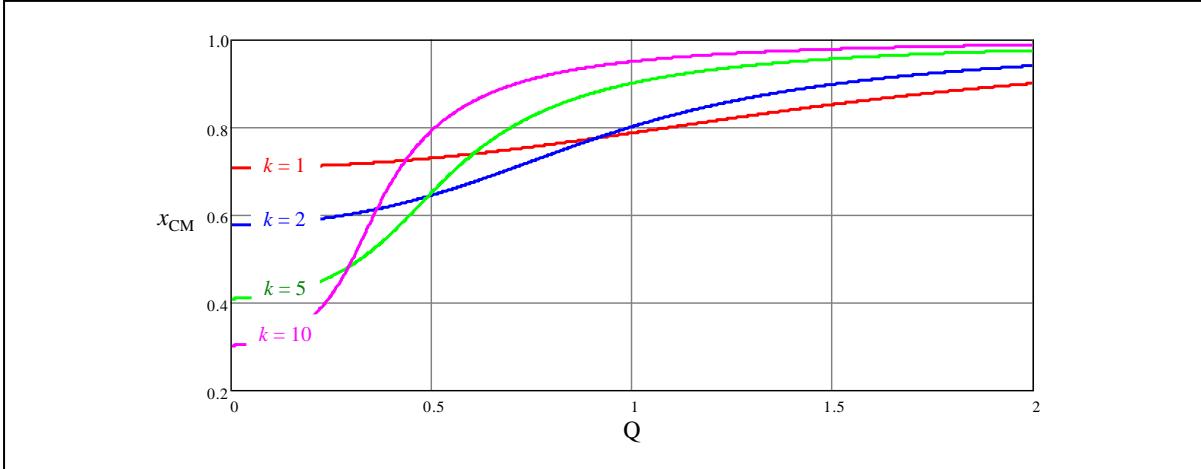
and its diagram vs  $x$  is plotted in figure 71 for a fixed value of  $k$  and different values of  $Q$ . The argument of  $Z_{in}(x, k, Q)$  (74) provides the voltage current phase-shift, i.e., the angle  $\varphi$  appearing in (52) – (54): when  $\arg[Z_{in}(x, k, Q)] > 0$  the tank current lags the input voltage (inductive behavior), when  $\arg[Z_{in}(x, k, Q)] < 0$  the tank current leads the input voltage (capacitive behavior). When  $\arg[Z_{in}(x, k, Q)] = 0$  the input impedance is resistive so that the tank current and the input voltage are in phase.

In the above resonance region ( $x > 1$ )  $\arg[Z_{in}(x, k, Q)]$  is always positive, which confirms that in that region the LLC tank has inductive behavior, with the input current lagging the input voltage; steady-state operation with ZVS is ensured.

**Figure 71. Plot of argument of  $Z_{in}(x, k, Q)$ .**



**Figure 72. Plot of normalized  $f_{CM}$ ,  $x_{CM}$ , as a function of the load ( $Q$ ).**



Below the lower resonant frequency ( $x < x_{R2}$ )  $\arg[Zin(x, k, Q)]$  is always negative, which means that in that region the LLC tank has capacitive behavior, with the input current leading the input voltage; this region belongs to the capacitive mode region where steady-state operation occurs without ZVS (then with type-2 hard switching).

In the region ( $x_{R2} < x < 1$ ) the sign of  $\arg[Zin(x, k, Q)]$  depends on the quality factor  $Q$  (i.e., on the load): if  $Q < Q_{CM}(x, k)$  then the sign is positive,  $Zin(x, k, Q)$  is inductive and the steady-state operation is with ZVS; if  $Q \geq Q_{CM}(x, k)$  then the sign is negative,  $Zin(x, k, Q)$  is capacitive and the steady-state operation is without ZVS.

The critical value  $Q_{CM}(x, k)$  is defined by  $\arg[Zin(x, k, Q)] = 0$ , that is by  $\text{Im}[Zin(x, k, Q)] = 0$ . When this condition is met, i.e., the input impedance is real, input voltage and tank current are exactly in phase. Assuming  $x$  is fixed, equating (74) to zero and solving for  $Q$ , the significant root is:

$$Q_{CM}(x, k) = \frac{1}{kx} \sqrt{\frac{(1+k)x^2 - 1}{1-x^2}} . \quad (75)$$

For a fixed value of  $Q$ , the normalized frequency where  $\text{Im}[Zin(x, k, Q)] = 0$  is the boundary condition between capacitive and inductive mode operation of the LLC resonant converter:

$$x_{CM}(k, Q) = \frac{1}{kQ} \sqrt{\frac{(kQ)^2 - (1+k) + \sqrt{[1+k-(kQ)^2]^2 + (2kQ)^2}}{2}} . \quad (76)$$

Of course,  $f_{CM} = x_{CM} f_{R1}$ . Figure 72 shows the plot of  $x_{CM}$  as a function of  $Q$  for different values of  $k$ . When  $Q \rightarrow 0$   $x_{CM} \rightarrow 1/\sqrt{1+k}$ . Irrespective of  $k$ , when  $Q$  increases  $x_{CM}$  tends to unity asymptotically;  $k$  determines how fast  $x_{CM}$  tends to unity as  $Q$  increases: the lower  $k$  is, the slower  $x_{CM}$  tends to unity and vice versa.

When the converter works at resonance the expression of the voltage current phase-shift is:

$$\arg[Zin(1, k, Q)] = \tan^{-1} \frac{1}{kQ} . \quad (77)$$

*Analysis of  $|Zin(x, k, Q)|$ .*

The complete expression of the magnitude (modulus) of (73) is:

$$|Zin(x, k, Q)| = Z_0 \sqrt{\left(Q \frac{k^2 x^2}{1+Q^2 k^2 x^2}\right)^2 + \left[x \left(1 + \frac{kx}{1+Q^2 k^2 x^2}\right) - \frac{1}{x}\right]^2} . \quad (78)$$

This quantity provides the amplitude of the tank current with a given input voltage and is also useful to evaluate the amplitude of the voltage across the resonant capacitor  $C_r$ . To be independent of the specific design it is convenient to refer to the normalized magnitude:

$$|Zin_n(x, k, Q)| = \frac{|Zin(x, k, Q)|}{Z_0} . \quad (79)$$

The diagram of the normalized impedance  $|Zin_n(x, k, Q)|$  vs  $x$  is plotted in figure 73 for a fixed value of  $k$  and different values of  $Q$ . The presence of a *load-independent point* stands out: all the curves for any value of  $Q$  pass through the point:

$$x_Z = \sqrt{\frac{2}{2+k}}, \quad \frac{Zin}{Z_0} = \frac{k}{2} \sqrt{\frac{2}{2+k}} . \quad (80)$$

Notice that with a fixed  $x > x_Z$  the magnitude of  $Zin_n(x, k, Q)$  and the load vary in the same manner: as  $I_{out}$  gets bigger  $|Zin_n(x, k, Q)|$  increases too. With a fixed  $x < x_Z$  the magnitude of  $Zin_n(x, k, Q)$  and the load vary conversely: as  $I_{out}$  increases  $|Zin_n(x, k, Q)|$  decreases.

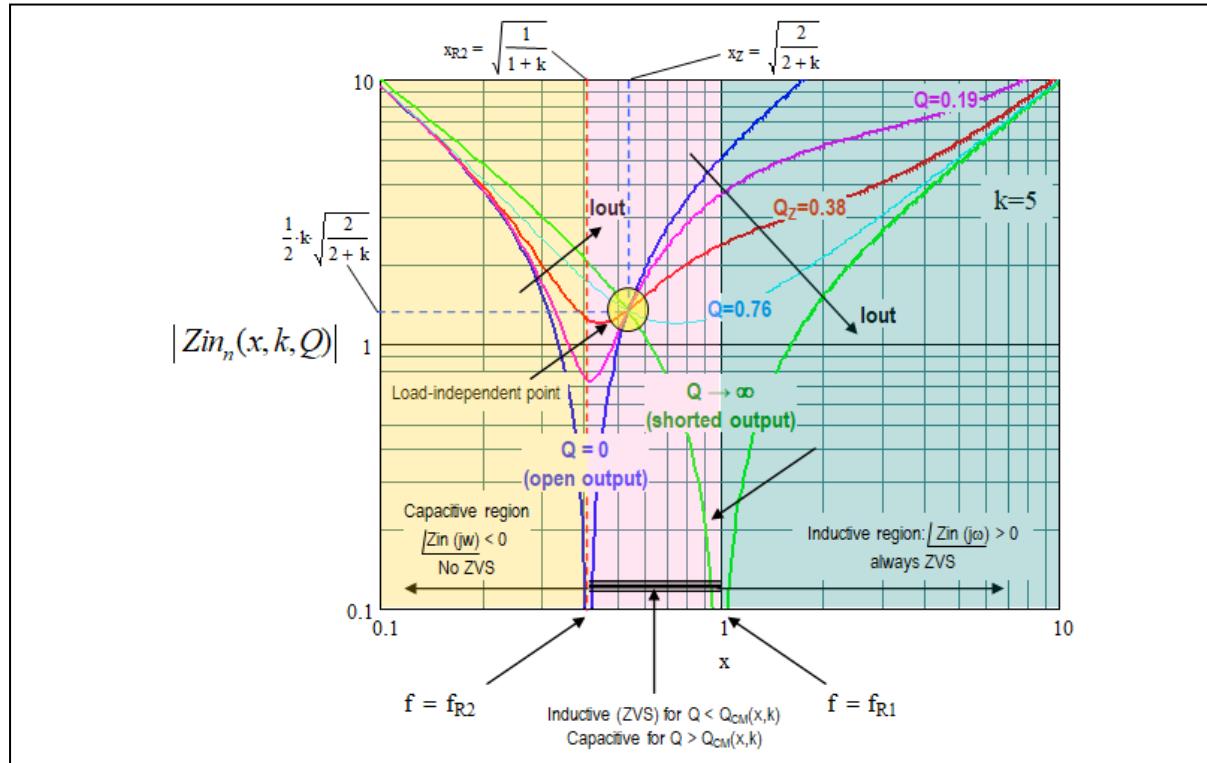
Fixing  $x$  means open-loop operation. In closed-loop operation frequency is not constant and load and magnitude of  $Zin_n(x, k, Q)$  vary in the same manner even at frequencies less than  $x_Z$ .

It is however worth noticing that all curves have a local minimum whose position depends on  $Q$ : with  $Q = 0$  the minimum is zero and is located at the lower resonance frequency  $x_{R2}$ ; as  $Q$  increases the value of the minimum rises and so does its position  $x_m$  until it equals  $x_Z$  when:

$$Q = Q_M = \frac{1}{k} \sqrt{\frac{3k^2+10k+8}{2(k+4)}} , \quad (81)$$

in which case the minimum reaches its maximum value  $Zin/Z_0$  given by (80). If  $Q$  further increases, it will be  $x_m > x_Z$  and the value of the minimum will start dropping until it becomes again zero at  $x = 1$  when  $Q \rightarrow \infty$ .

**Figure 73. Plot of magnitude of  $Zin_n(x, k, Q)$ .**



Evidently, the fact that  $|Zin_n(x, k, Q)|$  has a minimum means that the maximum current that can flow in the tank circuit (and, then, the power that the converter can output) has an upper limit, except at resonance ( $x = 1$ ) where the impedance is zero and the power capability is theoretically unlimited. Also notice that when  $x > x_m$  the magnitude of the impedance increases with  $x$  and this is consistent with the normal operation of the control loop that increases the switching frequency when the power demanded by the load decreases. With values  $x < x_m$  the magnitude of the impedance increases as  $x$  moves away from  $x_m$ , which causes feedback reversal and loss of regulation in a closed-loop system.

It is interesting to find where  $x_Z$  is located and if it belongs to the inductive or the capacitive region. Clearly, it is  $x_{R2} < x_Z < 1$ ; by comparing (76) and (80) it is possible to state that when  $Q$  equals:

$$Q_Z = \frac{\sqrt{2} \sqrt{k+2}}{2} , \quad (82)$$

it is  $x_Z = x_{CM}$ . It is possible to prove that it is always  $Q_Z < Q_M$ . To have a more exact idea of how  $x_Z$  and  $x_{CM}$  are related the capacitive mode region on the  $x - |Zin_n(x, k, Q)|$  plane needs to be identified.

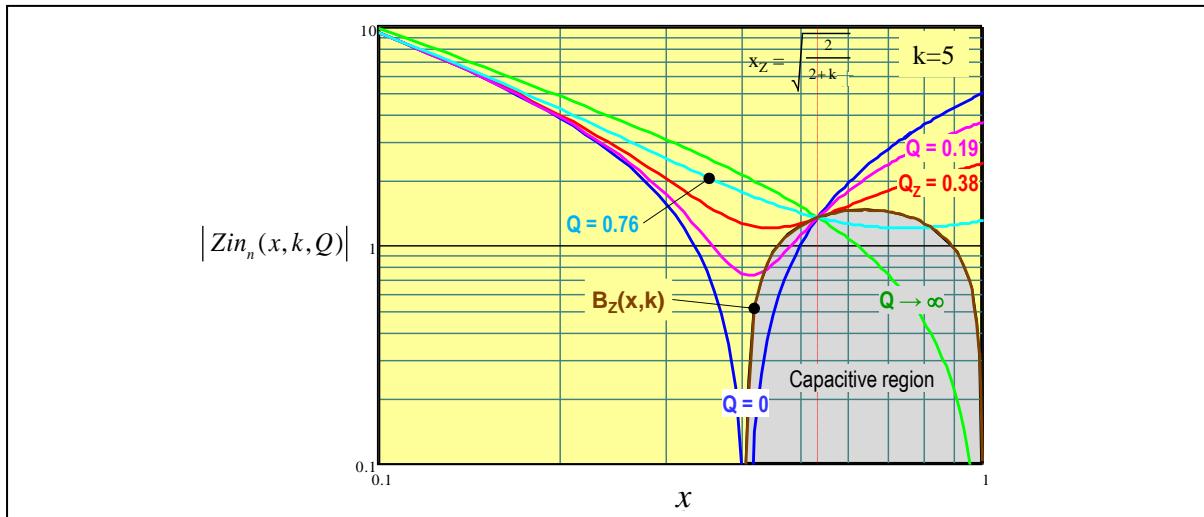
If we substitute (75) in (78), considering that when  $Q = Q_{CM}(x, k)$  the imaginary part of  $Zin(x, k, Q)$  is zero, we can find the equation describing the locus of the inductive-capacitive boundary on the  $x - |Zin_n(x, k, Q)|$  plane:

$$B_Z(x, k) = \frac{1}{x} \sqrt{(1-x^2)[(k+1)x^2 - 1]} . \quad (83)$$

This function is shown in the plot of figure 74. The points of the  $|Zin_n(x, k, Q)|$  curves falling in the region encircled by the  $B_Z(x, k)$  locus are characterized by capacitive-mode operation. It is possible to see that, moving from  $x = x_{R1} = 1$  to  $x_{R2}$ , if  $Q \leq Q_Z$  the curves enter the capacitive region at  $x = x_Z$  (79) (therefore,  $x_{CM} = x_Z$ ) and exits at a lower frequency, except for the curve  $Q = 0$  that stays entirely in the capacitive region.

It is possible to prove that the curve with  $Q = Q_Z$  is tangent to the  $B_Z(x, k)$  locus (83) in  $x = x_Z$  and the common slope in that point is  $k/2$ . For  $Q > Q_Z$  the capacitive region is entered at a frequency  $x_{CM} > x_Z$  and exited at  $x = x_Z$ . When  $Q \rightarrow \infty$  the curve is entirely in the capacitive region for  $x_Z < x < 1$ .

**Figure 74. Plot of  $B_Z(x, k)$  on  $x - |Zin_n(x, k, Q)|$  plane.**



Notice that, except for the curve  $Q = Q_Z$  that is tangent to the  $B_Z(x, k)$  locus, the local minimum for  $|Zin_n(x, k, Q)|$  is reached inside the capacitive region when  $Q > Q_Z$  and after crossing the capacitive region when  $Q < Q_Z$ . It is therefore reasonable to presume that the upper limit of the tank current (i.e., its maximum power capability) is reached at a frequency of no interest since it occurs for  $x < x_{CM}$ , outside the inductive operating region.

When the converter works at resonance the magnitude of the input impedance is:

$$|Zin_n(1, k, Q)| = \frac{k}{\sqrt{1+(kQ)^2}} . \quad (84)$$

Under no-load conditions the magnitude of the input impedance is:

$$|Zin_{n0}(x, k)| = |Zin_n(x, k, 0)| = \left| (1+k)x - \frac{1}{x} \right| . \quad (85)$$

In the spirit of a design-oriented approach, it is important to assess the peak amplitude of the (resonant) voltage  $V_{C1pk}$  across the resonant capacitor  $C_r$  to properly select its rated voltage.

The voltage  $V_{C1pk}$  (the subscript 1 reminds us that it is the first harmonic of  $V_C(t)$ ) is given by:

$$V_{C1pk} = V_{HB1pk} \frac{|X_{Cr}|}{|Zin(x, k, Q)|} , \quad (86)$$

where  $|X_{Cr}|$  is the module of the reactance of  $C_r$  at the operating frequency  $f_{sw}$ .

It is not difficult to show that with the symbolism in use this reactance can be expressed as:

$$|X_{Cr}| = \frac{1}{2\pi f_{sw} C_r} = \frac{Z_0}{x} . \quad (87)$$

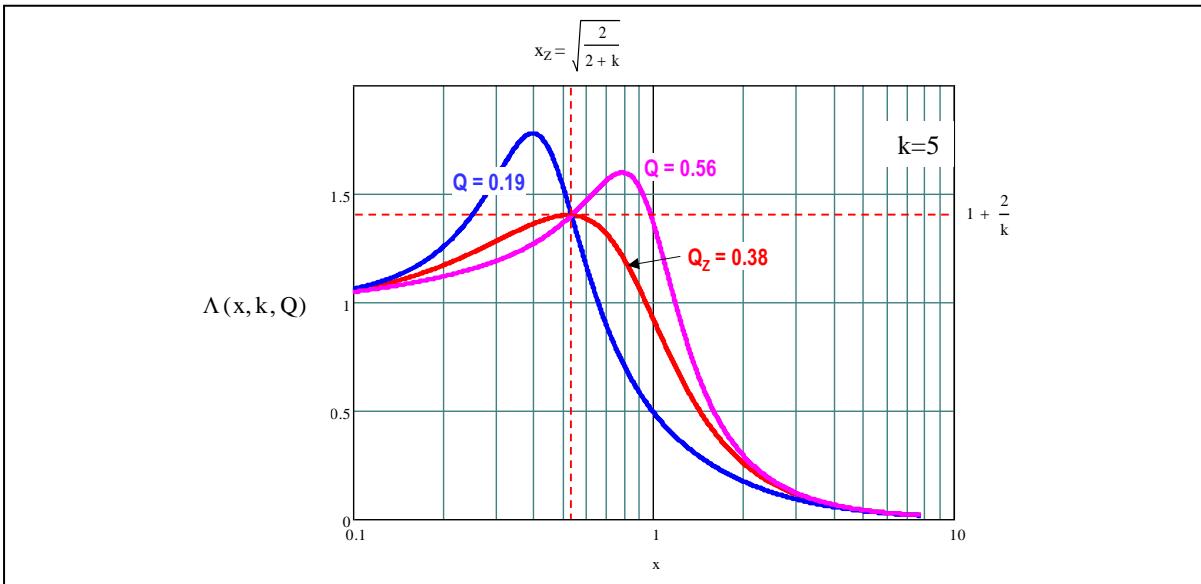
Therefore, (86) can be rewritten as:

$$\Lambda(x, k, Q) = \frac{V_{C1pk}}{V_{HB1pk}} = \frac{|X_{Cr}|}{|Zin(x, k, Q)|} = \frac{1}{x |Zin_n(x, k, Q)|} , \quad (88)$$

that is:

$$\Lambda(x, k, Q) = \frac{1}{x \sqrt{\left(Q \frac{k^2 x^2}{1+Q^2 k^2 x^2}\right)^2 + \left[x \left(1 + \frac{kx}{1+Q^2 k^2 x^2}\right) - \frac{1}{x}\right]^2}} . \quad (89)$$

**Figure 75. Plot of  $\Lambda(x, k, Q)$ .**



Equation (89) is plotted in figure 75. All curves tend asymptotically to  $\Lambda = 1$  when  $x \rightarrow 0$  and to 0 when  $x \rightarrow \infty$ . They also show the load independent point  $x = x_Z$ , where  $\Lambda = 1 + 2/k$ . The curve  $\Lambda(x, k, Q_Z)$ , with  $Q_Z$  given by (82), peaks exactly at the load-independent point; the curves  $\Lambda(x, k, Q)$  with  $Q > Q_Z$  peak at a frequency higher than  $x_Z$ , those with  $Q < Q_Z$  at a frequency lower than  $x_Z$ .

At resonance it is:

$$\Lambda(1, k, Q) = \frac{1}{k} \sqrt{1 + k^2 Q^2} . \quad (90)$$

To determine the actual voltage stress  $V_{C1max}$  on  $Cr$  we need to consider (86) along with (51), keeping in mind that in the half bridge configuration the resonant voltage is superimposed on the dc value  $V_{in}/2$ . Therefore:

$$V_{C1max} = \begin{cases} \left[ \frac{2}{\pi} \Lambda(x, k, Q) + \frac{1}{2} \right] V_{in} & (\text{HB}) \\ \frac{4}{\pi} \Lambda(x, k, Q) V_{in} & (\text{FB}) \end{cases} . \quad (91)$$

In the previous analysis on the ZVS conditions when the converter works close to the minimum operating frequency, it was shown that the necessary and sufficient condition is that the converter operates in the inductive region and that condition (18) is fulfilled. In that equation, as well as in (19)-(23), the voltage  $V_{co}$  across  $Cr$  at the instant of transitions appears. An expression of  $V_{co}$  at the transition Q2 ON-OFF & Q1 OFF-ON has been provided in (28) for the half bridge and in (29) for the full bridge.

It is interesting to find  $V_{co}$  within the FHA approach too, i.e.,  $V_{C10}$ .

The resonant voltage  $V_{C1}(t)$  lags the tank current  $i_{R1}(t)$  by 90 degrees; then reminding the expression (52) of  $i_{R1}(t)$ , taking (86) into account and considering  $2\pi f_{sw} t = -\pi/2$  to account for the 90 degrees phase-shift, it is possible to write:

$$V_{C10} = -\sqrt{2} I_{R1} \cos \varphi |X_{Cr}| . \quad (92)$$

Considering (53) and the expression of  $|X_{Cr}|$  in (87), finally:

$$V_{C10} = \begin{cases} -\frac{I_{in}}{2 Cr f_{sw}} & (\text{HB}) \\ -\frac{I_{in}}{4 Cr f_{sw}} & (\text{FB}) \end{cases} , \quad (93)$$

which leads to the same result provided in (28) and (29).

## Chapter 3

### FHA approach: voltage gain $M(f_{sw})$ analysis

Splitting (65) in its real and imaginary parts and considering (68)-(71), the expression of the voltage gain of the LLC tank becomes:

$$M(x, k, Q) = \frac{1}{1 + \frac{1}{k} \left(1 - \frac{1}{x^2}\right) + jQ \left(x - \frac{1}{x}\right)} . \quad (94)$$

The argument of this function provides information on the phase-shift between the input and output voltages, which is of little practical use. Therefore, only the magnitude of this complex function will be analyzed. Its expression is:

$$|M(x, k, Q)| = \frac{1}{\sqrt{\left[1 + \frac{1}{k} \left(1 - \frac{1}{x^2}\right)\right]^2 + Q^2 \left(x - \frac{1}{x}\right)^2}} . \quad (95)$$

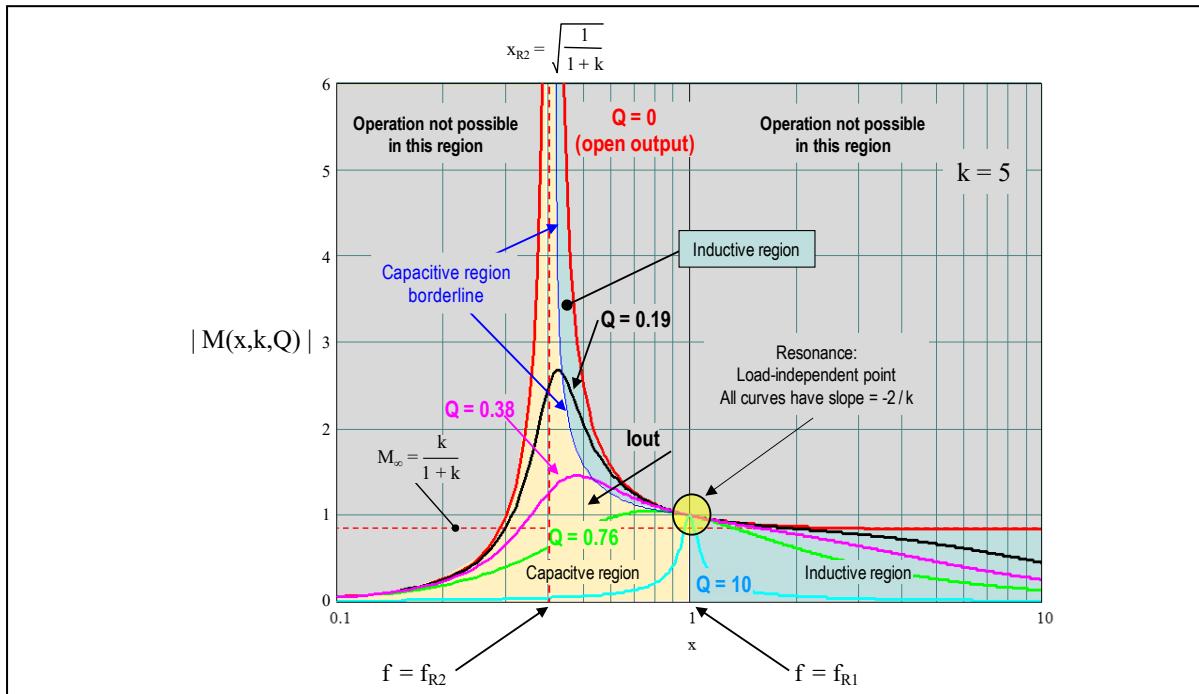
It is worth reminding that this is not the dc voltage conversion ratio  $G_V = V_{out}/V_{in}$  (66).

The diagram of the voltage gain  $|M(x, k, Q)|$  vs  $x$  is plotted in figure 76 for a fixed value of  $k$  and different values of  $Q$ . Notice in this case the presence of a load-independent point at resonance: all the curves for any value of  $Q$  pass through the point  $(1, 1)$ . Also notice that this load-independent point is different from that seen for  $Z_{in}$ , which occurred for  $x < 1$ .

By differentiating (95) and setting  $x = 1$ , it is possible to prove that all curves have a slope equal to  $-2/k$ .

Noticeably, this load-independent point occurs in the inductive region of the voltage gain characteristic, where the resonant tank lags the input voltage square waveform (which is a necessary condition for ZVS behavior). Considering this, if the converter is operated close to this point, the output voltage can be regulated against wide loads variations with a relatively small change in the switching frequency. This confirms what has been previously discussed.

**Figure 76. Plot of  $|M(x, k, Q)|$ .**



Looking at the curves in figure 76, it is evident that the wider the range of  $|M(x, k, Q)|$  that the converter is required to accommodate (i.e., the wider the input dc voltage range is), the wider the operating frequency range will be. Intuitively, this makes converter's optimization more difficult: this is one of the main drawbacks common to all resonant topologies.

This is one of the reasons why in most offline applications the LLC converter is powered by a PFC pre-regulator (the other is that the LLC converter is typically used at power levels where a PFC is required to comply with low-frequency emissions standards).

Even with a wide-range mains ( $85V_{ac} - 264V_{ac}$ ) the PFC pre-regulator provides a regulated voltage bus of around  $400 V_{dc}$  nominal, with just narrow variations in normal operation. The lower and upper ends of the operating voltage range depend, respectively, on the PFC pre-regulator hold-up capability during mains dips and on the trip level of its over voltage protection circuit, typically located about 10-15% above the nominal value. Therefore, the resonant converter can be optimized to operate at the load-independent point when the input voltage is at nominal value and letting the step-up/down capability of the LLC tank handle the deviations from the nominal value.

The red curve (i.e.,  $Q = 0$ ) in figure 76 represents the no-load voltage gain curve  $|M_0(x, k)|$ . Its expression is:

$$|M_0(x, k)| = \frac{1}{\left|1 + \frac{1}{k}\left(1 - \frac{1}{x^2}\right)\right|} . \quad (96)$$

As the normalized frequency  $x$  approaches  $x_{R2}$ ,  $M_0$  tends to infinity. As  $x$  goes to infinity,  $M_0$  tends to the asymptotic value  $M_\infty$ :

$$M_\infty = |M_0(x \rightarrow \infty, k)| = \frac{k}{1+k} . \quad (97)$$

It is possible to provide a geometrical interpretation of the LLC ability to regulate with no load with given  $V_{in}$  and  $V_{out}$ : in order for that to be possible there must be an intersection between the curve  $|M_0(x, k)|$  and the horizontal line related to the required value of the voltage gain  $M$  deduced by (66). The abscissa of this intersection is the cutoff frequency and is given by:

$$x_0 = \frac{1}{\sqrt{1+k\left(1-\frac{1}{M}\right)}} . \quad (98)$$

Noticeably, the branches of  $M_0(x, k)$  delimit the area of the  $x - |M(x, k, Q)|$  plane where the operating point of the converter may be situated: that lying below the curve. No operating point can lie in the area above the curve, the grey-shaded ones in figure 76.

The area under the curve  $M_0(x, k)$  with  $x \geq 1$  (above resonance) belongs to the inductive region; there it is always  $|M(x, k, Q)| < 1$  (step-down). In the area under the curve  $M_0(x, k)$  with  $x < 1$  (below resonance) the gain can exceed unity (step-up). This area is shared between the capacitive region and the inductive region and figure 76 shows the borderline between them. Its equation can be calculated by substituting the critical value  $Q_{CM}(x, k)$  given by (75), which nulls the imaginary part of the input impedance, in (95). The result is:

$$B_M(x, k) = x \sqrt{\frac{k}{(k+1)x^2 - 1}} , \quad (99)$$

Setting  $B_M(x, k) = M$  and eliminating  $x$  between (75) and (98) yields the value of  $Q$ ,  $Q_B$ , that marks the capacitive-inductive transition for a given voltage gain  $M$ :

$$Q_B = \frac{1}{kM} \sqrt{\frac{M^2}{M^2 - 1} + k} . \quad (100)$$

Therefore,  $Q_B$  is the maximum value of  $Q$  where ZVS is achieved, being fixed everything else. Besides, setting again  $B_M(x,k) = M$  solving (99) for  $x$  yields the normalized frequency  $x_{CMB}$  marking the capacitive-inductive transition for a given voltage gain  $M$ :

$$x_{CMB} = \frac{M}{\sqrt{(k+1)M^2 - k}} . \quad (101)$$

In the end, we can conclude that to achieve ZVS in the below resonance region with a given frequency, the gain  $M$  must be larger than  $B_M(x,k)$ . If  $M$  is fixed, to achieve ZVS the quality factor  $Q$  must be lower than  $Q_B$  (100) or, which is the same, the normalized switching frequency must be larger than  $x_{CMB}$  (101).

It is interesting to compare  $Q_B$  (100) with  $Q_Z$  (82) and, consequently, also  $x_{CMB}$  (101) with  $x_Z$  (80) to find under what conditions one is greater or less than the other. Equating (100) to (82) or, which is the same, (101) to (80) and solving for  $M$ , it is possible to find that when  $M > \sqrt{2}$  it is  $Q_B > Q_Z$  and  $x_{CMB} < x_Z$ ; for lower values of  $M$  it is  $Q_B < Q_Z$  and  $x_{CMB} > x_Z$ .

Also notice that the curve with  $Q = Q_Z$  crosses the capacitive-inductive boundary  $B_M(x,k)$  at the normalized frequency  $x = x_Z$  and at frequencies  $x < x_Z$  for values of  $Q < Q_Z$ , as seen during the analysis of the input impedance.

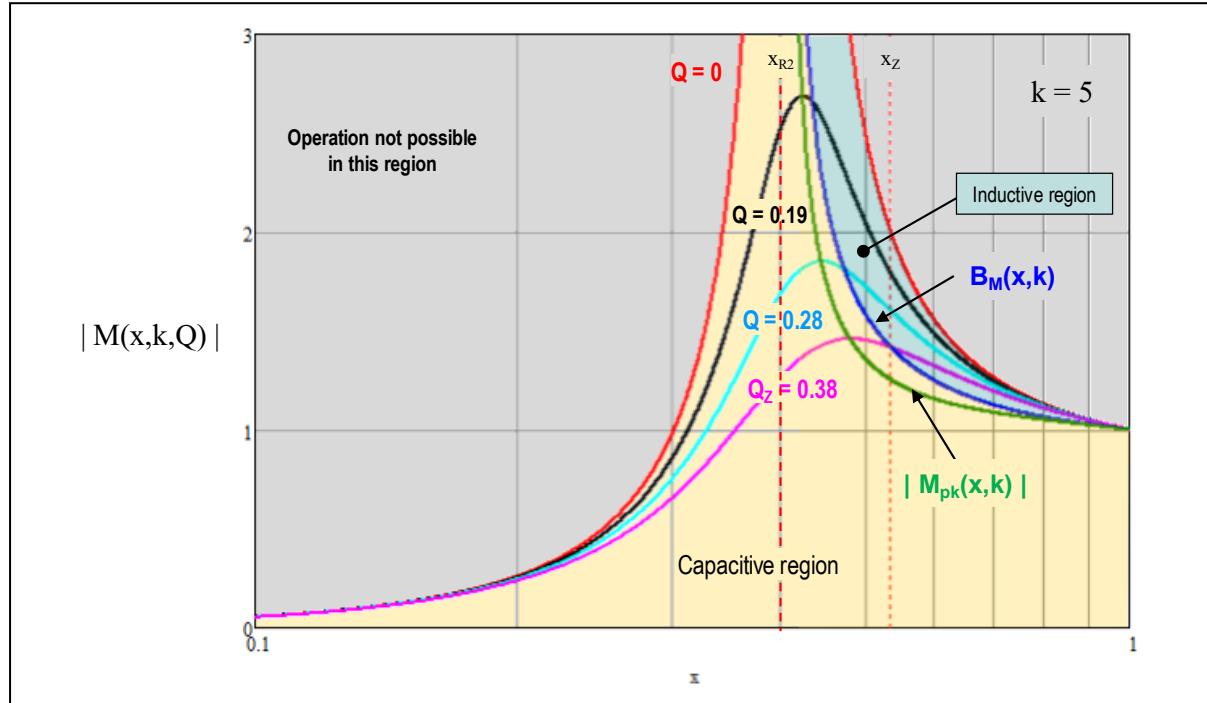
The gain curves  $|M(x,k,Q)|$  feature a peak at a certain  $x$  value that appears to be situated in the capacitive region. The locus that joins all the maxima of the gain curves can be found by looking for the minima of the denominator of the function  $|M(x,k,Q)|^2$ . Then, differentiating  $1/|M(x,k,Q)|^2$  with respect to  $x$ , equating the result to zero and solving for  $Q$  we find:

$$Q_{pk} = \frac{\sqrt{2}}{kx} \sqrt{\frac{(k+1)x^2 - 1}{1 - x^3}} . \quad (102)$$

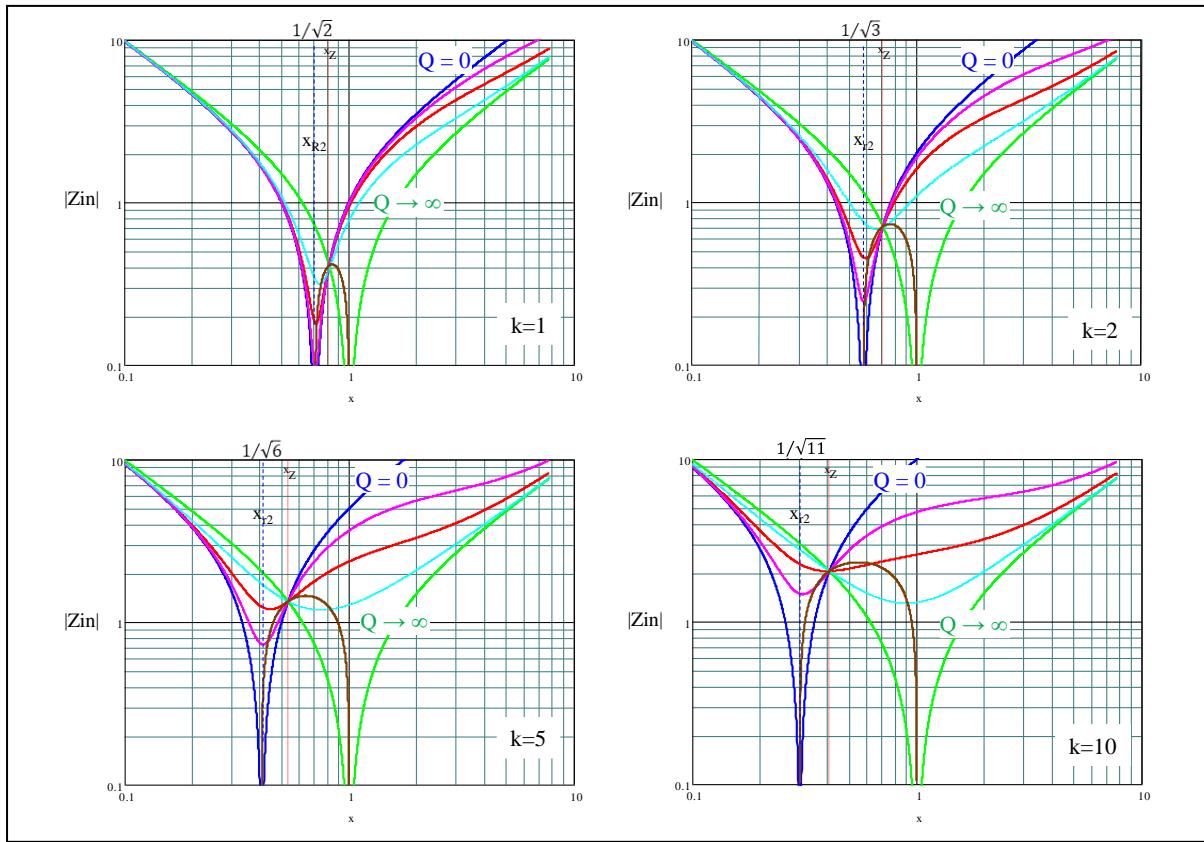
By substituting  $Q_{pk}$  given by (102) in (95) we find the equation of the peak gain locus  $|M_{pk}(x,k)|$ :

$$|M_{pk}(x,k)| = kx^2 \sqrt{\frac{x^2 + 1}{[(k+1)x^2 - 1][(k+1)x^4 + (k-2)x^2 + 1]}} . \quad (103)$$

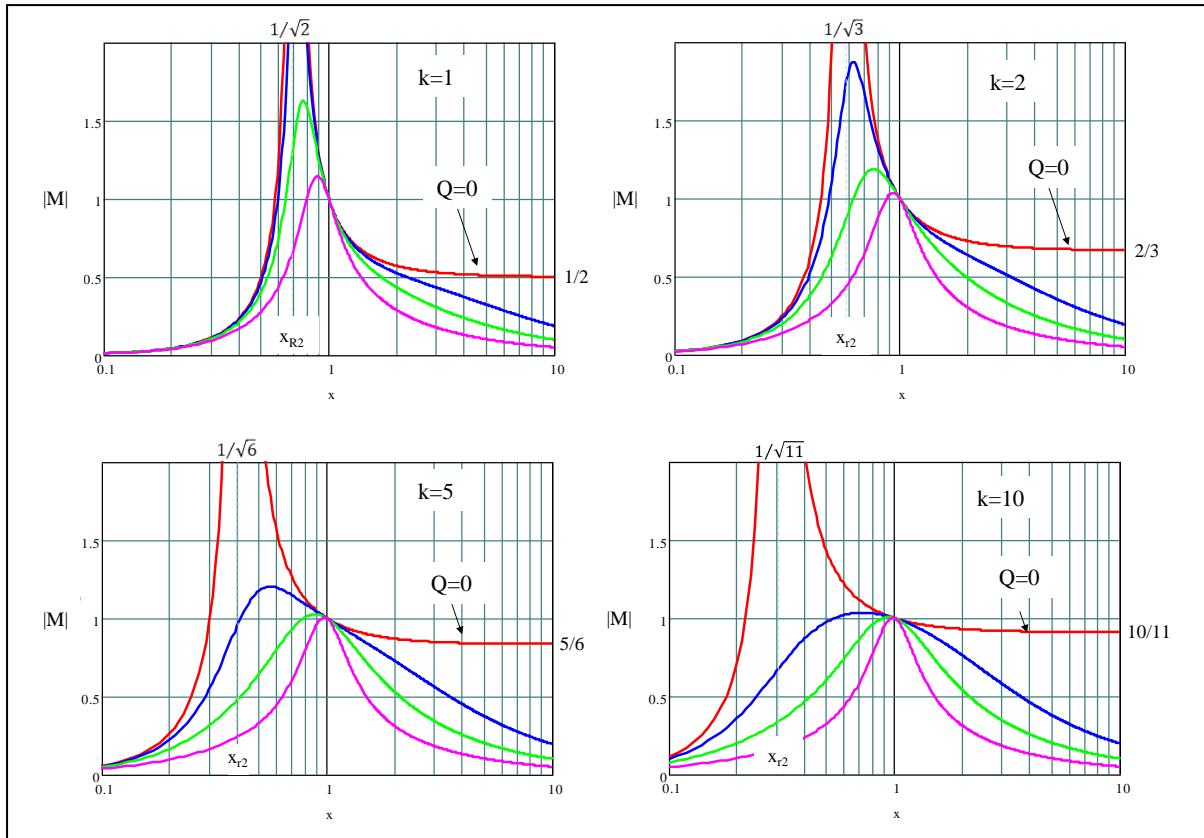
**Figure 77. Plot of  $|M_{pk}(x,k)|$  in the below resonance region of the  $x$  -  $|M(x,k,Q)|$  plane.**



**Figure 78. Plots of  $|Zin_n(x, k, Q)|$  for different values of  $k$ .**



**Figure 79. Plots of  $|M(x, k, Q)|$  for different values of  $k$ .**



The plot of (103) is shown in figure 77 (green curve) and is clearly located on the left of the capacitive-inductive borderline (blue curve). It is possible to prove that analytically by showing that the ratio  $|M_{pk}(x,k)| / B_M(x,k)$  has a local maximum at  $x = 1$ , therefore for any  $x$  in  $(x_{R2}, 1)$  it is  $|M_{pk}(x,k)| < B_M(x,k)$ .

It is useful to determine the value of  $Q$  for which the LLC tank has an assigned voltage gain  $M$  at a given frequency  $x$ . To do so we can simply solve (95) for  $Q$ . The result is:

$$Q_M = \frac{x}{|1-x^2|} \sqrt{\frac{1}{M^2} - \left(\frac{(k+1)x^2-1}{kx^2}\right)^2} . \quad (104)$$

So far, we have examined the plots of  $|Zin_n(x,k,Q)|$  and  $|M(x,k,Q)|$  for a fixed value of the inductance ratio  $k$  ( $k = 5$ , which is quite a typical value).

Looking at figures 78 and 79, we can see the effects of different values of  $k$  on the magnitude of the impedance and the voltage gain respectively.

In general,  $k$  determines the resonance frequencies gap, i.e., the ratio  $f_{R2} / f_{R1}$  given by (72); the smaller  $k$  is, the closer the two frequencies are and vice versa. In terms of normalized frequency,  $x_{R2}$  get closer to unity for lower values of  $k$  and gets smaller for higher values of  $k$ .

All the characteristic curves of  $|Zin(x,k,Q)|$  and  $|M(x,k,Q)|$  in the region  $(x_{R2}, 1)$  are therefore more or less compressed depending on the value of  $k$ .

As regards the magnitude of  $Zin(x,k,Q)$ :

- $k$  does not affect the impedance with  $Q \rightarrow \infty$ , it affects that with  $Q = 0$ : it shifts following  $x_{R2}$ , (the point where  $Zin = 0$ ) and changes the slope of its high frequency asymptote, which is proportional to  $1 + k$ .
- the load-independent point and the corresponding value of  $|Zin(x,k,Q)|$  moves as stated by (80):  $x_Z$  increases/decreases with  $k$ ,  $|Zin(x_Z,k,Q)|$  changes conversely.
- $k$  affects the value of the local minima: the larger  $k$  is, the higher the minima are, and vice versa.

As regards the voltage gain  $|M(x,k,Q)|$ :

- $k$  determines the resonance frequencies gap, i.e., the ratio  $f_{R2} / f_{R1}$  given by (72) and therefore affects the position of vertical asymptote for  $|M_0(x,k)|$ : increasing  $k$ ,  $x_{R2}$  gets smaller and the gap becomes larger.
- $k$  affects the operating frequency range for an assigned operating conditions range: increasing  $k$  the frequency range gets larger.
- $k$  affects the asymptotic value  $M_\infty$ , i.e., the minimum achievable voltage gain when operating above resonance and then the capability of regulating with no-load at a finite frequency. Larger values of  $k$  increase  $M_\infty$  and the no-load operating frequency. And vice versa.
- $k$  affects the peak gain for assigned  $Q$  value: as  $k$  increases the peak gain decreases and vice versa.

Note that if  $k \rightarrow \infty$   $M_\infty \rightarrow 1$ ,  $x_{R2} \rightarrow 0$  and the LLC tank becomes an LC tank with its well-known limitations

## Chapter 4

### FHA approach: output impedance analysis

Expanding (67) and considering (68)-(71), the expression of the output impedance  $Z_{out}(x, k)$  of the LLC tank becomes:

$$Z_{out}(x, k) = Z_0 \left[ jk \frac{x^2 - 1}{(1+k)x^2 - 1} x \right]. \quad (105)$$

Again, to be independent of the specific design it is convenient to refer to the normalized quantity:

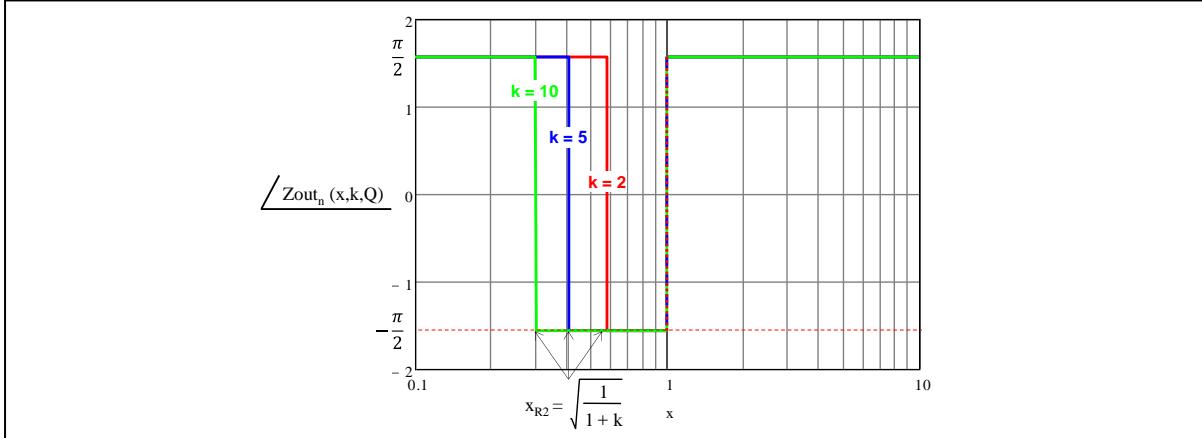
$$Z_{out,n}(x, k) = \frac{Z_{out}(x, k)}{Z_0}. \quad (106)$$

Figure 80 shows the plot of the argument of  $Z_{out,n}(x, k)$ , which is expressed by:

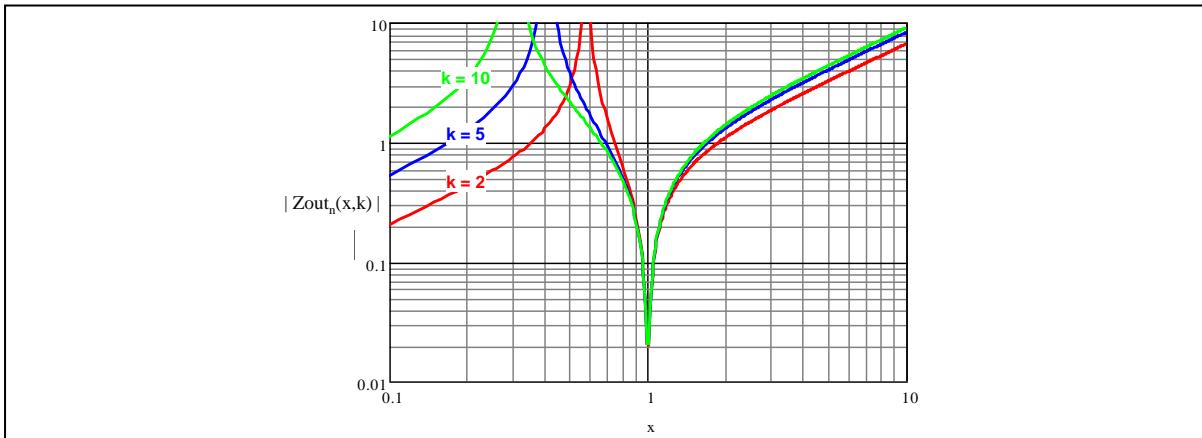
$$\arg[Z_{out,n}(x, k)] = \begin{cases} \frac{\pi}{2} & x < \sqrt{\frac{1}{1+k}}, \quad x > 1 \\ -\frac{\pi}{2} & \sqrt{\frac{1}{1+k}} < x < 1 \end{cases}. \quad (107)$$

The step discontinuities occur at the two resonance frequencies  $x = x_{R2}$  and  $x = 1$ . The plot of  $|Z_{out,n}(x, k)|$  is shown in figure 81.

**Figure 80. Plot of argument of  $Z_{out,n}(x, k)$ .**



**Figure 81. Plot of  $|Z_{out,n}(x, k)|$ .**



The modulus of  $Zout_n(x,k)$ :

$$|Zout_n(x,k)| = k \left| \frac{x^2 - 1}{(1+k)x^2 - 1} \right| x , \quad (108)$$

shows a vertical asymptote at  $x = x_{R2}$  and goes to zero at  $x = 1$ .

The output impedance of the LLC tank circuit allows us to investigate how the output voltage  $a \cdot v_{sec1}(x)$  changes with the load current  $i_{sec1}(x)/a$  at a given frequency using the Thevenin-equivalent circuit of figure 82 in the phasor domain.

The voltage generator is the open circuit output voltage amplitude, which is given by the input voltage  $v_{HB1}(x)$  multiplied by the open-circuit transfer function  $M_0(x,k) = M(x,k,0)$  given by (94). In this context, the normalized frequency  $x$  is to be considered a constant.

The fact that  $|Zout(1,k)| = 0$  confirms once more that at the upper resonance frequency the LLC tank behaves as an ideal voltage source. At different frequencies the output voltage is given by:

$$av_{sec1}(x) = M_0(x,k)v_{HB1}(x) \frac{Re}{Re + Zout(x,k)} , \quad (109)$$

while the output current will be:

$$\frac{i_{sec1}(x)}{a} = \frac{av_{sec1}(x)}{Re} . \quad (110)$$

The output characteristic of the LLC tank, i.e., the relationship that links the amplitude of  $i_{sec1}(x)/a$  to  $a \cdot v_{sec1}(x)$  with a given  $v_{HB1}(x)$  can be found by substituting (110) in (109) and then extracting the modulus of both sides of the resulting equation. The result, obtained after some algebraic manipulations, is:

$$(av_{sec1})^2 + \left( \frac{i_{sec1}}{a} \right)^2 |Zout(x,k)|^2 = |M_0(x,k)|^2 V_{HB1}^2 , \quad (111)$$

where  $V_{sec1}$ ,  $I_{sec1}$  and  $V_{HB1}$  are the moduli (rms value) of the phasors  $v_{sec1}(x)$ ,  $i_{sec1}(x)$  and  $v_{HB1}(x)$  respectively. Therefore, at a given frequency  $x$  the output characteristic is elliptical.

Introducing the open-circuit output voltage  $V_{sec1.o}$ :

$$a V_{sec1.o} = |M_0(x,k)| V_{HB1} , \quad (112)$$

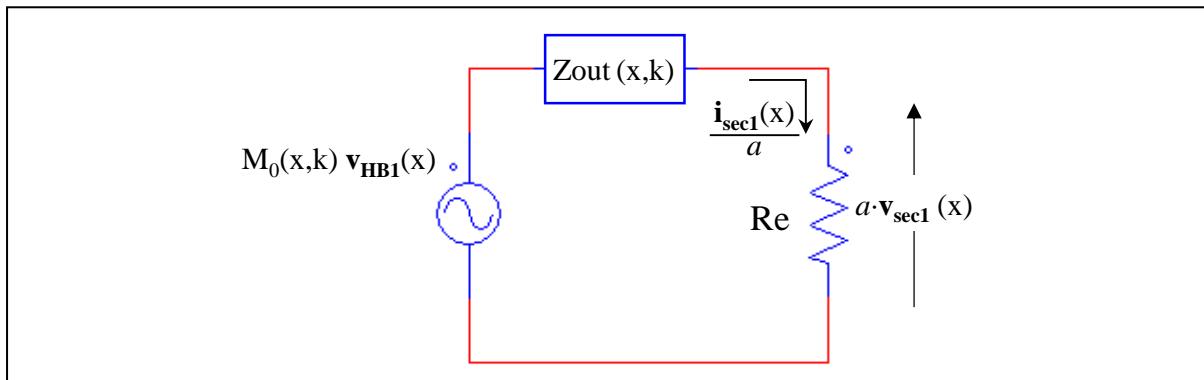
and the short-circuit output current  $I_{sec1.s}$ :

$$\frac{I_{sec1.s}}{a} = \frac{|M_0(x,k)|}{|Zout(x,k)|} V_{HB1} = \frac{a V_{sec1.o}}{|Zout(x,k)|} , \quad (113)$$

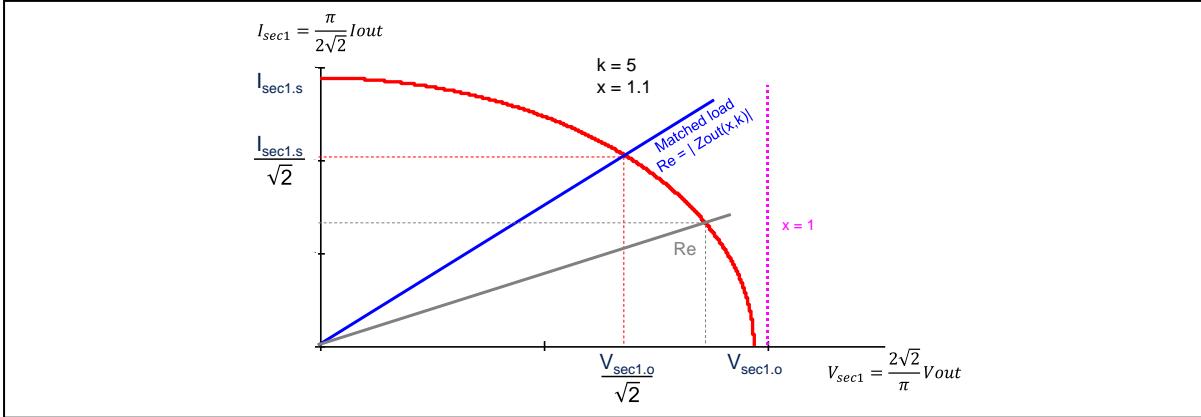
(111) can be rewritten as:

$$\frac{V_{sec1}^2}{V_{sec1.o}^2} + \frac{I_{sec1}^2}{I_{sec1.s}^2} = 1 . \quad (114)$$

**Figure 82. Thevenin-equivalent circuit that models the output port of the LLC tank.**



**Figure 83. Output characteristic of the LLC tank for a fixed frequency value.**



The ratio  $|M_0(x,k)|/|Zout(x,k)|$  in (113) is a function of  $x$  only:

$$\frac{|M_0(x,k)|}{|Zout(x,k)|} = \frac{1}{Z_0} \frac{x^2}{|x^2 - 1|}. \quad (115)$$

Figure 83 shows the plot of (114), which describes how, at a given switching frequency, the output voltage amplitude varies as the circuit is loaded. The output voltage at a given load is determined by the intersection of the elliptical characteristic (114) with the voltage-current characteristic of the load. For example, figure 83 also illustrates a superimposed resistive load line having slope  $1/Re$ .

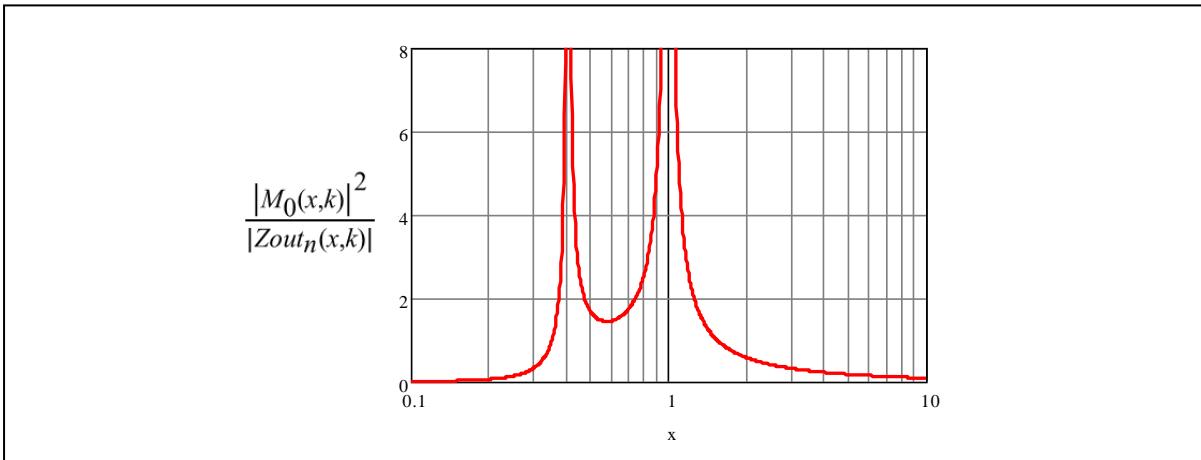
Notice that if  $x = 1$  the ellipse degenerates into a vertical straight line, which is the characteristic of an ideal voltage source in the  $V_{sec1}$ - $I_{sec1}$  plane.

Also notice that the axes can be rescaled in terms of the dc output voltage  $Vout$  and the dc output current  $lout$ . The product  $V_{sec1} \cdot I_{sec1} = Vout \cdot lout$  is the output power of the converter, graphically identified by the area of the rectangle whose opposite vertices are the origin and the intersection point with the characteristic of the load.

In the special case where  $Re = |Zout(x,k)|$  we have the so-called *matched-load operation*, in which the power output by the converter is maximized. It is possible to prove that in this case the operating point is located at  $(V_{sec1.o}/\sqrt{2}, I_{sec1.s}/\sqrt{2})$ . The maximum deliverable power is:

$$P_{out,x} = \frac{1}{2} V_{sec1.o} I_{sec1.s} = \frac{1}{2} \frac{|M_0(x,k)|^2}{|Zout(x,k)|} V_{HB1}^2. \quad (116)$$

**Figure 84. Plot of the quantity  $|M_0(x,k)|^2/|Zout_n(x,k)|$ .**



The quantity  $|M_0(x,k)|^2/|Z_{out}(x,k)|$  in (116) is given by:

$$\frac{|M_0(x,k)|^2}{|Z_{out}(x,k)|} = \frac{1}{Z_0} \frac{k x^3}{|(x^2-1)[(1+k)x^2-1]|}, \quad (117)$$

whose plot, normalized to  $Z_0$ , is drawn in figure 84.

The matched-load condition, considering (105) and (71), can be expressed as:

$$k \left| \frac{x^2-1}{(1+k)x^2-1} \right| x = \frac{1}{Q}. \quad (118)$$

It is interesting to determine where the locus of the matched-load operation is located on the  $x - |M(x,k,Q)|$  plane. To do so, considering only  $x > x_{R2}$ , (118) can be rewritten as follows:

$$Q = \frac{1}{k x} \frac{(1+k)x^2-1}{\sqrt{(x^2-1)^2}}, \quad (119)$$

and substituted into (95). The result is:

$$H_{ML}(x, k) = \frac{\sqrt{2}}{2} \frac{k x^2}{(1+k)x^2-1}. \quad (120)$$

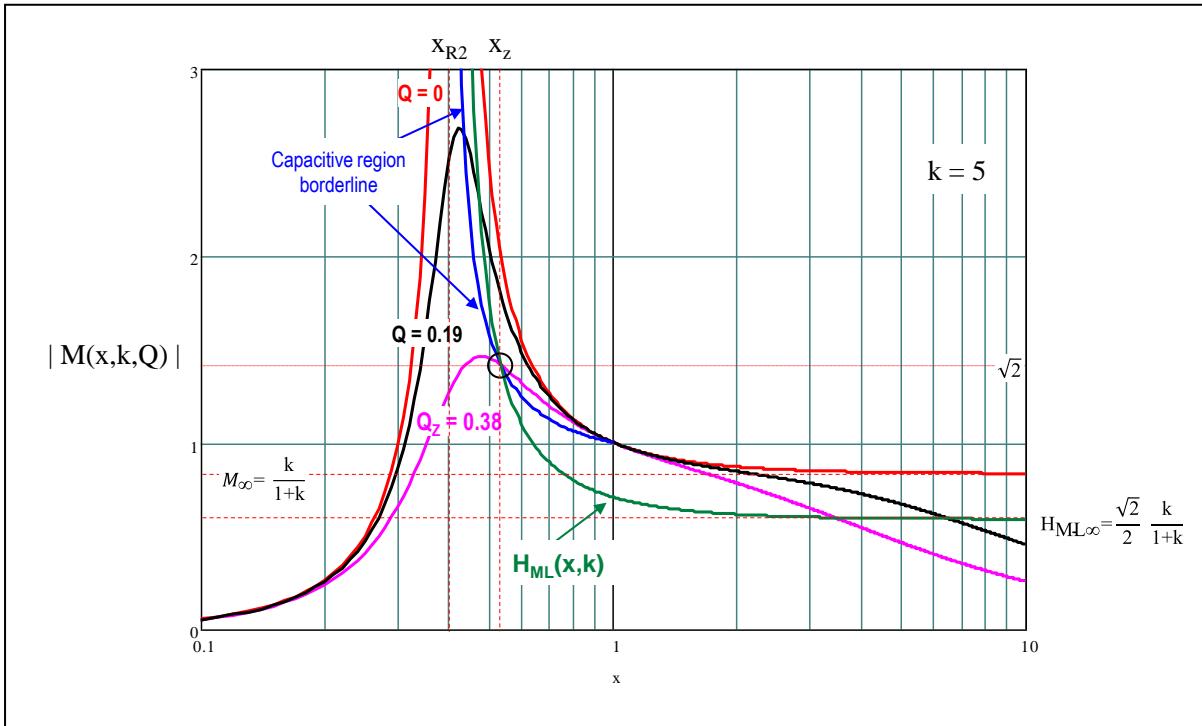
Its plot on the  $x - |M(x,k,Q)|$  plane is shown in figure 85. The frequency at which there is matched-load operation for a given voltage gain  $M$  is found by setting  $H_{ML}(x, k) = M$  in (120) and solving the resulting equation for  $x$ :

$$x_{ML} = \sqrt{\frac{1}{1 + \left(1 - \frac{\sqrt{2}}{2} \frac{1}{M}\right)k}}. \quad (121)$$

Substituting (121) in (119) yields the value of  $Q$  necessary to achieve matched-load operation for a given voltage gain  $M$ :

$$Q_{ML} = \frac{1}{k} \frac{\sqrt{2M + (2M - \sqrt{2})k}}{M(2M - \sqrt{2})}. \quad (122)$$

**Figure 85. Plot of  $H_{ML}(x, k)$  on the  $x - |M(x, k, Q)|$  plane.**



The function  $H_{ML}(x,k)$  has a vertical asymptote when  $x \rightarrow x_{R2}$  and a horizontal asymptote for  $x \rightarrow \infty$  located at

$$H_{ML\infty} = \frac{\sqrt{2}}{2} \frac{k}{1+k}, \quad (123)$$

lower than the horizontal asymptote  $M_\infty (= k/(1+k))$ .

Notice that the intersection of the locus of  $H_{ML}(x,k)$  and the capacitive region borderline occurs at  $x = x_z$ , the frequency of the load-independent point for the input impedance, where the voltage gain  $M$  equals  $\sqrt{2}$ . This can be easily demonstrated by equating (120) to (99).

For frequencies in the interval  $x_z < x < 1$  the locus lies in the capacitive region, then matched-load operation occurs without ZVS. For  $x < x_z$  matched-load operation may occur with ZVS but only if the voltage gain is larger than  $\sqrt{2}$ . Matched-load operation with ZVS may occur also above resonance ( $x > 1$ ) if  $Q$  is sufficiently large, but the gain should be lower than  $M_\infty$ , which would make it impossible output voltage regulation when  $Q$  is lower than a certain value.

In practice, matched-load operation will almost never occur in a real-world LLC converter.

## Chapter 5

### FHA approach: modeling feedback reversal at light load

In the description of the no-load operation, it was highlighted that the combined effect of the transformer's end-to-end capacitance of the secondary windings and the junction capacitance of the secondary rectifiers may cause a reversal of the power-frequency relationship. Now we want to analyze and quantify this phenomenon using the FHA approach.

As mentioned in the time-domain analysis, all these contributors can be lumped into a single capacitor and reflected to the primary side through the turns ratio. This capacitor  $C_p$  in parallel to  $L_p$  turns the LLC tank into a fourth-order LLCC tank. It is necessary to distinguish the cases of the center-tap full-wave rectification (CT-FW) and of the single-ended bridge (SE-B) rectification that are shown in figure 86.

With reference to the CT-FW configuration, assuming for simplicity that  $C_{2a} = C_{2b} = C_2$  and that  $C_{j1} = C_{j2} = C_j$ , the value of  $C_p$  will be:

$$C_p = \frac{2}{a^2} (C_2 + C_j) . \quad (124)$$

As regards the SE-B configuration, assuming for simplicity that  $C_{j1} = C_{j2} = C_{j3} = C_{j4} = C_j$ , the value of  $C_p$  will be:

$$C_p = \frac{1}{a^2} (C_2 + C_j/2 + C_j/2) = \frac{1}{a^2} (C_2 + C_j) . \quad (125)$$

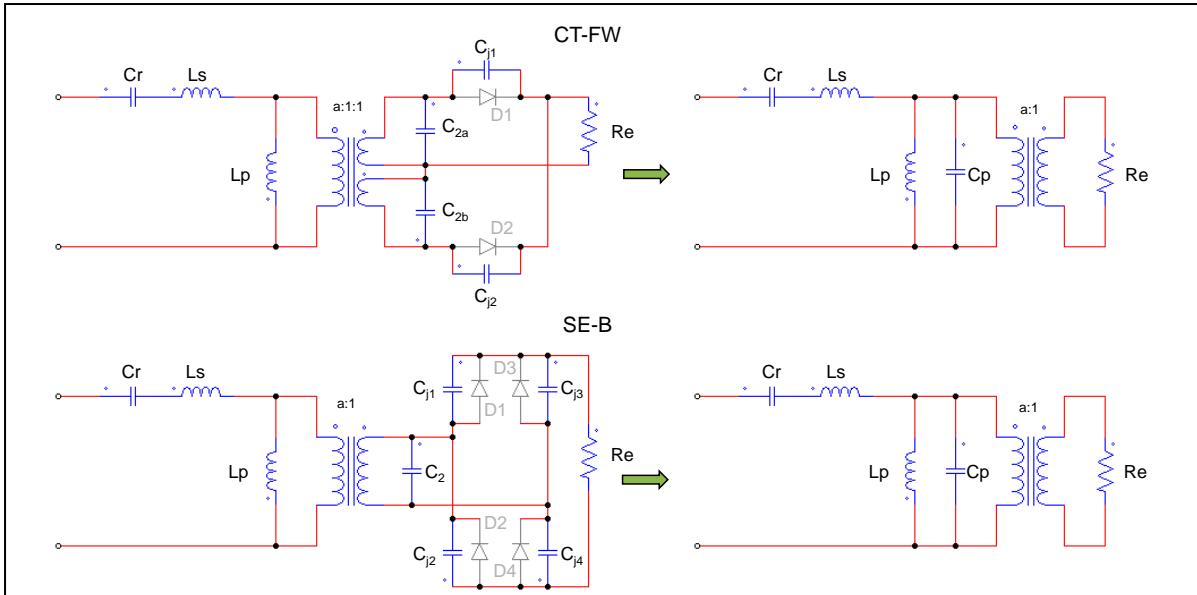
Introducing the parameter  $\Gamma = C_p/C_r$ , the voltage gain of this LLCC resonant tank has the following expression:

$$M'(x, k, \Gamma, Q) = \frac{1}{1 + \frac{1}{k} \left(1 - \frac{1}{x^2}\right) + \Gamma(1 - x^2) + jQ \left(x - \frac{1}{x}\right)} . \quad (126)$$

The expression of its magnitude is:

$$|M'(x, k, \Gamma, Q)| = \sqrt{\left[1 + \frac{1}{k} \left(1 - \frac{1}{x^2}\right) + \Gamma(1 - x^2)\right]^2 + Q^2 \left(x - \frac{1}{x}\right)^2} . \quad (127)$$

**Figure 86. Lumping transformer's and secondary rectifier's capacitances into  $C_p$ .**



In figure 87 we can see the plot of  $|M(x, k, \Gamma, Q)|$  with fixed  $k$  and  $\Gamma$ , for different  $Q$  values, along with the curve  $|M(x, k, 0, 0)| = |M(x, k, 0)|$  (the dotted red one), i.e., the no-load voltage gain of the LLC tank without the parasitic capacitor  $C_p$ . For  $Q = Q_Z = 0.38$  the curve tends to zero similarly to the curves of  $|M(x, k, Q)|$ ; the curve for  $Q = 0.19$  decreases and stays flat for a while before tending to zero at higher frequencies; the curve for  $Q = 0.13$  starts increasing at about  $x = 2$ , peaks and finally drops to zero at higher frequencies. In the frequency region where the slope is positive, we have feedback reversal.

The  $Q = 0$  red curve, after reaching the minimum value  $|M'_{0min}(k, \Gamma)|$

$$|M'_{0min}(k, \Gamma)| = \frac{k}{1+k(1+\Gamma)-2\sqrt{k\Gamma}} \quad (128)$$

at

$$x = x_V = \sqrt[4]{\frac{1}{k\Gamma}}, \quad (129)$$

starts rising (i.e., feedback reversal), and goes to infinity at

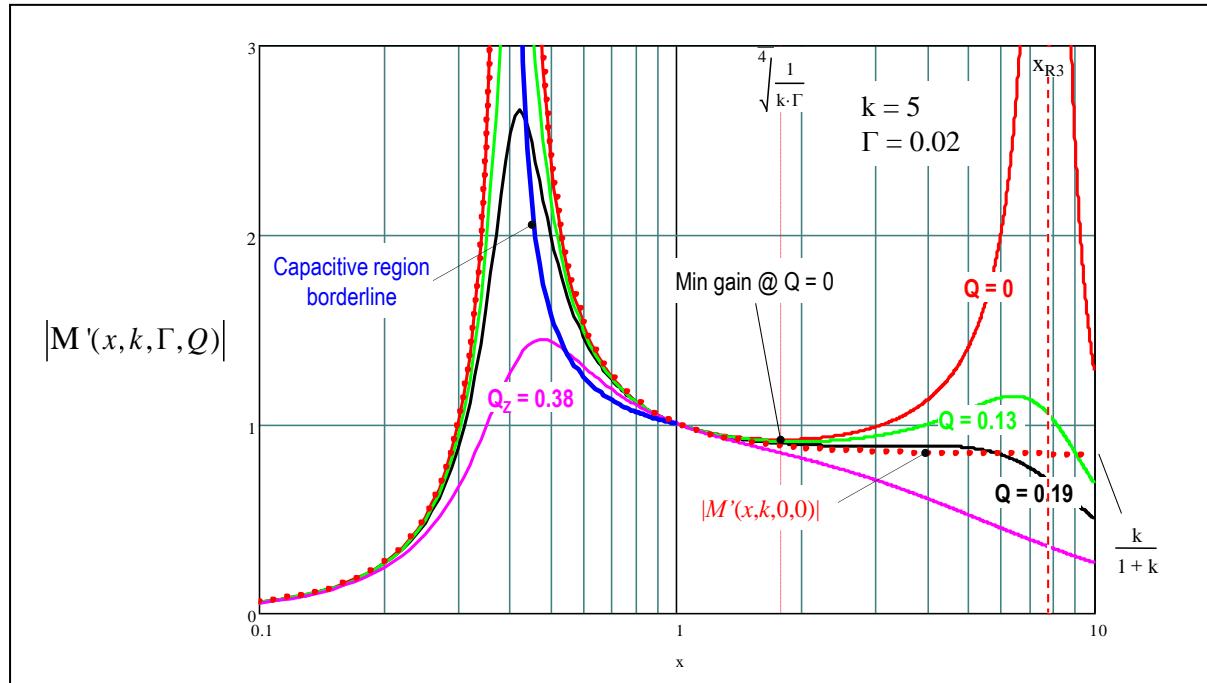
$$x = x_{R3} = \sqrt{\frac{1+k(\Gamma+1)+\sqrt{k\Gamma[k(\Gamma+2)-2]+(k+1)^2}}{2k\Gamma}}. \quad (130)$$

The minimum gain  $|M'_{0min}(k, \Gamma)|$  of the red curve is higher than the asymptotic value  $M_\infty$  of the dotted red line given by (97) for any value of  $k$  and  $\Gamma$ , as shown in the diagram of figure 88, where  $M_\infty$  is the value of  $|M'_{0min}(k, 0)|$ .

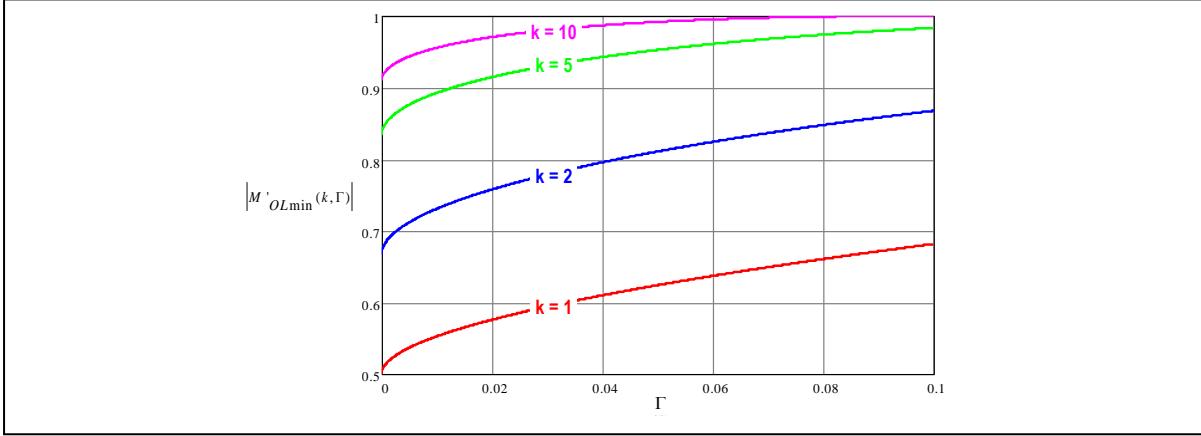
This means that, if the no-load (normalized) operating frequency is allowed to exceed  $x_V$  or the required gain to keep the output voltage regulated is lower than  $|M'_{0min}(k, \Gamma)|$ , the control loop of the converter will force the operating frequency to increase over  $x_V$ , in the attempt to keep the output voltage regulated, with a consequent feedback reversal.

The operating frequency will then jump to the maximum programmed value and the output voltage will drift high until energy balance is found at some point. Essentially, the system loses control, thus jeopardizing itself and the load.

**Figure 87. Plot of  $|M(x, k, \Gamma, Q)|$ .**



**Figure 88. Plot of  $|M'_{OLmin}|$  as a function of  $\Gamma$  for different values of  $k$ .**



The FHA model provides a partial view of the phenomenon. In fact, the FHA foresees feedback reversal only in the above resonance region, whereas the time domain analysis done in Part III, Chapter 1 shows that it may happen below resonance too. Considering the predictions above resonance, the FHA model provides an optimistic estimate of its onset: the actual voltage impressed to the tank circuit is the square wave  $V_{HB}(t)$ , and the contribution of the higher-order harmonics of the input voltage is enhanced by the gain characteristic having a larger gain for  $x > x_V$ . Feedback reversal then appears at frequencies lower and at loads higher than expected.

To avoid this problem, the capacitor ratio  $\Gamma$  must be minimized, trying to reduce  $C_2$  and  $C_i$  as much as possible (in other words, to achieve a transformer's self-resonance frequency as high as possible) and limiting the maximum operating frequency of the converter well below  $x_V$ . As to the effect of the inductance ratio  $k$ , a design with a higher value of  $k$  features a higher  $M_\infty$  but a lower rise of  $|M'_{OLmin}(k, \Gamma)|$  with the same value of  $\Gamma$ .

The problem of feedback reversal appears to be more critical in case of high output voltages; this happens because  $C_2$  increases with the turn number  $N_{sec}$  and the turns ratio  $a$  is smaller.

Being equal everything else, with the SE-B rectification the  $C_p$  value is half that with CT-FW rectification (compare (124) and (125)), which makes a converter with SE-B rectification less prone to feedback reversal. Similarly, since with the same input and output voltages and the same design criteria the turns ratio  $a$  in a full bridge is twice that in a half bridge, with equal values of  $C_2 + C_j$ , the full bridge is less prone to feedback reversal than the half bridge.

For design purposes it is useful to provide the expression of the magnitude of the input impedance under no-load conditions ( $Q = 0$ ):

$$|Zin'_{n0}(x, k, \Gamma)| = |Zin'_n(x, k, \Gamma, 0)| = \left| \left( 1 + \frac{k}{1 - k\Gamma x^2} \right) x - \frac{1}{x} \right|. \quad (131)$$

# Chapter 6

## FHA approach: ZVS conditions

Still in the spirit of a design-oriented analysis, it is necessary to review the ZVS conditions within the FHA approach. We will examine the two extreme conditions (no-load at maximum input voltage and full load at minimum input voltage) separately. A fixed dead-time  $T_D$  will be assumed.

*No-load operation.*

The necessary and sufficient condition for ZVS at no load  $T_T < T_D$  requires that the tank current at the transition instants be greater than a minimum value. From (23):

$$|I_{R0}| > \frac{V_{in}}{T_D} C_{HB}. \quad (132)$$

Under no-load conditions the tank current is purely reactive, then it lags the voltage  $V_{HB1}(t)$  by 90 degrees ( $\varphi = \pi/2$ ). Therefore, under these conditions (52) becomes:

$$i_{R1}(t) = -\sqrt{2} I_{R1} \cos 2\pi f_{sw} t. \quad (133)$$

$I_{R1}$  can be derived by dividing  $V_{HB1}$  given by (51) by the module of the input impedance at no load given by (85) in its normalized form. Therefore:

$$I_{R1} = \begin{cases} \frac{\sqrt{2} V_{in}}{\pi Z_0} \frac{x}{|(1+k)x^2-1|} & (\text{HB}) \\ \frac{2\sqrt{2} V_{in}}{\pi Z_0} \frac{x}{|(1+k)x^2-1|} & (\text{FB}) \end{cases}. \quad (134)$$

The transitions of the half or full bridge occur when the argument of the cosine function is  $0, \pi, 2\pi, \dots$ , therefore the current  $I_{R0}$  is the peak value of  $i_{R1}(t)$  given by (133):

$$I_{R0} = \begin{cases} \frac{2 V_{in}}{\pi Z_0} \frac{x}{|(1+k)x^2-1|} & (\text{HB}) \\ \frac{4 V_{in}}{\pi Z_0} \frac{x}{|(1+k)x^2-1|} & (\text{FB}) \end{cases}. \quad (135)$$

If we introduce (135) in (132) and consider (71), the ZVS condition sets a constraint on the maximum value of Q:

$$Q < \begin{cases} \frac{2}{\pi} \frac{x}{|(1+k)x^2-1|} \frac{T_D}{Re C_{HB}} & (\text{HB}) \\ \frac{4}{\pi} \frac{x}{|(1+k)x^2-1|} \frac{T_D}{Re C_{HB}} & (\text{FB}) \end{cases}. \quad (136)$$

If a preliminary estimate of the parasitic capacitor  $C_p$  suggests that its effect cannot be neglected,  $I_{R1}$  and  $I_{R0}$  are derived by dividing  $V_{HB1}$  by the module of the input impedance at no load given by (131). In this case the upper limit on Q becomes:

$$Q < \begin{cases} \frac{2}{\pi} \left| \frac{x(1-k\Gamma x^2)}{k\Gamma(x^2-x^4)(1+k)x^2-1} \right| \frac{T_D}{Re C_{HB}} & (\text{HB}) \\ \frac{4}{\pi} \left| \frac{x(1-k\Gamma x^2)}{k\Gamma(x^2-x^4)(1+k)x^2-1} \right| \frac{T_D}{Re C_{HB}} & (\text{FB}) \end{cases}. \quad (137)$$

*Full-load operation at minimum operating frequency.*

Under these operating conditions the ZVS condition (132) is only necessary. Following a flow similar to that used for the no-load operation, we consider the expression (52) of the tank current, reported here below for reader's convenience:

$$i_{R1}(t) = \sqrt{2} I_{R1} [\cos \varphi \sin 2\pi f_{sw} t - \sin \varphi \cos 2\pi f_{sw} t] , \quad (52)$$

keeping in mind that the transitions of  $V_{HB}(t)$  occur when the argument of the sine and cosine functions is  $0, \pi, 2\pi, \dots$ . Therefore, the tank current at the transition instants is:

$$|I_{R0}| = \sqrt{2} I_{R1} \sin \varphi . \quad (138)$$

In this case the value of  $I_{R1}$  can be derived from (53):

$$I_{R1} = \begin{cases} \frac{\pi}{\sqrt{2}} \frac{I_{in}}{\cos \varphi} & (\text{HB}) \\ \frac{\pi}{2\sqrt{2}} \frac{I_{in}}{\cos \varphi} & (\text{FB}) \end{cases} , \quad (139)$$

and (132) becomes:

$$\tan \varphi > \begin{cases} \frac{1}{\pi} \frac{V_{in} C_{HB}}{I_{in} T_D} & (\text{HB}) \\ \frac{2}{\pi} \frac{V_{in} C_{HB}}{I_{in} T_D} & (\text{FB}) \end{cases} . \quad (140)$$

Reminding that  $\varphi = \arg[Z_{in}(x, k, Q)]$  and considering (74), (140) can be rewritten as:

$$\frac{[1+k+Q^2 k^2(x^2-1)]x^2-1}{Qk^2x^3} > \begin{cases} \frac{1}{\pi} \frac{V_{in} C_{HB}}{I_{in} T_D} & (\text{HB}) \\ \frac{2}{\pi} \frac{V_{in} C_{HB}}{I_{in} T_D} & (\text{FB}) \end{cases} . \quad (141)$$

Now we set:

$$\Xi = \begin{cases} \frac{1}{\pi} \frac{V_{in} C_{HB}}{I_{in} T_D} & (\text{HB}) \\ \frac{2}{\pi} \frac{V_{in} C_{HB}}{I_{in} T_D} & (\text{FB}) \end{cases} , \quad (142)$$

and consider the equation

$$\frac{[1+k+Q^2 k^2(x^2-1)]x^2-1}{Qk^2x^3} = \Xi . \quad (143)$$

If we substitute the expression of  $Q$  for which the LLC tank has an assigned voltage gain  $M$  at a given frequency  $x$  (104) in (143) we obtain an equation in  $x$  whose significant solution provides the operating frequency  $x_\varphi$  where  $\tan \varphi = \Xi$  and the voltage gain is  $M$ . After some algebraic manipulations:

$$x_\varphi = M \sqrt{\frac{M^2(1+k)(1+\Xi^2)+k[\Xi \sqrt{M^2(1+\Xi^2)-1}-1]}{[M^2(1+k)-k]^2+(M\Xi)^2[M^2(1+k)^2-k^2]}} . \quad (144)$$

Substituting the value given by (144) in (104) we can find the corresponding value of  $Q_M$ ,  $Q_\varphi$ :

$$Q_\varphi = \frac{x_\varphi}{|1-x_\varphi^2|} \sqrt{\frac{1}{M^2} - \left(\frac{(k+1)x_\varphi^2-1}{kx_\varphi^2}\right)^2} . \quad (145)$$

Of course, the necessary ZVS condition will be:

$$Q < Q_\varphi . \quad (146)$$

Incidentally, notice that if in (144) we set  $\Xi = 0$ , we find again the expression of  $x_{CMB}$  (101). Also notice that it is definitely  $Q_\varphi < Q_B$ , with  $Q_B$  given by (100), and  $x_\varphi > x_{CMB}$ .

To make the ZVS condition sufficient the tank current must not change sign within the dead time. In the spirit of the FHA analysis, we can consider (52) in this form:

$$i_{R1}(t) = \sqrt{2} I_{R1} \sin(2\pi f_{sw} t - \varphi) . \quad (52)$$

The current crosses zero and changes sign at  $t = \varphi / 2\pi f_{sw}$  where the argument zeroes; therefore, the sign invariance condition is:

$$\frac{\varphi}{2\pi f_{sw}} = \frac{\varphi}{2\pi f_{R1} x} > T_D . \quad (147)$$

Equation (147) does not lend itself to simple calculations to determine a condition similar to (136) and (146). However, at the end of the design process it is possible to check if a design carried out with a  $Q$  value that fulfills (136) and (146) fulfills (147) too. If so, ZVS is ensured throughout the entire operating range and the design validated, otherwise one needs to iterate the process with a lower value of  $Q$ .

## Chapter 7

### FHA approach: LLC tank design considerations and procedure

Many degrees of freedom are available and many design procedures are possible, depending on the design objectives and constraints and on the parameters that are specified.

The first choice to make is the topology: half bridge or full bridge. It depends on several factors, here for simplicity we will consider only the power level. As a rule of thumb, with a PFC front-end a half bridge is preferable up to 500 W, over 500 W one might consider a full bridge.

Table 3 lists a typical set of electrical specifications for a draft design of an LLC resonant converter, and we will consider one of the simplest procedures based on these specifications.

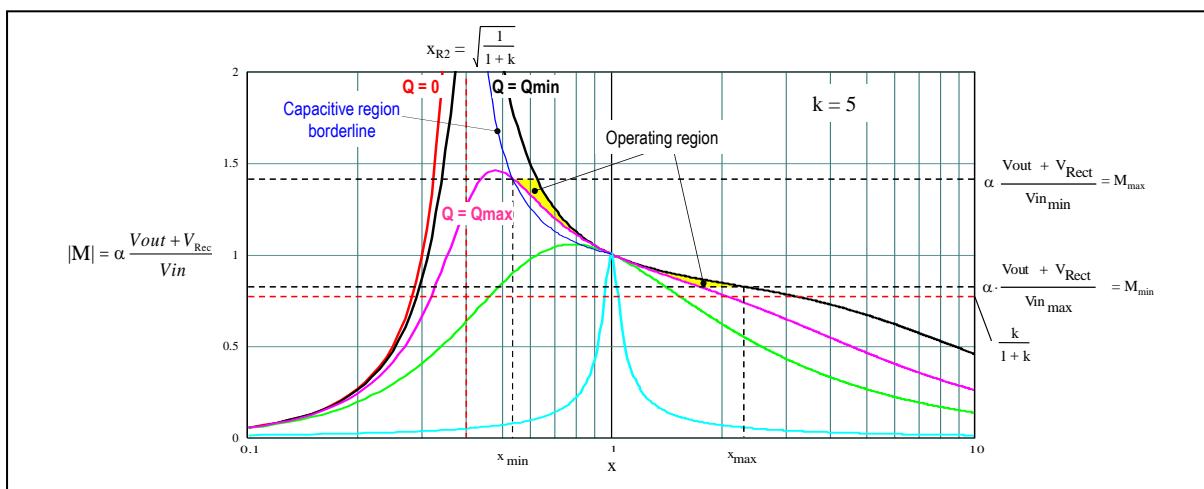
It is convenient to carry out some preliminary consideration based on the specifications of Table 3 using the  $x - M$  plane shown in figure 89.

Given the input voltage range ( $V_{in_{min}} - V_{in_{max}}$ ), it is possible to define the corresponding range for the required voltage gain  $M$ .

**Table 3. Reference electrical specification**

Symbol	Name	Unit
$V_{in_{min}} - V_{in_{max}}$	Input voltage range	Vdc
$V_{in_{nom}}$	Nominal input voltage	Vdc
$V_{out}$	Regulated output voltage	Vdc
$V_{Rect}$	Secondary rectifier average forward drop	Vdc
$P_{out_{min}} - P_{out_{max}}$	Output power range	W
$\eta$	Expected full-load efficiency	%
$f_{R1}$	Upper resonance frequency	kHz
$f_{max}$	Maximum switching frequency	kHz
$C_{HB}$	Half bridge midpoint(s) estimated capacitance	pF
$T_D$	Dead-time	ns

**Figure 89. LLC operating region on  $x - |M(x, k, Q)|$  plane.**



Based on (66),  $M$  can be expressed as:

$$M = \alpha G_V = \alpha \frac{V_{out} + V_{Rect}}{V_{in}} , \quad (148)$$

with  $\alpha = 2a$  in the half bridge and  $\alpha = a$  in the full bridge. In applications where the output voltage is regulated ( $V_{out} = \text{const.}$ ) it is:

$$M_{min} = \alpha \frac{V_{out} + V_{Rect}}{V_{in_{max}}} \quad M_{max} = \alpha \frac{V_{out} + V_{Rect}}{V_{in_{min}}} . \quad (149)$$

Three types of operation are possible:

- always below the resonance frequency ( $M_{min} > 1$ , step-up only operation)
- always above the resonance frequency ( $M_{max} < 1$ , step-down only operation)
- across the resonance frequency ( $M_{min} < 1 < M_{max}$ , step-up/down operation).

The position of the operating region depends solely on the transformer turns ratio  $a$ . The third option, shown in the diagram of figure 89, is normally the preferred choice to benefit of the operation at the load-independent point. Considering a fixed  $V_{out}$ , the vertical axis can be rescaled in terms of  $V_{in}$ .

The load range ( $P_{out_{min}}, P_{out_{max}}$ ) determines a corresponding range ( $Q_{min}, Q_{max}$ ) for the quality factor  $Q$ . From (71):

$$Q_{min} = \frac{\pi^2}{8} \frac{Z_0}{a^2} \frac{P_{out_{min}}}{V_{out}^2} \frac{1}{1 + \frac{V_{Rect}}{V_{out}}} \quad Q_{max} = \frac{\pi^2}{8} \frac{Z_0}{a^2} \frac{P_{out_{max}}}{V_{out}^2} \frac{1}{1 + \frac{V_{Rect}}{V_{out}}} . \quad (150)$$

In some cases, it is  $P_{out_{min}} = 0$  (so that  $Q_{min} = 0$ ); we will refer to this extreme case even when  $P_{out_{min}} > 0$  and  $Q_{min} > 0$  to account for some design margin against the inaccuracy of the FHA model.  $Q_{max}$ , based on the previous discussion, will be such that conditions (136), (146) and (147) are all met. If  $a$  is fixed, this will be accomplished by a proper choice of the characteristic impedance  $Z_0$ .

The intersection between the  $|M(x, k, Q_{max})|$  curve and the horizontal line  $M = M_{max}$  determines the minimum operating frequency  $x_{min}$ ; similarly, the intersection between the  $|M(x, k, Q_{min})|$  curve and the horizontal line  $M = M_{min}$  determines the maximum operating frequency  $x_{max}$ .

For a given input voltage (i.e., for a given horizontal line  $M$ ), when the load changes from the minimum to the maximum, the corresponding operating point sweeps the segment of the horizontal line  $M$  included between the intersections with the curves  $|M(x, k, Q_{min})|$  and  $|M(x, k, Q_{max})|$ . The closer to  $M = 1$  the horizontal line is, the shorter this segment is and, therefore, the smaller the corresponding frequency change is. It is apparent that the switching frequency is much more depending on  $M$  (i.e., on the input voltage  $V_{in}$ ) rather than on  $Q$  (i.e., on the load).

In the end, the four corners operating conditions of the LLC converter identify the small area of the  $x - M$  plane highlighted in yellow in figure 89. Notice that in figure 89  $Q_{max} = Q_B$ , so that the operating region in yellow extends down to the capacitive region borderline. In a real design  $Q_{max}$  will be lower than  $Q_B$  to ensure ZVS, so the actual operating region will be a little narrower.

The design strategy is based on the following cornerstones:

1. The LLC tank will be designed to work at resonance at nominal  $V_{in}$  ( $V_{in_{nom}}$ ) to benefit of the operation at the load-independent point. In a typical application an LLC converter is cascaded to a PFC pre-regulator and  $V_{in_{nom}}$  is its regulated output voltage.

2. Operation above resonance will be used to handle the subrange ( $V_{in_{nom}}, V_{in_{max}}$ ). This handles PFC's output overvoltage conditions that may occur when the load drops abruptly or is completely disconnected.
3. Operation below resonance will be used to handle the subrange ( $V_{in_{min}}, V_{in_{nom}}$ ). This handles the undershoots of the output voltage of the PFC pre-regulator caused by an abrupt load increase or the mains voltage anomalies (dips/sags, missing cycles) that cause the PFC stage to temporarily stop delivering power while the LLC converter is delivering the maximum power, energized only by the PFC's output bulk capacitor.
4.  $Q$  will be chosen so that converter will always work with ZVS, from zero load to  $P_{out_{max}}$ , from  $V_{in_{min}}$  to  $V_{in_{max}}$ .

Based on point 1 of the strategy, the transformer's turns ratio  $\alpha$  can be easily set: being  $M = 1$  at resonance and taking into account the forward drop of the secondary rectifiers too, from (148):

$$\alpha = \frac{V_{in_{nom}}}{V_{out} + V_{Rect}} \rightarrow \alpha = \begin{cases} \frac{1}{2} \frac{V_{in_{nom}}}{V_{out} + V_{Rect}} & (\text{HB}) \\ \frac{V_{in_{nom}}}{V_{out} + 2V_{Rect}} & (\text{FB}) \end{cases}. \quad (151)$$

Notice that with this selection (149) can be rewritten as follows:

$$M_{min} = \frac{V_{in_{nom}}}{V_{in_{max}}}, \quad M_{max} = \frac{V_{in_{nom}}}{V_{in_{min}}}. \quad (152)$$

Concerning point 2 of the strategy, the most severe condition is when the load of the LLC resonant converter is disconnected and the output overvoltage protection (OVP) of the PFC is triggered. The converter must be able to regulate with no load at the maximum input voltage ( $V_{in_{max}} = \text{PFC's OVP threshold}$ ) at the specified operating frequency  $f_{max}$ .

This requirement can be met by imposing that the minimum required gain  $M_{min}$ , calculated with  $\alpha$  fixed as per (151), be equal to  $|M_0(x_{max}, k)|$  (96). This provides an equation that can be solved for  $k$  yielding the required value for the  $L_p/L_s$  ratio:

$$k = \frac{M_{min}}{1 - M_{min}} \frac{x_{max}^2 - 1}{x_{max}^2}. \quad (153)$$

If a preliminary estimate of the parasitic capacitor  $C_p$  suggests that its effect cannot be neglected,  $M_{min}$  can be equated to  $|M(x_{max}, k, \Gamma, 0)|$ . The resulting equation, solved for  $k$  yields:

$$k = \frac{M_{min}(x_{max}^2 - 1)}{M_{min}[\Gamma(x_{max}^4 - x_{max}^2) - x_{max}^2] + x_{max}^2}. \quad (154)$$

Points 3 and 4 of the strategy are interrelated: in fact, the major concern in properly handling point 3 is to ensure the converter operates with ZVS even when  $V_{in} = V_{in_{min}}$  and  $P_{out} = P_{out_{max}}$ . The input current  $I_{in}$  ( $= P_{in}/V_{in} = P_{out}/\eta/V_{in}$ ) needs to be calculated in these conditions to find an estimate of  $\Xi$  with (142):

$$\Xi = \begin{cases} \frac{\eta}{\pi} \frac{V_{in_{min}}^2}{P_{out_{max}}} \frac{C_{HB}}{T_D} & (\text{HB}) \\ \frac{2\eta}{\pi} \frac{V_{in_{min}}^2}{P_{out_{max}}} \frac{C_{HB}}{T_D} & (\text{FB}) \end{cases}. \quad (155)$$

Once  $\Xi$  is known, equations (144) and (145) with  $k$  given by (153) or (154) and  $M = M_{max}$  can be used to calculate  $x_\phi$  and  $Q_\phi$  respectively. Selecting a value  $Q < Q_\phi$  will presumably ensure ZVS when  $V_{in} = V_{in_{min}}$  and  $P_{out} = P_{out_{max}}$ , unless the final check with (145) will say otherwise.

To ensure ZVS on the other extreme of the operating range ( $V_{in} = V_{in_{max}}, P_{out} = 0$ ), the condition (136) calculated with  $k$  given by (153) or the condition (137) calculated with  $k$  given

by (154) and  $x = x_{max}$ , provides a further upper limit  $Q_{OL}$  for  $Q$ . Of course, to ensure ZVS throughout the entire operating range,  $Q$  will be selected so that:

$$Q < \min(Q_\varphi, Q_{OL}). \quad (156)$$

Once a value  $Q_S$  fulfilling (156) has been selected, we have all the info to completely define the LLC tank. From (68)-(71) we can derive:

$$Z_0 = Re Q_S; \quad Cr = \frac{1}{2\pi f_{R1} Z_0}; \quad Ls = \frac{Z_0}{2\pi f_{R1}}; \quad Lp = k Ls. \quad (157)$$

However, before validating the design, it is necessary to check that condition (147) is met when computed with  $x = x_{min}$  and the corresponding value of  $\varphi$ .  $\varphi$  can be calculated with (74) using the value of  $k$  given by (153) or (154),  $Q = Q_S$  and just  $x = x_{min}$ . Nevertheless,  $x_{min}$  is still unknown and to calculate it we should solve the equation  $|M(x, k, Q_S)| = M_{max}$  for  $x$ . The resulting 3<sup>rd</sup> order equation is difficult to handle, and we will consider an approximate analytic solution.

As shown in the plot of figure 90, the intersection of the curve  $|M(x, k, Q_S)|$  with the horizontal line  $M = M_{max}$  occurs in a point that is included between the intersection of the curve  $|M(x, k, Q_B)|$  and that of the curve  $|M_0(x, k)|$  with the same horizontal line.

The abscissa of the intersection  $|M(x, k, Q_B)| = M_{max}$  is clearly  $x_{CMB}$  given by (101), which can be conveniently rewritten as:

$$x_{CMB} = \frac{1}{\sqrt{1+k\left(1-\frac{1}{M_{max}^2}\right)}}. \quad (158)$$

The equation  $|M_0(x, k)| = M_{max}$  can be easily solved and its significant root  $x_0 (> x_{R2})$ , which provides the cutoff frequency when  $M = M_{max}$ , is:

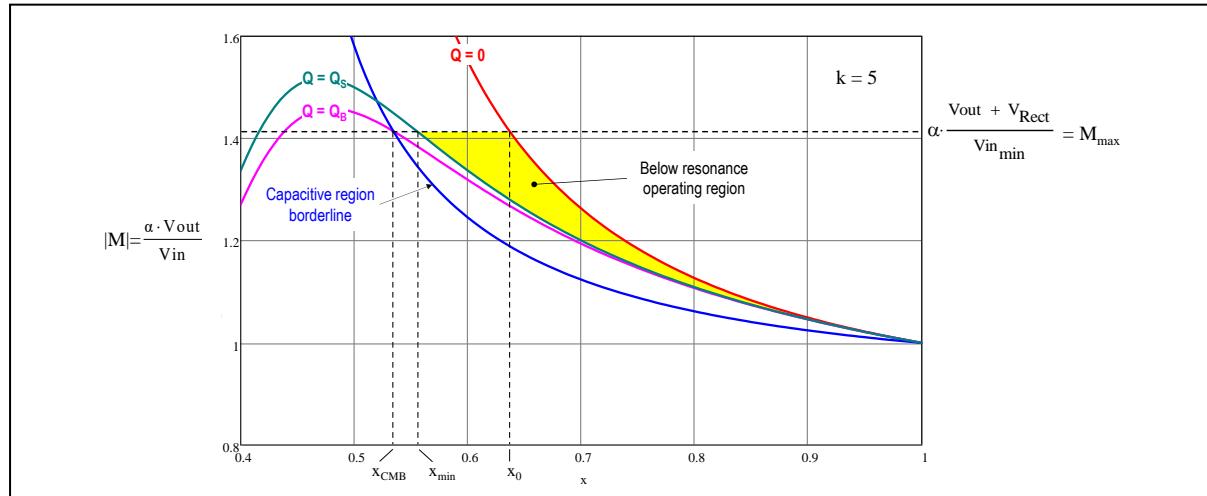
$$x_0 = \frac{1}{\sqrt{1+k\left(1-\frac{1}{M_{max}}\right)}}. \quad (159)$$

We can suppose that the approximate solution of the equation  $|M(x, k, Q_S)| = M_{max}$  can be given an expression similar to (158), (159) where the exponent of  $M_{max}$  is included between 1 and 2. This exponent must be a function of  $Q_S$  that provides values monotonically increasing from 1 to 2 when  $Q_S$  varies from 0 to  $Q_B$ .

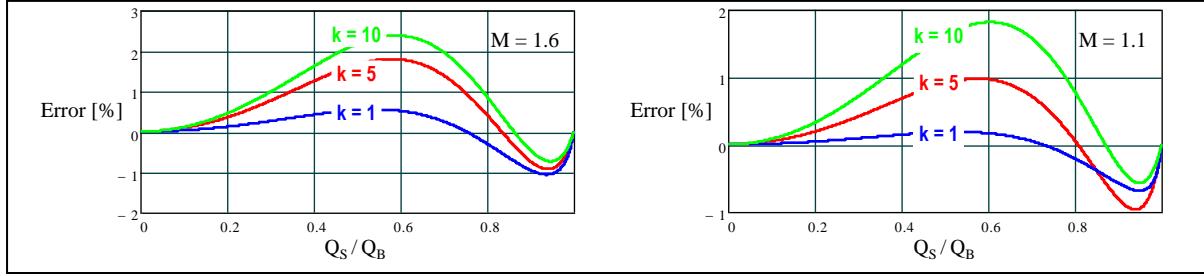
A simple function that provides a good approximation is the following:

$$F(Q_S) = 1 + \left(\frac{Q_S}{Q_B}\right)^q. \quad (160)$$

**Figure 90. Below resonance operating region on  $x$ - $|M(x, k, Q)|$  plane.**



**Figure 91. Relative error of  $x_{min}$  computed with (161) wrt exact solution, with  $q = 5$ .**



As shown in the plots of figure 91, with  $q = 5$  the error is kept very close to  $\pm 1\%$  in the range  $(0.8 Q_B, Q_B)$  that is the most interesting from the practical point of view, and below  $+3\%$  in the range  $(0, Q_B)$ . The span considered for  $k$  and  $M$  covers most practical cases. Therefore:

$$x_{min} \cong \frac{1}{\sqrt{1+k \left( 1 - \frac{1}{M_{max}} \left( 1 + \left( \frac{Q_S}{Q_B} \right)^5 \right) \right)}} . \quad (161)$$

The value of  $x_{min}$  thus calculated will be used not only to check if the condition (147) for ZVS is fulfilled or not but also to set the operating range of the control system that keeps the output voltage regulated: whatever control type will be used, the converter must be allowed to operate between  $f_{min} = x_{min} f_{R1}$  and  $f_{max} = x_{max} f_{R1}$ , tolerances included.

As discussed in Part III Chapter 2, in an LLC resonant converter (like in any power converter) it is necessary to provide overcurrent/overpower protection circuits to prevent the power components from overstressing in case of anomalous operating conditions such as overload or short circuit. To design an overcurrent protection circuit, it is necessary to predict the maximum amplitude of the tank current at  $V_{in} = V_{in\min}$ ,  $P_{out} = P_{out\max}$  so that the protection is triggered only when the current exceeds this maximum expected value.

Based on (53) and (54), the peak value  $I_{R1pk} = \sqrt{2} I_{R1}$  of the tank current can be found with.

$$I_{R1pk} = \begin{cases} \frac{\pi}{\eta} \frac{P_{out\max}}{V_{in\min} \cos \varphi_{min}} \frac{1}{k^2} & (\text{HB}) \\ \frac{\pi}{2\eta} \frac{P_{out\max}}{V_{in\min} \cos \varphi_{min}} \frac{1}{k^2} & (\text{FB}) \end{cases} \quad (162)$$

where  $\varphi_{min}$  is the phase-shift of the tank current that can be calculated with (74):

$$\varphi_{min} = \arg[Z_{in}(x_{min}, k, Q_S)] = \tan^{-1} \frac{[1+k+Q_S^2 k^2(x_{min}^2-1)]x_{min}^2-1}{Q_S k^2 x_{min}^3} . \quad (163)$$

In the end:

$$\cos \varphi_{min} = \frac{1}{\sqrt{1 + \left\{ \frac{[1+k+Q_S^2 k^2(x_{min}^2-1)]x_{min}^2-1}{Q_S k^2 x_{min}^3} \right\}^2}} . \quad (164)$$

The discussion presented so far can be summarized in a step-by-step design procedure able to fulfill the four points of the design strategy based on the specification given in Table 3.

Step 1. Calculate the required value of  $\alpha$  to make the converter operate at resonance at the nominal input voltage and the resulting value of the transformer turns ratio  $a$  with (151).

Step 2. Calculate the values of  $M_{min}$  and  $M_{max}$  with (152), as well as the normalized maximum switching frequency that will occur at no-load and maximum input voltage:

$$x_{max} = f_{max}/f_{R1} . \quad (165)$$

Step 3. Calculate the effective output resistance  $Re$  combining (61) and (64):

$$Re = \frac{8}{\pi^2} a^2 \frac{V_{out}^2}{P_{out,max}} \frac{1}{\left(1 + \frac{V_{Rect}}{V_{out}}\right)} \quad (166)$$

Step 4. To ensure that the converter can regulate the output voltage at no-load and maximum input voltage, calculate the  $L_p$  to  $L_s$  inductance ratio  $k$  with (153) or, in case a preliminary estimate of  $C_p$  and an educated guess of  $\Gamma = C_p/C_r$  are available and suggest differently, with (154). In the latter case, check also that  $x_{max}$  is less than  $x_V$  given by (129). If not, the specified  $f_{max}$  should be reduced or special care will need to be used to reduce  $C_p$  and  $\Gamma$ , or the use of burst-mode operation at light load is mandatory.

Step 5. To determine the maximum  $Q$  value to work with ZVS at  $V_{in} = V_{in,min}$ ,  $P_{out} = P_{out,max}$  calculate first the value of  $\Xi$  with (155) and  $x_\varphi$  from (142):

$$x_\varphi = M_{max} \sqrt{\frac{M_{max}^2(1+k)(1+\Xi^2)+k[\Xi\sqrt{M_{max}^2(1+\Xi^2)-1}-1]}{[M_{max}^2(1+k)-k]^2 + (M_{max}\Xi)^2[M_{max}^2(1+k)^2-k^2]}} \quad , \quad (167)$$

then calculate  $Q_\varphi$  from (168):

$$Q_\varphi = \frac{x_\varphi}{1-x_\varphi^2} \sqrt{\frac{1}{M_{max}^2} - \left(\frac{(k+1)x_\varphi^2-1}{kx_\varphi^2}\right)^2} \quad , \quad (168)$$

(the absolute value in  $1 - x_\varphi^2$  is not necessary since  $x_\varphi < 1$ ).

Step 6. Calculate the max  $Q$  value to work with ZVS at no-load and  $V_{in} = V_{in,max}$ ,  $Q_{OL}$ , applying (136) if  $\Gamma = C_p/C_r$  is not expected to be significant:

$$Q_{OL} = \begin{cases} \frac{2}{\pi} \frac{x_{max}}{|(1+k)x_{max}^2-1|} \frac{T_D}{Re C_{HB}} & (\text{HB}) \\ \frac{4}{\pi} \frac{x}{|(1+k)x_{max}^2-1|} \frac{T_D}{Re C_{HB}} & (\text{FB}) \end{cases} \quad , \quad (169)$$

applying (137) otherwise:

$$Q_{OL} < \begin{cases} \frac{2}{\pi} \left| \frac{x_{max}(1-k\Gamma x_{max}^2)}{k\Gamma(x_{max}^2-x_{max}^4)+(1+k)x_{max}^2-1} \right| \frac{T_D}{Re C_{HB}} & (\text{HB}) \\ \frac{4}{\pi} \left| \frac{x_{max}(1-k\Gamma x_{max}^2)}{k\Gamma(x_{max}^2-x_{max}^4)+(1+k)x_{max}^2-1} \right| \frac{T_D}{Re C_{HB}} & (\text{FB}) \end{cases} \quad . \quad (170)$$

Step 7. Calculate the value of  $Q$ ,  $Q_B$ , corresponding to the capacitive mode boundary when it is  $M = M_{max}$  from (100):

$$Q_B = \frac{1}{kM_{max}} \sqrt{\frac{M_{max}^2}{M_{max}^2-1} + k} \quad , \quad (171)$$

check that  $Q_B > Q_\varphi$  (if not there will be some calculation error somewhere), and select a value  $Q_S$  for the quality factor that fulfills (154):

$$Q_S < \min(Q_\varphi, Q_{OL}). \quad (172)$$

Step 8. Calculate the normalized minimum operating frequency at  $V_{in} = V_{in,min}$ ,  $P_{out} = P_{out,max}$ ,  $x_{min}$ , with (161).

Step 9. Calculate the phase-shift  $\varphi_{min}$  of the tank current at  $V_{in} = V_{in,min}$ ,  $P_{out} = P_{out,max}$  with (163) and check if the ZVS condition (147) is fulfilled:

$$\frac{\varphi_{min}}{2\pi f_{R1}} \frac{1}{x_{min}} > T_D \quad . \quad (173)$$

If so, proceed to step 10, otherwise choose a smaller value for  $Q_S$  and go back to step 8.

Step 10. Calculate the characteristic impedance of the tank circuit and all component values with (157).

Step 11. Considering an integrated magnetics implementation and assuming magnetic circuit symmetry, calculate the parameters of the real transformer with (32).

Step 12. Calculate the maximum peak of the tank current to set up the overcurrent means by combining (162) and (163):

$$I_{R1pk_{max}} = \begin{cases} \frac{\pi}{\eta} \frac{P_{out_{max}}}{Vin_{min}} \sqrt{1 + \left\{ \frac{[1+k+Q_S^2 k^2(x_{min}^2-1)]x_{min}^2-1}{Q_S k^2 x_{min}^3} \right\}^2} & (\text{HB}) \\ \frac{\pi}{2\eta} \frac{P_{out_{max}}}{Vin_{min}} \sqrt{1 + \left\{ \frac{[1+k+Q_S^2 k^2(x_{min}^2-1)]x_{min}^2-1}{Q_S k^2 x_{min}^3} \right\}^2} & (\text{FB}) \end{cases} . \quad (174)$$

### Remarks

1. The transformer's physical turns ratio  $n$  will be the ratio of two integer numbers, thus its value will be typically close to that resulting from the calculations in step 11 but not equal. So will be the resulting actual value of  $a$ ,  $a_a$ . Additionally, the resulting value of the resonant capacitor  $Cr$  will be unlikely one of the standard commercially available values and the closest standard value will be selected. These differences make the actual LLC tank circuit deviate from the original design.
2. The actual value  $a_a$  affects the input voltage  $Vin_{res}$  where the converter operates at resonance. If  $a$  and  $a_a$  do not differ much, the difference between  $Vin_{res}$  and  $Vin_{nom}$  may still fall within the tolerance of  $Vin_{nom}$ . If the difference is too large one might consider changing  $Vin_{nom}$  to get closer to  $Vin_{res}$ .
3. The actual value  $a_a$  affects  $M_{min}$ , which directly impacts on the no-load regulation ability. If  $a_a > a$ , the new value of  $M_{min}$  will be larger, then no load regulation is still ensured, although at a frequency lower than  $f_{max}$ . If  $a_a < a$ , the new value of  $M_{min}$  will be lower; if still larger than  $M_\infty$  (or  $|M'_{0min}(k, \Gamma)|$ ) then no load regulation will is still possible, although at a frequency higher than  $f_{max}$ . If not, there are two options:
  - a. Redo the design of the LLC tank starting from Step 4 with the  $a = a_a$ .
  - b. Try a different rounding of  $n$  that leads to an actual value  $a_a > a$ .
4. The actual value  $a_a$  affects  $Re$ , while the actual value of  $Cr$  affects  $Z_0$ . Both make the actual quality factor  $Q_a = Z_0/Re$  different from the selected value  $Q_S$ . If  $Q_a < Q_S$ , ZVS operation throughout the specified operating range is still ensured. If  $Q_a > Q_S$ , but still  $Q_a < \min(Q_\phi, Q_{OL})$  ZVS operation throughout the specified operating range is still ensured although with a lower safety margin. If  $Q_a > \min(Q_\phi, Q_{OL})$  ZVS operation is no longer ensured all over the operating range: There are two options:
  - a. Redo the design of the LLC tank starting from Step 4 with the  $a = a_a$ .
  - b. Try a different rounding of  $n$  that leads to an actual value  $a_a > a$ .
  - c. Select the standard value of  $Cr$  immediately larger than the calculated value.
 Options b. and c. can be used as an alternative or together.
5. The actual value of  $Cr$  affects the upper resonance frequency  $f_{R1}$ , which makes the actual range of operating frequency different from the specified one. If the difference is not too large, this is of no concern in most practical cases.

It is important to highlight that a similar review process will be needed when the parameters of the real physical samples of the transformer are available: the actual values of magnetizing and leakage inductance (thus the resulting values of  $L_p$  and  $L_s$ , as well as the

actual  $n$  to a ratio) will not be those calculated. However, this post-design check is much more worth being performed by simulation rather than calculation.

**Table 4. Exemplary AIO PC SMPS electrical specification**

Symbol	Name	Value	Unit
$V_{in_{min}} - V_{in_{max}}$	Input voltage range	300 - 450	Vdc
$V_{in_{nom}}$	Nominal input voltage	390	Vdc
$V_{out}$	Regulated output voltage	12	Vdc
$\Delta V_{out}$	Peak-to-peak output voltage ripple	120	mVdc
$V_{Rect}$	Secondary rectifier forward drop	0.1	Vdc
$P_{out_{min}} - P_{out_{max}}$	Output power range	0 - 240	W
$\eta$	Estimated efficiency @ $P_{out_{max}}, V_{in_{min}}$	95	%
$f_{R1}$	Upper resonance frequency	75	kHz
$f_{max}$	Maximum switching frequency	225	kHz
$C_{HB}$	Half bridge midpoint(s) estimated capacitance	200	pF
$T_D$	Dead-time	300	ns
$C_p$	Secondary-side parasitic capacitance (est.)	8	nF

### EXAMPLE

To illustrate the twelve-step design procedure previously outlined it is convenient to consider a fully developed example. Table 4 lists the electrical specification of an LLC half-bridge converter in an exemplary All-in-one (AIO) PC SMPS. Synchronous rectification will be used due the relatively low output voltage and the high efficiency target.

The LLC converter is powered by a boost PFC pre-regulator that provides a regulated bus voltage ( $V_{in_{nom}}$ ) starting from the ac line (typically, the PFC will be specified for a wide range mains 88 to 264 Vac). In case of a missing line cycle (holdup requirement) the PFC's output voltage is allowed to drop down to  $V_{in_{min}}$ . In case of load disconnection (i.e., a load transient from 100% load to no load) the PFC's output voltage may overshoot up to  $V_{in_{max}}$ .

Step 1. Calculate the required value of  $\alpha$  to make the converter operate at resonance at the nominal input voltage and the resulting value of the transformer turns ratio  $a$ :

$$a = \alpha = \frac{1}{2} \frac{V_{in_{nom}}}{V_{out} + V_{Rect}} = \frac{1}{2} \frac{390}{12 + 0.1} = 16.12 .$$

Step 2. Calculate the values of  $M_{min}$  and  $M_{max}$  as well as the normalized maximum switching frequency that will occur at no-load and maximum input voltage:

$$M_{min} = \frac{V_{in_{nom}}}{V_{in_{max}}} = \frac{390}{450} = 0.867 \quad M_{max} = \frac{V_{in_{nom}}}{V_{in_{min}}} = \frac{390}{300} = 1.3 .$$

$$x_{max} = f_{max}/f_{R1} = 225/75 = 3.$$

Step 3. Calculate the effective output resistance  $Re$ :

$$Re = \frac{8}{\pi^2} a^2 \frac{V_{out}^2}{P_{out_{max}}} \left( 1 + \frac{V_{Rect}}{V_{out}} \right) = \frac{8}{\pi^2} \cdot 16.12^2 \cdot \frac{12^2}{240} \left( 1 + \frac{0.1}{12} \right) = 127.4 \Omega .$$

Step 4. Having no clue on the value of  $\Gamma = Cp/Cr$ , to ensure that the converter can regulate the output voltage at no-load and maximum input voltage we will calculate the  $L_p$  to  $L_s$

inductance ratio  $k$  with (153). At the end of the design, we will check if the underlying assumption of a negligible effect of  $C_p$  is confirmed or not:

$$k = \frac{M_{min}}{1-M_{min}} \frac{x_{max}^2 - 1}{x_{max}^2} = \frac{0.867}{1-0.867} \frac{3^2 - 1}{3^2} = 5.794 .$$

Step 5. Calculate first the value of the quantity  $\Xi$ :

$$\Xi = \frac{\eta}{\pi} \frac{Vin_{min}^2}{Pout_{max}} \frac{C_{HB}}{T_D} = \frac{0.95}{\pi} \frac{300^2}{240} \frac{200 \cdot 10^{-12}}{300 \cdot 10^{-9}} = 0.076 .$$

Then calculate  $x_\phi$ :

$$x_\phi = M_{max} \sqrt{\frac{M_{max}^2(1+k)(1+\Xi^2) + k \left[ \Xi \sqrt{M_{max}^2(1+\Xi^2) - 1} - 1 \right]}{[M_{max}^2(1+k) - k]^2 + (M_{max}\Xi)^2 [M_{max}^2(1+k)^2 - k^2]}} = 0.562 ,$$

and finally, the maximum Q value to work with ZVS at  $Vin = Vin_{min}$ ,  $Pout = Pout_{max}$ ,  $Q_\phi$ :

$$Q_\phi = \frac{x_\phi}{1-x_\phi^2} \sqrt{\frac{1}{M_{max}^2} - \left( \frac{(k+1)x_\phi^2 - 1}{kx_\phi^2} \right)^2} = \frac{0.563}{1-0.563^2} \sqrt{\frac{1}{1.3^2} - \left( \frac{(5.794+1)0.563^2 - 1}{5.794 \cdot 0.563^2} \right)^2} = 0.367 .$$

Step 6. Calculate the max Q value to work with ZVS at no-load and  $Vin = Vin_{max}$ ,  $Q_{OL}$ :

$$Q_{OL} = \frac{2}{\pi} \frac{x_{max}}{|(1+k)x_{max}^2 - 1|} \frac{T_D}{Re C_{HB}} = \frac{2}{\pi} \frac{3}{|(1+5.794)3^2 - 1|} \frac{300 \cdot 10^{-9}}{124.5 \cdot 200 \cdot 10^{-12}} = 0.383 .$$

Step 7. Calculate the value of  $Q$ ,  $Q_B$ , corresponding to the capacitive mode boundary when it is  $M = M_{max}$ :

$$Q_B = \frac{1}{kM_{max}} \sqrt{\frac{M_{max}^2}{M_{max}^2 - 1} + k} = \frac{1}{5.794 \cdot 1.3} \sqrt{\frac{1.3^2}{1.3^2 - 1} + 5.794} = 0.381 .$$

It is actually  $Q_B > Q_\phi$ . Select a value  $Q_S$  for the quality factor lower than the smaller between  $Q_\phi$  and  $Q_{OL}$ . Let us consider about 10% margin:

$$Q_S = 0.367 \cdot 0.9 \approx 0.330 .$$

Step 8. Calculate the normalized minimum operating frequency at  $Vin = Vin_{min}$ ,  $Pout = Pout_{max}$ ,  $x_{min}$ :

$$x_{min} \cong \frac{1}{\sqrt{1+k \left( 1 - \frac{1}{M_{max}^{1+(Q_S/Q_B)^5}} \right)}} = \frac{1}{\sqrt{1+5.794 \left( 1 - \frac{1}{1.3^{1+(\frac{0.33}{0.381})^5}} \right)}} = 0.590 .$$

Step 9. Calculate the phase-shift  $\varphi_{min}$  of the tank current at  $Vin = Vin_{min}$ ,  $Pout = Pout_{max}$ , and check if ZVS condition (147) is fulfilled:

$$\varphi_{min} = \tan^{-1} \frac{[1+k+Q_S^2 k^2 (x_{min}^2 - 1)] x_{min}^2 - 1}{Q_S k^2 x_{min}^3} = \tan^{-1} \frac{[1+5.794+0.33^2 \cdot 5.794^2 (0.59^2 - 1)] 0.59^2 - 1}{0.33 \cdot 5.794^2 \cdot 0.59^3} = 0.231 \text{ rad} ;$$

$$\frac{\varphi_{min}}{2\pi f_{R1}} \frac{1}{x_{min}} = \frac{0.231}{2\pi \cdot 75 \cdot 10^3} \frac{1}{0.59} = 831 \cdot 10^{-9} \text{ s} > T_D = 250 \cdot 10^{-9} \text{ s} .$$

Step 10. Calculate the characteristic impedance of the tank circuit and all component values:

$$Z_0 = Re Q_S = 127.4 \cdot 0.33 = 42.05 \Omega;$$

$$Cr = \frac{1}{2\pi f_{R1} Z_0} = \frac{1}{2\pi \cdot 75 \cdot 10^3 \cdot 42.05} = 50.5 \text{ nF} ;$$

$$Ls = \frac{Z_0}{2\pi f_{R1}} = \frac{42.05}{2\pi \cdot 75 \cdot 10^3} = 89.2 \mu\text{H} ;$$

$$Lp = k Ls = 5.794 \cdot 89.2 \cdot 10^{-6} = 517 \mu\text{H} .$$

Step 11. Considering an integrated magnetics implementation and assuming magnetic circuit symmetry, calculate the parameters of the real transformer:

$$n = a \sqrt{1 + \frac{L_s}{L_p}} = 16.12 \sqrt{1 + \frac{1}{5.794}} = 17.46;$$

$$L_\mu = \sqrt{L_p L_1} = \sqrt{517(517 + 89.2)} = 559.8 \mu\text{H};$$

$$L_{L1} = L_1 - L_\mu = 517 + 89.2 - 559.8 = 46.4 \mu\text{H};$$

$$L_{L2} = \frac{L_{L1}}{n^2} = \frac{46.4}{17.46^2} = 0.152 \mu\text{H}.$$

Step 12. Calculate the maximum peak of the tank current to set up the overcurrent means:

$$I_{R1pk_{max}} = \frac{\pi}{\eta} \frac{P_{out_{max}}}{V_{in_{min}}} \frac{1}{\cos \varphi_{min}} = \frac{\pi}{0.95} \frac{240}{300} \frac{1}{\cos 0.231} = 2.72 \text{ A}.$$

- *Post-design checks:*

- Let us calculate the value of  $\Gamma = Cp/Cr$ .

$$\Gamma = \frac{Cp}{a^2 Cr} = \frac{8 \cdot 10^{-9}}{16.12^2 \cdot 50.5 \cdot 10^{-9}} = 6.1 \cdot 10^{-4}.$$

The normalized frequency where no-load gain reverses is:

$$x_V = \sqrt[4]{\frac{1}{k\Gamma}} = \sqrt[4]{\frac{1}{5.794 \cdot 6.1 \cdot 10^{-4}}} = 4.1 > x_{max} = 3.$$

Therefore, the initial assumption of considering negligible the effect of  $Cp$  in this design is correct.

- The ZVS condition check at  $V_{in} = V_{in_{min}}$ ,  $P_{out} = P_{out_{max}}$  has been done based on condition (23). According to the algorithm described in Part II chapter 5, we need to check if (23) is applicable. Let us calculate the value of the switched current in those conditions:

$$|I_{R0}| = I_{R1pk_{max}} \sin \varphi_{min} = 2.72 \sin 0.231 = 0.623 \text{ A}.$$

The critical value provided by (25) is:

$$I_{R0_{crit}} = \sqrt{\frac{C_{HB}}{L_s}} V_{in_{min}} = \sqrt{\frac{200 \cdot 10^{-12}}{89.2 \cdot 10^{-6}}} 300 = 0.449 \text{ A}.$$

$|I_{R0}|$  is about 40% larger than the critical value, then (23) is acceptable.

# Chapter 8

## LLC tank design improvements based on a simplified TDA

We have appreciated how the FHA approach provides considerable insight into the LLC converter's operation and properties and how the standard ac analysis can be conveniently used to deal with the circuit and derived a handy step-by-step design procedure.

However, the FHA approach cannot reveal the multi-resonant nature of the LLC converter, so it does not accurately predict the amplitude and the phase-shift of the tank current as well as the operating frequency in the below-resonance operating region, where the lower resonance frequency appears.

Unfortunately, when the input voltage is at the minimum specified value  $V_{in\min}$  the converter operates in the below resonance region; when the load is demanding the maximum power  $P_{out\max}$  too, the tank current hits the maximum peak and rms values and the switching frequency its minimum value  $f_{min}$  and these operating conditions are also those where the FHA model is less accurate (like above resonance in DCM operation).

To properly design the overcurrent/overpower protection circuits an accurate prediction of operating frequency and tank current amplitude under these conditions is needed: in fact, the protections should be designed so that the converter is still able to regulate the output voltage when  $V_{in} = V_{in\min}$  and  $P_{out} = P_{out\max}$  but should trip in case of further input current rise due to either a higher load or a lower input voltage.

As previously mentioned, bottom-limiting the switching frequency is used sometimes as an additional overcurrent countermeasure, thus also  $f_{min}$  should be quite accurately predicted. Therefore, a more accurate model is needed, hopefully as simple as the FHA one.

Reference [36] proposes the usage of the TDA approach to model the two extreme operating conditions: no-load at the maximum input voltage and full load at the minimum input voltage. The former condition is described with the exact model of the cutoff operating mode provided in [14]. As to the latter condition, the model in [36] describes a special case of the DCMB2 mode with a semi-empirical approach based on inspecting the tank current waveform.

On the whole, this approach results in a simple yet accurate design-oriented model that leads to a step-by-step design procedure based on the same specifications given in Table 3, and able to meet the same cornerstones as the FHA approach.

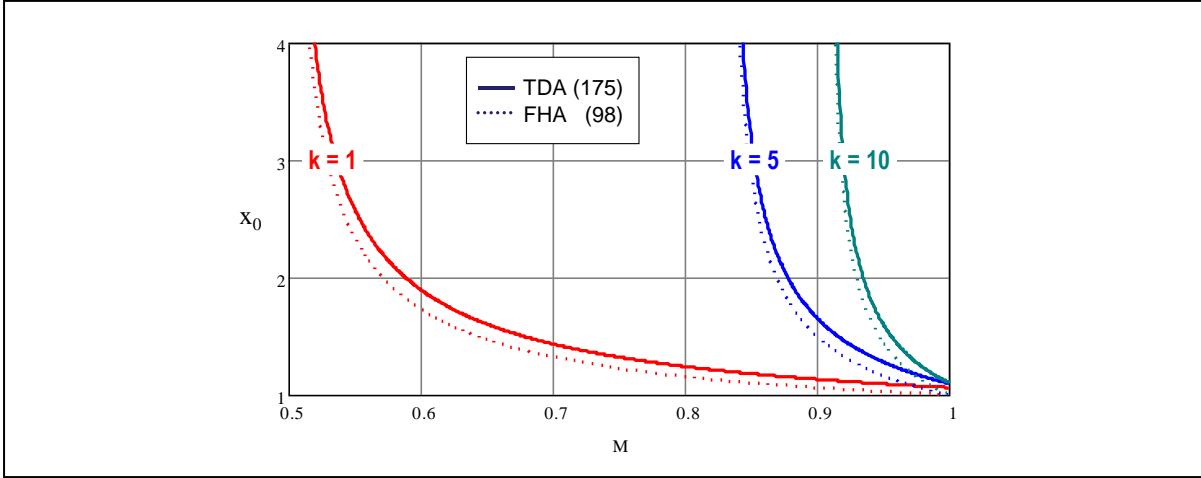
With the FHA approach the cutoff frequency is described by the intersection of the  $|M_0(x, k)|$  curve (96) with the horizontal line  $M$ , resulting in (98). With the TDA approach, [14] provides an expression for the cutoff frequency that with the notation used in this work, can be expressed in normalized form as:

$$x_0 = \frac{\pi}{2} \frac{1}{\sqrt{1+k}} \frac{1}{\cos^{-1}\left(\frac{1}{M} \frac{k}{1+k}\right)} . \quad (175)$$

This equation has the same role as (98) in the FHA approach. To ensure that the converter can regulate the output voltage at no-load and maximum input voltage at the maximum specified switching frequency  $f_{max}(x_{max})$  we need to substitute  $x_0$  with  $x_{max}$  and  $M$  with  $M_{min}$  in (175) and solve the resulting equation for  $k$ . This transcendental equation does not have an analytic solution; however, it is possible to rewrite it in the following form:

$$\frac{1}{M_{min}} \frac{k}{1+k} = \cos\left(\frac{\pi}{2} \frac{1}{\sqrt{1+k}} \frac{1}{x_{max}}\right) . \quad (176)$$

**Figure 92. Comparison of normalized cutoff frequency calculated with TDA and FHA.**



The cosine function can be conveniently expanded in Maclaurin series to the second order because its argument is typically  $< 1$ . The resulting equation can be solved for  $k$  and yields:

$$k = \frac{M_{min}}{1-M_{min}} \frac{x_{max}^2 - \pi^2/8}{x_{max}^2}. \quad (177)$$

This equation has the same role as (153) in the FHA approach. Notice that it has essentially the same form as (153), just with 1 replaced by  $\pi^2/8 \approx 1.234$ . Therefore, with the same  $M_{min}$  and  $x_{max}$ , (177) provides smaller values of  $k$ . This means that the expression (98) based on the FHA approach slightly underestimates the cutoff frequency  $x_0$ , as shown in figure 92.

To assess if ZVS is achieved under no-load conditions we apply (132) and need to know  $I_{R0}$ . Denoting with  $I_{R0\_0}$  the value of  $I_{R0}$  with no-load, [14] (refer to its equations (30) and (32)) teaches us that its value, after adapting the formula to the present notation, is given by:

$$I_{R0\_0} = \frac{a V_{out}}{Z_0} \frac{1}{M_{min} k} \sqrt{\frac{M_{min}^2 (1+k)^2 - k^2}{1+k}}. \quad (178)$$

To determine the model of the special case of DCMB2 mode intended for the operation at full load and minimum input voltage let us refer to the key waveforms illustrated in figure 93.

Considering the half switching cycle where  $V_{HB}$  is positive, i.e., just after the positive-going  $V_{HB}$  transition, the tank current  $I_R(t)$  can be expressed as:

$$I_R(t) = \begin{cases} \frac{I_{R0}}{\sin \theta} \sin(2\pi f_{R1} t - \theta) & 0 \leq t \leq T_H \\ \frac{I_A}{\sin \psi} \sin(2\pi f_{R2} t - \psi) & T_H < t \leq \frac{T_{sw}}{2} \end{cases}, \quad (179)$$

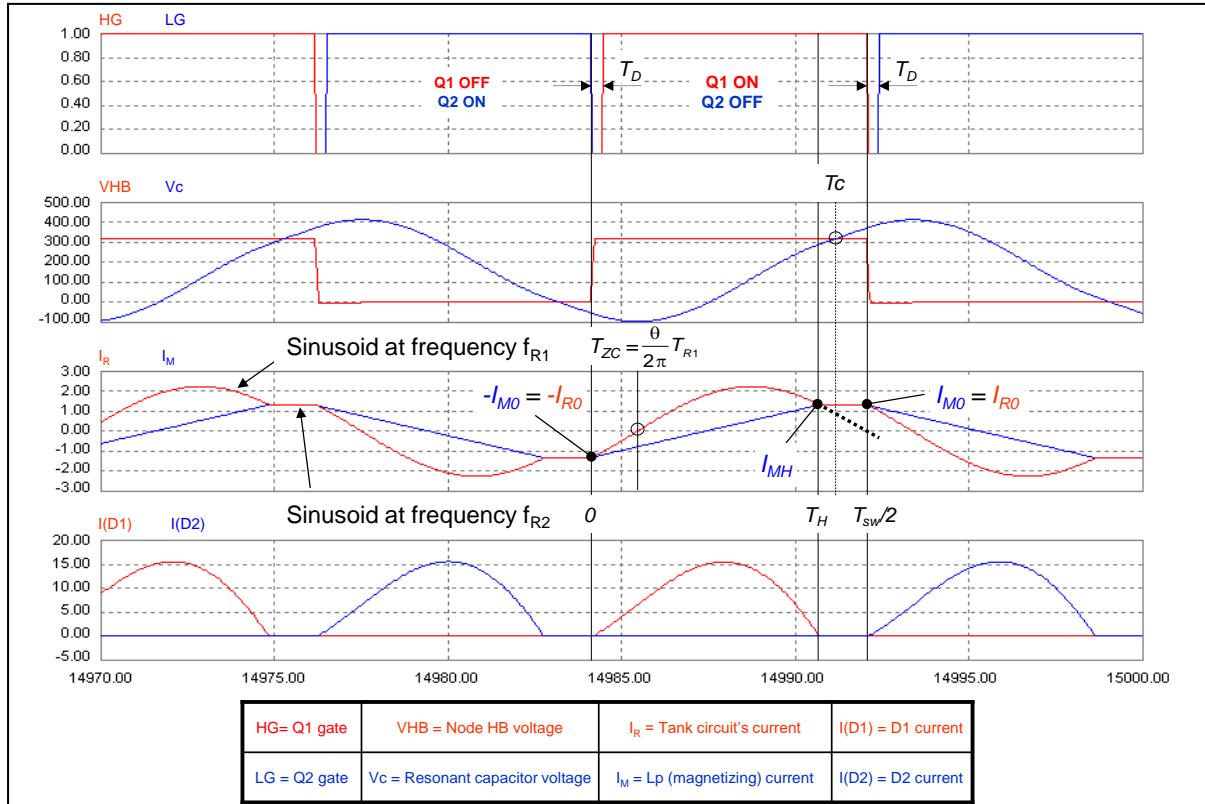
where  $T_H$  is the time instant when  $I_R = I_M$ , i.e., when the secondary current zeroes. The current  $I_M(t)$  through  $L_p$  (we will call it *magnetizing current* for brevity, with the caveat that it is not the true magnetizing current, as discussed speaking of the APR model of the transformer), can be expressed as:

$$I_M(t) = \begin{cases} -I_{M0} + \frac{I_{M0} + I_{MH}}{T_H} t & 0 \leq t \leq T_H \\ I_R(t) & T_H < t \leq \frac{T_{sw}}{2} \end{cases}. \quad (180)$$

In the same half switching cycle the secondary current flowing through the rectifier D1 is:

$$I_{D1}(t) = a[I_R(t) - I_M(t)], \quad (181)$$

**Figure 93. DCMB2 mode operation below resonance: key waveforms.**



which is zero in  $(T_H, T_{sw}/2)$ . Being a DCM operating mode, in the instants of the positive-going  $V_{HB}$  transition the resonant current and the magnetizing current are the same:  $-I_{M0} = -I_{R0}$ .

By symmetry, in the instants of the negative-going  $V_{HB}$  transition it is  $I_{M0} = I_{R0}$ , as pointed out in figure 93.

In general, the equations that describe the below resonance DCMB2 mode operation do not have a closed-form solution. However, we make the following assumptions:

1. The common value  $I_{MH}$  of the resonant current and the magnetizing current in the time instant  $T_H$  ( $I_M(T_H) = I_R(T_H) = I_{MH}$ ) equals the resonant current value in the instant of the negative-going  $V_{HB}$  transition:  $I_{MH} = I_{R0}$ . Then,  $I_{M0} = I_{MH} = I_{R0}$ . Notice that this implies that  $T_H$  is half the upper resonant period, then  $T_H = 1/(2 f_{R1}) = T_{R1}/2$ . Additionally, the average value of the magnetizing current in the interval  $(0, T_H)$  is zero.
2. The instant  $Tc$  where the sinusoid at frequency  $f_{R2}$  in (179) has its peak is the center of the time interval  $(T_H, T_{sw}/2)$ , thus that sinusoid is maximally flat in that interval. Notice that this implies that at  $t = Tc$  the voltage applied to the  $L_s + L_p$  series is zero and, therefore, that the voltage  $V_C$  across the resonant capacitor  $C$  equals the input voltage  $V_{in}$ . Considering the other half-cycle where  $V_{HB}$  is negative, it is  $V_C = 0$  in the half bridge and  $V_C = -V_{in}$  in the full bridge.

These two assumptions, combined with the fact that the duration of the time interval  $(T_H, T_{sw}/2)$  is small compared to  $1/f_{R2}$ , allows us to assume that in  $(T_H, T_{sw}/2)$  the sinusoid at frequency  $f_{R2}$  can be approximated by a horizontal straight line. Therefore, considering that  $T_H = T_{R1}/2$ , (179) can be rewritten as:

$$I_R(t) = \begin{cases} \frac{I_{R0}}{\sin \theta} \sin(2\pi f_{R1} t - \theta) & 0 \leq t \leq \frac{T_{R1}}{2} \\ I_{R0} & \frac{T_{R1}}{2} < t \leq \frac{T_{sw}}{2} \end{cases}, \quad (182)$$

whereas (180) and (181) are still valid. With this approximation it is possible to find the following fundamental relationships that describe the operating point  $V_{in} = V_{in_{min}}$ ,  $P_{out} = P_{out_{max}}$ ,  $f_{sw} = f_{min}$ :

$$f_{min} = \begin{cases} \left(1 - \frac{2a I_{in_{max}} - I_{out_{max}}}{a I_{R0}}\right) f_{R1} & (\text{HB}) \\ \left(1 - \frac{a I_{in_{max}} - I_{out_{max}}}{a I_{R0}}\right) f_{R1} & (\text{FB}) \end{cases}, \quad (183)$$

$$\tan \theta = \begin{cases} \frac{2}{\pi} \left(1 - a \frac{2 I_{in_{max}} - I_{R0}}{I_{out_{max}}}\right) & (\text{HB}) \\ \frac{2}{\pi} \left(1 - a \frac{I_{in_{max}} - I_{R0}}{I_{out_{max}}}\right) & (\text{FB}) \end{cases}, \quad (184)$$

where it is clearly  $I_{out_{max}} = P_{out_{max}} / V_{out}$  and  $I_{in_{max}} = P_{out_{max}} / (\eta V_{in_{min}})$ , with  $\eta$  converter's efficiency in those operating conditions assumed to be known with an educated guess.

As a result of assumption 1, in these equations  $I_{R0}$  is given by:

$$I_{R0} = I_{M0} = \frac{a V_{out} + V_{Rect}}{4 L_p f_{R1}} = \frac{\pi a V_{out} + V_{Rect}}{2 k Z_0}. \quad (185)$$

For model consistency we need to consider the consequence of assumption 2:  $V_C(T_c) = V_{in}$ . It is possible to show that this condition can be expressed as:

$$V_{in_{min}} = \begin{cases} \frac{I_{R0}}{\pi \tan \theta C r f_{R1}} = 2 \frac{I_{R0}}{\tan \theta} Z_0 & (\text{HB}) \\ \frac{I_{R0}}{2 \pi \tan \theta C r f_{R1}} = \frac{I_{R0}}{\tan \theta} Z_0 & (\text{FB}) \end{cases}. \quad (186)$$

If we now substitute the expression (184) of  $\tan \theta$  in (186), solve the resulting equation for  $I_{R0}$ , take (66) into consideration and compare the result to (185) we can find the characteristic impedance  $Z_0$  necessary to achieve the intended operation:

$$Z_0 = \begin{cases} \frac{\pi a^2 (V_{out} + V_{Rect})}{4 a k I_{in_{max}} + \left(\frac{\pi^2}{2} M_{max} - 2k\right) I_{out_{max}}} & (\text{HB}) \\ \frac{\pi a^2 (V_{out} + V_{Rect})}{2 a k I_{in_{max}} + \left(\frac{\pi^2}{2} M_{max} - 2k\right) I_{out_{max}}} & (\text{FB}) \end{cases}. \quad (187)$$

It is also interesting to combine (185) and (186), which leads to a simple expression of  $\tan \theta$ , alternative to (184), valid for both the half bridge and the full bridge:

$$\tan \theta = \frac{\pi}{2k} M_{max}. \quad (188)$$

In chapter 2 the maximum peak amplitude of the voltage  $V_{C1max}$  across the resonant capacitor  $Cr$  was assessed using the FHA approach, which resulted in (91). The model of the special case of DCMB2 mode developed in this chapter can be used to find a more accurate estimate.

It is convenient to start from the values of  $V_C(0) = V_{C0}$  and  $V_C(T_{sw}/2)$  given by (28) and (29) respectively. Of course, the negative peak  $V_{Cmin}$  of the capacitor voltage will be reached when the resonant current crosses zero turning from negative to positive, i.e., with reference to the waveforms in figure 93, at  $t = T_{zc}$ . Similarly, the positive peak  $V_{Cmax}$  will occur when the resonant current crosses zero turning from positive to negative at  $t = T_{sw}/2 + T_{zc}$ . Then, we need to add to  $V_C(0)$  and  $V_C(T_{sw}/2)$  the charge/discharge contributions of the resonant current in the time intervals  $(0, T_{zc})$  and  $(T_{sw}/2, T_{sw}/2 + T_{zc})$ . It is therefore possible to write:

$$V_{Cmin} = V_{C0} + \frac{1}{Cr} \int_0^{T_{zc}} I_R(t) dt, \quad (189)$$

$$V_{Cmax} = V_C(T_{sw}/2) + \frac{1}{Cr} \int_{T_{sw}/2}^{T_{sw}/2 + T_{zc}} I_R(t) dt, \quad (190)$$

with  $I_R(t)$  given by (182). Developing the calculations, we arrive at the following result:

$$V_{Cmin} = \begin{cases} \frac{1}{2} \left[ Vin_{min} - \frac{1}{Cr f_{min}} \left( Iin_{max} + \frac{I_{R0}}{\pi(1+\cos\theta)} \right) \right] & (\text{HB}) \\ -\frac{1}{Cr f_{min}} \left( \frac{Iin_{max}}{4} + \frac{I_{R0}}{\pi(1+\cos\theta)} \right) & (\text{FB}) \end{cases}, \quad (191)$$

$$V_{Cmax} = \begin{cases} \frac{1}{2} \left[ Vin_{min} + \frac{1}{Cr f_{min}} \left( Iin_{max} + \frac{I_{R0}}{\pi(1+\cos\theta)} \right) \right] & (\text{HB}) \\ \frac{1}{Cr f_{min}} \left( \frac{Iin_{max}}{4} + \frac{I_{R0}}{\pi(1+\cos\theta)} \right) & (\text{FB}) \end{cases}, \quad (192)$$

where  $I_{R0}$  is given by (185).

By using (184) or (188) and (185) it is possible to quickly check if ZVS conditions are met or not. The value resulting from (185) is used to check if (132) is fulfilled, and the value of  $\tan \theta$  resulting from (184) or (188) is used to check that the tank current (182) crosses zero after the end of the dead-time  $T_D$ . In fact, the tank current (182) crosses zero at  $t = T_{ZC}$ , where the argument of the sine function zeroes; therefore, the ZVS condition is:

$$T_{ZC} = \frac{\theta}{2\pi f_{R1}} = \frac{1}{2\pi f_{R1}} \tan^{-1} \left( \frac{\pi}{2k} M_{max} \right) > T_D. \quad (193)$$

The proposed step-by-step design procedure resulting from this discussion is the following.

Step 1. Calculate the required value of  $\alpha$  to make the converter operate at resonance at the nominal input voltage and the resulting value of the transformer turns ratio  $a$  with (151).

Step 2. Calculate the values of  $M_{min}$  and  $M_{max}$  with (152), as well as the normalized maximum switching frequency  $x_{max} = f_{max} / f_{R1}$  that will occur at no-load and maximum input voltage.

Step 3. To ensure that the converter can regulate the output voltage at no-load and maximum input voltage, calculate the  $L_p$  to  $L_s$  inductance ratio  $k$  with (177).

Step 4. Calculate the maximum input and output dc currents  $Iin_{max}$ ,  $Iout_{max}$ .

Step 5. Calculate the characteristic impedance  $Z_0$  with (187).

Step 6. Calculate  $I_{R0\_0}$  with (178) and check if the ZVS condition (132) is met under no-load conditions at  $Vin = Vin_{max}$ .

Step 7. Calculate the voltage-current phase-shift  $\theta$  with (188),  $I_{R0}$  with (185) and check if the ZVS condition (132) is met and that (193) is fulfilled too.

If both step 6 and step 7 give a positive result proceed to step 8, otherwise try one or more of the following actions: reduce  $f_{max}$ , increase  $f_{R1}$ , reduce  $a$ , reduce  $C_{HB}$ .

Step 8. Calculate the minimum operating frequency  $f_{min}$  with (183) and all the components of the tank circuit with (157).

Step 9. Considering an integrated magnetics implementation and assuming magnetic circuit symmetry, calculate the parameters of the real transformer with (32).

Step 10. Calculate the peak of the tank current ( $I_{R0} / \sin \theta$ ) to set up the overcurrent means.

Step 11. Calculate the maximum peak voltage across the resonant capacitor  $Cr$  with (192) to define its voltage rating.

### Remarks

1. The approximation offered by this simplified TDA approach is excellent because the discrepancy is very small and concerns only a minor portion of the tank current waveform. Additionally, the variations of the position of  $T_C$  due to the tolerance of the components have little influence on the quality of the approximation. Estimating

converter's efficiency  $\eta$  is likely to be a major source of error. Experience and comparison with similar designs will help make an educated guess as close to reality as possible.

2. As previously stated, the proposed model describes only a special case of the DCMB2 mode occurring below resonance. Designing the resonant tank so that the converter works in this mode at full load and minimum input voltage can be considered a good design choice for at least three reasons:
  - a. It trades off a good utilization of the below-resonance region against a reasonable safety distance from the capacitive mode operation. In many cases, it also accommodates the tolerance of the parameters of both the tank circuit and the control circuit.
  - b. Being the tank and magnetizing currents essentially constant, the flux density in the transformer core does not increase during the interval  $(T_c, T_{sw}/2)$ . In this regard, the transformer can be designed as if operated at the resonance frequency  $f_{R1}$  instead of the actual operating frequency  $f_{min}$ .
  - c. A simple and accurate model is available.

It may be interesting to compare the equivalent value of the quality factor  $Q$  of the tank circuit resulting from this simplified TDA approach with  $Q_B$ , the one that marks the capacitive-inductive transition and resulting from the FHA approach for given values of  $k$  and  $M_{max}$  (100).

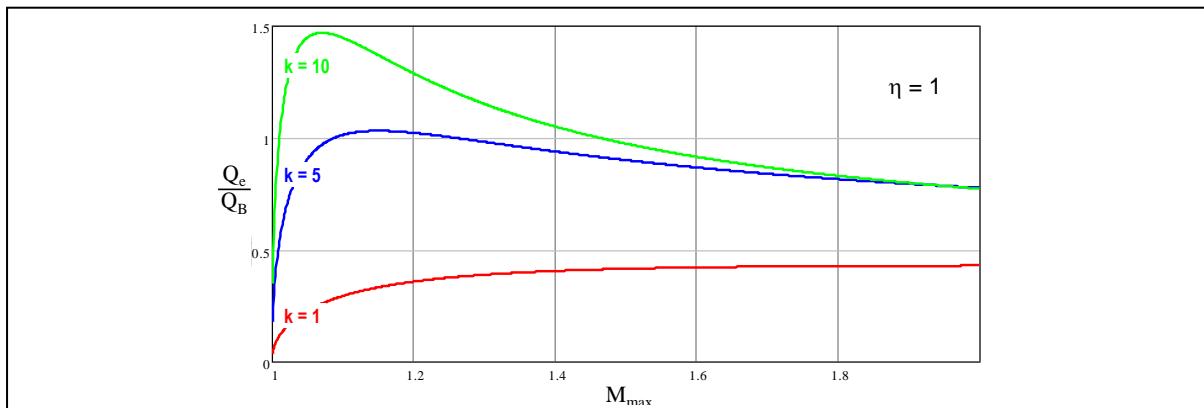
Considering just the half bridge version and recalling that  $Q = Z_0 / R_{eq}$ , the equivalent quality factor is expressed by:

$$Q_e = \frac{\pi^3}{4} \frac{1}{\left(\frac{4k}{\eta} + \pi^2\right) M_{max} - 4k} . \quad (194)$$

Figure 94 shows the plot of  $Q_e / Q_B$  in the interval  $M_{max} \in (1, 2)$  for fixed values of  $k$ . It is worth noticing that  $Q_e$  refers to a design that makes the LLC tank definitely operate in the inductive region, thus it is expected that  $Q_e$  given by (194) be lower than the  $Q_e$  associated to a design that makes the LLC tank operate at the boundary between capacitive and inductive mode.

However, considering the value  $Q_B$  provided by the FHA approach we can see that with low  $k$  values the ratio  $Q_e / Q_B$  is less than 1 as expected, whereas with higher values of  $k$  ( $k > 4.725$  with  $\eta = 1$ , with  $\eta < 1$  this critical value of  $k$  is higher) there is an interval of  $M_{max}$  values where the ratio is greater than 1. This means that in that interval the FHA approach provides a very conservative value and that it would be possible to use  $Q$  values higher than those provided by the FHA procedure.

**Figure 94. Plot of the ratio  $Q_e / Q_B$  as a function of  $M_{max}$  for fixed values of  $k$ .**



Reasonably, this occurs with higher  $k$  values, which extends the below resonance region further from the resonance point, where the FHA model is less and less accurate.

### EXAMPLE

To illustrate the eleven-step design procedure just outlined we will consider a fully developed design example. The same converter specified in Table 4, and whose design based on the FHA model has been carried out in the previous chapter, is taken into consideration. In this way it will be interesting to compare the two designs.

Step 1. Calculate the required value of  $\alpha$  to make the converter operate at resonance at the nominal input voltage and the resulting value of the transformer turns ratio  $a$ :

$$a = \alpha = \frac{1}{2} \frac{V_{in,nom}}{V_{out} + V_{Rect}} = \frac{1}{2} \frac{390}{12 + 0.1} = 16.12 .$$

Step 2. Calculate the values of  $M_{min}$  and  $M_{max}$  as well as the normalized maximum switching frequency that will occur at no-load and maximum input voltage:

$$M_{min} = \frac{V_{in,nom}}{V_{in,max}} = \frac{390}{450} = 0.867 \quad M_{max} = \frac{V_{in,nom}}{V_{in,min}} = \frac{390}{300} = 1.3 .$$

$$x_{max} = f_{max}/f_{R1} = 225/75 = 3.$$

Step 3. Calculate the  $L_p$  to  $L_s$  inductance ratio  $k$  to ensure that the converter can regulate the output voltage at no-load and maximum input voltage:

$$k = \frac{M_{min}}{1 - M_{min}} \frac{x_{max}^2 - \pi^2/8}{x_{max}^2} = \frac{0.867}{1 - 0.867} \frac{3^2 - 1.234}{3^2} = 5.625 .$$

Step 4. Calculate the maximum input and output dc currents  $I_{in,max}$ ,  $I_{out,max}$ .

$$I_{in,max} = \frac{1}{\eta} \frac{P_{out,max}}{V_{in,min}} = \frac{1}{0.95} \frac{240}{300} = 0.842 \text{ A} .$$

$$I_{out,max} = \frac{P_{out,max}}{V_{out}} = \frac{240}{12} = 20 \text{ A} .$$

Step 5. Calculate the characteristic impedance  $Z_0$  of the LLC tank circuit that ensures the desired operation at  $V_{in} = V_{in,min}$ ,  $P_{out} = P_{out,max}$ :

$$Z_0 = \frac{\pi a^2 (V_{out} + V_{Rect})}{4 a k I_{in,max} + \left( \frac{\pi^2}{2} M_{max}^2 - 2k \right) I_{out,max}} = \frac{\pi 16.12^2 (12 + 0.1)}{4 \cdot 16.12 \cdot 5.625 \cdot 0.842 + \left( \frac{\pi^2}{2} 1.3^2 - 2 \cdot 5.625 \right) 20} = 47.32 \Omega .$$

Step 6. Calculate  $I_{R0\_0}$  and check if the ZVS condition is met at no-load with  $V_{in} = V_{in,max}$ :

$$I_{R0\_0} = \frac{a V_{out}}{Z_0} \frac{1}{M_{min} k} \sqrt{\frac{M_{min}^2 (1+k)^2 - k^2}{1+k}} = \frac{16.12 \cdot 12}{47.32} \frac{1}{0.867 \cdot 5.625} \sqrt{\frac{0.867^2 (1+5.625)^2 - 5.625^2}{1+5.625}} = 0.379 \text{ A} .$$

$$|I_{R0\_0}| = 0.379 \text{ A} > \frac{V_{in,max}}{T_D} C_{HB} = \frac{450}{300 \cdot 10^{-9}} 200 \cdot 10^{-12} = 0.3 \text{ A} .$$

Step 7. Calculate  $I_{R0}$  and the voltage-current phase-shift  $\theta$ ; then check if the ZVS condition (193) is fulfilled:

$$I_{R0} = \frac{\pi a V_{out} + V_{Rect}}{2 k Z_0} = \frac{\pi 16.12 \cdot 12 + 0.1}{2 \cdot 5.625 \cdot 47.32} = 1.15 \text{ A} .$$

$$\theta = \tan^{-1} \left( \frac{\pi}{2k} M_{max} \right) = \tan^{-1} \left( \frac{\pi}{2 \cdot 5.625} 1.3 \right) = 0.348 \text{ rad} .$$

$$T_{ZC} = \frac{\theta}{2\pi f_{R1}} = \frac{0.348}{2\pi 75 \cdot 10^3} = 738 \cdot 10^{-9} \text{ s} > T_D = 300 \cdot 10^{-9} \text{ s} .$$

Step 8. Calculate  $x_{min}$ , the minimum operating frequency  $f_{min}$  and all the components of the tank circuit:

$$x_{min} = \left( 1 - \frac{2a I_{in,max} - I_{out,max}}{a I_{R0}} \right) = \left( 1 - \frac{2 \cdot 16.12 \cdot 0.842 - 20}{16.12 \cdot 1.15} \right) = 0.615 ;$$

$$f_{min} = x_{min} f_{R1} = 0.615 \cdot 75 \cdot 10^3 = 46.1 \text{ kHz} ;$$

$$Cr = \frac{1}{2\pi f_{R1} Z_0} = \frac{1}{2\pi 75 \cdot 10^3 \cdot 47.32} = 44.8 \text{ nF} ;$$

$$L_s = \frac{Z_0}{2\pi f_{R1}} \frac{47.32}{2\pi 75 \cdot 10^3} = 100 \mu\text{H} ;$$

$$L_p = k L_s = 5.625 \cdot 100 \cdot 10^{-6} = 563 \mu\text{H} .$$

Step 9. Considering an integrated magnetics implementation and assuming magnetic circuit symmetry, calculate the parameters of the real transformer with (32).

$$n = a \sqrt{1 + \frac{L_s}{L_p}} = 16.12 \sqrt{1 + \frac{1}{5.625}} = 17.49 ;$$

$$L_\mu = \sqrt{L_p L_1} = \sqrt{563(563 + 100)} = 611 \mu\text{H} ;$$

$$L_{L1} = L_1 - L_\mu = 563 + 100 - 611 = 52 \mu\text{H} ;$$

$$L_{L2} = \frac{L_{L1}}{n^2} = \frac{52}{17.49^2} = 0.170 \mu\text{H} .$$

Step 10. Calculate the peak of the tank current to set up the overcurrent means:

$$I_{RpK} = \frac{I_{R0}}{\sin \theta} = \frac{1.15}{\sin 0.348} = 3.372 \text{ A} .$$

It is interesting to notice that this result is almost one fourth larger than that provided by the FHA-based design.

Step 11. Calculate the maximum peak voltage across the resonant capacitor  $Cr$  with (192) to define its voltage rating:

$$V_{Cmax} = \frac{1}{2} \left[ 300 + \frac{1}{44.8 \cdot 10^{-9} \cdot 46.1 \cdot 10^3} \left( 0.842 + \frac{1.15}{\pi (1 + \cos 0.348)} \right) \right] = 399.5 \text{ V} .$$

Notice that with the FHA approach, (91) yields  $V_{C1max} = 331.6 \text{ V}$ , a value 17% lower. This once more confirms the poor accuracy of the FHA approach to describe the below resonance operation and the value of the simplified TDA approach.

There is no need to do the post-design checks:  $a$  is unchanged,  $k$  is nearly the same and  $Cr$  is only 10% lower than the value calculated with the FHA design flow, then  $x_v$ , which depends on the fourth root, will be about 2.5% smaller, still larger than  $x_{max}$ ; the current  $|I_{R0}|$  is larger than the value calculated with the FHA flow and  $L_s$  is larger too, then the critical value for ZVS is smaller.

# Chapter 9

## Power stage design

The previous chapters have addressed the design of the LLC tank, which is among the most delicate parts of the design of an LLC converter. Once this has been completely defined, it is possible to also address the design of all the other parts of the power stage.

To do so, we need to determine the worst-case voltage and current stress for all the involved parts. The scenario under discussion is again that of a typical offline application where the LLC converter is cascaded to a PFC pre-regulator that provides a regulated output voltage that becomes the input voltage for the LLC converter.

Considering the design strategy followed so far, outlined in chapter 7, the LLC converter will be electrically designed to let the maximum current flow and to withstand the maximum voltages, conditions that occur (not all simultaneously) at one the four corners of the specified operating region  $V_{in} \in (V_{in_{min}}, V_{in_{max}})$ ,  $P_{out} \in (P_{out_{min}}, P_{out_{max}})$ . For example, we have seen that the overcurrent/overpower protection circuits must be designed so that they do not step in when  $V_{in} = V_{in_{min}}$  and  $P_{out} = P_{out_{max}}$ , to allow the converter to still regulate the output voltage; however, they will be tripped in case of further input current rise due to either a higher load or a lower input voltage.

The thermal design, instead, will be carried out considering the maximum output power  $P_{out_{max}}$  and the nominal input voltage  $V_{in_{nom}}$ , because the converter will operate around that input voltage nearly all the time. It will occasionally work with input voltages between  $V_{in_{min}}$ , and  $V_{in_{nom}}$  or with a power demand larger than  $P_{out_{max}}$  just for short time intervals that are not thermally significant. A missing cycle that causes an input voltage drop lasts less than 22 ms worst-case with a 50 Hz line, operation under overload or short-circuit conditions may last some hundred ms when the converter is properly equipped with the related protection circuits.

This design approach leads to a higher power-dense converter without sacrificing its reliability.

### *Determination of maximum voltage stress*

The components of the power stage whose maximum voltage stress needs to be determined for their proper selection are the power switches and the resonant capacitor on the primary side and the rectifier block and the output capacitors on the secondary side.

As to the power switches on the primary-side, since the voltage they see during their off state is top- and bottom-clamped by the body diodes of the complementary one, their maximum voltage stress clearly equals the maximum input voltage  $V_{in_{max}}$ . Normally, some extra margin (at least 20-25%) is considered to account for anomalous conditions such as input voltage surges that may occur on the power line and that occasionally take the output voltage of the PFC pre-regulator well above its regulated value.

As to the resonant capacitor, the maximum voltage stress is determined as the step 11 of the design procedure provided in the previous chapter and given by (192). Notice that this applies both to the single-capacitor and the split-capacitors versions: in the latter case, each capacitor shares half the dc input voltage and undergoes half the total resonant current; since each capacitor has half the total value, the amplitude of the resonant voltage is the same too.

As to the voltage applied to the reverse-biased secondary rectifiers, as discussed in Part II Chapter 1, it depends on their configuration.

In case of SE-B configuration, the reverse voltage is simply  $V_{out} + V_{Rect}$ , where  $V_{Rect}$  – it is worth reminding – is the voltage drop across the conducting rectifiers. In case of CT-FW configuration, the reverse voltage is, to a first approximation,  $2 \cdot V_{out} + V_{Rect}$ .

Considering the leakage inductance associated to the secondary windings of the transformer, we need to add the peak value of the related voltage drop  $V_{Lsec} = L_{Lsec} \cdot d i_{sec} / dt$  to  $2V_{out} + V_{Rect}$ .  $L_{Lsec}$  can be estimated as:

$$L_{Lsec} \approx \gamma \frac{L_S}{a^2}, \quad (195)$$

where  $\gamma \in (0, 1)$  is a coefficient that expresses how the total leakage inductance is allotted between primary and secondary side: in case of magnetically symmetric structure, it is  $\gamma = 0.5$ , it is  $\gamma < 0.5$  if the leakage inductance is more located on the primary side,  $\gamma > 0.5$  if the leakage inductance is more located on the secondary side.

An estimate of the maximum  $d i_{sec} / dt$  is found considering (181), (180) and (182) at  $t = 0$ :

$$\left. \frac{di_{sec}}{dt} \right|_{max} \approx 2 \left( \frac{\pi}{\sin \theta} - 2 \right) a f_{R1} I_{R0}, \quad (196)$$

In the end:

$$V_{Lsec} \approx \gamma \frac{1}{a} \left( \frac{1}{\sin \theta} - \frac{2}{\pi} \right) Z_0 I_{R0}, \quad (197)$$

In case of voltage doubler (VD) configuration (refer to fig. 10), the reverse-biased rectifier will see a reverse voltage equal to  $V_{out}/2 + V_{Rect}$ .

The voltage stress on the output capacitor(s) in case of voltage regulation is obviously  $V_{out}$ . In case of a converter with a regulated output current or with the output voltage that can be regulated in a range of values, the maximum output voltage  $V_{out,max}$  will be considered.

Often, in case the control loop that regulates the output voltage/current fails open, an *overvoltage protection* function is in place to stop the converter and prevent the output voltage to drift high uncontrolled. It is a good practice to consider at least the worst-case *overvoltage threshold*, i.e., the maximum output voltage allowed by the overvoltage protection function, as the maximum voltage stress for the output capacitor(s).

All these results are summarized in Table 5.

**Table 5. Maximum voltage stress on power components**

Part	Configuration	Max. voltage stress	Ref.
Primary switches	Half & Full Bridge	$V_{in,max}$	I
Resonant capacitor	Half Bridge (single & split capacitor)	$V_{Cmax} = \frac{1}{2} \left[ V_{in,min} + \frac{1}{Cr f_{min}} \left( I_{in,max} + \frac{I_{R0}}{\pi (1 + \cos \theta)} \right) \right]$	II
	Full Bridge	$V_{Cmax} = \pm \frac{1}{Cr f_{min}} \left( \frac{I_{in,max}}{4} + \frac{I_{R0}}{\pi (1 + \cos \theta)} \right)$	
Secondary rectifiers	CT-FW	$V_{rev} = 2 V_{out} + V_{Rect} + \beta \frac{1}{a} \left( \frac{1}{\sin \theta} - \frac{2}{\pi} \right) Z_0 I_{R0}$	III
	SE-B	$V_{rev} = V_{out} + V_{Rect}$	
	VD	$V_{rev} = V_{out}/2 + V_{Rect}$	
Output capacitor	---	$V_{out}$ ( $V_{out,max}$ )	IV
Note: in these equations $I_{R0}$ is given by (185) and $\theta$ by (188).			

### Determination of current stress for thermal design

Based on the design strategy outlined in chapter 7, the LLC converter operates at resonance when  $V_{in} = V_{in,nom}$ . In view of the thermal design, we need to calculate the power losses in all the power components, and a key element is the calculation of the circulating currents to determine the conduction losses and the switching losses due to voltage-current overlap.

An immediate estimate of the rms value of the tank (primary) current can be carried out using the results of the FHA analysis. Based on (54), and reminding that  $P_{in} = P_{out} / \eta$ , it is possible to find:

$$I_{R1} = \begin{cases} \frac{\pi}{\eta\sqrt{2}} \frac{P_{out,max}}{V_{in,nom}} \frac{1}{\cos \varphi} & (\text{HB}) \\ \frac{\pi}{2\eta\sqrt{2}} \frac{P_{out,max}}{V_{in,nom}} \frac{1}{\cos \varphi} & (\text{FB}) \end{cases}, \quad (198)$$

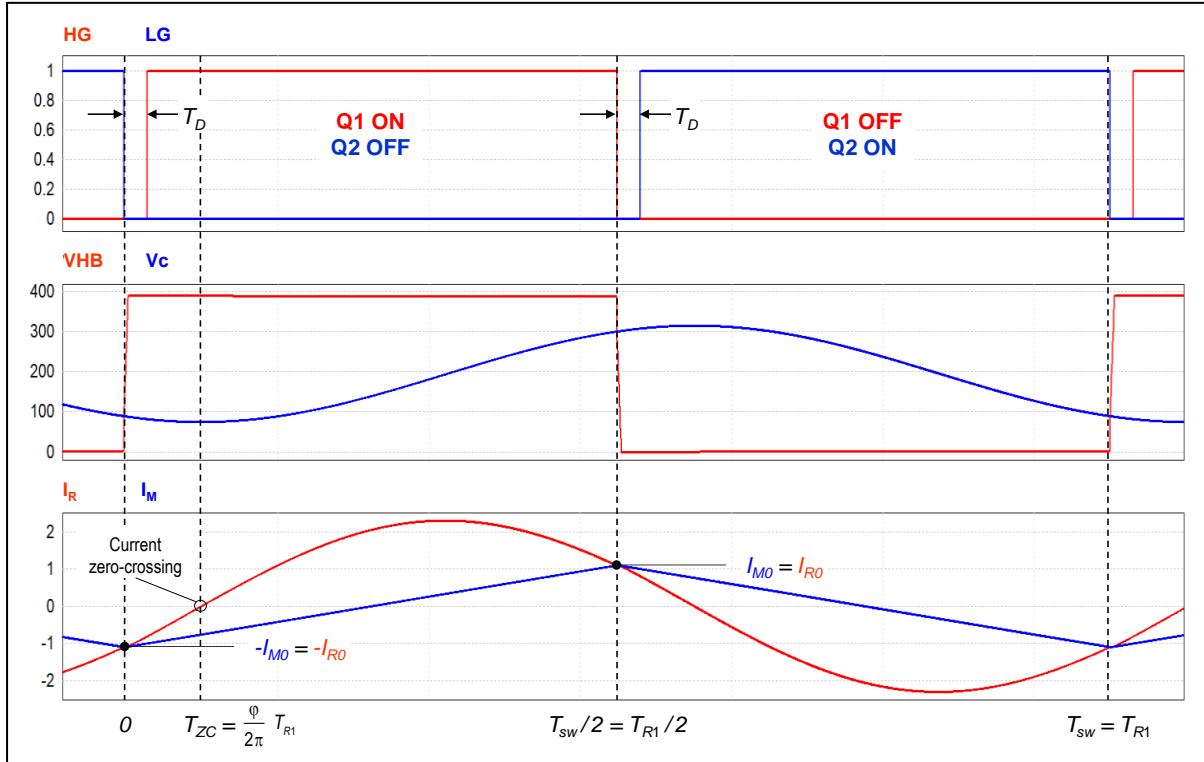
where the lagging phase-shift  $\varphi$  of the tank circuit at resonance is given by (77), here reported for reader's convenience:

$$\varphi = \arg[Z_{in}(1, k, Q)] = \tan^{-1} \frac{1}{kQ}. \quad (77)$$

Though operating at resonance, where the FHA model is maximally accurate, this result is not exact, it is just a good approximation. In fact, in the FHA approach all currents are sinusoidal: while this is true for the overall tank current, the magnetizing current (flowing through  $L_p$ ) is actually triangular. The FHA approach considers only its fundamental component, and this introduces an error.

Fortunately, the TDA approach, which in principle can provide exact results, is straightforward when just considering operation at resonance. This analysis can be carried out with the aid of the timing diagram of figure 95, which shows a zoomed view in a single switching cycle of some of the key waveforms at resonance illustrated in figure 36.

**Figure 95. Key waveforms at resonance.**



The tank current  $I_R(t)$  can be expressed as:

$$I_R(t) = \frac{I_{R0}}{\sin \varphi} \sin(2\pi f_{R1} t - \varphi) , \quad (199)$$

whereas the magnetizing current  $I_M(t)$  is expressed as:

$$I_M(t) = \begin{cases} -I_{M0} + 4 \frac{I_{M0}}{T_{R1}} t & 0 \leq t \leq \frac{T_{R1}}{2} \\ I_{M0} - 4 \frac{I_{M0}}{T_{R1}} \left(t - \frac{T_{R1}}{2}\right) & \frac{T_{R1}}{2} < t \leq T_{R1} \end{cases} . \quad (200)$$

Notice that in the instants  $t = 0$ ,  $t = T_{R1}/2$  and  $t = T_{R1}$ , where the magnetizing current  $I_M(t)$  has its negative and positive peaks  $\mp I_{M0}$ , the resonant current equals the magnetizing current and their common value  $I_{M0} = I_{R0}$  is still given by (185):

$$I_{M0} = I_{R0} = \frac{a}{4} \frac{V_{out} + V_{Rect}}{L_p f_{R1}} = \frac{\pi}{2} \frac{a}{k} \frac{V_{out} + V_{Rect}}{Z_0} . \quad (185)$$

In addition, averaging the resonant current along a switching cycle provides the dc input current  $I_{in} = P_{out,max} / (\eta V_{in,nom})$ :

$$I_{in} = \frac{P_{out,max}}{\eta V_{in,nom}} = \frac{1}{T_{R1}} \int_0^{T_{R1}} \frac{I_{R0}}{\sin \varphi} \sin(2\pi f_{R1} t - \varphi) dt = \begin{cases} \frac{I_{R0}}{\pi \tan \varphi} & \text{HB} \\ \frac{2I_{R0}}{\pi \tan \varphi} & \text{FB} \end{cases} . \quad (201)$$

It is just worth reminding that in the half-bridge configuration  $I_R(t)$  is expressed by (199) only in  $(0, T_{R1}/2)$ , and it is zero in  $(T_{R1}/2, T_{R1})$ . Solving (201) for  $\varphi$  completely defines (199):

$$\varphi = \begin{cases} \tan^{-1} \left( \frac{I_{R0} \eta V_{in,nom}}{\pi P_{out,max}} \right) & \text{HB} \\ \tan^{-1} \left( \frac{2 I_{R0} \eta V_{in,nom}}{\pi P_{out,max}} \right) & \text{FB} \end{cases} . \quad (202)$$

Clearly, the peak and the rms values of the tank current  $I_R(t)$  at resonance are:

$$I_{Rpk} = \frac{I_{R0}}{\sin \varphi}; \quad I_{Rrms} = \frac{I_{R0}}{\sqrt{2} \sin \varphi} . \quad (203)$$

By comparing (202) to (77), even with  $\eta = 1$  the FHA approximation slightly underestimates  $\varphi$  and, as a result, underestimates the peak and rms values of  $I_R(t)$ . It is worth noticing that (77) would provide the same numerical result as (202) if we eliminated the factor  $\pi^2/8$  from Q. Incidentally this very same factor links the peak amplitude of a triangular waveform like that expressed by (200) and the amplitude of its fundamental harmonic, which is consistent with the fact that the FHA approach considers only the first harmonic of that triangular waveform.

Considering the current flowing through the primary power switches, its peak value is the same as that of the tank current but its rms value is  $1/\sqrt{2}$  because it just flows half the time:

$$I_{SWpk} = I_{Rpk}; \quad I_{SWrms} = \frac{1}{\sqrt{2}} I_{Rrms} . \quad (204)$$

A final notice concerning the currents on the primary side: the current  $I_{R0}$  provided by (185) is the switched current, corresponding to the transitions of the half-bridge leg(s) and therefore it determines, along with the switching frequency, the switching losses due to voltage-current overlap.

The current flowing on the secondary side is given by

$$I_{sec}(t) = a[I_R(t) - I_M(t)] . \quad (205)$$

As to its average value in a switching cycle, which is given by:

$$I_{sec\_dc} = \frac{2}{T_{R1}} \int_0^{T_{R1}} \left[ \frac{I_{R0}}{\sin \varphi} \sin(2\pi f_{R1} t - \varphi) - \left( -I_{R0} + 4 \frac{I_{R0}}{T_{R1}} t \right) \right] dt , \quad (206)$$

it equals the dc output current  $I_{out,max} = P_{out,max}/V_{out}$ . However, the value of  $\varphi$  in (206) is affected by the overall efficiency  $\eta$  that accounts for all power losses in the converter, whereas in this case only the output losses should be considered. These losses are somehow included in  $I_{R0}$  because its value considers the drop  $V_{Rect}$  across the secondary rectifiers.

It is therefore suggested to solve (206) for  $\varphi$ , rename this new phase-shift angle with  $\psi$  and use this value for the following calculations of the other significant quantities. The result is:

$$\psi = 2 \tan^{-1} \left[ \sqrt{\left( \frac{\pi I_{out,max}}{2 a I_{R0}} \right)^2 + 1} - \frac{\pi I_{out,max}}{2 a I_{R0}} \right]. \quad (207)$$

The rms value of  $I_{sec}(t)$  can be found from:

$$I_{sec\_rms} = a \sqrt{\frac{2}{T_{R1}}} \int_0^{T_{R1}/2} [I_R(t) - I_M(t)]^2 dt . \quad (208)$$

Developing the calculations, we finally find:

$$I_{sec\_rms} = a I_{R0} \sqrt{2 \left( \frac{1}{4 \sin^2 \psi} + \frac{1}{6} - \frac{4}{\pi^2} \right)} , \quad (209)$$

with  $I_{R0}$  given by (185) and  $\psi$  by (207). This value can be approximated very well by:

$$I_{sec\_rms} \approx \frac{\pi}{2\sqrt{2}} I_{out,max} , \quad (210)$$

which is the value listed in Table 1 that neglects the negative contribution of  $I_M(t)$  and assumes that the secondary current is perfectly sinusoidal, thus it slightly underestimates  $I_{sec\_rms}$ .

Based on (210), which for all practical purposes is accurate enough, the peak and the ac values, useful for the selection of the output capacitors, can be determined as:

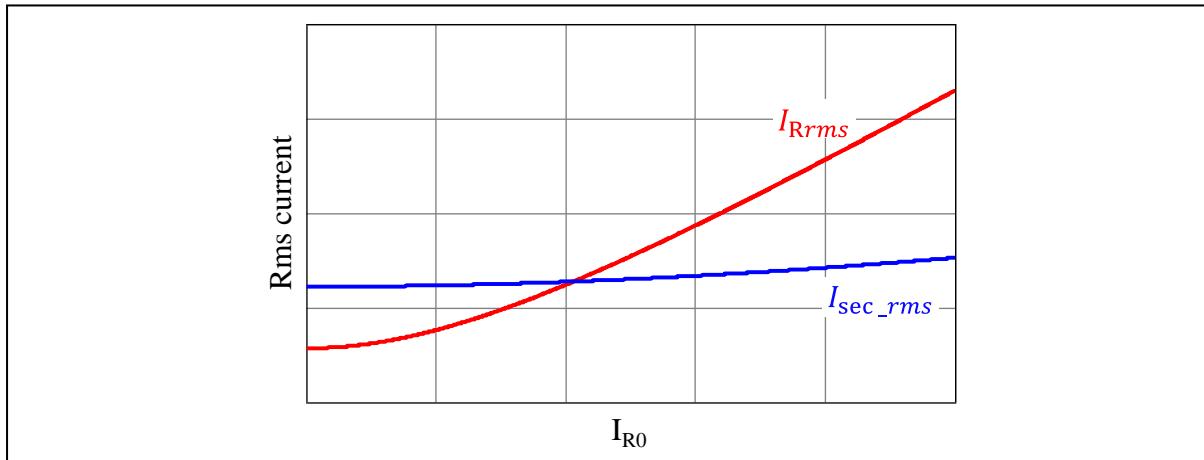
$$I_{sec\_pk} = \frac{\pi}{2} I_{out,max} ; \quad (211)$$

$$I_{sec\_ac} = \sqrt{I_{sec\_rms}^2 - I_{out,max}^2} = \sqrt{\frac{\pi^2}{8} - 1} I_{out,max} . \quad (212)$$

Each secondary rectifier will carry half the dc current  $I_{out,max}$  and  $1/\sqrt{2}$  the total  $I_{sec\_rms}$ . All these results are summarized in Table 6.

Notice that both the primary and secondary rms currents depend on  $I_{R0}$ , the secondary current only slightly, the primary current more pronouncedly, as shown in the plots of figure 96.

**Figure 96. Plot illustrating how the primary and secondary rms currents depend on  $I_{R0}$ .**



**Table 6. Maximum current stress on power components**

Part	Configuration	Max. current stress		Ref.
Switched current	Half and Full Bridge	$I_{R0} = \frac{a V_{out} + V_{Rect}}{4 Lp f_{R1}}$		I
	Half Bridge	$I_{SWrms} = \frac{I_{R0}}{2 \sin \varphi}$		II
Primary switches	Full Bridge	$I_{SWrms} = \frac{I_{R0}}{2\sqrt{2} \sin \varphi}$		
Primary winding	Half and Full Bridge	$I_{Rrms} = \frac{I_{R0}}{\sqrt{2} \sin \varphi}$		III
Resonant capacitor	Half Bridge Single capacitor	$I_{Rrms} = \frac{I_{R0}}{\sqrt{2} \sin \varphi}$		
	Half Bridge Split capacitors	$\frac{I_{Rrms}}{2} = \frac{I_{R0}}{2\sqrt{2} \sin \varphi}$		IV
	Full Bridge	$I_{Rrms} = \frac{I_{R0}}{\sqrt{2} \sin \varphi}$		
Dc output current	Half and Full Bridge	$I_{outmax}$		V
Peak output current	Half and Full Bridge	$I_{sec\_pk} = \frac{\pi}{2} I_{outmax}$		VI
Secondary winding(s)	CT-FW	$I_{sec1,2\_dc} = I_{outmax}/2$	$I_{sec1,2\_rms1} = \frac{\pi\sqrt{2}}{8} I_{outmax}$	
	SE-B and VD	$I_{sec\_dc} = I_{outmax}$	$I_{sec\_rms1} = \frac{\sqrt{2}}{3} I_{outmax}$ (*)	VII
Secondary (output) rectifiers	CT-FW	$I_{D1,D2\_dc} = I_{outmax}/2$	$I_{D1,D2\_rms} = \frac{\pi}{4} I_{outmax}$	
	SE-B	$I_{D1-D4\_dc} = I_{outmax}/2$	$I_{D1-D4\_rms} = \frac{\pi}{4} I_{outmax}$	VIII
	VD	$I_{D1,D2\_dc} = I_{outmax}$	$I_{D1,D2\_rms} = \frac{\pi}{2\sqrt{2}} I_{outmax}$	
Output capacitor(s)	---		$I_{sec\_ac} = \sqrt{\frac{\pi^2}{8} - 1} I_{outmax}$	IX
Note: in these equations $\varphi$ is given by (202). (*) Fundamental frequency = $2 f_{R1}$ .				

As it is possible to deduce from (185), increasing  $Lp$  reduces  $I_{R0}$ , the rms currents and the conduction losses but this tends to require a larger core for the resonant transformer. Decreasing  $Lp$  increases  $I_{R0}$ , the rms currents and the conduction losses but allows the use of a smaller core. There is clearly a tradeoff between these two design objectives.

The same considerations apply to the switching losses at turn-off which are essentially directly proportional to  $I_{R0}$  and then, inversely to  $Lp$ .

#### *Integrated transformer design guidelines*

Transformer design is an iterative process based on a trial-and-error approach. A wisely chosen starting point may reduce considerably the number of iterations needed.

The first step is the selection of the magnetic core material and geometry. As to the magnetic material, Ni-Zn soft ferrites for power applications such as 3C94, 3C95, 3F3 or 3F4

are a good choice because they have low core losses, especially in designs where the switching frequency is pushed to higher values to increase power density.

The geometry, a gapped core-set with slotted bobbin, can be a popular E or E-derived type like in the examples shown in Part II, chapter 6. Other configurations, such as RM or PQ cores, are quite popular because they are inherently high leakage geometries, since they result in narrower and thicker windings. Planar transformers are gaining momentum due to their offering good thermal performance, compact design, high repeatability, ability to implement a large variety of winding patterns, that enable low profile and flat designs.

Among the various shapes and styles offered by manufacturers the most suitable one will be selected with technical and economic considerations.

The next step is to choose core size. Ideally, the transformer's core must be able to handle the power throughput  $P_{inT}$  providing the required  $L_s$  and  $L_p$  with acceptable power losses and with the minimum size. A most common way of describing core size is the so-called Area Product ( $AP$ ), which is the product of the effective cross-sectional area of the core ( $A_e$ ) times the window area available to accommodate the windings ( $A_w$ ). It is possible to define the minimum  $AP$  required by a specific application and the chosen core should have an  $AP$  value larger than the minimum required.

Assuming that the transformer physical model shown in figure 33 has been completely defined starting from those of the APR model, an important property of the gapped core plus slotted bobbin assembly should be recalled.

The reluctance of the leakage flux path is constant for a given core geometry and is independent of the gap thickness  $I_G$ : essentially, it is a function of the physical dimensions of the core and the distance between the windings. This implies that the leakage inductance of the primary winding,  $L_{L1}$ , depends only on the turn number of primary turns  $N_1$  and will not change if  $I_G$  is adjusted. The total primary inductance  $L_1 = L_{L1} + L_\mu$  is strongly affected by the gap thickness, but it is only the magnetizing inductance  $L_\mu$  that changes. Therefore, once the ferrite core and the associated bobbin are defined, it is possible to control  $L_{L1}$  and  $L_\mu$  separately, acting on  $N_1$  and  $I_G$  respectively.

The specific leakage inductance factor  $A_{Llk}$  of the selected core plus slotted bobbin assembly should be known by characterization, and at that point the number of primary turns  $N_1$  can be calculated from  $L_1 = N_1^2 \cdot A_{Llk}$ :

$$N_1 = \sqrt{\frac{L_1}{A_{Llk}}} , \quad (213)$$

Again,  $A_{Llk}$  is a function of bobbin's geometry, independent of the air gap thickness.

The number of secondary turns  $N_2$  can be obtained by dividing  $N_1$  by the actual turn ratio  $n$  given by (32). Further adjustments might be needed to make the ratio  $N_1 / N_2$  of two integer numbers as close as sensibly possible to the target  $n$ . It is worth reminding that a value of  $n$  different from the target will shift the input voltage where the LLC converter operates at resonance.

Unlike transformers for other topologies such as the forward converter, the flux density swing in an LLC transformer depends on the volt-seconds on the secondary windings. In general, the relationship that links the peak flux density  $B_{pk}$  to the primary turn number  $N_1$  is:

$$B_{pk} = \frac{a}{4} \frac{V_{out} + V_{Rect}}{N_1 A_e f_{R1}} , \quad (214)$$

where  $A_e$  is the effective cross section of the ferrite core (expressed in  $m^2$ ).

Notice once more that if the LLC tank has been designed with the approach proposed in chapter 7, when the converter works below resonance, in the time interval when no current flows on the secondary side the magnetizing current is essentially constant and the flux density in the transformer core does not increase. Even if the transformer works at a frequency lower than  $f_{R1}$ , (214) still applies as if the converter was operated at the resonance frequency  $f_{R1}$ .

$B_{pk}$  in (214) should not exceed 0.3-0.4 T (depending on the ferrite grade) to prevent the core from saturating but might be even significantly lower to achieve acceptable core losses.

In fact, core losses are proportional to the quantity  $f_{sw}^{\rho} B_{pk}^{\sigma}$  (where  $\sigma$  is a number normally included between 2 and 3): too large a  $B_{pk}$  value would cause excessive core losses, especially with a high operating frequency  $f_{sw}$ .

A further design constraint is that the temperature rise caused by the total losses should not exceed the maximum allowed by the specification. This not only poses limits on core losses, as previously mentioned, but also on the so-called *copper losses*, that is the conduction losses in the windings.

This is a quite delicate design phase because of the high frequency effects that cause eddy currents to flow in winding conductors: *skin effect* and *proximity effect*. These eddy currents add to the winding current flowing in the conductor, causing additional power losses.

Skin effect causes current in an isolated conductor to flow only in a small portion of its entire cross section, as if it was concentrated in an annulus tangent to its surface. The width of this annulus is called *skin depth* or *penetration depth*, is denoted with  $\delta$  and varies with the inverse square root of frequency. At 100 kHz frequency, the skin depth in copper almost equals the diameter  $d$  of a thin AWG 30 wire (0.255 mm diameter). For a full utilization of the wire cross section, one should use conductors such that  $d/\delta$  is not too larger than 1.

Proximity effect is caused by the ac component of the magnetic field around a conductor carrying high-frequency current that induces eddy currents in adjacent conductors. In inductors and transformers this effect makes copper losses increase very quickly with the  $d/\delta$  ratio and with the number  $m$  of layers in a winding and is usually dominant over skin effect.

The combination of these two effects can be schematized by introducing the *ac resistance* of the wire,  $R_{ac}$ , defined as:

$$R_{ac} = F_H F_R R_{dc}, \quad (215)$$

where the *harmonic loss factor*  $F_H$  and the *resistance factor*  $F_R$  are quantities greater than unity, and  $R_{dc}$  is the dc resistance of the winding (the one exhibited with a dc winding current  $I_{dc}$  and that can be measured with an ohmmeter).

$F_R$  depends on the  $d/\delta$  ratio and the number of layers in a winding and presumes a sinusoidal current as shown in the plots of figure 97 (Dowell's curves).

$F_H$  depends on the winding geometry, the harmonic content of the winding current waveform and on the  $d/\delta_1$  ratio, where  $\delta_1$  is the skin depth at the fundamental harmonic, i.e., the frequency of the winding current waveform. The plots of  $F_H$  for a full-wave rectified sinusoid and for a half-wave rectified sinusoid are shown in figure 98.

In the end, the conduction losses in a winding can be expressed as:

$$P_{Cu} = I_{dc}^2 R_{dc} + I_{rms1}^2 R_{ac}, \quad (216)$$

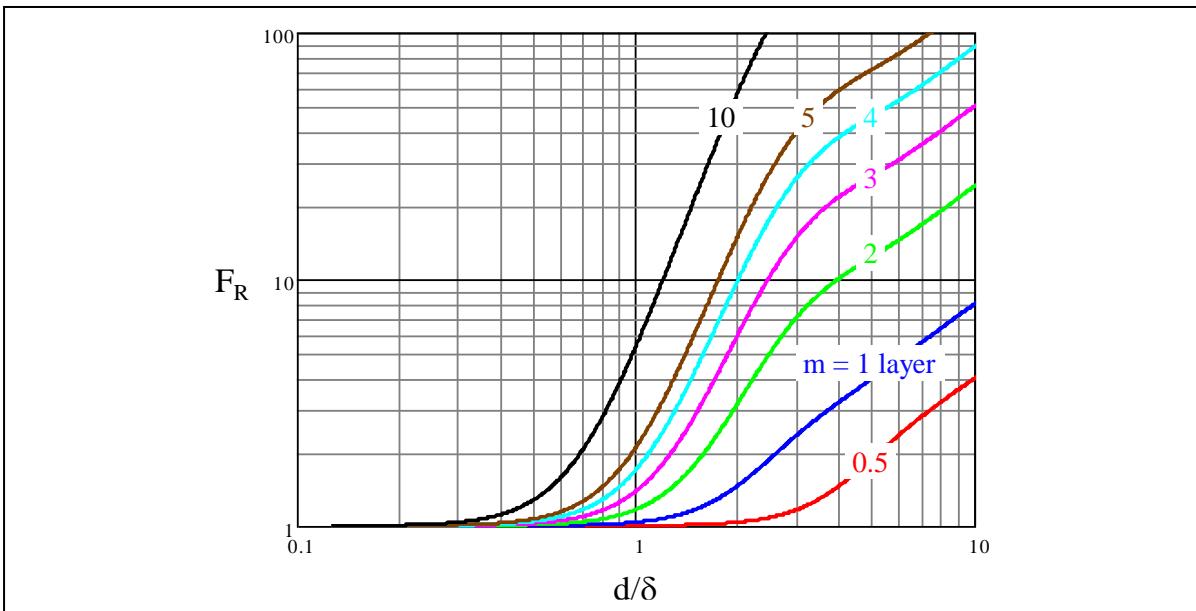
where  $I_{rms1}$  is the rms amplitude of the first harmonic of the winding current waveform.

In a resonant transformer operated at resonance the primary (tank) current is sinusoidal, hence  $F_H = 1$  in (215), while in (216)  $I_{dc}$  is zero and  $I_{rms1}$  equals the  $I_{rms}$  value given by equation III in Table 6. To calculate the secondary conduction losses the  $I_{rms1}$  value in (216) is given by equations VII in Table 6. Of course, in case of CT-FW configuration, the losses in a single winding will be doubled to obtain the total secondary losses.

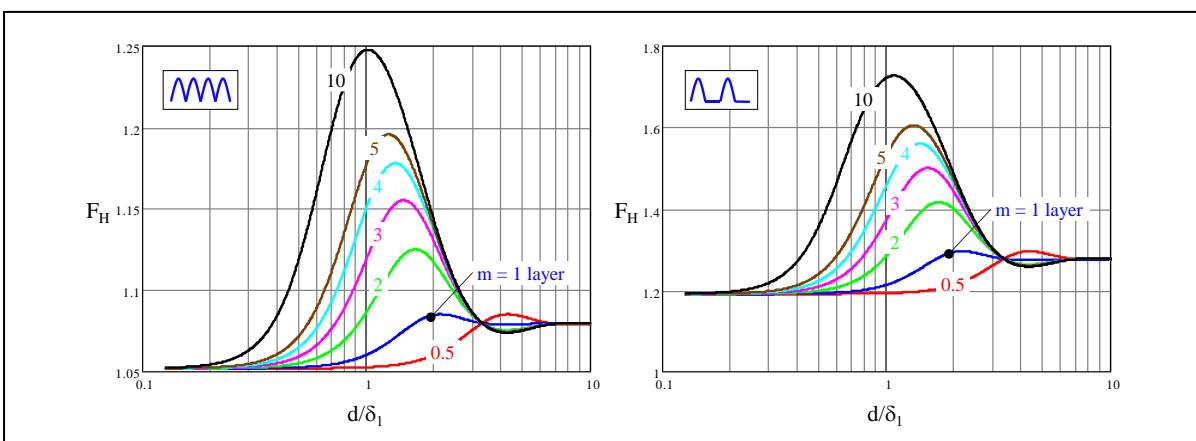
It is apparent that one of the design objectives in a resonant transformer design is to achieve an ac resistance not too larger than the dc resistance while not increasing  $R_{dc}$  significantly.

To this aim, it is recommended the use of litz or multi-strand wires for both the primary and the secondary winding. Strands should be twisted or transposed, so that each strand passes through each possible position in the bundle they form, to prevent high frequency currents from circulating between strands. Litz or multi-strand wires need to be used wisely because they themselves are composed by multiple layers and  $R_{ac}$  quickly increases with the number of layers.

**Figure 97. Dowell's curves:  $R_{ac}/R_{dc}$  ratio ( $F_R$ ) in a two-winding transformer with sinusoidal winding current.**



**Figure 98.  $F_H$  plots:  $R_{ac}$  rise induced by waveform harmonics. Rectified sinusoid (left); half-wave rectified sinusoid (right).**



Since the primary and the secondary currents are substantially in phase, interleaving the windings can significantly lower  $R_{ac}$  and reduce proximity losses. Also, core geometries that can accommodate more turns in a single layer can result in a lower number of layers with a consequent reduction of proximity effect and  $R_{ac}$ .

A good target is to achieve  $R_{ac} / R_{dc} = F_H F_R = 1.5$ , thus the designer can choose the equivalent single-strand wire gauge based on the budgeted copper losses for that winding and then select the strand configuration (strand diameter and number of paralleled strands) that provides an  $R_{ac} / R_{dc}$  ratio close to the target. For example, if the budgeted primary side copper loss is 0.6 W, and it is  $I_{Rms} = 2$  A, the primary wire gauge will be such that the  $R_{dc}$  resistance of the winding will be  $0.6/2^2/1.5 = 0.1 \Omega$ .

Comparing the CT-FW and the SE-B configurations of the secondary rectifiers, notice that with CT-FW the rms value of the current flowing into each secondary winding is  $1/\sqrt{2}$  times the current flowing through the single-ended secondary winding with the SE-B configuration. Therefore, the wire gauge of each winding can be cut in half (the number of secondary turns  $N_2$  is obviously the same). Also notice that in SE-B configuration the fundamental frequency of the winding current where  $d/\delta_1$  is to be computed is twice the switching frequency ( $2 f_{R1}$ ).

There is another important aspect to consider in case of CT-FW configuration: the two windings must be tightly coupled to each other, so that the leakage inductance, measured on the primary side with only one secondary winding short circuited, is the same whichever winding is shorted. In case the two leakage inductances are substantially different, the tank circuit will exhibit two different resonance frequencies during each half cycle, which causes the resonant current to be asymmetric and, consequently, makes the two secondary currents different. This will cause a larger output voltage ripple and, above all else, a different thermal stress of the secondary rectifiers that might jeopardize their reliability.

To achieve good coupling between the two secondary windings, a good practice is to wind them in parallel (bifilar winding).

#### *Resonant capacitor selection*

The resonant capacitor needs to be selected considering its ac current rating. Since it carries the entire tank current, its rating must be larger than the rms value of the tank current given by equations IV in Table 6. In fact, exceeding the rating will cause the capacitor to overheat due to the excessive power dissipation on its ESR, which shortens its lifetime.

Sometimes manufacturers provide the ac current rating specifications indirectly, e.g., by specifying the maximum applicable ac voltage as a function of frequency. Again, the point is the maximum allowed current that provides an internal temperature rise not significantly affecting reliability.

Sometimes it is more practical to parallel two or more capacitors to meet the ac current rating requirement rather than looking for a single capacitor with that rating. If one did not take it into account already, this might suggest the use of the split capacitor configuration.

As to the voltage rating, (the other strong accelerator of failure mechanisms), it must be larger with some safety margin (20-25% is adequate) than the maximum peak voltage that can be found across its terminals. This voltage can be found with equations II in table 5.

As to the selection of capacitor technology, the prime guidelines come from the need of having a low ESR or, as sometimes specified, a low dissipation factor (DF) to keep power losses low, and of being able to withstand bipolar voltages (this is especially true for the full bridge configuration).

Electrolytic capacitors are polarized, so they can withstand only positive voltages; multilayer X7R ceramic types usually are not low-ESR devices, have a capacitance value that drifts with the applied voltage and with temperature and therefore are not recommended; C0G capacitors do have a low ESR and are exceptionally stable in temperature and voltage but their ac current rating is seldom specified and they are not always available with the desired voltage rating and capacitance value combination; sometimes their cost can be a concern.

Therefore, the most common selection power designers do is to use metalized polypropylene film capacitors. These devices have all the characteristics needed for being successfully used in LLC converters: low ESR, stable characteristics, ac current rating is characterized, large availability of capacitance value and voltage rating combinations.

### Primary switches selection

Having already selected the topology (half bridge or full bridge) during the design of the LLC tank, and then decided their number, the selection of the primary switches is done essentially based on the maximum voltage they need to withstand (specified by equation I in Table 5) and with the objective of minimizing their total power losses, sometimes trading this off with cost considerations.

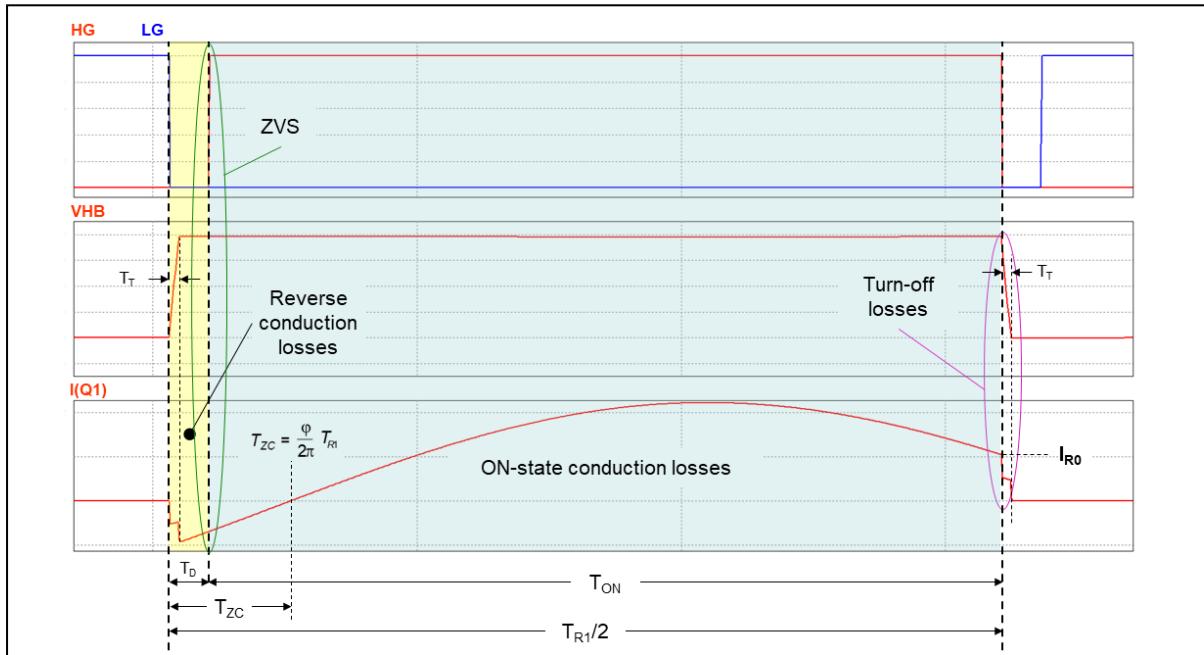
There are essentially three sources of power loss, as illustrated in figure 99.

- *Reverse conduction losses.* During  $T_T$  the drain voltage falls discharging the  $C_{HB}$  capacitance (charging the  $C_{oss}$  capacitance of Q1); at  $t = T_T$  current starts flowing in the power switch injecting the body diode (in case the power switch is a MOSFET) or making the switch reverse conduct (in case the power switch is a GaN HEMT) along the entire dead-time  $T_D$ .

In that short interval the switch current, given by (199), can be approximated by a straight line (corresponding to the first term of the Maclaurin series expansion) and its average value expressed as:

$$I_{RTD} = I_{R0} \left( \pi \frac{T_D + T_T}{\tan \varphi} f_{R1} - 1 \right). \quad (217)$$

**Figure 99. Details of losses in primary switch Q1.**



The source-to-drain voltage  $V_{DS}$  while the power switch is reverse conducting can be approximated with:

$$V_{DS} = \begin{cases} -V_F & (\text{MOSFET}) \\ -(V_{GS(th)} - V_{GSo\text{ff}}) + I_{RTD} R_{DS(on-rev)} & (\text{HEMT}) \end{cases}. \quad (218)$$

In this expression,  $V_{GS(th)}$  is the on-threshold of the device,  $V_{GSo\text{ff}}$  is the voltage used to keep the device off (typically,  $V_{GSo\text{ff}} = 0$ ) and  $R_{DS(on-rev)}$ , the on resistance while the device operates in reverse conduction mode. Normally,  $R_{DS(on-rev)} \approx R_{DS(on)}$ .

All these approximations are acceptable since these losses normally represent a minor portion of the total losses. In the end, reverse conduction losses can be expressed as:

$$P_{\text{revcon}} = I_{RTD} V_{DS}(T_D - T_T) f_{R1}. \quad (219)$$

- *Conduction losses.* Conduction losses  $P_{\text{cond}}$  depend essentially on its  $R_{DS(on)}$ :

$$P_{\text{cond}} = R_{DS(on)} I_{SWrms}^2, \quad (220)$$

with  $I_{SWrms}$  given by equations II in Table 6.

$R_{DS(on)}$  has a strong dependence on the operating temperature. Normally MOSFET datasheets specify the  $R_{DS(on)}$  @  $T_j = 25^\circ\text{C}$  and @  $T_j = T_{j\max}$  (typically, 125 or 150 °C) and show some typical curves  $R_{DS(on)}$  vs.  $T_j$ . Based on the specified data, the  $R_{DS(on)}$  at other temperatures can be estimated with:

$$R_{DS(on)}(T_j) = R_{DS(on)}(25^\circ\text{C}) e^{h(T_j-25)}, \quad (221)$$

Where  $h$  is given by:

$$h = \frac{1}{T_{j\max}-25} \ln \left( \frac{R_{DS(on)}(T_{j\max})}{R_{DS(on)}(25^\circ\text{C})} \right), \quad (222)$$

These formulas fit equally well both MOSFETs and GaN HEMTs.

- *Turn-off losses.* The turn-off losses are given by the product of the energy dissipated by voltage-current overlap as either switch is turned off, times the switching frequency. The energy due to the voltage-current overlap depends on the fall time of the drain current at turn-off, the total capacitance node  $C_{HB}$  and on the way it modulates with the  $V_{HB}$  voltage.

The nonlinearity of  $C_{oss}$  (refer to Figure 21) makes  $V_{HB}$  increase slowly at its low and high values, and much faster when it is halfway in its swing. This reduces the voltage-current overlap and, consequently, the associated power loss with respect to a linear capacitor. However, the mathematical expression of the loss is overly complex, so it is possible to provide a rough estimate using the time-equivalent linear capacitance  $C_{eT}$  to build the overall  $C_{HB}$ .

Considering the turn-off transient of the low-side switch Q2 and under the assumption that the switch current fall time  $T_f$  is shorter than the transition time  $T_T$  of the HB node, it is possible to write:

$$I_{C_{HB}}(t) = C_{HB} \frac{dV_{HB}}{dt} \rightarrow V_{HB}(t) = \frac{1}{C_{HB}} \int_0^t I_{C_{HB}}(t) dt = \frac{1}{C_{HB}} \int_0^t I_{R0} - I(Q2, t) dt, \quad (223)$$

where  $I_{R0}$  is given by equation I in Table 6. Power losses due to voltage-current overlap occur only during the time interval  $(0, T_f)$  where  $I(Q2, t)$  is non-zero. Assuming that  $I(Q2, t)$  at turn-off falls to zero linearly:

$$I(Q2, t) = I_{R0} - \frac{I_{R0}}{T_f} t, \quad (224)$$

$V_{HB}(t)$  expressed by (223) in the interval  $(0, T_f)$  is:

$$V_{HB}(t) = \frac{1}{C_{HB}} \int_0^t \frac{I_{R0}}{T_f} t dt = \frac{I_{R0}}{2 C_{HB} T_f} t^2, \quad (225)$$

Note that with this assumption in the remainder interval ( $T_f$ ,  $T_f$ ) the voltage  $V_{HB}$  will ramp up linearly because charged by the constant current  $I_{R0}$ .

The energy lost because of voltage-current overlap will be calculated by integration of the product of (224) and (225):

$$E_{off} = \int_0^{T_f} V_{HB}(t) I(Q2, t) dt = \frac{I_{R0}^2}{2 C_{HB} T_f} \int_0^{T_f} t^2 \left(1 - \frac{t}{T_f}\right) dt = \frac{(I_{R0} T_f)^2}{24 C_{HB}}, \quad (226)$$

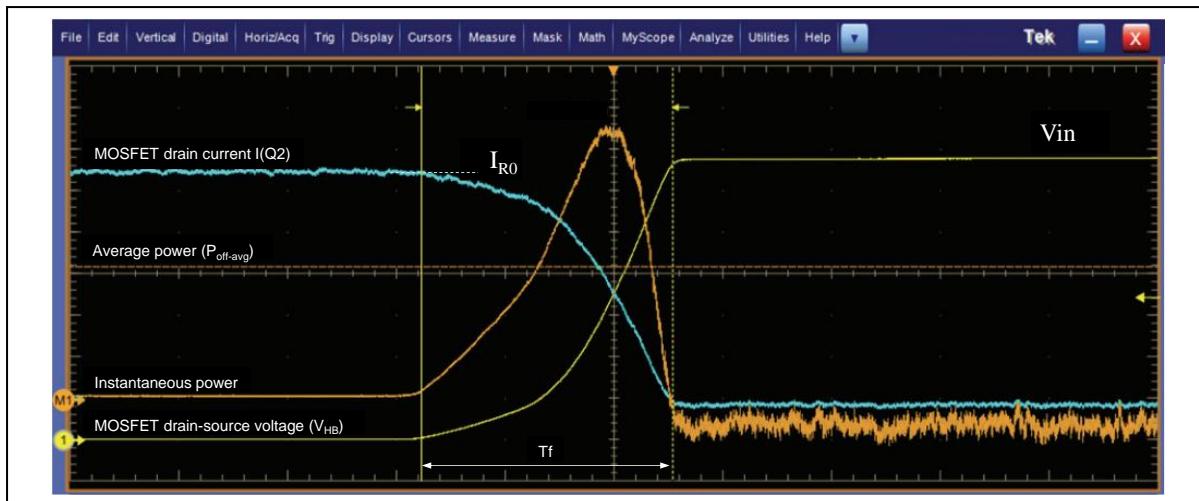
Power loss will be obtained multiplying the energy loss given by (226) by the switching frequency  $f_{sw}$ .

It is often more practical to measure this energy using the math functions of the oscilloscope as in the example shown in figure 100, rather than a theoretical estimate.

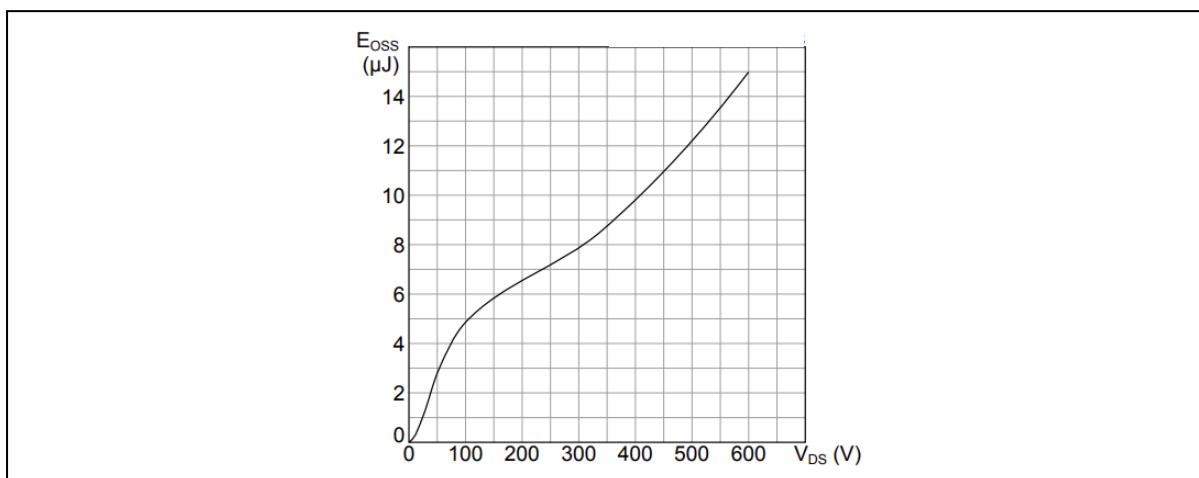
However, this must be done with great care concerning not only voltage and current probing and measurement setup, but also the interpretation of the result.

In fact, the current that can be measured with a probe is the superposition of the current flowing through the channel and that flowing through the  $C_{oss}$  of the power switch. This capacitive component does not generally dissipate power (though it is not exactly true with some MOSFET technologies) therefore the energy measured in this way,  $E_{off} = P_{off\_avg} T_f$  must be reduced by the energy  $E_{oss}$  stored in the  $C_{oss}$ .

**Figure 100. Oscilloscope measurement of turn-off power loss in a MOSFET switch.**



**Figure 101. Output capacitance stored energy in an exemplary MOSFET.**



Typically, a plot like that in figure 101, representing  $E_{oss}$  as a function of the drain-source voltage is provided by most power switch manufacturers. The value of  $E_{oss}$  to be considered is the one with the drain-source voltage in the instant when the drain current zeroes.

Alternatively, if available, one might consider the energy-equivalent capacitance  $C_{eE}$  and use the classical  $(1/2) C V^2$  formula. As a first step, one might start from half the estimated  $C_{HB}$  value.

In the end, the turn-off losses in a power switch can be calculated as:

$$P_{off} = f_{sw} (E_{off} - E_{oss}) . \quad (227)$$

Of course, the same discussion and conclusions can be applied to the turn-off of the high-side switch Q1.

There is actually a fourth source of losses associated to the power switches: gate driving losses. Generally, only a minor portion of these losses are dissipated inside the switches, most of the dissipation occurs in the gate driver circuit. They will negligibly contribute to the thermal stress of the power switches, but they will impact on the overall efficiency, especially at light load where they tend to increase while other losses become insignificant .

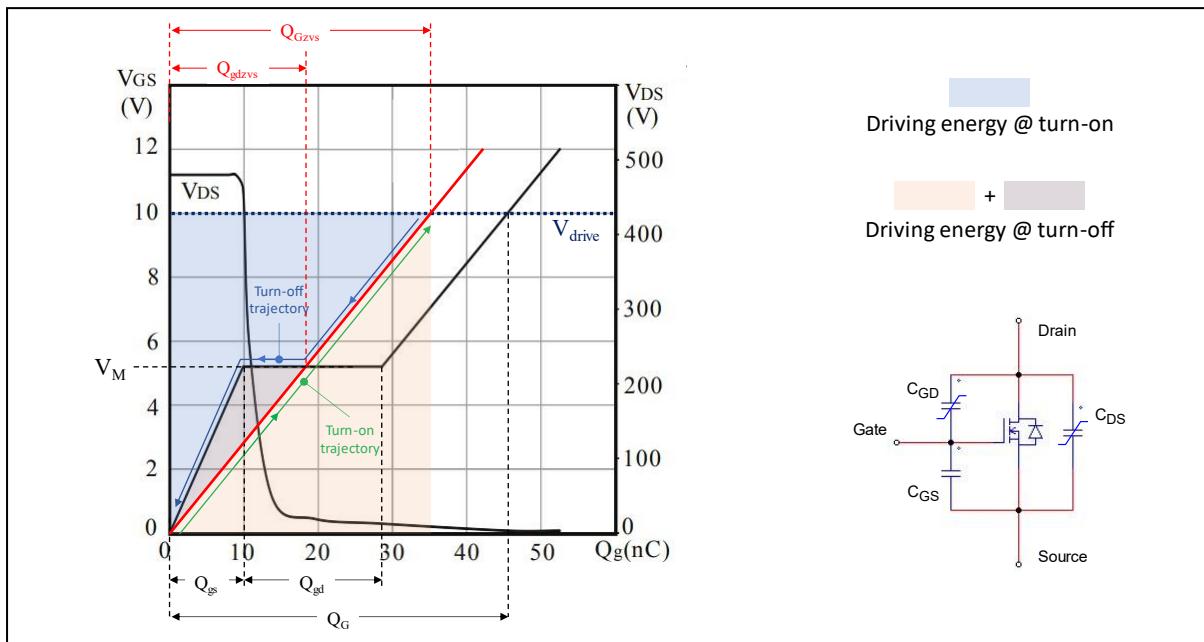
In switches operated with hard switching their expression is:

$$P_{drive} = V_{drive} Q_G f_{sw} , \quad (228)$$

where  $V_{drive}$  is the supply voltage of the gate driver (not necessarily equal to the voltage  $V_{GS}$  delivered to the gate) and  $Q_G$  the total gate charge of the power switch that can be deduced from its gate-charge characteristic, which shows how the gate-source voltage  $V_{GS}$  depends on the stored charge  $Q_g$  in the gate structure. An example is depicted in figure 102.

When power switches are turned on with ZVS like in the LLC converter, i.e., their gate is driven high when their drain-source voltage is zero, the Miller effect due to drain-to-source voltage modulation is absent, and this reduces the gate charge required to turn the power switch fully on. However, as previously seen, turn-off is with hard switching, then the Miller effect is there.

**Figure 102. Gate-charge characteristic for an exemplary MOSFET (black lines: hard switching; red lines: ZVS at turn-on).**



In this case the  $Q_g$  associated to power switches and the relevant driving losses deserve some discussion. Again, these aspects can be conveniently examined on the gate-charge characteristic of the device like that shown in figure 102 for an exemplary power MOSFET.

The black curve is the normal piecewise-linear gate-charge curve: the first portion is that related to the charge of the input capacitance  $\approx C_{GS} + C_{GD}$ , and  $Q_{gs}$  is the charge needed to rise the gate voltage up to the plateau value  $V_M$  that lets the MOSFET carry the specified current.

The flat portion is the so-called *Miller plateau*, where the gate voltage does not increase because the drain-source voltage is falling and  $C_{GD}$  is sucking out the charge delivered to the gate, until the charge  $Q_{gd}$  has been supplied; the third rising portion is related to the overcharge of  $C_{GS} + C_{GD}$  needed to minimize its  $R_{DS(on)}$ .

Note that the slope of third portion,  $(V_{drive} - V_M) / [Q_G - (Q_{gs} + Q_{gd})]$ , is lower than that of the first one,  $V_M / Q_{gs}$ , due to the modulation of  $C_{GD}$ , which is now considerably larger ( $C_{GS}$  is essentially constant). The total gate charge supplied to the gate to take its voltage up to the final value  $V_{GS}$  ( $= V_{drive}$  in figure 102) is  $Q_G$ . The values of  $Q_{gs}$ ,  $Q_{gd}$ ,  $Q_G$  are specified in the datasheet for given  $V_{DS}$ ,  $I_D$  conditions.

When the MOSFET is turned on with ZVS,  $V_{DS} \approx 0$  and  $C_{GD}$  has already its maximum value, then  $V_{GS}$  rises along the red line that starts from the origin of axes and has the same slope as the third portion in the black curve, until it reaches  $V_{drive}$ .

The bluish area included between the gate-charge curve and the  $V_{drive}$  horizontal line is the energy  $E_{drive-on}$  lost in the gate driver to charge the gate up to the final value  $V_{drive}$  and turn the MOSFET fully on. Its value can be found with simple geometric considerations:

$$E_{drive-on} = \int_0^{Q_{Gzvs}} Q_g [V_{drive} - V_{GS}(Q_g)] dQ_g = \frac{1}{2} V_{drive} Q_{Gzvs}, \quad (229)$$

where  $Q_{Gzvs}$  is the value of  $Q_g$  at the intersection of the red line with the  $V_{drive}$  horizontal line. Its value is given by:

$$Q_{Gzvs} = \frac{V_{drive}}{V_{drive} - V_M} [Q_G - (Q_{gs} + Q_{gd})]. \quad (230)$$

When the MOSFET is turned off, initially  $V_{GS}$  falls following the same red line, until it reaches the Miller plateau  $V_M$ , where  $V_{GS}$  moves again along the black curve: the gate voltage does not decrease because the drain-source voltage is rising and  $C_{GD}$  is injecting the charge that is being removed from the gate, until and the modulation of  $V_{DS}$  is over and  $Q_g \approx Q_{gs}$ .

The light ocher area below the red gate charge curve, along with the grayish area between the red line and the black curve represents the energy  $E_{drive-off}$  lost in the gate driver to discharge the gate from  $V_{drive}$  to zero. Again, from simple geometric considerations:

$$E_{drive-off} = \int_0^{Q_{Gdzvs}} Q_g V_{GS}(Q_g) dQ_g = \frac{1}{2} V_{drive} Q_{Gzvs} + \frac{1}{2} V_M (Q_{gdzvs} - Q_{gs}), \quad (231)$$

where  $Q_{gdzvs}$  is the value of  $Q_g$  at the intersection of the red line with the Miller plateau  $V_M$ . Its value is given by:

$$Q_{gdzvs} = \frac{V_M}{V_{drive} - V_M} [Q_G - (Q_{gs} + Q_{gd})]. \quad (232)$$

The total driving energy is therefore given by:

$$E_{drive} = E_{drive-on} + E_{drive-off} = V_{drive} Q_{Gzvs} + \frac{1}{2} V_M (Q_{gdzvs} - Q_{gs}), \quad (233)$$

In the end, it is possible to define an equivalent gate-charge  $Q_{Gzvs\_e}$  that can be used in (228) in place of  $Q_G$  to estimate the driving losses  $P_{drive}$ :

$$Q_{Gzvs\_e} = Q_{Gzvs} + \frac{1}{2} \frac{V_M}{V_{drive}} (Q_{gdzvs} - Q_{gs}). \quad (234)$$

So, finally:

$$P_{drive} = V_{drive} Q_{Gzvs\_e} f_{R1}. \quad (235)$$

These formulas fit equally well both MOSFETs and GaN HEMTs. In the end, the total losses in a power switch will be given by:

$$P_{switch} = P_{revcond} + P_{cond} + P_{off}, \quad (236)$$

and the thermal design will be based on this result.

Normally, the maximum ambient temperature  $T_{a\max}$  and the maximum junction temperature  $T_{j\max}$  are specified, so with the datum of power dissipation  $P_{switch}$  one can also determine the  $R_{th,j-a}$  of the package necessary to achieve thermal stability:

$$R_{th,j-a} = \frac{T_{j\max} - T_{a\max}}{P_{switch}}, \quad (237)$$

The driving losses (235) will be added to assess the overall power dissipation associated to a power switch for efficiency estimate.

If the total loss budget in the power switches is provided, do not forget that each switch accounts for one half of the total budget in a half bridge and for one fourth in a full bridge.

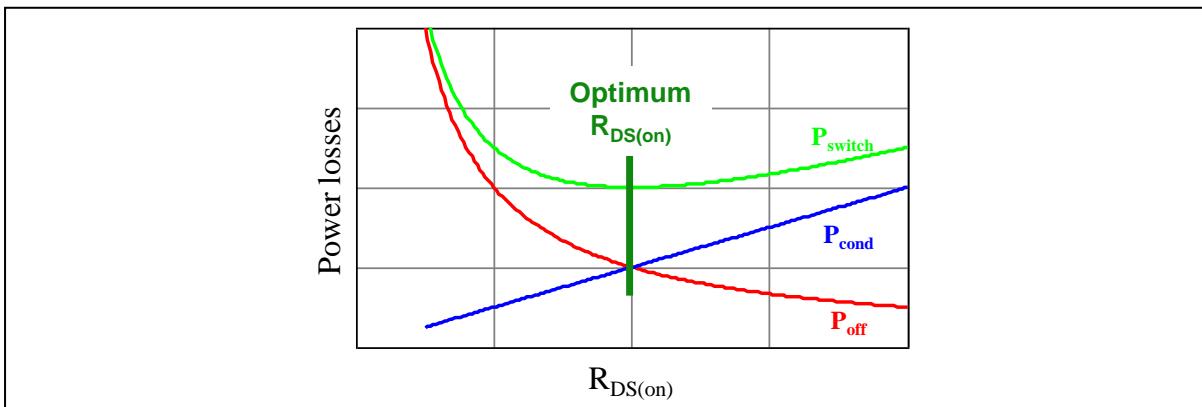
We have now all the elements to choose the most appropriate power switch in each application. The selection will aim at optimizing efficiency, and to do so a well-balanced ratio between turn-off losses and conduction losses needs to be found. The selection is even more complex if high efficiency is specified on a wide load range: at heavy load, conduction losses are the biggest contributor to the total losses, then calling for the lowest  $R_{DS(on)}$ , at light load conduction losses play a minor role and turn-off losses, which tend to be larger, are dominant.

As shown in the plot of figure 103, to choose the best fitting MOSFET, there is an optimum value of  $R_{DS(on)}$  that minimizes the overall losses. This value depends on the load conditions; thus, the assessment should be repeated considering an adequate number of operating points covering the load range.

However, as a rule, targeting an  $R_{DS(on)}$  slightly larger than the optimum value is advantageous for two reasons. Going above the optimum value, the total power losses increase almost linearly, whereas going below the optimum value they increase much faster. Additionally, at light load turn-off losses will be reduced and efficiency improved over a wider load range.

The selection of the package will be essential too, to have a junction-ambient thermal resistance  $R_{th,j-a}$  such that the junction temperature will not exceed the maximum specified. In case, heat sinking must be provided.

**Figure 103. Power losses vs.  $R_{DS(on)}$ .**



### Output rectification design and secondary rectifiers selection

The first choice concerns the output rectification configuration, whether CT-FW or SE-B, or VD. In the introduction to the LLC converter, it was stated that CT-FW is preferable with a low output voltage and high output current, whereas SE-B better suits high output voltage applications. As a rule of thumb, CT-FW is nearly always used with output voltages up to 12 V, SE-B with output voltages of 48 V and above. In the middle, either configuration can be found, and the selection is often a compromise between efficiency, PCB real estate, cost, transformer construction issues. For higher voltages (100 V and above) and low power levels (say below 500 W) VD configuration could be a good solution.

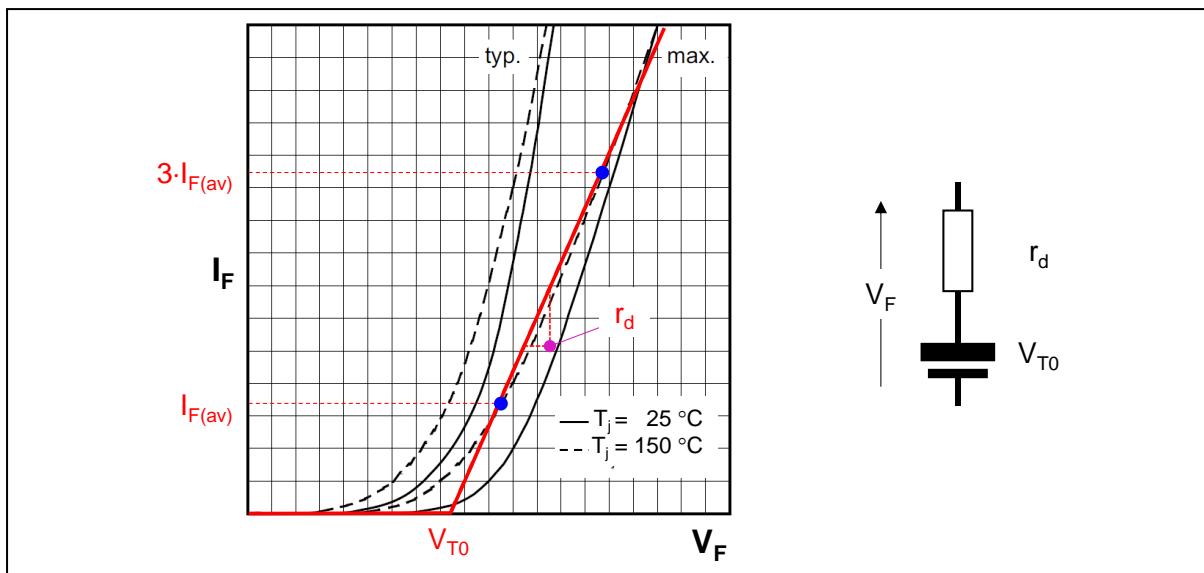
The second choice concerns the rectification devices: diodes or MOSFETs (synchronous rectification). It depends primarily on efficiency, cost, and power density targets, as well as on design complexity: diodes do not need any control, synchronous rectification does, but this will be examined more in details in Part VI, chapter 1.

Like with the primary switches, the selection of the rectification devices, whether they are diodes or MOSFETs, will be based on their voltage and current rating, finding the best compromise between power losses and overall cost (included that of heatsinks if necessary).

Their voltage stress can be determined with the aid of equations III in Table 5. It is always a good practice to consider some safety margin (20%-25%).

Considering diode rectification, although the secondary rectifiers always work with ZCS, it is recommended to use ultrafast p-n diodes or, whenever allowed by the reverse voltage, Schottky diodes because they feature a lower forward drop  $V_F$  and therefore minimize conduction losses. Some care, however, needs to be taken with the selection of the voltage rating of Schottky diodes. In diodes the forward drop for a given current rating and a given current level is lower if their voltage rating is lower (the silicon die is less resistive if its voltage breakdown is lower), thus one might be tempted to use a voltage class barely enough to withstand the voltage stress in view of minimizing losses. Schottky diodes, however, have a significant leakage current when they are reverse biased, which increases with the applied reverse voltage and with temperature, and that causes significant power losses. It is not infrequent, then, that using Schottky diodes with a higher breakdown voltage, one obtains lower losses and achieves higher efficiency despite the larger forward drop.

**Figure 104. Diode forward characteristic, piecewise linear model, and equivalent circuit.**



As to the current rating, it is a common design practice to choose a diode rated for 2-3 times the dc current it is supposed to carry, given by equations VIII in Table 6. Once selected a diode, the power losses must be computed anyway before confirming the selection.

Conduction losses are essentially the sole power losses source, ZCS (or nearly so) operation makes forward and reverse recovery losses negligible.

To estimate conduction losses in a diode, it is customary to approximate its exponential-like forward characteristic with a piecewise linear one, as illustrated in figure 104.

Considering the forward characteristic at the maximum forward voltage and maximum operating temperature, an oblique line is drawn that intersects this characteristic at the dc current the diode is supposed to carry ( $I_{F(av)}$ ) and at 3  $I_{F(av)}$  (the blue dots in figure 104). The slope of this line determines the resistance  $r_d$  of the equivalent circuit, and the intersection with the horizontal axis the threshold voltage  $V_{T0}$ . With this approximation, the forward drop  $V_F$  is given by:

$$V_F = V_{T0} + r_d I_F . \quad (238)$$

Normally,  $V_{T0}$  and  $r_d$  are provided in the datasheet for each part number. With this linearized model the expression of the conduction losses is:

$$P_{D-cond} = V_{T0} I_{F(av)} + r_d I_{F(rms)}^2 , \quad (239)$$

where  $I_{F(rms)}$  is the rms value of the diode current, given by equations VIII in Table 6.

Considering synchronous rectification (SR), the selection of the optimum SR MOSFET follows essentially the same guidelines as the primary switches. Power losses will be originated mostly by conduction losses:

$$P_{SR-cond} = R_{DS(on)} I_{SR(rms)}^2 , \quad (240)$$

where  $I_{SR(rms)}$  is given by equations VIII in Table 6. If the control of the SR MOSFET does not emulate exactly the behavior of a diode, reverse conduction losses due to the body diode should be considered too:

$$P_{SR-revcon} = 2 \alpha I_{RTD} V_F T_{BD} f_{R1} , \quad (241)$$

where  $I_{RTD}$  is given by (217), the forward drop  $V_F$  of the body diode can be identified with its  $V_{T0}$  and  $T_{BD}$  is the total conduction time of the body diode in each switching half cycle.

To properly select the  $R_{DS(on)}$  it is important to also evaluate the impact of the driving losses that, again, do not affect the thermal design of the SR MOSFETs but do affect efficiency. In this case, since the SR MOSFET operates with ZVS (and ZCS) at turn-on and with ZCS at turn-off, the operating point of the gate drive circuit moves entirely on the red line of the gate charge characteristic shown in figure 102. Therefore, the driving losses can be expressed by:

$$P_{SR-drive} = V_{drive} Q_{Gzvs\_e} f_{R1} . \quad (242)$$

where it is:

$$Q_{Gzvs\_e} = Q_{Gzvs} = \frac{V_{drive}}{V_{drive}-V_M} [Q_G - (Q_{gs} + Q_{gd})] . \quad (243)$$

Another aspect to consider is their  $C_{oss}$ . As highlighted in Part III, chapter 1, it affects the light-load and no-load operation of the converter, potentially originating the feedback reversal phenomenon. Then, the compromise that finds the optimum  $R_{DS(on)}$  for the SR MOSFET involves not only the  $P_{SR-cond}$  vs.  $P_{SR-drive}$  losses trade-off but also the resulting  $C_{oss}$ , which normally increases as  $R_{DS(on)}$  decreases. This can orient the choice of SR MOSFETs to technologies that offer not only a low  $Q_G \cdot R_{DS(on)}$  but also a low  $C_{oss} \cdot R_{DS(on)}$  FOM.

It is worth reminding that if the total loss budget in the secondary rectifiers is provided, the power losses calculated so far accounts for one half of the total budget in case of CT-FW or VD configuration, and for one fourth in case of SE-B configuration.

#### *Output capacitor selection*

We have seen that the LLC converter is characterized by a voltage sink output structure, so that the output rectifiers push current directly in the output capacitive filter. Therefore, large, low-ESR electrolytic capacitors usually do the filtering work. Aluminum polymer capacitors are particularly suitable because of their favorable characteristics.

The parameters to be considered for their selection are the working voltage, the ac current rating and the ESR. Unless special cases, the actual capacitance value  $C_{out}$  is not that important.

Obviously, the dc working voltage must be greater than  $V_{out}$ , as specified by equation IV in Table 5. A margin of 25% is recommended for the sake of reliability.

The ac current that flows through the output capacitor causes power dissipation on its ESR and a resulting temperature rise, which is the major responsible for capacitor degrading. It is important not to operate the capacitor beyond its ac current rating, otherwise its lifetime will be compromised. This parameter is usually specified at 85 °C or 105 °C ambient temperature, and there are some special classes rated at 130 °C. The value could be derated considering the actual maximum ambient temperature ( $T_{a_{max}}$ ) and the desired capacitor's lifetime.

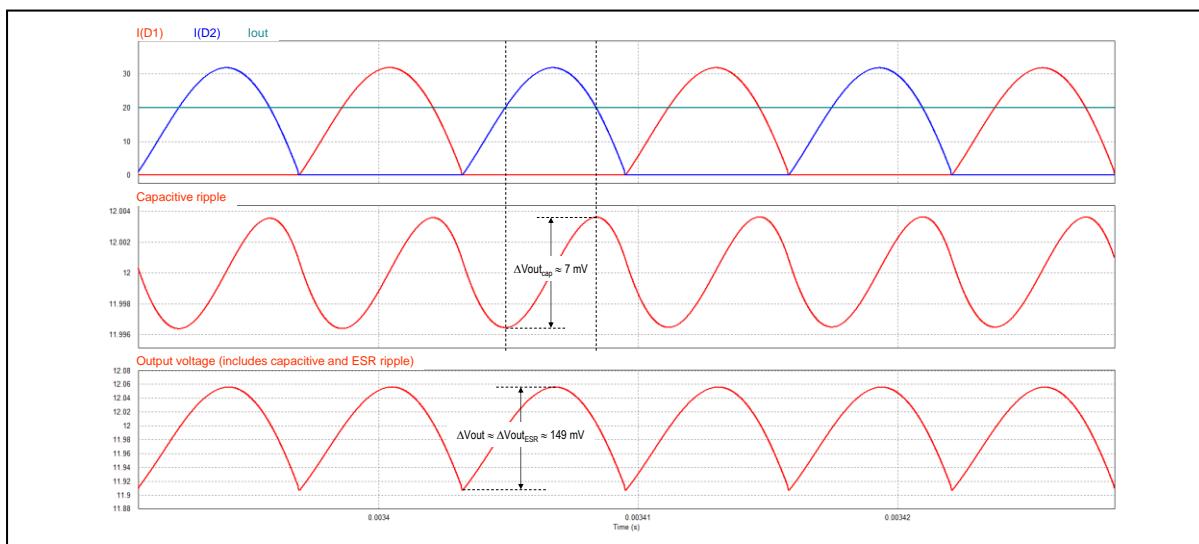
In a conservative design no derating is applied, and the ac current capability must be larger than  $I_{sec\_ac}$  given by equation IX in Table 6. Usually, the specification cannot be met using a single capacitor, so several of them connected in parallel are often used.

The ESR, besides being responsible for capacitor heating, is what basically determines the voltage ripple at the switching frequency superimposed on top of the dc value and illustrated in figure 105. The peak-to-peak amplitude of this ripple, given by:

$$\Delta V_{out,ESR} = I_{sec\_pk} \text{ ESR ,} \quad (244)$$

with  $I_{sec\_pk}$  given by equation VI in Table 6, is normally much larger than the capacitive contribution to the ripple, as shown in figure 105.

**Figure 105. Capacitive component and ESR component of output voltage ripple.**



Its peak-to-peak amplitude is given by:

$$\Delta V_{out, cap} = \frac{I_{out}}{2\pi f_{R1} C_{out}} \left( 2 \sin^{-1} \frac{2}{\pi} - \pi + \sqrt{\pi^2 - 4} \right) \approx \frac{I_{out}}{3\pi f_{R1} C_{out}} . \quad (245)$$

This is true if the following condition is met:

$$ESR \cdot C_{out} \gg \frac{2}{3\pi^2 f_{R1}} . \quad (246)$$

Therefore, the specification on the maximum allowed output ripple  $\Delta V_{out}$  is translated into a requirement on the maximum ESR of the capacitor:

$$ESR < \frac{2}{\pi} \frac{\Delta V_{out}}{I_{out, max}} . \quad (247)$$

Picking a capacitor (or a certain number of capacitors) that fulfill the specification on either the ac ripple current or the ESR, the resulting capacitance value very likely meets condition (246). If not, considering that the two ripple components are in quadrature, the total ripple can be found with:

$$\Delta V_{out} = \sqrt{\Delta V_{out, ESR}^2 + \Delta V_{out, cap}^2} . \quad (248)$$

It is worth noticing that the power dissipation on the ESR might affect the computation of converter's efficiency. This dissipation can be estimated as follows:

$$P_{ESR} = I_{sec\_ac}^2 ESR = \left( \frac{\pi^2}{8} - 1 \right) I_{out, max}^2 ESR . \quad (249)$$

If the requirement on ESR is very tight, there is an alternative to using many output capacitors: it is possible to tolerate a higher ripple on  $C_{out}$  (provided the ac ripple requirement is met) and add an LC post filter, like the one shown in figure 106, that may attenuate the ripple to the desired level.

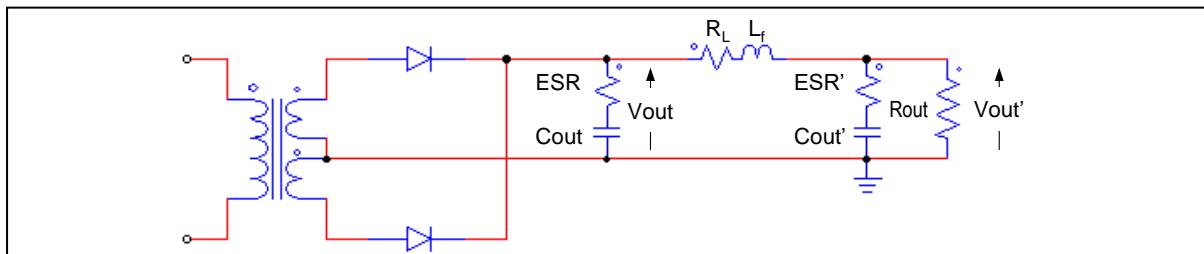
A first-harmonic analysis shows that the attenuation factor of such filter, if its cutoff frequency is at least one decade lower than  $f_{R1}$ , is approximately given by:

$$\frac{\Delta V_{out'}}{\Delta V_{out}} \approx \frac{2}{3\pi^2} \frac{ESR'}{f_{R1} L_f} . \quad (250)$$

It is convenient to choose an off-the-shelf choke and then select a capacitor with an ESR low enough to get the desired attenuation level. For low output current (less than 1 A) ferrite beads may be used. The most significant drawback of this approach is the drop across the series resistor  $R_L$ , its adverse effect on converter's load regulation and the associated power losses. Trying to compensate the drop on  $R_L$  by feedback might result in stability issues due to the additional phase shift introduced by the LC network.

A final note on the overall rectification plus filtering block: the secondary rectification current paths should be as symmetric as possible to assure the same parameters for tank circuit in each switching half cycle. Doing otherwise would cause the same asymmetry issues aroused by asymmetric secondary windings in case of CT-FW rectification configuration.

**Figure 106. Output post filter for output voltage ripple reduction.**



## EXAMPLE

It may be instructive to consider a design example based on the converter specified in Table 4 and whose LLC tank has been designed in the previous chapter. It is worth stating that a real design procedure is way more complex and is based on more detailed specifications that includes also non-electrical items. The intent here is to provide just a guideline that may help the neophyte to familiarize with the LLC design challenges.

First, let's try to establish a power loss budget. Based on the expected efficiency, the total power losses will be:

$$P_{loss} = P_{out,max} \left( \frac{1}{\eta} - 1 \right) = 240 \left( \frac{1}{0.95} - 1 \right) = 12.6 \text{ W} .$$

The specification on the secondary rectifier forward drop provides a clue on what the power loss level on them could be:

$$P_{SR} \approx I_{out,max} V_{Rect} = 20 \cdot 0.1 = 2 \text{ W} ,$$

1 W per each rectifier. Obviously, to achieve this  $V_{Rect}$  synchronous rectification is mandatory.

**Table 7. Provisional power losses allotment for converter specified in Table 4**

Part	Loss Budget [W]
Integrated transformer	4
Resonant capacitor	0.5
Primary switches	3
Secondary rectifiers	2
Output capacitors	0.5
Other losses (driving losses, sense resistors, PCB traces, etc.)	1.6
<b>Total losses</b>	<b>12.6</b>

**Table 8. Max voltage stress on power components of converter specified in Table 4**

#	Part	Max. voltage stress [Vdc]
1	Primary switches	450
2	Resonant capacitor	400
3	Secondary rectifiers	30
4	Output capacitor(s)	12

**Table 9. Max current stress on power components of converter specified in Table 4**

#	Part	Max. current stress [A]
1	Switched current	$I_{R0} = 1.15$
2	Primary switches	$I_{SWrms} = 1.17$
3	Primary winding & resonant capacitor	$I_{Rrms} = 1.65$
4	Dc output current	$I_{out,max} = 20$
5	Peak output current	$I_{sec,pk} = 31.4$
6	Secondary windings	$I_{sec1,2,dc} = 10$
		$I_{sec1,2,rms1} = 11.1$
7	Secondary rectifiers	$I_{D1,D2,dc} = 10$
		$I_{D1,D2,rms} = 15.7$
8	Output capacitor(s)	$I_{sec,ac} = 9.67$

Table 7 shows a first-cut allotment of the losses, which will be very likely to be reviewed in a post-design check. Tables 8 and 9, instead, show the numerical values of the quantities in Tables 5 and 6 respectively, calculated for the converter specified in Table 4.

### *Transformer design results*

As already mentioned, a detailed discussion of the transformer design is beyond the scope of the present work. Here we just summarize in Table 10 the electrical specification of a transformer that meets the requirements of the LLC tank design carried out in Chapter 8 and those listed in Table 9.

**Table 10. Resonant transformer electrical specification**

Parameter	Value	Test conditions
Primary inductance	$660 \mu\text{H} \pm 10\%$	10 kHz, 100 mV. Secondaries open
Primary leakage inductance	$100 \mu\text{H} \pm 10\%$	Secondaries shorted
Primary leakage inductance mismatch	< 5%	One secondary shorted at a time
Number of primary turns	35	
Number of secondary turns	2	
Primary winding dc resistance	$150 \text{ m}\Omega \pm 10\%$	T <sub>a</sub> = 20 °C
Secondary windings dc resistance	< 5 mΩ	T <sub>a</sub> = 20 °C
Insulation voltage	3200 Vac	T <sub>a</sub> = 20 °C, 1 minute
Ferrite Core	E36/18/11 – 3C94	

### *Resonant capacitor selection*

The C<sub>r</sub> value closest to the target (44.8 nF) can be obtained by paralleling two 22 nF capacitors. Alternatively, one could consider a 47 nF part. The selected capacitor should be rated for a dc voltage larger than 400 V (Table 8, line 2) and an ac current rating greater than 1.65 A (Table 9, line 3). Capacitor series with 5% tolerance on the capacitance value are recommended.

As to the voltage rating, most manufacturer provide metallized polypropylene parts rated 630 Vdc, which is adequate also considering the safety margin ( $400 \text{ V} \cdot 1.25 = 500 \text{ V}$ ).

As to the current rating, sometimes manufacturers do not provide it explicitly, they specify the maximum permissible ac (sinusoidal) voltage, usually in terms of rms value. Therefore, it is useful to estimate the amplitude of the resonant voltage on top of the dc value. From equation II in Table 5:

$$\Delta V_{C(pk)} = V_{Cmax} - \frac{1}{2}V_{inmin} = 400 - \frac{1}{2}300 = 250 \text{ V} ,$$

which corresponds to  $250/\sqrt{2} = 176$  Vrms. A single capacitor should have a maximum permissible ac voltage greater than 176 Vrms. In case of two paralleled capacitors, each should have a maximum permissible ac voltage greater than  $176/2 = 88$  Vrms.

### *Primary Switch (MOSFET) selection*

Considering the maximum expected voltage stress (Table 8, line 1) and 25% safety margin ( $450 \cdot 1.25 \approx 560$  Vdc), 600 or 650 V rated MOSFETs will be considered. One might also consider using MOSFETs with a fast body-diode for greater safety.

We have 3 W loss budget for the primary switches, 1.5 W each. An initial estimate of the switching losses and the reverse conduction losses provides:

- Turn-off losses: from (226), assuming a reasonable  $T_f = 50$  ns:

$$E_{off} \approx \frac{(I_{R0} T_f)^2}{24 C_{HB}} = \frac{(1.15 \cdot 50 \cdot 10^{-9})^2}{24 \cdot 200 \cdot 10^{-12}} \approx 0.7 \mu\text{J} ,$$

Without additional info, we consider:

$$E_{oss} \approx \frac{1}{2} \frac{C_{HB}}{2} V_{in nom}^2 = \frac{1}{2} \cdot 100 \cdot 10^{-12} \cdot 400^2 \approx 8 \mu\text{J} ,$$

Clearly, losses cannot be negative, so we can initially assume that turn-off losses are negligible.

- Reverse conduction losses: from (23) we can estimate that  $T_T \approx 70$  ns; assuming an average drop of 1 V across the body diode, from (219), in combination with (217) and (218) we can compute:

$$P_{revcon} = I_{RTD} V_{DS}(T_D - T_T) f_{R1} = -0.97(-1)(300 \cdot 10^{-9} - 70 \cdot 10^{-9}) 75 \cdot 10^3 \approx 17 \text{ mW} ,$$

Therefore, only conduction losses will be significant. The  $R_{DS(on)}$  required at the expected operating temperature can be estimated form (220):

$$R_{DS(on)} = \frac{P_{cond}}{I_{SW rms}^2} = \frac{1.5}{1.17^2} \approx 1 \Omega ,$$

With no other information available, considering the typical trend of  $R_{DS(on)}$  vs.  $T_j$  in high-voltage MOSFETs, we can assume that the  $R_{DS(on)}$  @  $T_j = 25$  °C is half this value. Then, after selecting a MOSFET with about  $0.5 \Omega$   $R_{DS(on)}$  @  $T_j = 25$  °C, it is possible to re-iterate the process just described using its electrical parameters. In few iterations one should converge to an acceptable selection.

For example, let us consider a 600V/ 0.6 Ω part number that in the typical operating conditions has  $T_f = 23$  ns,  $C_{eT} = 120$  pF,  $E_{oss}$  @390 V ≈ 1 μJ, and  $1 \Omega$   $R_{DS(on)}$  @  $T_j = 100$  °C.

With these data,  $E_{off} = 0.1 \mu\text{J}$  ( $C_{eT}$  must be counted 2 times), so turn-off losses are really negligible.  $P_{revcon}$  does not change much and is still negligible too. 100 °C maximum junction operating temperature is a reasonable target, thus this part number fits the initial requirement.

Assuming that the maximum ambient temperature is 40 °C, the package should have no more than 40 °C/W  $R_{thj-a}$  when properly assembled on the PCB. Should this package not be available, one should choose a device with a lower  $R_{DS(on)}$ , or use a heatsink. Being the other losses negligible it is possible to significantly reduce the  $R_{DS(on)}$  and the conduction losses, without significant penalty. Anyway, this is part of the design optimization process.

### *Secondary (synchronous) rectifier selection*

The selection of the synchronous rectifier MOSFET follows essentially the same flow as that described for the primary switches.

Considering the maximum expected voltage stress (Table 8, line 3) and 25% safety margin ( $30 \cdot 1.25 \approx 38$  Vdc), 40 or 60 V rated MOSFETs will be considered. If a 5 or 6 V supply line is available, one might consider using logic-level driving MOSFETs for a lower  $P_{SR-drive}$ .

Since SR MOSFETs work with ZCS at both turn-on and turn-off, one can skip the first step of pre-assessing switching losses and concentrate on conduction losses only.

We have 2 W loss budget, 1 W for each SR MOSFET. Based on equation VIII in Table 6, the required  $R_{DS(on)}$  at the expected operating temperature can be estimated from:

$$R_{DS(on)} = \frac{P_{SR-cond}}{I_{SR(rms)}^2} = \frac{1}{15.7^2} \approx 4 \text{ m}\Omega ,$$

Considering that in low-voltage MOSFETs the  $R_{DS(on)}$  increases with temperature more slowly than in high-voltage MOSFETs, it is possible to estimate that the  $R_{DS(on)}$  @  $T_j = 25^\circ\text{C}$  is two thirds this value.

Then, after selecting a MOSFET with about  $2.9 \text{ m}\Omega$   $R_{DS(on)}$  @  $T_j = 25^\circ\text{C}$ , it is possible to re-iterate the process just described using its electrical parameters. In few iterations one should converge to an acceptable selection.

For example, let us consider a 40V/ 2.8 mΩ logic-level driving part number that in the typical operating conditions, if driven at 10 V, has about 3.9 mΩ  $R_{DS(on)}$  @  $T_j = 100^\circ\text{C}$ ,  $Q_G = 32 \text{ nC}$  and 5.3 mΩ  $R_{DS(on)}$  @  $T_j = 100^\circ\text{C}$ ,  $Q_G = 16 \text{ nC}$  when driven at 5 V. Also, it has  $Q_{gs} = 5.5 \text{ nC}$ ,  $Q_{gd} = 5.1 \text{ nC}$ ,  $V_M = 2.4 \text{ V}$ , and a  $C_{oss}$  @  $V_{DS} = 0$  less than 3 nF.

$100^\circ\text{C}$  maximum junction operating temperature is a reasonable target, thus this part number fits the  $R_{DS(on)}$  requirement if driven at 10 V. When driven at 5 V, the conduction losses would increase at 1.35 W, causing 0.7 W additional power losses. It is however interesting to compare the driving losses with the two driving voltages.

Considering 10 V driving, fitting the values in (243) we find  $Q_{Gzvs\_e} = 28 \text{ nC}$  and a total driving power of 21 mW. One word of caution here: we are assuming that a 10 V supply line is somehow available to power the gate drivers for SR MOSFETs. With 12 V output one could consider driving the gate directly from the output line. In this case  $V_{drive} = V_{out}$  and all  $Q_{gxx}$  should be evaluated at 12 V, resulting in  $Q_{Gzvs\_e} = 34 \text{ nC}$  and a total driving power of 30 mW.

With 5 V driving it is  $Q_{Gzvs\_e} = 10.4 \text{ nC}$  and the total driving power is 4 mW. To this we need to add the loss in stepping down from the output voltage (12 V) to the driving voltage (5 V). Considering that the equivalent gate-drive current amounts at  $10.4 \text{ nC} \cdot 75 \text{ kHz} \approx 800 \text{ uA}$ , these additional losses are 4 mW more for a total of 8 mW against 21 mW (or 30 mW).

In applications with severe no-load consumption requirements it might be worth accepting some more conduction losses and a slightly lower efficiency at full load to achieve the no-load target more easily.

This part number has also a  $C_{oss}$  capacitance lower than the initial estimate, therefore its impact on light load and no-load operation will be lower than expected.

Assuming that the maximum ambient temperature is  $40^\circ\text{C}$ , the package should have no more than  $60^\circ\text{C/W}$   $R_{thj-a}$  when properly assembled on the PCB. Should this package not be available, one should choose a device with a lower  $R_{DS(on)}$  or consider using a heatsink. Also in this case the fact that the other losses are negligible hints at the possibility to significantly reduce the  $R_{DS(on)}$  and the conduction losses, without significant penalty. Anyway, this is part of the design optimization process.

#### *Output capacitor selection*

Considering the maximum expected voltage stress (Table 8, line 4) and 25% safety margin ( $12 \cdot 1.25 \approx 15 \text{ Vdc}$ ), 16 or 20 V rated capacitors will be considered.

Their ac current handling capability can be derived from Table 9, line 8 (9.67 A) while is maximum ESR from

$$ESR < \frac{2 \Delta V_{out}}{\pi I_{out,max}} = \frac{2 \cdot 0.12}{\pi \cdot 20} = 3.8 \text{ m}\Omega .$$

No today available technology can provide a single capacitor with these characteristics. Therefore, after selecting a capacitor family (reminder: aluminum polymer capacitors are a good choice) one can fix a capacitor value and, based on its ac current rating and ESR

calculate how many of them are needed to meet both specifications. Ideally, the two specifications should be met with the same number of capacitors; if not, one can try with a different capacitance value. If, in the end, the capacitors needed to meet the ESR requirement are many more than those needed to meet the ac current specification, one can consider using an LC post-filter.

For example, the 16 V / 330  $\mu$ F part of an aluminum polymer capacitor family withstands 3.3 A ac current at a temperature lower than 105 °C at 100 kHz, with a derating factor of 0.7 for frequencies lower than 100 kHz. In our case, then, its ac rating will be  $3.3 \cdot 0.7 \approx 2.3$  A. Its maximum ESR is 22 m $\Omega$ . We will need 5 of them ( $5 \cdot 2.3 = 11.5$  A > 9.67 A) to meet the ac current requirement and 6 of them ( $22 / 6 \approx 3.7$  m $\Omega$ ) to meet the ESR requirement. The difference is only one and could be acceptable. Also, it would not make any sense using an LC post-filter, which would require two more components.

The resulting peak-to-peak output voltage ripple (all attributed to the ESR) will be:

$$\Delta V_{out} = \frac{\pi}{2} I_{out,max} ESR = \frac{\pi}{2} 20 \cdot 3.7 = 116 \text{ mV} .$$

The capacitive ripple can be estimated with (245):

$$\Delta V_{out,cap} \approx \frac{I_{out}}{3\pi f_{R1} C_{out}} = \frac{20}{3\pi \cdot 75 \cdot 10^3 (6 \cdot 330 \cdot 10^{-6})} \approx 14 \text{ mV} ,$$

which is actually negligible.

The power dissipated in the ESR of the capacitor is:

$$P_{ESR} = I_{sec\_ac}^2 ESR = 9.67^2 \cdot 3.7 \cdot 10^{-3} = 346 \text{ mW} ,$$

below the target of 0.5 W.

Trying with the next part, 16 V / 680  $\mu$ F, the derated current capability is  $\approx 3.5$  A, with 14 m $\Omega$  ESR. We will need 3 of them for the ac current and 4 of them for the ESR. Again, there is still a difference of one but the number of paralleled parts is lower.

The resulting peak-to-peak output voltage ripple (all attributed to the ESR) will be:

$$\Delta V_{out} = \frac{\pi}{2} I_{out,max} ESR = \frac{\pi}{2} 20 \cdot \frac{14}{4} = 110 \text{ mV} .$$

The capacitive ripple can be estimated with (245):

$$\Delta V_{out,cap} \approx \frac{I_{out}}{3\pi f_{R1} C_{out}} = \frac{20}{3\pi \cdot 75 \cdot 10^3 (4 \cdot 680 \cdot 10^{-6})} \approx 10 \text{ mV} .$$

The power dissipated in the ESR of the capacitor is:

$$P_{ESR} = I_{sec\_ac}^2 ESR = 9.67^2 \cdot \frac{14}{4} \cdot 10^{-3} = 327 \text{ mW} ,$$

below the target of 0.5 W.

From the electrical standpoint, the two choices are practically equivalent. However, since the diameter is the same for both capacitors (8 mm), using the 680  $\mu$ F parts will save some PCB area. One more point to look at is that height of the 330  $\mu$ F part is 6.9 mm, while that of the 680  $\mu$ F part is 11.9 mm. If this higher height is not an issue the second option would be preferable from the power density point of view. The difference in cost between the two options should be evaluated as well.

This example shows that there are cases where the final selection is influenced by mechanical considerations and/or cost concerns.

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# PART V

## CONTROL METHODOLOGIES AND SMALL-SIGNAL ANALYSIS

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### Chapter 1

#### Introduction

In most practical cases converters require a closed-loop, negative-feedback control system that keeps the output voltage (or the output current in some systems such as LED drivers and battery chargers) at a constant value (setpoint) upon variations of the operating conditions, i.e., the input voltage and the power demanded by the load.

The control system should be properly designed to ensure the following control objectives:

- a stable control loop: upon disturbances of the operating conditions, once the transient caused by the disturbance has finished, the output voltage or current will reach a new setpoint, i.e., a new steady-state constant value;
- good regulation: the new and the old setpoints will be very close to one another;
- good dynamic performance: the transient will have a short duration and will not cause the output voltage or current to excessively deviate from the setpoint;
- good ripple rejection ratio: the system must be capable of suppressing any noise or ripple superimposed on the dc input voltage to the output. In particular, this applies to offline applications, where the input ripple at twice the ac line frequency (100/120 Hz) that results from input rectification tends to appear on the output voltage and must be attenuated below the specified level.

To do so we need a dynamic model of the converter that enable us to predict how the output voltage or current reacts when the operating conditions change and perturb its steady-state operation.

The difficulty with power converters is that they are inherently nonlinear and time-varying systems because of the switching action; however, and under certain assumptions, they can be approximated by linear and time-invariant (LTI) systems, so that they can be described and represented with the means used for these systems. In particular, they can be described in the frequency domain by a transfer function characterized by gain, zeroes and poles and analyzed with well-known tools such as pole-zero plots and Bode plots.

Additionally, the above-mentioned control objectives, which are often specified in the time domain as transient overshoot/undershoot, settling time and steady-state regulation, may be expressed in terms of some characteristic quantities of the transfer function of the control loop, such as the bandwidth, the phase margin, the dc gain.

Once the transfer function of the converter (*the plant*, in control theory terminology) is known, it is possible to face the design of the control loop. Figure 107 shows a typical block

diagram of a closed-loop control system of an isolated converter with a regulated output voltage, where the converter (power stage) is represented by its transfer function  $G_P(j\omega)$ .

Regulation is achieved by comparing a portion of the output voltage to a reference voltage  $V_{ref}$ . The difference, or error signal  $e$ , between the value provided by the output voltage sensing system (usually, a resistor divider) and the reference value is amplified by an error amplifier and transformed into a control signal  $V_{Cs}$  that is sent to the primary side crossing the isolation barrier and becoming  $V_{Cp}$ . Then  $V_{Cp}$  is transformed by the power modulator into a quantity  $X$  that determines the energy carried by the converter during each switching cycle. The quantity  $X$  is essentially linked to the control methodology, which is therefore a major responsible for providing a given converter topology its dynamic properties.

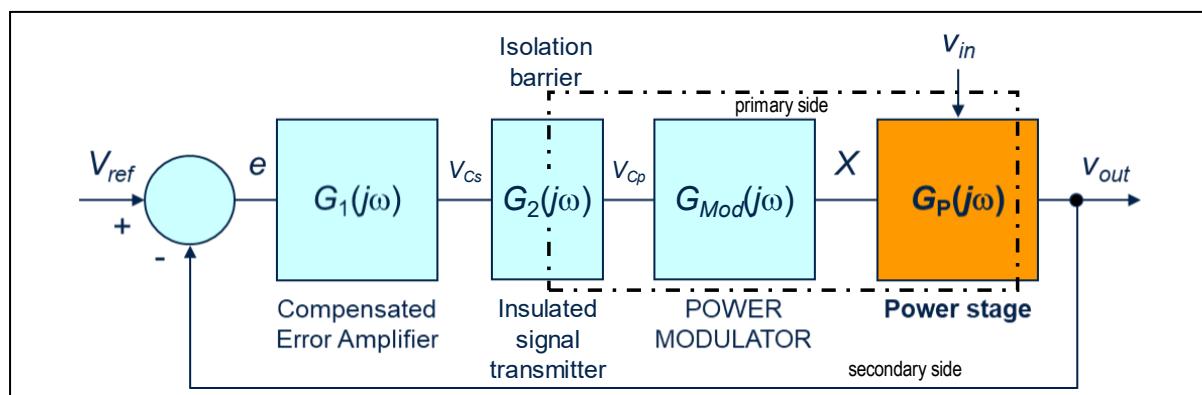
In resonant converters, historically the quantity used to control the converter is the switching frequency of the square wave applied to the resonant circuit (Direct Frequency Control, DFC), therefore most of the converters developed until the first decade of 2000s considered  $X = f_{sw}$ .

The control objectives are achieved by acting on the frequency response of the error amplifier, that is, by shaping gain and phase of its transfer function  $G_1(j\omega)$  with an appropriate placement of poles and zeroes (frequency compensation). This is normally done by using passive networks comprising resistances and capacitors of appropriate value connected to the amplifier (typically, an op-amp). In many practical cases, the control objectives require an open-loop crossover frequency (where the gain is 0 dB) not much higher than  $f_{sw}/10$ .

The converter's transfer function  $G_P(j\omega)$  is the result of the earlier mentioned transformation of a nonlinear time-varying system into a linear time-invariant system. This transformation occurs through a process called *ac modeling* whose objective is to capture the important dominant behavior of the system, neglecting those phenomena that have a minor impact on system's behavior and make the resulting model unnecessarily complicated if not intractable.

At the foundation of the ac modeling process there is the concept of averaging: the strongly nonlinear effects of switching can be removed by considering the average value of the involved quantities in a switching cycle instead of their instantaneous values. This average value may change from one cycle to the next, in a sort of moving average, in this way modeling low frequency variations. However, the resulting equations generally involve the product of time-varying quantities, which generates harmonics, which is a nonlinear process. To be able to use the standard tools of ac circuit analysis we need to take an extra step: we need to linearize those equations.

**Figure 107. Block diagram of the control loop of an isolated power converter.**



Assuming to consider small perturbations of the dc quiescent values around a given operating point of the converter, the equations are manipulated to extract the first-order ac terms, while the dc terms (already known) and the second-order ac terms (much smaller than the first-order ac terms) are discarded. The result of this step is the desired small-signal model of the converter that enables the designer to predict its dynamic behavior.

A lot of ac modeling techniques have been developed over the years, all of them based on the concepts of averaging and small-signal linearization, most of them leading to equivalent end results. For PWM-controlled converters the most relevant two are perhaps the space-state-averaging technique [37] and the circuit-averaging technique [38]. These techniques work well because in PWM-controlled converters the natural frequency of the linear network (the output filter) is much lower than the switching frequency, so that the former acts as a low pass filter. Also, energy modulation is achieved through the low frequency content in the control signal that modulates the dc value of the quantities in the converter which energy depends on.

Unfortunately, these techniques are not applicable to resonant converters, and specifically to the LLC converter, when  $X = f_{sw}$ . In fact, in resonant converters the switching frequency is close to the natural frequency of the linear network represented by the tank circuit that acts as a low-Q bandpass filter, followed by the output low-pass filter. Energy modulation is achieved by interaction between the switching frequency and the resonance frequency. The state variables contain mainly switching frequency components and, unlike in PWM-controlled converters, do not generally have dc content. Averaging methods eliminate the information of switching frequency and consider the low-frequency modulation of dc values, so they are totally unable to predict resonant converter's dynamic properties.

To make things even more complicated, energy modulation causes a simultaneous presence of frequency and amplitude modulation with the consequent generation of numerous sidebands that contribute to the energy transfer process significantly. This harmonic-reach energy flow, going through the nonlinearity represented by the output rectifiers undergoes a frequency mixing process with the generation of the dc component and plenty of even and odd harmonics and the associated sidebands.

This extremely complicated scenario explains why the dynamic behavior and the small-signal modeling of frequency-controlled resonant converters has been for a long time not entirely understood and why simple expressions for  $G_P(j\omega)$  like those of PWM-controlled converters do not exist.

To deal with this intricacy, several approaches have been tried, exploring both the time and the frequency domain.

V. Vorperian in [39] worked out the first small-signal analysis, based on state-space approach and involving both continuous-time and discrete-time analysis. The model could predict the dynamic behavior of the series and the parallel resonant converter with great accuracy but was too complex to provide any physical insight into them.

Sampled-data modeling was first proposed in [40] mainly addressing resonant converters but, again, the results were too complicated and lacking physical insight.

Another line of investigation concerned the frequency domain. The state-space averaging technique [37], which focused on the variations of the dc component only, was extended in [41] by including the switching frequency component too. It assumed that the tank circuit was a selective bandpass filter, so that no other harmonic was considered. That was essentially the small-signal version of the FHA approach and suffered from the same limitations.

The first breakthrough came with the disclosure of the *extended describing function* method [42]-[43]. With this method, the small-signal model of a periodical operating converter can be derived accounting for any order of harmonics of the switching frequency.

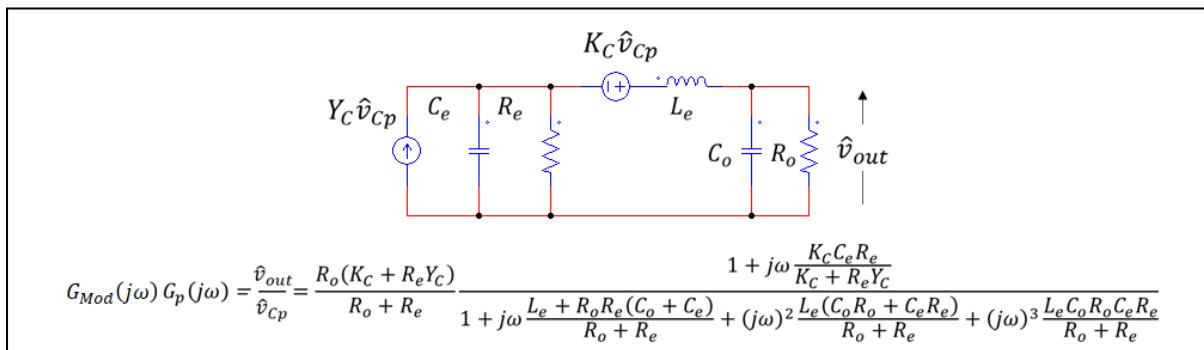
This method includes the state space averaging method as a particular case where only the dc components of the state variables are taken into account, thus it can be used to model PWM converters too. For resonant converters, where, as previously said the switching frequency and its harmonics are key in the power transfer process, the adequate number of higher order harmonics can be included so that the desired accuracy level can be achieved. For single-resonant topologies, such as the LC-series resonant converter and the LC-parallel resonant converter, the fundamental harmonic of the switching frequency is sufficient to provide an accurate small signal model [42]. For multi-resonant converters like the LLC resonant converter, higher-order harmonics are expected to be necessary.

As to the LLC converter, in [15] it is shown that the control-to-output transfer function can be adequately modeled by the fundamental harmonic in the above-resonance operation, which is reasonable since in that operating region the LLC and the LC-series converter are very similar. When operated below resonance, where the lower resonance frequency appears, the control-to-output transfer function needs to account for the third and the fifth harmonic in addition to the fundamental component to achieve adequate accuracy. Adding more harmonics does not make any significant change.

In [42] the extended describing function method correctly predicted the third-order behavior of the series resonant converter as long as the frequency range of interest is lower than the Nyquist frequency  $f_{sw}/2$ . It also predicted the phenomenon known as *beat-frequency oscillation* (interaction between the resonance frequency and the switching frequency), which is modeled with a pair of complex poles. The third pole is related to the output capacitor and the load.

The extended describing function method proved to be a fruitful approach and originated many subsequent works (e.g., [44]-[45]) that gradually refined the method and the model and culminated in [46]-[48].

**Figure 108. Design-oriented small-signal model of LLC resonant converter [47].**



In [47] it is disclosed a design-oriented small-signal equivalent model of the LLC resonant converter, shown in figure 108 along with the resulting  $G_{Mod}(j\omega)$   $G_p(j\omega)$ . It is derived based on an improved describing function approach and employs a process of simplification that reduces the initial infinite-order model to a third-order model capable of accurately describing the transfer function up to  $f_{sw}/2$ .

The five parameters of the model ( $Y_C$ ,  $K_C$ ,  $C_e$ ,  $R_e$ ,  $L_e$ ) are linked to those of the tank circuit and to the operating conditions by complex relationships, some of them obtained by curve

fitting methods. Therefore, in spite of its apparent simplicity, the usage of the model demands extensive calculations and appropriate SW and HW tools.

The merit of this model is its ability to bridge the mathematical model with the physical properties of the LLC tank circuit. The equivalent resistance  $R_e$  represents the impedance of the tank circuit while the equivalent inductance  $L_e$  represents the total energy stored in it. The equivalent capacitance  $C_e$  along with  $L_e$  model the beat frequency phenomenon. The control signal  $v_{Cp}$  (see figure 107) acts on the tank circuit via  $Y_C$  and  $K_C$ , which correctly predicts the dc gain and the position of the RHP zero. Notice that  $Y_C$  and  $K_C$  embed the modulator gain  $G_{Mod}$ .

As previously said, DFC is the traditional control method, applied to essentially all resonant converters and that has been the most used in industry for a long time for the LLC converter as well. Although it is the most straightforward way to control the LLC resonant converter, it is not devoid of shortcomings, especially as far as its dynamic behavior is concerned.

For these reasons several other control methodologies have been developed over the years, especially recently, with the objective of improving the “natural” dynamic behavior with DFC, and some of them are available today in commercial control ICs for resonant converters.

It is worth specifying that switching frequency is the physical quantity that energy flow ultimately depends on, but with control methods other than DFC it is no longer directly controlled. It sets itself at the value that causes converter’s input-output power flow to match the load demand as a result of the control action exercised on a different physical quantity.

In this dissertation the focus will be on these control methodologies, though just a few of them will be reviewed: those that are industry standard today or expected to be in a near future.

As to their underlying small signal characteristics, no tedious derivation will be given, with one exception. It concerns a novel control methodology that seems to outperform the existing ones and that provides the LLC converter with a dynamic behavior that, in the spirit of a design-oriented approach, can be described by a simple approximated small-signal model.

For the other control methods, a descriptive approach will be followed that illustrates the fundamental results of the small-signal analysis and the resulting dynamic properties.

Table 11 shows an inexhaustive list of control methodologies that have been applied to the LLC resonant converter. Those listed in the left-hand column will be reviewed in the next chapters.

One of the objectives of the review is to compare their performance in terms of response speed. To this purpose, some PSIM simulation will be carried out on an exemplary converter whose main electrical specification and parameters are shown in Table 12.

A useful test that enables a straightforward assessment of the inherent response speed of the converter with any control method is to fix the input and the output voltage, apply a step change to the control signal so that the output current changes between two specified values, and observe the time that the output current takes to reach the new steady-state condition.

In this way, one measures the speed at which the tank circuit is capable of changing the amount of power it carries when the quantity  $X$  that modulates the input-to-output power flow with that specific control method is changed.

Before running the open-loop test, the system is simulated closed loop to determine the values of the control signal corresponding to the two specified output current levels at the minimum, typical and maximum input voltage.

**Table 11. Main control methodologies used in LLC resonant converters**

Control method	Ref.	Control method	Ref.
Direct frequency control (DFC)	[49]	<i>Self-sustained oscillation</i>	[60]-[61]
Time-shift control (TSC)	[50]-[51]	<i>Current-mode control</i>	[62]
Charge-mode control (CMC)	[53]-[58]	<i>Average current mode control</i>	[63]-[64]
Average input current control (AICC)	[59]	<i>Optimal trajectory control</i>	[8], [65]

**Table 12. Electrical specification of exemplary LLC resonant half-bridge converter**

Symbol	Name	Value	Unit
$V_{in_{min}} - V_{in_{max}}$	Input voltage range	300 - 450	Vdc
$V_{in_{nom}}$	Nominal input voltage	390	Vdc
$V_{out}$	Regulated output voltage	12	Vdc
$P_{out_{min}} - P_{out_{max}}$	Output power range	0 - 240	W
$f_{R1}$	Upper resonance frequency	78	kHz
$f_{max}$	Maximum switching frequency	225	kHz
$a$	Transformer turns ratio (APR model)	16:1	---
$L_s$	Series inductor	105	$\mu$ H
$L_p$	Parallel inductor	560	$\mu$ H
$C_r$	Resonant capacitor	39	nF
$V_F$	Secondary rectification average forward drop	0.1	Vdc
$\eta$	Estimated efficiency @ $P_{out_{max}}, V_{in_{min}}$	96	%
$C_{HB}$	Half bridge midpoint estimated capacitance	200	pF
$T_D$	Dead-time	300	ns
$C_{out}$	Output capacitor	8 x 470	$\mu$ F
$R_c$	Output capacitor's ESR	38 / 8	$m\Omega$

## Chapter 2

### Direct frequency control (DFC)

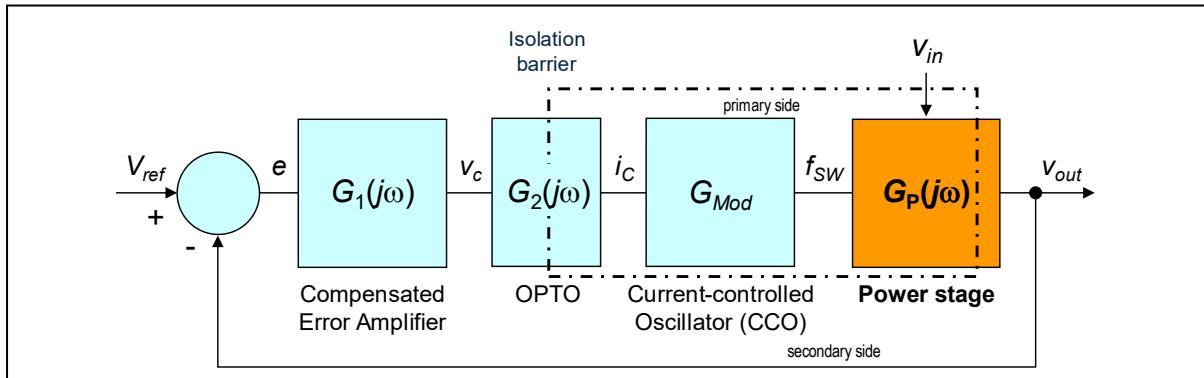
The analysis of the operation of the LLC converter has shown that the switching frequency determines the input-to-output power flow: increasing the frequency, the power diminishes; reducing the frequency, the power increases.

With DFC the controls act directly on the switching frequency to modulate the input-to-output power flow, as shown in the block diagram of figure 109. To do so, the feedback signal directly controls a voltage-controlled oscillator (VCO) or a current-controlled oscillator (CCO), which the switching frequency of the half/full bridge is locked to. This oscillator acts as the power modulator that transforms the control signal into the quantity that the energy carried by the converter substantially depends on, the switching frequency in the present case.

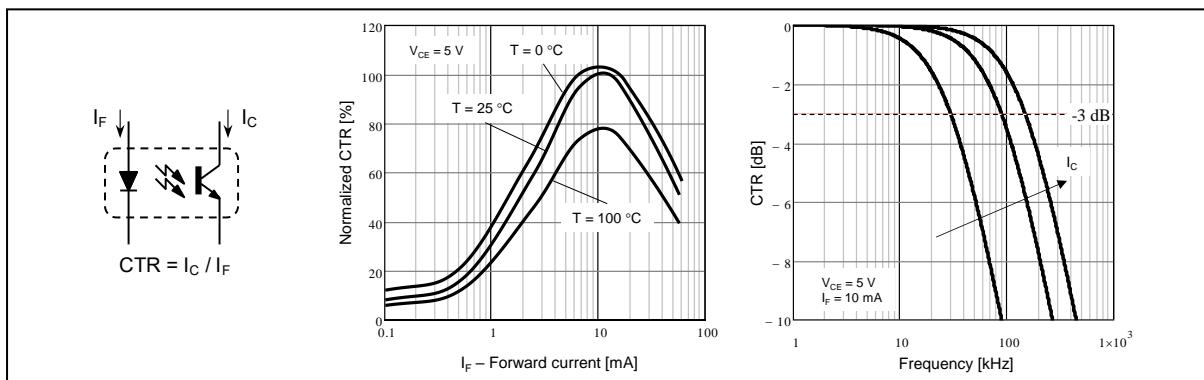
Until not long ago, this was the only control method available in commercially available resonant control ICs. Most of them use a CCO, so that the control variable is a current ( $I_C$ ).

This chimes with the usage of an optocoupler as the insulated signal transmitter to make the control signal  $V_C$ , typically located on the secondary side of the converter, cross the isolation barrier and reach the controller typically located on the primary side. In fact, optocouplers are functionally current-controlled current sources: a current flowing in the photodiode (the input) makes a proportional current flow in the phototransistor (the output) as shown on the left-hand side in figure 110.

**Figure 109. Block diagram of the control loop of an LLC resonant converter with DFC.**



**Figure 110. Typical optocoupler and its CTR vs. photodiode current, temperature and frequency.**



The ratio of the output current to the input current is the Current Transfer Ratio (CTR), one of the most important parameters that define the performance of the device. Unfortunately, the CTR is far from being a constant: as shown in figure 110, its value depends substantially on the photodiode current and on temperature, it suffers from aging and its tolerance is quite loose (sorting is almost invariably used by manufacturers).

Under dynamic conditions the CTR depends on frequency and introduces a pole in the open-loop transfer function. Experience shows that if the desired open-loop bandwidth is in the kHz this pole significantly affects the overall system response.

Despite these concerns, however, optocouplers are successfully used in a wide range of insulated power supplies.

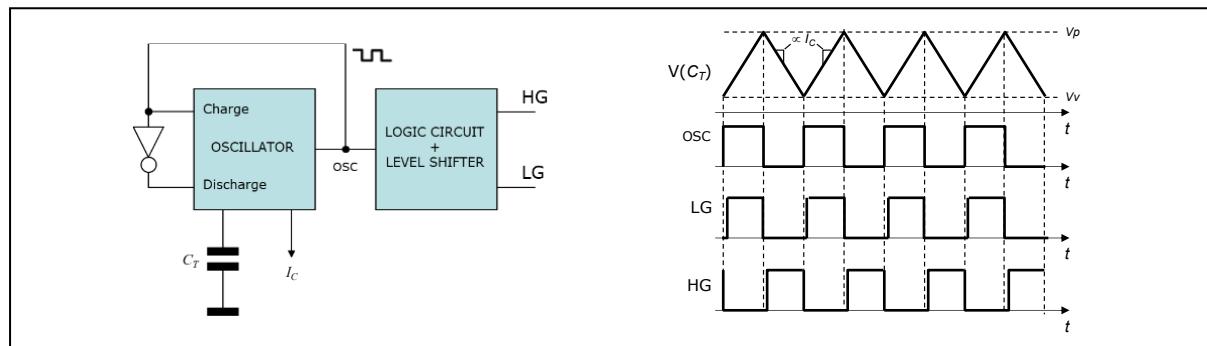
#### *Modulator (CCO) implementation*

Among the many possible implementations of a CCO two are those most found in commercial control ICs for resonant converters. The first implementation, shown in figure 111 on the left-hand side, is based on generating a triangular carrier: the timing capacitor  $C_T$  is alternately charged and discharged between two voltage levels ( $V_p$ ,  $V_v$ ) with a current proportional to the control current  $I_C$ . Every time either level is hit, the half/full bridge is toggled, as shown in the timing diagram of figure 111, right-hand side.

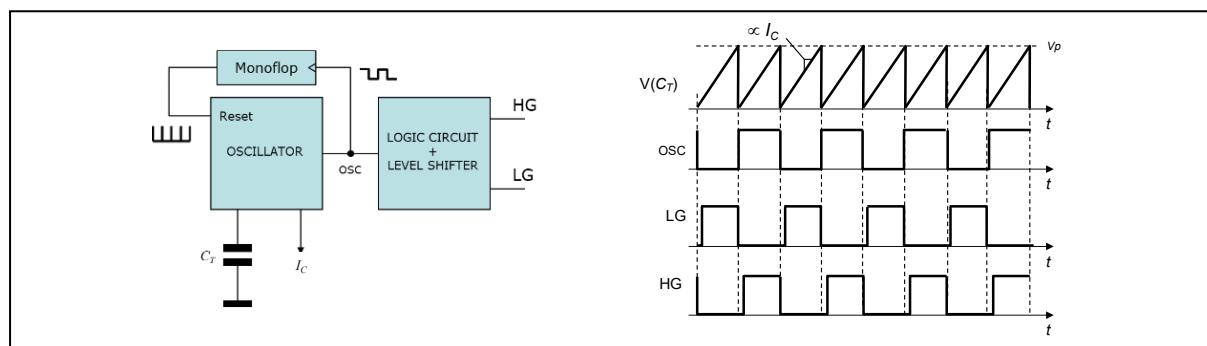
The main challenge with this implementation is to make the charge and discharge currents exactly equal to ensure that a 50% duty cycle square wave is generated.

The second implementation shown in figure 112 on the left-hand side, is based on generating a sawtooth carrier: the timing capacitor  $C_T$  is charged from zero to a peak level ( $V_p$ ) with a current proportional to the control current  $I_C$ . Every time the ramp thus generated hits  $V_p$ ,  $C_T$  is quickly reset at zero and the half/full bridge is toggled, as shown in the timing diagram of figure 112, right-hand side.

**Figure 111. CCO with triangular carrier; block diagram (left) and key waveforms (right).**



**Figure 112. CCO with sawtooth carrier; block diagram (left) and key waveforms (right).**



With this implementation the square wave symmetry is ensured; the frequency of the sawtooth carrier is twice the switching frequency; the fast discharge of  $C_T$  is a potential source of noise.

Assuming that the internal delays in the oscillator circuit are negligible compared to the oscillation period, the frequency-to-control relationship with both implementations is:

$$f_{sw} = \frac{k_T I_C}{2 C_T \Delta V_{C_T}}, \quad (251)$$

where  $k_T$  is the ratio between the charge/discharge current of  $C_T$  and  $I_C$  and  $\Delta V_{C_T}$  the voltage swing on  $C_T$ , i.e.,  $V_p - V_v$  for the triangular carrier generator of figure 111,  $V_p$  for the sawtooth carrier generator of figure 112.

Equation (251) shows a relationship of direct proportionality between the switching frequency and the control signal  $I_C$ , whence the denomination “direct frequency control”.

Regardless of the specific implementation, if the frequency range of interest for the design of the compensator is sufficiently lower than the Nyquist frequency  $f_{sw}/2$ , the modulator gain  $G_{Mod}$  can be considered constant and can be found by differentiating (251). Its expression is:

$$G_{Mod} = \hat{f}_{sw} = \frac{\hat{f}_{sw}}{I_C}, \quad (252)$$

where  $\hat{x}$  denotes the small-signal expression of  $x$ .

#### *Small-signal characteristics of $G_P(j\omega)$*

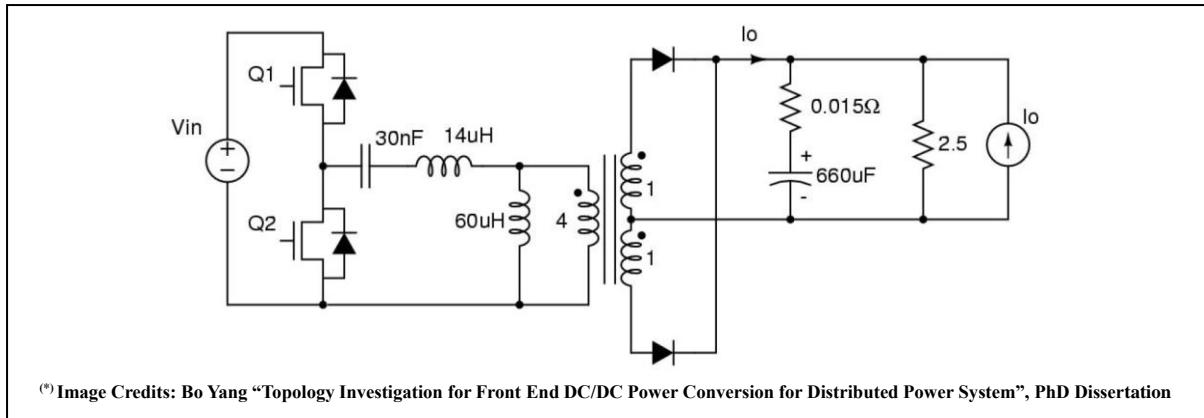
The analytic expression of the transfer function  $G_P(j\omega)$  of the power stage, is shown along the equivalent model in figure 108. As one can see, even neglecting the zero due to the ESR of the output capacitor, the expression is quite complicated; the link of its five parameters to those of the tank circuit, reported in [47], is even more so.

Therefore, in this context it is considered more informative to examine its fundamental characteristics and how the poles and the zeroes move as a function of the operating conditions, as well as of the parameters of the LLC tank, following the discussion in [15].

Considering the frequency range below  $f_{sw}/2$ , the small-signal characteristics of  $G_P(j\omega)$  can be summarized as follows:

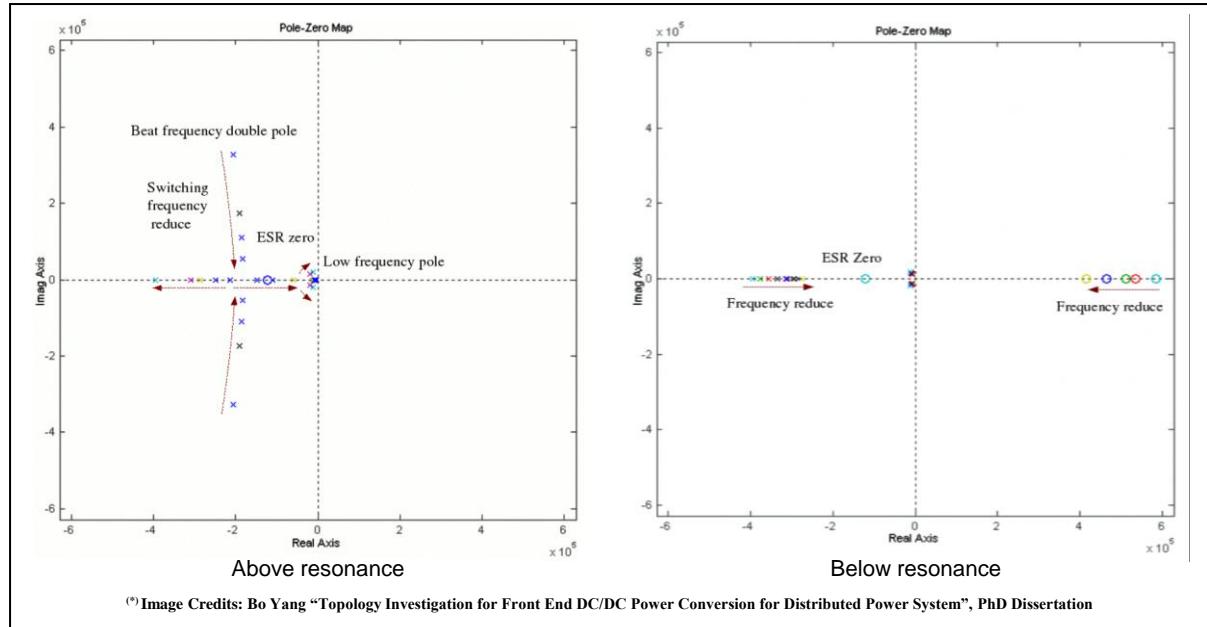
- It is fundamentally a three-pole and one zero dynamic system
  - One low-frequency pole is associated to the output capacitor, two poles to the tank circuit, and the zero to output capacitor's ESR.

**Figure 113. Exemplary LLC converter used to characterize  $G_P(j\omega)$  (\*)**



- The positions of poles change with the switching frequency in a way that depends on converter's operating mode (above, at or below resonance)
  - Above resonance, the behavior is very similar to that of the LC series resonant converter (beat-frequency oscillation)
  - No beat-frequency when operating at resonance or below resonance
  - Below resonance the pole locations are quite stable and a Right-Half-Plane (RHP) zero appears.

**Figure 114. Pole-zero plot of  $G_P(j\omega)$  vs. switching frequency (\*).**



**Figure 115. Bode plot of  $G_P(j\omega)$  vs. switching frequency (\*).**

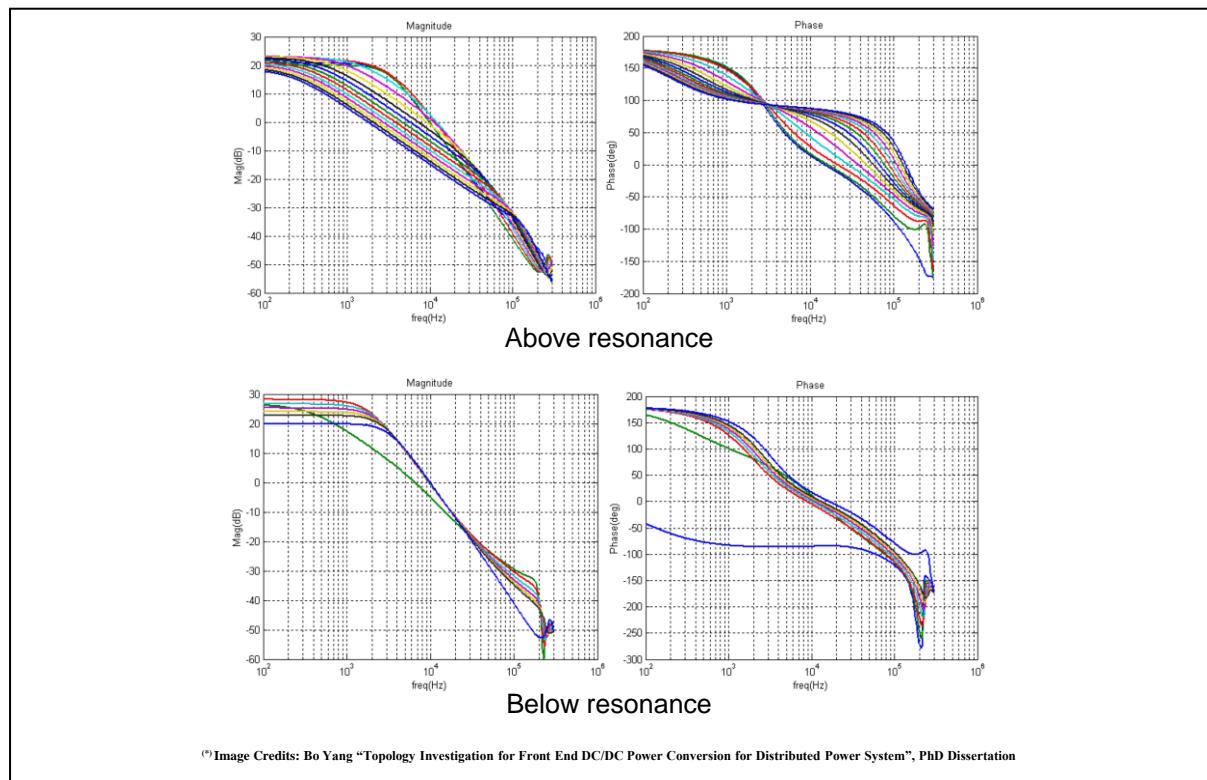


Figure 114 shows the pole-zero plot of  $G_P(j\omega)$  for the exemplary LLC converter shown in figure 113 when operating above and at resonance (a), and below resonance (b), parameterized with respect to the switching frequency  $f_{sw}$ . Figure 115 refers to the same scenario showing the Bode plots of  $G_P(j\omega)$  for different values of  $f_{sw}$ .

When operating above resonance, at a frequency higher than  $f_{R1}$ ,  $G_P(j\omega)$  features a pair of complex conjugate poles (beat frequency double pole), one real low frequency pole and one ESR zero.

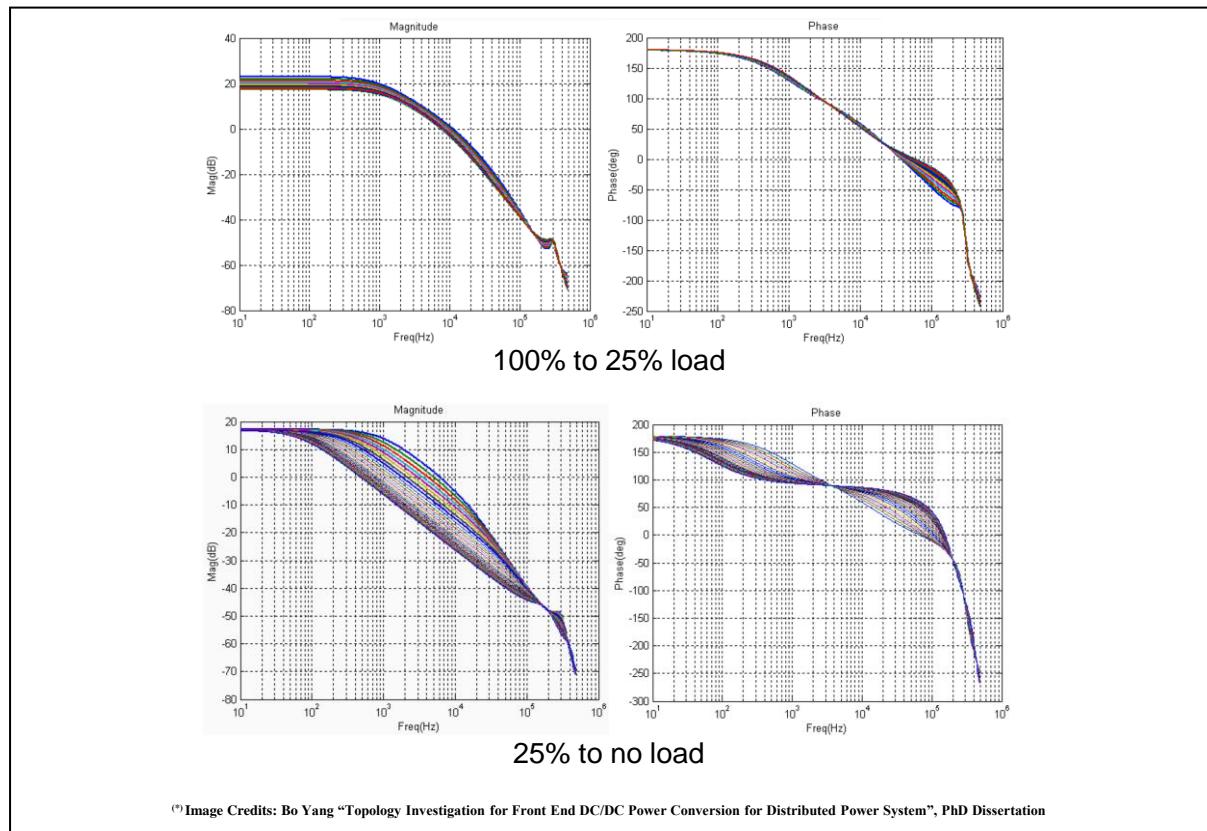
As the switching frequency decreases and moves towards  $f_{R1}$ , the beat frequency double pole moves to a lower frequency. At some point  $f_{sw} > f_{R1}$ , the beat frequency double pole splits and becomes two real poles.

From that point on, as the switching frequency gets closer to and eventually reaches  $f_{R1}$ , one pole moves to higher frequencies and one to lower frequencies. The latter eventually combines with the low frequency pole due to the output capacitor and the load resistor forming a double pole.

When operating below resonance it is possible to observe three poles and one ESR zero in the left-half plane and a RHP zero.

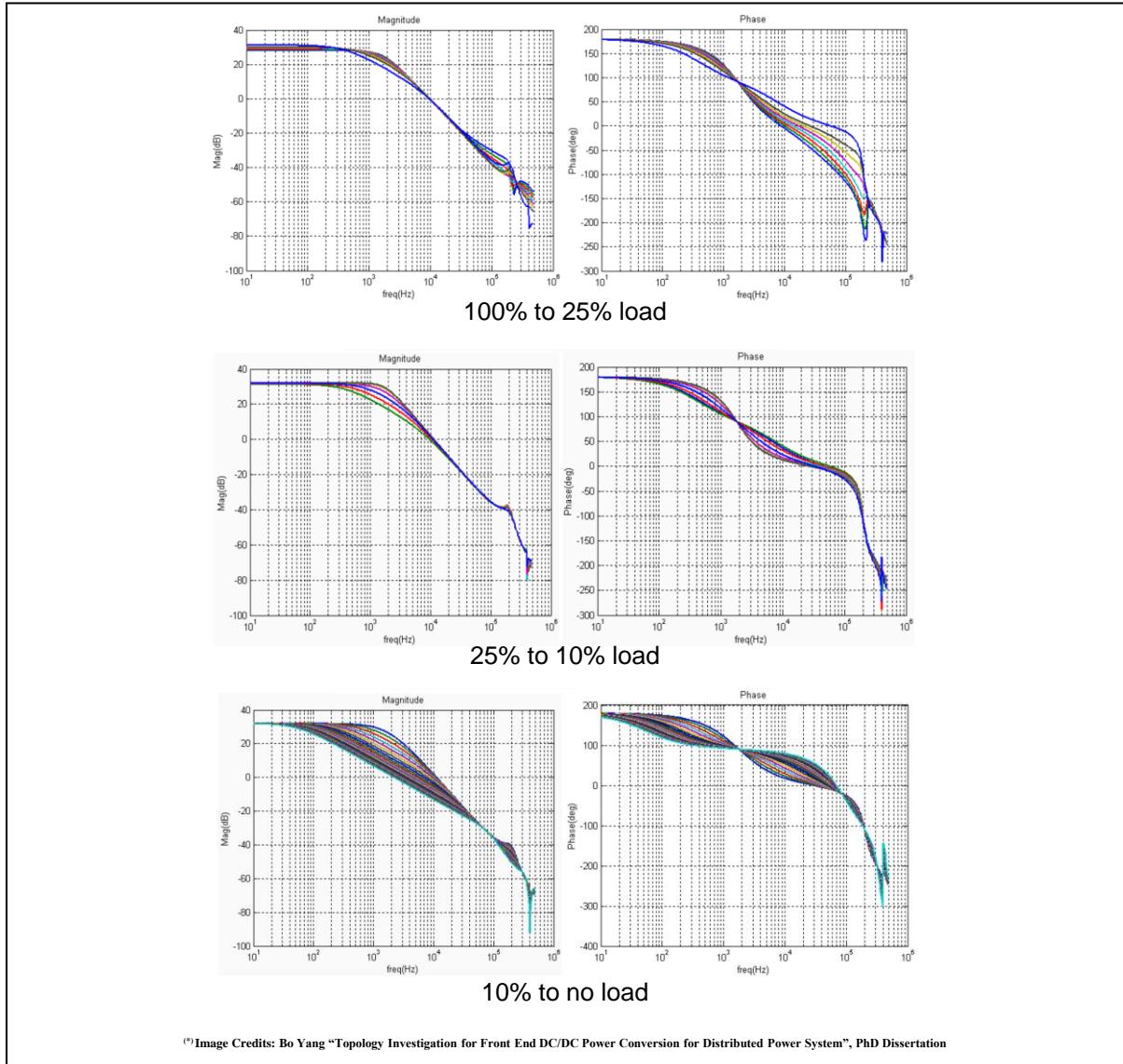
As the switching frequency is reduced below  $f_{R1}$ , the pole that in the above resonance operation had moved to higher frequencies moves back to lower frequencies but stays away from the low frequency region and can be disregarded. The double pole at low frequency is not much affected by the switching frequency reduction. As the switching frequency approaches  $f_{R2}$ , the beat frequency dynamics can be observed again and phase jumps by 180 degrees. This is the feedback reversal observed within the FHA analysis when the switching frequency goes below the value where the gain curves  $|M(x,k,Q)|$  have a maximum.

**Figure 116. Bode plot of  $G_P(j\omega)$  vs. load; above resonance operation ( $f_{sw}/f_{R1} = 1.2$ )<sup>(\*)</sup>.**



<sup>(\*)</sup> Image Credits: Bo Yang "Topology Investigation for Front End DC/DC Power Conversion for Distributed Power System", PhD Dissertation

**Figure 117. Bode plot of  $G_P(j\omega)$  vs. load; below resonance operation ( $f_{sw}/f_{R1} = 0.8$ ) (\*)**.



The RHP zero moves to lower frequencies when the switching frequency is reduced but stays away from the low frequency region, so it is of no practical concern.

Figure 116 shows the Bode plots of  $G_P(j\omega)$  for an exemplary LLC converter operating above resonance at a fixed frequency ( $x = 1.2$ ) for different load conditions ranging from full load to no-load.

When the converter operates above resonance, the small signal characteristics can be divided into two regions. In the first region, where the converter is working in CCM (from full load to approximately 25% load), the characteristics do not change much. In the second region, at light load (from 25% to no load), the converter works in DCM. The low frequency pole moves to lower frequencies and the beat frequency double pole to higher frequencies.

At light load, the LLC resonant converter can be considered as a first order system in a very wide frequency range.

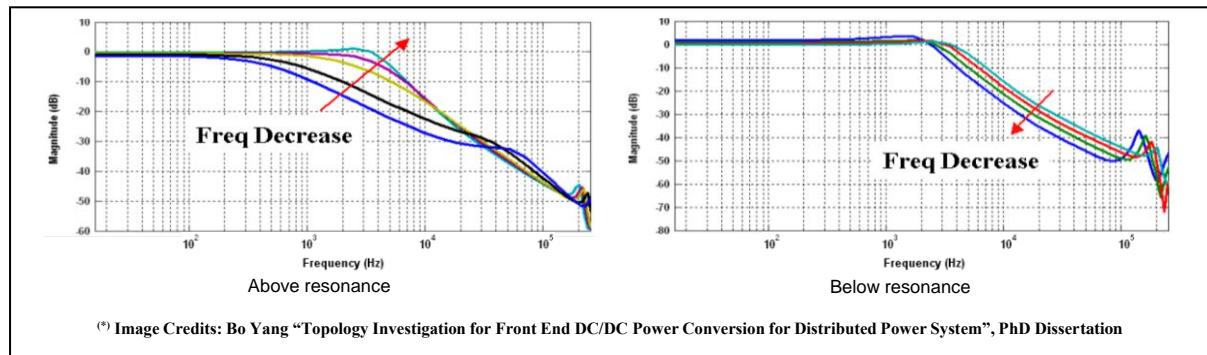
Figure 117 shows the Bode plots of  $G_P(j\omega)$  for an exemplary LLC converter operating below resonance at a fixed frequency ( $x = 0.8$ ) for different load conditions ranging from full load to no-load.

When the converter operates below resonance, the small signal characteristics can be divided into three regions. In the first region, as the load decreases down to about 25%, the Q of the low frequency double pole reduces, the RHP zero moves to higher frequencies and eventually exceeds half the switching frequency.

In the second region, as the load further decreases down to about 10%, the Q of the low frequency double pole increases. In the third region, as the load becomes extremely light and goes to zero, the low frequency double pole splits, one moves to low frequency and one to high frequency.

Coming to the effect of the parameters of the LLC tank on  $G_P(j\omega)$ , the parallel inductance  $L_p$  has an almost negligible impact when the converter operates above resonance. This is quite predictable since  $L_p$  is shunted by the output voltage in most of the operating range.

**Figure 118. Bode plot of audiosusceptibility vs. switching frequency (\*).**



Conversely,  $L_p$  significantly impacts in the below resonance operation: as  $L_p$  increases the dc gain decreases and the RHP zero shifts to lower frequencies.

With a given resonance frequency  $f_{R1}$ , the small-signal characteristics of  $G_2(j\omega)$  are strongly impacted by the characteristic impedance of resonant tank  $Z_0$  given by (70).

With both above and below resonance operation, as  $Z_0$  increases the dc gain increases and the low frequency pole moves to higher frequencies. This suggests that the low frequency pole does not depend on output filter only, as inferable by the small-signal equivalent schematic of figure 108 as well. In the below resonance operation, it is also observed that with larger  $L_s$  values, one low frequency pole also moves to higher frequencies.

The output capacitor impacts only the low frequency pole (and the ESR zero), it has no impact on high frequency poles.

To conclude the description of the small-signal characteristics of the LLC converter with DFC, it is worth to take a look at the audiosusceptibility.

As shown in figure 118 the input-to-output transfer function is close to unity in a large frequency range. This means that the open-loop input ripple rejection is poor and that the reduction of the low-frequency ( $2 \cdot f_{line}$ ) ripple on the output voltage is obtained by closing feedback loop. Therefore, the specification on the residual low-frequency output ripple poses a constraint on the gain of the output-to-control transfer function at  $2 \cdot f_{line}$ .

#### Open-loop step response test

Figure 119 shows the simulation results of the open-loop step responses of the converter specified in Table 12 operated with DFC. Step changes are applied to the control current  $I_C$  such that the dc output current is changed from 10 to 20 A (50% to 100% load) and then back

to 10 A. The output voltage is set at 12 V, the test is repeated at the minimum, typical and maximum input voltage.

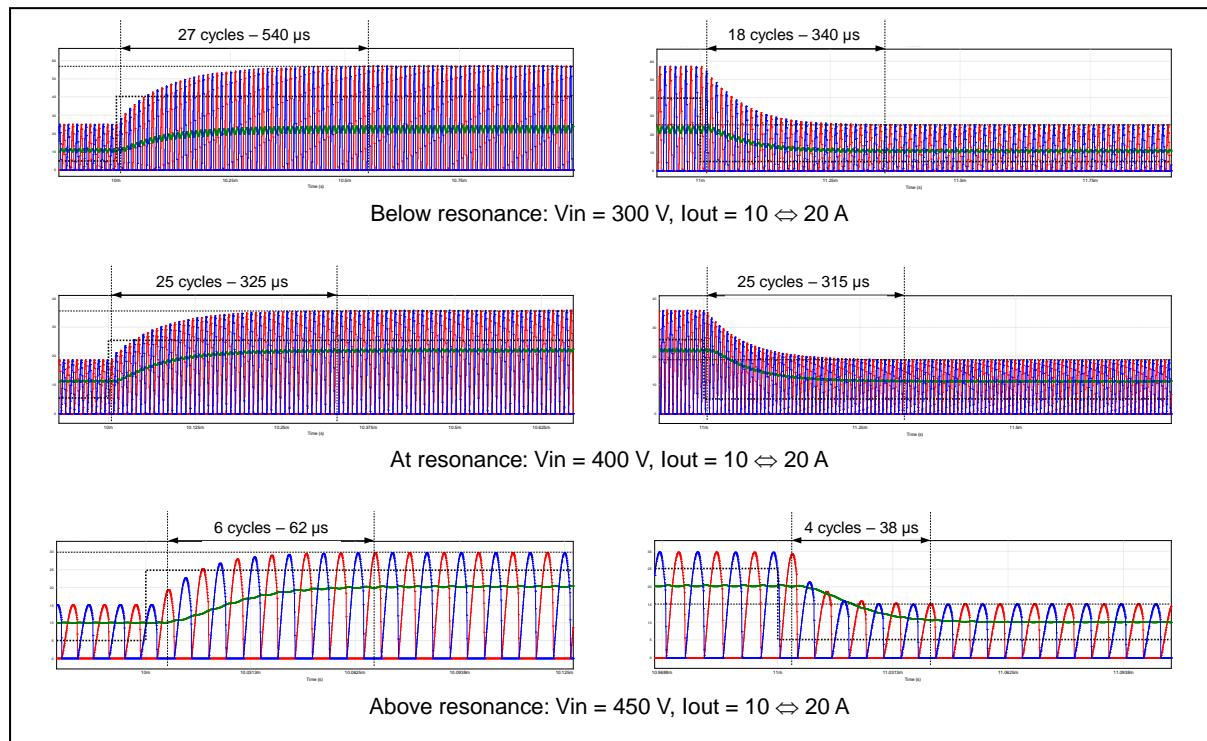
At low input voltage (below-resonance operation) is pretty slow: it takes 27 cycles for the secondary currents to reach steady state in the 10 → 20 A transition and 18 cycles in the opposite transition.

At resonance the response speed is almost the same in the 10 → 20 A transition (25 switching cycles, the time is 40% shorter because the switching frequency is higher), a bit slower in the 20 → 10 A transition but the response is symmetric.

At high input voltage (above resonance operation) the response is much faster (6 cycles in the 10 → 20 A, and only 4 cycles in the 20 → 10 A transition).

The big difference in the response speed between operating below or above resonance and the asymmetric behavior are indicative of the highly variable dynamic behavior of DFC-controlled LLC converters.

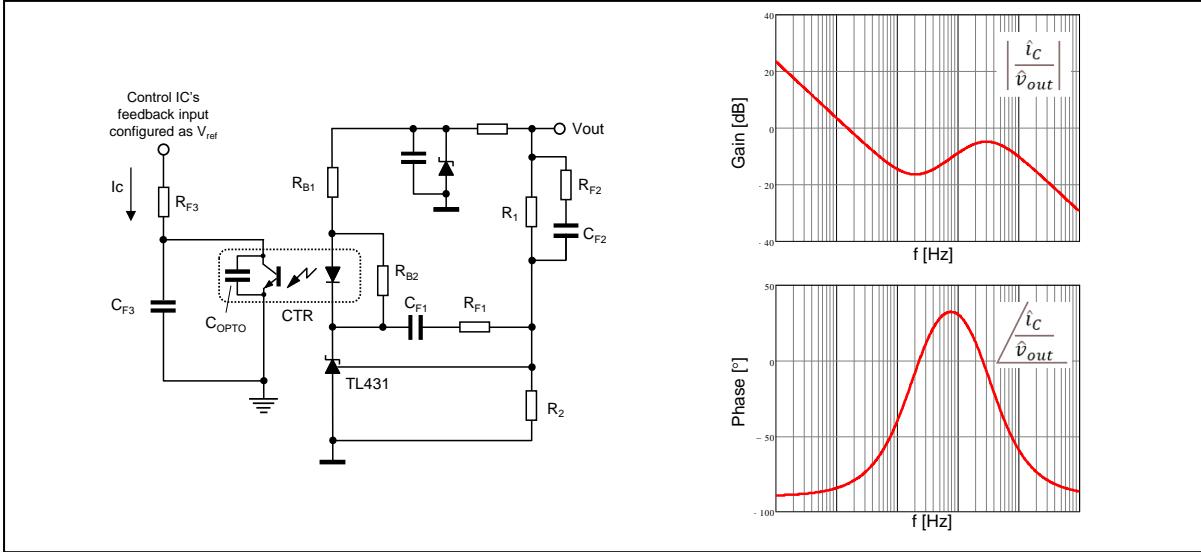
**Figure 119. Open-loop transient response of the converter specified in Table 12 with DFC. Red and blue traces: secondary currents; green trace: output current ( $I_{out}$ ); dotted black line: control signal.**



#### Feedback loop design with DFC

One challenge when tackling the design of the feedback loop (i.e., finding the structure and the parameters of the transfer function  $G_1(j\omega)$  of the compensated error amplifier) is that one must account for operation both above and below resonance, as dictated by a design strategy that aims to provide the converter with optimized steady-state operation. In fact, the different way poles move above and below resonance and the need of having a relatively high low-frequency gain to minimize the  $2 \cdot f_{line}$  ripple on the output voltage make the task all but simple. Sometimes it is very difficult to reach an acceptable compromise.

**Figure 120. TL431-based type-3 error amplifier.**



The feedback loop will be implemented using a popular arrangement with a TL431, which combines the secondary reference voltage with an error amplifier and drives the optocoupler that transfers the control signal to the primary side.

It is assumed that feedback input of the control integrated circuit is configured as a fixed voltage reference  $V_{ref}$  capable of sourcing the control current  $I_C$  that programs the CCO.

The type-3 amplifier (pole at origin plus two poles and two zeroes) shown in figure 120 works in most cases. Its transfer function is:

$$G_1(j\omega) = \frac{\hat{i}_C}{\hat{v}_{out}} = \frac{CTR}{j\omega R_1 R_{B1} C_{F1}} \frac{1+j\omega(R_1+R_{F2})C_{F2}}{1+j\omega R_{F2} C_{F2}} \frac{1+j\omega R_{F1} C_{F1}}{1+j\omega R_{F3}(C_{F3}+C_{OPTO})}. \quad (253)$$

The pole at origin provides good load and line regulation characteristics; the two zeroes are placed at low frequency to compensate the double pole and counteract their phase lag; the poles are placed to compensate ESR zero and provide more attenuation at the switching frequency. Notice that  $C_{OPTO}$ , which models the pole introduced by the optocoupler, limits the maximum attainable frequency of the second pole.

It is possible to get rid of  $C_{OPTO}$ , so that the pole is associated to  $R_{F3}$   $C_{F3}$  only, with appropriate external circuits. Of course,  $C_{OPTO}$  will still there because it is inherent in the physical structure of the phototransistor but does not come into play.

To do so, the phototransistor must work with a constant (or nearly so) collector-emitter voltage: in this way  $C_{OPTO}$  is dynamically shunted and will not affect the small-signal behavior. Figure 121 shows a couple of examples of these circuits.

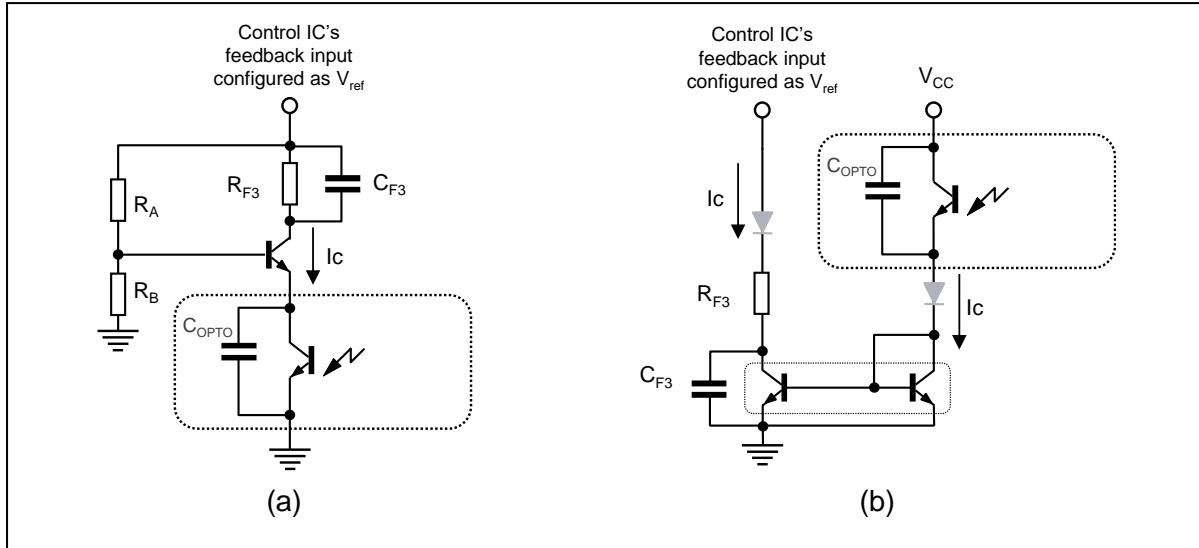
In circuit (a) the phototransistor is cascaded by an NPN BJT whose base is at an essentially fixed voltage  $V_{ref} R_B / (R_A + R_B)$  so that its emitter is one  $V_{be}$  below. In this way, when the control current  $I_C$  changes, the collector-emitter voltage of the phototransistor remains essentially constant as intended, making  $C_{OPTO}$  essentially transparent.

In circuit (b) the phototransistor's collector is connected to a fixed voltage ( $V_{CC}$ ) and its emitter drives a current mirror made with a pair of NPN BJTs, so that the collector-emitter voltage of the phototransistor is essentially constant as intended. BJT pairs with matched characteristics are commonly available in a single low-cost package. Diodes can be added to clamp current mirror's output in case of overdrive and avoid saturation.

As a conclusion, though DFC is the most straightforward control methodology and lends itself to a simple control implementation, there are significant drawbacks. Specifically:

- High sensitivity to input voltage and poor open-loop input ripple rejection
- The design of a compensator that closes the control loop achieving adequate stability margin and input ripple rejection, as well as acceptable load transient response under all the specified operating conditions is not easy, sometimes extremely difficult.
- The control variable ( $I_C$ ) is weakly related to load conditions and is sensitive to the tolerance of the components in the tank circuit, so it cannot be used as a load monitor to establish burst-mode operation or detect overload. A dedicated circuitry is required.

**Figure 121. Secondary circuit arrangements to take  $C_{OPTO}$  out from the feedback loop.**



# Chapter 3

## Time-shift control (TSC)

The so-called time-shift control (TSC) [50] has been developed with the aim of alleviating some of the issues of DFC. As will be shown hereinafter, the LLC converter is turned into a low-Q second order system that in many cases behaves like a first-order one, with a single dominant pole plus the zero due to the ESR of the output capacitor. The compensator design is thereby considerably simplified, and it is much easier to achieve a large open-loop bandwidth with adequate phase margin, having a high gain at twice the line frequency as well. Simply said, the load transient response can be faster and the input voltage ripple rejection higher.

The TSC method, however, does not solve other issues of DFC. The dependence of the control variable on the input voltage remains essentially the same as with DFC. Both DFC and TSC are not robust against parameter variations in the tank circuit: their tolerance shifts the closed-loop operating range of the control variable, and any limitation imposed on it must account for this extended range due to this shift.

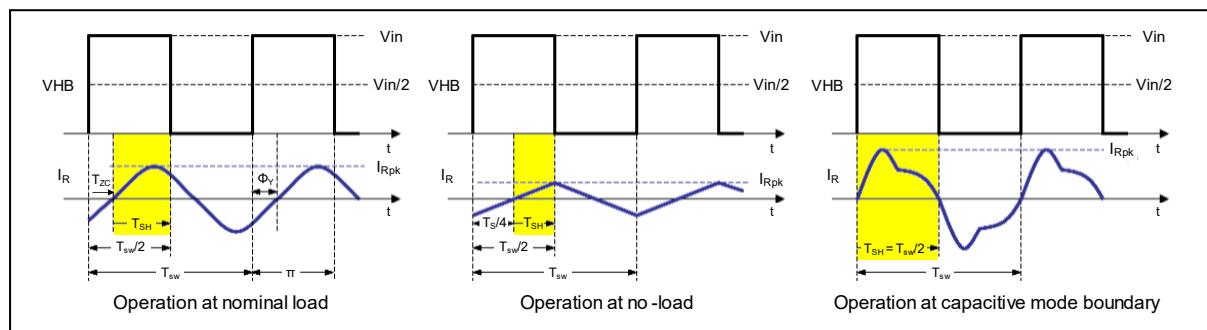
### *Concept of Time-shift*

TSC consists in controlling the amount of time  $T_{SH}$  from a zero-crossing of the tank current to the next switching of the half (or full) bridge, as shown in figure 122 by the time interval highlighted in yellow.

Notice that this can be regarded as controlling the time between the zero-crossing of the tank current and the zero-crossing of the first harmonic of the applied square-wave voltage. Also notice that, since the resonant tank current must lag the applied square-wave voltage to achieve ZVS, the voltage zero-crossing commanded at the end of  $T_{SH}$  must have the opposite direction compared to the current zero-crossing that initiated  $T_{SH}$ . In figure 122, it is possible to see that a negative-going zero-crossing of the applied voltage is commanded after a positive-going zero-crossing of the tank current and vice versa.

It is always  $T_{ZC} + T_{SH} = T_{sw}/2$  and  $T_{ZC}$  ranges between zero at the capacitive-mode boundary, when current and voltage are in phase, and  $T_{sw}/4$  under no-load conditions, when current and voltage are in quadrature. Therefore, in principle, the time-shift  $T_{SH}$  imposed by the control circuit may vary between a minimum of  $T_{swmin}/4$  ( $T_{swmin} = 1/f_{max}$ ) under no-load conditions, and a maximum of  $T_{CM}/2$  ( $T_{CM} = 1/f_{CM}$ ) at the boundary with capacitive-mode operation.

**Figure 122. Concept of time-shift and its range.**



In practice, since adequate safety distance from capacitive-mode operation is normally required, in a converter that operates in the frequency range ( $f_{min}, f_{max}$ ) with  $f_{min} > f_{CM}$ , the  $T_{SH}$  range will be:

$$T_{SH} \in \left( \frac{1}{4f_{max}}, \frac{1}{2f_{min}} \right). \quad (254)$$

There is a link between time-shift and the phase-shift of the tank current. With reference to figure 122, “Operation at nominal load”:

$$\Phi_Y = \pi \left( 1 - 2 \frac{T_{SH}}{T_{sw}} \right), \quad (255)$$

### *Control loop structure and stability analysis*

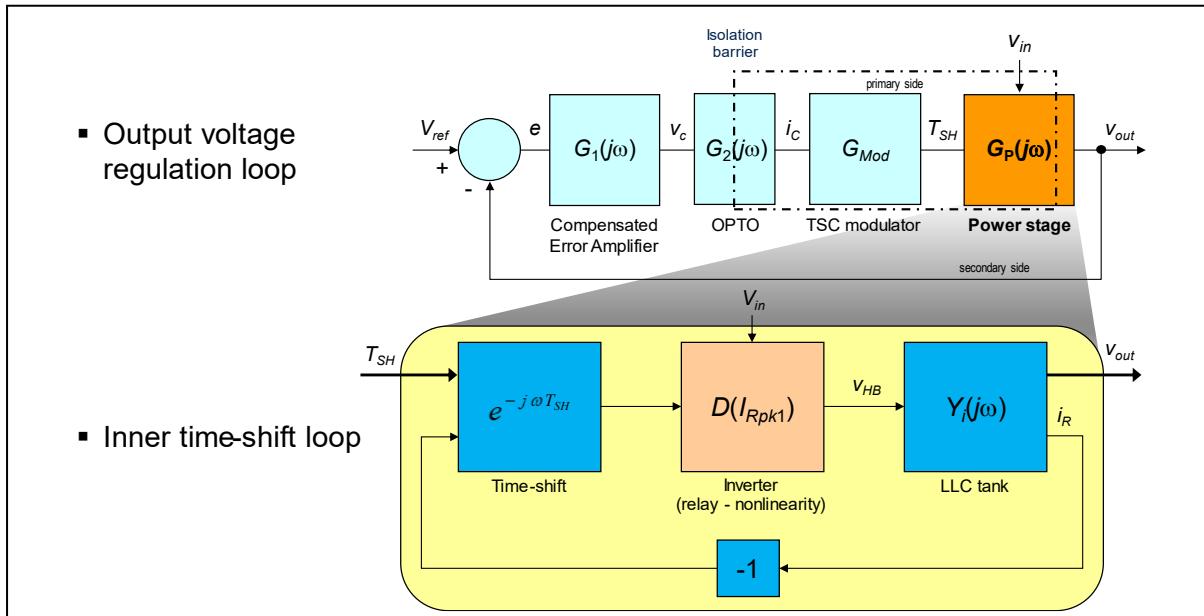
Conceptually, TSC is a two-loop control with an inner loop that controls the time-shift between the tank current and the input voltage zero-crossings, and the outer loop, which regulates the output voltage, that provides the reference for the inner loop. This structure is illustrated in figure 123.

The feedback variable is the tank circuit current  $I_R$ , whose zero-crossings are used as the starting point for the time-shift, while the input quantity to the tank circuit is the applied square-wave voltage  $V_{HB}$ . In the frequency domain, therefore, the tank circuit is represented by its input admittance  $Y_{in}(j\omega) = 1/Z_{in}(j\omega)$ , with  $Z_{in}(j\omega)$  given by (73). The block  $e^{-j\omega T_{SH}}$  represents the time-shift imposed by the control circuit, while the block designated with  $D(I_{Rpk1})$  represents the inverter action of the half (or full) bridge.  $T_{SH}$  is the reference for the loop, while converter’s input voltage  $V_{in}$  represents a disturbance.

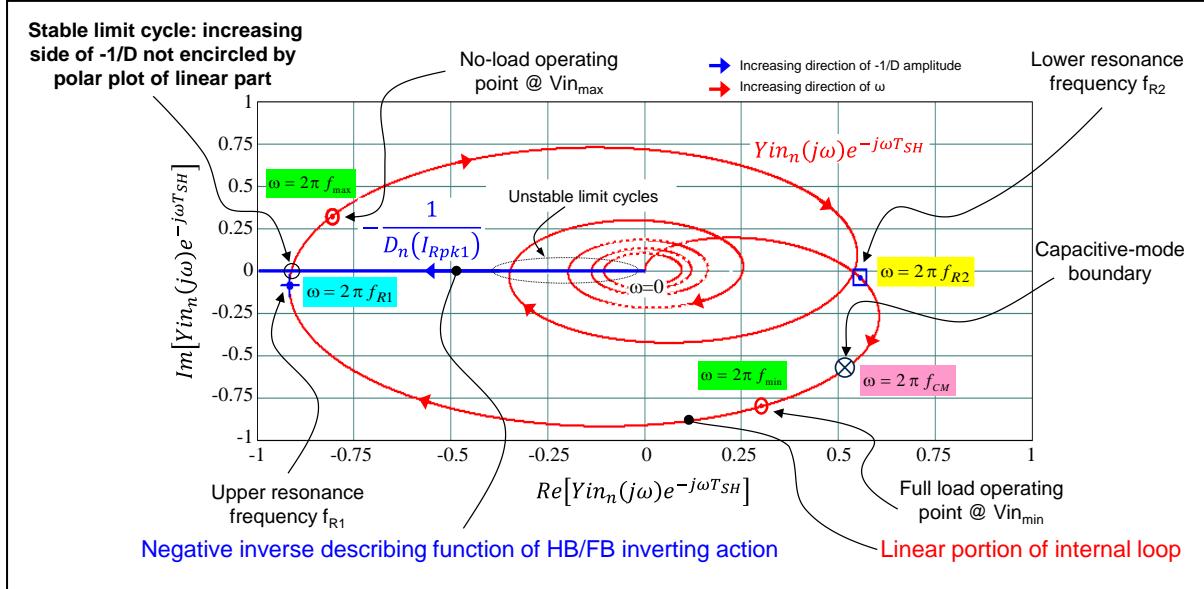
An approximate stability analysis of the inner loop can be carried out with the describing function method [66], which is essentially an extension of the FHA method applicable to a certain class of nonlinear systems, under the assumption that they respond primarily to the first harmonic of their input and negligibly to the higher order harmonics.

With this approach, the non-linear part of the system, i.e., the inverter action of the half (or full) bridge, is represented in the frequency domain by its describing function  $D(I_{Rpk1})$ , where  $I_{Rpk1}$  is the peak value of the first harmonic of  $I_R$ .

**Figure 123. Two-loop structure of TSC.**



**Figure 124. Polar plot of normalized  $Yin(j\omega) e^{-j\omega T_{SH}}$  and  $-1/D_n(I_{Rpk1})$  locus used to study the oscillations of the inner loop in figure 123.**



In the half bridge the voltage applied to the resonant tank oscillates between  $\pm Vin/2$ , whereas in the full bridge between  $\pm Vin$ , therefore:

$$D(I_{Rpk1}) = \begin{cases} \frac{2 Vin}{\pi I_{Rpk1}} & (\text{HB}) \\ \frac{4 Vin}{\pi I_{Rpk1}} & (\text{FB}) \end{cases}. \quad (256)$$

The theory of the describing function method states that the intersection points of the locus of the negative inverse of the describing function (256),  $-1/D(I_{Rpk1})$ , and the polar plot of the transfer function of the linear blocks ( $Yin(j\omega) e^{-j\omega T_{SH}}$  in our case) define a limit cycle. In other words, if these intersections exist the system can oscillate and, if the associated limit cycle is stable, the values of  $I_{Rpk1}$  and of the angular frequency  $\omega$  at the intersection point define the amplitude and the frequency of the oscillation, respectively.

The stability criterion for limit cycles states that if the points of the curve  $-1/D(I_{Rpk1})$  near the intersection in the direction of increasing  $I_{Rpk1}$  are not encircled by the polar plot of the linear part, then the corresponding limit cycle is stable, otherwise it is unstable.

Figure 124 shows the locus of  $-1/D_n(I_{Rpk1})$  and the polar plot of  $Yin_n(j\omega) e^{-j\omega T_{SH}}$  where  $D_n$  and  $Yin_n$  are  $D$  and  $Yin$  normalized to the tank circuit's characteristic admittance  $Y_0 = 1/Z_0 = (Cr/Ls)^{1/2}$ .

The delay term  $e^{-j\omega T_{SH}}$  causes infinite intersections between the two curves and then infinite possible limit cycles; however, considering (254), the only significant intersection is the one falling in the  $\omega$  range  $(2\pi f_{min}, 2\pi f_{max})$  shown in figure 124. According to the above-mentioned stability criterion the corresponding limit cycle is stable.

#### TSC modulator implementation

The TSC modulator can be obtained by simple modifications in the operation of the CCO used with DFC and illustrated in figures 111 and 112 by adding a comparator that senses the tank current  $I_R$  to determine its sign and some logic gates to generate the signals that drive the

oscillator. The inverting input of the comparator is referred to zero, thus the comparator outputs a high logic level when  $I_R$  is positive, a low logic level when  $I_R$  is negative.

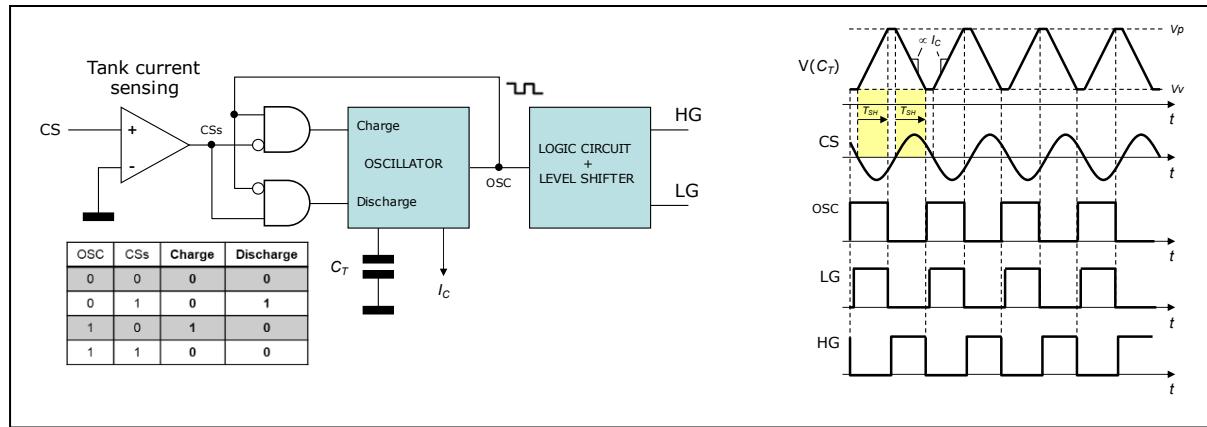
Figure 125 shows on the left-hand side the TSC modulator derived from the triangular carrier CCO shown in figure 111.

The Charge and Discharge commands are generated by the two AND gates according to the truth table shown below them. Whenever OSC and the sign of CS are equal the Charge and Discharge commands are both zero the oscillator is stopped; when OSC and the sign of CS are opposite the oscillator is running, ramping up or down.

Notice that the voltage  $V_{HB}$  applied to the tank circuit is high (positive) from the moment LG goes low to the moment HG goes low, i.e., when OSC is low, and vice versa. Therefore, the timing capacitor  $C_T$  is alternately charged and discharged between two voltage levels ( $V_p$ ,  $V_v$ ) with a current proportional to the control current  $I_C$  only in the time intervals when  $V_{HB}$  and  $I_R$  have equal signs and is not operated when they are opposite. Every time either level is hit, the half/full bridge is toggled, and the oscillator stopped waiting for the tank current to assume the correct sign, as shown in the timing diagram of figure 125, right-hand side. The ramps are therefore synchronized to the zero-crossings of the tank current and generate a trapezoidal waveform. The time the ramps take to go from one level to the other defines the time-shift  $T_{SH}$ .

Also in this case, one main challenge is to make the charge and discharge currents exactly equal to ensure that the same time-shift is commanded in each half switching cycle.

**Figure 125. TSC modulator with triangular carrier; block diagram with truth table (left), key waveforms (right).**



**Figure 126. TSC modulator with sawtooth carrier; block diagram with truth table (left), key waveforms (right).**

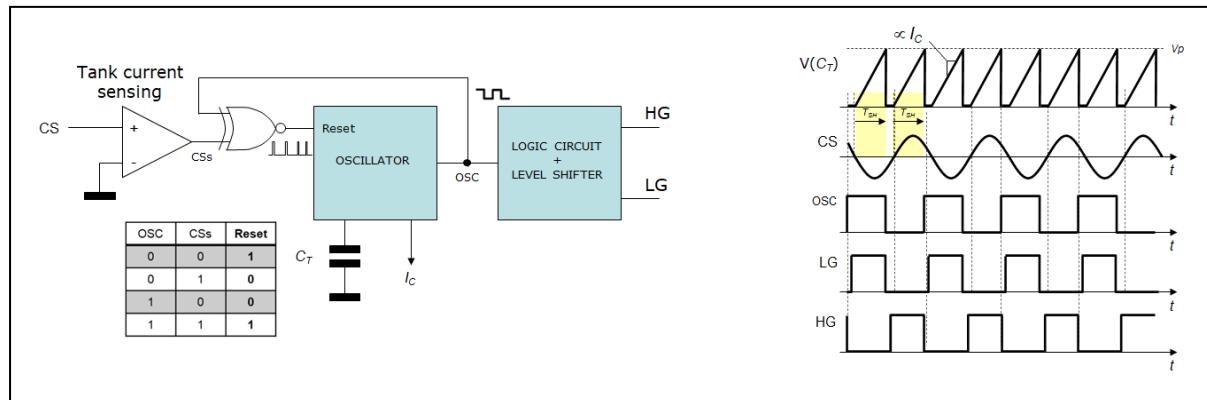


Figure 126 shows on the left-hand side the TSC modulator derived from the sawtooth carrier CCO shown in figure 112. The Reset command is generated by combining in an XNOR gate the output of the comparator and the signal OSC. Whenever OSC and the sign of CS are equal the Reset signal is high, the oscillator is stopped; when OSC and the sign of CS are opposite the oscillator is running.

Also in this case,  $V_{HB}$  and OSC have opposite signs, so the timing capacitor  $C_T$  is charged from zero to a peak level ( $V_p$ ) with a current proportional to the control current  $I_C$  only in the time intervals when  $V_{HB}$  and  $I_R$  have equal signs and is kept at zero when they are opposite. Every time the ramp thus generated hits  $V_p$ , the half/full bridge is toggled,  $C_T$  is quickly reset at zero and remains at zero waiting for  $I_R$  to change sign, as shown in the timing diagram of figure 126, right-hand side. The ramps are therefore synchronized to the zero-crossings of the tank current, generating a sawtooth with non-contiguous triangles. The time the ramps take to go from zero to  $V_p$  defines the time-shift  $T_{SH}$ .

With this implementation the equality of the time-shift commanded in each half switching cycle is ensured; the frequency of the sawtooth carrier is twice the switching frequency; the fast discharge of  $C_T$  is a potential source of noise.

With both implementations the most difficult challenge concerns the zero-crossing comparator: in fact, it must be fast not to affect the control loop significantly (its delay adds up to the commanded  $T_{SH}$ , then it should be  $\ll T_{SH\min}$ ) and with the same response time on positive and negative-going zero-crossings not to introduce asymmetry in the  $T_{SH}$ . For the same reason, it must have a very small input offset. This requires a careful design.

Assuming that the internal delays in the oscillator circuit are negligible compared to the oscillation period, the time-shift-to-control relationship with both implementations is:

$$T_{SH} = C_T \frac{\Delta V_{CT}}{k_T I_C}, \quad (257)$$

where the symbols have the same meaning as for (251).

Notice that with the TSC modulator the excursion of the control signal  $I_C$ , intended as the ratio of the maximum value to the minimum value,  $2f_{max}/f_{min}$ , twice that of the DFC modulator that equals  $f_{max}/f_{min}$ .

Regardless of the specific implementation, being interested in a frequency range much lower than  $f_{sw}/2$ , the modulator gain  $G_{Mod}$  can be simply found by differentiating (257), which yields:

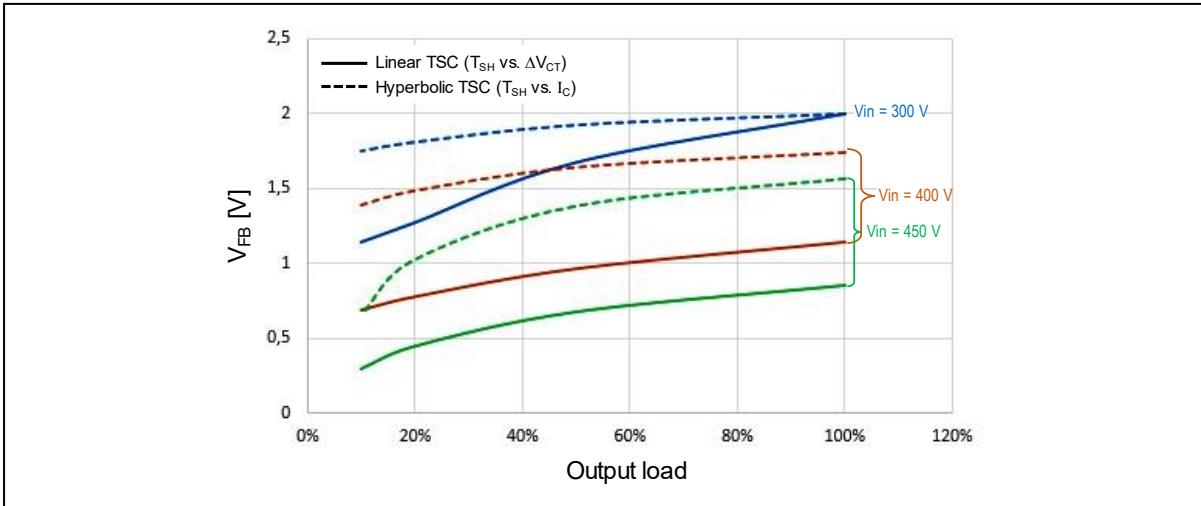
$$G_{Mod} = \frac{\hat{t}_{sh}}{\hat{i}_c} = -\frac{T_{SH}}{I_C}, \quad (258)$$

Equation (257) shows a relationship of inverse proportion (hyperbolic) between  $T_{SH}$  and the control variable  $I_C$ . If one wants a proportional (linear) relationship it is possible to use a fixed current  $I_C$  to charge/discharge  $C_T$  and modulate  $T_{SH}$  by modulating  $\Delta V_{CT}$ . This change in the control variable does not affect the TSC modulator architectures shown in figures 125 and 126 nor their operating principle (of course the circuit-level implementation will be different).

There is no significant difference between the “hyperbolic” and the “linear” TSC modulator as far as the resulting small-signal characteristics and dynamic behavior are concerned, the difference is just in the static  $T_{SH}$  vs.  $I_C$  map that differs from the  $T_{SH}$  vs.  $\Delta V_{CT}$  map, as shown in the diagram of figure 127, though the excursion is  $2f_{max}/f_{min}$  too.

The “linear” TSC modulator lends itself very well to a digital implementation. In fact, TSC is based on counting time, a task that digital machines are very efficient to deal with.

**Figure 127. Hyperbolic vs. linear TSC modulator: time-shift vs. control variable maps.**



The block diagram in figure 128 shows an exemplary implementation of the digital TSC modulator located on the primary side. Because of isolation requirements, it is possible to assume that the part of the feedback loop on the secondary side is essentially analog, with the TL431 and the relevant frequency compensation network.

The error signal generated on the secondary side is transferred to the primary side via an optocoupler ( $V_E$ ) and provided to the digital controller where it is sampled by an A/D converter. A lookup table then converts the output of the A/D converter into a digitized time value  $T_{SH}$  following a linear control law:

$$T_{SH} = p V_E + q , \quad (259)$$

where  $p$  and  $q$  are such that the required  $T_{SH}$  regulation range (254) resulting from converter's large signal characterization is entirely covered by the  $V_E$  range. The  $T_{SH}$  value is handled by the MCU that implements the TSC algorithm: The PWM generator, driven by the MCU, outputs the driving signals for the switches of the half/full bridge.

Figure 129 depicts a simplified control algorithm (protections are excluded) modeled with a state machine, showing both the state diagram and the corresponding time diagram. The digital timers are represented by analog ramps for clarity.

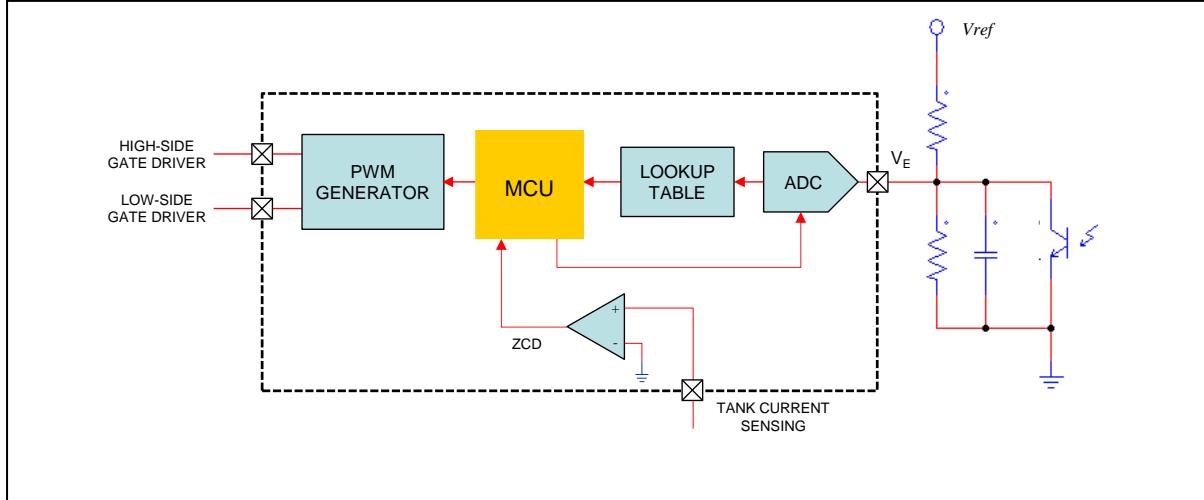
After Power-on Reset (POR) the state machine is in its initial idle state, with both outputs (Out1, Out2) low. As the clock is enabled, the timer counter is reset at zero, and the state transitions to S0, which represents the dead-time before turning on the low-side switch LG, where a register is loaded with the value of the dead-time  $T_D$ .

As the timer counter reaches  $T_D$  the state transitions from S0 to S1. In this state Out1 (LG) goes high, turning on the low-side switch, and the system waits for the positive-to-negative zero-crossing of the tank current.

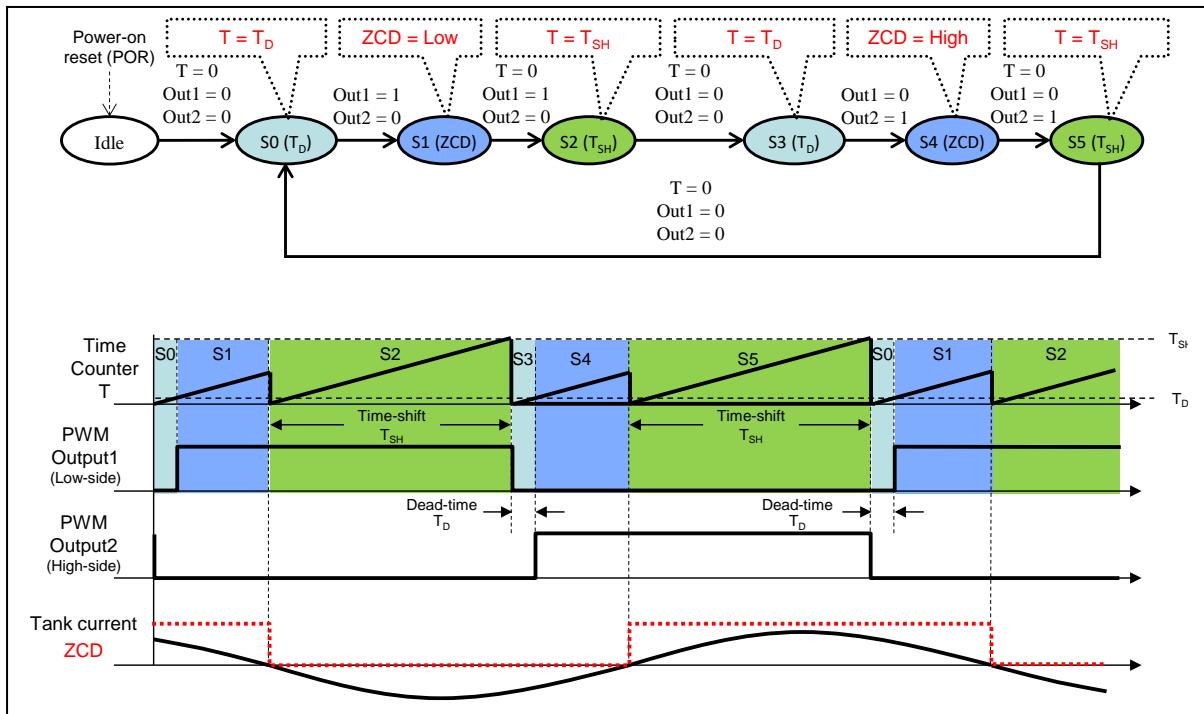
As this event is detected by the ZCD signal going low, the state S2 is entered. During this transition the outputs are unchanged, but the timer counter is reset at zero to be ready to count the time-shift  $T_{SH}$  programmed by the control loop and stored in a register.

As the timer counter reaches the programmed  $T_{SH}$ , the state transitions from S2 to S3. This transition causes Out1 to go low so that the low-side switch is turned off, and the timer counter to be reset at zero. This state corresponds to the dead-time between the turn-off of the low-side switch and the turn-on of the high-side switch.

**Figure 128. Feedback loop: primary side digital part.**



**Figure 129. Digital implementation of the TSC algorithm.**



As the timer counter reaches  $T_D$  the state transitions from S3 to S4. In this state Out2 (HG) goes high, turning on the high-side switch, and the system waits for the negative-to-positive zero-crossing of the tank current.

As this event is detected by the ZCD signal going high, the state S5 is entered. Going from S4 to S5 the outputs are unchanged, and the timer counter is reset at zero to count the time-shift  $T_{SH}$  programmed by the control loop and stored in the register.

As the timer counter reaches the programmed  $T_{SH}$ , Out2 goes low so that the high-side switch is turned off, the timer counter is reset at zero, the state transitions back to S0 and the cycle restarts.

It is worth noticing that the low-side switch is activated first as discussed in Part III, Chapter 3.

### *Small-signal characteristics of $G_P(j\omega)$*

Theoretically,  $G_P(j\omega)$  can be expressed as follows:

$$G_P(j\omega) = \frac{\hat{v}_{out}}{\hat{t}_{sh}} = \frac{\hat{v}_{out}}{\hat{f}} \frac{\hat{f}}{\hat{\varphi}} \frac{\hat{\varphi}}{\hat{t}_{sh}} , \quad (260)$$

The first factor on the right-hand side of (260) is the  $G_P(j\omega)$  with DFC. The term  $\varphi$  in the other two factors is the phase-shift between the tank current and the square-wave voltage  $V_{HB}$ . In the spirit of the FHA approach, already used in the previous section to study the stability of the inner loop,  $\varphi$  is the phase of the input impedance  $Zin(j\omega)$ ,  $\arg[Zin(j\omega)]$ , of the tank circuit (74). The second factor is, therefore, the reciprocal of the derivative of  $\arg[Zin(j\omega)]$  with respect to frequency.

The third factor relates phase-shift to time-shift. It can be calculated from (255):

$$\frac{\hat{\varphi}}{\hat{t}_{sh}} = -\frac{2\pi}{T_{sw}} = -\omega_{sw} , \quad (261)$$

The analytical expression of (260) is by far too complex to be of any practical usage. Also in this case, it is considered more informative to examine its fundamental characteristics with an empirical approach based on simulations in the frequency domain.

The results of these simulations are shown in figure 130. The Bode plots include the TSC modulator gain too, which provides just a fixed gain. The explored frequency range extends from 10 Hz to half the resonance frequency  $f_{R1}$ . The ESR zero is located at about 9 kHz.

No gain peaking nor phase-flip is observed, which prompts the existence of poles located close to the real axis, if not real poles. Looking at the phase plots, the worst-case overall phase change occurs at 100% load with the minimum input voltage ( $Vin = 300$  V), where it exceeds 180° close to  $f_{R1}/2$  despite the phase boost by the ESR zero.

It is possible to notice that the -3 dB cutoff frequency is close to the ESR zero frequency and that the phase-shift is slightly less than 50°, which is compatible with the phase shift of two poles at a lower frequency plus the ESR zero. This is confirmed by the gain plot: at frequencies lower than the ESR zero the gain rolls off at a slope included between -1 and -2 because of the effect of the zero and then seems to flatten out. The phase-shift instead tends to increase.

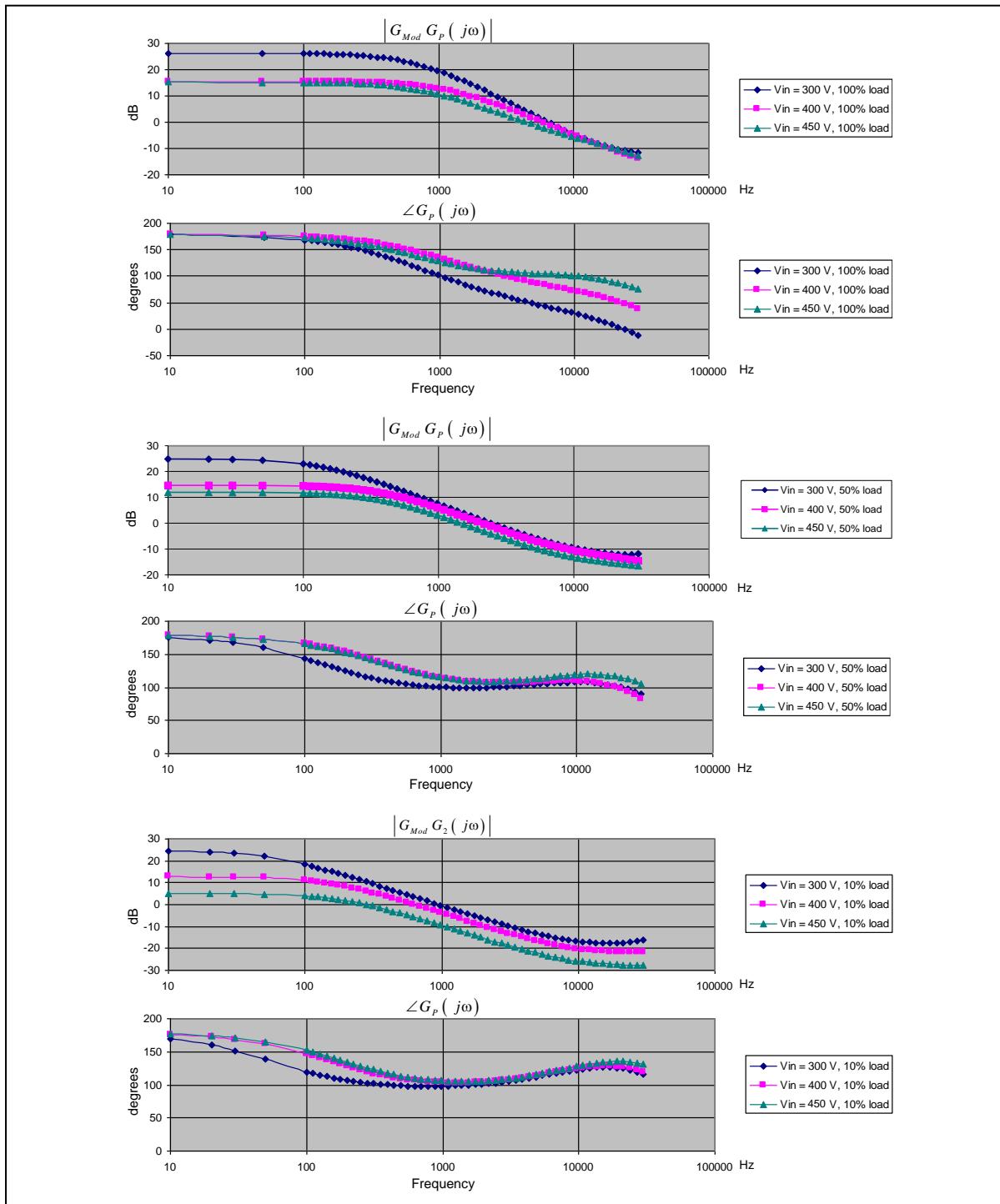
The most probable explanation of this behavior is the existence of at least an RHP zero located at frequencies around  $f_{R1}$ , whose effect starts arising.

Still at 100% load at higher input voltages both the phase-shift and the gain roll off are smaller, which suggests that one of the two low-frequency poles has moved to higher frequencies. Therefore, if there was a pair complex conjugate poles at the minimum voltage, a higher input voltage must have caused them to split in two real poles, one quite stably located at low frequency and the other moving towards higher frequencies.

At 50% load and 10% load, the maximum phase-shift slightly exceeds 100° and the gain slope is almost exactly -1, which confirms the same behavior: a pole must have migrated to higher frequencies leaving only one pole in the low-frequency region. In these conditions, we have a first-order system at least up to the frequency of the ESR zero. The RHP zero(es) is/are still there, apparently in a quite stable position in the vicinity of  $f_{R1}$ .

A dominant pole approximation is then acceptable. Additionally, designing the compensator to ensure closed-loop stability at full load and minimum input voltage ensures closed-loop stability everywhere.

**Figure 130. Frequency-domain simulations of converter specified in Table 12 at 100%, 50% and 10% load with  $V_{in} = 300$  V, 400 V, 450 V.**

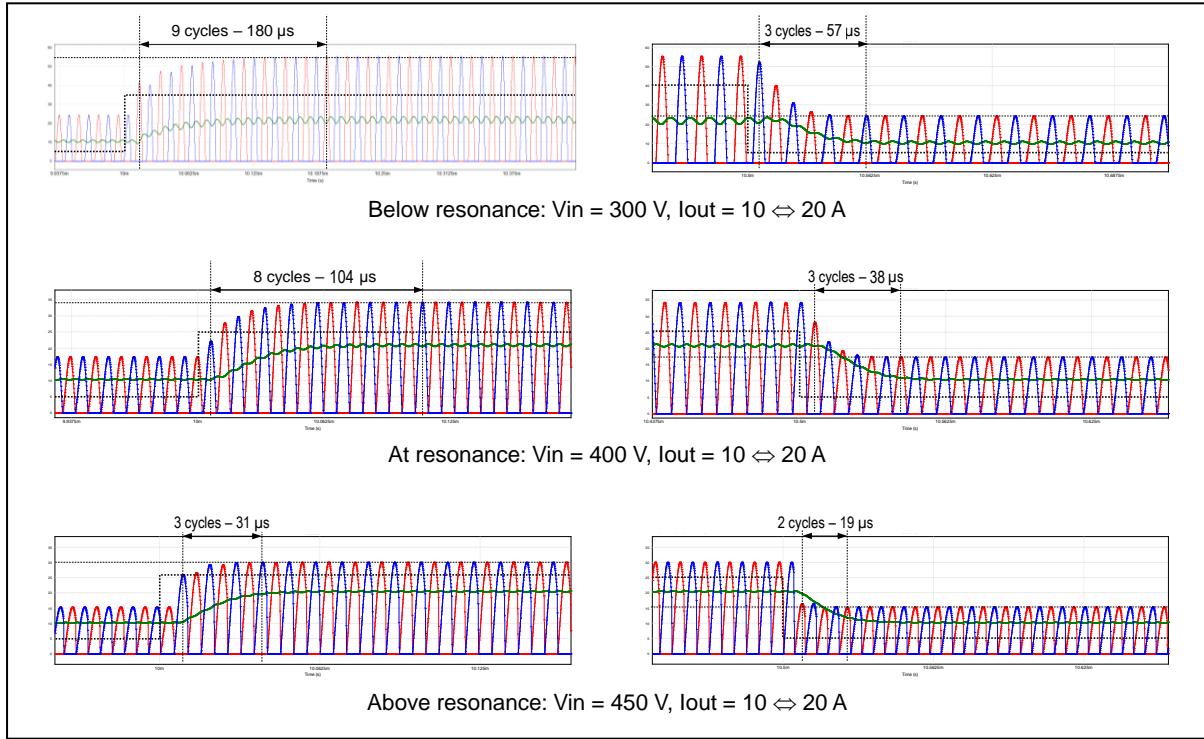


#### Open-loop step response test

Figure 131 shows the simulation results of the open-loop step response of the converter specified in Table 12 operated with TSC.

The same procedure used for the DFC method is used here: step changes are applied to the control current  $I_C$  such that the dc output current is changed from 10 to 20 A (50% to 100% load) and then back to 10 A. The output voltage is set at 12 V, the test is repeated at the minimum, typical and maximum input voltage.

**Figure 131. Open-loop transient response of converter specified in Table 12 with TSC.**  
**Red and blue traces: secondary currents; green trace: output current ( $I_{out}$ ); dotted black line: control signal**



Also with TSC, at low input voltage (below-resonance operation) the system responds more slowly compared to the other conditions, even though the response is much faster than DFC: it takes 9 cycles for the secondary currents to reach steady state in the  $10 \rightarrow 20$  A transition and only 3 cycles in the opposite transition.

At resonance the response speed is almost the same in the  $10 \rightarrow 20$  A transition (8 switching cycles), and 3 cycles in the  $20 \rightarrow 10$  A transition.

At high input voltage (above resonance operation) the response is even faster: 3 cycles in the  $10 \rightarrow 20$  A, and 2 cycles in the  $20 \rightarrow 10$  A transition, close to the optimum speed of the *Optimal Trajectory Control* method [8], [65] that responds in just one switching cycle.

Table 13 compares the results of the open-loop response test for TSC and DSC. DSC speed (defined as the reciprocal of the number of cycles) is used as the baseline. With this definition, the numbers state how much faster the response with TSC is compared to that with DFC.

**Table 13. Comparison of open-loop test response speed for TSC and DFC**

$V_{in}$	#Cycle ratio (DFC / TSC)	
	$10 \text{ A} \Rightarrow 20 \text{ A}$	$20 \text{ A} \Rightarrow 10 \text{ A}$
300	3	6
400	3.13	8.33
450	2	2

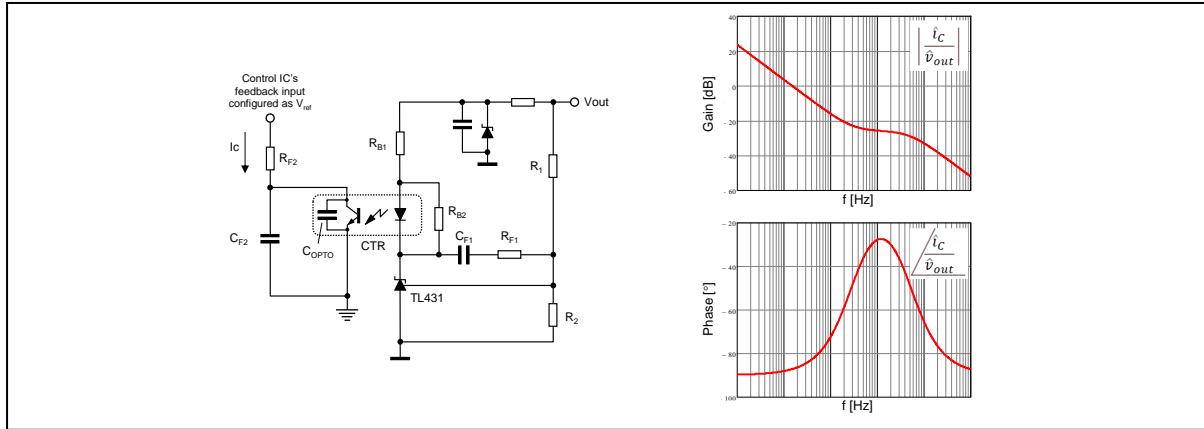
### Feedback loop design with TSC

The task of designing a compensator for a TSC-based LLC converter is significantly facilitated by its favorable small-signal characteristics. Not only will it be possible to achieve better closed-loop dynamic behavior, but this will be possible with a simpler configuration of the frequency compensation network.

The feedback loop will be implemented using a type-2 error amplifier (pole at the origin plus one pole and one zero) with the already familiar arrangement with a TL431 plus optocoupler, shown in figure 132.

Also in this case, the feedback input of the control integrated circuit is configured as a fixed voltage reference  $V_{ref}$  able to source the control current  $I_c$  that drives the TSC modulator.

**Figure 132. TL431-based type-2 error amplifier.**



The transfer function of the type-2 amplifier in figure 132 is:

$$G_1(j\omega) = \frac{i_c}{v_{out}} = \frac{CTR}{j\omega R_1 R_{B1} C_{F1}} \frac{1 + j\omega R_{F1} C_{F1}}{1 + j\omega R_{F2} (C_{F2} + C_{OPTO})}. \quad (262)$$

The pole at origin provides good load and line regulation characteristics; the zero is placed at low frequency to compensate the low frequency poles and counteract their phase lag; the pole is placed at high frequency to provide more attenuation at the switching frequency.

In this case  $C_{OPTO}$ , which limits the maximum attainable frequency of the second pole, may be even more annoying than with DFC. In fact, in view of the characteristics of TSC, one might easily design the loop for a higher bandwidth. The proposed solutions shown in figure 121 to get rid of the effects of  $C_{OPTO}$  are applicable to TSC as well.

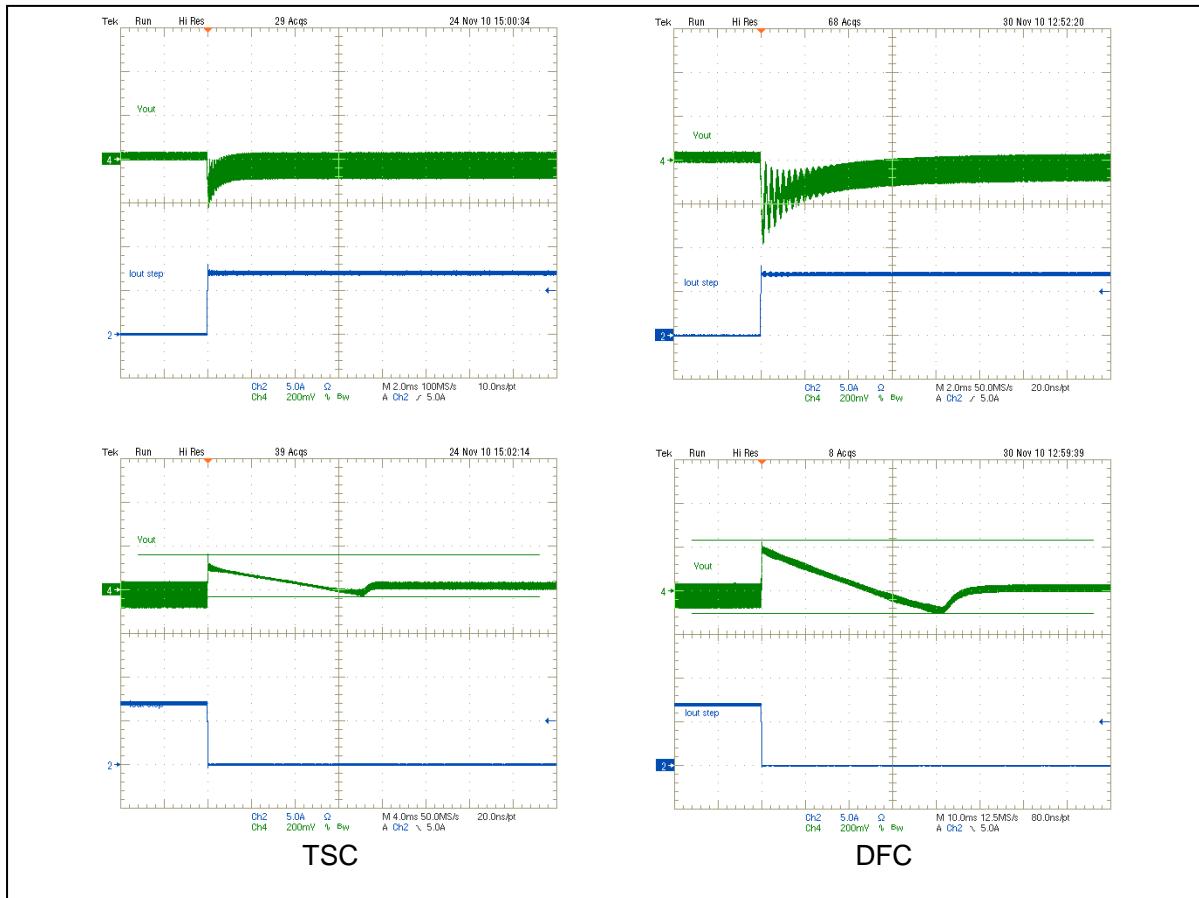
With TSC it is also possible to achieve an open-loop gain at  $2 \cdot f_{line}$  much higher than what DSC permits, with a consequent reduction of the residual ripple on the output voltage.

The scope pictures in figures 133 and 134 allow a comparison of the different performance of DFC and TSC in a real system, a 170 W (24 V, 7A) LLC half bridge converter powered from a PFC pre-regulator in a flat screen TV SMPS.

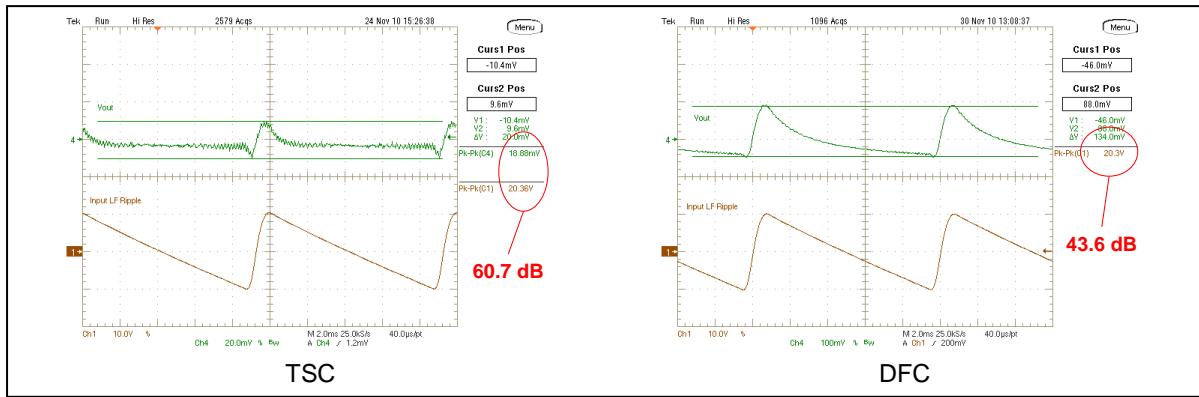
The comparison is done on the same converter operated with the two methods and optimizing the frequency compensation network for the maximum response speed with each method, using a type-2 amplifier with TSC and a type-3 amplifier with DFC.

In the load transients shown in figure 133, the load is changed from 7 A to 0 and vice versa. It is possible to notice that with TSC the undershoot and the overshoot are significantly lower (about 50% smaller) and how faster the settling time is in the 0 to 7 A transient (about 4 times).

**Figure 133. TSC-DFC load transient response comparison in a 170 W LLC half bridge.**



**Figure 134. TSC-DFC Input ripple attenuation comparison in a 170 W LLC half bridge.**



In the 7 A to 0 transient the time the output voltage takes to go back to the regulated value does not depend on the control, it is dictated by the discharge of the output capacitor with the residual load (e.g., the feedback network). It is worth noticing that with DFC the discharge ends when the output voltage falls about 100 mV below the regulated value, while with TSC it ends about 50 mV below the regulated value.

On an extreme level, the input ripple rejection test, whose results are shown in the scope pictures of figure 134, has been done powering the LLC converter with a rectified 280 Vac at 50 Hz. In this way the dc level was almost the same as with the PFC front-end but with a larger ripple, also richer in higher order harmonics and then involving the gain at frequencies higher than  $2 \cdot f_{line}$  that is presumably lower.

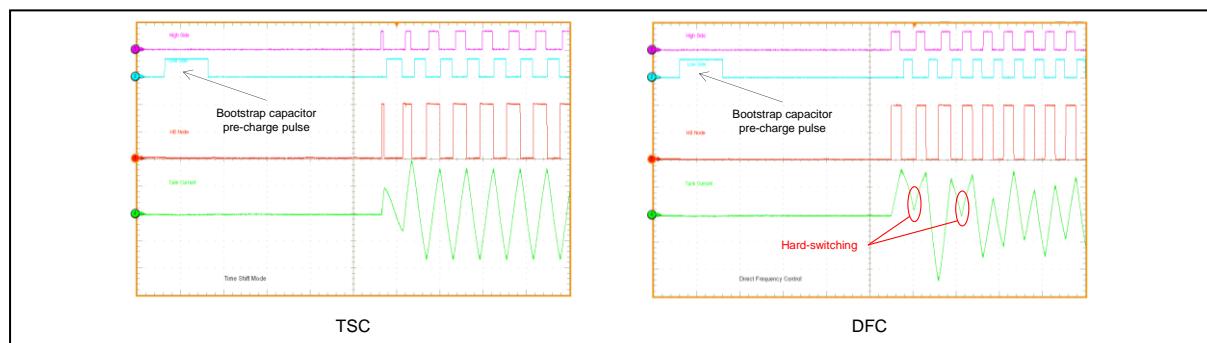
With around 20 V pk-pk of input ripple, the residual low-frequency ripple at the output goes from more than 130 mV pk-pk with DFC to less than 20 mV pk-pk with TSC, gaining more than 16 dB of attenuation. The resulting attenuation level (60.7 dB) is comparable to that observable in PWM-controlled converters with peak current mode control. Since the open-loop input ripple rejection ratio is the same for TSC and DFC this improvement is all due the higher low-frequency gain.

### Converter start-up with TSC

TSC has an additional merit: unlike DFC, TSC inherently prevents the flux doubling issue at start-up, discussed in Part III Chapter 3, that affects the half bridge version. It naturally performs the suggested corrective action that is part of the safe-start procedure [25], i.e., synchronizing  $V_{HB}$  to the zero-crossings of the tank current.

The scope pictures in figure 135 show the start-up of the 170W LLC half-bridge converter for flat screen TV SMPS with both methods.

**Figure 135. Half bridge converter's start-up: TSC prevents flux doubling of DFC.**



### Summary and conclusions

As a conclusion, TSC provides several benefits, specifically:

- TSC makes LLC converter behave almost as a first-order system
  - Frequency compensation is much easier, response to perturbations is non-oscillatory, large bandwidth loop designs are possible
- TSC improves load transient response
  - Overshoots and undershoots are nearly halved, settling time is 3-4 times shorter
- TSC improves closed-loop input ripple rejection
  - 100/120 Hz gain can be increased considerably, the ripple rejection ratio may increase by more than 15 dB
- TSC prevents hard switching at start-up
  - Converter reliability is improved

There are, however, also some drawbacks. Specifically:

- Like with DFC, with TSC the control variable is strongly related to the input voltage and weakly related to load conditions, and is also sensitive to the tolerance of components in the tank circuit
  - Additional means need to be considered to limit the maximum current during overloads or establish burst-mode operation at light load.
- Open-loop audio susceptibility of TSC and DFC are essentially identical

- The improvement of the input ripple rejection ratio is due only to a higher low-frequency gain of the compensator
- Zero-current detection may be sensitive to noise
- The zero-current comparator must have very low input offset and equally fast response to negative-going and positive going zero-crossings.
  - If not, duty cycle of generated square wave may significantly deviate from 50%

# Chapter 4

## Charge-mode control (CMC)

Charge-mode control (CMC), initially developed for PWM-controlled converters, was first proposed in resonant converters in [52]. To author's knowledge, its first significant industrial usage, most probably in LCC resonant converters, dates back to the years between the end of the past century and the beginning of 2000s [12]. Through the years, several variants of CMC have been developed and today the latest control ICs developed by many semiconductor makers use CMC in one of its many flavors.

As suggested by its name, CMC controls the per-cycle electric charge of the switch current of a converter. In most cases, which include resonant converters, the controlled switch current is very close to the input current, so it is not entirely wrong to say that CMC control the per-cycle electric charge that a converter draws from the input source.

We should remind that electric current is the rate of flow of electric charge: when current flows for a certain time in a switch, a certain amount of electric charge has gone through that switch:  $\text{charge} = \text{current} \times \text{time}$ . Therefore, CMC requires a form of integration of the switch current.

CMC is one of the many existing ways to use current in a converter as part of its feedback control mechanism to achieve better dynamic response. Peak current mode control, which one can find quite ubiquitously in PWM-controlled converters, is perhaps the simplest and the most common one. Unfortunately, there is a fundamental roadblock to using peak current mode control in resonant converters: unlike in PWM-controlled converters, the active switches do not always turn off when their current reaches its peak value. We have seen this clearly, for example, in the LLC converter operated at resonance.

However, if current is not always monotonic in a switch conduction cycle, as long as current does not change sign its integral always increases monotonically and can be used in place of the instantaneous current to determine the turn-off of the switch.

In the following discussion we will see that there are many different possible implementations of CMC in resonant converters. No matter how it is implemented, CMC results in an essentially single pole dynamic system. Other singularities exist but in a frequency range that is not of practical interest for the design of a compensator.

As a result, CMC boasts excellent dynamic performance across the entire range of operating conditions and like TSC, makes the compensator design and fine tuning much easier. Additionally, since the amount of electric charge provided in a given time depends on the input voltage, if the per-cycle charge is fixed, there will be an automatic correction of the switching frequency. CMC, therefore, offers an input ripple rejection ratio better than that of DFC and TSC. Finally, being based on integration, it is inherently little noise sensitive.

In addition to its excellent properties, a couple of shortcomings of CMC must be mentioned. Firstly, CMC suffers from the subharmonic oscillation issue like peak current mode. The trigger conditions are different (to the author's knowledge those for resonant converters are not even documented): with CMC it appears at light load. The cure, however, is the same: slope compensation. The side-effect of the cure is also the same, a slight degradation of the dynamic performance.

Secondly, it will be shown that the control signal in the feedback loop is still a function of the switching frequency. For a set LLC tank design and set operating conditions, the switching frequency is affected by the tolerance of its parameters  $L_s$ ,  $L_p$  and  $C_r$ , and so does the control signal. Therefore, what is a common practice in PWM-controlled converters, i.e., the use of the control signal as a load monitor to establish burst-mode operation at light load or to detect overload conditions, is still lacking repeatability.

#### *Charge-mode control fundamentals*

With reference to the integration process, the CMC methodologies for resonant converters can be divided into two groups: those that use the natural integration of the resonant current operated by the resonant capacitor [12], [53]-[56] and those where integration is done by processing the signal representative of the resonant current [57]-[58]. The second group can be further split in two subgroups: with resettable integrator and with continuous integration. This scenario is illustrated in figure 136.

##### Natural integration by resonant capacitor

The principle which the CMC using the integration of the tank current operated by the resonant capacitor is based on has been already described in Part II, Chapter 5 and here briefly reminded for reader's convenience.

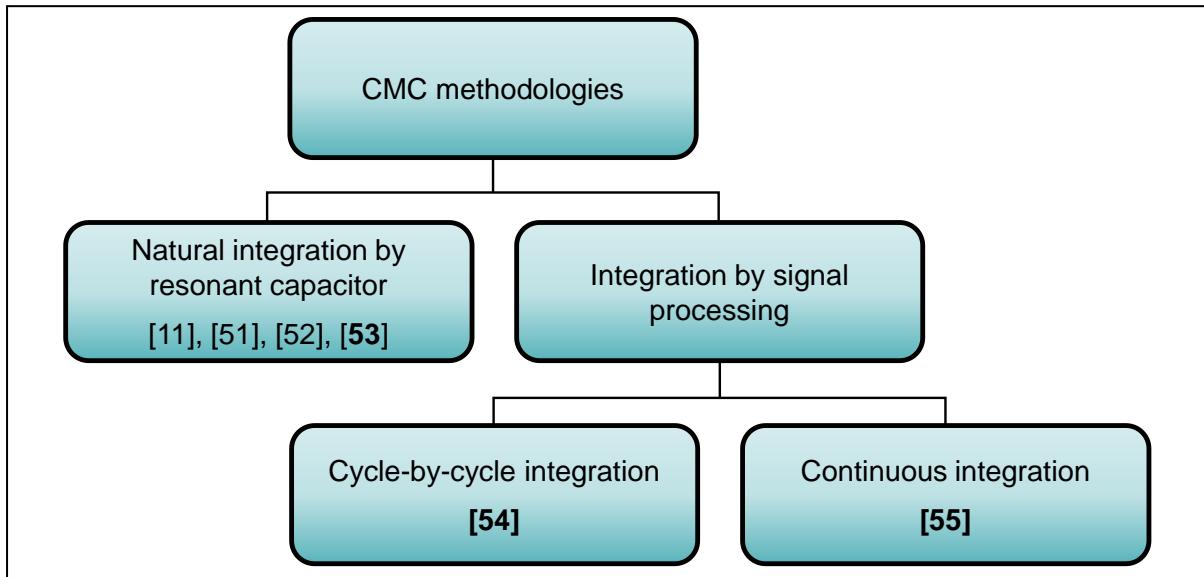
Since the resonant capacitor voltage  $V_C(t)$  is the integral of the resonant tank current  $I_R(t)$  the change  $\Delta V_C$  in  $V_C(t)$  in half a switching period  $T_{sw}/2$  is:

$$\Delta V_C = \frac{1}{Cr} \int_0^{T_{sw}/2} I_R(t) dt. \quad (26)$$

The integral in (26) is the controlled electric charge  $Q_c$ . To a first approximation,  $Q_c$  can be considered equal to  $Qin$ , the charge taken from the input source in a switching cycle by a half bridge; in a full bridge it is  $Q_c = Qin/2$ . The dc input current to the converter  $I_{in}$  is the per-cycle electric charge  $Qin$  multiplied by the switching frequency  $f_{sw}$ , hence:

$$\Delta V_C = \begin{cases} \frac{Qin}{Cr} = \frac{I_{in}}{Cr f_{sw}} & (\text{HB}) \\ \frac{Qin}{2 Cr} = \frac{I_{in}}{2 Cr f_{sw}} & (\text{FB}) \end{cases}. \quad (27)$$

**Figure 136. Classification tree of CMC methods. Methods to be analyzed are in bold.**



Assuming that  $t = 0$  is the instant of the positive-going edge of  $V_{HB}$ , the values of  $V_C(t)$   $V_C(0)$  and  $V_C(T_{sw}/2)$  are respectively:

$$V_C(0) = \begin{cases} \frac{1}{2} \left( V_{in} - \frac{I_{in}}{Cr f_{sw}} \right) & (\text{HB}) \\ -\frac{I_{in}}{4 Cr f_{sw}} & (\text{FB}) \end{cases}, \quad (28)$$

$$V_C(T_{sw}/2) = \begin{cases} \frac{1}{2} \left( V_{in} + \frac{I_{in}}{Cr f_{sw}} \right) & (\text{HB}) \\ \frac{I_{in}}{4 Cr f_{sw}} & (\text{FB}) \end{cases}. \quad (29)$$

Therefore, by controlling  $\Delta V_C$  - or  $V_C(0)$  and  $V_C(T_{sw}/2)$  - one can control  $Q_{in}$ . In other words, the controller senses the voltage across the resonant capacitor and toggles the half/full bridge when the voltage, or the voltage change, reaches predetermined values.

As previously mentioned, CMC is unstable at light load, so slope compensation is required and is realized by adding a properly synchronized ramp to the signal representative of the resonant voltage across  $Cr$ . As a result, at light load, when the integral signal becomes small and the slope compensation ramp dominates, CMC tends to DFC; this does not cause any stability issue because with DFC the LLC converter behaves as a first-order system at light load.

This gradual transition from CMC to DFC at light load is the reason why some authors term this method "hybrid" [55]-[56].

#### Integration by signal processing

The operating principle is based on sensing the tank current  $I_R(t)$  through a sense resistor  $Rs$  and integrating the voltage  $V_S(t)$  across  $Rs$ . The value of this integral is controlled by toggling the half/full bridge whenever its integral reaches a predetermined level  $H_q$ . The integration can be realized by charging/discharging a timing capacitor  $C_T$  with a current  $I_T$  proportional to the sensed voltage  $V_S$ , for example using an operational transconductance amplifier (OTA) whose transconductance is  $G_m$ . Therefore:

$$H_q = \frac{G_m}{C_T} \int_0^{T_{sw}/2} V_S(t) dt = \frac{G_m}{C_T} R_S \int_0^{T_{sw}/2} I_R(t) dt = \begin{cases} \frac{G_m}{C_T} R_S Q_{in} & (\text{HB}) \\ \frac{G_m}{2 C_T} R_S Q_{in} & (\text{FB}) \end{cases}, \quad (263)$$

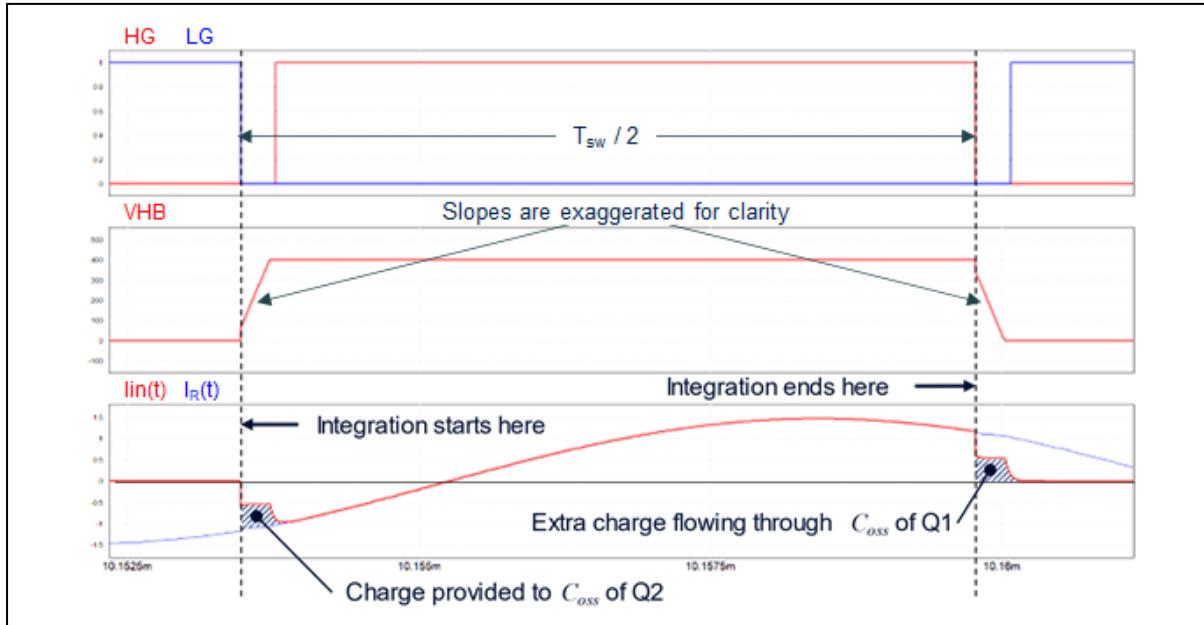
Also in this case, the instability of CMC at light load requires slope compensation so that at light load, CMC tends to DFC. It seems that the need for slope compensation makes hybridity as previously intended a necessary characteristic of any CMC method.

When integrating internally the signal representative of the resonant current, there are two options: resetting the integrator, i.e., forcing the timing capacitor  $C_T$  to zero every cycle or half-cycle like in the traditional CMC or continuously integrating so as to emulate the voltage  $V_C(t)$  of the resonant capacitor  $Cr$  on the timing capacitor  $C_T$ .

Before going through the various CMC implementations, it is important to clarify where the approximation in considering  $Q_c = Q_{in}$  in a half bridge and  $Q_c = Q_{in}/2$  in a full bridge lies. This can be explained with the help of figure 137, where the  $C_{oss}$  of the power switches have been abnormally increased on purpose to magnify the phenomenon.

Integration starts as LG turns off and ends when HG turns off. The final value of the integrator is proportional to the area included between  $I_R(t)$  (the blue curve) and the horizontal axis. Just after LG turns off, a portion of the tank current  $I_R(t)$  charges the  $C_{oss}$  of the low-side switch Q2 and takes its voltage from 0 to  $V_{in}$ . The remaining part of  $I_R(t)$  discharges the  $C_{oss}$  of the low-side switch Q1, taking its voltage from  $V_{in}$  to 0, and returns to the input source.

**Figure 137. Half bridge transition details showing the difference between  $I_R(t)$  and  $lin(t)$ .**



The shaded area between  $I_R(t)$  and  $lin(t)$  represents the charge involved in this transition that is not returned to the input source: it is a reduction of a negative contribution to the total charge  $Qin$ ; therefore, it is a positive contribution to  $Qin$ .

Just after HG turns off and integration is stopped, there is a “current tail” in  $lin(t)$  that charges the  $C_{oss}$  of the high-side switch Q1 taking its voltage from 0 to  $Vin$ . The  $C_{oss}$  of the low-side switch Q1 is discharged by the difference between  $I_R(t)$  and the tail of  $lin(t)$ . The shaded area between  $lin(t)$  and the zero horizontal axis represents this extra charge coming from the input source. It is an additional positive contribution to  $Qin$ .

Both contributions move the voltage across a capacitance  $C_{oss}$  (assumed to be the same for both Q1 and Q2) from 0 to  $Vin$ , then the exact expression of  $Qin$  for the half bridge is:

$$Qin_{HB} = Q_c + 2C_{eq}Vin , \quad (264)$$

whereas for the full bridge, everything doubles:

$$Qin_{FB} = 2Q_c + 4C_{eq}Vin . \quad (265)$$

In (264) and (265)  $C_{eq}$  is the linear charge-equivalent value of the  $C_{oss}$  of a single switch (it is therefore less than half the value of the total capacitance  $C_{HB}$ ).

At heavy load,  $Q_c$  normally dominates, and the second addend is negligible, so the approximate formulas (27) to (29) and (263) can be considered sufficiently accurate. At light or very light load, it is the other way round, thus the approximation may not be acceptable anymore.

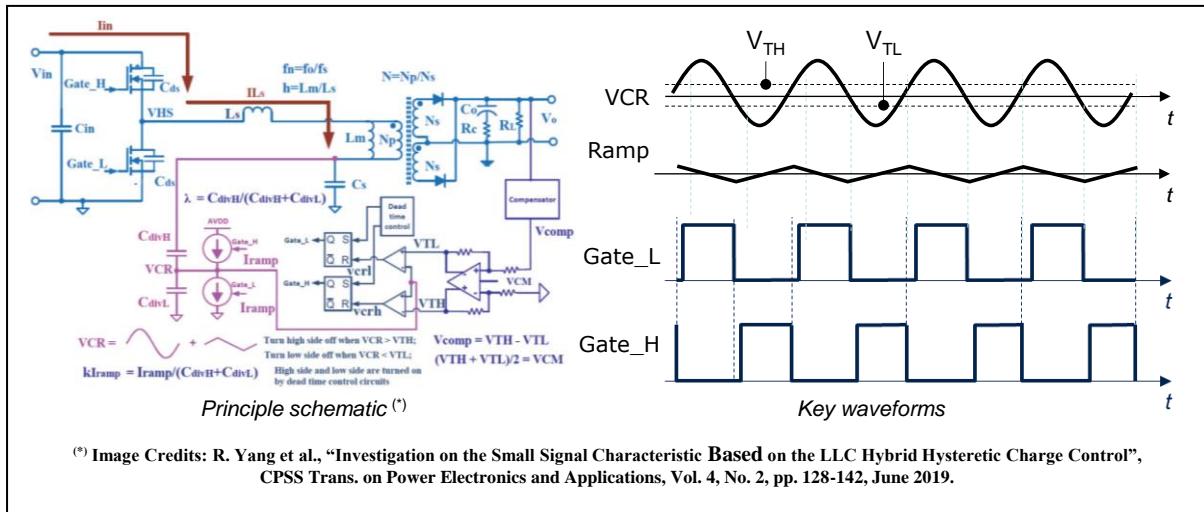
The controlled charge in a switching half cycle is therefore:

$$Q_c = \begin{cases} Qin - 2C_{eq}Vin & (\text{HB}) \\ \frac{Qin}{2} - 2C_{eq}Vin & (\text{FB}) \end{cases} . \quad (266)$$

#### *Natural integration – Hybrid Hysteretic Charge Control (HHCC)*

Figure 138 shows the schematic illustrating the basic operating principle of HHCC [55], [56] in a half bridge LLC converter on the left-hand side, along with the key waveforms on the right-hand side.

**Figure 138. Principle schematic and key waveforms of HHCC.**



LG is turned off (and HG is turned on after the dead-time) when  $VCR$  goes below  $V_{TL}$ , while HG is turned off (and LG is turned on after the dead-time) when  $VCR$  exceeds  $V_{TH}$ . Notice that the sum of the scaled down  $V_C(t)$  and the slope compensation ramp is done by injecting the current  $\pm I_{ramp}$  into the capacitor divider that senses  $V_C(t)$ .

The control law of this arrangement is:

$$V_{TH} - V_{TL} = \lambda \frac{Q_c}{C_r} + \frac{T_{sw} I_{ramp}}{2 \lambda C_{divL}}, \quad (267)$$

where  $\lambda$  is the gain of the capacitive divider:

$$\lambda = \frac{C_{divH}}{C_{divH} + C_{divL}}. \quad (268)$$

The challenge with this method is to have a very good matching between the charge and the discharge value of  $I_{ramp}$ .

Similar techniques are proposed in [53] and [54], where slope compensation is not mentioned. In [53], the same mechanism as in [54] to produce a triangular ramp to be superimposed on the integral signal is proposed to ensure 50% duty cycle of the generated square wave.

#### *Integration by signal processing – resettable integrator*

Figure 139 shows the operating principle of CMC with resettable integrator [57] in a half bridge LLC converter on the left-hand side, along with the key waveforms on the right-hand side.

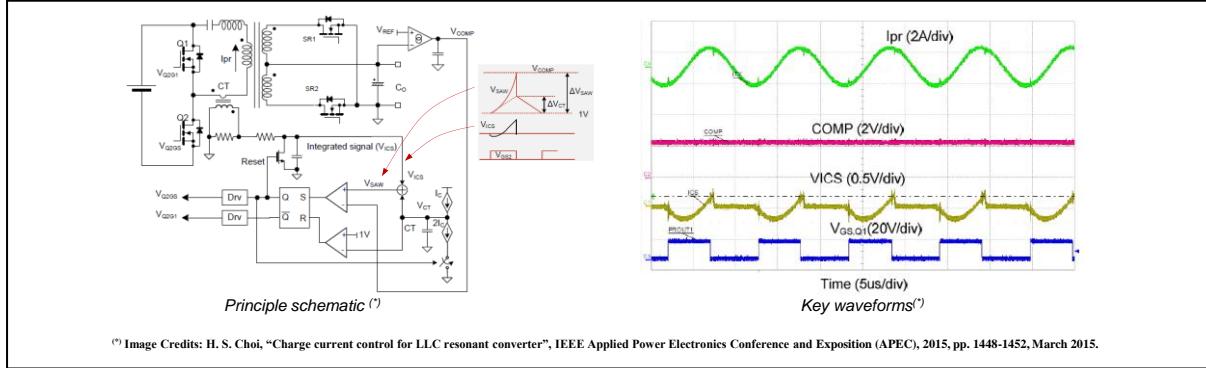
The tank current  $I_{pr}$  is sensed and integrated inside the control IC with an RC low-pass filter, generating the signal  $V_{ics}$ .

Notice that the tank current is connected to the input voltage bus instead of ground like, for example, in the typical schematic of figure 14. This exchanges the roles of the switches Q1 and Q2: the positive voltage  $V_{HB}$  is applied to the resonant tank when Q2 is on and the negative voltage when Q1 is on.

An up/down ramp ( $V_{CT}$ ) is generated by charging a capacitor  $CT$  with a current  $I_C$  always active and discharging it with a switched current  $2I_C$  synchronized to gate drive signals in such a way that the ramp goes up while the low-side switch is on and goes down while the high-side switch is on. In this way the capacitor is charged and discharged by equal currents  $\pm I_C$ .

The two signals are added together generating  $V_{SAW}$  that is compared to the control variable  $V_{COMP}$ . When, during the half-cycle while the low-side switch is on,  $V_{SAW}$  hits  $V_{COMP}$  the low-side switch is turned off (and the high-side switch is turned on after the dead-time); at the same time the integrator is reset by the Reset switch and kept in reset state as long as the high-side switch is on. When  $V_{CT}$ , which is now ramping down, equals 1 V the high-side switch is turned off and the low-side switch is turned on after the dead-time.

**Figure 139. Principle schematic and key waveforms of CMC with resettable integrator.**



Therefore, the charge control is done only during the half-cycle where the low-side switch is on (where the converter draws energy from the input source), while the voltage  $V_{CT}$  that performs slope compensation during that half-cycle acts as a timer in the other half-cycle, thus ensuring a 50% duty cycle square wave voltage.

The control law of this arrangement is:

$$V_{COMP} = F(Qin, Vin, T_{sw}) + \frac{T_{sw} I_C}{2 CT}, \quad (269)$$

where  $F$  is a function of  $Qin$ ,  $Vin$  and  $T_{sw}$  that depends on the ratio of the RC time constant of the integrator and the switching period.

Also in this case, the challenge is to have a very good matching between the charge and the discharge value of  $I_C$ .

#### *Integration by signal processing – continuous integration*

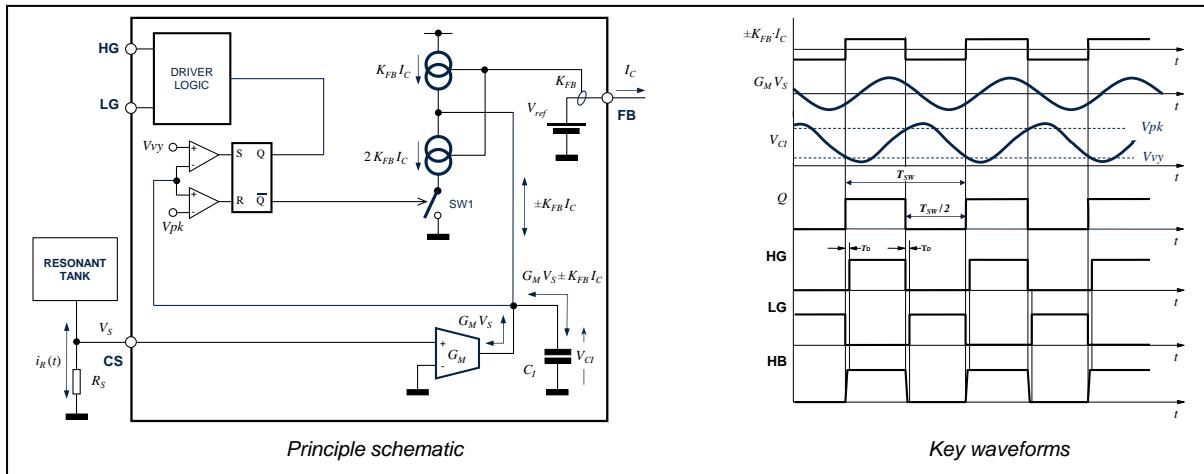
Figure 140 shows the schematic illustrating the operating principle of CMC with continuous integration [58] on the left-hand side, along with the key waveforms on the right-hand side.

The control device has two inputs: CS, which receives the voltage  $V_s(t)$  across the sense resistor  $R_s$ , proportional to the current  $I_R(t)$  in the resonant tank, and FB, which sources the control current  $I_C$  representative of the feedback loop that regulates converter's output voltage  $V_{out}$  or current  $I_{out}$ . The two outputs, HG and LG, drive the transistors Q1 and Q2 of the half-bridge.

The logic is such that, when the output Q of the SR latch is high, HG is high and the high-side MOSFET Q1 is ON (LG is low and the low-side MOSFET Q2 is OFF); whereas, when it is low, LG is high (Q2 is ON) and HG is low (Q1 is OFF).

The tank current  $I_R(t)$  is sensed, and a current proportional to the current sense voltage  $V_s(t)$ ,  $G_M V_s(t) = G_M R_s I_R(t)$  is generated through an OTA. The tank current and then, also the signal  $V_s(t)$  are both positive and negative, so that the OTA sinks and sources current depending on the sign of  $V_s(t)$ : current is sourced when  $V_s(t) > 0$ , sunk when  $V_s(t) < 0$ .

**Figure 140. Principle schematic and key waveforms of CMC with continuous integration.**



A pair of current generators  $K_{FB} I_C$  and  $2K_{FB} I_C$  are operated to generate a current square wave  $\pm K_{FB} I_C$  synchronized to the gate drive signals ( $K_{FB} I_C$  while HG is on,  $-K_{FB} I_C$  while LG is on).

The sum of OTA's output current and the square-wave current charges and discharges the integrating capacitor  $C_I$  generating the signal  $V_{Cl}$ . When  $V_{Cl} = V_{pk}$  HG is turned off and LG is turned on after the dead-time, when  $V_{Cl} = V_{vy}$  LG is turned off and HG is turned on after the dead-time.

To determine the control law, let us consider the swing  $\Delta V_{Cl} = V_{pk} - V_{vy}$  of  $V_{Cl}$  in the switching half-cycle where  $V_{HB} > 0$  ( $Q1$  is on), which is given by:

$$\Delta V_{Cl} = \frac{1}{C_I} \int_0^{T_{sw}/2} [K_{FB} I_C + G_M R_S I_R(t)] dt . \quad (270)$$

where  $I_C$  is supposed to be constant in  $(0, T_{sw}/2)$ . This considering, (270) becomes:

$$\Delta V_{Cl} = \frac{1}{C_I} \left[ T_{sw} \frac{K_{FB} I_C}{2} + G_M R_S \int_0^{T_{sw}/2} I_R(t) dt \right] . \quad (271)$$

Considering that the integral in (271) is the controlled charge  $Q_c$ , (271) can be rewritten as:

$$\Delta V_{Cl} = \frac{1}{C_I} \left( T_{sw} \frac{K_{FB} I_C}{2} + G_M R_S Q_c \right) . \quad (272)$$

Solving (272) for  $I_C$  we can find the steady-state value of the control variable:

$$I_C = \frac{2}{K_{FB} T_{sw}} (C_I \Delta V_{Cl} - G_M R_S Q_c) . \quad (273)$$

Then, also with this CMC method  $I_C$  depends on  $T_{sw}$ ; under given operating conditions  $T_{sw}$  depends on the parameters of the resonant tank and is therefore affected by their tolerance.

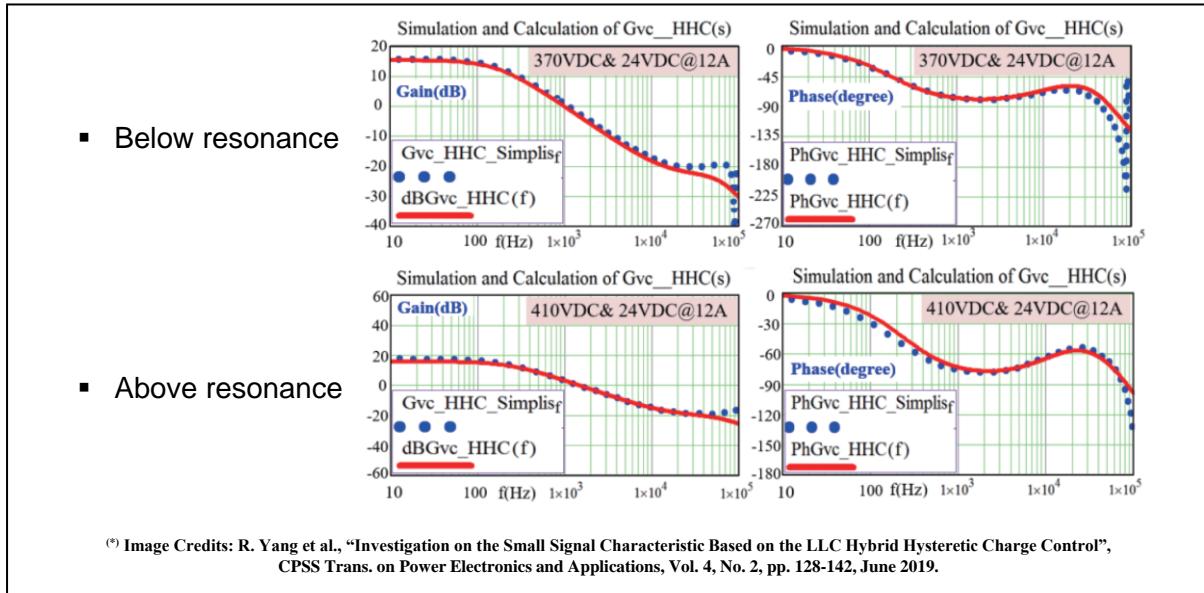
Note that the current  $\pm K_{FB} I_C$ , besides closing the feedback loop consistently with its typical implementations shown in figures 120 and 132 ( $I_C$  varies inversely with the load), performs also slope compensation and eliminates the subharmonic instability of CMC.

Unlike the previously discussed CMC methods, which introduce a fixed amplitude slope compensation, in this case slope compensation changes with the load. At full load, where  $I_{in}$  is at a maximum and slope compensation is not needed,  $\pm K_{FB} I_C$  has the minimum amplitude; as the load decreases and slope compensation may become necessary,  $\pm K_{FB} I_C$  increases reaching its maximum at no-load. In this way it is possible to have "more CMC" at full load, where one can maximally benefit of its dynamic characteristics.

### Small-signal characteristics of $G_P(j\omega)$

It is worth noticing that in the control laws (267), (269) and (273) include quantities that are directly linked to the energy flow and that are essentially dc quantities. Controlling the per-cycle charge hides the complex interaction between the switching frequency and the resonance frequency that governs the small-signal behavior of the LLC converter with DFC.

**Figure 141. Bode plot of  $G_P(j\omega)$  with HHCC in below and above resonance operation.**



Since the small-signal information on energy modulation contained in the controlled quantity does not have significant switching frequency components, there are the conditions for using an ac modeling method based on averaging. Actually, this is the approach used to derive the small-signal model in [55] and [56].

With just small differences, all CMC methods result in a single pole system in the frequency range of interest for the design of the compensator  $G_1(j\omega)$ , in all the operating conditions. As a representative example, figure 141 shows the bode plots of  $G_P(j\omega)$  with HHCC [55], [56], comparing calculations and simulations. [53] and [54] show very similar results.

Simulations shows the presence of a double-pole at the switching frequency, which is not predicted by the calculated small-signal model. However, their position does not impact the design of the compensator.

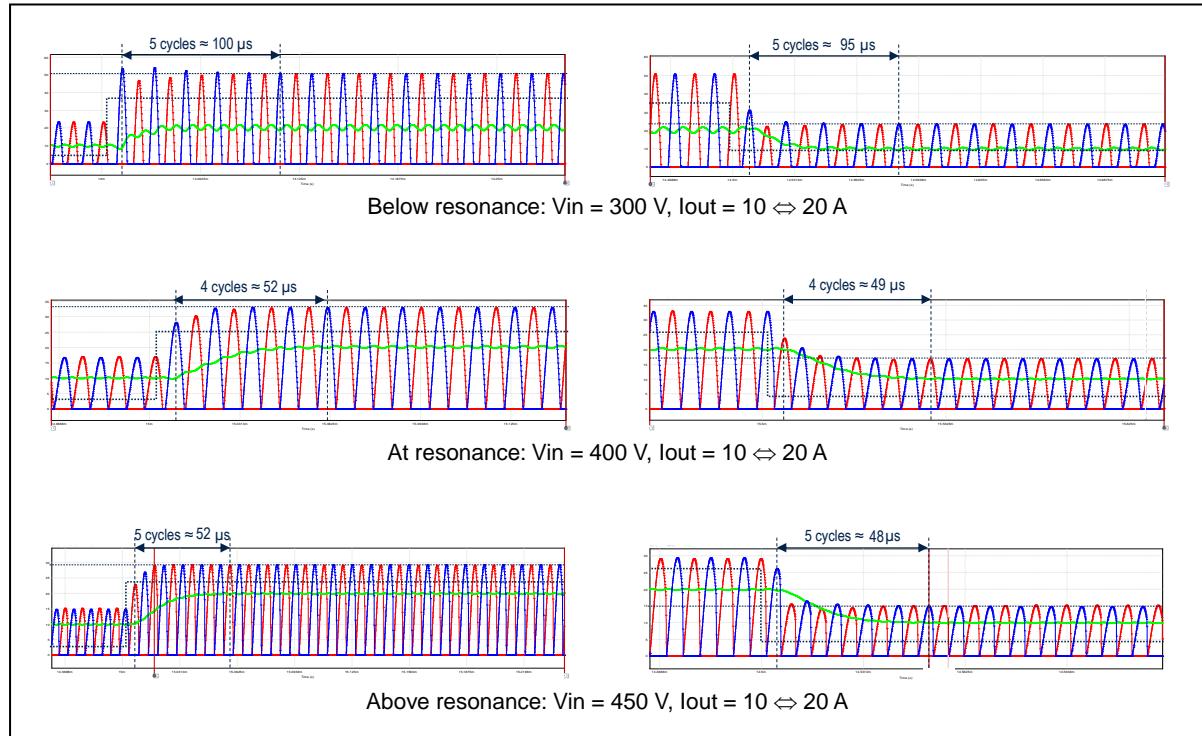
#### Open-loop step response test

Figure 142 shows the simulation results of the open-loop step response of the converter specified in Table 12 operated with the CMC control circuit illustrated in figure 140 (continuous integration of sensed tank current).

The test procedure is still the same: step changes are applied to the control current  $I_C$  to change the dc output current from 10 to 20 A and then back to 10 A (50%  $\Rightarrow$  100%  $\Rightarrow$  50% load). The output voltage is fixed at 12 V, and the test is done at the minimum, typical and maximum input voltage.

Table 14 compares the results of the open-loop response test for CMC, TSC and DSC. DSC speed (defined as the reciprocal of the number of cycles) is used as the baseline.

**Figure 142. Open-loop transient response of the converter specified in Table 12 with CMC (continuous integration). Red and blue traces: secondary currents; green trace: output current ( $I_{out}$ ); dotted black line: control signal.**



**Table 14. Comparison of open-loop test response speed for CMC, TSC and DFC**

$V_{in}$	#Cycle ratio (DFC / TSC)		#Cycle ratio (DFC / CMC)	
	$10 \text{ A} \Rightarrow 20 \text{ A}$	$20 \text{ A} \Rightarrow 10 \text{ A}$	$10 \text{ A} \Rightarrow 20 \text{ A}$	$20 \text{ A} \Rightarrow 10 \text{ A}$
300	3	6	5.4	3.6
400	3.13	8.33	6.25	6.25
450	2	2	1.2	0.8

With CMC the response is the same in both directions and little dependent on the input voltage. Compared to DFC, the improvement is substantial below and at resonance, while above resonance it is only slightly faster in case of a positive step change and slightly slower in the negative step change. TSC is the fastest in the above resonance operation and always the fastest in the negative step change.

#### *Feedback loop design with CMC*

Also, with CMC the feedback loop will be implemented using a type-2 error amplifier (pole at the origin plus one pole and one zero) equal to that shown in figure 142 and with the same transfer function (267).

Like with TSC, one might consider designing the loop for a higher bandwidth and need to get rid of the effects of  $C_{OPTO}$  using one of the solutions shown in figure 121.

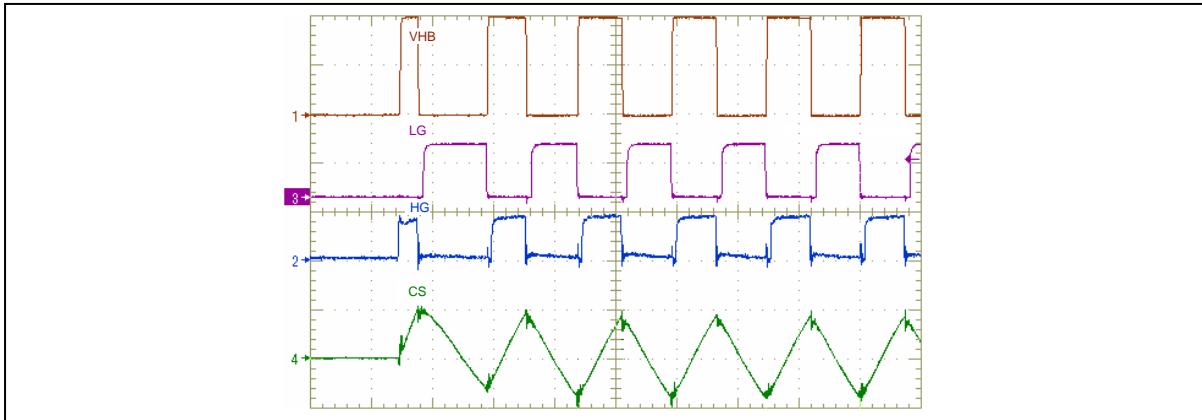
#### *Converter start-up with CMC*

CMC, like TSC, inherently prevents the flux doubling issue at start-up that affects the half bridge version of the LLC converter. It naturally ensures that the tank current has the right sign

when the half bridge is toggled: either the capacitor voltage or the internal integrator voltage can move, for example, from the lower threshold to the upper threshold only if the tank current is positive, as long as it is negative it cannot move in that direction.

The scope picture in figure 143 shows the start-up of the 170W LLC half-bridge converter for flat screen TV SMPS taken as an example also for TSC demonstration.

**Figure 143. Half bridge converter's start-up: CMC prevents flux doubling.**



#### *Comparison between different CMC implementations*

From the dynamic point of view all CMC methods offer similar good performance and the same easiness of compensator design and fine tuning. The following comparison, then, addresses the cost and the challenges of their implementations

The CMC methods with the natural integration operated by the resonant capacitor need a high voltage capacitive divider and a dedicated input in the control IC. Essentially, they are then characterized by a higher external component count with respect to CMC methods where integration is based on signal processing.

In fact, they do not need any extra external component or dedicated input in the control IC because they use the current sensing input and the current sense resistor that are already existing for protection purposes.

With a simple RC integration, the amplitude of the signal depends on both current and frequency, therefore their nonlinearity is substantial. Using an OTA this issue is mitigated but the implementation of the OTA is quite critical and needs special care.

In fact, its  $G_M$  must be well controlled and the same while sinking and sourcing current and essentially constant over a wide frequency range (at least up to 1/10 of the maximum switching frequency). Any sink/source asymmetries in  $G_M$  would cause asymmetry in the tank current in the two half switching cycles. Therefore, different currents would flow through the secondary rectifiers causing a larger output voltage ripple and different thermal stress in the secondary rectifiers. Any significant change of  $G_M$  in frequency will introduce a nonlinearity in the actual  $I_C$  vs.  $Q_C$  relationship (273).

In short, the benefit of a lower component count offered by signal processing integration comes with an increased internal complexity, which is normally less expensive overall.

As previously highlighted, in all implementations it is crucial to have an excellent matching between the charge and discharge currents that generate the triangular ramp used for slope compensation and/or for timing. Their mismatch will have cause asymmetry in the tank current in the two half switching cycles with all that this implies.

### *Summary and conclusions*

As a conclusion, CMC provides several benefits, specifically:

- CMC makes the LLC converter behave as a first-order system
  - Frequency compensation is much easier, response to perturbations is damped and large control bandwidths are possible
- Integration makes control system little sensitive to noise
- Open-loop input ripple rejection is good
  - Lower 100/120 Hz gain of the compensator is needed to obtain a good input ripple rejection ratio
- CMC prevents hard switching at start-up
  - Converter reliability is improved

There is, however, still a drawback, specifically:

- Though with CMC the correlation of the control variable with the load is much better than with DFC and TSC, it is however much influenced by the input voltage
- The dependence on the switching frequency makes it sensitive to the tolerance of the components in the tank circuit
  - These two drawbacks limit the usage of the control variable as a load monitor to establish burst-mode operation or detect overload.

# Chapter 5

## Average input current control (AICC)

The Average Input Current Control (AICC) [59] has been developed with the intent of overcoming one of the residual drawbacks of CMC – the dependence of the control voltage on the switching frequency – while retaining all its good properties.

AICC blends CMC with a special implementation of Average Current Mode Control (ACMC) able to perform a sort of instant averaging, thus overcoming the drawbacks of the traditional ACMC too.

Traditionally, ACMC features two nested loops where the inner loop controls the average value of a current in the converter, based on a reference level set by the outer loop that regulates the output voltage or current. A major strength of ACMC is robustness: the inner loop reduces the sensitivity of the outer loop to the characteristics and the parameters of the power stage.

ACMC was initially developed for PWM-controlled converters but has been applied to resonant converters too [63], [64]. Compared to CMC, however, the price to pay for robustness is slower dynamics, greater circuital complexity as well as more design and fine-tuning effort due to the task of compensating two loops.

AICC brings CMC to the next level, keeping its benefits, adding the robustness of ACMC with none of the above-mentioned drawbacks. More specifically, its characteristics and benefits can be synthesized as follows:

- AICC regulates the dc input current to the converter based on a reference level set by the control loop that regulates the output voltage or current.
- Unlike the traditional ACMC, AICC is characterized by a seemingly single loop control architecture like peak current mode control in PWM-controlled converters; this explains why it requires less design and fine-tuning effort, as well as fewer external parts than traditional ACMC schemes with their two-loop control architecture.
- Averaging of the input current is done on a cycle-by-cycle basis, thus AICC provides also excellent dynamic properties, aligned to those of CMC control, unlike traditional ACMC schemes where averaging slows down the overall dynamics of the converter.
- The feedback loop that regulates the output voltage or current is insensitive to the parameters of the LLC tank and to their tolerance. There are just second-order effects due to the unavoidable nonidealities.
- To a first approximation, the control signal in the feedback loop is a (linear) function of converter's dc input current only; if the input voltage is regulated, like when the LLC converter is powered by a PFC pre-regulator, the control signal may be used as a load monitor to establish burst-mode operation or detect overload with good accuracy and statistical repeatability in mass production.
- The obvious fact that the control signal is bounded within a range, implies that the input current to the converter will be inherently limited too; this lends *Limited Power Source* (LPS) characteristics to the converter and enables a simple overload detection, and a simpler implementation of the overload protection circuits.

It goes without saying that these characteristics and benefits are maintained irrespective of the resonant tank order and configuration.

### AICC operating principle

Figure 144 shows the schematic illustrating the operating principle of AICC on the left-hand side, along with the key waveforms on the right-hand side.

It is possible to notice that the principle schematic of figure 144 is the same as that of the CMC with continuous integration in figure 140 with the addition of the block in the shaded area that generates the voltage reference  $V_{pk}$  and that includes the sub-block “TIMER” and a summer.

To better understand its purpose, let us start from the equation that provides the steady-state value of the control variable for the CMC system with continuous integration:

$$I_C = \frac{2}{K_{FB} T_{sw}} (C_I \Delta V_{CI} - G_M R_S Q_c) , \quad (274)$$

and for the moment let us assume that  $Q_c = Qin$  (in the half bridge,  $Q_c = Qin/2$  in the full bridge). Their difference is normally negligible at heavy load and becomes significant at light load, when  $Q_c$  tends to zero. Equation (274), also reminding that  $I_{in} = Qin / T_{sw} = Qin f_{sw}$ , can then be rewritten as follows:

$$I_C = \frac{2}{K_{FB}} \left( \frac{C_I \Delta V_{CI}}{T_{sw}} - \frac{G_M R_S}{\beta} I_{in} \right) , \quad (275)$$

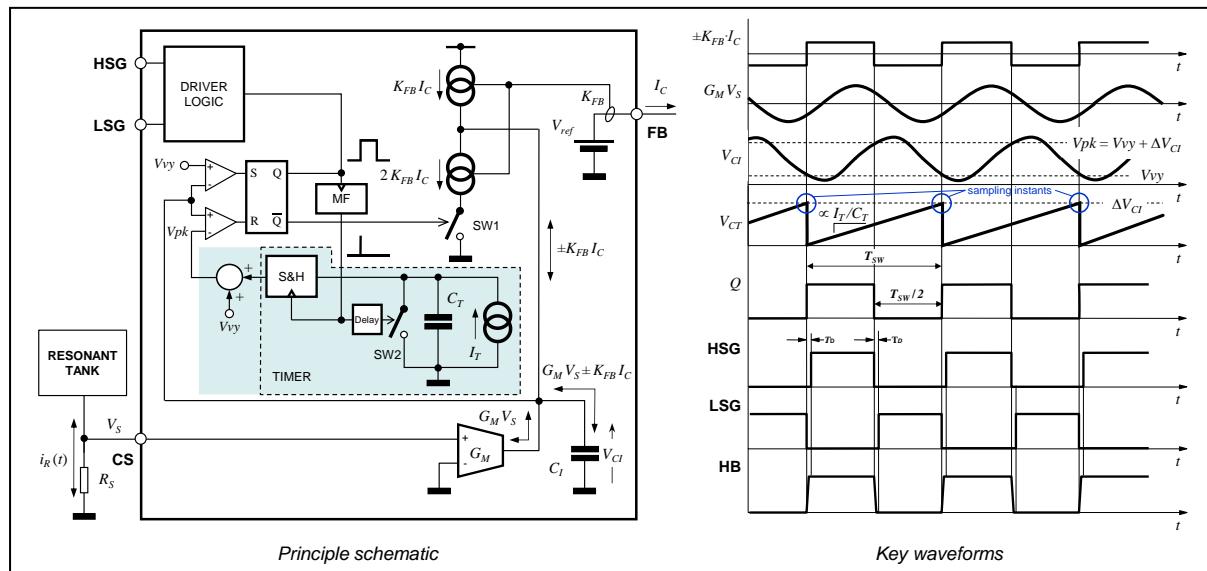
where  $\beta = 1$  for the half bridge and  $\beta = 2$  for the full bridge.

As previously mentioned, the objective of AICC is to eliminate the dependence of the control voltage on the switching frequency (i.e.,  $T_{sw}$ ), because for assigned operating conditions  $T_{sw}$  depends on the parameters of the resonant tank and is therefore affected by their tolerance. To eliminate this dependence,  $\Delta V_{CI}$  should be proportional to  $T_{sw}$ .

This is exactly the purpose of the block TIMER that outputs the voltage  $V_{pk}$  used as the upper reference by the comparator that resets the SR latch: a timing capacitor  $C_T$  is charged with a constant current  $I_T$ , generating a voltage ramp  $V_{CT}$ ; its peak value  $V_T = I_T T_{sw} / C_T$  is sampled and held on the positive-going edges of the signal  $Q$  via the pulses delivered by the monostable MF; the ramp is reset at zero immediately after. Finally,  $V_T$  is offset by  $V_{vy}$  and output as  $V_{pk}$ . As a result:

$$\Delta V_{CI} = V_{pk} - V_{vy} = V_T = \frac{I_T}{C_T} T_{sw} . \quad (276)$$

**Figure 144. Principle schematic and key waveforms of AICC.**



Substituting this in (275) yields:

$$I_C = \frac{2}{K_{FB}} \left( I_T \frac{C_I}{C_T} - \frac{G_M R_s}{\beta} I_{in} \right). \quad (277)$$

$I_C$  is now a function of internal parameters of the controller ( $K_{FB}$ ,  $I_T$ ,  $C_I$ ,  $C_T$ ,  $G_M$ ), of an external tuning parameter ( $R_s$ ) and is related to the dc input current  $I_{in}$  only. There is no dependence on the parameters nor on the tank configuration and this shows the robustness of AICC.

As to the accuracy of the internal parameters of the controller,  $K_{FB}$  is a mirror gain, which can be tightly controlled within a few percent;  $C_I$  and  $C_T$  can be matched so that their ratio is accurate; the transconductance  $G_M$  of the OTA is proportional to its bias current that can be matched with  $I_T$  for better accuracy of the ratio  $I_T / G_M$ ;  $I_T$  can be trimmed and temperature compensated to minimize the spread.

Notice that there is a good correlation between  $I_C$  and the output load as well. Recalling that  $I_{in} = P_{out} / (\eta V_{in})$  the mismatch in the correlation is due to the variation of the efficiency  $\eta$  with the load. Additionally, a change in the switching frequency due to parameters tolerance may have a small impact on  $\eta$ . This will slightly change  $I_{in}$  for given load and  $V_{in}$ , and slightly change  $I_C$  as well.

Equation (277) is an acceptable approximation as long as the load is large enough that the difference  $Q_{in} - Q_C$  (in the half bridge,  $Q_C - Q_{in}/2$  in the full bridge) is small.

For a more general formula that includes also light load conditions, when the above-mentioned condition is no longer true, we need to consider (272), so that (277) is rewritten as:

$$I_C = \frac{2}{K_{FB}} \left[ I_T \frac{C_I}{C_T} - G_M R_s \left( \frac{I_{in}}{\beta} - 2C_{eq}V_{in}f_{sw} \right) \right]. \quad (278)$$

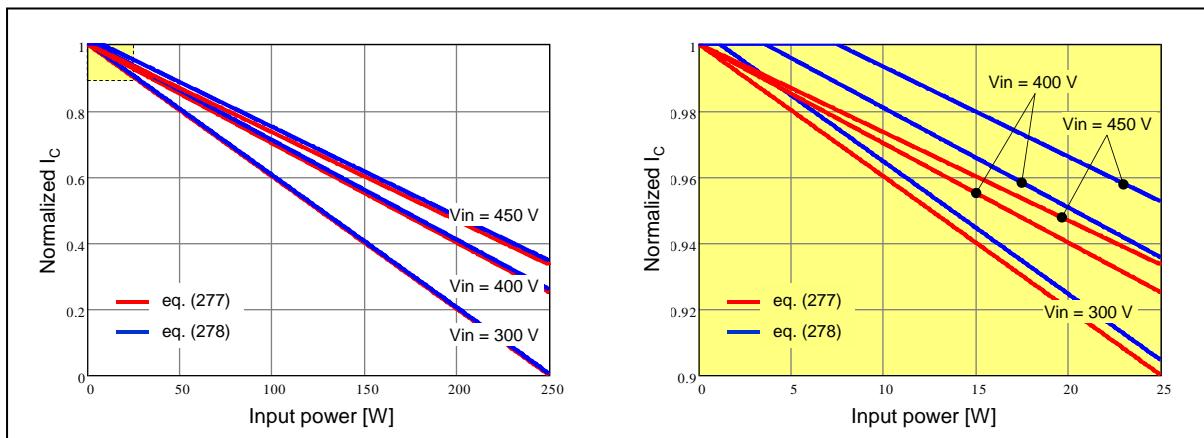
The term proportional to  $V_{in} \cdot f_{sw}$  causes additional dependence of  $I_C$  on the input voltage and reduces its insensitivity to the parameters of the resonant tank and their tolerance.

The plots of figure 145 illustrate this trend for the half bridge converter specified in Table 12 showing the value of the control variable  $I_C$ , normalized to the value

$$I_{Cn} = \frac{2}{K_{FB}} I_T \frac{C_I}{C_T}. \quad (279)$$

that corresponds to  $I_{in} = 0$  in (277). The plot on the left-hand side, shows  $I_C$  as a function of the input power in the 0-100% range for the minimum, typical and maximum input voltage.

**Figure 145. Normalized  $I_C$  vs. Input power at different input voltages for the converter specified in Table 12. 0-100% load range (left), 0-10% load range (right).**



That on the right-hand side shows the zoom of the 0-10% load range region, highlighted in yellow in the plot on the left. In both plots the red lines refer to the approximate equation (277), the blue lines to (278).

Quite obviously, the gap between the two set of curves increases with the input voltage and is significant at light and very light load, where the term proportional to  $V_{in} \cdot f_{sw}$  dominates. At high voltage the control current  $I_C$  may exceed the value  $I_{Cn}$  given by (279) and this must be taken into account when designing the feedback circuit, for example like that of figure 132.

The half-bridge converter specified in Table 12 has been simulated with PSIM including all reasonably expected nonidealities both in the control and in the power circuit to explore its large-signal properties.

The plot on the left-hand side of figure 146 shows the theoretical control law (277) with the black dotted line and the simulated ones (round markers) in the load range 1% to 100% at the minimum, typical and maximum input voltage.

As expected from the plots of figure 145, the major effect of the nonidealities is to add an offset to  $I_C$  that depends on the input voltage, while the slope is nearly unaffected. The nonlinearity is very small, and the curves are essentially straight lines.

The plot on the right-hand side of figure 146 shows the difference between the results shown on the left and the values predicted by (278). The maximum error is limited to less than 6% in a 100:1 load range across the  $V_{in}$  range.

The large-signal model can be found by solving (278) for  $I_{in}$ :

$$I_{in} = \beta \left[ \frac{1}{G_M R_S} \left( I_T \frac{C_I}{C_T} - \frac{K_{FB}}{2} I_C \right) + 2C_{eQ} V_{in} f_{sw} \right], \quad (280)$$

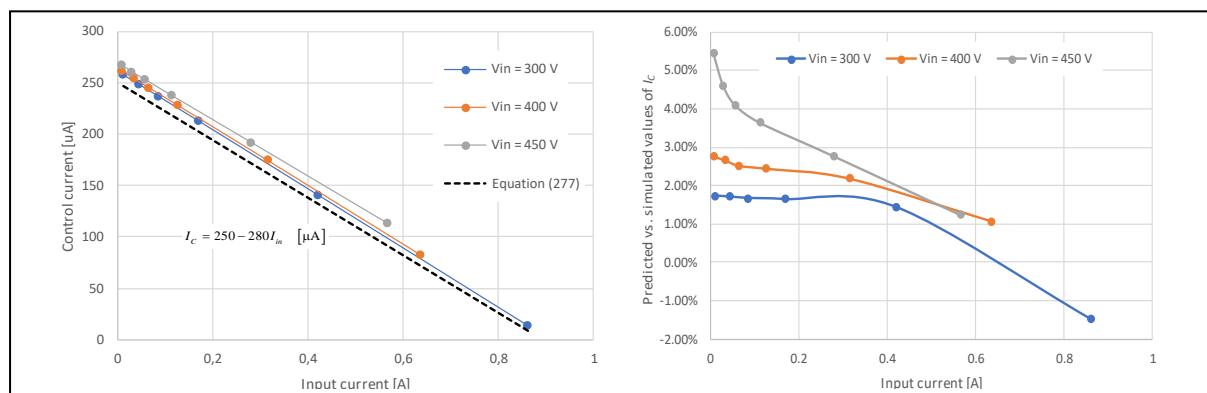
where  $\beta = 1$  for the half bridge and  $\beta = 2$  for the full bridge. Notice that when  $I_C = 0$  the input current  $I_{in}$  reaches its maximum value that, neglecting the contribution of the term proportional to frequency that should be significantly smaller, is expressed by:

$$I_{in_{max}} = \frac{\beta}{G_M R_S} I_T \frac{C_I}{C_T}. \quad (281)$$

The maximum input current is inherently bounded, and the converter is automatically protected against overcurrent with no need of a dedicated protection function.

It is worth emphasizing once more that in all these considerations the configuration of the resonant tank is irrelevant and the properties of AICC apply to the LLC converter just as to the LCC or whatever type of class D resonant converter.

**Figure 146. Comparison of theoretical control law (277) and simulated  $I_C$  vs  $I_{in}$  plots for the converter specified in Table 12 (left); error in predictions of (278) with respect to simulated  $I_C$  vs  $I_{in}$  relationships (right).**



### Small-signal characteristics of $G_P(j\omega)$

Since the crossover frequency  $f_c$  of the open-loop gain in many real-world feedback designs is typically not exceeding  $f_{sw}/10$ , we will consider a low-frequency approximation of the small-signal model that neglects energy storage/exchange phenomena in the resonant tank, as well as the sampled nature of  $\Delta V_{CI}$  (276).

Under these assumptions, the small-signal model of a resonant converter with AICC can be derived by linearizing the average large signal model (281) around the steady-state operating point.

For the sake of simplicity, we will assume that the converter is 100% efficient and that the frequency dependent term in (281) is negligible. Reminding that  $V_{in} I_{in} = V_{out} I_{out}$ , we can write:

$$I_{out} = \frac{V_{in}}{V_{out}} I_{in} = \frac{V_{in}}{V_{out}} \frac{\beta}{G_M R_S} \left( I_T \frac{C_I}{C_T} - \frac{K_{FB}}{2} I_C \right). \quad (282)$$

Therefore, differentiating (282) we find:

$$\hat{i}_{out} = K_i \hat{v}_{in} + K_o \hat{v}_{out} + K_c \hat{i}_c, \quad (283)$$

where:

$$K_i = \frac{\partial i_{out}}{\partial v_{in}} = \frac{i_{in}}{v_{out}}, \quad (284)$$

$$K_o = \frac{\partial i_{out}}{\partial v_{out}} = -\frac{i_{out}}{v_{out}} = -\frac{1}{R_{out}}, \quad (285)$$

$$K_c = \frac{\partial i_{out}}{\partial i_c} = -\beta \frac{V_{in}}{V_{out}} \frac{K_{FB}}{2 G_M R_S}. \quad (286)$$

Eq. (283) results in the Norton-type small-signal equivalent schematic shown in figure 147.  $Z_{out}$  is the impedance of the load connected to the power stage, which comprises the parallel of the output capacitor  $C_{out}$  (including its ESR  $R_C$ ) with the small-signal resistance of the load  $r_{out}$ . The expression of  $Z_{out}$  in the frequency domain is therefore:

$$Z_{out}(j\omega) = r_{out} \frac{1+j\omega R_C C_{out}}{1+j\omega(R_C+r_{out}) C_{out}}. \quad (287)$$

Of course, it is:

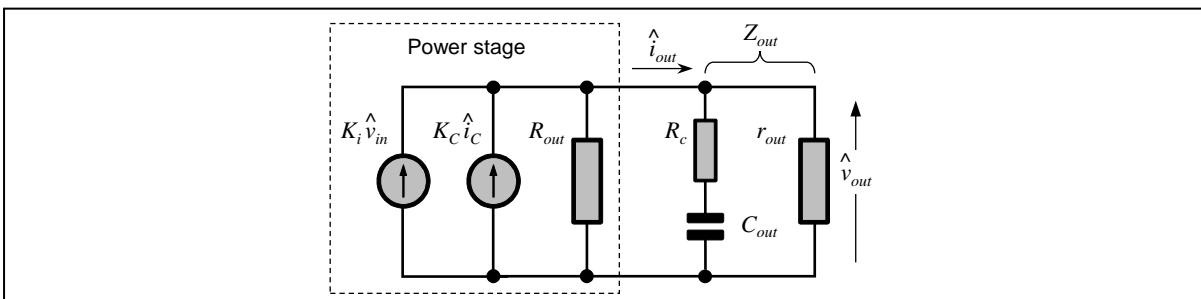
$$\hat{v}_{out} = \hat{i}_{out} Z_{out}(j\omega). \quad (288)$$

Since we are interested in the control-to-output transfer function  $G_P(j\omega) = \hat{v}_{out}/\hat{i}_c$  we assume that  $V_{in}$  is constant (then  $\hat{v}_{in}=0$ ). The general expression of  $G_P(j\omega)$  is found by substituting (283) in (288) and collecting  $\hat{v}_{out}$ :

$$G_P(j\omega) = \frac{\hat{v}_{out}}{\hat{i}_c} = K_c \frac{Z_{out}(j\omega)}{1-K_o Z_{out}(j\omega)}. \quad (289)$$

The actual expression of  $G_P(j\omega)$  depends on the nature of the load, which determines the small-signal load resistance  $r_{out}$ . We will consider three practical cases.

**Figure 147. Equivalent small-signal model of a resonant converter with AICC.**



- If the load is resistive, the small-signal load resistance equals the large-signal load resistance, i.e.,  $r_{out} = Rout = V_{out} / I_{out}$ . In this case the expression of  $G_P(j\omega)$ , obtained by combining (286) and (282) is:

$$G_P(j\omega) = G_{Pr}(j\omega) = \frac{K_c Rout}{2} \frac{1+j\omega R_C C_{out}}{1+j\omega(R_C + \frac{Rout}{2}) C_{out}}. \quad (290)$$

- During bench tests it is customary to use a constant-current load. In this case, the small-signal load resistance is an open circuit ( $r_{out} \rightarrow \infty$ ) and  $G_P(j\omega)$  is:

$$G_P(j\omega) = G_{Pi}(j\omega) = K_c Rout \frac{1+j\omega R_C C_{out}}{1+j\omega(R_C + Rout) C_{out}}. \quad (291)$$

- In case the converter supplies another switch-mode converter, which behaves as a constant-power load, it is  $r_{out} = -Rout$ . Then  $r_{out}$  and  $Rout$  cancel out and the controlled current generator drives only the capacitor and its ESR:

$$G_P(j\omega) = G_{Pp}(j\omega) = K_c \frac{1+j\omega R_C C_{out}}{j\omega C_{out}}. \quad (292)$$

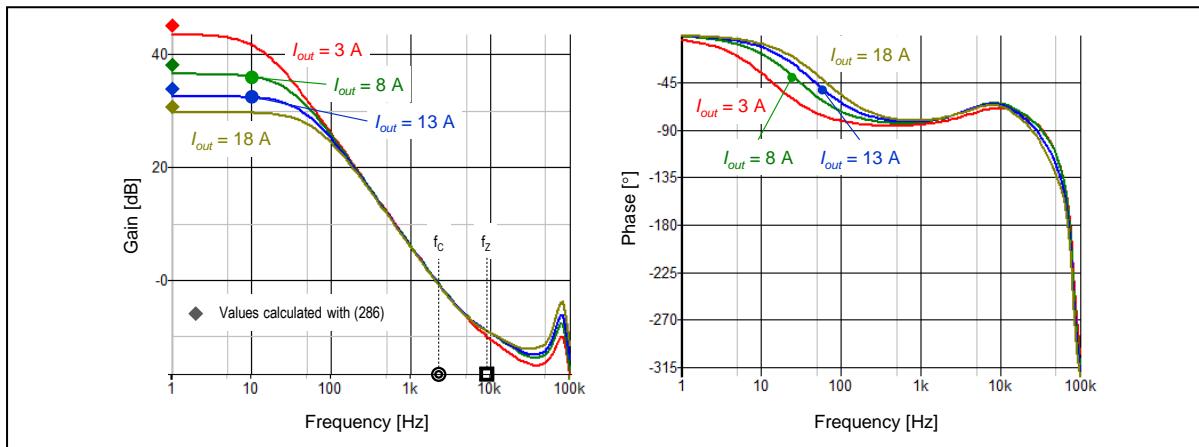
Notice that this small-signal model looks very much like that of a discontinuous-conduction-mode flyback converter operated at a fixed-frequency with peak current mode control. Pole and zero are exactly the same but the dc gain is different: in a flyback it depends on the square root of  $Rout$  does not depend on  $V_{in}$ .

Also notice that (292) does not depend on the load. Since it is normally  $R_C \ll Rout$ , the gain-bandwidth product in (290) and (291) does not depend on the load. In most practical cases, therefore, the open-loop crossover frequency  $f_c$  will be load-independent. It will depend on  $V_{in}$  only through  $K_c$  (286) and will achieve its maximum value at the maximum  $V_{in}$ .

The Bode plots of the transfer function (291) at the nominal  $V_{in}$  with different load conditions for the converter specified in Table 12, resulting from SIMPLIS simulations are shown in figure 148. It is apparent that the system has a single-pole characteristic in a quite broad frequency range (up to at least  $f_{sw}/10$ ). The numerical results are in good agreement with the theoretical predictions; there is just a few dB offset in the dc gain, supposedly due to the approximations inherent in (291), that has little impact on system stability and compensator design. The crossover frequency is also very close to the calculated value.

The simulations show a double-pole at the switching frequency, like with CMC not predicted by the small-signal model in figure 147.

**Figure 148. Bode plots of  $G_P(j\omega)$  with AICC at  $V_{in} = 400$  V, under different load conditions for the converter specified in Table 12.**



### Open-loop step response test

Figure 149 shows the simulation results of the open-loop step response of the converter specified in Table 12 operated with the AICC subject to the usual test procedure, here briefly reminded for readers' convenience.

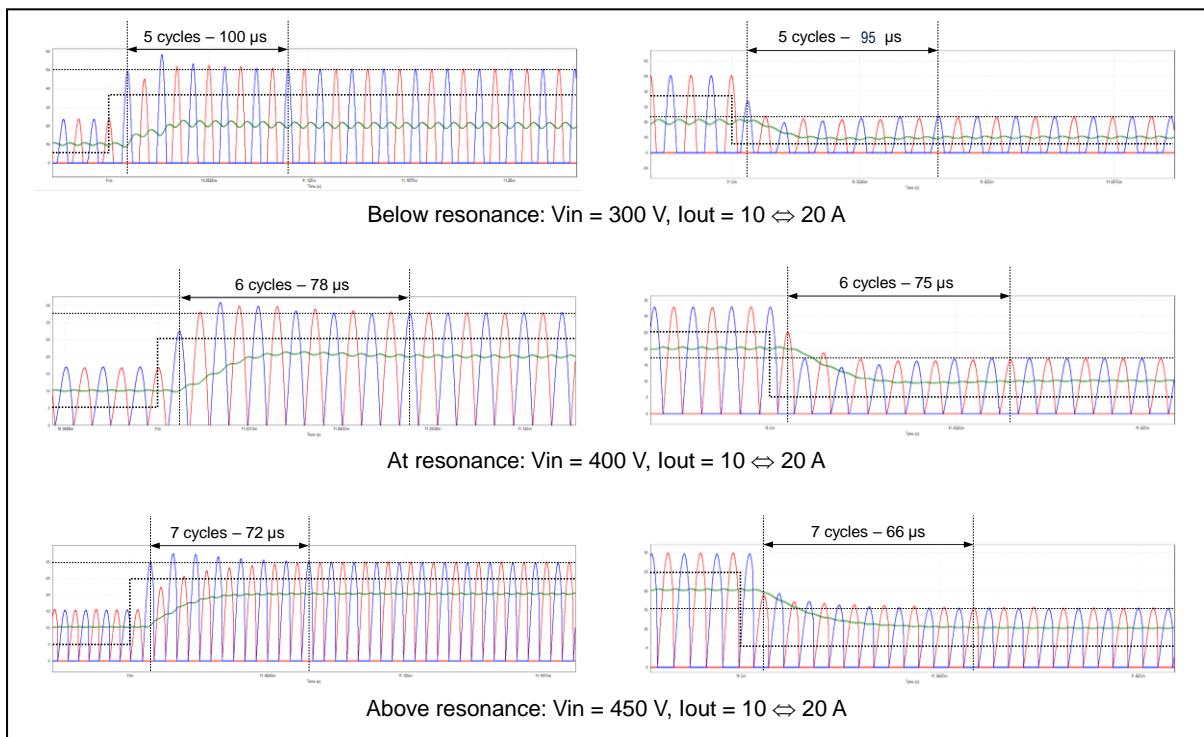
The control current  $I_C$  is changed with steps such that the dc output current goes from 10 to 20 A and then back to 10 A ( $50\% \Rightarrow 100\% \Rightarrow 50\%$  load) with the output voltage fixed at 12 V, repeating the test at the minimum, typical and maximum input voltage.

Like with CMC, with AICC the response is the same in both directions and little dependent on the input voltage. The response is as fast as that of CMC below resonance and only slightly slower at and above resonance.

The circuit in figure 144 envisages one switching period sampling every switching cycle. Simulations where sampling is done every half switching cycle have shown no speed increase.

Table 15 compares the results of the open-loop response test for AICC, CMC, TSC and DSC, still using the response of DFC as baseline.

**Figure 149. Open-loop transient response of the converter specified in Table 12 with AICC. Red and blue traces: secondary currents; green trace: output current ( $I_{out}$ ); dotted black line: control signal.**



**Table 15. Comparison of open-loop test response speed for AICC, CMC, TSC and DFC**

$V_{in}$	#Cycle ratio (DFC / TSC)		#Cycle ratio (DFC / CMC)		#Cycle ratio (DFC / AICC)	
	$10 \text{ A} \Rightarrow 20 \text{ A}$	$20 \text{ A} \Rightarrow 10 \text{ A}$	$10 \text{ A} \Rightarrow 20 \text{ A}$	$20 \text{ A} \Rightarrow 10 \text{ A}$	$10 \text{ A} \Rightarrow 20 \text{ A}$	$20 \text{ A} \Rightarrow 10 \text{ A}$
300	3	6	5.4	3.6	5.4	3.6
400	3.13	8.33	6.25	6.25	4.17	4.17
450	2	2	1.2	0.8	0.86	0.57

To summarize the comparison between the response speed of the various control methods, it is possible to state:

- DFC offers the slowest response overall, though above resonance it is comparable to CMC and slightly faster than AICC
- CMC and AICC have a more uniform response, little dependent on the input voltage, a similar speed, with CMC on average slightly faster
- TSC is fastest in negative-going transients and in the above resonance operation approaches the speed of the Optimal Trajectory Control

#### *Feedback loop design with AICC*

Also with AICC, the feedback loop will be implemented using a type-2 error amplifier with a pole at the origin plus a zero and a high frequency pole like that shown in figure 132 and with the same transfer function (262).

Like with TSC or CMC, one might consider designing the loop for a higher bandwidth and need to get rid of the effects of  $C_{OPTO}$  using one of the solutions shown in figure 121.

#### *Converter start-up with AICC*

AICC is based on a CMC control core and has the same cycle-by-cycle mechanism, and then can prevent flux doubling in half bridge LLC converters as shown in figure 150.

#### *AICC methodology enhancement*

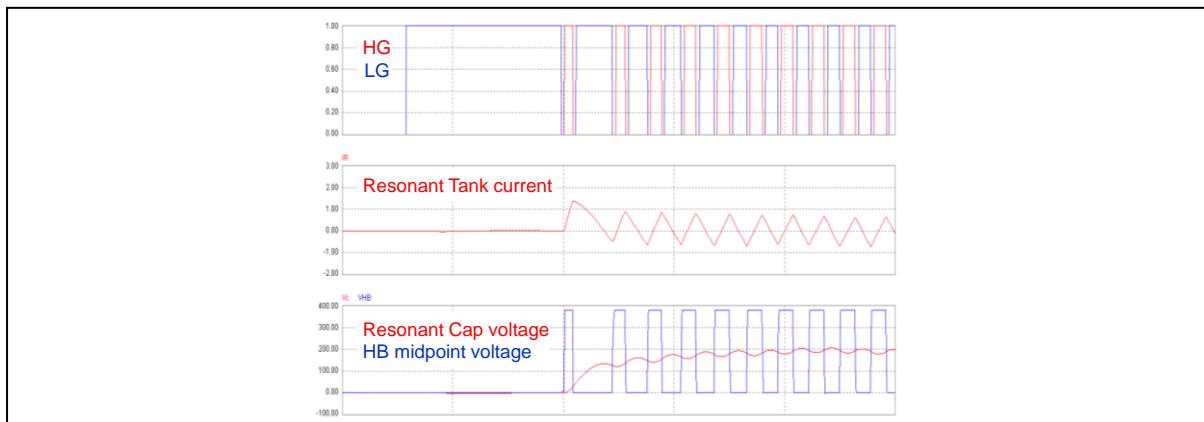
The seemingly only unsolved issue of AICC in resonant converters is the dependence of the control variable on the input voltage, which prevents its usage as a load monitor in systems with a wide-range input voltage.

This can be solved with an enhancement of AICC that could be termed AIPC, Average Input Power Control. The relevant principle schematic of the control circuit and its key waveforms are shown in figure 151.

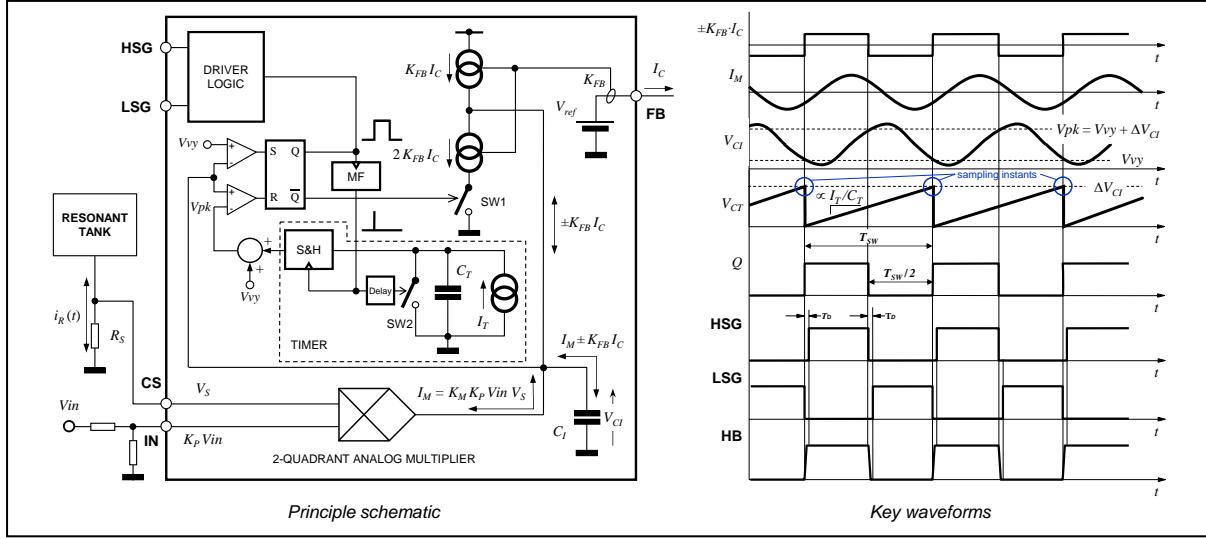
Compared to the AICC circuit of figure 144, the OTA that outputs a current proportional to the signal  $V_S$  on the current sense input is replaced by a two-quadrant multiplier whose inputs are the same signal  $V_S$  representative of the tank current and a voltage proportional to the input voltage  $V_{in}$  sensed via a resistor divider,  $K_P V_{in}$ . The multiplier outputs a current  $I_M$  proportional to the multiplication of the two input signals:

$$I_M = K_M K_P V_{in} V_S , \quad (293)$$

**Figure 150. Half bridge converter's start-up: AICC prevents flux doubling.**



**Figure 151. Principle schematic and key waveforms of the input power control method.**



where  $K_M$  is the multiplier gain. With this modification the control law (277) becomes:

$$I_C = \frac{2}{K_{FB}} \left( I_T \frac{C_I}{C_T} - \frac{K_M K_P R_S}{\beta} V_{in} I_{in} \right) = \frac{2}{K_{FB}} \left( I_T \frac{C_I}{C_T} - \frac{K_M K_P R_S}{\beta} P_{in} \right), \quad (294)$$

and the large-signal model:

$$P_{in} = \frac{\beta}{K_M K_P R_S} \left( I_T \frac{C_I}{C_T} - \frac{K_{FB}}{2} I_C \right). \quad (295)$$

The challenges of AIPC implementation are in the symmetry of the currents  $\pm K_{FB} I_C$  and in the linearity and the accuracy of the gain  $K_M$  of the multiplier.

### Summary and conclusions

The most important characteristics of AICC can be summarized as follows:

- Single loop control architecture unlike traditional Average Current Mode schemes, which have a two-loop architecture that requires more design and fine-tuning effort
- Averaging of input current is done on a cycle-by-cycle basis, which provides excellent dynamic properties aligned to those of CMC control
- The feedback loop is little sensitive to parameters of power stage. AICC can be classified as a *robust control*, applicable to any configuration of the tank circuit (LLC, LCC, etc.).
- With good approximation, the control variable is a linear function of converter's dc input current only. If the resonant converter is powered by a PFC, then with a regulated input voltage, the control variable may be used as a load monitor. The correlation with the load is good, affected only by efficiency changes.
- The bounds of the control signal cause the input current to converter to be inherently limited, thus overload protection circuits can be simplified.
- AICC can be further enhanced using a two-quadrant analog multiplier that enables the control of the input power and, to a first-order approximation, eliminates any dependence on the input voltage.

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# PART VI

## MISCELLANEOUS TOPICS

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### Chapter 1

### Synchronous rectification

Secondary rectification losses are a major source of inefficiency in any power converter. In an LLC resonant converter that processes power very efficiently, they are very likely the top source of losses. Figure 152 shows the loss breakdown in a typical LLC design based on diode rectification, where the secondary conduction losses are clearly the biggest source of loss, most of them located in the diode rectifiers.

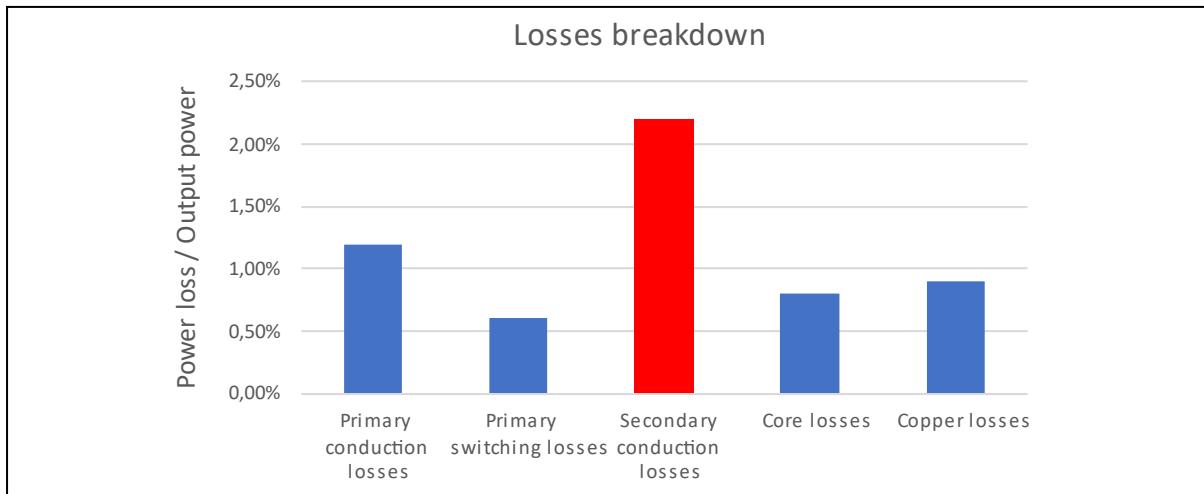
The loss of efficiency due to the secondary rectification can be easily estimated for any insulated converter. If  $V_{Rect}$  is the average forward drop across the secondary rectifiers during conduction and  $I_{out}$  is the dc (i.e., average) output current, the power output by the transformer is  $(V_{out} + V_{Rect}) \cdot I_{out}$ , while that delivered to the load is  $V_{out} \cdot I_{out}$ . If  $V_{Rect}$  was zero all the power output by the transformer would be delivered to the load and efficiency would be unity; instead, the power  $V_{Rect} \cdot I_{out}$  is dissipated in the rectifiers and the resulting efficiency of the rectification block is  $V_{out} / (V_{out} + V_{Rect})$ . Therefore, the efficiency loss caused by rectification is:

$$\Delta\eta = 1 - \frac{V_{out} I_{out}}{(V_{out} + V_{Rect}) I_{out}} = \frac{V_{Rect}}{V_{out} + V_{Rect}}, \quad (296)$$

which can be approximated with  $V_{Rect} / V_{out}$  if  $V_{out} \gg V_{Rect}$ .

With reference to the LLC converter, in the CT-FW rectification configuration it is  $V_{Rect} = V_F$ , in the SE-B rectification and voltage double configurations it is  $V_{Rect} = 2V_F$ , where  $V_F$  is the drop across a rectifier diode.

**Figure 152. Loss breakdown in a typical LLC design with diode rectification.**



Normally, Schottky diodes are selected because of their lower forward voltage drop that, for physical limitations, cannot be reduced below approximately 0.3 V. Actually, Schottky rectifiers with an even lower voltage drop are available (OR-ing diodes) but their reverse leakage current is large enough to waste the benefit of a lower  $V_F$  and their use is not recommended.

To meet the demand of higher efficiency and higher power density, key to the reduction of size and weight especially in portable or handheld devices, in the late 1990s power designers began adopting Synchronous Rectification (SR), i.e., using MOSFETs in place of diodes to achieve the rectification function.

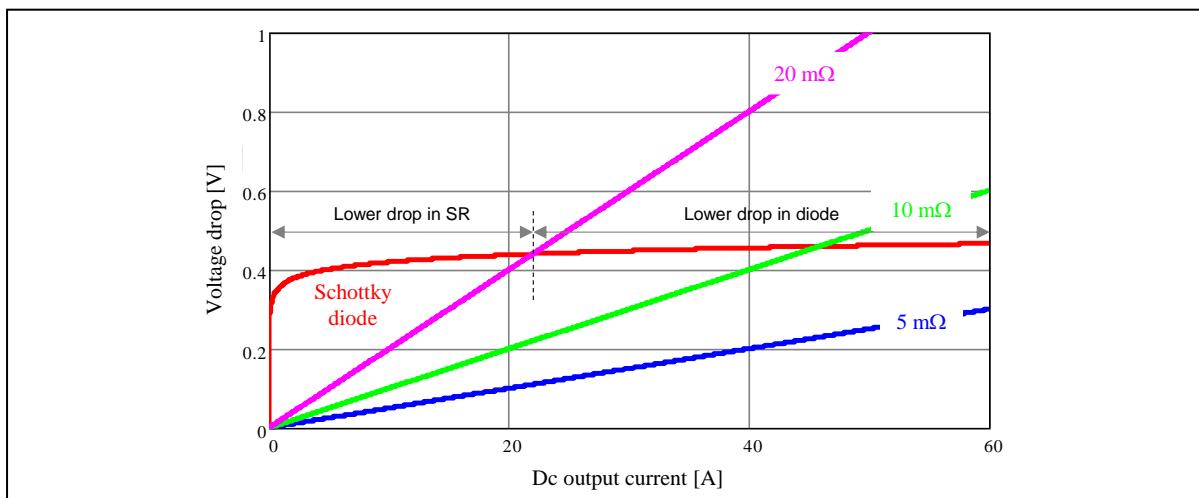
SR improves efficiency, reduces thermal performance requirements allowing higher power density, increasing reliability, and decreasing the Total Cost of Ownership (TCO) of power supply systems.

In fact, the on resistance,  $R_{DS(on)}$ , of MOSFETs can be lowered, either by increasing the die size or by paralleling multiple discrete devices to the point that the resulting  $V_{Rect}$  of MOSFETs can be significantly smaller than the  $V_F$  of a properly sized diode at a given current. This is shown in figure 153. Figure 154 shows the comparison of power losses. Diode losses are almost linear with the load, whereas MOSFET losses are parabolic, therefore, at a current high enough, diode losses can be lower, as shown in the plot on the left-hand side. Notice that the load level where SR losses equal diode losses is lower than that where voltage drops are equal: losses in diode depend on both the dc level and the rms level, those in SR MOSFETs depend on rms only.

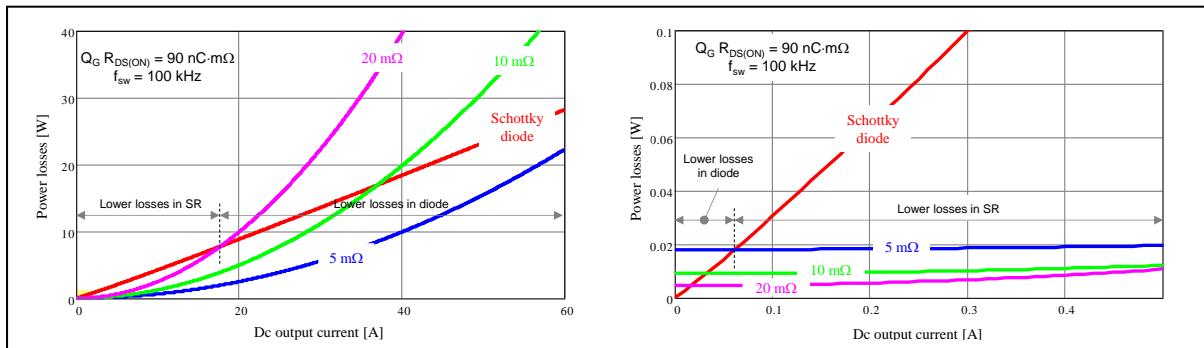
The use of MOSFETs brings additional losses due to the energy needed to drive their gate, however on the one hand MOSFETs generally work with soft switching so that they require less gate charge  $Q_G$  and driving energy, on the other hand MOSFET manufacturers have constantly introduced new technologies featuring lower  $R_{DS(on)}$  and total gate charge  $Q_G$ , which have made SR more and more advantageous. As shown in figure 154 on the right-hand side these driving losses are anyway a loss pedestal that at very low current make total SR losses higher than those in the diode. This suggests that at very light load it might be advantageous not to drive any more an SR MOSFET and let their body diode conduct.

Just to give a quantitative idea of a typical efficiency gain that SR can provide, it is useful to refer to Table 16, which shows the comparison of the efficiency of the same unit, the 240 W LLC converter specified in Table 12, with diode rectification and SR.

**Figure 153. Voltage drop of a 60 A Schottky diode vs SR MOSFET with various  $R_{DS(on)}$ .**



**Figure 154. Power losses in a 60 A Schottky diode vs SR MOSFET with various  $R_{DS(on)}$ : full range (left), zoom at low current range (right).**



**Table 16. Efficiency comparison @ Vin = 400 V for the 240 W PSU specified in Table 12.**

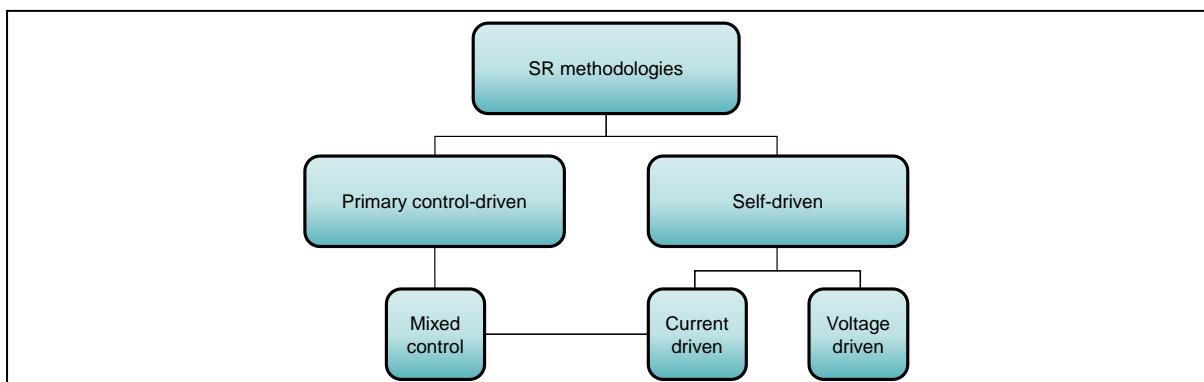
	Vout [V]	Iout [A]	Pout [W]	Pin [W]	$\eta$ (%)
<b>SR MOSFET</b> <b>(2.5 mΩ, 40 V)</b>	11.98	19.23	230.37	242.50	95.00
	11.99	10.00	119.90	127.10	94.33
<b>Schottky diode</b> <b>(2 // 20 A, 40 V)</b>	11.98	19.23	230.37	249.70	92.26
	11.99	10.00	119.90	130.45	91.91

At full load there is an increase of 2.74% that becomes +2.42% at 50% load. It is worth noticing that a reduction of the power dissipated in the secondary rectifiers means a lower power processed by the transformer that, in turn, causes a slight reduction of the losses on the primary side.

The use of MOSFETs, in addition to the previously mentioned benefits, also brings some issues. Of course, the need for controlling the SR MOSFETs increases the circuital complexity but this is amply compensated by the benefits. The biggest issue in SR is that it creates for the secondary current the possibility to reverse in case of improper driving, which is something that does not happen with diodes. Since MOSFETs are bidirectional devices, if they are erroneously turned on in a time interval when a diode in their place would be reverse biased, the secondary current will reverse.

A significant reversal may disrupt converter's operation and lead to catastrophic failures but even a modest reverse current can be a source of troubles because a SR MOSFET turned off with a reverse current will be subject to large voltage spikes that may exceed its rating. In the end, current reversal is the enemy number one of SR and must be prevented at all costs.

**Figure 155. SR driving methods for isolated topologies: classification.**



Essentially all topologies, both non-isolated and isolated, can be synchronously rectified. In isolated topologies providing adequate gate drive signals with the right timing to the SRs, to make them emulate the behavior of a diode is more challenging.

As illustrated in figure 155, there are two fundamental types of driving techniques for SR MOSFETs of isolated topologies: self-driven and primary-control-driven SR.

The primary-control-driven method utilizes the PWM signal generated on the primary side to derive the gate drive signal for the SR MOSFET. This method requires an extra isolation circuit to transfer the timing signal or the gate drive directly to the secondary side and is applicable when the conduction timing of the secondary side is synchronized to the on and off timing of the primary side.

As regards LLC converters, this match in timing occurs only in a CCM mode operation. In case of a DCM mode, since MOSFETs conduct in both directions, the secondary current will reverse during the time interval where it is supposed to be zero. This method, therefore, is not recommended for LLC converters.

Self-driven SR can be done in two ways: voltage-driven and current-driven. Their basic principle is shown in figure 156 considering the example of a forward converter.

In the voltage-driven method the gate drive signals are taken from the secondary winding directly or from an auxiliary winding of the transformer, with just few external discrete parts or none at all in some fortunate cases.

The method is simple and low cost but is suitable for voltage-fed topologies with an inductive output filter, where the changes in the polarity of the secondary winding voltage are driven by the primary side. Besides, it works well when the secondary winding voltage is a square wave.

Coming to resonant converters, this method could be applicable to the LC parallel resonant converter (see figure 12 b)) or the series-parallel resonant converter (figure 13 a)). However, the sinusoidal shape of the secondary voltage waveform makes the driving voltage low at the beginning and the end of the conduction interval, causing higher conduction losses.

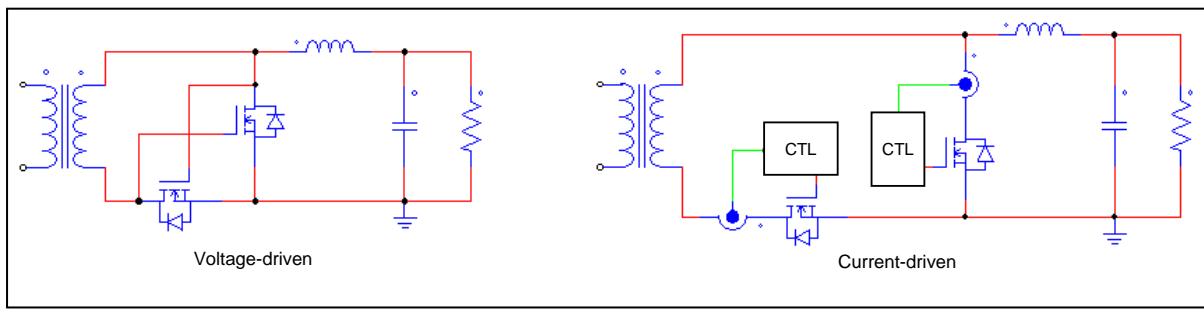
The voltage-driven method is not applicable to the LLC converter, which is a current-fed capacitor-loaded topology, where the polarity of the voltage on the secondary winding can change only after the SR MOSFET is turned off (as long as current is flowing on the secondary side, the voltage on the secondary winding is fixed at  $V_{out}$ ).

With the current-driven method the current flowing through the SR MOSFET is sensed and the information is processed by a control circuit to turn it on or off properly. The good point is that this method is applicable to any topology because a current-driven SR MOSFET can in principle really emulate a diode.

Sometimes it is possible to find SR control solutions that are a combination of the primary-control-driven method and the self-driving current-driven method. In this case, the information from the primary side is typically used to turn on the SR MOSFET and the current information to turn it off. This methodology also combines the complexity of the two approaches, so it is typically used when the conditions are such that a full self-driving current-driven method does not ensure reliable operation.

From now on, the discussion will focus on the self-driving current-driven method. The approach is apparently straightforward and perfectly matching the characteristics of the secondary currents in the LLC converter, which start from zero and go back to zero at the end of the conduction period. We will see that, instead, it poses challenges not easy to tackle.

**Figure 156. SR self-driving methods for isolated topologies: voltage-driven and current-driven.**



The most appropriate way to sense the SR MOSFET current is by using a current transformer, but in an LLC converter we need two of them, which has a not negligible impact on PCB real-estate, power losses and cost. For this reason, using the  $R_{DS(on)}$  of the SR MOSFET in the on state as a sense resistor has become an industry standard current sensing method for SR control, available in many commercial ICs (and not only for LLC converters).

This solution is successful despite its accuracy and reliability are highly affected by several adverse factors. It is not only the tolerance and the temperature dependence of the  $R_{DS(on)}$  of the SR MOSFET that come into play but also its package and the layout of the printed circuit board (PCB).

Last but not least, the fact that the control operates on signals in the mV range that live together with gate driving pulsed currents and secondary currents of several amperes makes its implementation in a control IC all but simple.

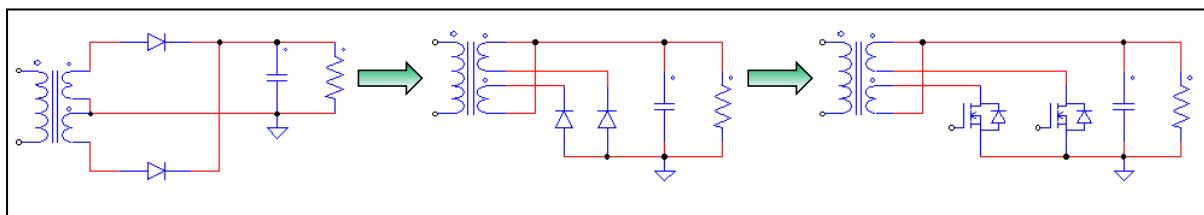
#### *SR configurations in LLC converters*

As seen in Part II, Chapter 1, the rectifier block in LLC converters can be configured as either a full-wave rectifier, which needs a center tap arrangement of transformer's secondary winding (CT-FW configuration) or as a bridge rectifier, in which case tapping is not needed (SE-B configuration).

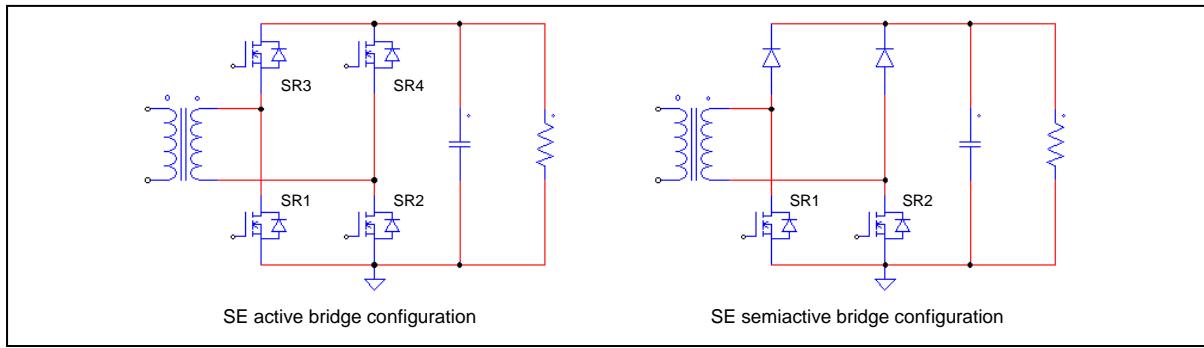
It is worth reminding that the first option is preferable with a low voltage / high current output and the second option with a high voltage / low current output. In the latter case the rectifier block may be configured also as a voltage doubler (VD configuration).

In case of CT-FW configuration replacing diodes with MOSFETs needs a preliminary relocation of the rectifiers so that they can be driven ground-referenced. The steps of this modification are shown in figure 157: each rectifier is moved to the other side of each half-winding so that their anode is connected to ground, then they can be replaced by source-grounded SR MOSFETs that can be easily driven. Notice that the SR MOSFETs will normally work in the third quadrant, i.e., current will flow from the source to the drain.

**Figure 157. Rectifier relocation in CT-FW configuration for ground-referenced driving.**



**Figure 158. Synchronous SE-B rectifier configurations.**



In case of SE-B rectification, replacing all diodes with MOSFETs necessarily involves SR MOSFETs that need a floating driver. Sometimes an acceptable cost-performance tradeoff is represented by the so-called semi-active bridge, where only the two low-side diodes of the bridge are replaced by MOSFETs. Both solutions are shown in figure 158.

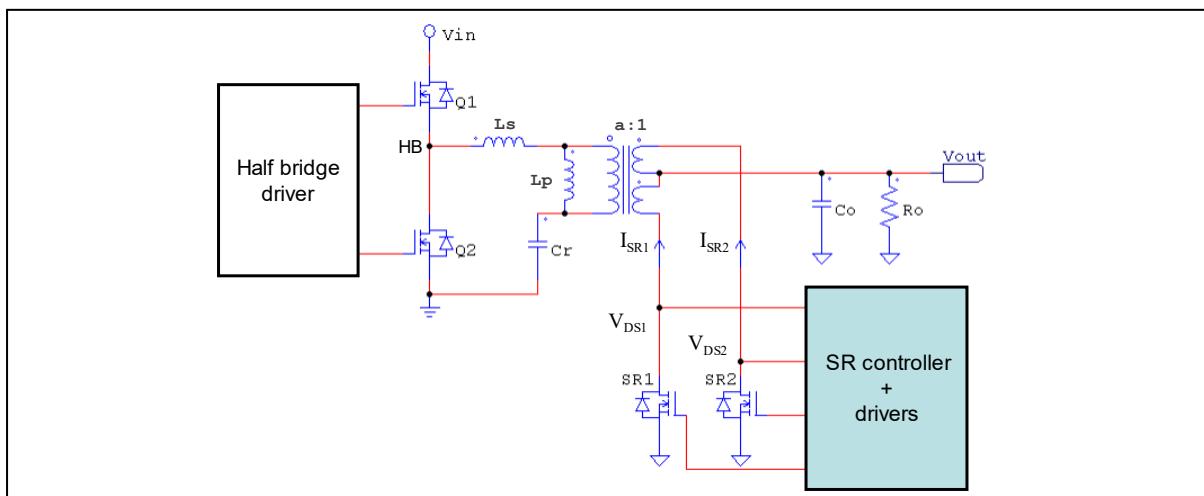
Of course, it is possible to synchronously rectify also the voltage doubler configuration, which essentially requires a half bridge leg. However, normally the voltage doubler configuration is used when the output voltage is very high, where synchronous rectification offers quite limited benefits, so it will not be taken into consideration.

Normally in the SE-B rectification the driving scheme of the four SR MOSFETs aims to emulate the behavior of the diode bridge, where the two diagonals conduct alternately: SR1 and SR4 are driven on and off simultaneously, like SR2 and SR3 but with opposite phase. In this case the control action can be exercised on the low-side MOSFETs only and the control requirements and solutions are not different from those of the CT-FW configuration.

With different driving schemes, where for example there are time intervals where SR1 and SR2 (SR3 and SR4) are both in the on state, or by properly shifting the driving signals of the primary side switches in a full bridge with respect to those of the SR MOSFETs it is possible to enhance some features of the converter or even provide bi-directional power flow capability. These aspects are beyond the scope of the present discussion and will not be considered.

In the end, we will concentrate the following discussion on the CT-FW configuration where the SR MOSFETs are controlled with the self-driving current-driven method, with the implicit assumption that all that will be said can be extended to the case of SE-B configuration as well.

**Figure 159. Synchronous CT-FW configuration (reference).**



The system we will refer to is illustrated in figure 159. Its operation can be simply described as composed by three phases that are equal for both secondary half windings:

1. The secondary current through either half winding ( $I_{S1}$  or  $I_{S2}$ ) starts flowing into the corresponding SR MOSFET body diode
2. The SR controller detects the diode conduction (drain-source voltage becomes slightly negative) and switches on the SR MOSFET; notice: this is a ZVS turn-on anyhow.
3. The SR controller detects that the current of the SR MOSFET in the on state is zeroing and switches it off.

To implement this ideal behavior, illustrated in figure 160, the SR controller will be provided with at least a pair of comparators. The first one will be referred to a slightly negative voltage  $V_{TH\_ON}$  and responsive to a negative-going edge of the drain voltage  $V_{DS}$  to detect the onset of the body diode conduction and drive the SR MOSFET on. The second comparator (Zero-current comparator, ZCC) will be referred to a negative voltage  $V_{TH\_OFF}$  very close to zero and responsive to a positive-going edge of the drain voltage  $V_{DS}$  to detect the zeroing of the current in the SR MOSFET and whose output is used to switch it off.

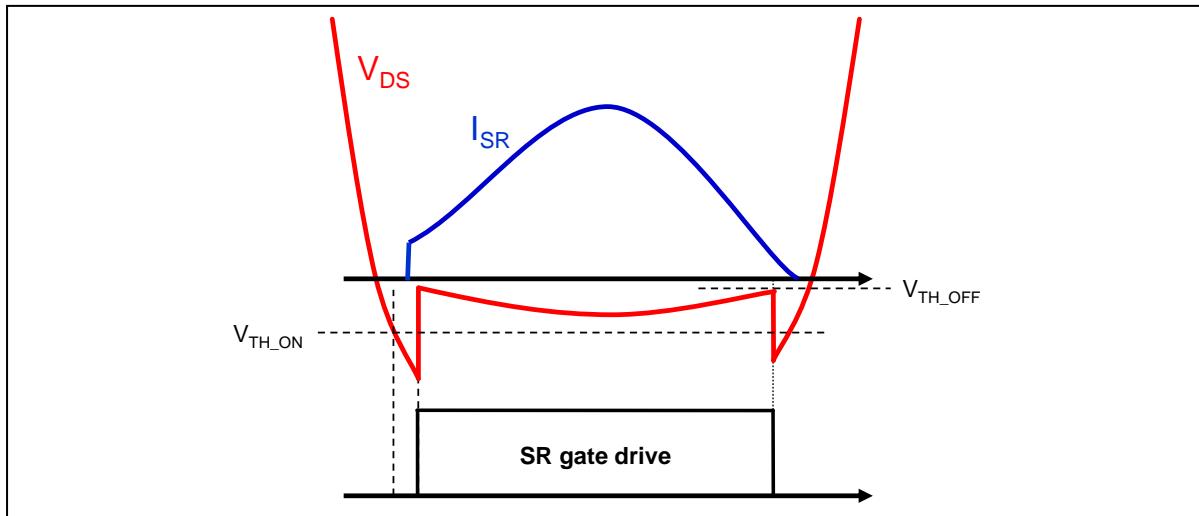
Before examining the challenges posed by the SR control in details, it is convenient to re-examine the shapes of the secondary currents under the various operating conditions that have been described in Part III, Chapter 1.

Figure 161 shows the typical secondary current in a half winding and the cathode-to-ground voltage across the rectifier (a diode), along with the gate drive waveform that the SR controller should generate.

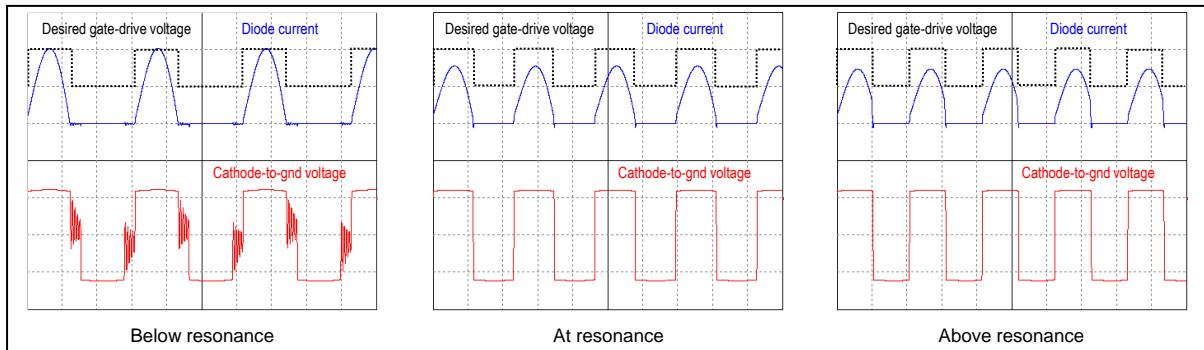
At turn-on, the secondary current shows a step-change that is smaller at resonance and below resonance, and a bit larger above resonance. This is due to the parasitic capacitance of the secondary rectifiers, which has been discussed in Part III, Chapter 1 and Part IV, Chapter 5 dealing with the feedback reversal phenomenon. This initial current causes the secondary rectifiers to lose exact ZCS at turn-on, but as long as the secondary current is large enough this initial current is embedded in the current generated by the normal energy transfer mechanism and does not pose any special problem to the SR control.

However, at light and very light load the superposition of the two contributions can even split, originating two distinct conduction intervals, as depicted in figure 162 that shows the same waveforms as in figure 161 with a progressively lower load from left to right.

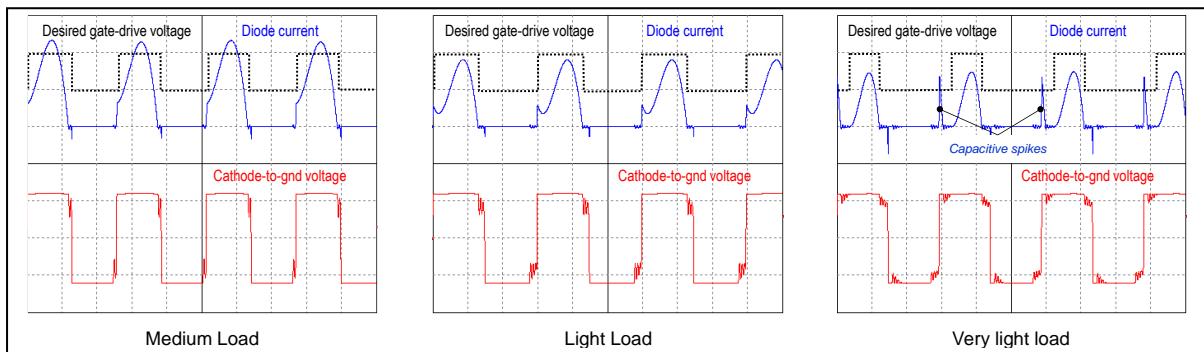
**Figure 160. Ideal behavior of a SR MOSFET in LLC converters.**



**Figure 161. Secondary-side current and voltage at full load in a half-winding of CT-FW.**



**Figure 162. Secondary-side current and voltage vs. load in a half-winding of CT-FW.**



ZCS at turn off is confirmed under all conditions. The most critical situation for the zero-current detection to turn off the SR MOSFET is above resonance, where the last portion has a very large  $di/dt$  thus requiring ultra-fast detection and turn-off.

#### *SR control challenges: SR MOSFET turn-on.*

Let us assume that the converter is operating at a load not too light, such that the waveform of the secondary current is like one of those shown in figure 161 or like the first two scope pictures from the left of figure 162.

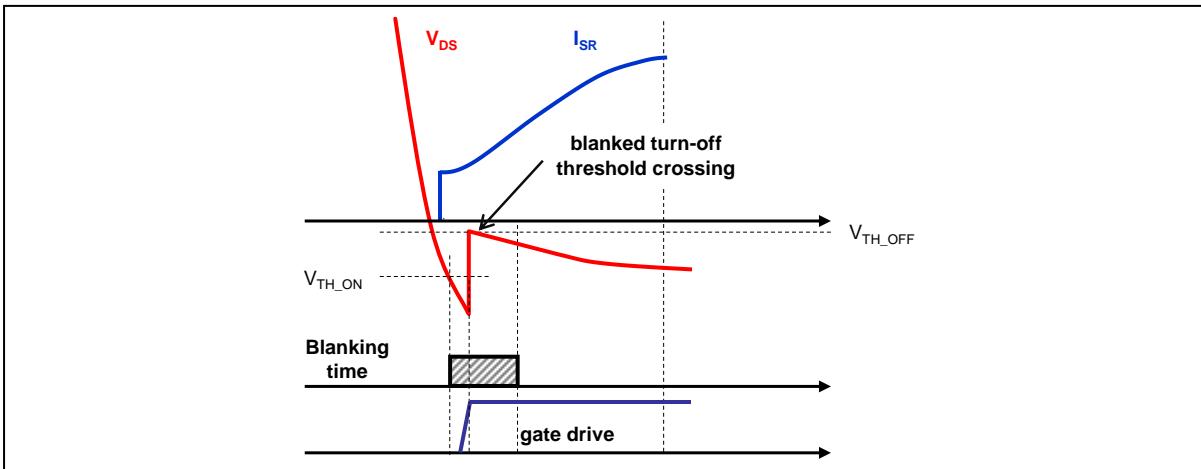
As mentioned earlier, the SR MOSFET should be turned on when  $V_{DS}$  becomes more negative than  $V_{TH\_ON}$ , a slightly negative threshold (e.g., -0.3 V), which denotes that body diode is about to conduct. However, as the SR MOSFET is turned on, its  $V_{DS}$  collapses from the drop  $-V_F$  of forward biased diode to a very low value ( $V_{DS(on)} = -I_{SR} \cdot R_{DS(on)}$ ) and this could be erroneously taken for current zeroing should this voltage exceed the turn-off threshold. This is quite likely because  $I_{SR}$  is initially small, and the SR MOSFET could be prematurely turned off.

To prevent this erroneous behavior the SR controller typically provides a blanking time during which the ZCC output is ignored, to let  $I_{SR}$  build up below the zero current detection threshold. This is illustrated in the time diagram of figure 163.

This blanking time is useful to filter the noise generated by the SR MOSFET turn-on too. This noise can be anyway minimized by using a gate driver with a low source current capability: in fact, the SR MOSFET is turned on with ZVS so there is no need to turn it on fast.

The blanking time determines a minimum on-time for the SR MOSFET; thus, its duration will be a tradeoff between preventing the SR MOSFET from misbehaving during normal operation and the need of turning it off as quickly as possible in case of an abnormal operating condition that causes the secondary current to reverse just after the beginning of the conduction period.

**Figure 163. SR controller operation at turn-on of SR MOSFET: turn-off blanking time.**



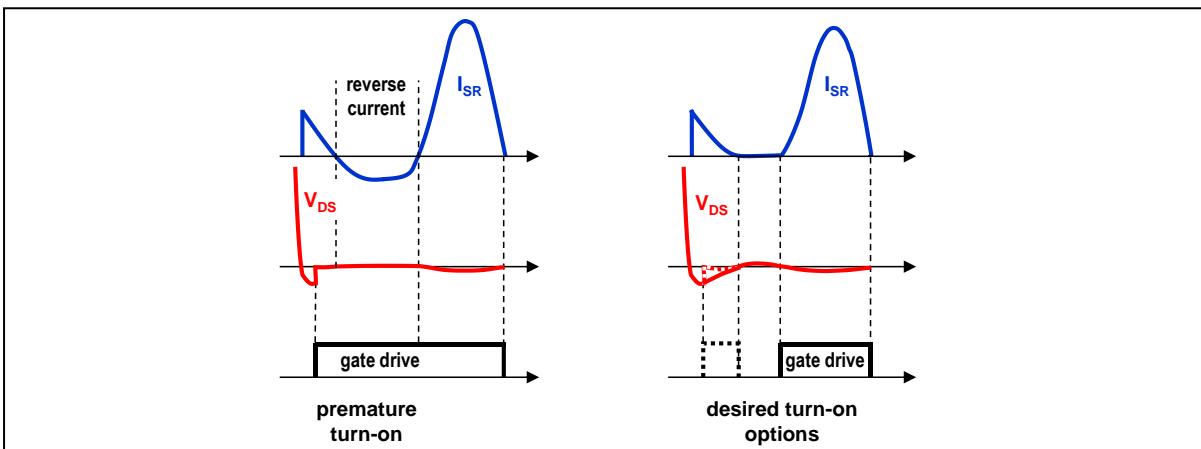
As visible in the rightmost oscillogram of figure 162, when the load is very light the initial non-conductive period of the DCMAB mode lasts longer than the duration of the initial current injection so that there are two distinct conduction intervals in a half-cycle. To be noticed also that the initial spike may have an amplitude comparable to that of the “main” conduction.

The initial current may prematurely turn-on the SR MOSFET, i.e., when the secondary voltage is not yet large enough to make it work in the third quadrant, as shown in the timing diagram of figure 164. Therefore, as the capacitive injection ends, the secondary current will reverse until the secondary voltage builds up to the point that the main conduction starts. This current reversal discharges the output capacitor acting as a sort of *dummy load*, which increases the rms current, lowers efficiency, and may induce the converter to oscillate.

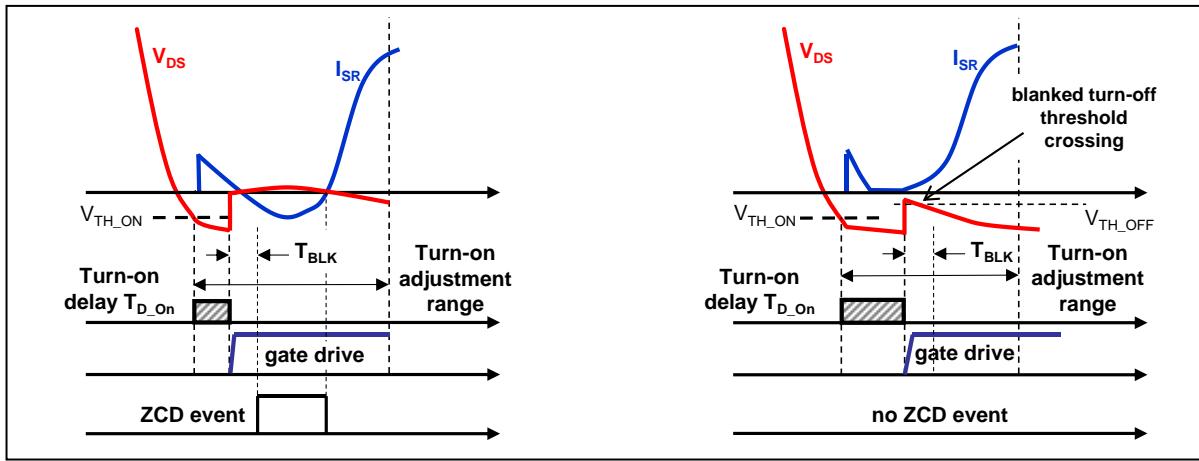
Ideally, either the turn-on should be delayed until the main conduction takes place or accept a dual turn-on/turn-off in a switching half-cycle. The first solution costs some power loss due to the flow of the initial current through the body diode, then with a much larger voltage drop, the second implies a waste of driving energy. Both solutions adversely affect the input power consumption, and the better option depends on the specific design.

An elegant implementation of the first solution is an adaptive control that automatically synchronizes the turn-on instant to the main conduction interval under essentially all operating conditions. Its operation can be described with the aid of figure 165 and includes the following steps that are equal for both secondary half windings:

**Figure 164. SR controller behavior at turn-on of SR MOSFET with a very light load.**



**Figure 165. Principle of adaptive turn-on delay.**



1. When the drain-source voltage  $V_{DS}$  falls below the turn-on threshold  $V_{TH\_ON}$  the SR MOSFET is turned on after a certain delay  $T_{D\_On}$ . This delay is initially set at a certain point of the adjustment range, which is normally proportional to duration of a switching half-cycle.
2. After a blanking time  $T_{BLK}$  following turn-on (to prevent a premature turn-off), if current reversal is detected (ZCD event), the delay  $T_{D\_On}$  is increased in the next conduction half cycle, otherwise it is unchanged.
3. If no current reversal occurs in a fixed number of consecutive switching cycles, the delay  $T_{D\_On}$  is decreased in the next conduction half cycle to check if conditions have changed and a shorter  $T_{D\_On}$  is sufficient to prevent current reversal.

This functionality, with slight variations, can be found in several commercial ICs.

#### *SR control challenges: SR MOSFET turn-off*

Despite the secondary rectifiers always turn off with ZCS, generating the proper timing of SR MOSFET turn-off is far from being trivial, rather it is probably the most challenging aspect of SR control.

On the one hand, the SR MOSFET must be turned off before the secondary current reverses to prevent all the troubles that even a slight current reversal causes. On the other hand, if the SR MOSFET is turned off too early, current will go on flowing through the body diode, then with a much higher voltage drop and, consequently, much higher power. This will significantly hurt efficiency, so the residual conduction time, if any, should be as short as possible.

Fulfilling both requirements under all static and dynamic operating conditions is the challenge, which is made sharper by the non-monotonic shape of the secondary current waveform.

As previously said, in principle the matter is quite simple: since we are sensing the drain source voltage,  $V_{DS(on)} = -I_{SR}R_{DS(on)}$ , a comparator referred to a negative voltage very close to zero and responsive to a positive-going edge of the drain voltage (ZCC) will serve the purpose of detecting the zeroing of the current. However, there are several issues that need to be addressed.

A first issue is represented by the accuracy of the turn-off threshold  $V_{TH\_OFF}$ : its value is in the mV, the same order of magnitude as the input offset voltage of a real-world comparator, which can therefore be the biggest source of inaccuracy. The input offset can be reduced by

making the input differential pair physically bigger, but this slows down the response of the ZCC, and here we need to be very fast in detecting the zero-current condition and turning off the SR MOSFET (typically less than 30 ns). Techniques such as chopper amplifiers, autozeroing or other offset cancellation techniques can be utilized to reduce the input offset to levels that have a minor impact on the threshold accuracy.

A second issue is the ZCC propagation delay and its dispersion, i.e., its dependence on temperature, slope of the input signal and overdrive (no common-mode dependence in this case, since the comparator is essentially referred to zero). Special circuit configurations and design techniques are necessary to achieve a very fast comparator with low propagation delay dispersion because the ZCC is required to work with a very small input signal, then with a very small slope, and tiny overdrive.

As to the gate driver, whereas a low source capability is required to turn the SR MOSFET on, a much larger sink capability (several Amps) is needed to turn the SR MOSFET off as quickly as possible. Additionally, also its propagation delay must be very short (in the 10 ns) because it adds up to the propagation delay of the ZCC to determine the overall turn-off delay of the SR controller.

In addition to these implementation issues, there are a couple of system-level issues that need to be taken into consideration.

A first system-level issue can be easily solved: realistically, the SR MOSFET will be turned off slightly before its current zeroes, to have some safety margin against current reversal. Therefore, its  $V_{DS}$  will suddenly go from nearly zero to  $-V_F$  to let the residual current flow through the body diode of the SR MOSFET until it actually zeroes. The turn-on threshold  $V_{TH\_ON}$  will be definitely crossed but this must not cause the SR MOSFET to turn on again. Typically, either a blanking time after turn-off or an appropriate control logic can prevent an erroneous turn-on.

A second issue, the so-called *inductive early turn-off* illustrated in figure 166 along with its root cause, is much more difficult to solve and has been the topic of extensive research over the last fifteen years [67]-[75].

The intent of measuring the drop across the SR MOSFET  $R_{DS(on)}$  is deceived by the packaging of the SR. The stray inductance of the package (and the PCB traces if the layout is not well optimized), makes the sensed drain-source voltage  $V_{DS}$  differ from the drop  $V_{ON}$  across  $R_{DS(on)}$ :

$$V_{DS}(t) = R_{DS(on)} I_{SR}(t) + L_{stray} \frac{dI_{SR}(t)}{dt}, \quad (297)$$

where  $L_{stray} = L_{source} + L_{drain} + L_{trace}$ . Therefore, in the final part of the half-cycle, where  $dI_{SR}(t)/dt$  is negative, the drop on  $L_{stray}$  is negative and the sensed voltage  $V_{DS}$  is smaller than  $V_{ON}$ . As a result,  $V_{DS}$  will cross the turn-off threshold  $V_{TH\_OFF}$  well before  $V_{ON}$  would do, causing the SR MOSFET to turn off when  $I_{SR}$  is still well above zero.  $I_{SR}$  will go on flowing through the body diode until zeroing, but the higher voltage drop will significantly hurt efficiency.

Considering that  $V_{TH\_OFF}$  is so small that it can be considered zero, the leading time  $T_{LEAD}$  shown in figure 166 i.e., how much earlier the SR MOSFET turns off with respect to the actual zero of the secondary current, can be estimated with the following formula:

$$T_{LEAD} = \frac{1}{2\pi f_{sw}} \tan^{-1} \left( 2\pi f_{sw} \frac{L_{stray}}{R_{DS(on)}} \right). \quad (298)$$

$L_{stray}$  and  $R_{DS(on)}$  are the parameters of a lossy inductor representing the SR MOSFET in the on-state and the argument of the  $\tan^{-1}$  function can be regarded as the quality factor  $Q$  of this inductor.

The plot on the left-hand side of figure 167 shows the plot of the normalized  $T_{lead}$  ( $2 T_{LEAD} f_{sw}$ ) given by (238) as a function of  $f_{sw}$  for different values of the ratio  $L_{stray}/R_{DS(on)}$ , where  $R_{DS(on)}$  is fixed at  $10 \text{ m}\Omega$  and the typical value associated to various packages is used for  $L_{stray}$ ; the plot on the right-hand side of figure 167 shows the plot of the normalized  $T_{LEAD}$  as a function of the quality factor  $Q$  of the lossy inductor representing the SR MOSFET in the on-state.

Note that if  $Q$  is sufficiently small, then  $\tan^{-1}(Q) \approx Q$ , therefore  $T_{LEAD}$  can be approximated by:

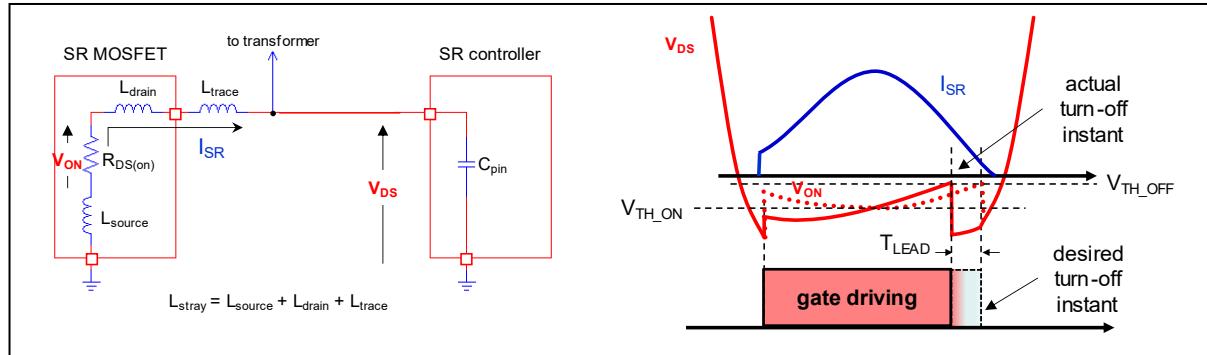
$$T_{LEAD} \approx \frac{L_{stray}}{R_{DS(on)}}. \quad (299)$$

This is represented in the plot on the right-hand side of figure 167 by the blue line. Eq. (299) provides an overestimate of  $T_{LEAD}$  not exceeding 10% as long as  $Q < 0.569$ .

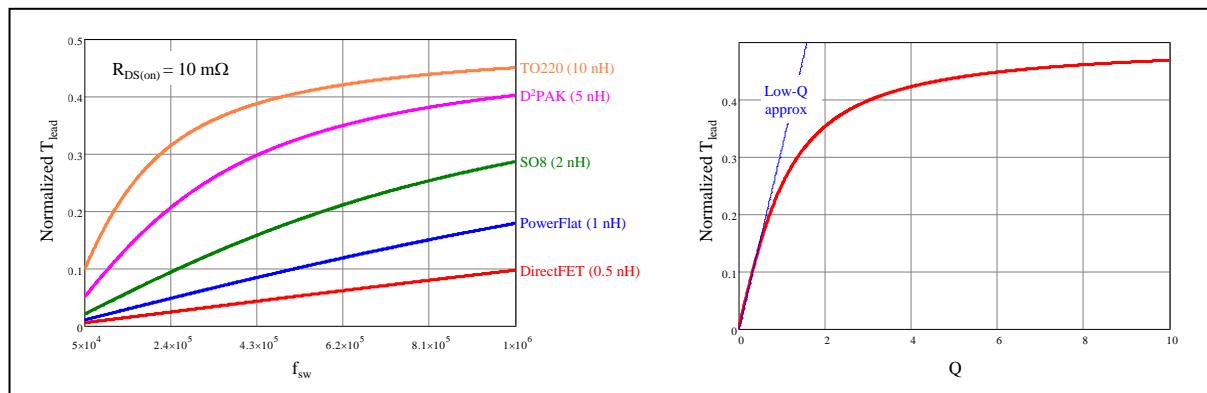
Therefore, for a given  $R_{DS(on)}$  the selection of the package is of crucial importance to determine the extent of the inductive early turn-off. The higher the switching frequency is, the more its stray inductance impacts on that. A package like the popular TO220 originates a significant  $T_{LEAD}$  even at low frequency, so it is inadequate for high frequency designs, where packages like DirectFET® or Powerflat™ are preferred.

For a given package i.e., for a given  $L_{stray}$ , the lower the  $R_{DS(on)}$  is the longer  $T_{LEAD}$  is, and this might limit the usage of very low  $R_{DS(on)}$  MOSFETs and create the need of a tradeoff.

**Figure 166. Inductive early turn-off: root cause (left), key waveforms (right).**



**Figure 167. Normalized  $T_{LEAD}$  vs. switching frequency  $f_{sw}$  for different packages (left); normalized  $T_{LEAD}$  vs.  $Q$  of  $L_{stray}$  lossy inductor.**



In any case, as much as the inductive early turn-off can be mitigated by appropriate design choices, normally it cannot be reduced to the point that its impact can be disregarded. Thus, it has become a common requirement for SR controllers to address this issue with the objective of making it negligible.

Now we will go through four of the most common strategies used in industry for minimizing the inductive early turn-off issue.

- Strategy one: RC compensation [72].

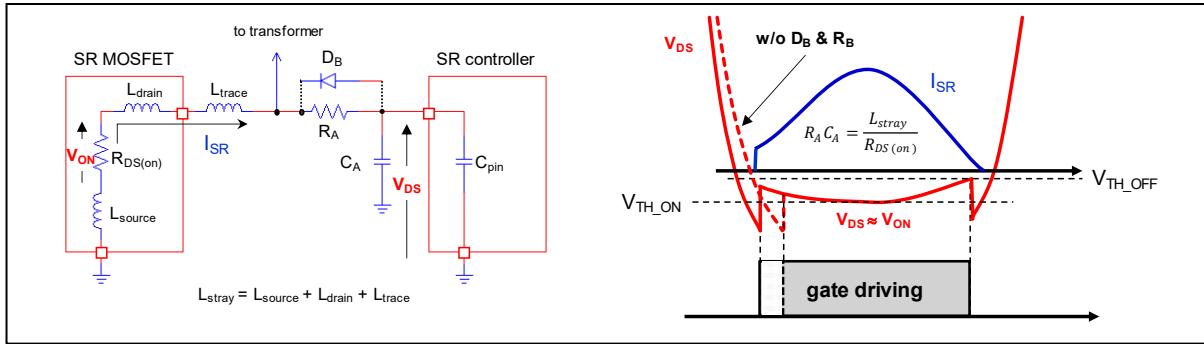
As illustrated in figure 168, the signal for the  $V_{DS}$  sensing input goes through an RC low-pass filter ( $R_A$ ,  $C_A$ ). As usual, the SR MOSFET is turned off when  $V_{DS}$  exceeds the turn-off threshold  $V_{TH\_OFF}$ .

If the time constant  $R_A C_A$  of the low pass filter equals the time constant associated to the lossy inductor,  $L_{stray}/R_{DS(on)}$ , the inductive early turn-off will be compensated.

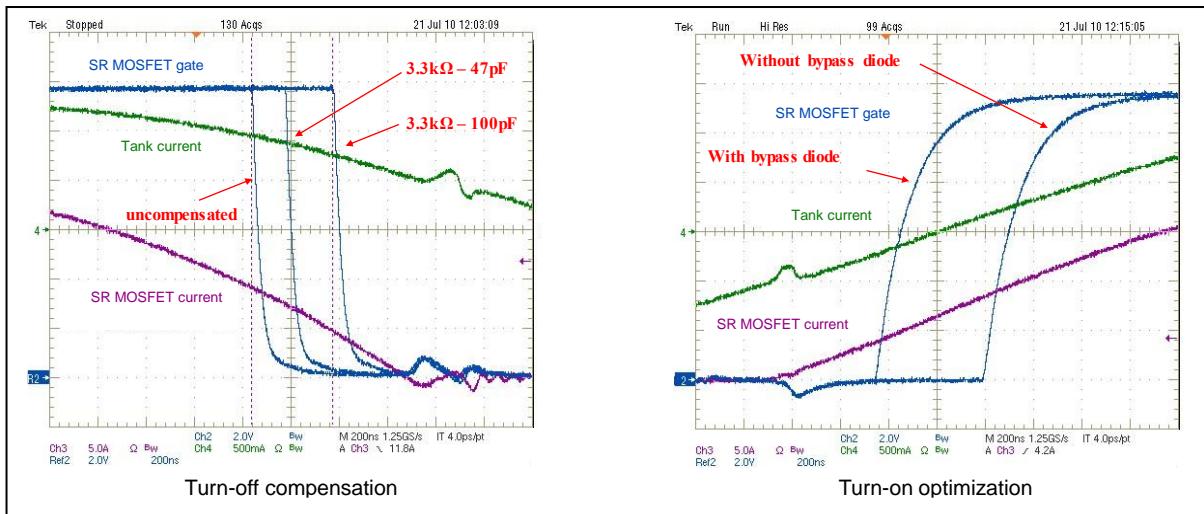
The tolerance of  $R_{DS(on)}$  and its changes with temperature limit the effectiveness of the compensation. Another shortcoming is that in practice the time constant needs to be tuned for the worst-case  $V_{DS}$  rate of rise, which occurs above resonance, where the last part of  $I_{SR}$  has a very high  $dI/dt$ . This means that at resonance and below resonance the inductive early turn-off will not be optimally compensated.

The simple addition of the RC low-pass filter delays not only the turn-off instant but also the turn-on instant because it delays and slows down the negative-going edge of  $V_{DS}$ , so that this will cross the turn-on threshold  $V_{TH\_ON}$  later.

**Figure 168. Inductive early turn-off compensation by RC circuit.**



**Figure 169. Inductive early turn-off compensation and turn-on optimization.**



This additional turn-on delay extends the duration of the conduction through the body diode, thus deteriorating efficiency. To minimize this additional delay a bypass diode  $R_B$  is backward connected in parallel to  $R_A$ . Its junction capacitance along with its low forward impedance will act as a speed-up.

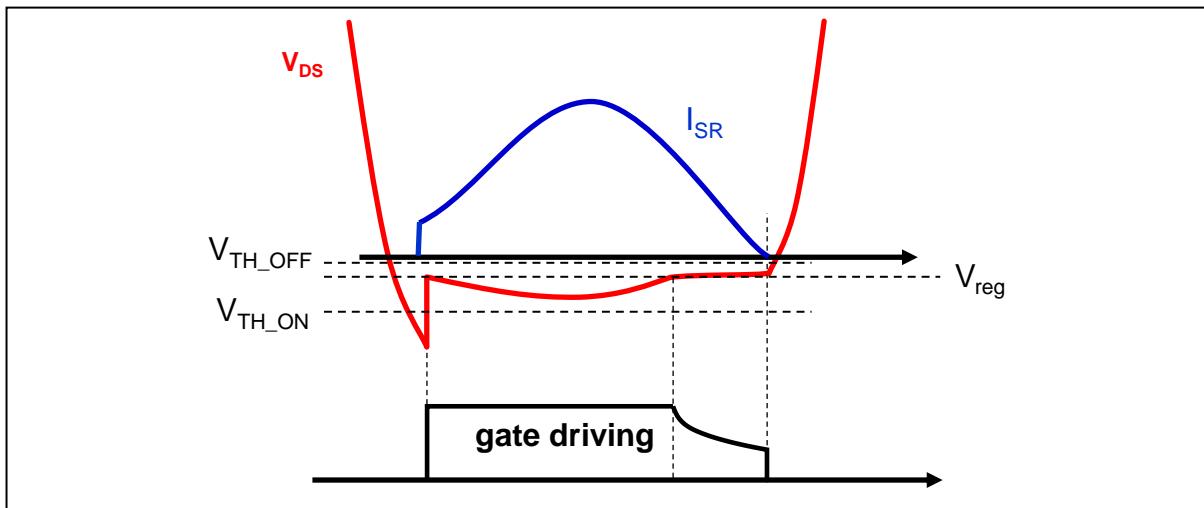
The oscilloscope plots of figure 169 show the effect of the RC compensation.

- Strategy two:  $V_{DS}$  regulation [76].

With this technique, depicted in figure 170, as  $V_{DS}$  exceeds a preset threshold  $V_{reg}$  (e.g., -30 mV), the gate-drive voltage is modulated to keep  $V_{DS} = V_{reg}$  until the gate-drive voltage falls below the gate threshold or the current zeroes, whichever occurs first. Usually a turn-off threshold  $V_{TH\_OFF}$  is provided anyway as a safety guard against current reversal. If  $V_{DS}$  exceeds  $V_{TH\_OFF}$  the gate of the SR MOSFET is quickly pulled to ground with a low impedance switch.

The principle behind this approach is that as current approaches zero and the gate-drive voltage approaches the threshold of the SR MOSFET, its  $R_{DS(on)}$  increases, thus  $T_{LEAD}$  is reduced, and the inductive early turn-off issue minimized. Additionally, the SR MOSFET can be switched off more quickly when current zeroes because the gate-drive voltage is close to the threshold.

**Figure 170.  $V_{DS}$  regulation principle.**



- Strategy three: adaptive turn-off [75].

The control algorithm, graphically illustrated in figure 171, minimizes the conduction time of SR MOSFET body diode after it turns off.

Leveraging the inductive early turn-off, a turn-off delay is initiated from the instant when the zero-crossing of  $V_{DS}$  is detected. This delay is updated cycle-by-cycle in small steps to obtain a body diode conduction time not exceeding a preset duration (e.g., 80 ns). Once the preset duration has been reached, the actual duration of the body diode conduction time jitters by one adjustment step around the target value.

This residual conduction time is a safety margin against current reversal in case of changes in the operating conditions.

A fast comparator referred to a slightly positive threshold prevents current reversal in case of fast transients.

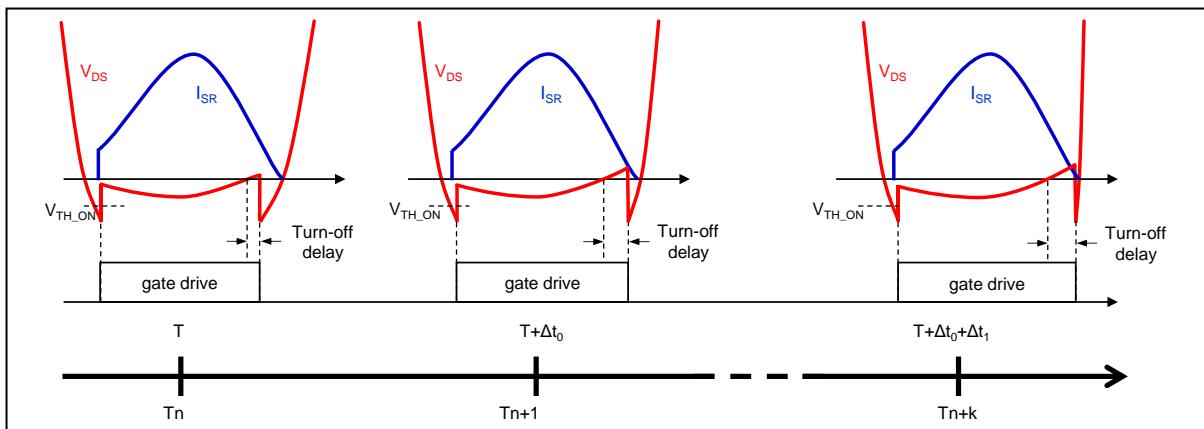
- Strategy four: Stray inductance compensation [77].

This technique considers an external compensation inductor  $L_{comp}$  (if its value is less than 10 nH, it can be realized with a PCB trace; rule of thumb:  $L_{trace} \approx 7 \text{ nH/cm}$ ), and a dedicated compensation input in the SR control IC, as shown in figure 172.

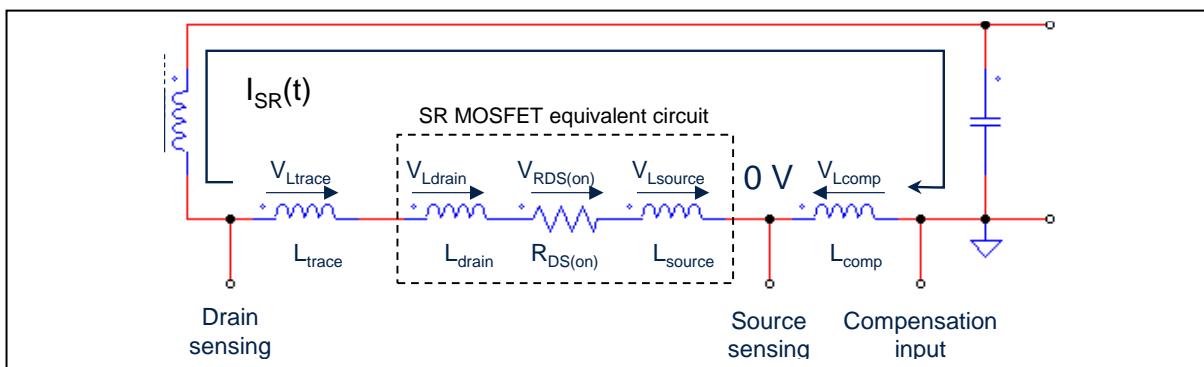
The source sensing input of the SR control IC represent the 0 V reference voltage; considering the direction of the secondary current  $I_{SR}(t)$  the voltage drops across  $L_{source}$ ,  $L_{drain}$ ,  $L_{trace}$  and  $R_{DS(on)}$  are conventionally negative, whereas the voltage drop across  $L_{comp}$  is positive. The voltage on the drain sensing input and that on the compensation input are internally summed and the resulting signal is compared to the turn-off threshold  $V_{TH\_OFF}$ .

If  $L_{comp} = L_{source} + L_{drain} + L_{trace}$ , the inductive drops are equal and cancel each other, so that the controller sees  $V_{RDS(on)}$  only.

**Figure 171. Adaptive turn-off principle.**



**Figure 172. Stray inductance compensation operating principle.**



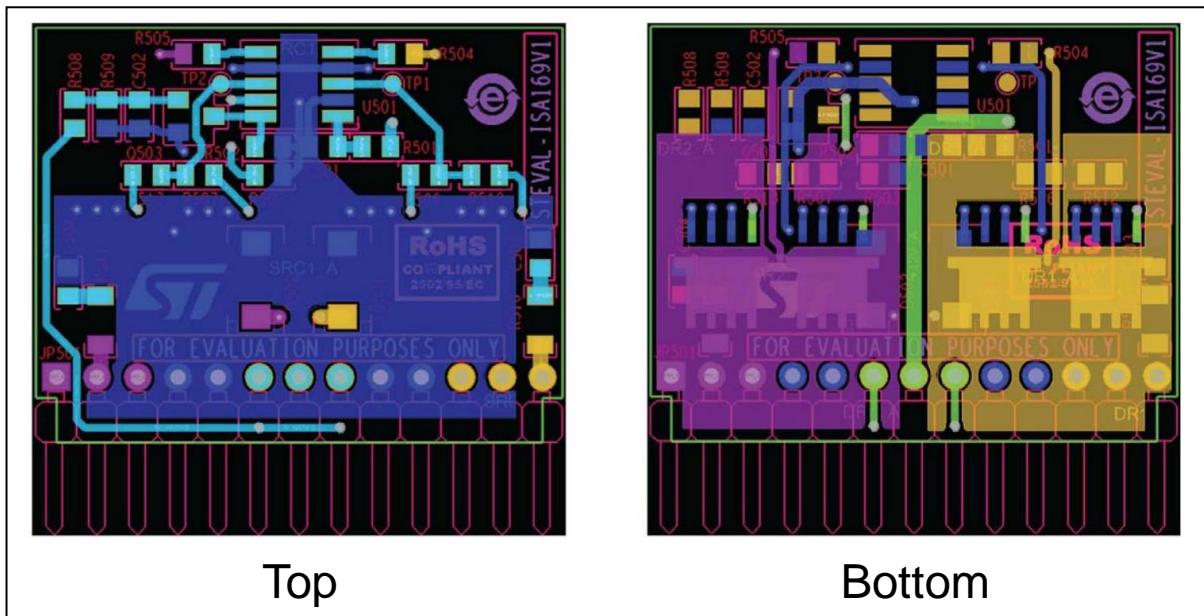
#### Printed circuit board layout hints

A proper PCB layout is essential for good operation of synchronous rectification. Here below a few hints that can help make a successful implementation. Figure 173 shows an example.

- Route the output current loop as short as possible by connecting the drain terminals of the SR MOSFETs as close as possible to the respective transformer “hot” terminations, and the source terminals close to the ground terminals of the output capacitor and as close as possible to one another. If the connection of the center tap to the positive terminals of the output capacitors cannot be short, consider bypassing it to ground with ceramic capacitors.

- Design the PCB and place the SR MOSFETs as more geometrically symmetrical as possible with respect to the transformer, to make circuit operation as much electrically symmetric as possible. This includes routing the connection between the drain of the two SR MOSFETs and the transformer terminals symmetrically to one another.
- Use “Kelvin sensing” to sense  $V_{DS}$ , placing the connections as physically close as possible to the drain and source terminals of the SR MOSFETs.
- Route the trace that connects MOSFET sources to the ground pin of the control IC as short as possible and separately from the load current return path.
- Use bypass ceramic capacitors between the supply pin and the ground pin of the IC, located as close to them as possible.
- If the control IC has the ground pin that carries both the return of the device bias current and that of the gate drive currents, this ground pin should be routed to the common point where the source terminals of both SR MOSFETs are connected.

**Figure 173. Exemplary PCB layout.**



## Chapter 2

# Interleaving of LLC resonant converters

Multiphase converters are a parallel combination of two or more switch-mode converters in any topology (typically the same for all), in a way that they share the same voltage source and provide power to the same load.

Multiphase converters are used when it is impossible or economically disadvantageous to comply with the design specifications with a single converter. The most common situation in which this approach is used is at a high power level: the total power demanded by the load is shared among a number  $N$  of converters, each one designed to carry  $1/N$  of the total.

Very often, in multiphase converters control methods are actuated that essentially consist in staggering the pulse trains that control each converter in an appropriate manner. This is what is typically called *interleaving*. More specifically, interleaving consists in separating the signals used to drive each stage at the same frequency by some phase difference, with the total phase on all signals equal to  $180^\circ$  or  $360^\circ$ , according to the topology and design purpose.

With interleaving it is possible to provide a multiphase converter with properties that the individual converter does not possess. Compared to single-phase converters, multiphase interleaved converters offer the following benefits:

1. Multiphase converters extend the obtainable power range. Single-phase converters work well up to certain amount of current, at higher currents power dissipation and efficiency start to become an issue. As previously mentioned, with an  $N$ -stage multiphase converter each individual stage manages  $1/N$  of the total power, which reduces each stage's current to more manageable levels.
2. Compared to a single-phase approach, in a multiphase converter the ripple current superposition at the input or the output results in a lower – sometimes theoretically zero - overall ripple and a lower ripple voltage across the input or output capacitors. The number of input or output capacitors and their ac ripple rating can be reduced.
3. The differential-mode input or output EMI filtering requirements decrease in a multiphase converter due to the reduced ripple current.
4. Compared to a single-phase converter carrying the total power, with the multiphase approach the size of the magnetic devices (inductor and transformers) is drastically reduced because of the lower rms current and saturation current requirements. The form factor of multiphase converters is generally better than that of a single converter carrying the same power
5. In multiphase converters the load transient performance can be improved: in the end a system of  $N$  interleaved converters, each operating at a frequency  $f_{sw}$ , behaves as a single converter working at a frequency  $N \cdot f_{sw}$ , then potentially faster to react.
6. In multiphase converters the efficiency can be kept very high on a broader load range resorting to the so-called *phase shedding*, i.e., shutting down the unnecessary phases when the load is low enough to be managed by a lower number of phases, and therefore reducing the losses associated to switching. For example, in a system of three interleaved converters, one can be shut down when the load is lower than  $2/3$  of

the full load, and a single converter can be left running when the load is lower than 1/3 of the full load.

Of course, the price to pay for these benefits is a greater system and control complexity, but this is normally worth the trouble.

It would be then very beneficial to adopt the multiphase approach in LLC converters too, especially when handling higher power levels (roughly,  $> 1 \text{ kW}$ ) or when there are special requirements on form factor or efficiency over a wide load range. In particular, LLC converters may benefit from using interleaving to reduce the output current ripple, which is one of their few drawbacks (refer to Table 1).

The bar chart in figure 174 shows the theoretical output ripple amplitude reduction as a function of the number of phases. Compared to a single-phase converter, with two phases the ripple amplitude becomes about 1/5, with three phases about 1/11. Increasing the number of phases, the ripple amplitude is reduced even further but the improvement becomes marginal while the system complexity and cost increase almost proportionally.

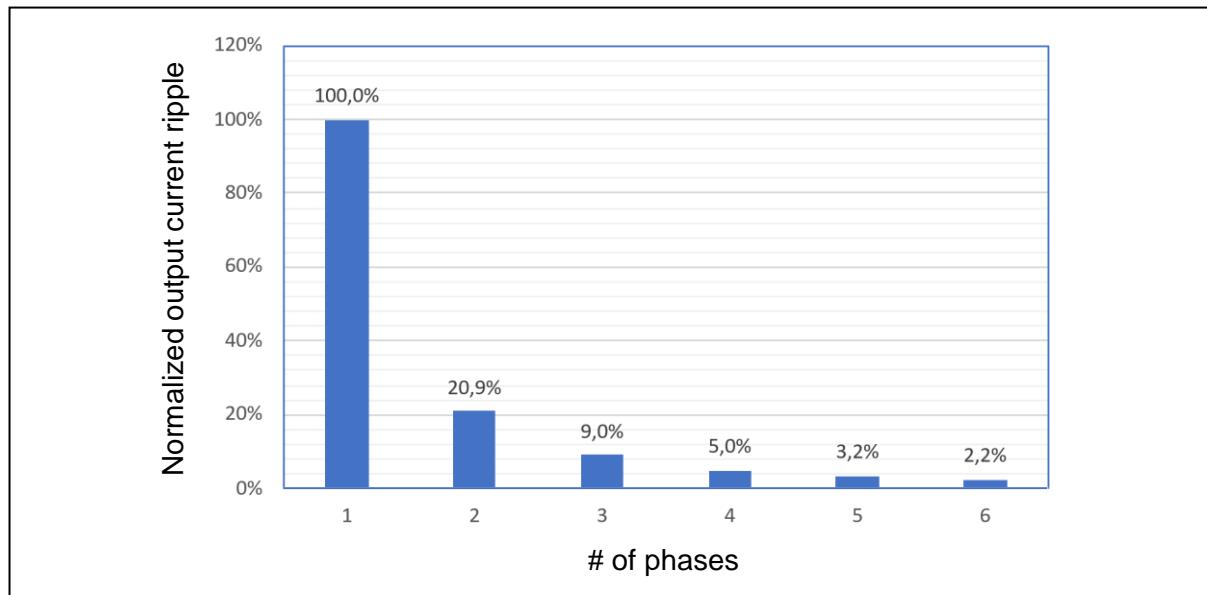
From the practical standpoint, special cases excluded, there is no point in going over 4 phases (which attenuate the ripple 20 times) and the majority of applications can be addressed with two and three phase interleaving.

While interleaving in PWM-controlled converters is relatively straightforward, this is not the case in resonant converter in general, and in LLC converters in particular. In fact, with the LLC converter *load sharing*, i.e., the capacity for the individual stages of equally sharing the current to be sourced to the load, is troublesome. This will be the focus of the discussion in this chapter.

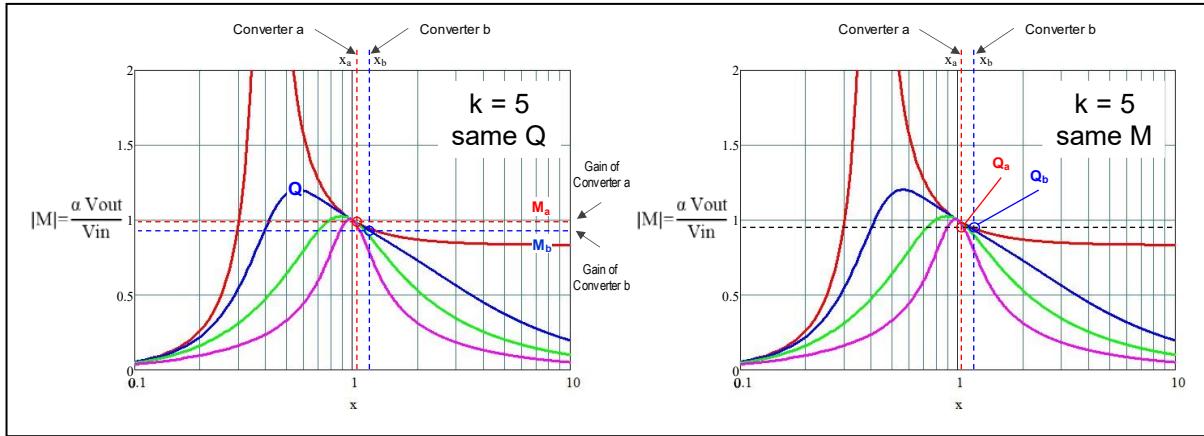
#### *Load sharing issue in interleaved LLC resonant converters*

Let us consider two nominally equal LLC converters that are paralleled with the intention of building a multiphase interleaved LLC converter. It is worth noticing that to meet this goal the output currents must be phase shifted by  $180^\circ$ ; however, considering the frequency doubling effect of the secondary rectification (the secondary current has a periodicity of a switching half-cycle), the PWM pulse trains driving the primary-side switches must be phase shifted by  $90^\circ$ .

**Figure 174. Output current ripple reduction in interleaved LLC converters vs. phase #.**



**Figure 175. Gain mismatch due to tolerance of tank circuits in LLC converters.**



Despite nominally equal, the actual values of the parameters of the two resonant tanks ( $L_s$ ,  $L_p$ ,  $C_r$ ) will not be the same, due to the tolerance of the physical components. Typically,  $L_s$  and  $L_p$  have 8-10% tolerance while  $C_r$  can be selected in a 5% tolerance series. Tighter tolerances entail a part selection (binning) to exclude those parts that are out of the desired tolerance band. This practice is typically not recommended in mass production because it is expensive and time consuming.

The effect of these tolerances is that the two tank circuits will have different resonance frequencies  $f_{R1}$ ,  $f_{R2}$ . It is possible to deduce the consequences of this difference based on the FHA model of the converters and using the plot of the voltage gain  $|M(x, k, Q)|$ . To do so, let us refer to the diagrams of figure 175 that illustrate the effects of the mismatch of  $f_{R1}$ ,  $f_{R2}$ , assuming for simplicity that the ratio  $k = L_p / L_s$  is unchanged.

Interleaved converters operated at the same frequency  $f_{sw}$  (they must be, to keep a fixed phase difference) have different normalized frequencies ( $x_a = f_{sw}/f_{R1a} \neq x_b = f_{sw}/f_{R1b}$ ), thus they have different dc gains  $M_a$ ,  $M_b$  if operated with the same  $Q$  (i.e., the same load), as shown in the  $|M|$  plot on the left-hand side. This violates the initial assumption of paralleled converters, which have the same input and output voltage.

Vice versa, if operated with the same voltage gain  $M$  as shown in the  $|M|$  plot on right-hand side, they have different  $Q$  values,  $Q_a$ ,  $Q_b$ . Consequently, the converter with a higher gain has a higher  $Q$  and delivers most power, the other may be even nearly unloaded.

For a better understanding of the issue, and with the aim of developing some design guidelines to help minimize the effects of the component tolerance on load sharing, it is interesting to analyze the impact of the tolerance of the individual components. This analysis is reported in [78] and can be synthesized in the following points:

- The mismatch of the upper resonance frequencies  $f_{R1a}$ ,  $f_{R1b}$  has by far the largest impact. The reason is the low output impedance in the vicinity of the upper resonance frequency, where the voltage gain is unity (load-independent point).
- The impact of the parallel inductances  $L_p_a$ ,  $L_p_b$  mismatch is small in the above resonance operation, more accentuated in the below resonance operation. This is consistent with the fact that the lower resonance frequency  $f_{R2}$ , which is associated to  $L_p$ , shows up in the below resonance operation only.
- The characteristic impedance mismatch (i.e., the mismatch of the  $L_s/C_r$  ratio) has a small impact under all operating conditions.

To get a quantitative idea, [78] reports that in a 2-phase interleaved LLC converter, assuming  $\pm 2.5\%$  tolerance of  $L_s$ ,  $L_p$ ,  $C_r$  (which is possible in mass production only using binning), the worst-case load sharing error is larger than  $\pm 20\%$  when operating at resonance at full load, and the sharing error gets even higher at lower output loads.

From a practical point of view, it is important to have a good load current sharing between phases when their mismatch degrades converter's characteristics or performance or cause significant stress or thermal differences that in the long run may cause reliability issues.

For example, unequal load sharing causes a larger output current ripple -see figure 176 - that, in turn, causes a larger output voltage ripple and an increase stress on the output capacitor bank. This means that load sharing is critical especially at heavy and intermediate load. In a system with phase shedding, good load sharing should be ensured down to a power level where a single phase remains active.

This high sensitivity of load sharing performance to component value mismatches prevents the use of multiphase interleaved LLC converters without some workaround. It is worth mentioning that power losses act as a balancing element and an analysis made taking them into account shows that load imbalance is smaller than one would expect using simpler ideal models. However, it makes little sense to denature the high efficiency property of the LLC converter to enable a better load sharing.

The question is then how to compensate for the resonant tank mismatch and force phases to share load current equally (current balancing).

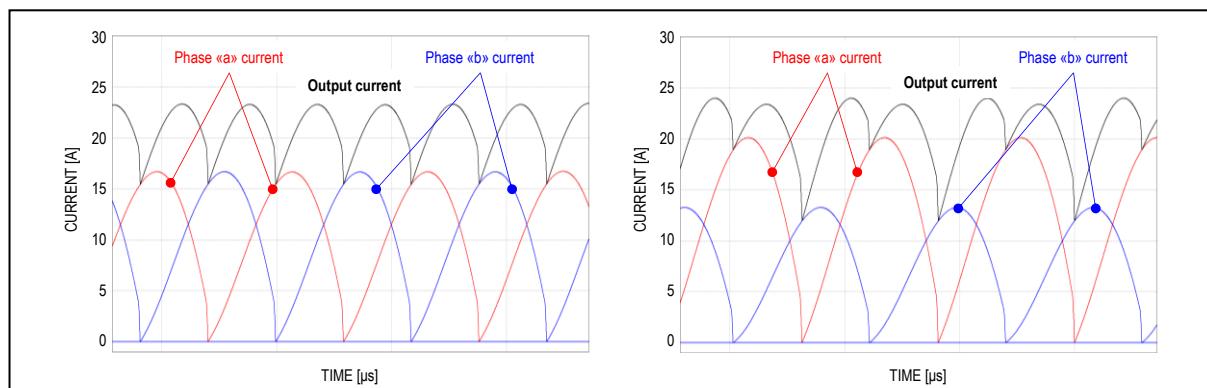
As previously mentioned, the frequency of the  $V_{HB}$  square wave applied to each tank current must remain the same for all phases, otherwise the superposition of the currents of each stage will continuously oscillate at the beating frequency. In principle the duty cycle of  $V_{HB}$  could be moved from 50% to increase converter's gain but doing so is not recommended because it will simply shift the problem elsewhere: from load current imbalance between phases to current imbalance in the two half-cycles of the duty-modulated converter.

We need an extra degree of freedom, like in a full bridge where the phase-shift of the two switching legs can be used to this purpose.

Considering 2-phase interleaved LLC half bridges, it is possible to mitigate the effects of mismatch with an appropriate design of the tank circuits (passive method). For a significant reduction of the effects of mismatch, one should consider some active method.

Considering 3-phase interleaved LLC half bridges, self-balancing topologies exist, and an example will be given in the following discussion.

**Figure 176. Secondary currents superposition in a 2-phase interleaved LLC converter: no mismatch (left), 2.5% mismatch of resonant capacitors (right).**



### Designing tank circuits for interleaving

To mitigate the effects of tank circuit mismatch on load sharing, the individual converters should be designed so that their dc gain does not change much in case of  $f_{R1}$  mismatch that, as stated in the previous section, is the major responsible for unequal load sharing.

In addition to that, it is intuitive that the more converters tend to behave as voltage sources, the more the effects of their mismatch increase: just think of what happens when trying to parallel voltage sources. Therefore, the individual converters should be designed to behave more as current sources i.e., designed for a higher output impedance  $|Z_{out}|$  and to be operated in a frequency region where the output impedance  $|Z_{out}|$  is higher. The FHA analysis can provide some insight.

Firstly, looking at the plot of  $|Z_{out}|$ , on the left-hand side of figure 177, the individual converters should not operate at resonance, where  $Z_{out}$  is theoretically zero (low in real-world operation).

Looking at the plot of  $|M|$ , on the right-hand side of figure 177, all  $|M|$  curves cross the load-independent point  $(1, 1)$  with a  $-2/k$  slope; around that point, curves with  $Q$  larger than a certain value (roughly corresponding to the blue curve) have a lower slope below resonance and a higher slope above resonance.

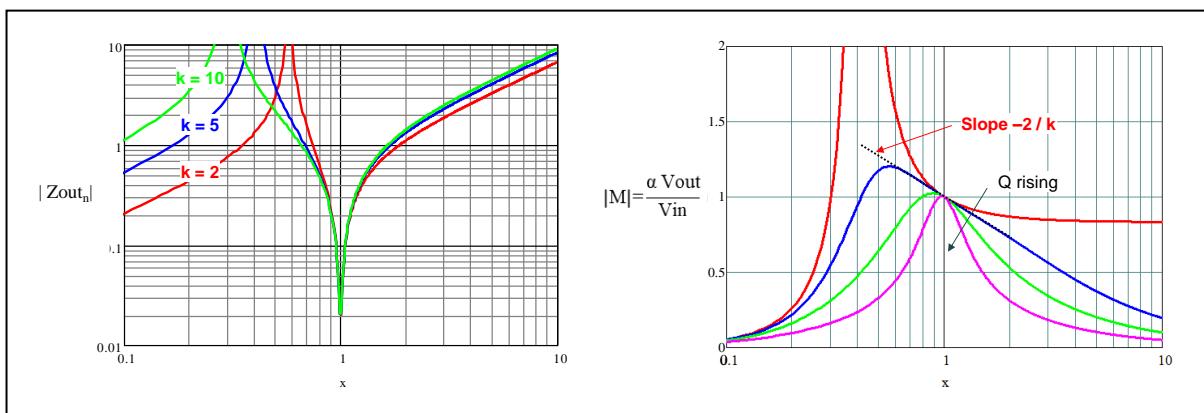
Therefore, based on these observations, the tank circuit should be designed according to the following three guidelines:

- To minimize the impact of  $f_{R1}$  mismatch, the tank circuit should be designed with a low  $|M|$  curve slope, then a high  $k = L_p/L_s$ , but with some care (see the last point).
- To achieve a higher  $|Z_{out}|$ , the tank circuit should be designed with a high characteristic impedance  $Z_0 = (L_s/C_r)^{1/2}$  (i.e., high  $L_s$ , low  $C_r$ ).
- Since  $Q = Z_0 / R_{ac}$ , a high  $Z_0$  implies a high  $Q$ ; to reduce the slope of the  $|M|$  curve with increasing  $Q$ , the converter must be operated below resonance. Notice that with higher  $k$  values the rate of rise of the output impedance  $|Z_{out}|$  with decreasing frequency in the below operating region gets smaller. Then  $k$  should be increased as long as the benefit of a lower slope of  $|M|$  prevails on the lower  $|Z_{out}|$  rate of rise.

This approach, however, has some significant shortcomings, specifically:

- Working away from resonance worsens efficiency in nominal conditions: operating always in DCMB mode below resonance involves a worse form factor of both the primary and secondary currents, leading to higher conduction losses.

**Figure 177.  $|Z_{out,n}|$  plot and  $|M|$  plot suggest design rules to mitigate mismatch effects.**



- Each converter will work closer to the capacitive mode region. Care must be taken to safely handle out of spec operating conditions (e.g., an input voltage lower than the minimum specified).
- Ultimately, the load current mismatch is mitigated but still significant; as a result, each converter must be designed for a power considerably larger than their theoretical share of the total power.

#### *Active interleaving in 2-phase interleaved LLC half bridge converters*

Several current balancing methods have been proposed to solve the load sharing issue. In this section some of them, referred to 2-phase systems, will be reviewed.

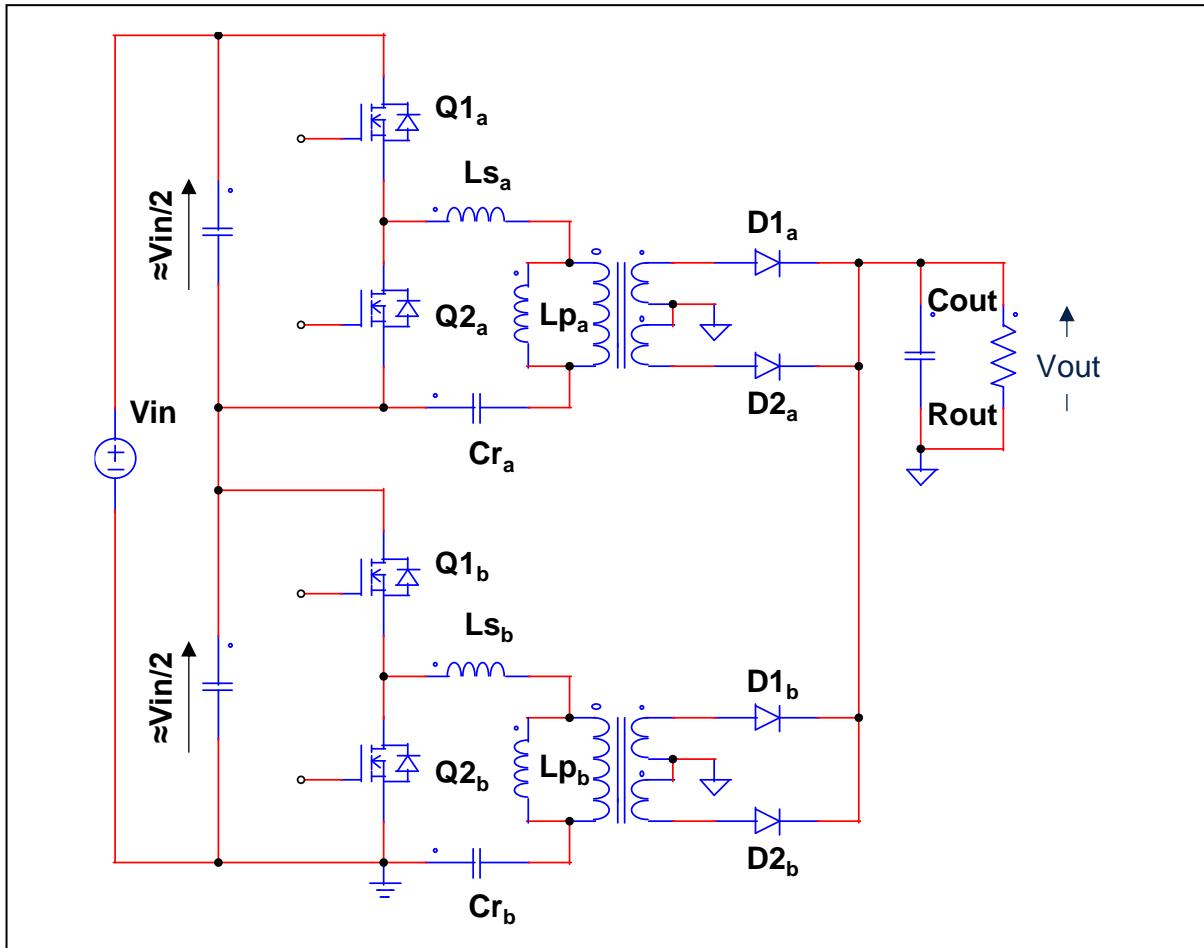
- Series-parallel connection [79], [80]

With this technique the input voltage is split by two capacitors and fed to the two phases connected in series. The outputs are connected in parallel, as shown in figure 178.

This arrangement provides intrinsic negative feedback that improves load sharing, though not fully equalizing the individual currents.

Its operating principle can be explained considering that, if one phase has a higher dc gain, that phase will provide more power and its input capacitor will be discharged more; the voltage on the capacitor of other stage will increase accordingly because the sum of the two voltages must equal  $V_{in}$ . This input voltage imbalance contrasts the dc gain mismatch, and the resulting load current mismatch will be reduced.

**Figure 178. Series-parallel connection of a 2-phase interleaved LLC converter.**



Unfortunately, this technique has a couple of non-negligible drawbacks. Firstly, the input voltage of the individual phases is halved, so the input current is doubled, as if it was a single-phase converter. Conduction losses will be higher, efficiency will be impaired. Secondly, phase shedding is not possible: in fact, if one phase is shut down there is no dc path for the input current. From a different angle, the negative feedback mechanism that tends to balance currents pushes the input capacitor voltage of the disabled phase (which carries no power) to the maximum ( $V_{in}$ ), discharging the completely the other, whose voltage goes to zero.

- Separate supply rails [78]

With this solution, illustrated in figure 179, each LLC converter is powered by a separate dc-link voltage generated by two separate PFC stages.

A current balancing loop adjusts the output voltage setpoint of one PFC stage (or both), so that  $I_{out_a}$  and  $I_{out_b}$  are equal:  $I_{out_a} = I_{out_b} = I_{out}/2$ .

The main drawback of this technique is the system complexity and cost. However, it is a viable solution in high power converters that use an interleaved PFC front-end. In this case there is no significant increase in complexity, but the ripple cancellation on the output bulk capacitor is lost. This is often acceptable because largely repaid by the benefit on the most stressed components, the output capacitors of the LLC converter.

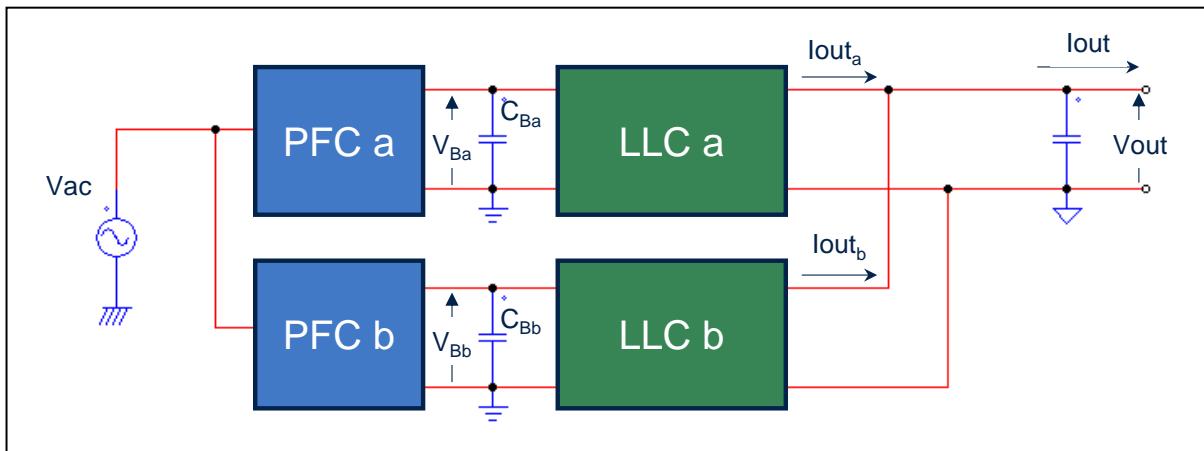
- Current-controlled inductor [81]

With this approach, as illustrated in figure 180, two additional inductors are added on the primary side: a fixed value inductor ( $L_F$ ) is in series to the tank circuit of one phase and a current-controlled inductor in series to the tank circuit of the other phase. The purpose of the variable inductor is to equalize the upper resonance frequencies of the two tank circuits and, ultimately, equalize the currents of each phase.

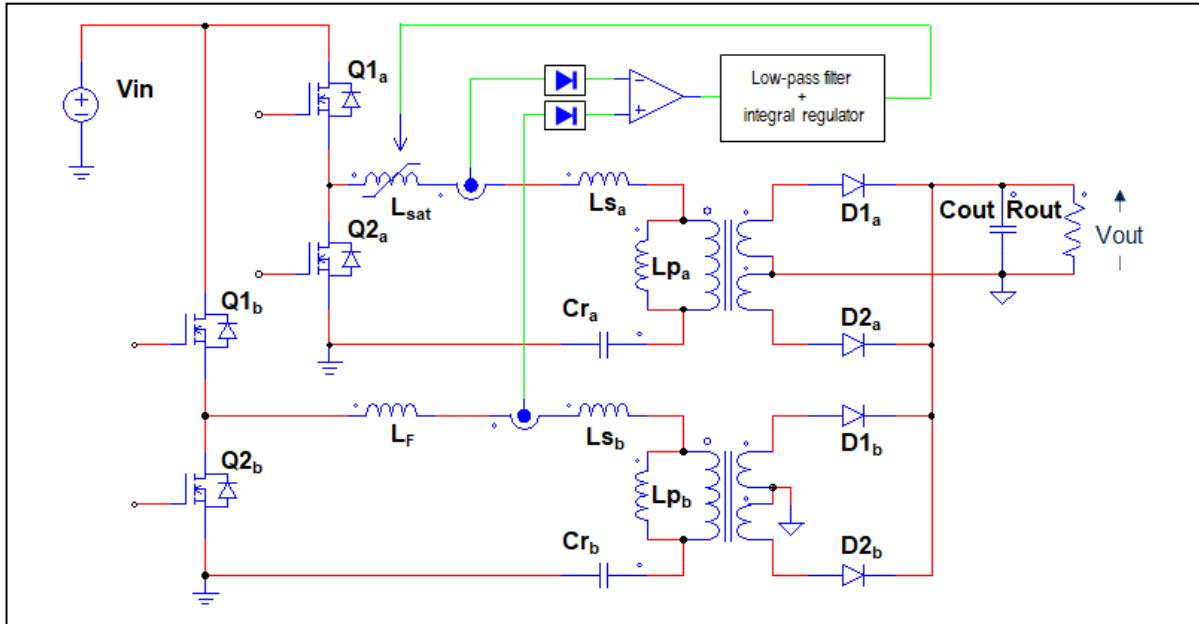
The variable inductor is built as conceptually illustrated in figure 181 (left). The  $N_L$  turns on the center post of the core are used to obtain  $L_{sat}$ , while two series-connected windings of  $N_S$  turns each wound on the outer legs of the core make the control winding that is used to modulate  $L_{sat}$ .

This modulation is achieved by forcing a dc-current (control current,  $I_{CTL}$ ) through the control winding. This causes the core to slightly saturate, therefore changing its effective magnetic permeability and thus modulating the value of  $L_{sat}$ : the higher  $I_{CTL}$  is, the lower  $L_{sat}$  will be, as shown in the plot on the right hand-side of figure 181.

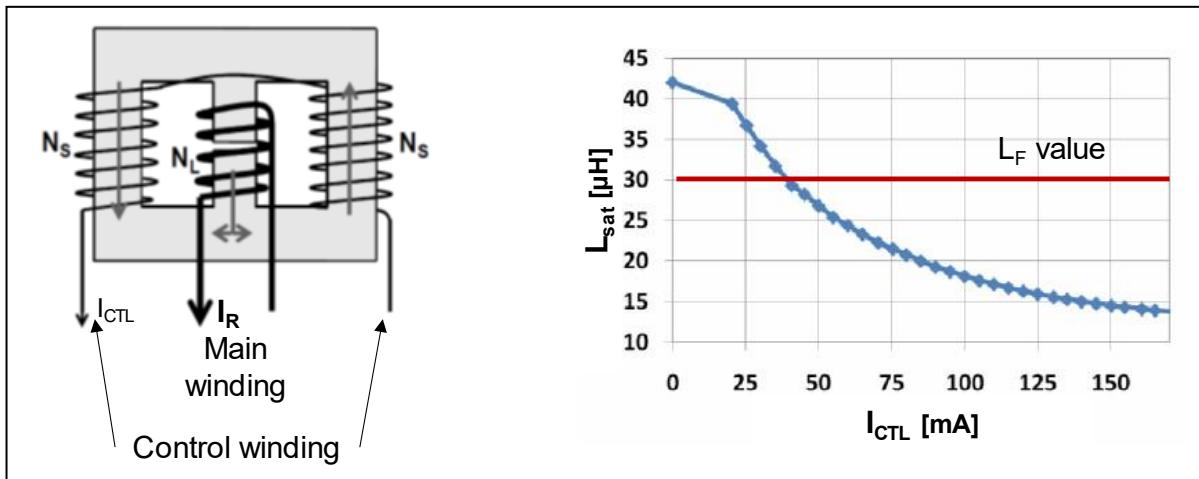
**Figure 179. Dual dc-link configuration of 2-phase interleaved LLC converter.**



**Figure 180. Load current balancing in a 2-phase interleaved LLC converter through a current-controlled inductor.**



**Figure 181. Current-controlled inductor and  $L_{sat}$  vs.  $I_{CTL}$  relationship.**



The adjustment of  $L_{sat}$  goes in one direction only, whereas it is necessary to adjust in both directions because the sign of the mismatch is not known. This requires the addition of the fixed inductor  $L_F$ , whose value will be chosen roughly in the middle of the adjustment range of  $L_{sat}$ . An alternative approach like purposely imbalance the leakage inductance of one transformer to predefined the needed adjustment direction, (i.e., embedding  $L_F$  in its leakage inductance) would require the use of different transformers for the two phases, which is not usually a recommended practice.

Though the system works effectively, the addition of two magnetic parts, as well as of the current balancing regulator, increases system cost and size.

One aspect needing attention is the power consumption associated to the current balancing regulator, which will degrade converter's efficiency. This can be minimized by using a large turns number  $N_s$  to reduce the amplitude of  $I_{CTL}$  and keeping the voltage source that produces  $I_{CTL}$  as small as possible.

Using phase shedding the controlled phase can be shut down at light load along with the current balancing regulator, which therefore will not affect light load efficiency.

Notice that in the system of figure 180, the current balancing loop is based on the comparison of the resonant tank currents of the two phases. This provides a good output current balancing as long as the magnetizing current is negligible compared to the total resonant current, i.e., at medium and heavy load. At light load the tolerance of  $L_p$  worsens current balancing significantly. To improve this behavior, the secondary currents should be sensed instead. Since in interleaved systems the output current is normally high, the introduction of additional losses due to sensing might be an issue. Additionally, in primary-controlled systems current sensors should transfer the signal from the secondary to the primary side, so they should guarantee safety isolation.

- Switch-controlled capacitor [82]

This approach, shown in figure 182, can be considered conceptually the dual one of the current-controlled inductor method: to match the upper resonance frequencies of the two tank circuits, the effective value of the resonant capacitor is modulated.

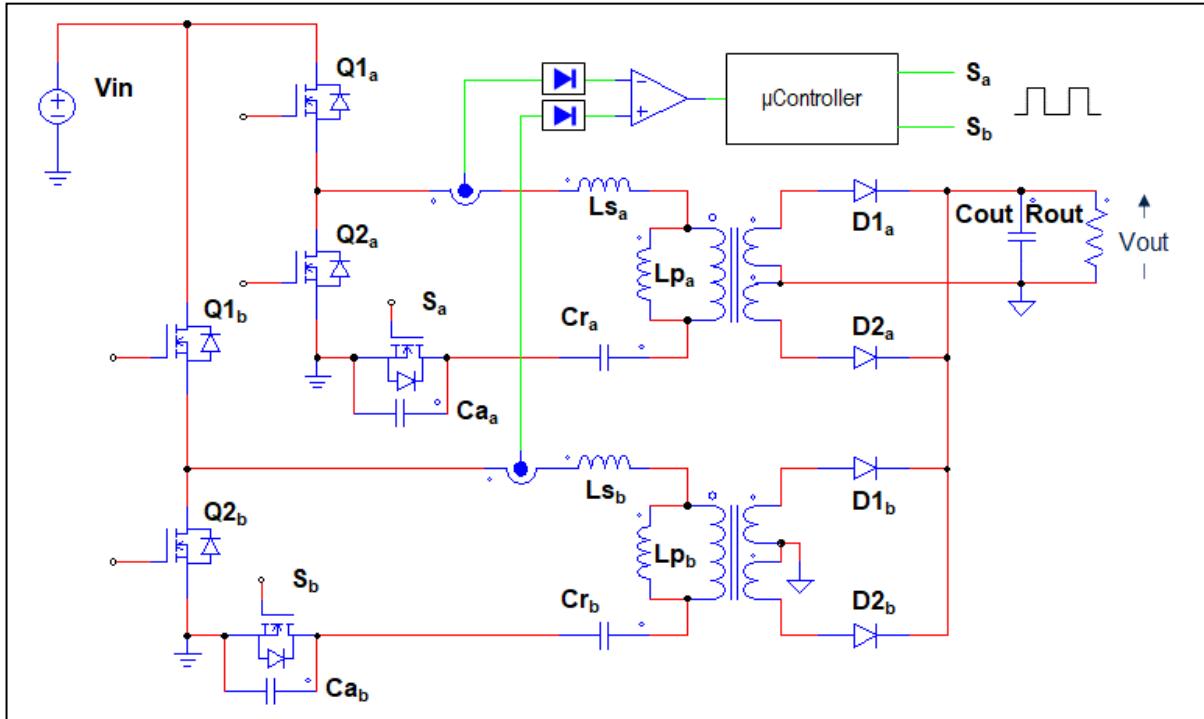
This is achieved by adding the capacitor  $C_a$  and changing its value by modulating the duty-cycle of the switches  $S_a, S_b$ . With reference to figure 183, a first harmonic analysis shows that the effective capacitance value,  $C_{a_e}$ , is a function of the control angle  $\alpha$ :

$$C_{a_e} = \frac{2 C_a}{2 - \frac{2\alpha - \sin 2\alpha}{\pi}}. \quad (300)$$

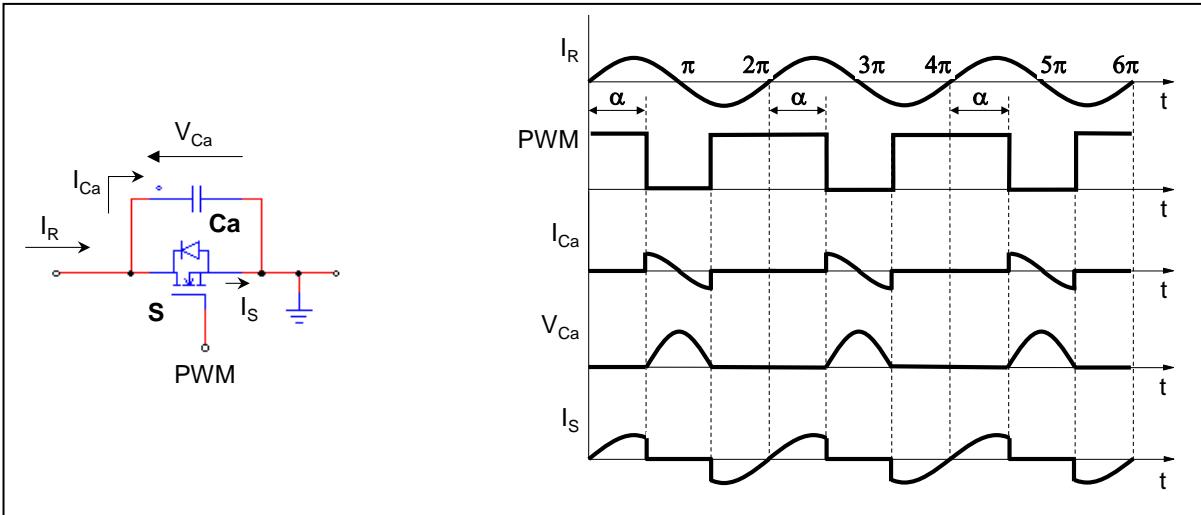
$C_{a_e}$  goes from  $C_a$  when  $\alpha = 0$ , i.e., when the switch  $S$  is always off to  $\infty$  (a short circuit can be assimilated to an infinite capacitance) when  $\alpha = \pi$ , i.e., when  $S$  is always on.

As a result, the overall resonance capacitor  $C_r$  goes from  $C_r$  when the switch  $S$  is always on, to the series combination of  $C_r$  and  $C_a$  when the switch  $S$  is always off.

**Figure 182. Load current balancing in a 2-phase interleaved LLC converter through switch-controlled capacitors.**



**Figure 183. Structure (left) and key waveforms (right) of a switch-controlled capacitor.**



Of course,  $C_a$  will be selected so as to cover all the necessary adjustment range. Normally, it needs to accommodate small variations, so its value is not much different from that of  $C_r$ , sometimes it is even larger. This is a favorable fact because the peak voltage across  $C_a$  will not be that high and lower voltage rating MOSFETs can be used as the switch  $S$ .

To minimize switching losses,  $S$  is operated with ZVS at turn-on:  $S$  is turned on when its drain-source voltage falls to zero after the positive peak.  $S$  is turned off when the control angle  $\alpha$  programmed by a current balancing loop has been reached. Notice that the angle  $\alpha$  is counted starting from a positive-going zero-crossing of the tank current. Digital control is practically a must.

#### *Three-phase interleaved LLC converters – an example*

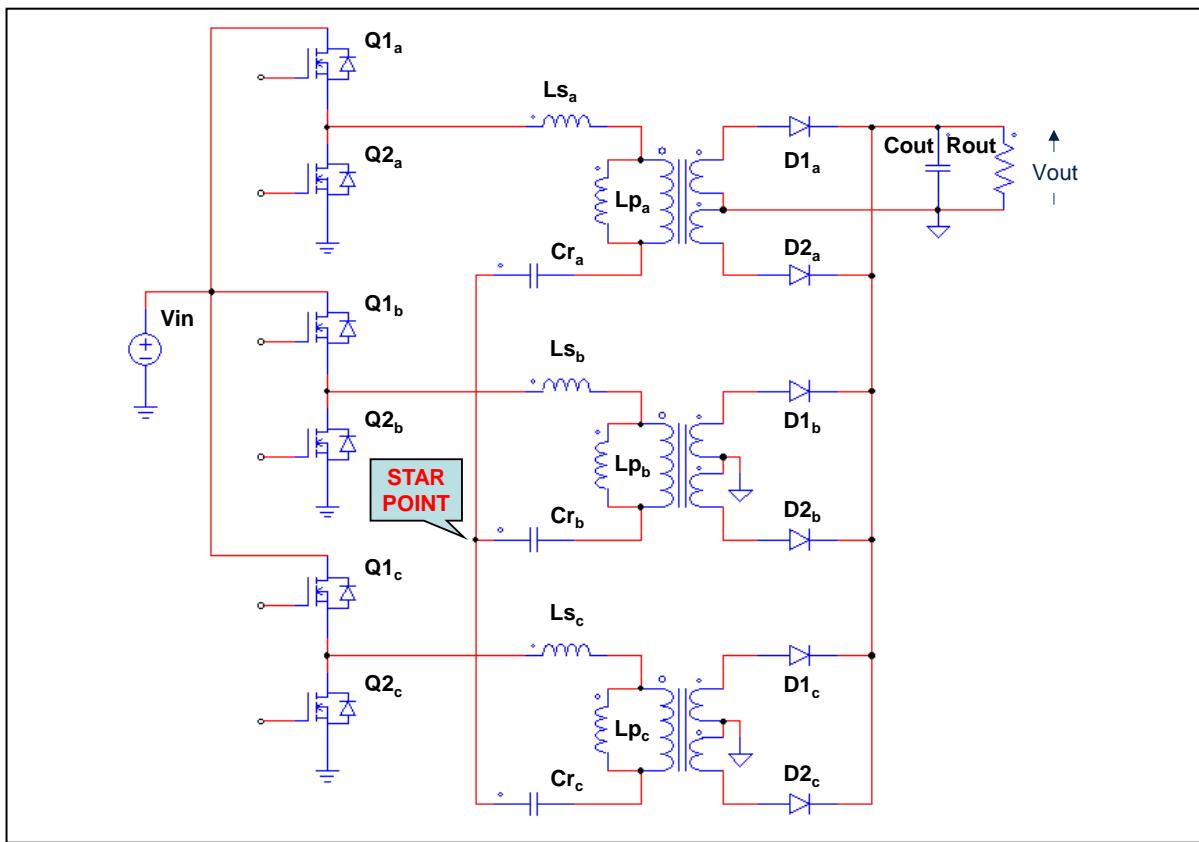
For power levels in the range of kW one could consider splitting the load power in more than 2 phases to optimize the design of each individual phase. Among the many three-phase interleaved LLC converters that have been described in the literature [83]-[87], we will review one particular solution, based on the use of three LLC converters with a Y connection of the tank circuits [83]-[84].

Differently from other multi-phase solutions that are greatly sensitive to resonant components' tolerance causing current imbalance, this topology exhibits an inherent load sharing capability. Should its native balancing ability not suffice to meet the design requirements, a closed-loop phase-shift control can be implemented to compensate for the residual current mismatch and completely balance the current supplied by each phase.

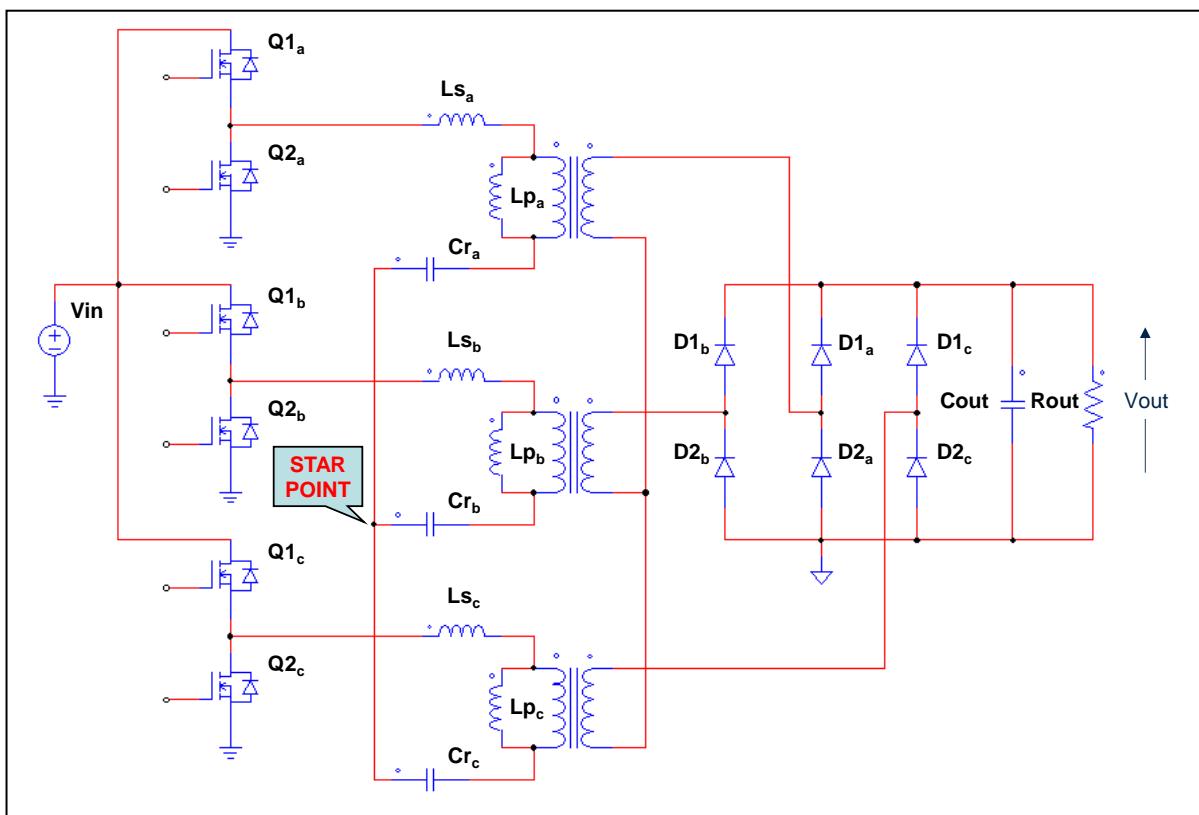
The schematic of this topology is shown in figure 184. A version with single-ended secondaries and a three-phase bridge rectification is shown in figure 185.

The floating star point that connects all the three tank circuits provides the degree of freedom that enables the three converters to run at the same frequency with  $120^\circ$  phase-shift between each phase and equally share the overall current. The interesting property of this topology is that the voltage of the floating star point moves so as to automatically balance the currents in each phase.

**Figure 184. Three-phase interleaved LLC converter with Y connection of tank circuits and FW-CT secondary rectification.**



**Figure 185. Three-phase interleaved LLC converter with Y connection of tank circuits, single ended secondaries and three-phase bridge rectification.**



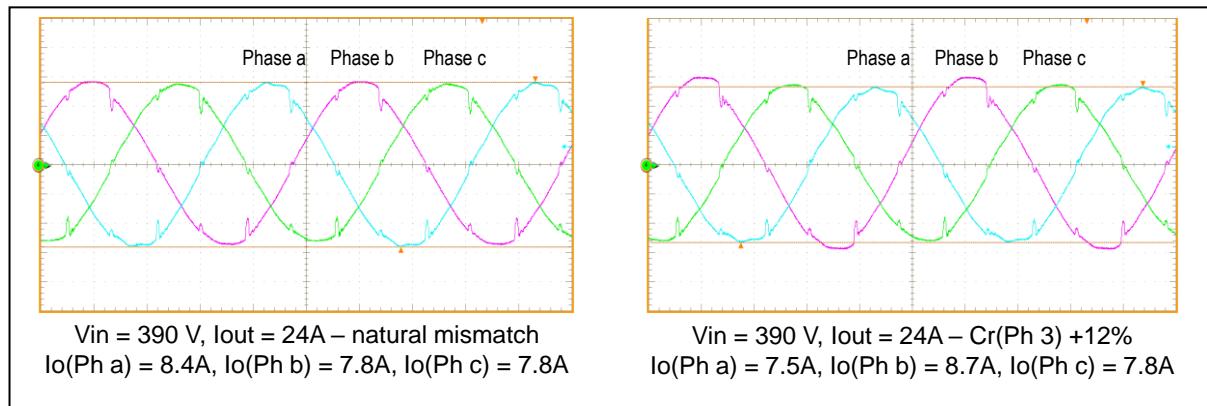
The oscilloscope picture on the left-hand side of figure 186 shows the tank current in each phase of a 3-phase prototype loaded with a total output current of 24 A, with their natural mismatch. The deviations of the individual output currents from the target value (8 A) are +5% in phase a and -2.5% in phases b and c. On an extreme level, on the right-hand side the same waveforms are shown after increasing the value of  $C_{r_c}$  by 12%. The deviations from target are now -6.25% in phase a, +8.75% in phase b and -2.5% in phase c.

The results of the same measurements done with the star point grounded, so that the three phases are simply paralleled, are shown in figure 187. Now the deviations of the individual output currents from the target value (8 A) with the natural mismatch are +61% in phase a, -36% in phase b and -25% in phase c. Increasing the value of  $C_{r_c}$  by 12% the deviations from the target become +95% in phase a, -2.5% in phase b and -92.5% in phase c.

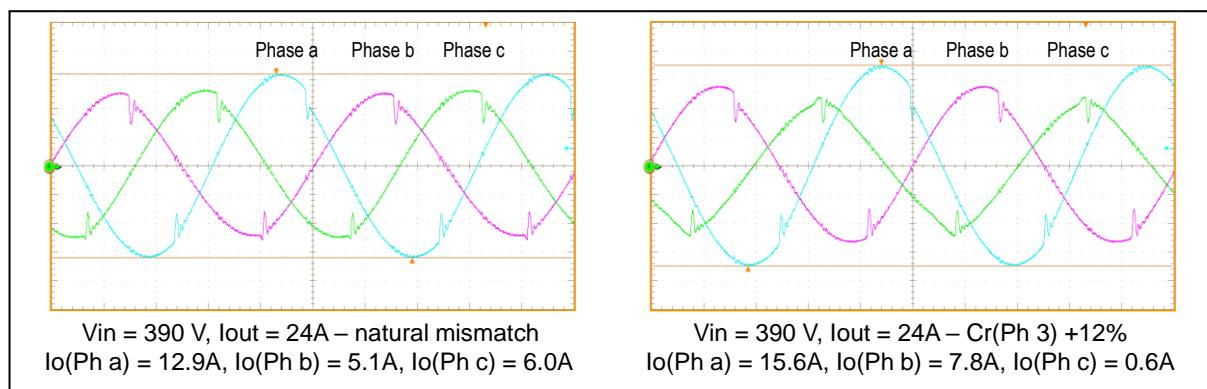
The benefit of the floating star connection is dramatic. In a system where a  $\pm 10\%$  mismatch in the individual output currents is acceptable, there is no need for current sharing control. In case of more stringent requirements, a current balancing loop can be closed that acts on the phase-shift between phases to equalize the individual currents.

With this loop the individual current can be balanced to less than 5% [84] down to about 1/3 of full load with a primary current sensing. As to this accuracy and possible improvements, the same comments made about the current balancing loop in the current-controlled inductor method apply also here.

**Figure 186. Resonant currents in a three-phase interleaved LLC converter with Y connection (star point floating).**



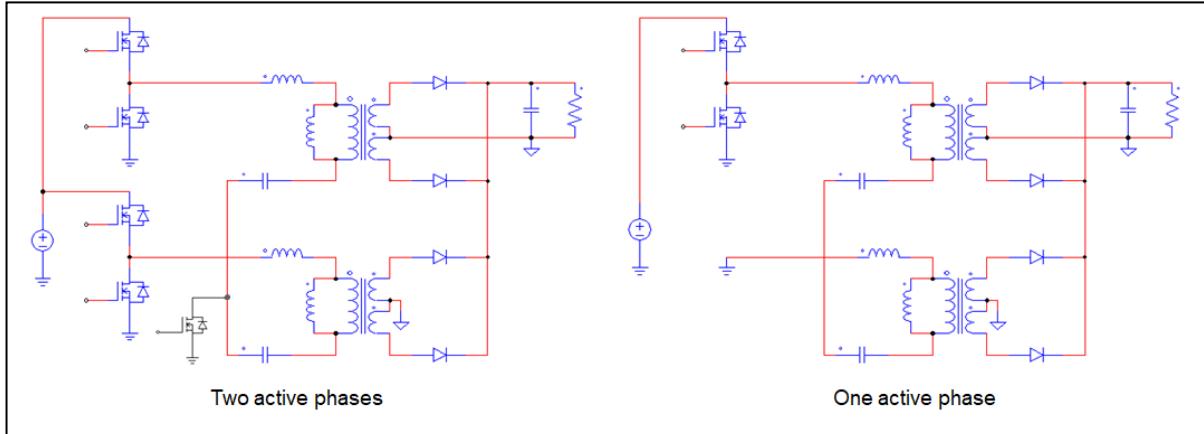
**Figure 187. Resonant currents in the same three-phase interleaved LLC converter with star point grounded.**



The floating star point connection brings current balancing but unfortunately prevents the traditional phase shedding, where one phase is simply shut down and the phase-shift between the remaining phases properly adjusted (from  $120^\circ$  to  $90^\circ$  going from three to two active phases).

Figure 188 (left-hand side) shows two possible 2-phase configurations obtained by shutting down phase c. If both MOSFETs Q<sub>1c</sub> and Q<sub>2c</sub> are kept off and the phase-shift of the driving signals of phase b changed from  $120^\circ$  to  $180^\circ$  (with respect to phase a), phase a and b become a full bridge sharing the series of their tank circuits.

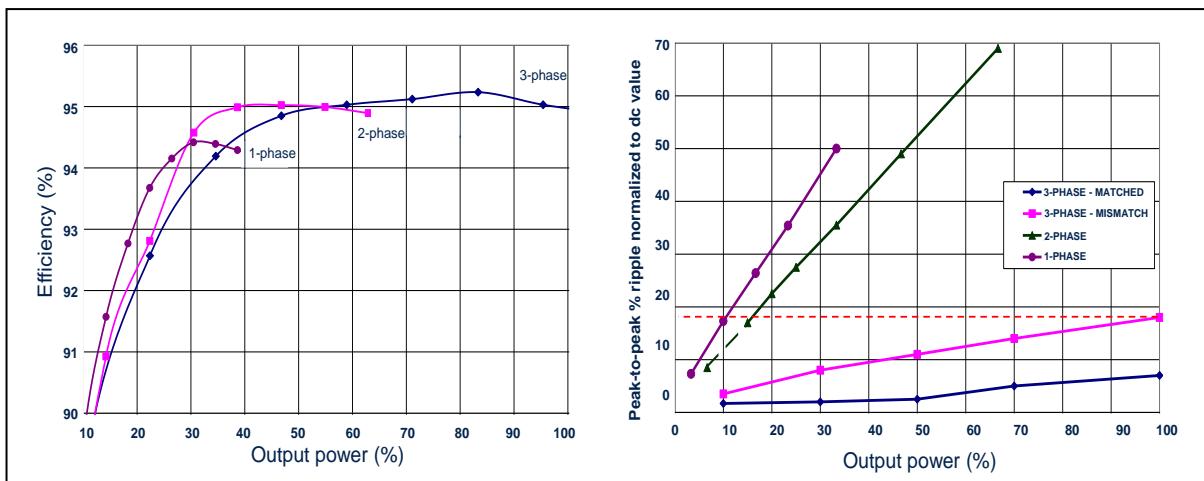
**Figure 188. Three-phase interleaved LLC converter with Y connection: phase shedding.**



Using an auxiliary switch that is turned on connecting the star point to ground when phase c is shut down, the two active phases are actually paralleled. Changing the phase-shift of the driving signals of phase b from  $120^\circ$  to  $90^\circ$  a traditional interleaving between phases a and b is possible but with no inherent load sharing property, with all the issues previously described.

Figure 188 (right-hand side) shows a possible single-phase configuration resulting from shutting down phases b and c. To provide a return path for the resonant current, however, the low-side MOSFET of phase b is kept on. The tank circuits of phases a and b therefore in series and operated as a single half bridge converter. Notice that it is not a true single-phase operation because the components of two phases are involved in current conduction.

**Figure 189. Efficiency (left) and output ripple (right) vs. load and phase shedding in a three-phase interleaved LLC converter with Y connection.**



When going from three to two active phases the output current ripple increases significantly: either the system turns to a single full bridge - in which case there is no staggering of the secondary currents - or is a 2-phase interleaved system where the individual currents can be even heavily imbalanced.

When going from two to one active phase, of course there is no possible ripple reduction, but this happens at light load and the resulting ripple is low, presumably less than the ripple at full load with three active phases.

The issue is then at intermediate loads, where a trade-off between efficiency improvement and output current ripple is necessary. Figure 189 shows the plots of efficiency vs. load and output ripple vs. load for the same 3-phase converter whose waveform were shown in figures 186 and 187, to get a quantitative idea of the compromise.

## Chapter 3

### Topology variants

LLC converters, like essentially all power converters, can be modified to enhance certain characteristics or to meet some specific design requirements more easily.

Some simple examples of these so-called topology variants have been encountered already during the present discussion: for example, the half bridge and the full bridge versions, the split-capacitor version (see figure 17) or the various configurations of secondary rectification (see figure 11).

Many topology variants have been proposed in the literature over the years [88] and the extension of the application range in power and the continuously increasing performance demand is driving further evolutions. A few topology variants that are in use in industry will be overviewed in this chapter. For a deeper analysis readers are referred to the related literature.

#### *Two-transformer LLC converter*

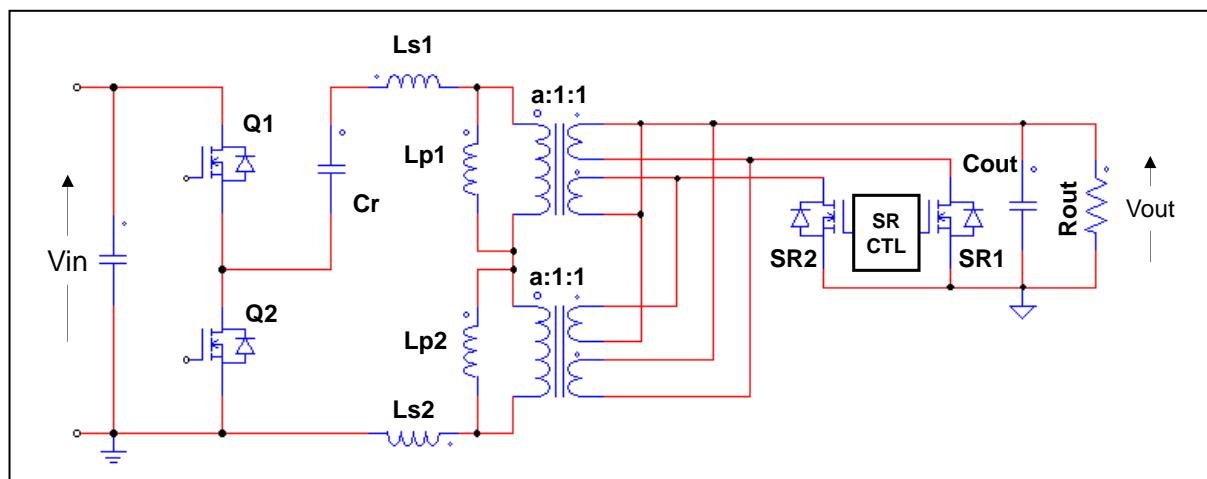
This topology variant, shown in figure 190 in its half-bridge version, can be found in some high power (e.g., server power) or slim designs (e.g., flat TV SMPS [89]). Two transformers are connected with the primary windings in series and the secondary windings in parallel. The series connection of the primary windings ensures equal current sharing between the two transformers. The operation is essentially the same as that of a conventional HB or FB.

The schematic of figure 190 shows a CT-FW rectification configuration but the SE-B can be used too as in [89]. Synchronous rectifiers are considered because this topology is normally employed in power-dense applications with a high output current, as previously mentioned.

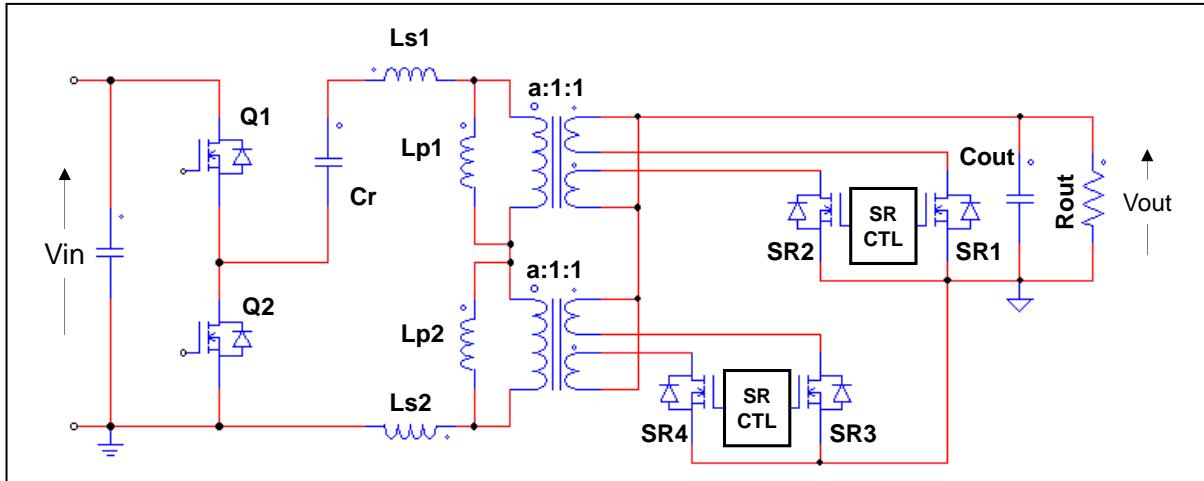
Notice in figure 190 the cross-connection paralleling of the secondary windings, an expedient to minimize the asymmetry of the secondary currents due to the unavoidable transformer asymmetries.

Comparing the characteristics of each transformer to those of a single transformer designed for the same application, since the voltage applied to the primary winding of each transformer is half the voltage applied to the entire inductive section of the LLC tank, all its parameters ( $a$ ,  $L_s$ ,  $L_p$ ) are cut in half.

**Figure 190. Two-transformer half bridge LLC converter (version I).**



**Figure 191. Two-transformer half bridge LLC converter (version II).**



Due to the parallel connection on the secondary side, the voltage seen by each secondary is the same output voltage, so each transformer can be designed with the same secondary volt per turn. Therefore, the number of secondary turns does not change, and the number of primary turns is cut in half. Furthermore, since each secondary winding carries half the total output current, the cross-sectional area of the secondary windings can be cut in half too.

Clearly, it is possible to reduce the size of each transformer because of a reduction of the core window area and achieve a higher power density.

Figure 191 shows a different version of this topology, where each transformer has its own secondary rectification and paralleling occurs after the rectification blocks. Also in this case, the converter can be an HB or a FB and the secondary rectification configuration CT-FW or SE-B. In [90], for example the converter is a FB with a dual SE-B rectification.

This version definitely requires more external parts and is therefore more expensive. However, although it might appear less efficient too, it is not necessarily so. The parallel connection after the rectifiers prevents possible current flow, due to transformer mismatch, that may occur in the current mesh that exists in the version of figure 190 as a result of the connection of the secondary windings before the rectifiers.

#### *LLC converter with matrix transformer*

LLC converters with matrix transformer can be considered a generalization of the two-transformer LLC converter shown in figure 191.

By definition, as reported in [91], a matrix transformer is an array of smaller parts called *elements* properly interconnected so that the whole functions as a single transformer. Each element is a single small transformer with a preset turns ratio (e.g., 1:1, 2:1, etc.) and the desired turns ratio is achieved by connecting the primary windings of the elements in series or parallel and the secondary windings in series or parallel, depending on the design objective. In our case of converters operated off the power line and required to deliver a relatively high current, the most appropriate combination is to connect the primary windings in series and the secondary windings in parallel.

Matrix transformers offer significant benefits: they can split a large current between the parallel-connected secondary windings, reduce the secondary-side leakage inductance by lowering the number of secondary turns (1 turn is quite common in high output current applications) and improve the overall thermal performance by distributing the power loss

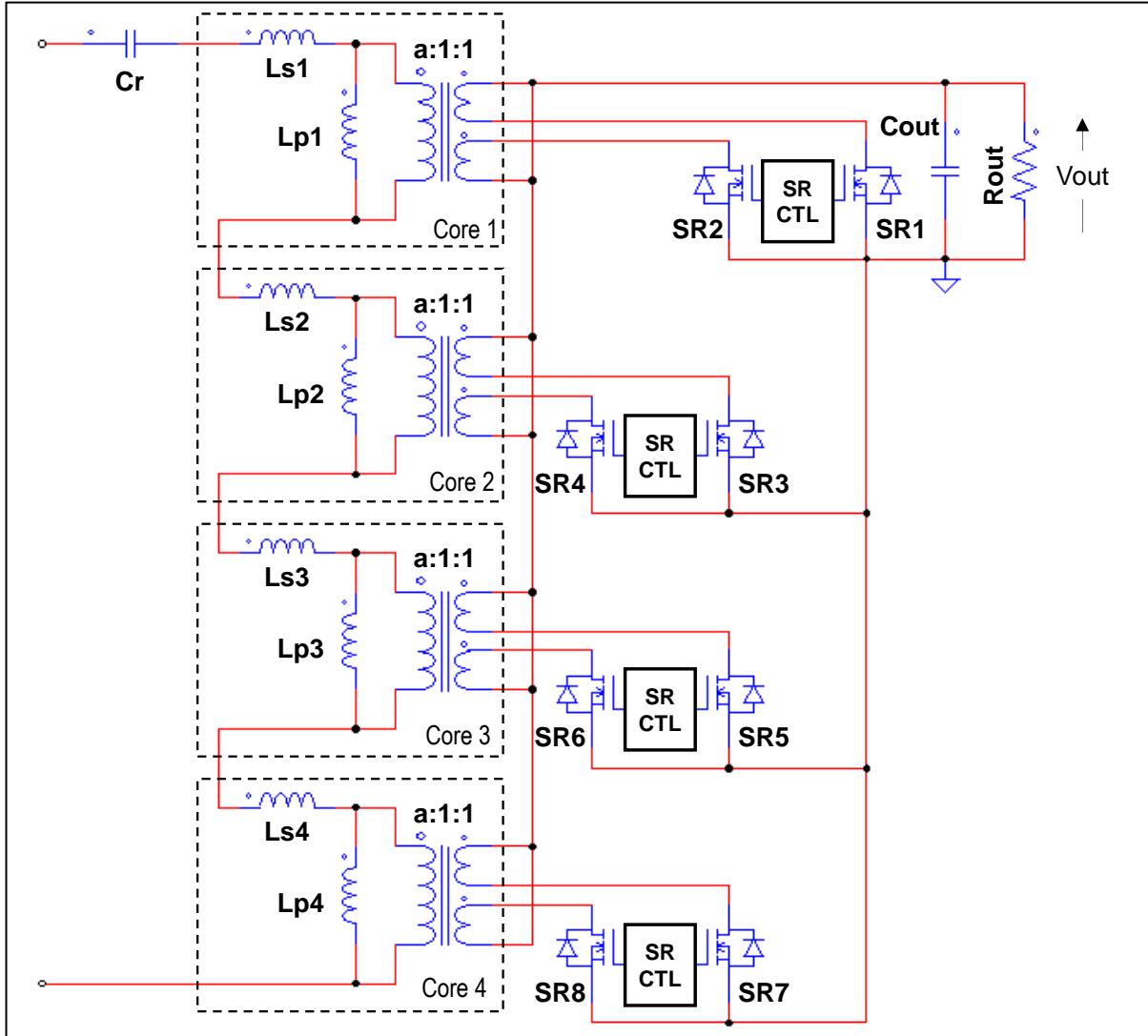
throughout the various elements. Additionally, with appropriate interleaved structures matrix transformers can significantly reduce the magnetomotive force (MMF) of the windings, thus reducing leakage inductance and winding ac resistance due to skin and proximity effects, which is particularly advantageous in high switching frequency applications.

Matrix transformers find their construction of choice using planar magnetic cores and with windings realized on a multilayer PCB that accommodates also the rectifier block (SR will be used for high efficiency) and the output capacitors bank to minimize leakage and termination loss.

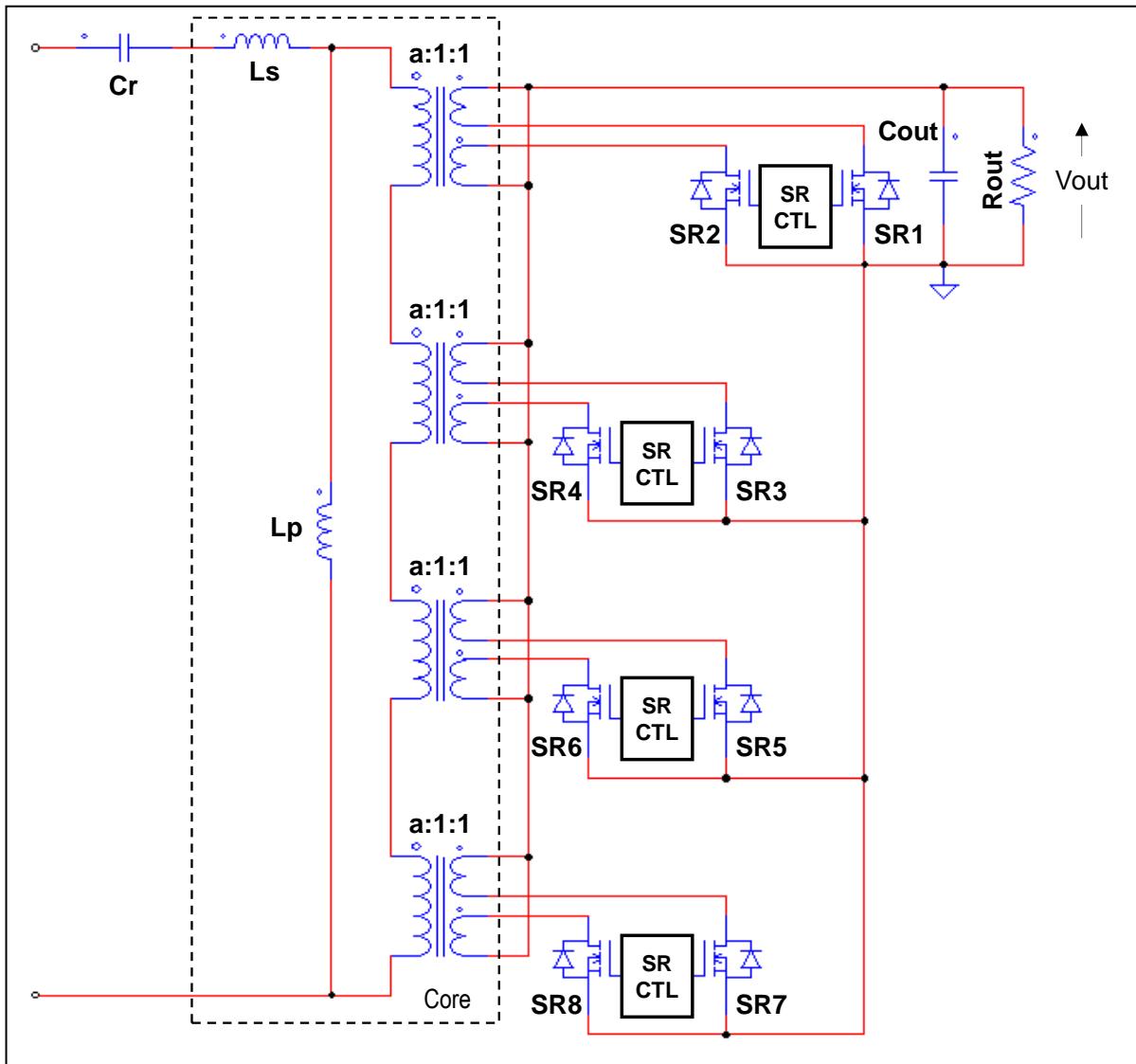
Figure 192 shows the secondary side of an LLC converter with matrix transformer as reported in [92], where a single big transformer is replaced by four smaller transformers. Comparing the characteristics of each transformer to those of a single transformer designed for the same application, all its parameters ( $a$ ,  $L_s$ ,  $L_p$ ) are reduced four times. Also, the number of primary turns will be four times smaller.

The drawback of this approach is that a magnetic ferrite core is required for each elementary transformer. Reference [93] reports a different matrix transformer structure that integrates multiple transformers into a single magnetic core as schematically shown in figure 193.

**Figure 192. Tank circuit and output stage of an LLC converter with matrix transformer.**



**Figure 193. Tank circuit and output stage of an LLC converter with a single-core matrix transformer.**



This approach utilizes flux cancellation to reduce flux density in the magnetic limbs and the relevant core losses. Additionally, it does not require a PCB with large number of layers, thus offering a considerable cost reduction compared to a multi-core matrix transformer.

#### *Three-level LLC converter*

The multilevel approach can be considered as the dual of the multiphase approach: while in multiphase converters the switch structures are essentially connected in parallel, in multilevel converters the switch structures are stacked on top of each other. Compared to a multiphase approach, which requires a magnetic device per each phase, in multilevel converters a single magnetic device is generally needed.

This technology has been used widely in railway systems, ship electric power distribution systems, fuel cell systems, renewable energy systems (photovoltaic and wind turbine) and other high-voltage systems, e.g., those operated from medium voltage distribution lines or the three-phase line. In fact, its fundamental benefit is that the voltage across each switch is reduced proportionally to the number of levels.

Therefore, high voltages can be handled with moderate voltage rating switches, which are generally better than high-voltage devices. Consider, for example, that the die area necessary to achieve a given  $R_{DS(on)}$  increases with the voltage rating following a power law with an exponent greater than 2. A larger die size to withstand higher voltages means not only more expensive switches but also switches with larger parasitic capacitances that are harder to drive and have larger losses.

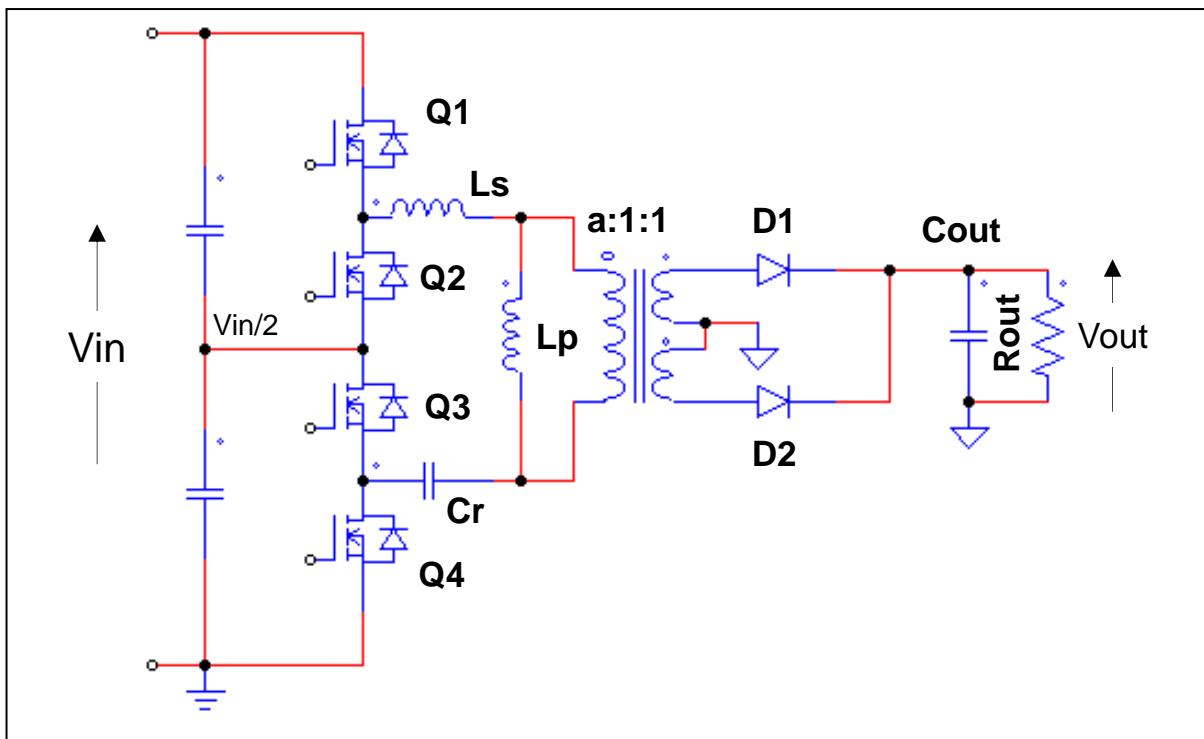
In addition, the multilevel approach reduces the voltage swing that switches undergo, thus reducing not only conduction losses due to a lower  $R_{DS(on)}$  but also switching and capacitive losses. As a positive side effect, this produces less common-mode voltage, thus reducing the EMC issues.

Considering three-level systems, the voltage rating of the switches can be half the input voltage. This property could be used the other way round in offline applications, i.e., handling input voltages that are normally handled by conventional converters with multilevel converters, using lower voltage switches featuring a much lower  $R_{DS(on)}$ .

Unfortunately, using only three levels is not a viable solution. Today 600 V devices are commonly used in a conventional half bridge (or a full bridge) operated from a 400 V input voltage bus provided by a PFC pre-regulator. With three levels one could use 300 V rated devices and this is a voltage area where there has been not much industry focus: few part numbers are available, and the technology has not been extensively developed like for higher or lower voltage parts. One more level should be added to use 150 V rated devices, where the technology offers a significant  $R_{DS(on)} \times$  die area reduction.

This, however, emphasizes the biggest drawback of this approach: the need of a great number of switches (4 with a three-level converter, 6 with a four-level converter and two more for each additional level), each requiring a related gate-drive circuit (all floating except one). This may cause the overall system to be more expensive and overly complex.

**Figure 194. Three-level half bridge LLC converter.**



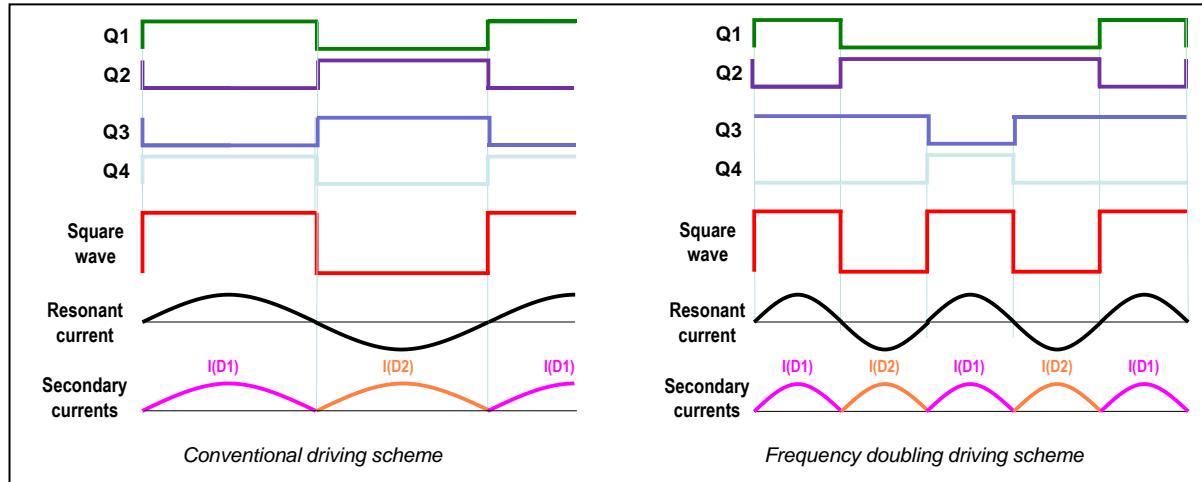
A three-level LLC resonant converter is illustrated in figure 194. It consists of two stacked half bridges and the resonant tank is connected to the two midpoints.

In the most straightforward driving scheme, Q1 and Q4 are turned on and off simultaneously and so do Q2 and Q3. The advantage of this scheme is that it can be readily implemented using any commercially available resonant controller IC with the addition of two gate drive transformers. Operation and waveforms are exactly those of a conventional half bridge.

A slightly different connection is considered in [94], which requires a slightly different driving scheme, but the operation and the waveforms are essentially unchanged.

The multilevel approach, however, enables different driving schemes that may provide the converter with new properties. This is the case, for example, of the frequency doubling driving scheme proposed in [95] that is shown in the timing diagrams of figure 195 along with the conventional driving scheme previously considered.

**Figure 195. Two possible driving schemes for three-level half bridge LLC converter.**



In this driving scheme, the pair Q1-Q4 is turned on with 25% duty cycle and the pair Q2-Q3 with 75% duty cycle, with the two PWM pulse trains displaced by 50% of switching period.

By doing so, the tank circuit is driven with half input voltage at a frequency double of that of the two PWM pulse trains. This is quite interesting because, according to the design objective, one can reduce the transformer size while keeping switching losses at a low level or keep the same transformer size and further reduce switching losses.

A drawback of this operation is the different current stress for the two pairs: the Q1-Q4 pair carries  $\frac{1}{4}$ , and the Q2-Q3 pair  $\frac{3}{4}$  of total resonant current.

Finally, another good point to mention is that with both driving schemes there is an intrinsic input voltage self-balance mechanism so that the two stacked half bridges share the input voltage equally, which is a benign characteristic since it saves control overhead and increases converter reliability.

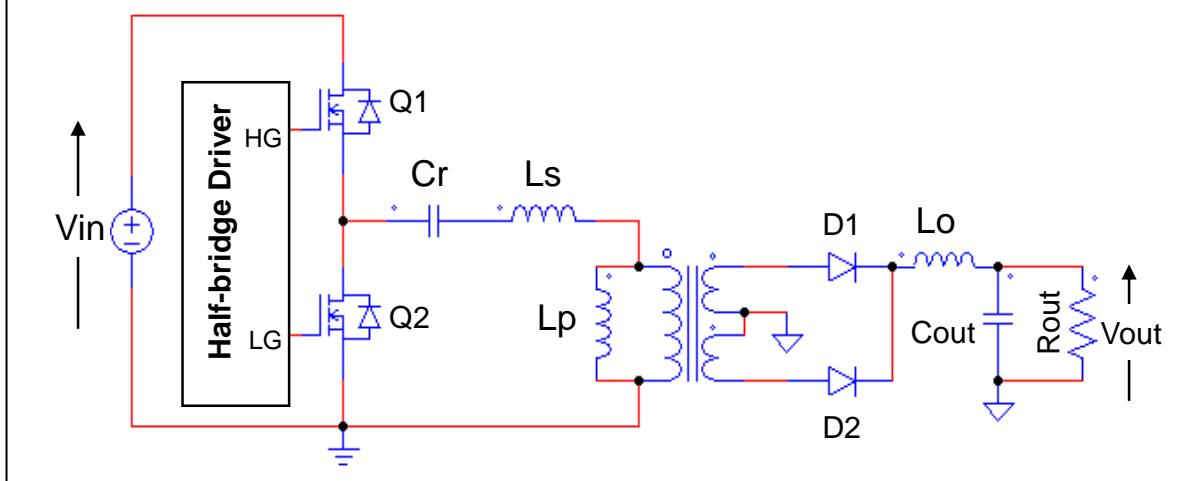
#### *LLC resonant converter with current sink output filter*

We have seen already that a weak point of the LLC converter is the large current stress on the output capacitor, so that it needs to be designed to withstand the ac component of the secondary current. We have also seen that one way to avoid this issue is to use the multiphase

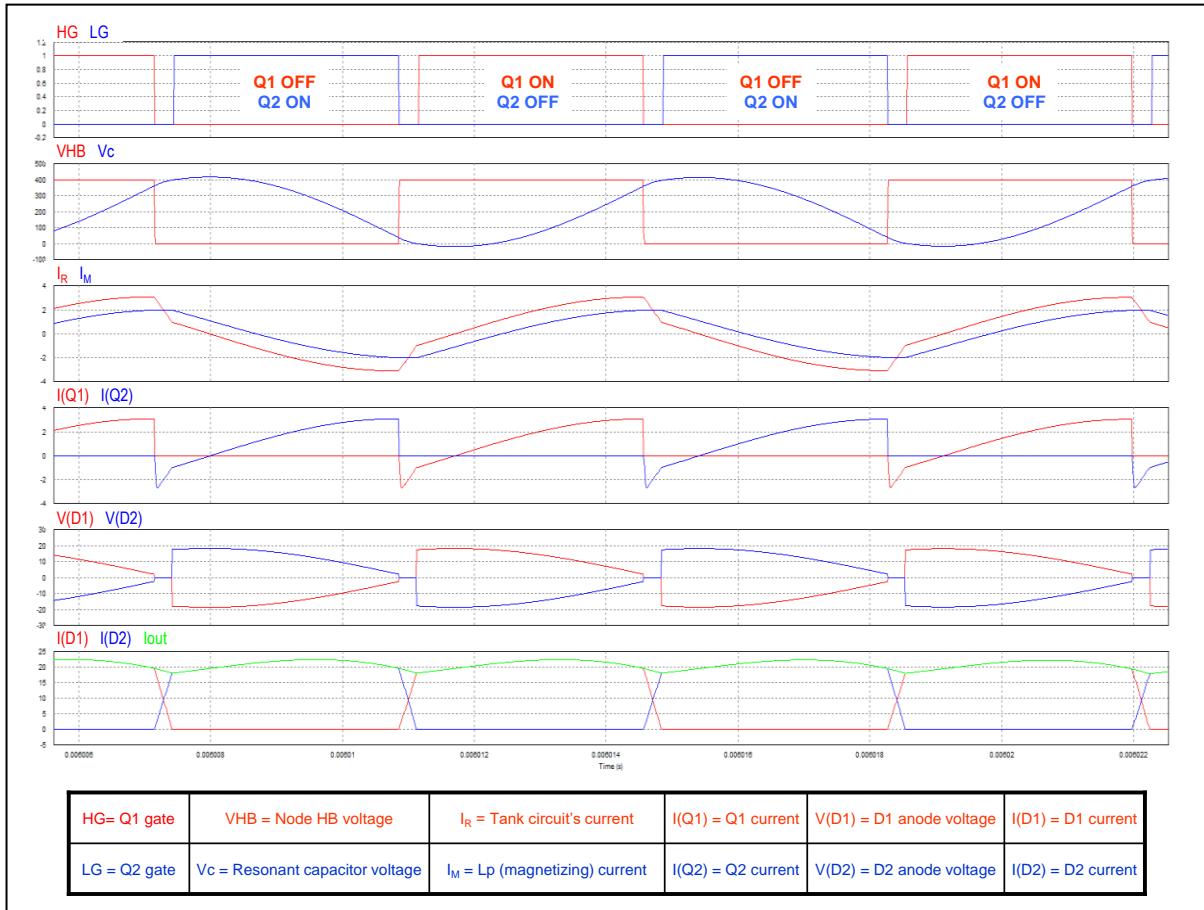
approach with interleaving, which however increases complexity and cost, so that it appears more justified at higher power levels.

In [96], [97] a modification of the LLC converter is proposed that uses a current sink output filter, i.e., adds an output inductor  $L_o$  between the rectifier block and the output capacitor as depicted in figure 196. Figure 197, instead, shows the typical key waveforms. With this addition, the output capacitor can be significantly reduced, thus also reducing its size, weight, and cost. It is therefore an interesting topology for high output current applications.

**Figure 196. LLC resonant converter (half bridge) with current sink output filter.**



**Figure 197. LLC resonant converter with current sink output filter: key waveforms.**



Compared to the conventional LLC converter, the current sink output filter changes the operation of the converter completely.

The main resonant tank is composed of  $L_p$  and  $C_r$  and there is essentially a single resonance frequency. The converter can operate only above resonance and, as visible in figure 197, the tank current looks much like that of the conventional LLC converter when operated above resonance.

To a first-order approximation, neither  $L_s$  nor  $L_o$  participate to resonance.  $L_s$  just smooths the edges of the resonant current that follow the half bridge toggling, and in some cases may help achieve ZVS. Normally it can be substantially reduced, so that slotted bobbins might be unnecessary for magnetic integration.  $L_o$  can be regarded as a sort of current flywheel and in the analysis of the circuit can be replaced by a current source.

The switching frequency range is basically as narrow as with the traditional LLC. Rather, at light load is definitely narrower.

In fact, the output inductor cancels the effect of the parasitic capacitance of the secondary rectifiers because it blocks the initial “current spike” that occurs when one rectifier is going to be forward biased and that in the conventional LLC converter goes to the output. In this case this current spike goes through the parasitic capacitance of the other rectifier. For this reason, the switching frequency does not need to go that high to reduce the energy per cycle transferred by the normal mechanism. Needless to say, for the same reasons this topology is immune to the feedback reversal phenomenon at light load.

The adverse side effect of the output inductor  $L_o$  is that the reverse voltage applied to the secondary rectifiers increases significantly, 50% or even more than  $2 \cdot V_{out}$ , depending on the characteristics of the tank circuit.

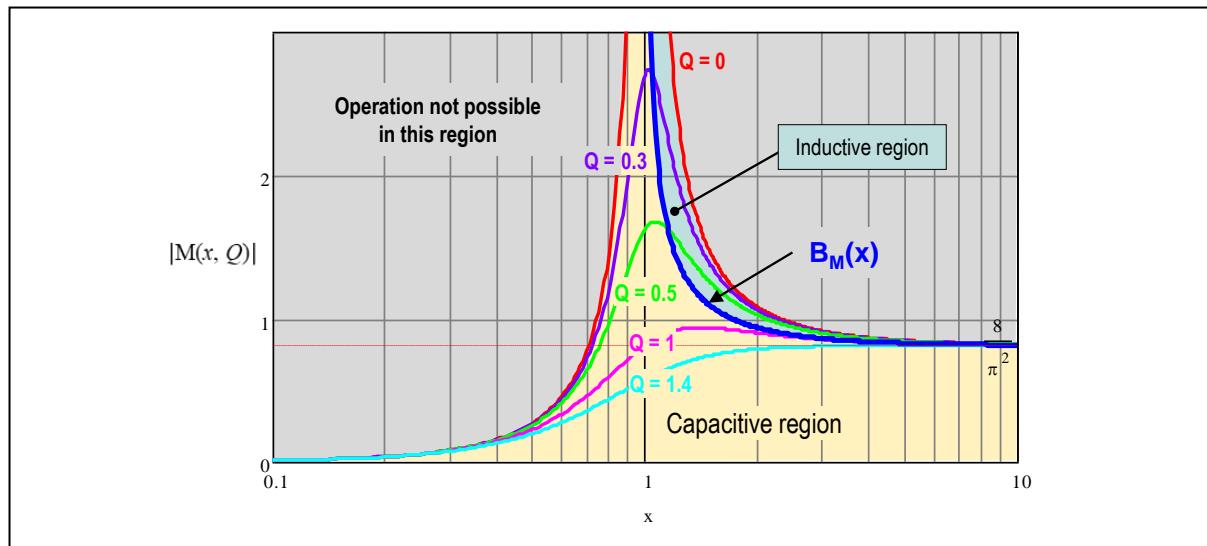
Some additional insight on its operation can be given by its FHA analysis. Figure 198 shows the plot of the voltage gain  $|M|$ :

$$|M(x, Q)| = \frac{8}{\pi^2} \frac{x^2}{\sqrt{(x^2-1)^2+Q^2x^2}}, \quad (301)$$

where:

$$f_R = \frac{1}{2\pi\sqrt{L_p C_r}}; \quad Q = \frac{Z_0}{R_e} = \frac{8}{\pi^2} \frac{Z_0}{a^2 R_{out}}; \quad Z_0 = \sqrt{\frac{L_p}{C_r}}. \quad (302)$$

**Figure 198. LLC resonant converter with current sink output filter: plot of  $|M(x, Q)|$ .**



All curves have a horizontal asymptote  $M_\infty = 8/\pi^2$  when  $x \rightarrow \infty$ . This poses a constraint on  $\alpha$  and then, on the turn ratio  $a$  (reminder:  $\alpha = 2a$  in the half bridge and  $\alpha = a$  in the full bridge); in the half bridge:

$$a > \frac{4}{\pi^2} \frac{V_{in\max}}{V_{out}} . \quad (303)$$

The curve with  $Q = 0$  has a vertical asymptote when  $x \rightarrow 1$ . The inductive operating region will be that included between the curve  $Q = 0$  and the curve  $B_M(x)$  representing the capacitive mode borderline. A necessary condition for the converter to operate in the inductive region is to operate above resonance ( $x > 1$ ).

As visible in the key waveforms of figure 197 the shape of the resonant current is piecewise sinusoidal and has significant harmonics. Therefore, the quantitative results of an FHA-based analysis are not so accurate, and a reliable design procedure should be rather based on a TDA analysis.

## Chapter 4

### Single-stage LLC PFC

The IEC 61000-3-2 regulation sets limits to the harmonic currents drawn by electrical equipment connected to public low-voltage distribution systems, with the objective of maintaining mains voltage quality. It is applicable to electrical and electronic equipment using voltage not less than 220 Vac and having a rated input current not exceeding 16 A per phase.

This regulation considers four classes of electronic equipment, the most important of which in this context are class C (lighting equipment with a rated input power in excess of 5 W) and Class D. The IEC 61000-3-2 specifies that class D equipment includes personal computers and personal computer monitors, television receivers, refrigerators, and freezers with one or more variable-speed drives to control one or more compressor motors, with a rated input power included between 75 W and 600 W.

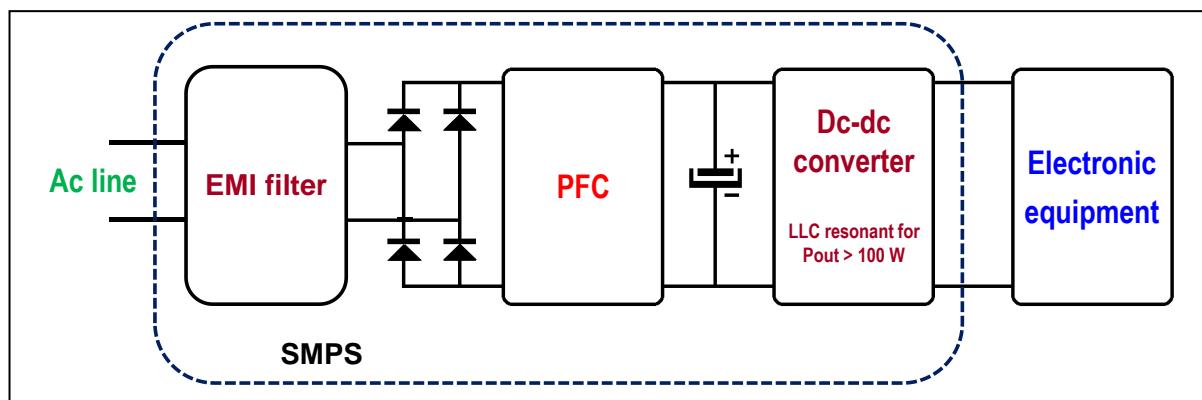
De facto, all ICT equipment (e.g., ac-dc adapters for portable computers, large printers) with an input power over 75 W is considered as belonging to class D and then required to comply with the IEC 61000-3-2. Not only: even power supplies of equipment not considered by the regulation are quite often specified and built to comply with the class D limits (e.g., server and telecom SMPS).

There are different solutions to address the compliance with the IEC 61000-3-2 but by far the most common in industry is the addition of an electronic front-end circuit, the so-called active power factor corrector (PFC). In its typical implementation, a PFC is a switch-mode converter directly supplied by the rectified mains, without any energy buffer capacitor after the bridge rectifier (the so-called bulk capacitor) and controlled to draw from the power line a sinusoidal current in phase with the voltage. This results in unity power factor,  $\text{PF} = 1$ .

As shown in figure 199, a typical power-factor-corrected SMPS has therefore a two-stage architecture: a PFC stage front-end. The term pre-regulator stems from the fact that the PFC front-end normally provides a regulated output voltage to the cascaded dc-dc converter, whose design can then be optimized for a narrow input voltage range.

Usually, a PFC pre-regulator is realized with a boost converter, which is a non-isolated topology, so that the cascaded dc-dc converter is responsible for providing the safety isolation required in essentially all power supplies of class D equipment.

**Figure 199. Typical two-stage architecture of a power factor corrected SMPS.**



The boost converter can essentially cover the entire power range of class C and D equipment, whereas the cascaded dc-dc converter uses different topologies depending on the power level. Flyback converters are most used in the low power range, say up to 100 W, the LLC resonant converter has replaced other topologies at power levels over 100 W.

However, there are applications where having an isolated PFC cascaded by one or more non-isolated converters may be advantageous. This is the case, for example, of multioutput SMPS or LED drivers, or the case of USB-PD compliant chargers for mobile equipment, single and multiport. Other applications (e.g., battery chargers) are tolerant to the low-frequency ripple of a PFC output and an isolated PFC might offer substantial cost saving by using a single-stage architecture.

Flyback-based isolated PFCs are a good choice up to 50-60 W (they are very often used in lighting equipment). For higher power levels there are solutions based on Cuk or SEPIC converters; unfortunately, there is no simple and effective way to introduce isolation in the conventional boost converter. In this context, an isolated PFC based on the LLC resonant converter, i.e., a *Single-stage LLC PFC*, might be an attractive solution.

The question that arises is if the LLC converter can perform as a PFC stage when supplied from a rectified sinusoidal voltage that goes all the way from zero to the peak. When the instantaneous input voltage moves toward a zero-crossing, to regulate the output voltage the required voltage gain becomes larger and larger and tends to infinity when the instantaneous input voltage is zero. However, since the objective is to draw from the power line a current proportional to the line voltage, as the instantaneous input voltage moves toward a zero-crossing the load becomes lower and lower. As the FHA analysis has shown, the LLC converter has a much higher voltage gain at light load than at heavy load, and that it even goes to infinity at zero load ( $Q = 0$ ) when the switching frequency equals the lower resonance frequency  $f_{R2}$ . Therefore, the LLC converter has the potential to work as a PFC stage.

#### *FHA analysis of LLC PFC*

The FHA analysis of the LLC converter discussed in Part IV was developed based on the assumption that the converter was supplied by a dc input voltage (or, rather, by a substantially dc input voltage), and led to a series of design guidelines for the tank circuit.

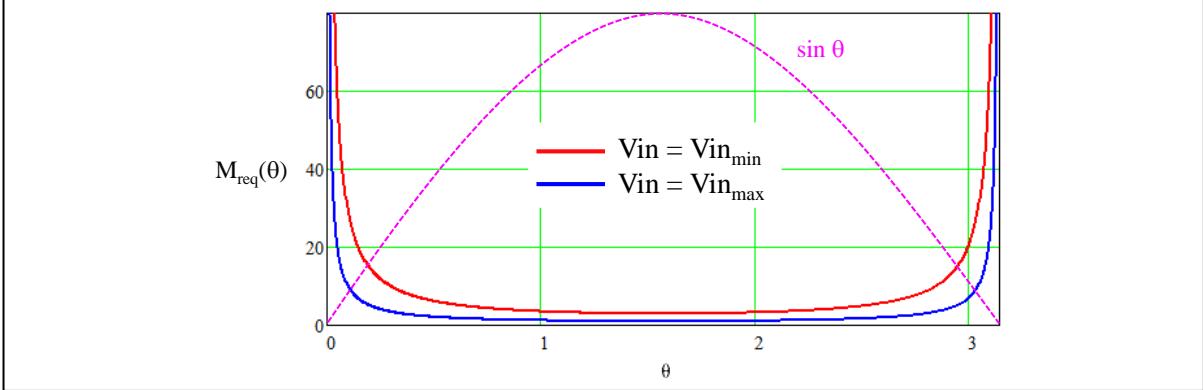
The FHA approach can be extended to an LLC converter supplied by a rectified sinusoidal voltage at the line frequency  $f_{line}$  that goes all the way from zero to the peak. The underlying assumption is the so-called quasi-static approximation: the operating point changes with the instantaneous phase angle  $\theta$  of the rectified sinusoid slowly enough to consider the system always operating in steady-state conditions. This is justified by the line frequency  $f_{line}$  being much lower than the characteristic frequency associated to the response time of the converter.

As previously highlighted, since the output voltage will be regulated at a constant value, the required gain will not be constant but will vary along the instantaneous phase angle  $\theta$ . If with  $V_{in}$  we denote the rms value of the line voltage, equation (148) can be rewritten as follows:

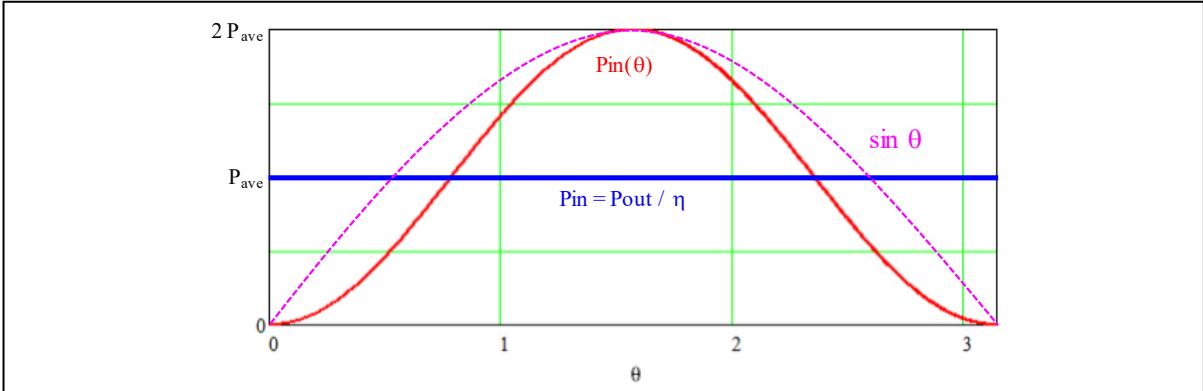
$$M_{req}(V_{in}, \theta) = \alpha \frac{V_{out} + V_{Rect}}{\sqrt{2} V_{in} \sin \theta}. \quad (304)$$

Its plot is shown in figure 200. Furthermore, having  $PF=1$  implies that also the input and output power are not constant along  $\theta$ . Irrespective of the topology, in a PFC stage, which can be regarded as a *resistor emulator*, the instantaneous input power swings all the way from 0 (at the zero-crossings of voltage and current) to twice the average power  $P_{in}$  (equal to  $P_{out}/\eta$ , where  $\eta$  is the efficiency) on the peaks of voltage and current, as inferable from (305) and shown in the plot of figure 201:

**Figure 200. Minimum gain required for regulation in a single-stage PFC LLC.**



**Figure 201. Instantaneous power and average (dc) power.**



$$Pin(\theta) = 2 Vin Iin \sin^2 \theta = 2 Pin \sin^2 \theta = 2 \frac{Pout}{\eta} \sin^2 \theta , \quad (305)$$

where  $Iin$  is the rms value of the line current. Reminding that the average power  $Pin$  can be expressed also as half the product of the peak line voltage  $Vin_{pk} = \sqrt{2} Vin$  and peak line current  $Iin_{pk} = \sqrt{2} Iin$ , from (305) evaluated at  $\theta = \pi/2$  we derive:

$$Pin = Vin_{pk} Iin_{pk} . \quad (306)$$

Therefore, on the peak of the sinusoidal line voltage the converter operates as if it was powered by a dc voltage equal to  $Vin_{pk}$ , drawing a dc current equal to  $Iin_{pk}$ . As a consequence, the first-harmonic representation of the input port can be described by the same equations seen for the dc case where  $Vin_{pk}$  replaces  $Vin$  in (50), (51) and (54), and  $Iin_{pk}$  replaces  $Iin$  in (53) and (54).

The ac resistance (61) and the quality factor (71) vary along  $\theta$  too. Substituting (305) in (61) and (71) yields respectively:

$$Rout_{ac}(\theta) = \frac{4}{\pi^2} \frac{Vout^2}{Pout \sin^2 \theta} \left( 1 + \frac{V_{Rect}}{Vout} \right) , \quad (307)$$

$$Q(\theta) = \frac{\pi^2 Z_0}{4} \frac{Pout}{a^2 Vout^2} \frac{1}{1 + \frac{V_{Rect}}{Vout}} \sin^2 \theta = Q_0 \sin^2 \theta . \quad (308)$$

Finally, the voltage gain  $|M|$  given by (95) will be a function of  $\theta$  too:

$$|M(x, k, Q_0, \theta)| = \frac{1}{\sqrt{\left[ 1 + \frac{1}{k} \left( 1 - \frac{1}{x^2} \right) \right]^2 + Q_0^2 \sin^4 \theta \left( x - \frac{1}{x} \right)^2}} . \quad (309)$$

**Figure 202. Voltage gain curves for different phase angles and comparison to the minimum required gain to achieve output voltage regulation.**

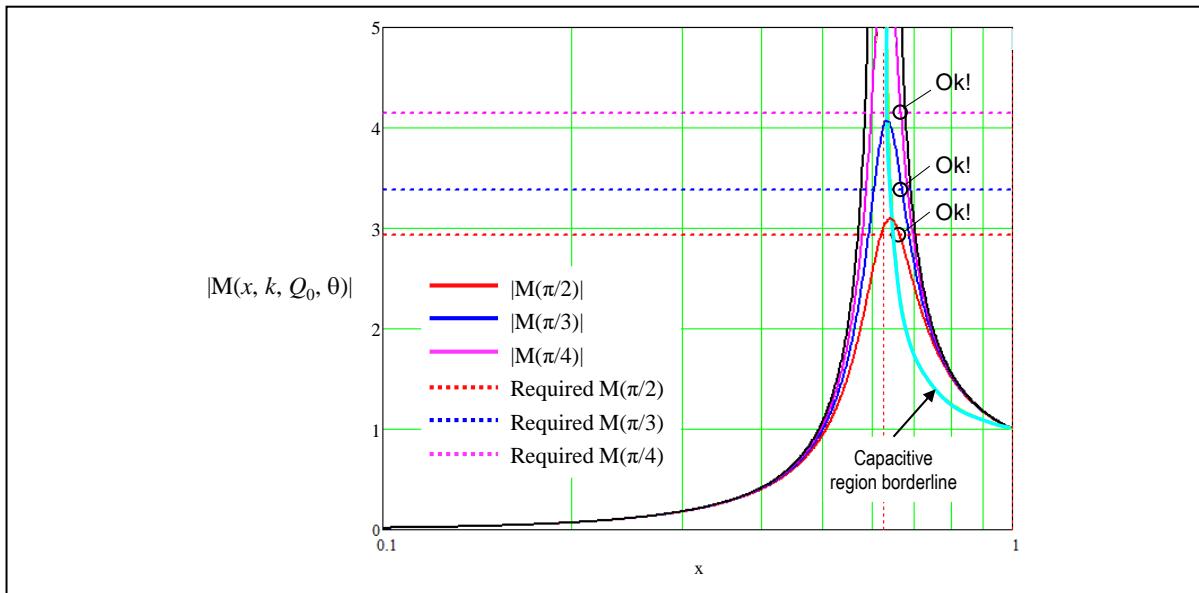


Figure 202 shows the voltage gain  $|M|$  vs. the normalized frequency, plotted at a fixed output level, with the phase angle  $\theta$  as the parameter.

Three plots are provided at  $\pi/2$ ,  $\pi/3$ ,  $\pi/4$  while the horizontal dashed lines are the required gains at the minimum input voltage (where the gain needs to be highest), with  $\theta$  equal to  $\pi/2$ ,  $\pi/3$ ,  $\pi/4$  respectively.

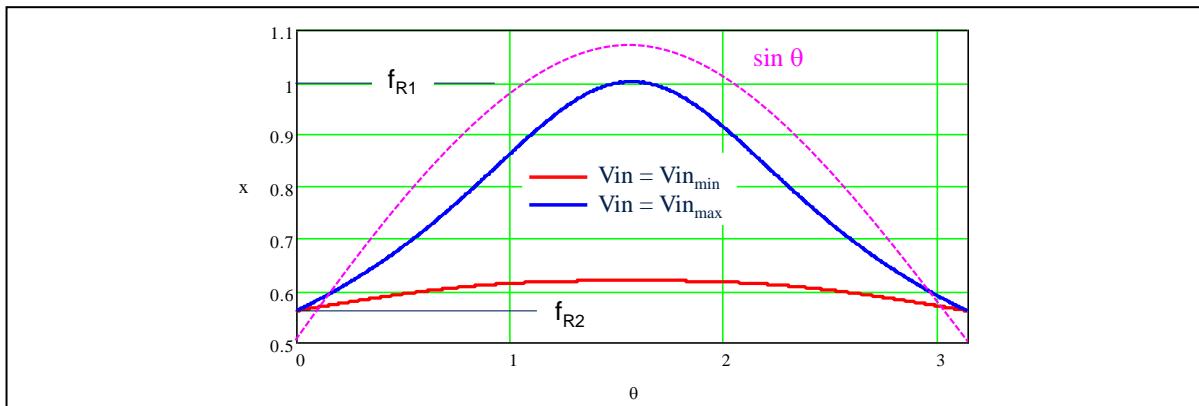
It is possible to see that at all these angles there is an intersection of the horizontal line with the corresponding  $|M|$  curve that lies in the inductive region. This means that an operating point for the converter exists and that in this operating point the converter works with ZVS. This condition, however, should be verified for any angle  $\theta$  included in  $(0, \pi/2)$  to ensure that the output voltage can be regulated.

In [98] it is demonstrated that a sufficient condition for the converter to achieve regulation in all operating conditions is that voltage gain at  $f_{sw} = f_{R2}$  and  $\theta = \pi/2$  is larger than the required gain at the minimum input voltage and  $\theta = \pi/2$ :

$$\frac{1}{Q_0} \frac{\sqrt{1+k}}{k} > \alpha \frac{V_{out}}{\sqrt{2} V_{in\min}}. \quad (310)$$

This condition is a fundamental design constraint.

**Figure 203. Normalized switching frequency vs instantaneous phase angle.**



By equating the voltage gain  $|M|$  (309) to the required gain (304) it is possible to find how the normalized switching frequency vary along the phase angle  $\theta$ . This is illustrated in the plot of figure 203.

The switching frequency peaks at  $\theta = \pi/2$  and decreases as the instantaneous line voltage goes towards the zero-crossing, where it reaches the lower resonance frequency  $f_{R2}$ .

#### *Design considerations and step-by-step design procedure*

Although with a single-stage LLC PFC it is possible to handle power levels well above 1 kW using the full bridge configuration [99], the majority of the target applications for such a single-stage LLC PFC stage are in the few hundred watts. Therefore, we will consider the half bridge configuration and it will be  $\alpha = 2a$ .

Table 17 lists a typical set of electrical specifications for a draft design of a single-stage LLC PFC converter. We will consider a procedure based on them, tracing those outlined for the dc input voltage case in Part IV, Chapter 7, though based on a slightly different strategy:

1. The converter will be designed to work in the below resonance region with the switching frequency ranging between the lower and the upper resonance frequencies. In terms of normalized frequency this means:

$$\frac{1}{\sqrt{1+k}} < x < 1 . \quad (311)$$

There is not a predefined nominal input voltage where the converter may operate in optimal conditions. It seems that there is no special benefit in operating the converter above resonance, it just widens the frequency range.

2. The converter will work at resonance ( $M = 1$ ) at the maximum input voltage for  $\theta = \pi/2$ . This determines the transformer turns ratio (APR model):

$$a = \frac{\sqrt{2}}{2} \frac{V_{in_{max}}}{V_{out} + V_{Rect}} . \quad (312)$$

With this choice, reminding that in the half bridge, the required gain at minimum input voltage for  $\theta = \pi/2$  is:

$$M_{req} \left( V_{in_{min}}, \frac{\pi}{2} \right) = 2a \frac{V_{out} + V_{Rect}}{\sqrt{2} V_{in_{min}}} = \frac{V_{in_{max}}}{V_{in_{min}}} . \quad (313)$$

3. The converter must be able to regulate down to zero load at maximum input voltage.

**Table 17. Reference electrical specification for a single-stage LLC PFC**

Symbol	Name	Unit
$V_{in_{min}} - V_{in_{max}}$	Input voltage range (rms values)	Vac
$V_{out}$	Regulated output voltage	Vdc
$P_{out_{min}} - P_{out_{max}}$	Output power range	W
$\eta$	Estimated efficiency @ $P_{out_{max}}, V_{in_{min}}$	%
$f_{R1}$	Upper resonance frequency	kHz
$f_{R2}$	Lower resonance frequency	kHz
$C_{HB}$	Half bridge midpoint estimated capacitance	pF
$T_D$	Dead-time	ns

4. The quality factor  $Q_0$  will be chosen so that converter will always work with ZVS, from zero load to  $P_{out,max}$ . As also visible in figure 202, the operating point closest to the capacitive region borderline is when the converter works with the minimum input voltage and full load, on the peak of the sinusoid ( $\theta = \pi/2$ ). Choosing  $Q_0$  so that ZVS and minimum gain conditions are both fulfilled, that will guarantee that the required voltage gain is always intercepted, and that unity power factor ( $PF=1$ ) can be achieved while operating with ZVS.

The discussion presented so far can be summarized in a step-by-step design procedure based on the specification given in Table 17.

Step 1. Calculate  $a$  so that converter will work at resonance at maximum input voltage peak using (312).

Step 2. Calculate the output resistance  $Re$ :

$$Re = \frac{4}{\pi^2} a^2 \frac{V_{out}^2}{P_{out,max}} \left( 1 + \frac{V_{Rect}}{V_{out}} \right). \quad (314)$$

Step 3. Calculate the maximum voltage gain  $M_{max}$  at  $V_{in} = V_{in,min}$  and  $\theta = \pi/2$  using (304).

$$M_{max} = 2a \frac{V_{out}+V_{Rect}}{\sqrt{2} V_{in,min}}. \quad (315)$$

Step 4. Calculate  $k$  so that the actual lower resonance frequency is  $f_{R2}$ :

$$k = \left( \frac{f_{R1}}{f_{R2}} \right)^2 - 1. \quad (316)$$

Step 5. Calculate the maximum  $Q_0$  value,  $Q_{max1}$ , necessary to stay in the inductive region at minimum  $V_{in}$  and maximum load. From (100):

$$Q_{max1} = \frac{1}{k M_{max}} \sqrt{\frac{M_{max}^2}{M_{max}^2 - 1} + k}. \quad (317)$$

Step 6. Calculate the maximum  $Q_0$  value,  $Q_{max2}$ , to ensure ZVS at zero load and maximum  $V_{in}$ . From (169), reminding that  $x_{max} = 1$ :

$$Q_{max2} = \frac{2}{\pi} \frac{1}{k} \frac{T_D}{Re C_{HB}}. \quad (318)$$

Step 7. Calculate the maximum  $Q_0$  value,  $Q_{max3}$ , to ensure that the minimum gain requirement is fulfilled. From (310):

$$Q_{max3} = \frac{\sqrt{2}}{2} \frac{1}{a} \frac{\sqrt{1+k}}{k} \frac{V_{in,min}}{V_{out}+V_{Rect}}. \quad (319)$$

Step 8. Choose a value of  $Q_0$ ,  $Q_S$ , such that  $Q_S \leq \min(Q_{max1}, Q_{max2}, Q_{max3})$ .

Step 9. Calculate the normalized minimum operating frequency at  $V_{in} = V_{in,min}$ ,  $P_{out} = P_{out,max}$  and  $\theta = \pi/2$ ,  $x_{min}$ , using (161) with  $Q_B = Q_{max1}$ :

$$x_{min} \cong \frac{1}{\sqrt{1+k \left( 1 - \frac{1}{M_{max}^{1+\left(\frac{Q_S}{Q_{max1}}\right)^5}} \right)}}. \quad (320)$$

Step 10. Calculate the phase-shift  $\phi_{min}$  of the tank current at  $V_{in} = V_{in,min}$ ,  $P_{out} = P_{out,max}$  and  $\theta = \pi/2$  with (163) and check if the ZVS condition (173) is fulfilled. If so, proceed to step 11, otherwise choose a smaller value for  $Q_S$  and go back to step 9.

Step 11. Calculate the characteristic impedance of the tank circuit and all component values with (157), here reported for reader's convenience:

$$Z_0 = Re Q_S; \quad Cr = \frac{1}{2\pi f_{R1} Z_0}; \quad Ls = \frac{Z_0}{2\pi f_{R1}}; \quad Lp = k Ls. \quad (157)$$

Step 12. Considering an integrated magnetics implementation and assuming magnetic circuit symmetry, calculate the parameters of the real transformer with (32), here reported for reader's convenience:

$$n = a \sqrt{1 + \frac{L_s}{L_p}}; \quad L_\mu = \sqrt{L_p L_1}; \quad L_{L1} = L_1 - L_\mu; \quad L_{L2} = \frac{L_{L1}}{n^2}. \quad (32)$$

Step 13. Calculate the maximum peak of the tank current to set up the overcurrent means by (162) where the dc value  $V_{in}$  becomes  $V_{in_{pk}} = \sqrt{2} V_{in}$ , with  $V_{in}$  rms value of the line voltage:

$$I_{R1pk} = \begin{cases} \frac{\pi}{\sqrt{2}\eta} \frac{P_{out_{max}}}{V_{in_{min}}} \frac{1}{\cos \varphi_{min}} & (\text{HB}) \\ \frac{\pi}{2\sqrt{2}\eta} \frac{P_{out_{max}}}{V_{in_{min}}} \frac{1}{\cos \varphi_{min}} & (\text{FB}) \end{cases}. \quad (321)$$

#### EXAMPLE

To illustrate the just outlined design procedure let us consider a fully developed example. Table 18 lists the electrical specification of an exemplary single-stage LLC-PFC intended to power an LED driver. Diode rectification will be used due to the high output voltage.

Step 1. Calculate  $a$  so that converter will work at resonance at the peak of  $V_{in_{max}}$ :

$$a = \frac{\sqrt{2}}{2} \frac{V_{in_{max}}}{V_{out} + V_{Rect}} = \frac{\sqrt{2}}{2} \frac{264}{60+0.5} = 3.086.$$

Step 2. Calculate the output resistance  $R_e$ :

$$R_e = \frac{4}{\pi^2} a^2 \frac{V_{out}^2}{P_{out_{max}}} \left(1 + \frac{V_{Rect}}{V_{out}}\right) = \frac{4}{\pi^2} 3.086^2 \frac{60^2}{120} \left(1 + \frac{0.5}{60}\right) = 116.8 \Omega.$$

Step 3. Calculate the maximum voltage gain  $M_{max}$ :

$$M_{max} = 2a \frac{V_{out} + V_{Rect}}{\sqrt{2} V_{in_{min}}} = 2 \cdot 3.086 \frac{60+0.5}{\sqrt{2} \cdot 88} = 3.$$

Step 4. Calculate  $k$  so that the actual lower resonance frequency is  $f_{R2}$ :

$$k = \left(\frac{f_{R1}}{f_{R2}}\right)^2 - 1 = (2)^2 - 1 = 3.$$

Step 5. Calculate the maximum  $Q_0$  value,  $Q_{max1}$ , necessary to stay in the inductive region at minimum  $V_{in}$  and maximum load:

$$Q_{max1} = \frac{1}{k M_{max}} \sqrt{\frac{M_{max}^2}{M_{max}^2 - 1} + k} = \frac{1}{3 \cdot 3} \sqrt{\frac{3^2}{3^2 - 1} + 3} = 0.226.$$

**Table 18. Exemplary single-stage LLC PFC for LED driver: electrical specification**

Symbol	Name	Value	Unit
$V_{in_{min}} - V_{in_{max}}$	Input voltage range (rms values)	88 - 264	Vac
$V_{out}$	Regulated output voltage	60	Vdc
$V_{Rect}$	Secondary rectifier forward drop	0.5	Vdc
$P_{out_{min}} - P_{out_{max}}$	Output power range	0 - 120	W
$\eta$	Estimated efficiency @ $P_{out_{max}}, V_{in_{min}}$	91	%
$f_{R1}$	Upper resonance frequency	200	kHz
$f_{R2}$	Lower resonance frequency	100	kHz
$C_{HB}$	Half bridge midpoint estimated capacitance	150	pF
$T_D$	Dead-time	300	ns
$C_p$	Secondary-side parasitic capacitance (est.)	2	nF

Step 6. Calculate the maximum  $Q_0$  value,  $Q_{max2}$ , to ensure ZVS at zero load and maximum  $V_{in}$ :

$$Q_{max2} = \frac{2}{\pi} \frac{1}{k} \frac{T_D}{Re C_{HB}} = \frac{2}{\pi} \frac{1}{3} \frac{300 \cdot 10^{-9}}{116.8 \cdot 150 \cdot 10^{-12}} = 3.634 .$$

Step 7. Calculate the maximum  $Q_0$  value,  $Q_{max3}$ , to ensure that the minimum gain requirement is fulfilled:

$$Q_{max3} = \frac{\sqrt{2}}{2} \frac{1}{a} \frac{\sqrt{1+k}}{k} \frac{V_{in_{min}}}{V_{out+V_{Rect}}} = \frac{\sqrt{2}}{2} \frac{1}{3.086} \frac{\sqrt{1+3}}{3} \frac{88}{60+0.5} = 0.222 .$$

Step 8. Choose a value of  $Q_0$ ,  $Q_S$ , such that  $Q_S \leq \min(Q_{max1}, Q_{max2}, Q_{max3})$ :

$$Q_S = 0.2 .$$

Step 9. Calculate the normalized minimum operating frequency at  $V_{in} = V_{in_{min}}$ ,  $P_{out} = P_{out_{max}}$  and  $\theta = \pi/2$ ,  $x_{min}$ :

$$x_{min} \cong \frac{1}{\sqrt{1+k \left( 1 - \frac{1}{M_{max}^{1+\left(\frac{Q_S}{Q_{max1}}\right)^5}} \right)}} = \frac{1}{\sqrt{1+3 \left( 1 - \frac{1}{3^{1+\left(\frac{0.2}{0.226}\right)^5}} \right)}} = 0.538 .$$

Step 10. Calculate the phase-shift  $\varphi_{min}$  of the tank current at  $V_{in} = V_{in_{min}}$ ,  $P_{out} = P_{out_{max}}$  and  $\theta = \pi/2$ , and check if ZVS condition (147) is fulfilled:

$$\varphi_{min} = \tan^{-1} \frac{[1+k+Q_S^2 k^2(x_{min}^2-1)]x_{min}^2-1}{Q_S k^2 x_{min}^3} = \tan^{-1} \frac{[1+3+0.2^2 \cdot 3^2(0.538^2-1)]0.538^2-1}{0.2 \cdot 3^2 \cdot 0.538^3} = 0.29 \text{ rad} ;$$

$$\frac{\varphi_{min}}{2\pi f_{R1} x_{min}} = \frac{0.29}{2\pi \cdot 200 \cdot 10^3} \frac{1}{0.538} = 429 \cdot 10^{-9} \text{ s} > T_D = 250 \cdot 10^{-9} \text{ s} .$$

Step 11. Calculate the characteristic impedance of the tank circuit and all component values:

$$Z_0 = Re Q_S = 116.8 \cdot 0.2 = 23.36 \Omega;$$

$$Cr = \frac{1}{2\pi f_{R1} Z_0} = \frac{1}{2\pi \cdot 200 \cdot 10^3 \cdot 23.36} = 34.1 \text{ nF} ;$$

$$L_S = \frac{Z_0}{2\pi f_{R1}} \frac{23.36}{2\pi \cdot 200 \cdot 10^3} = 18.6 \mu\text{H} ;$$

$$L_p = k L_S = 3 \cdot 18.6 \cdot 10^{-6} = 55.8 \mu\text{H} .$$

Step 12. Considering an integrated magnetics implementation and assuming magnetic circuit symmetry, calculate the parameters of the real transformer:

$$n = a \sqrt{1 + \frac{L_S}{L_p}} = 3.086 \sqrt{1 + \frac{18.6}{55.8}} = 3.563 ;$$

$$L_\mu = \sqrt{L_p L_1} = \sqrt{55.8 (55.8 + 18.6)} = 64.4 \mu\text{H} ;$$

$$L_{L1} = L_1 - L_\mu = 55.8 + 18.6 - 64.4 = 10 \mu\text{H} ;$$

$$L_{L2} = \frac{L_{L1}}{n^2} = \frac{10}{3.563^2} = 0.788 \mu\text{H} .$$

Step 13. Calculate the maximum peak of the tank current to set up the overcurrent means:

$$I_{R1pk} = \frac{\pi}{\sqrt{2}} \frac{P_{out_{max}}}{\eta} \frac{1}{V_{in_{min}} \cos \varphi_{min}} = \frac{\pi}{\sqrt{2} \cdot 0.91} \frac{120}{88 \cos 0.29} = 3.473 \text{ A} .$$

- Post-design checks:

a) Let us calculate the value of  $\Gamma = Cp/Cr$  to assess the effect of  $Cp$ :

$$\Gamma = \frac{Cp}{a^2 Cr} = \frac{2 \cdot 10^{-9}}{3.086^2 \cdot 34.1 \cdot 10^{-9}} = 0.012 .$$

The normalized frequency where no-load gain reverses is:

$$x_V = \sqrt[4]{\frac{1}{k\Gamma}} = \sqrt[4]{\frac{1}{3 \cdot 0.012}} = 2.29 > x_{max} = 2 .$$

Therefore, the initial assumption of considering negligible the effect of  $Cp$  in this design is correct.

b) The ZVS condition check  $Vin = Vin_{min}$ ,  $Pout = Pout_{max}$  has been done based on condition (23). According to the algorithm described in Part II chapter 5, we need to check if (23) is applicable. Let us calculate the value of the switched current in those conditions:

$$|I_{R0}| = I_{R1pk_{max}} \sin \varphi_{min} = 3.473 \cdot \sin 0.29 = 0.993 \text{ A} .$$

The critical value provided by (25), adapted to the ac input case, is:

$$I_{R0crit} = \sqrt{2 \frac{C_{HB}}{L_s}} Vin_{min} = \sqrt{2 \frac{150 \cdot 10^{-12}}{18.6 \cdot 10^{-6}}} 88 = 0.353 \text{ A} .$$

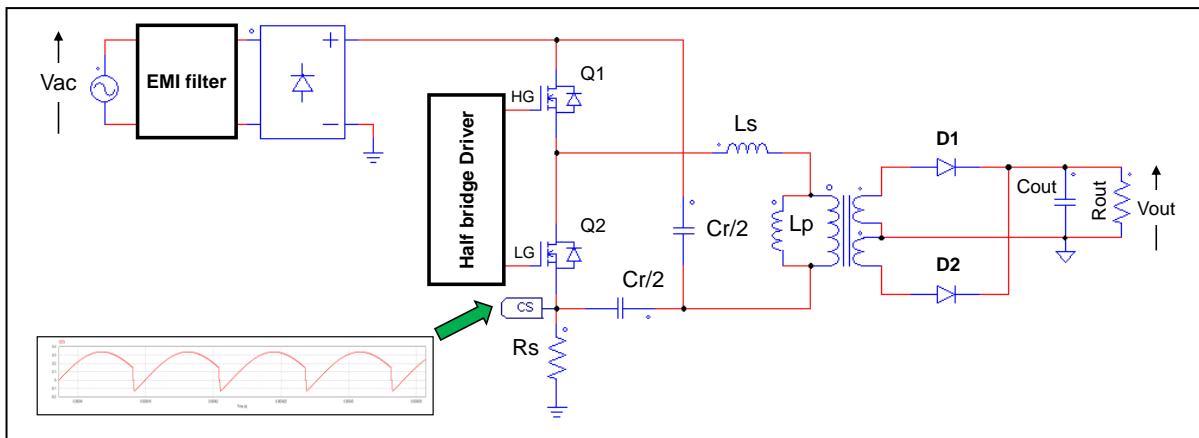
$|I_{R0}|$  is more than twice larger than the critical value, then (23) is acceptable.

### Single-stage LLC PFC control strategy

Among the available control techniques for resonant converters, average current mode control (ACMC) is the most suitable. DFC control, though not limiting the dynamic behavior of such a system (it is worth reminding that a PFC stage is a narrow bandwidth system, typically  $< 20$  Hz), is not applicable: the frequency profile in a line half-cycle is a too complex function of the input voltage, the output load, and the instantaneous phase angle  $\theta$  to be programmed directly.

To conveniently apply ACMC to the half bridge single-stage LLC PFC, it is necessary to properly configure the power circuit. The suggested configuration is that with split resonant capacitors shown in figure 204 and already discussed in Part II, Chapter 1. Notice how the sense resistor is connected, which allows the tank current to flow in the sense resistor  $Rs$  during both half cycles with the same (positive) sign. This makes the extraction of the average input current much easier and cleaner: a sense resistor in series to the tank circuit would result in zero average current, while sensing the input current only in the half-cycle where the high-side switch is on would result in an asymmetrical tank current.

**Figure 204. Single-stage LLC-PFC: power circuit reference schematic.**



ACMC is based on two nested loops: the inner current loop and the outer voltage loop, like in fixed-frequency CCM-operated boost PFC converters. The purpose of the current loop is to make the average input current closely track a sinusoidal reference, typically obtained from the rectified input voltage and properly adjusted in amplitude. The purpose of the voltage loop is to regulate the output voltage by properly setting the amplitude of the sinusoidal reference for the inner current loop. This structure is shown in the block diagram of figure 205.

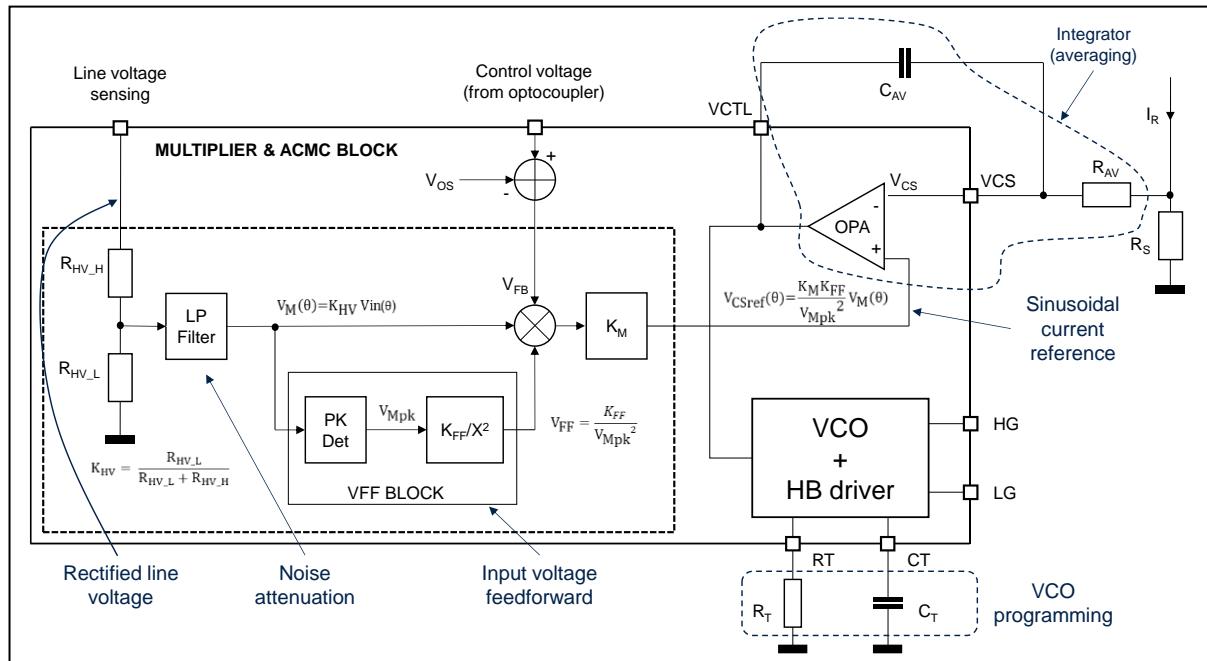
The output of the multiplier provides the current sense reference voltage  $V_{CSref}$ , by multiplying the feedback voltage  $V_{FB}$  coming from the voltage loop by a scaled down rectified input voltage to program the sinusoidal shape for the input current.

The VFF (voltage feedforward) block makes the feedback voltage  $V_{FB}$  dependent only on the output power level, eliminating the dependence on the input voltage.

The OPA, configured as an integrator, compares the current sense reference to the averaged voltage across the sense resistor  $R_s$ , connected as shown in figure 204. The output of the OPA is the control voltage of the VCO that determines the switching frequency of the converter. Finally, the driver logic block drives the MOSFETs of the half bridge.

The outer loop can be based on a traditional TL431 + optocoupler arrangement like that shown in figure 132: in fact, ACMC makes type-2 amplifier viable.

**Figure 205. Single-stage LLC PFC: ACMC control loop block diagram.**



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