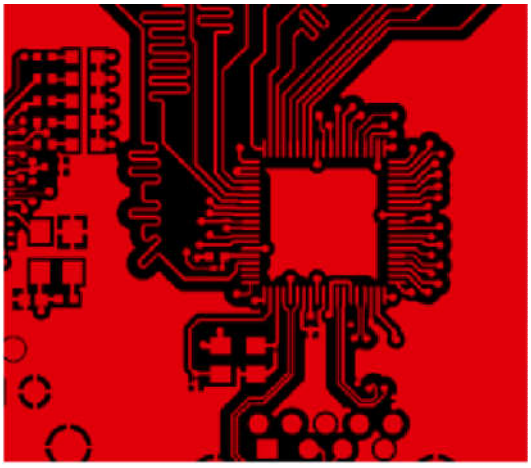
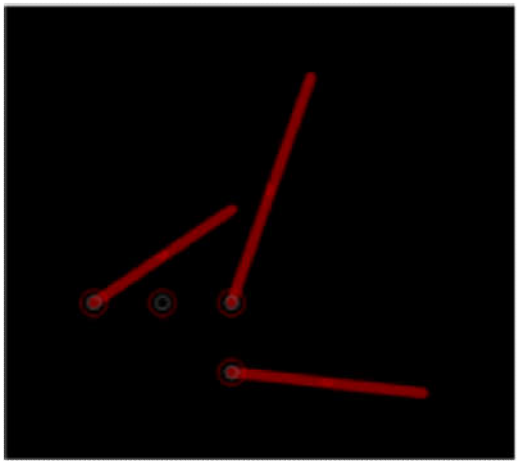
31 PCB Design and Layout Tips

1. Trace length should include the length of vias and pads.

2. The trace angle is preferably 135°. Tracing out at any angle will cause processing problems in PCB manufacturing.

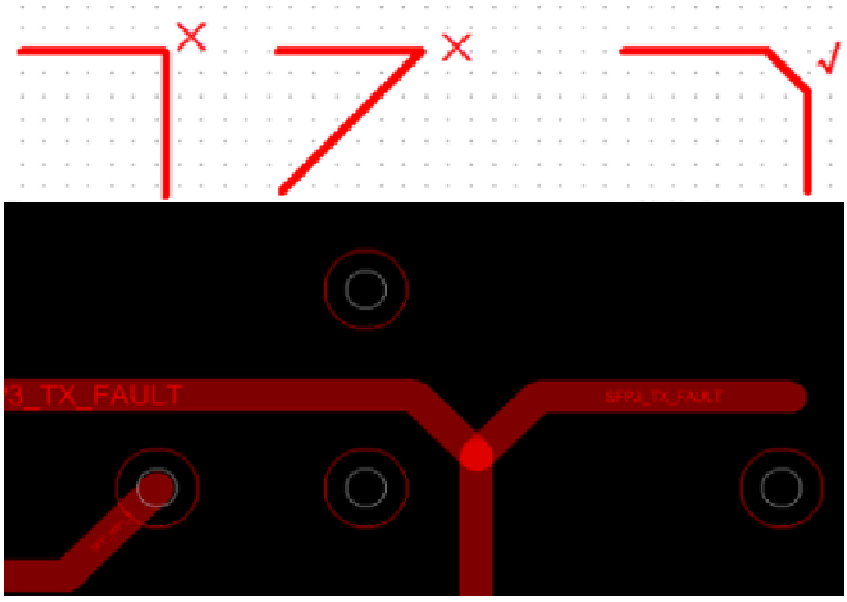


Preferred

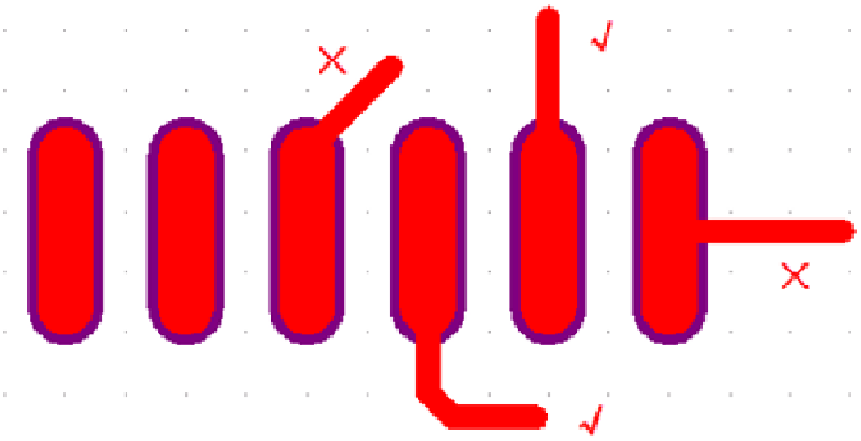


Not Suggested

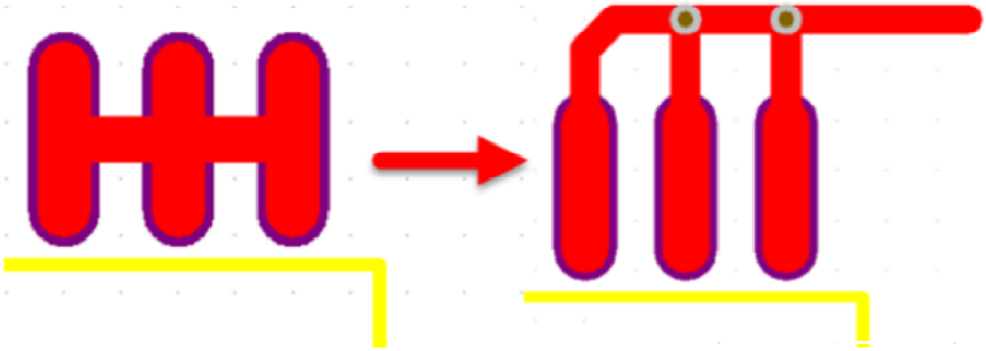
3. Avoid trace at right angles or acute angles, which will cause line width changes at corners and impedance changes, causing signal reflection, as shown in the figure below.



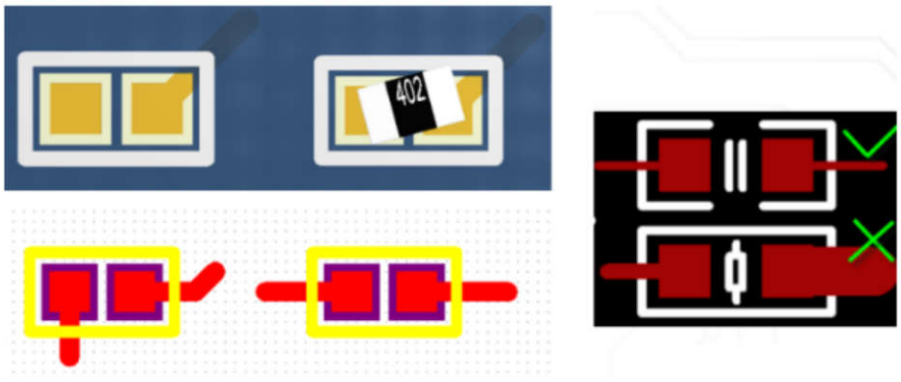
4. The trace should be routed from the long direction of the pad and avoid the width direction or the four corners of the pad. The corners of the trace should be at least 6 mil away from the pad position, as shown in the figure below.



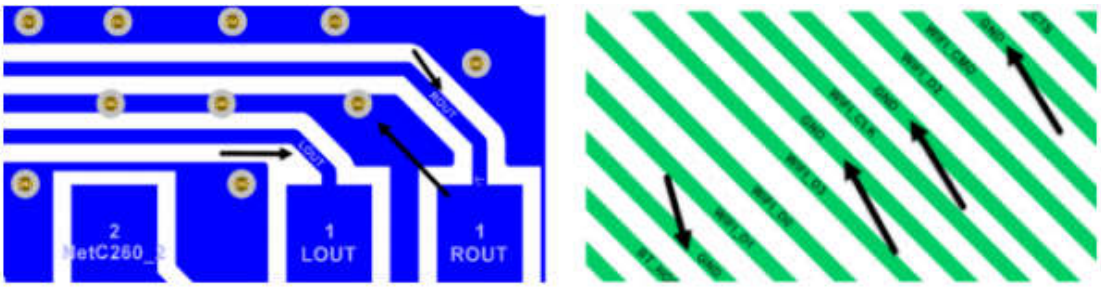
5. As shown in the figure below, adjacent pads are on the same network and cannot be directly connected. It needs to connect the pads first and then connect them. Direct connection is easy to connect with tin during manual soldering.



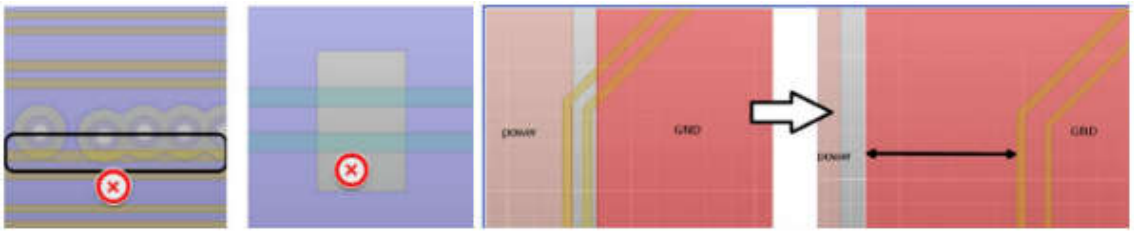
6. For small CHIP devices, pay attention to the symmetry of the trace and keep the trace width at both ends consistent. For example, if one pin is covered with copper, the other pin should also be covered with copper as much as possible to reduce the drift and rotation of the device after component placement, as shown in the figure below .



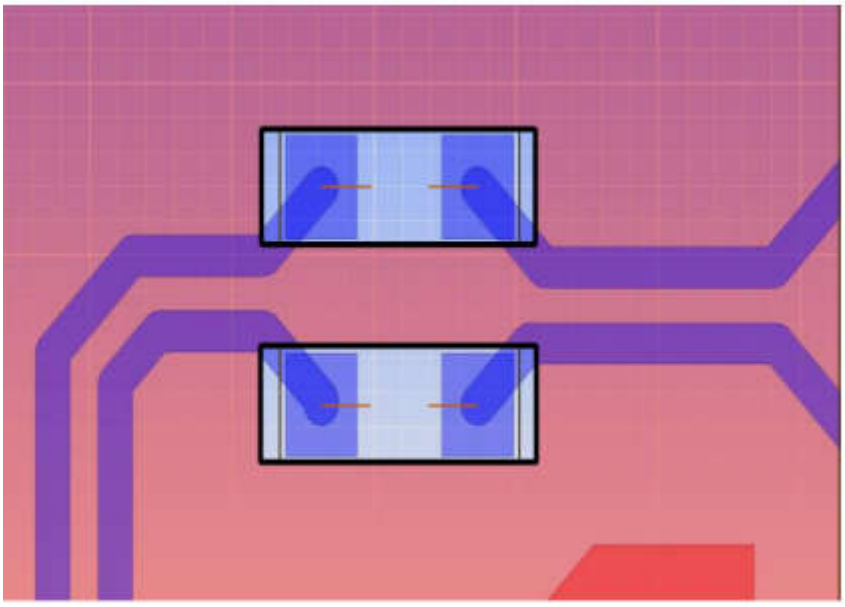
7. For signals that require grounding, the integrity of the grounding must be ensured, and GND holes should be drilled on the grounding line as much as possible. The distance between the two GND holes should not be too far, and should be kept around 50-150mil, as shown in the figure below.



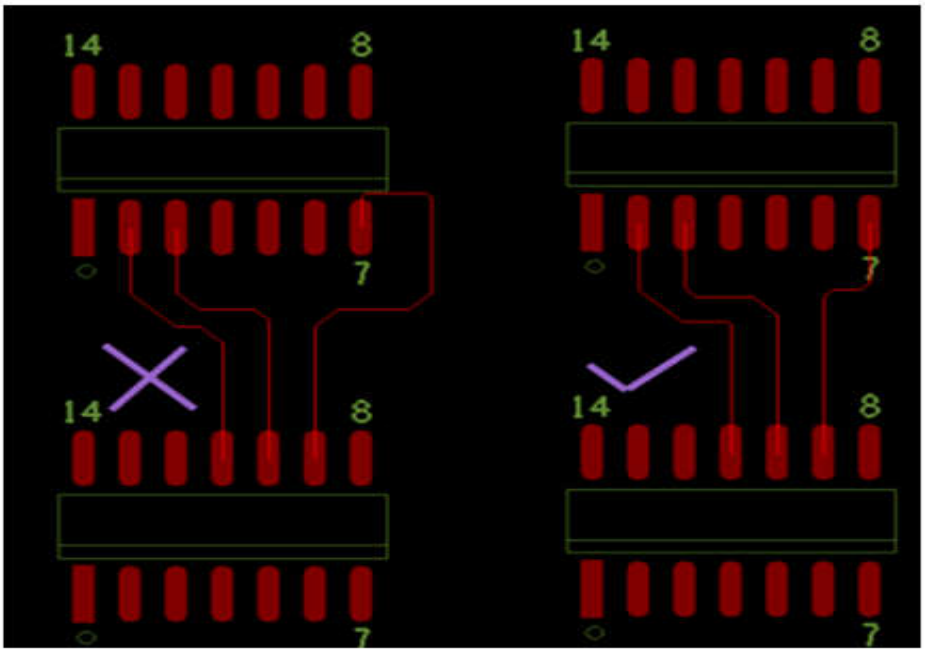
8. The trace should have a complete and continuous reference layer plane to avoid high-speed signal crossover. It's recommended that high-speed signals be at least 40mil from the edge of the reference plane, as shown in the figure below.



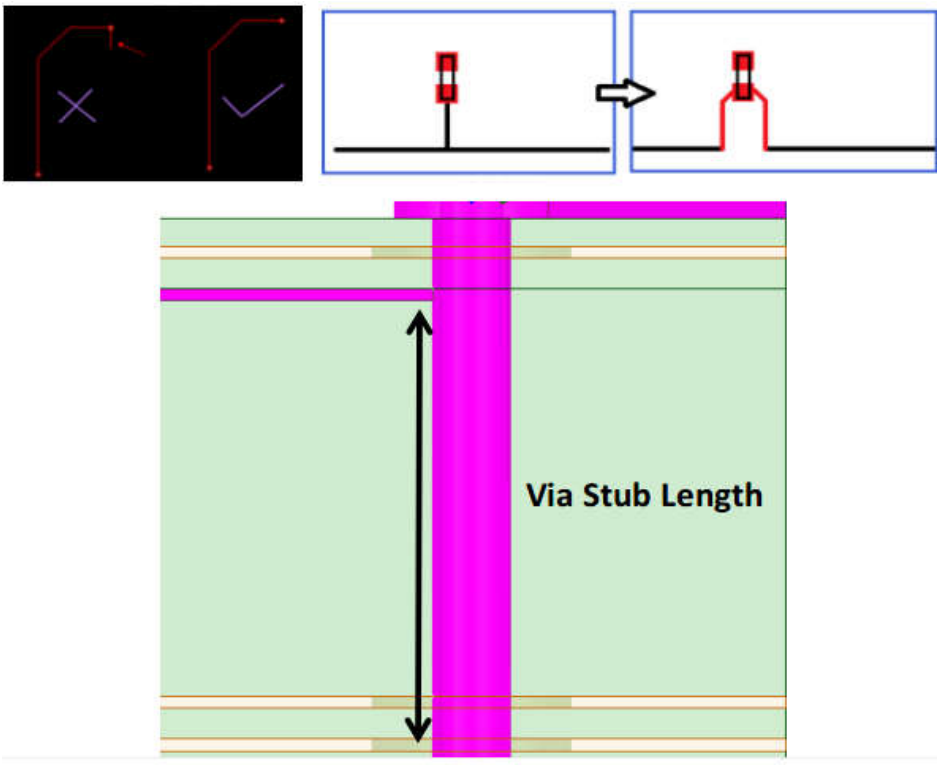
9. Since the SMD pad will cause the impedance to decrease, in order to reduce the impact of sudden impedance changes, it's recommended to dig out a reference layer according to the size of the pad directly below the surface mount pad. Commonly used SMD include: capacitors, ESD, common mode suppression inductors, connectors, etc., as shown in the figure below.



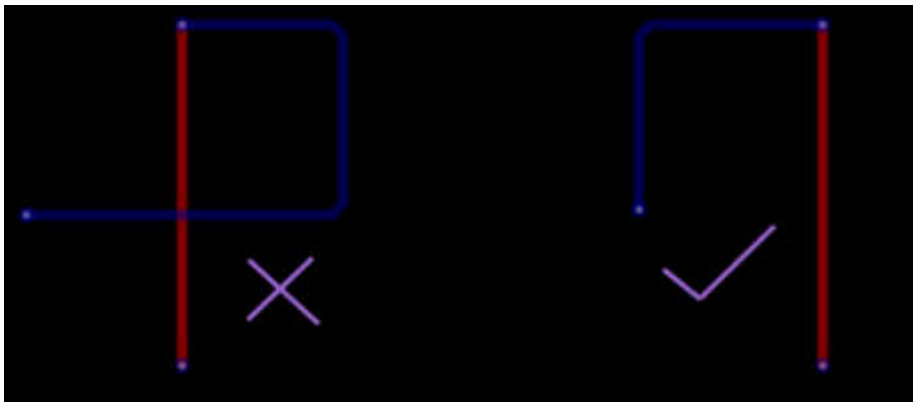
10. As shown in the figure below, the loop area formed by the signal line and its loop should be as small as possible. The loop area is small, the external radiation is small, and the interference received from the outside is also small.



11. As shown in the figure below (top), STUB is not allowed in the trace. The length of the stub should be minimized. It's recommended that the length of the stub be zero. And to avoid the via stub effect, especially when the stub length exceeds 12 mil, it's suggested to evaluate the impact of via stubs on signal integrity through simulation, as shown in the figure below (bottom)

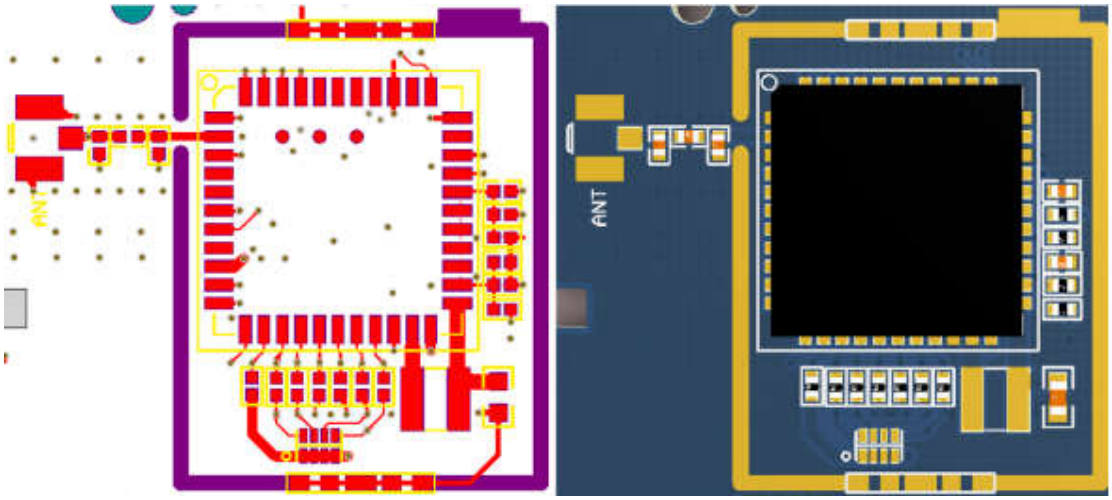


12. Try to avoid traces forming self-loops on different layers. Such problems are prone to occur in multi-layer board designs, and self-loops will cause radiation interference. As shown below.



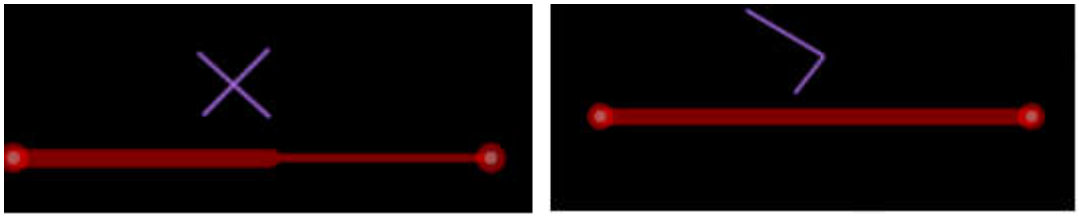
13. Not to place test points on high-speed signals.

14. For signals that will cause interference or are sensitive (such as radio frequency signals), a shielding can must be planned. The width of the shielding cover is generally 40mil (generally kept above 30mil, which can be confirmed with the customer manufacturer). Make as many GND vias as possible on the shielding can to increase its welding effect.

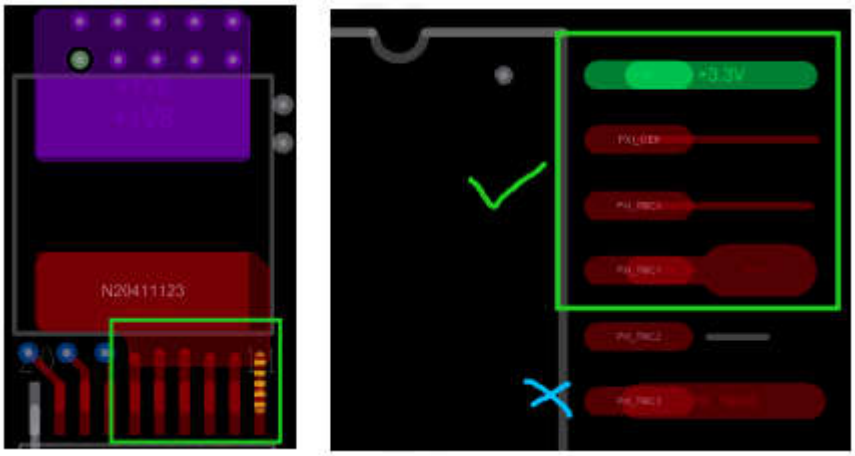


15. The trace must be connected to the pad, center of the via.

16. The trace width of the same network should be consistent. Changes in trace width will cause uneven trace characteristic impedance, and reflection will occur when the transmission speed is high. Under certain conditions, such as connector lead wires and BGA package lead wires with similar structures, it may be impossible to avoid trace width changes because the spacing is too small. The effective length of the inconsistent part in the middle should be minimized, as shown in the figure below.



17. The trace width of the IC pin outlet must be less than or equal to the pad width, and the outlet width cannot be larger than the pad width. Due to current carrying requirements for some signals, the wider trace can first be kept consistent with the pin width, and then the trace width can be thickened about 6-10 mil after the layout is led out of the pad, as shown in the figure below.



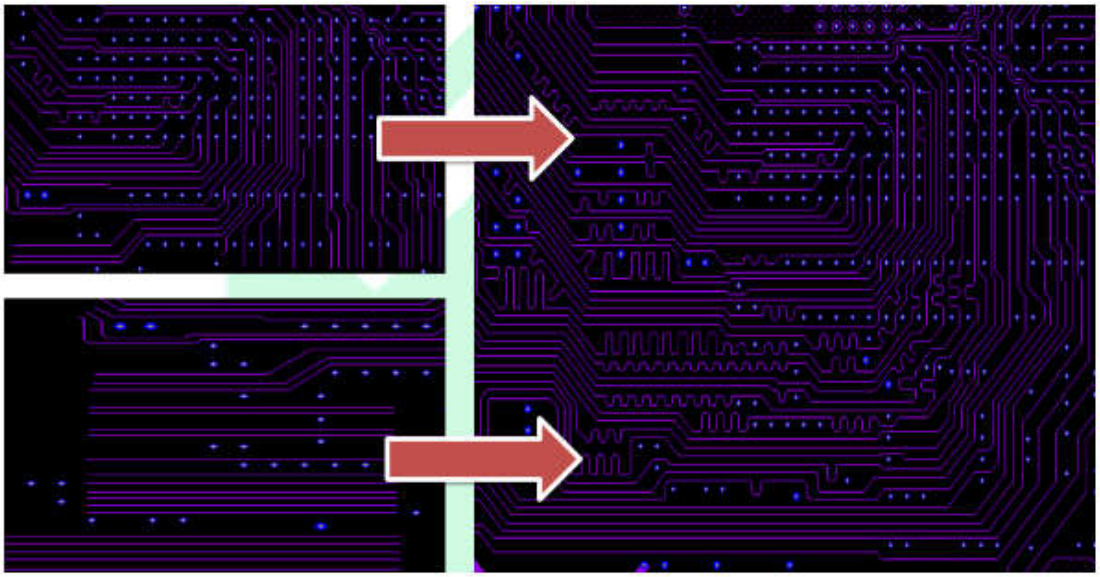
18. If the design contains multiple DDR or other memory chips, the layout must be confirmed with the customer and whether there is a reference document.

19. The series resistor should be placed close to the sending end device, and the terminating resistor should be placed close to the end. For example, the series resistor on the eMMC clock signal is recommended to be placed close to the CPU side (within 400mil).

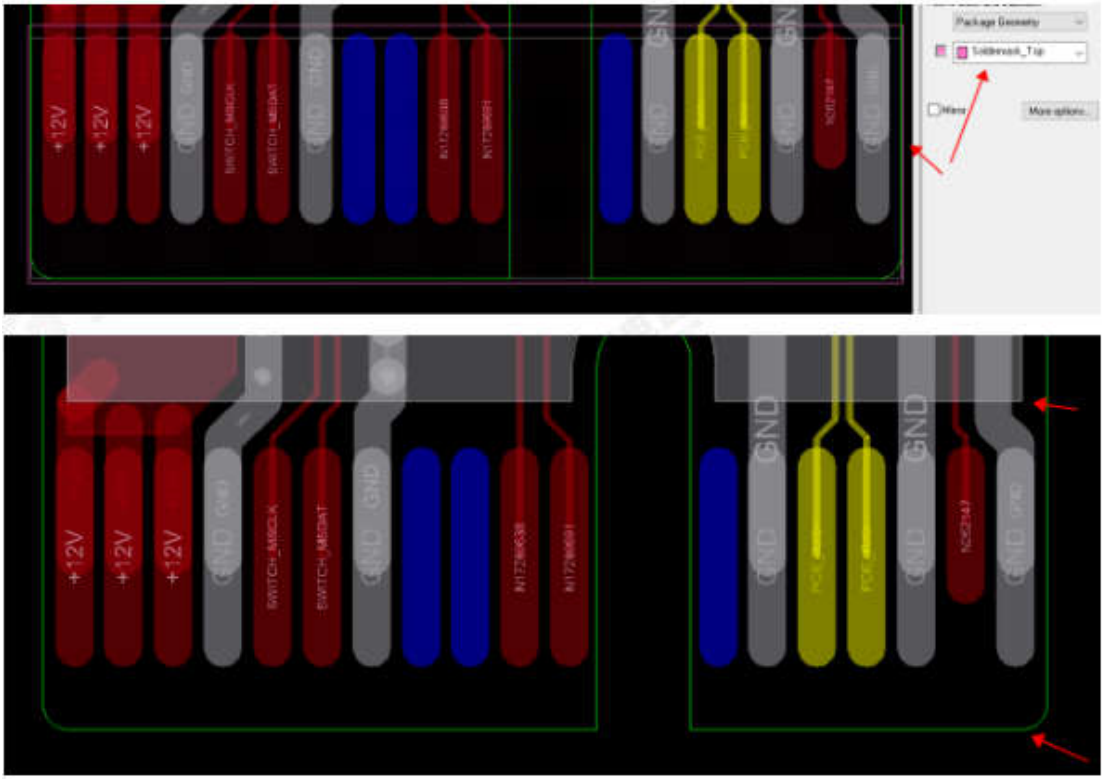
20. If there is a high-voltage signal, the creepage distance must be ensured. The specific parameters are as shown in the figure below.

1) Creepage distance		2)Electrical clearance
1. General AC-DC power supply (120VAC-240VAC)		
L→N	3.2 Before insurance	2.5
	2.5 After insurance	2.0
Primary→Ground	3.4	2.5
Rectifier bridge Before→After	2.5	2.0
F(front)→F(back)	3.2	2.5
MOS→Ground	4.0	2.8
Primary→Secondary	8.0	5.0
Secondary→Ground	1.4	0.7
2. With PFC circuit AC-DC		
Primary→Ground	4.5	2.7
Primary→Secondary	9.0	5.4
3. Power supply above 60V, below 100V DC-DC		
Primary→Secondary	3.5	2.0
Primary→Ground	1.8	1.0
Insurance V+→V-	1.8	1.0

21. Layout should plan the channel situation at the bottleneck in advance, and reasonably plan the trace capacity at the narrowest point of the channel.

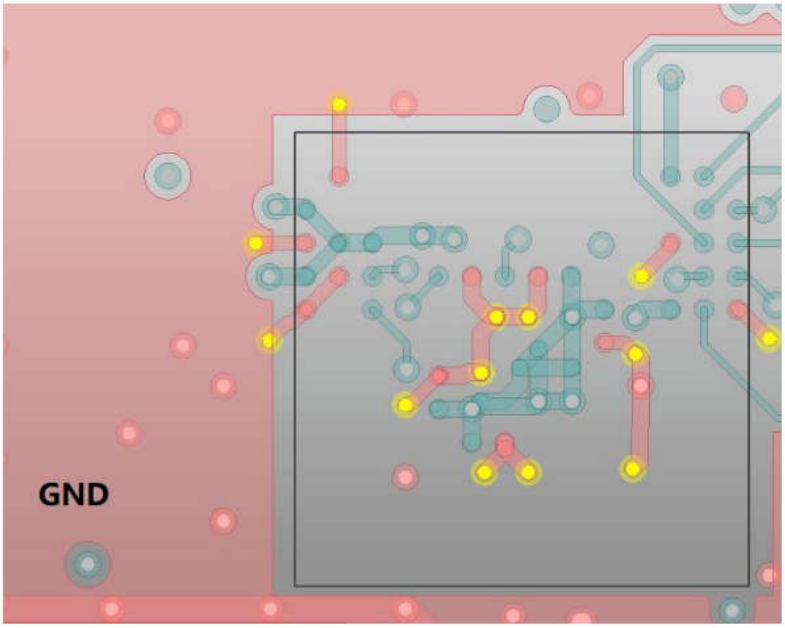


22. The gold finger area needs to be opened as a whole window. When designing multi-layer boards, the copper on all layers below the gold finger should be hollowed out. The distance between the hollowed ground copper and the board frame is generally more than 3mm.

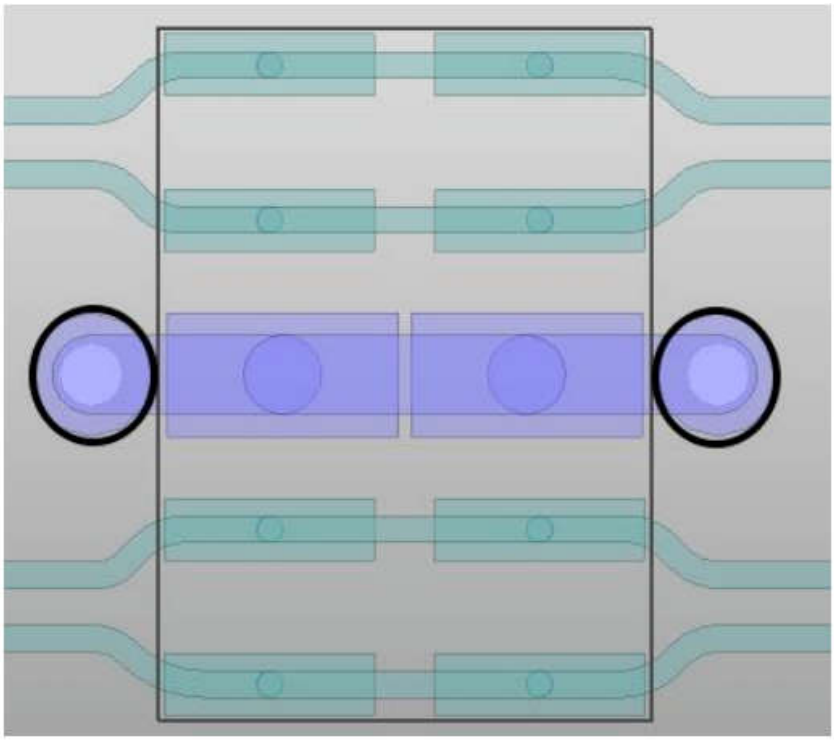


23. Place the coupling capacitor as close to the connector as possible.

24. It's recommended to drill a ground through hole on each ground pad of the IC (such as eMMC, FLASH, etc.) to effectively shorten the reflow path, as shown in the figure below.

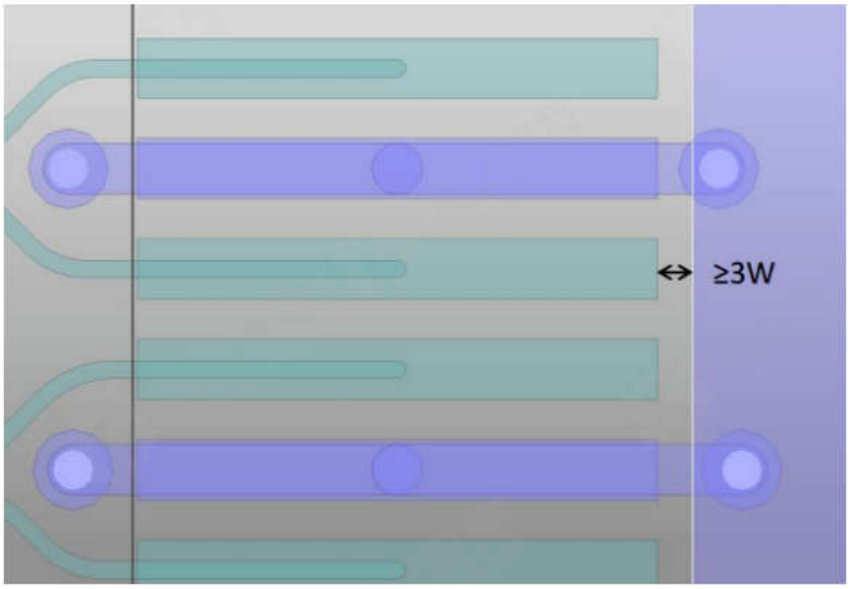


25. It's recommended that each ground pad of the ESD device be drilled with a ground through hole, and the through hole should be as close to the pad as possible, as shown in the figure below.

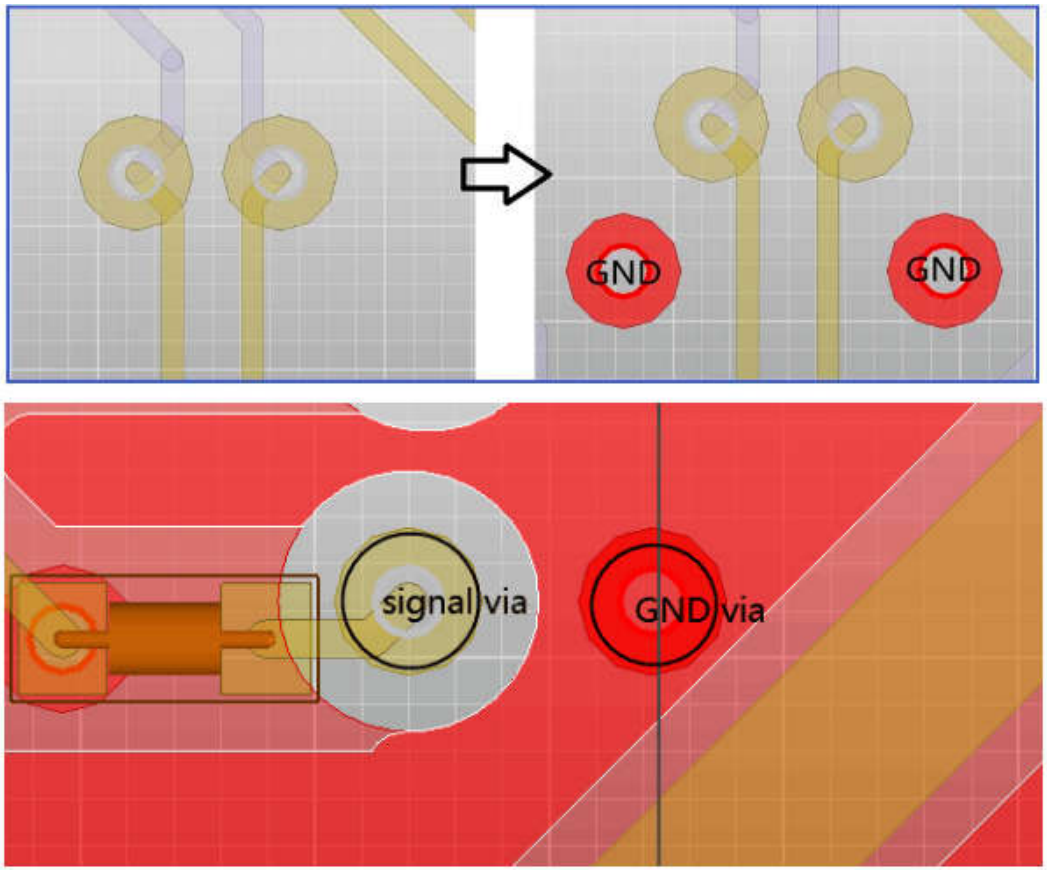


26. Avoid traces around clock devices (such as crystals, crystal oscillators, clock generators, clock distributors), switching power supplies, magnetic devices, plug-in vias, etc.

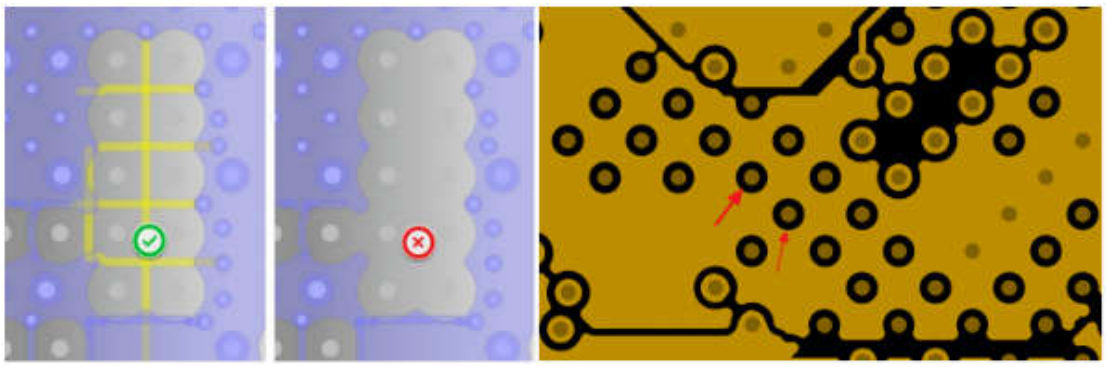
27. The distance between the ground copper of the connector and the signal PAD must be at least 3 times the line width, as shown in the figure below.



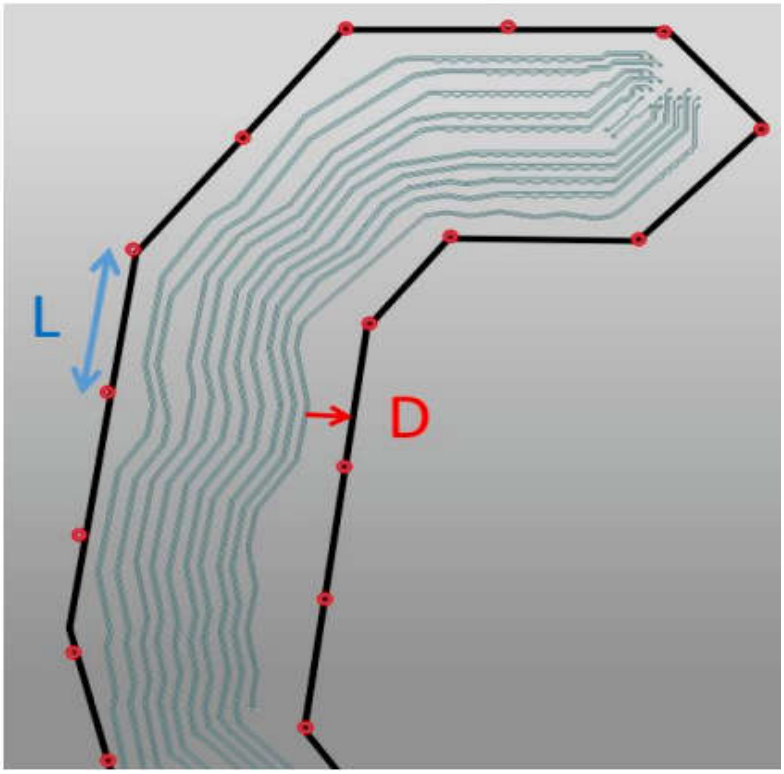
28. When the trace layer is changed and the reference layer before and after the layer change is the ground plane, a companion via needs to be placed next to the signal via to ensure the continuity of the return path. For differential signals, signal vias and return vias should be placed symmetrically, as shown in the figure below (top); for single-ended signals, it's recommended to place a return via next to the signal via to reduce crosstalk between vias, as follows As shown in the figure (below).



29. Use traces to connect the plane disconnections in the BGA area, or shave pad to avoid damaging the plane integrity, as shown in the figure below.



30. When PCB layout needs to be grounded, the recommended grounding method is as follows, as shown in the figure below. L is the spacing between the ground wire and the via hole; D is the distance between the ground wire and the signal line. It is recommended that ≥4*W.



31. Some important high-speed single-ended signals, such as clock signals, reset signals, etc. (such as emmc_clk, emmc_datastrobe, RGMII_CLK, etc.) are recommended to be grounded. The ground trace must be drilled with at least one ground hole every 500 mil, as shown in the figure below.