



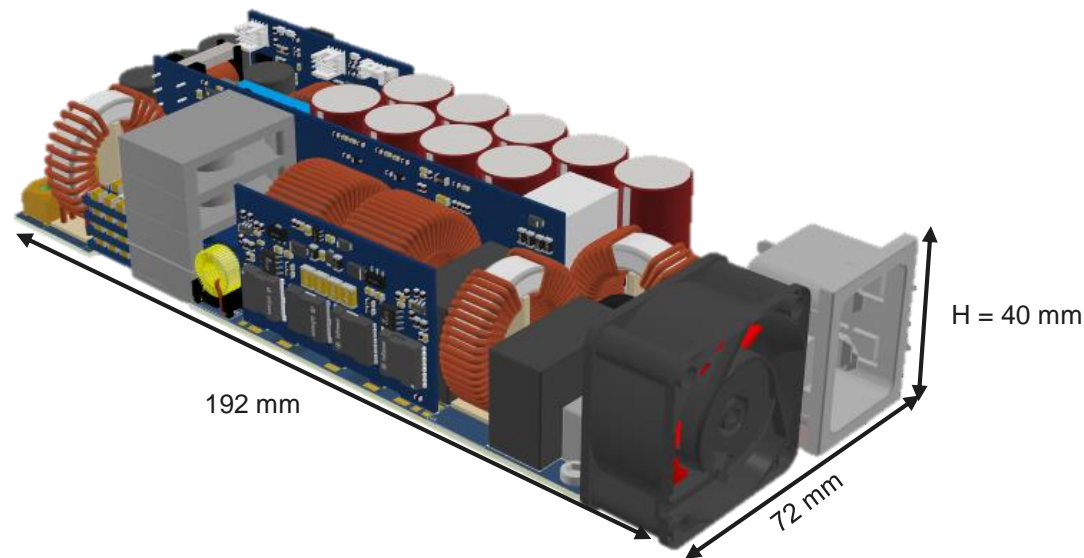
500 kHz high density 3 kW GaN rectifier for server and telecom applications

April 2024



3 kW high frequency and high power density (HF/HD) rectifier

REF_3K3W_HFHD_PSU

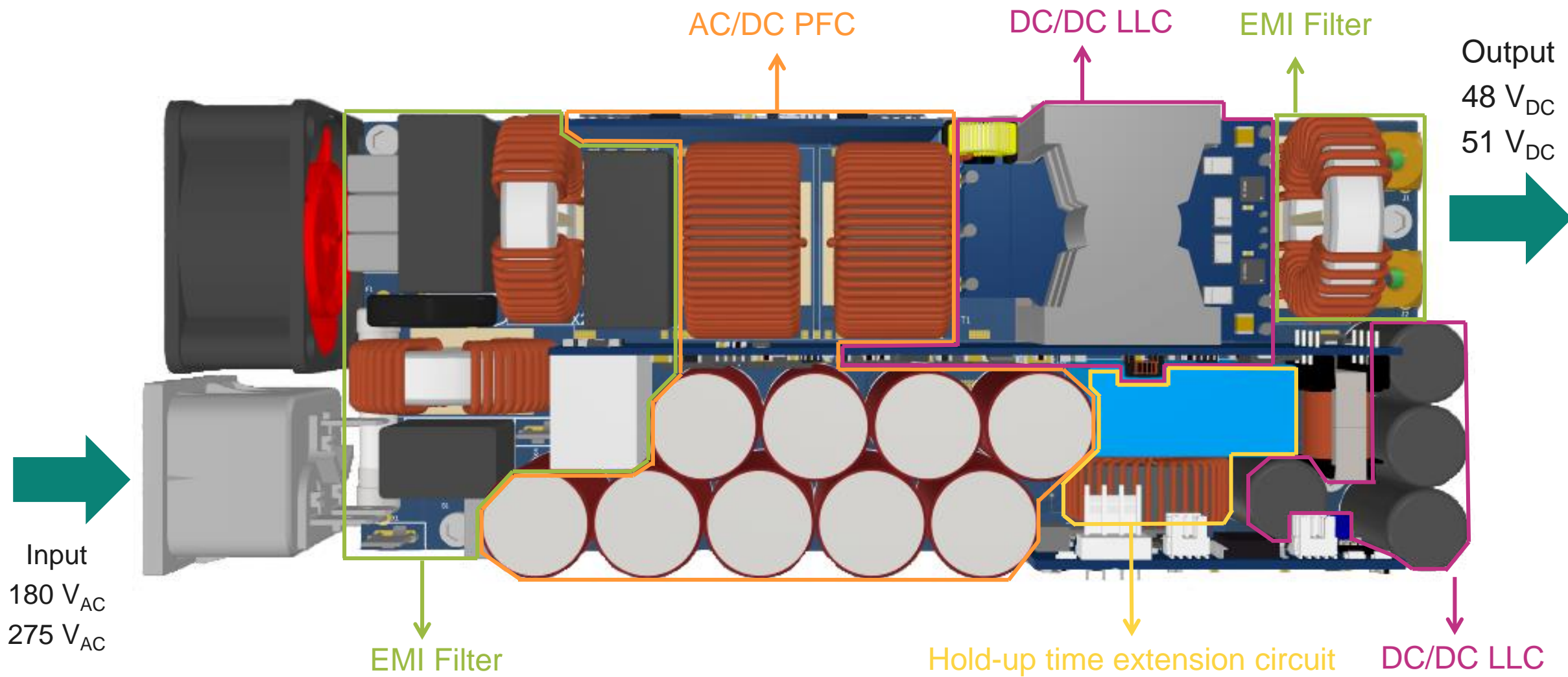


Parameter	Value
Input voltage range	180 V _{AC} ~ 275 V _{AC}
Output voltage range	51 - 48 V _{DC}
Output current nominal	@ 51 V = 65 A @ 50 V = 66 A @ 48 V = 69 A
Output power maximum	3300 W
Efficiency target	~97.5 % (without fan)
Power factor (load > 10%)	PF > 0.95 @ 180 ~ 275 V _{AC} iTHD < 10 % @ 180 ~ 275 V _{AC}
Ambient temperature	0 °C to 50 °C
LLC Resonant frequency	530 kHz
Learn more	
Infineon components	IMT65R057M1H, IGT60R042D1, IPT60R022S7, IPT60R080G7, IDL10G65C5, 2EDB9259Y, 1EDN8511B, 1EDN8550B, 1EDB8275F, IQE046N08LM5, ICE2QR2280G, BAT46WJ, BAT165, BSS138N, XMC4200, TLS4120D0EPV33, 4DIR1400H
Application	Industrial SMPS, Telecom Rectifier

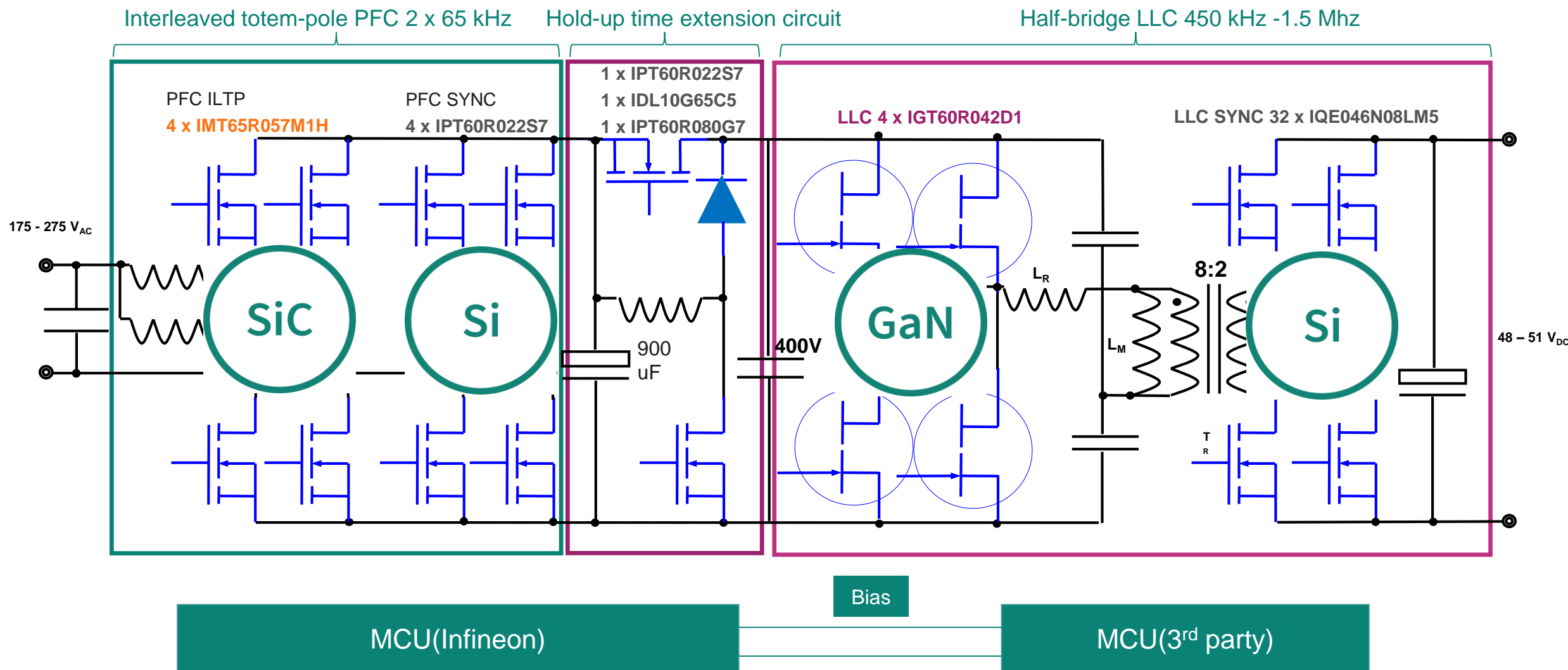
Features
<ul style="list-style-type: none">– Benchmark 97.4% of efficiency: ~96W/in³ in 1U form-factor– Highest efficiency & power density with CoolMOS™, CoolSiC™, CoolGaN™– Custom integrated planar magnetic construction– Full digital control (PFC and DCDC)– Totem-pole SiC PFC + half-bridge GaN LLC

Benefits
<ul style="list-style-type: none">– Full Infineon semiconductor solution– Complete power supply unit (PSU) including PFC + DCDC– High efficiency, custom and in-house design integrated magnetics– Hold up time extension circuit

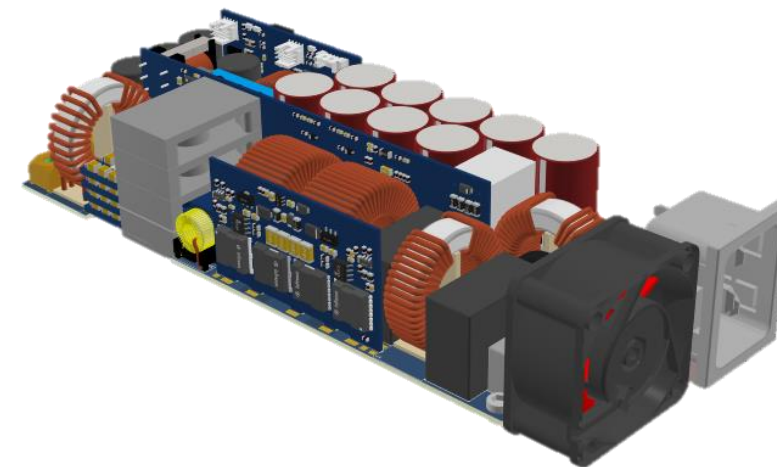
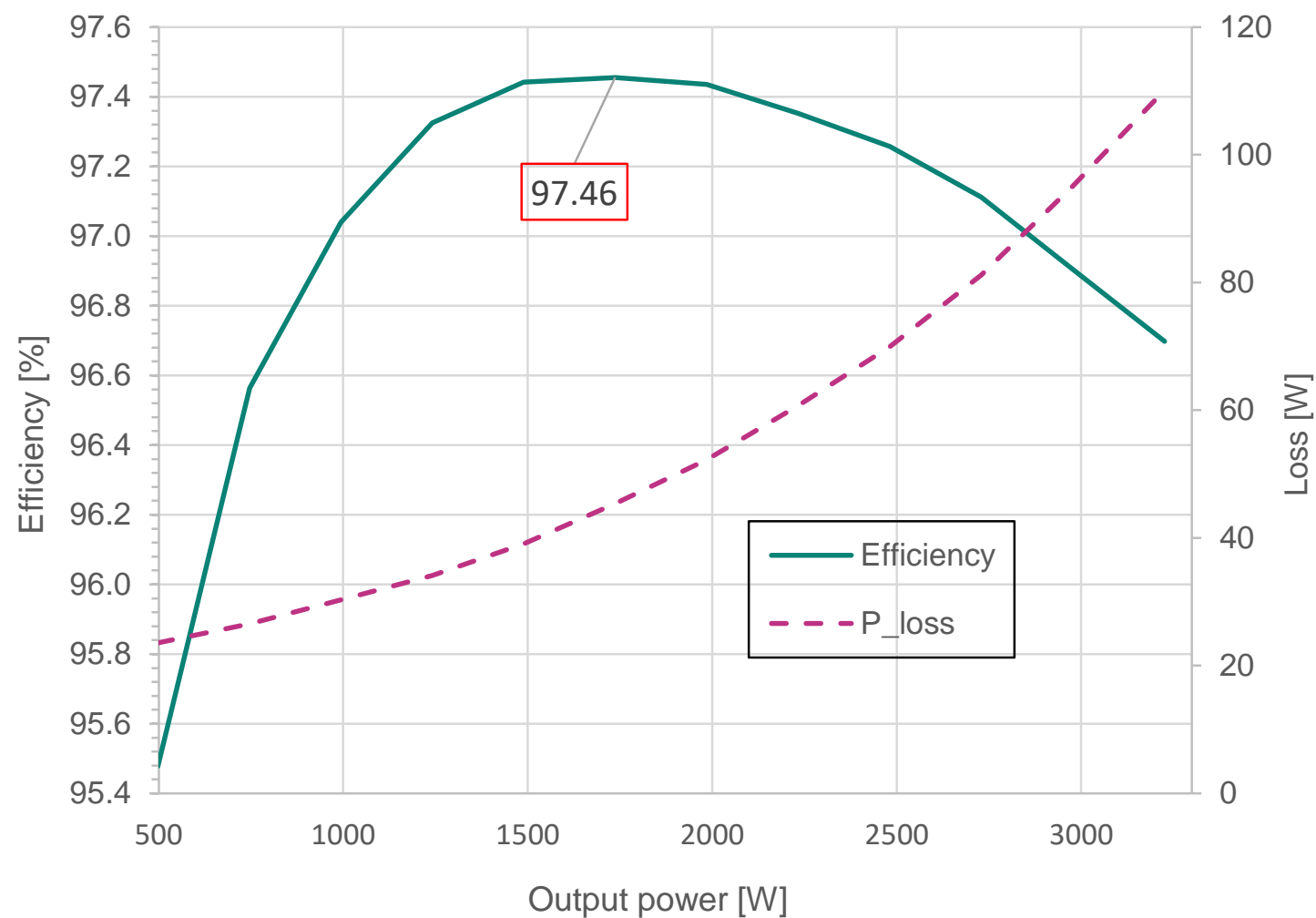
Board hardware overview



Basic schematic of the HF/HD rectifier



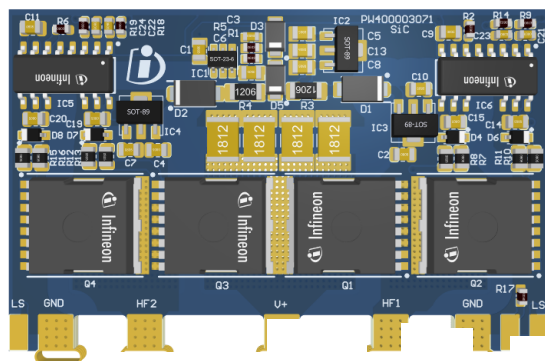
Measured efficiency of the full PSU



- Measurement conditions:
- $V_{in} = 230 V_{AC}$
 - $V_{out} = 50 V_{DC}$
 - I_{out} up to 65 A

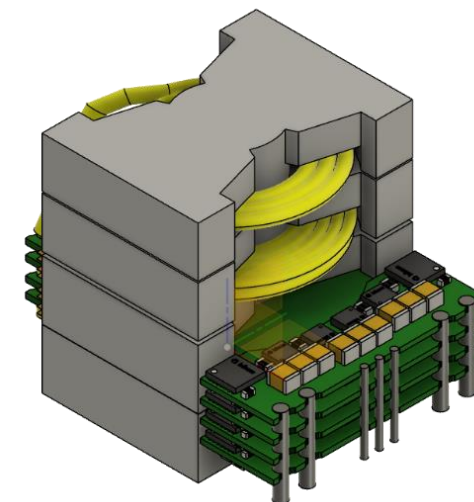
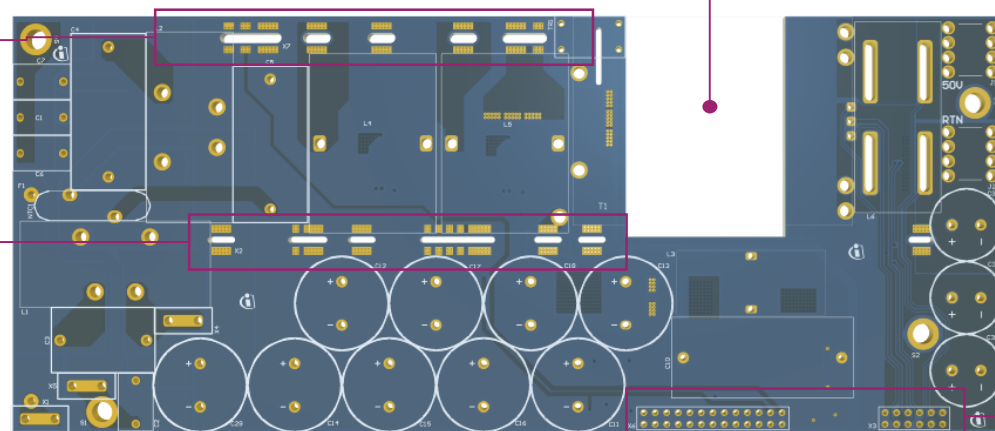
Sub-assembly

Overview of the sub-assembly

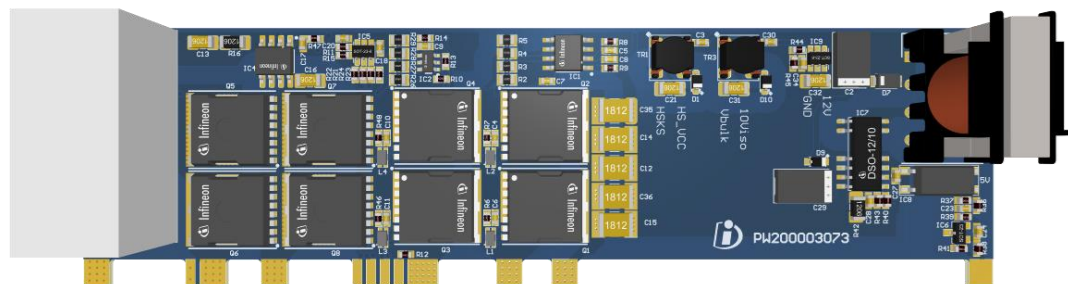


Interleaved totem-pole PFC

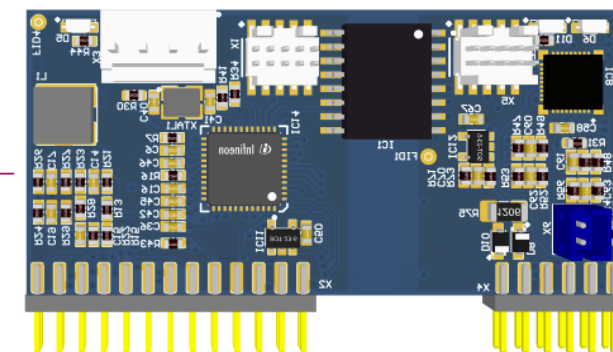
Main board, input and output EMI filters, electrolytic capacitors, hold up time circuit.



Main transformer, series inductor, parallel inductor and including rectifiers.



Half Bridge LLC, auxiliary fly-back and totem-pole grid rectifiers



PFC and LLC control card

The schematic diagram illustrates the driver circuitry for two phases, Phase A and Phase B, using 2EDB9259Y ICs.

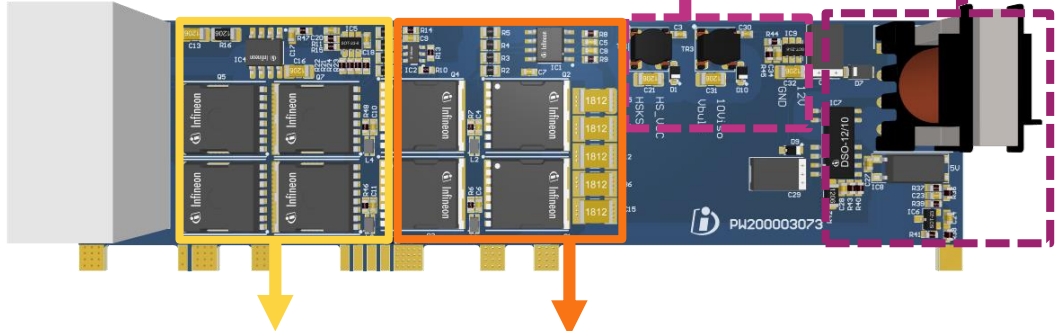
Phase A (Top): The IC6 (2EDB9259Y) is configured with inputs INA, INB, VDDI, GNDI, DISABLE, STP/DTC, NC, and VDDI. The outputs are OUTA (13), OUTB (10), and GND (9). The circuit includes components like R9, R14, C21, C23, C9, R2, C14, and C15. The power supply is 18V (PRI_18V) and 50V (50V X7R).

Phase B (Bottom): The IC5 (2EDB9259Y) is configured with inputs INA, INB, VDDI, GNDI, DISABLE, STP/DTC, NC, and VDDI. The outputs are OUTA (13), OUTB (10), and GND (9). The circuit includes components like R18, R19, C22, C24, C1, R6, C19, and C20. The power supply is 18V (PRI_18V) and 50V (50V X7R).



Half-bridge LLC daughter card

2 x isolated bias for GaN LLC high-side primary 3 x V_{out} fly-back
+ baby-boost disconnect switch



PFC LF SRs

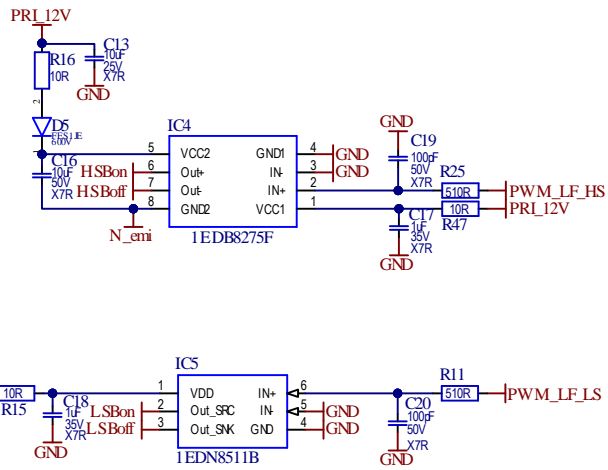
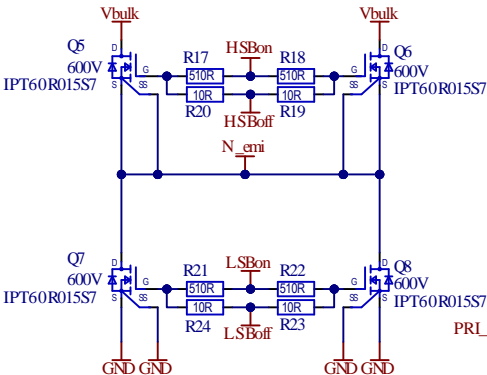
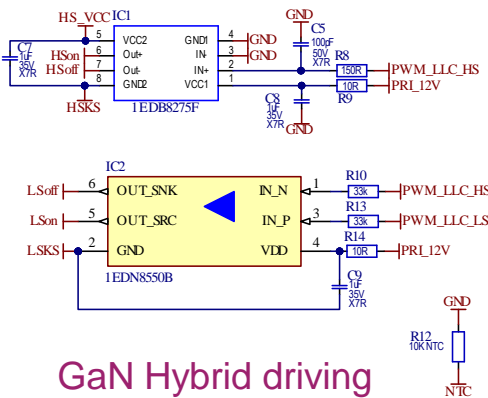
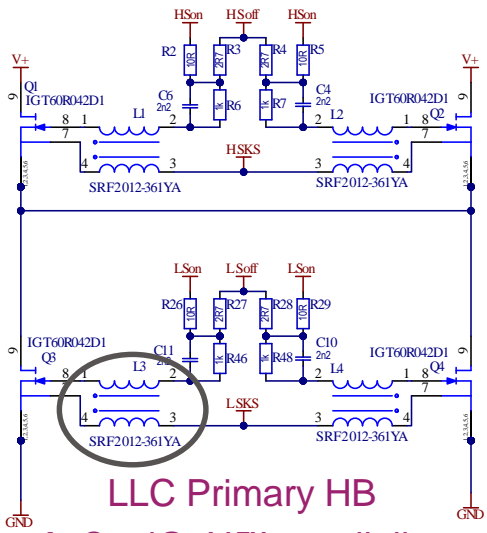
LLC primary HB

CoolMOS™ SJ
MOSFET S7
IPT60R015S7

42 mΩ CoolGaN™
power transistor 600 V
IGT60R042D1

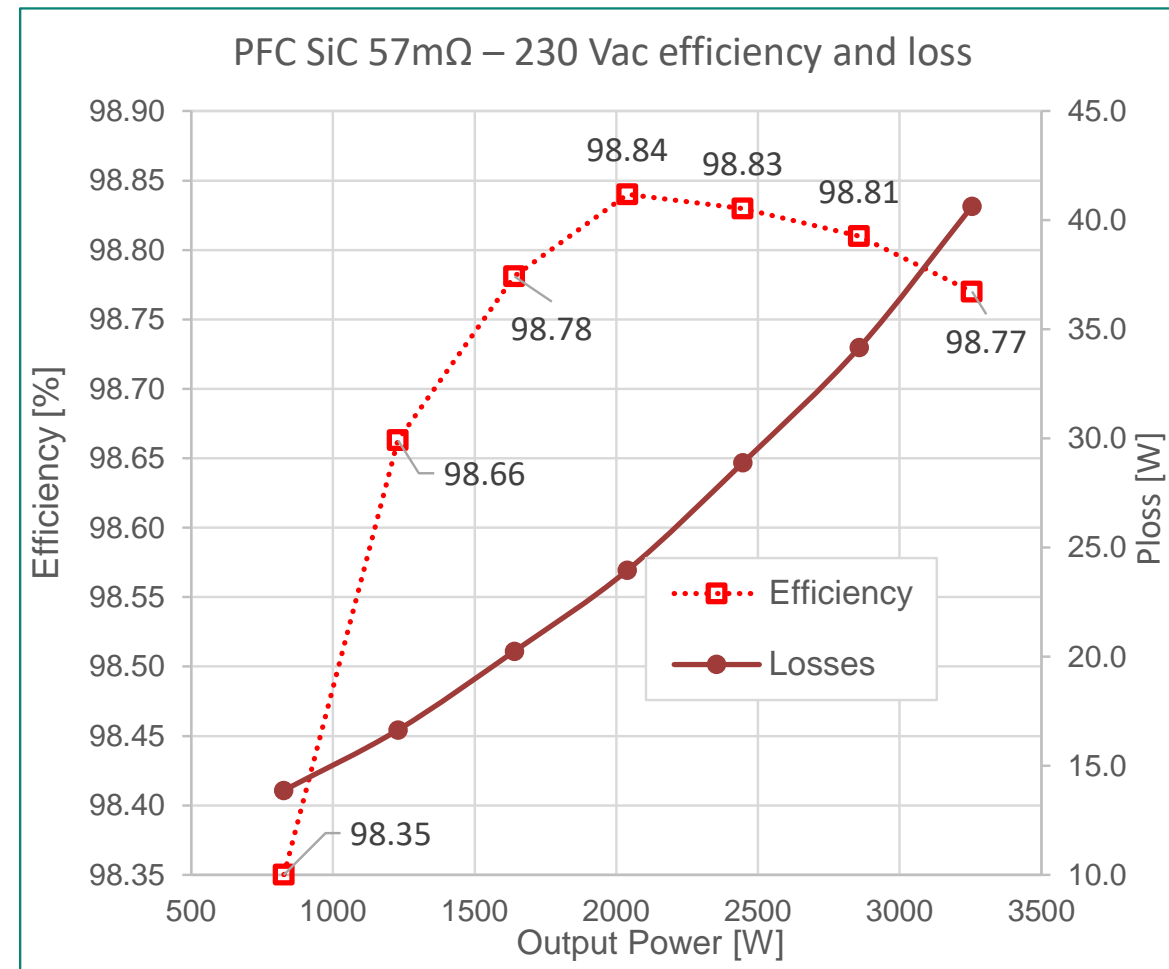
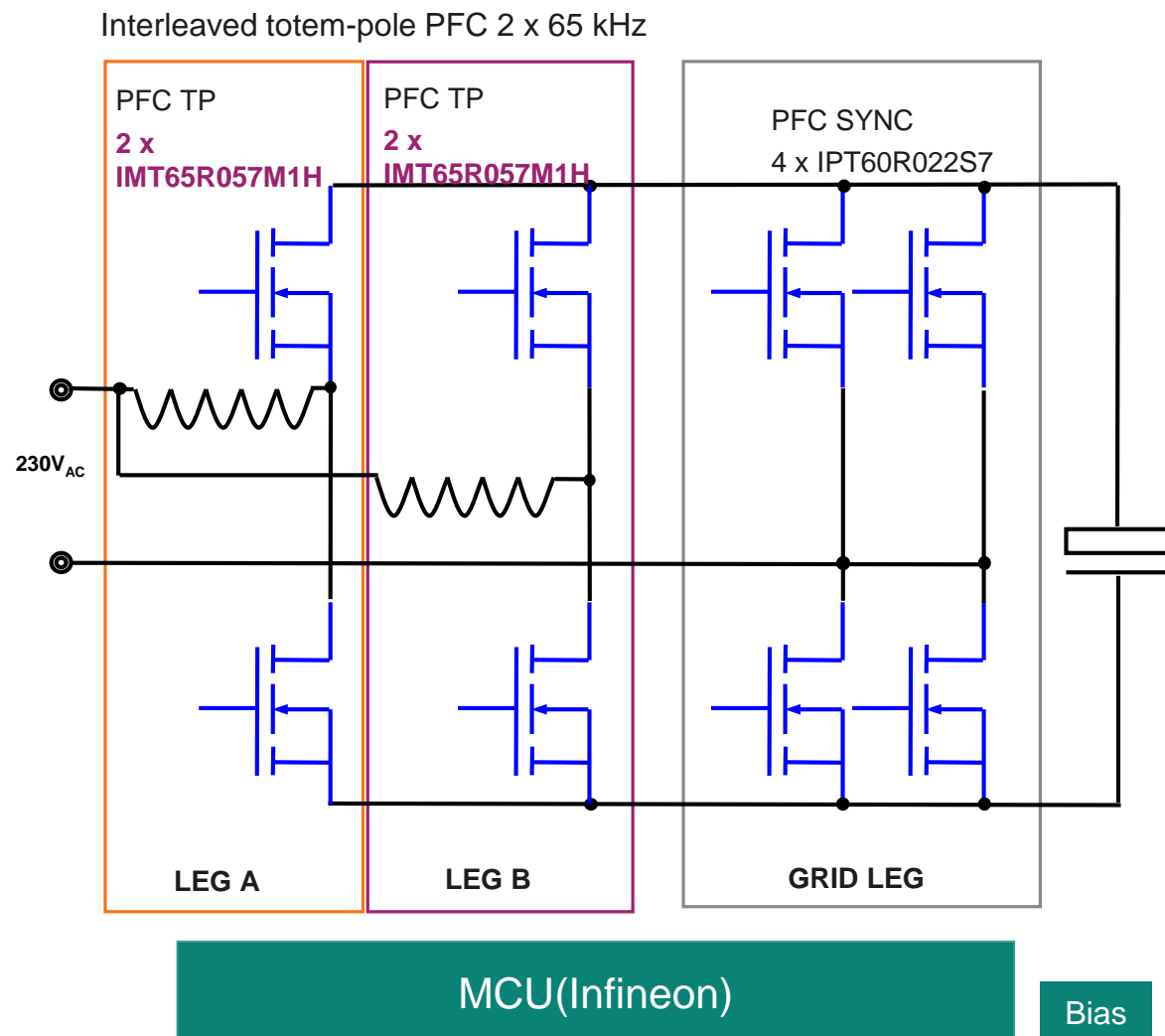


"How to parallel CoolGaN 600V HEMT in half-bridge configurations for higher-power applications"



Interleaved totem-pole

Efficiency of PFC stage stand-alone

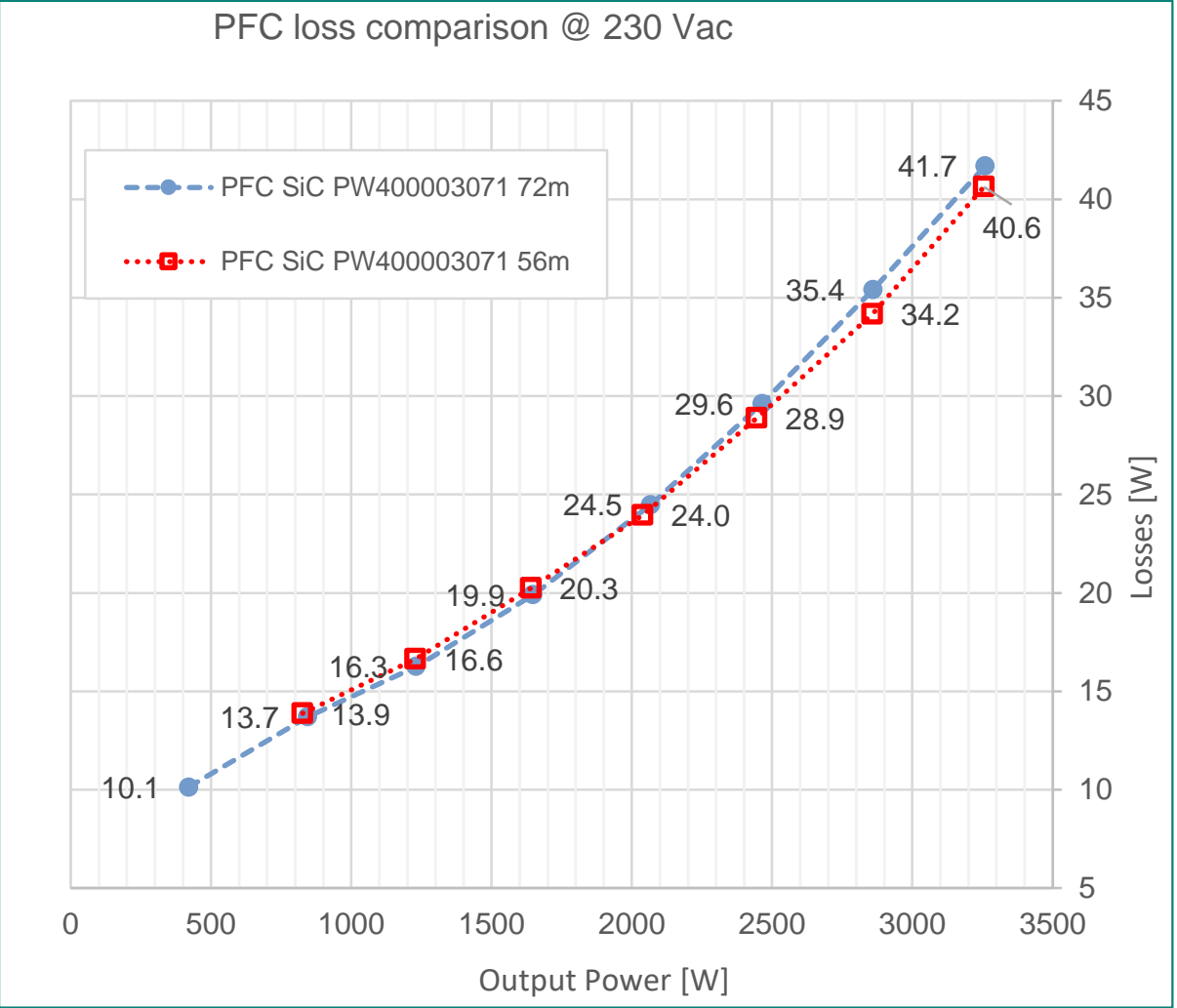
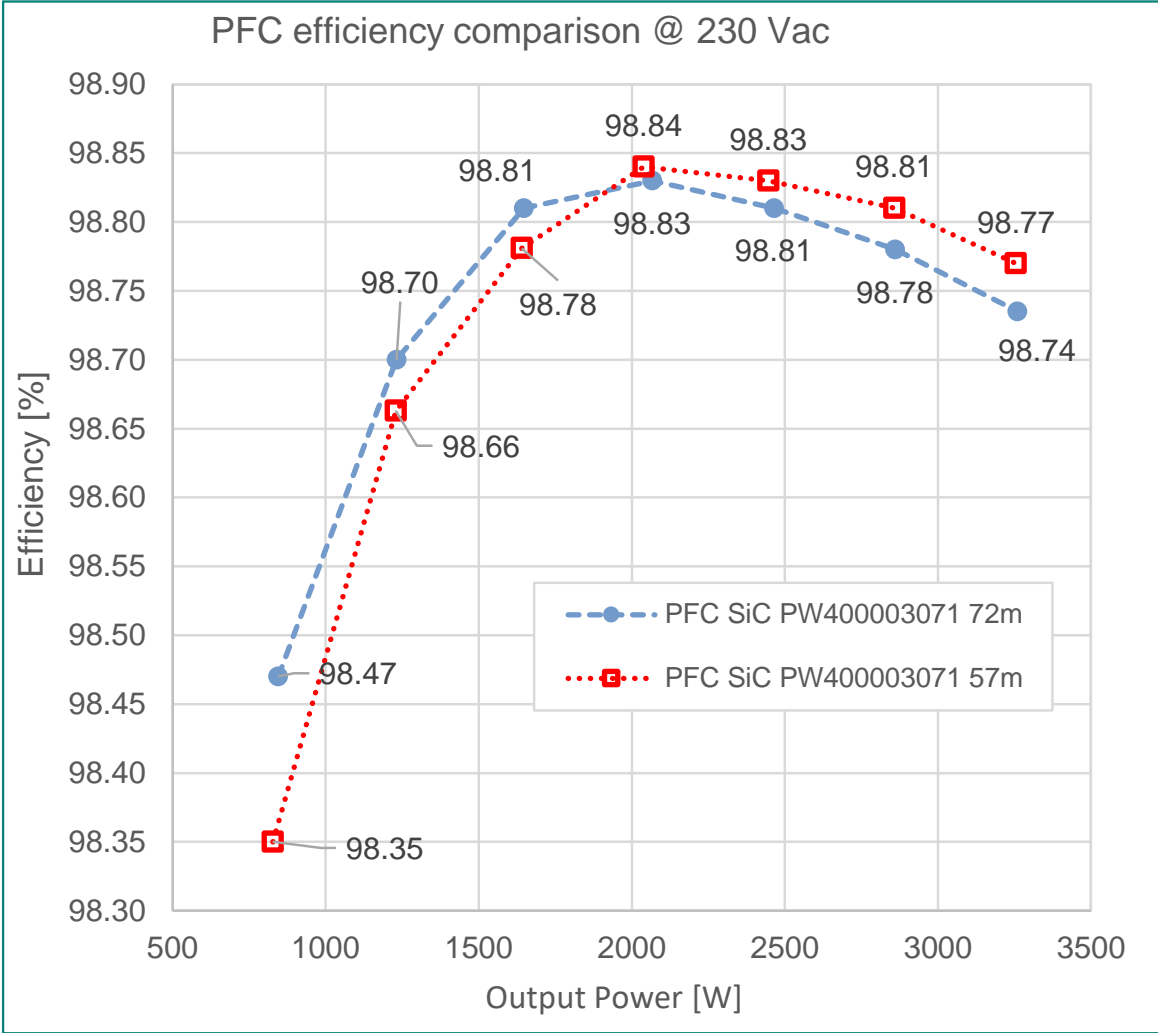


Settings WT3000: 64AVG – line filter: input 500 Hz, output 1 kHz

*Fan supplied externally, no enclosure

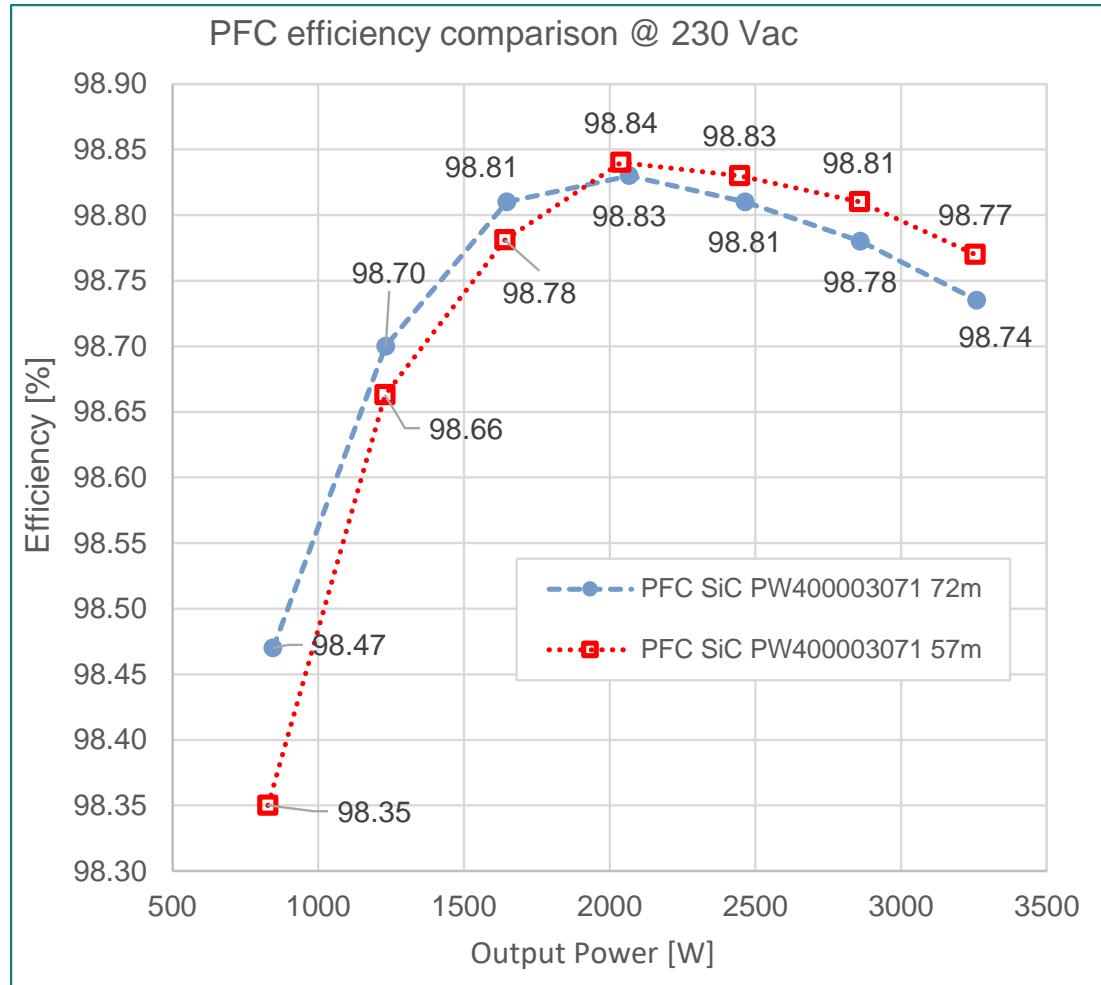
Efficiency PFC stage stand-alone

SiC 72 mΩ vs 57 mΩ $R_{DS(on)}$ (1/2)

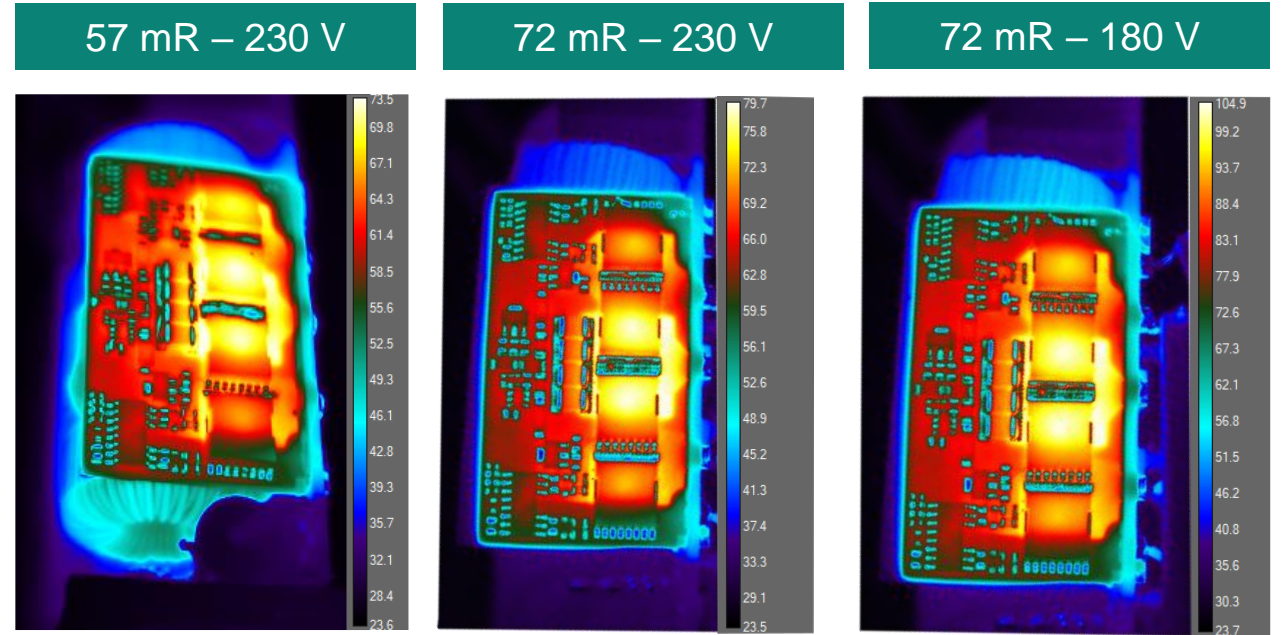


Settings WT3000: 64AVG – line filter: input 500 Hz, output 1 kHz

Efficiency PFC stage stand-alone. SiC 72 mΩ vs 57 mΩ $R_{DS(on)}$ (2/2)



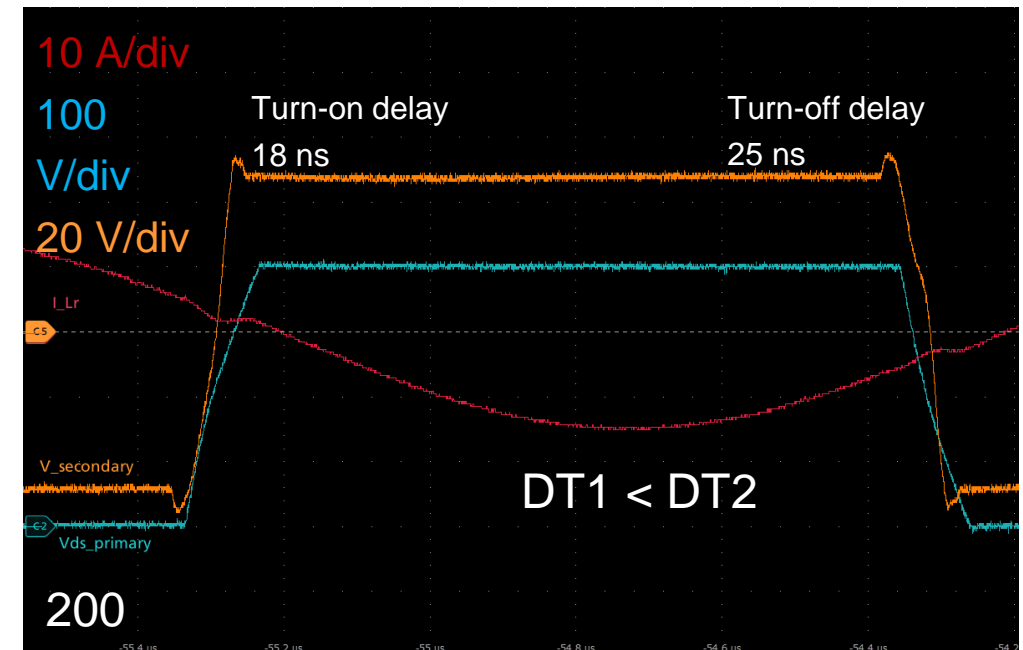
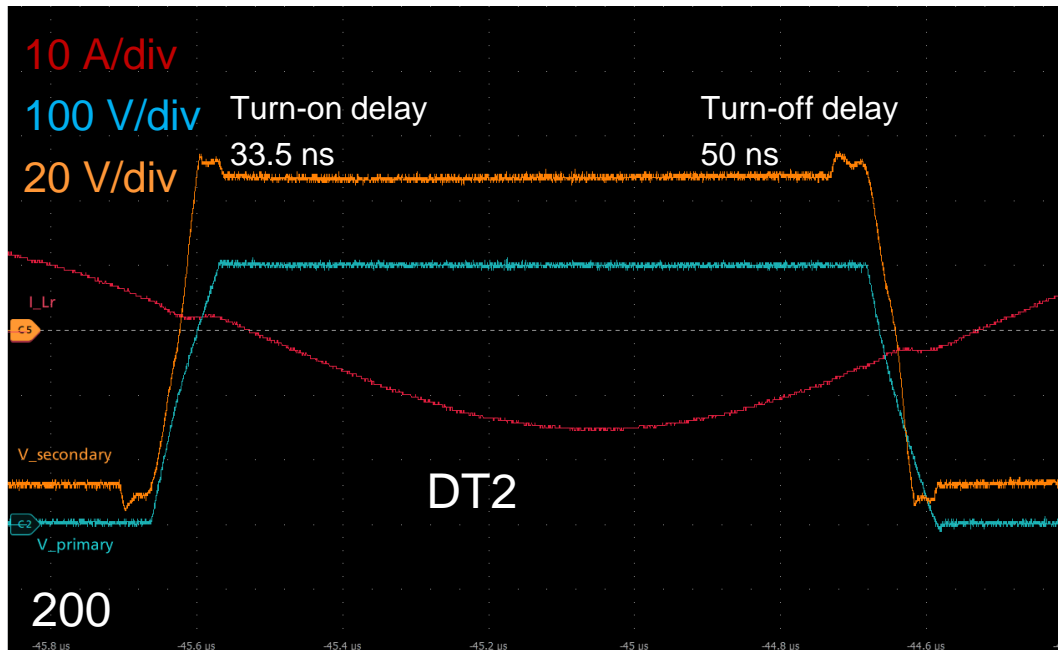
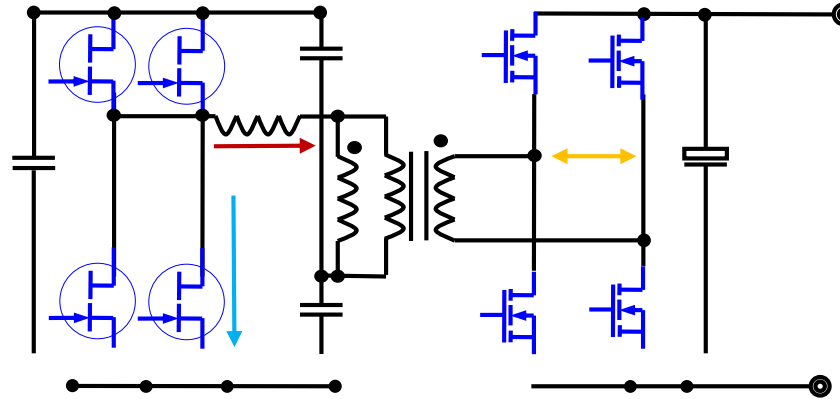
Settings WT3000: 64AVG – line filter: input 500 Hz, output 1 kHz



* Infrared camera measurement at open frame

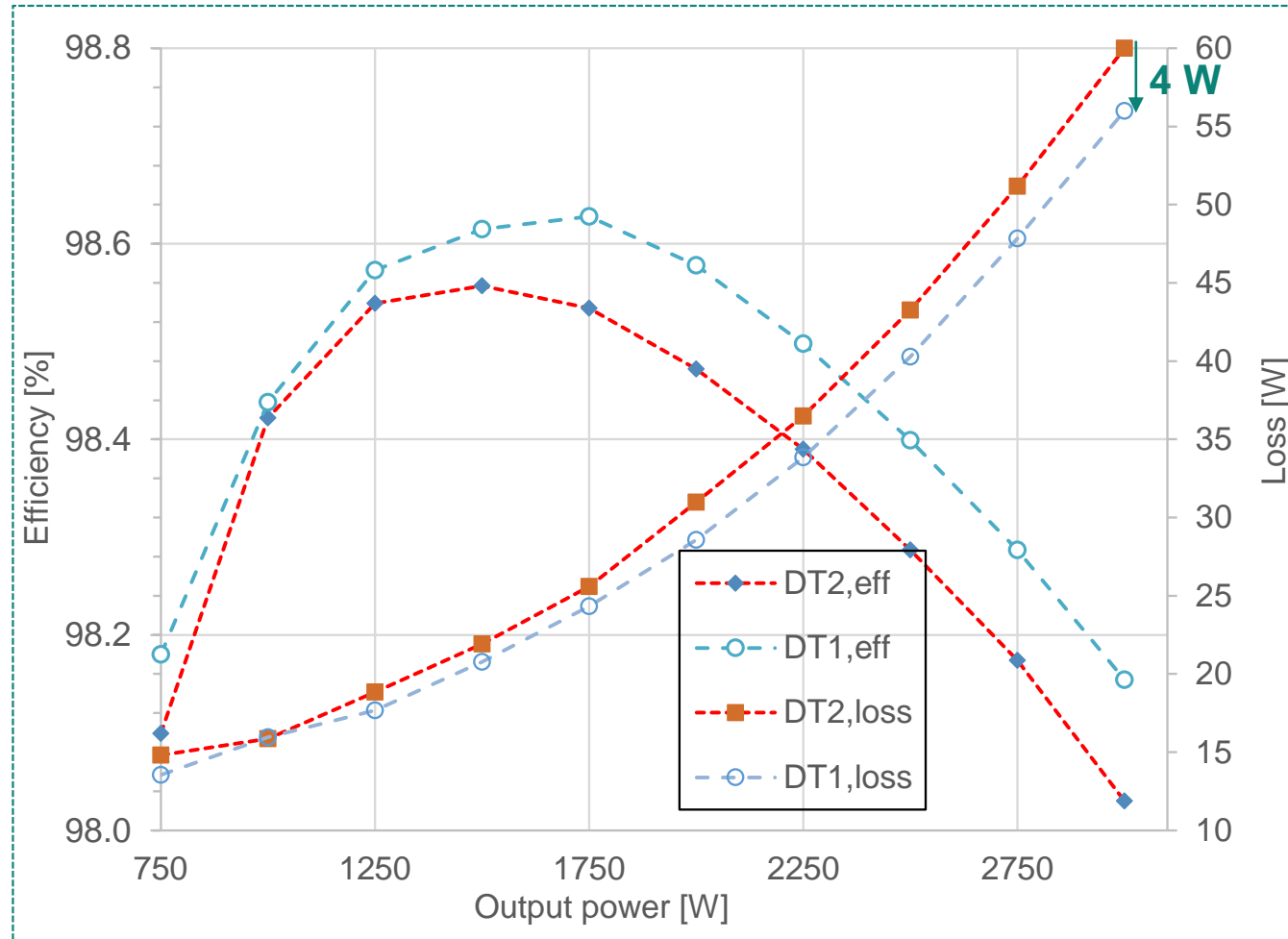
HALF-BRIDGE LLC

Impact of the synchronous rectifiers' body diode conduction time (1/2)

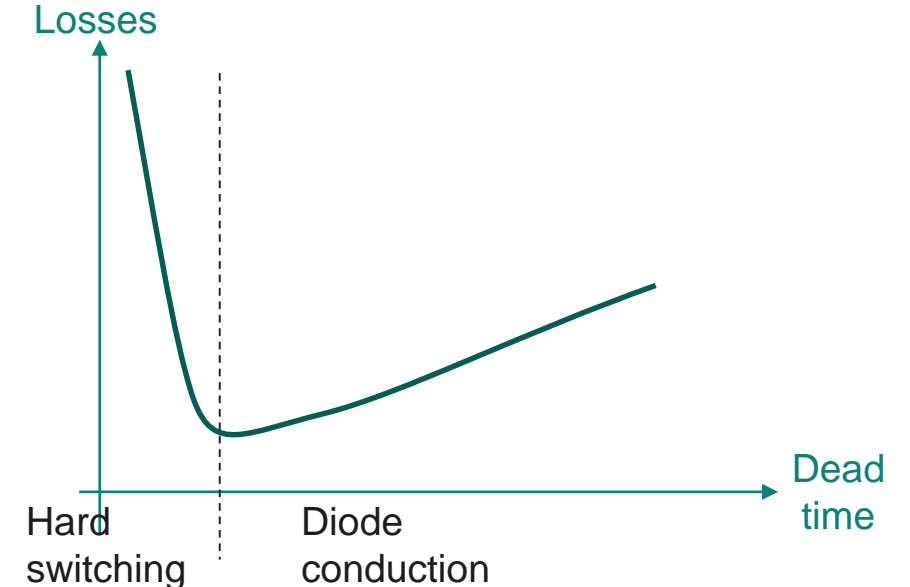


Impact of the synchronous rectifiers' body diode conduction time (2/2)

LLC with $DT1 < DT2$ (DT secondary side dead times)

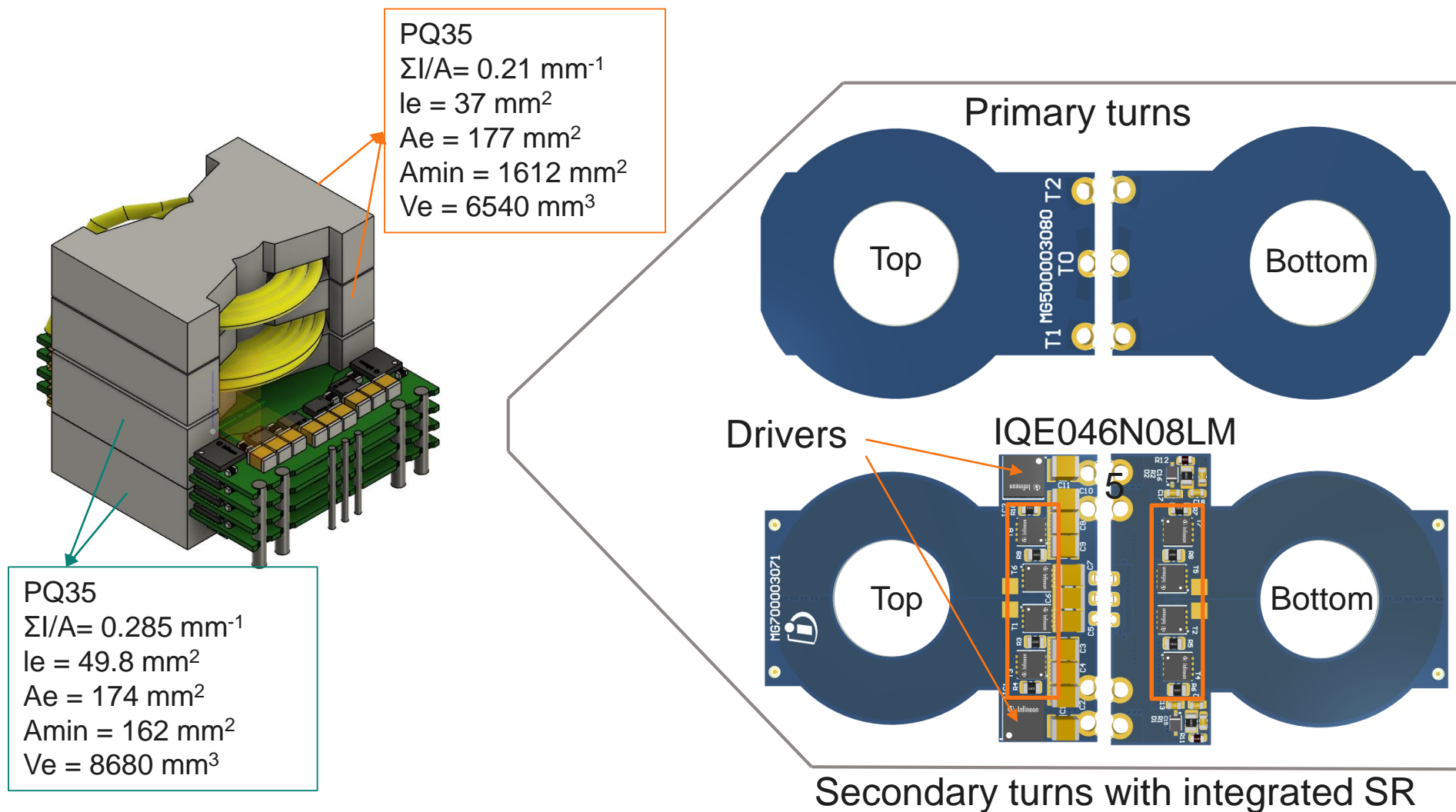


- In high frequency LLC design, dead times play a fundamental role in order to obtain high efficiency
→ **Minimized DT**
- Hard switching needs to be avoided, even if WBG devices would be used and only low voltage is hard switched. With the high frequency the impact is not negligible → **Minimum DT**



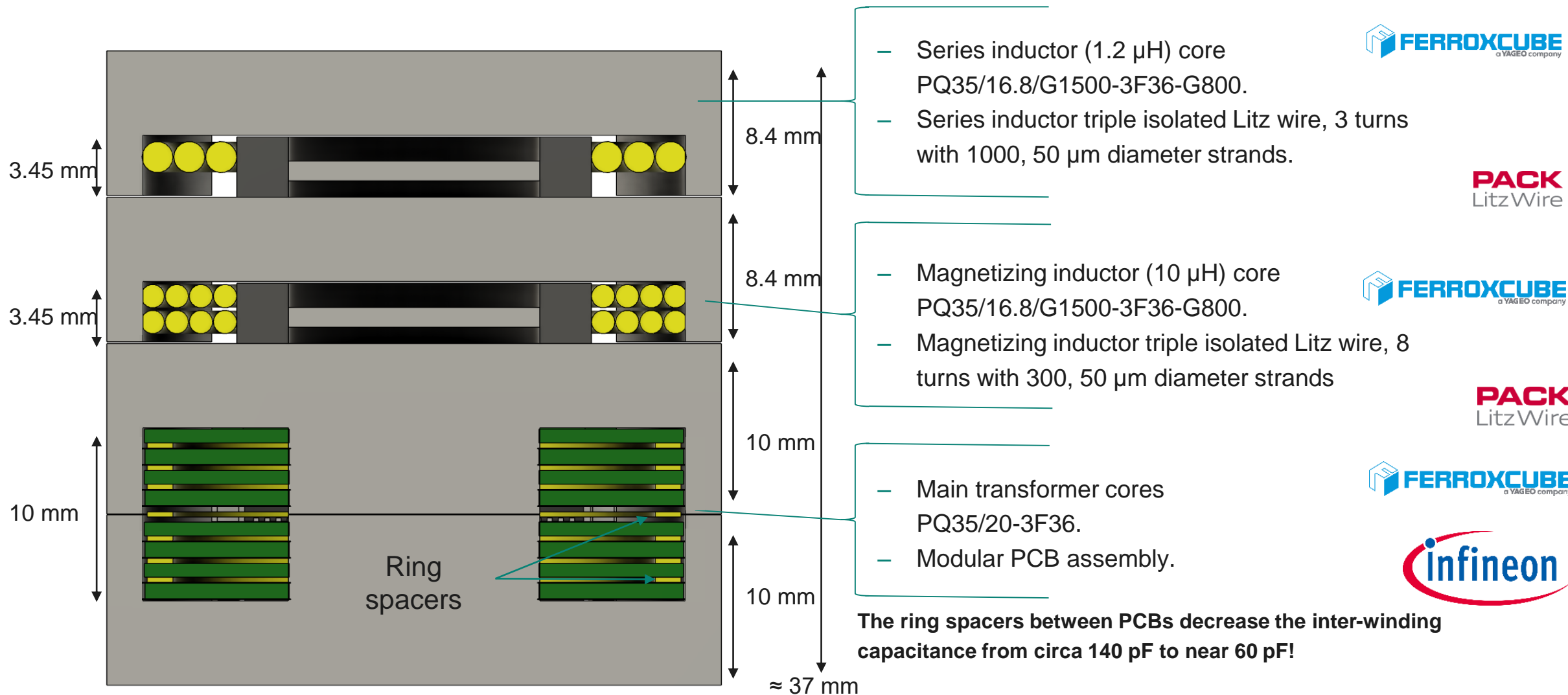
Planar transformer

Transformer assembly stack (1/2)

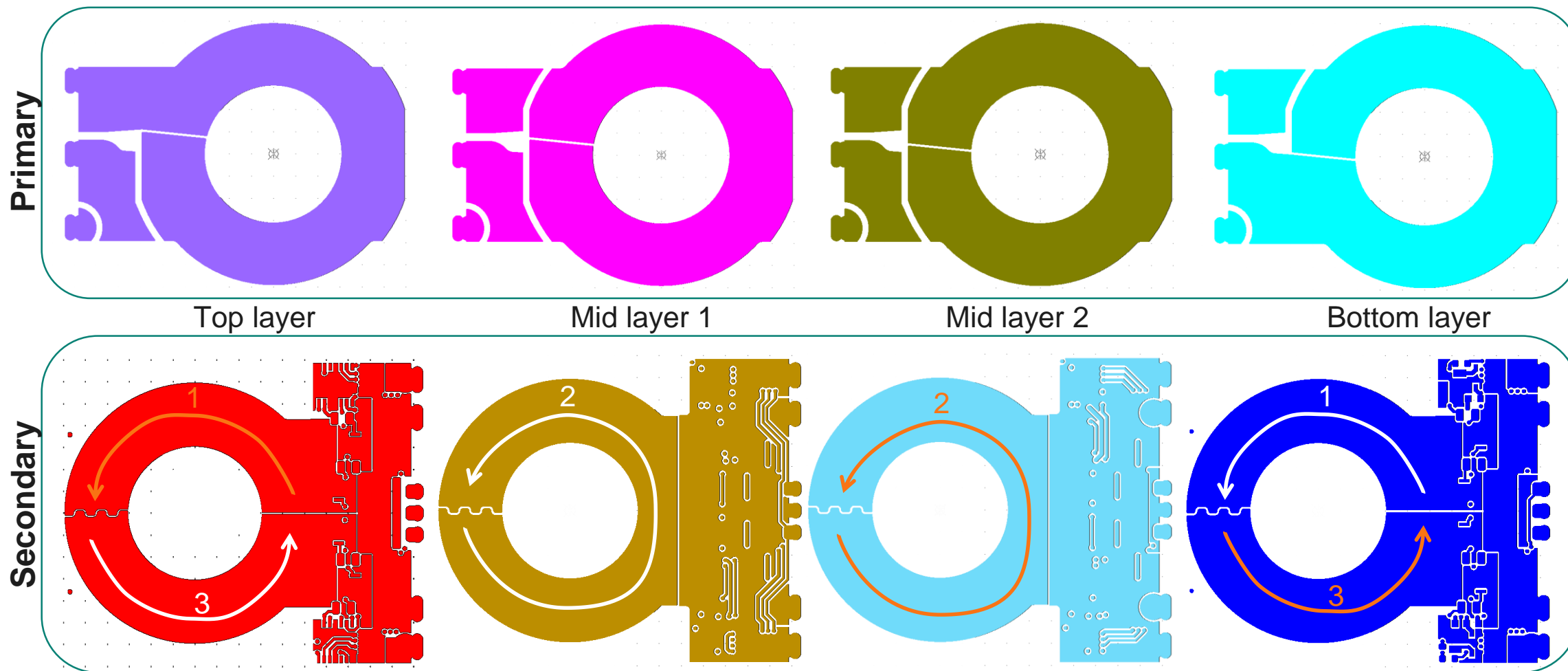


Total estimated volume = $0.055 \text{ dm}^3 = 3.36 \text{ in}^3$
 Estimated power density $\approx 54 \text{ kW/l} \approx 893 \text{ W/in}^3$

Transformer assembly stack (2/2)



Layout of the transformer's PCBs



Secondary-side PCB has exchange of layers from bottom to top to balance the copper usage in a non-sandwiched PCB (Litz wire like exchange of layers).

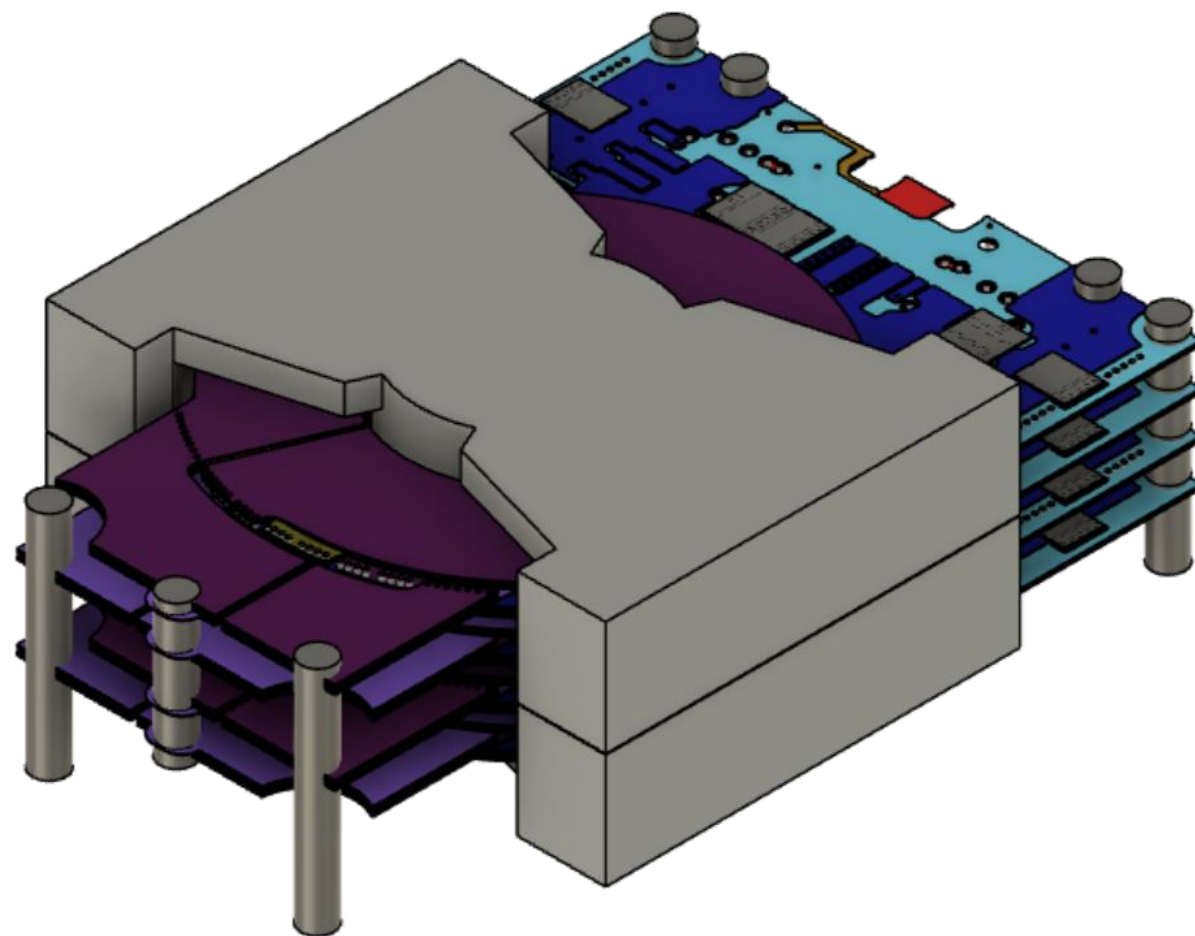
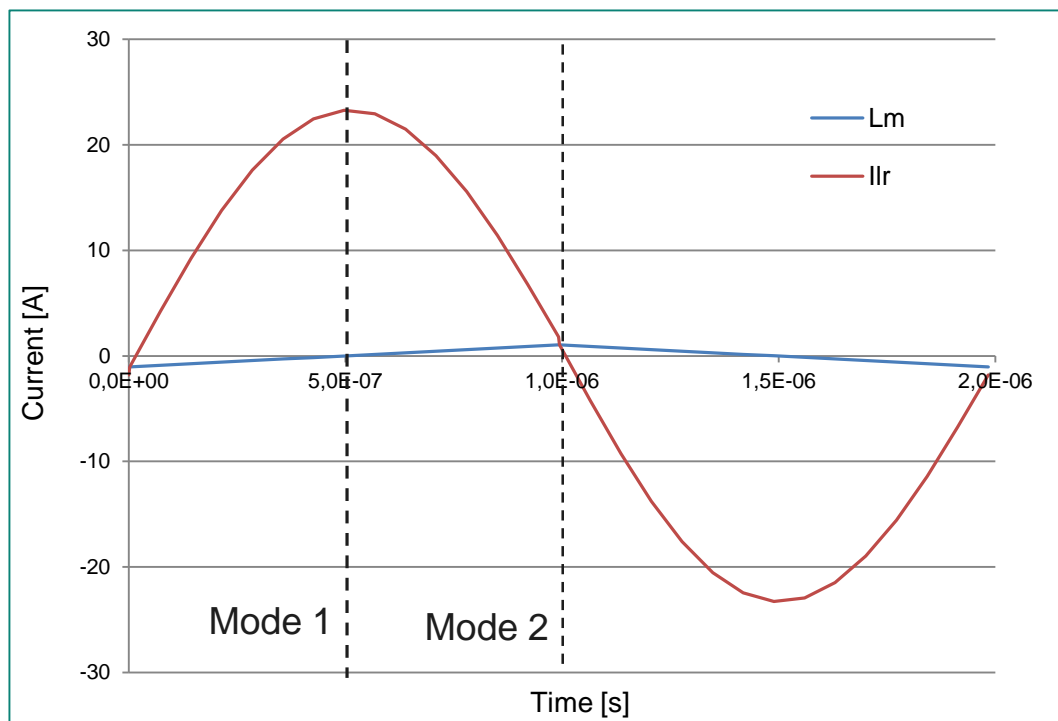
Complete model for FEA (Ansys Electromagnetic) simulation

Starting from top of right hand side figure: P-S-P-S-P-S-P-S

Core 3F36 with B-H curve and 60 μm gap

Simulation conditions:

- 500 KHz
- Primary sinewave 30 A peak (0 A magnetizing)
- Secondary sinewave 120 A peak



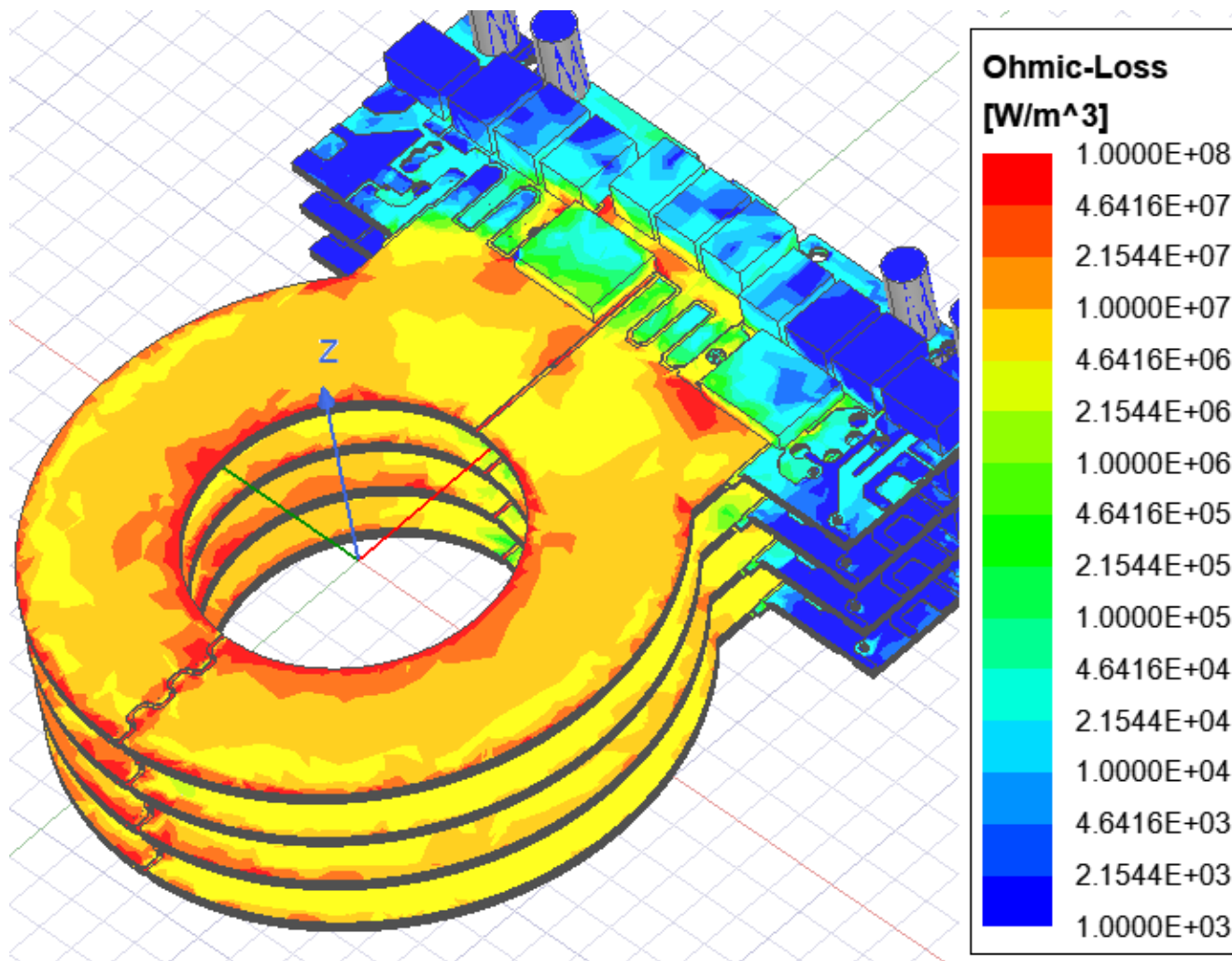
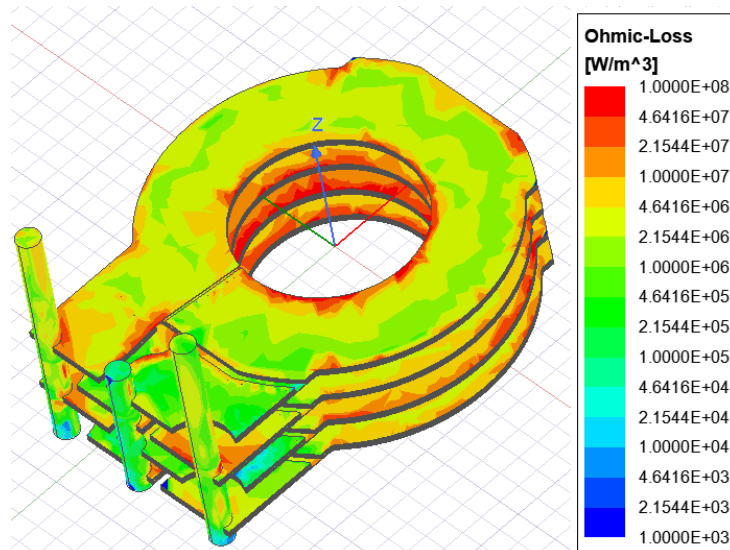
Transformer ohmic loss at full load. 4 PCBs of final layout.

Simulation conditions:

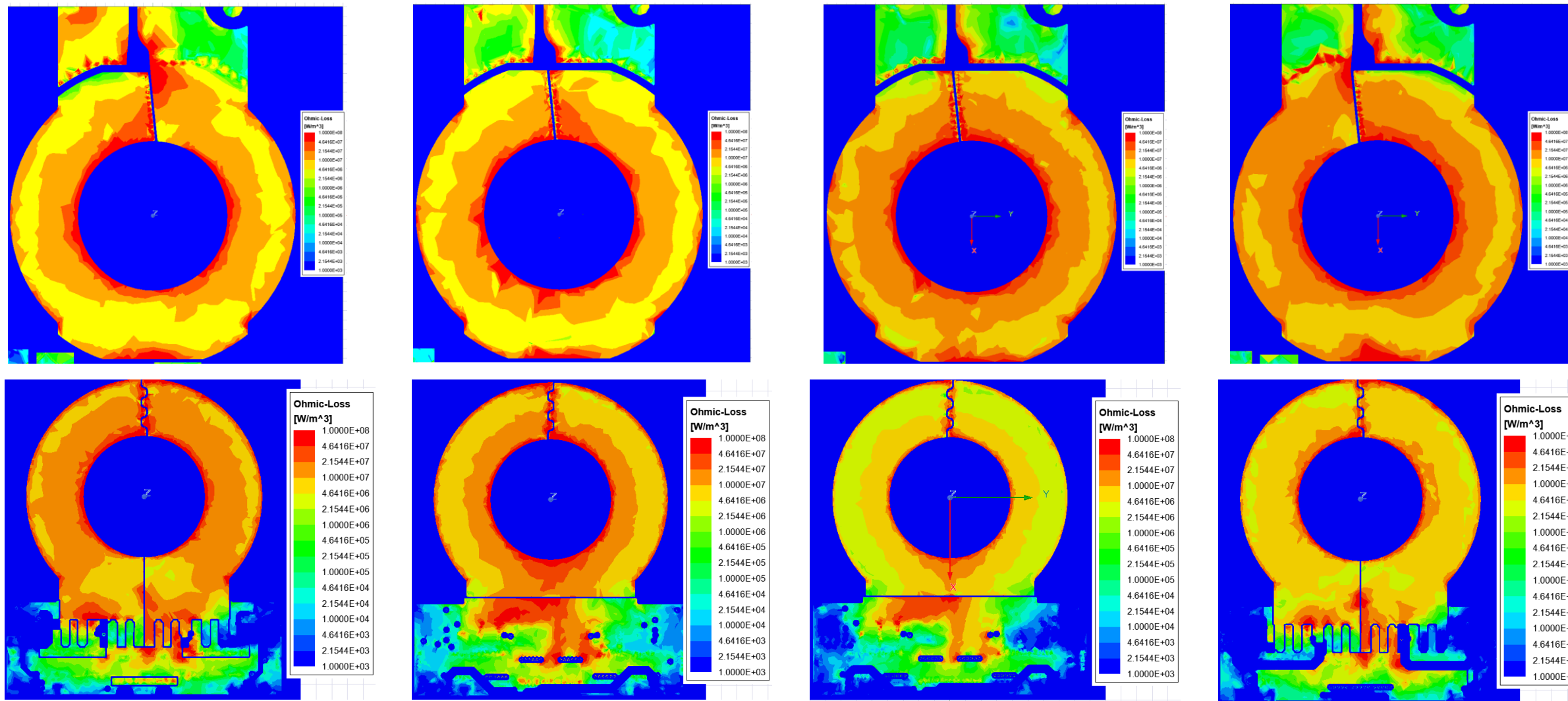
- 500 kHz
- Primary sinewave 30 A peak (Mode 1)
- Secondary sinewave 120 A peak

Results:

- Primary: 6.01 W, 13.36 mΩ
- Secondary: 7.83 W, 1.09 mΩ
- Total: 13.84 W



Transformer ohmic loss at full load



Summary

Summary

Full Infineon system solution for server and telecom applications

- CoolGaN™ + CoolSiC™ + CoolMOS™ + OptiMOS™

High power density and efficiency: 3 kW – 96 W/in³ – η_{peak} =97.5%

- Interleaved PFC (EMI – PFC choke)
- High-freq LLC (transformer + Lm + Lr)
- Hold-up time extension (bulk capacitance)

Modular design

- Power boards: SMD TOLL

Interleaved Totem-pole PFC, $\eta_{\text{peak}} > 98.8\%$

- 57 mΩ CoolSiC™ / 72 mΩ CoolSiC™ with power derating at 180 V

High-frequency LLC ($f_{\text{res}} = 530\text{kHz}$) with CoolGaN™ and OptiMOS™, $\eta_{\text{peak}} > 98.6\%$

- Dead time high impact on performance at high-freq
- SR integrated in transformer PCB
- Planar transformer: FEA for design optimization

