CS250 Lab1 Pi-Feng Chiu

Q1. W=16 vs. W=32 (For Verilog implementation only)

- What changes would you need to make to the gcdGCDUnit rtl module?

Ans: Substitute W=16 with W=32.

- what changes do you need to make in order to test our new 32-bit gcdGCDUnit rtl module? Demonstrate that your 32-bit gcdGCDUnit rtl functions correctly.

Ans: Double the bitwidth of input/output/test patterns

Comarison: Since the register number is nearly doubled, the cell count and area consumption are larger than twice of the 90nm results. In the meantime, more cells would lead to more switching activity and more leakage current, which mean larger power consumption. Timing-wise, the larger critical path length may be due to larger parasitic capacitance after place and route.

Q2. Chisel vs. Verilog

I modified the original swap method of original Verilog and use “if A>B: A:=A-B, if B>A: B:=B-A and operation is done when A==B”, which leads to 4 less cycle for one calculation. The performance would be better regardless of the critical path length. However, the cell count would be enlarged for the operation and would lead to larger area.
The power would also be larger due to more switching nodes and more gates.

Q3. 90nm vs. 32nm

Time: The advanced technology would intrinsically have better performance (as shown in the critical path length in post synthesis result). However, there might be larger parasitic due to wire coupling, which resulting in larger critical path length in post place-and-route result.
Power: The average power in Prime Time result is slightly smaller than

90nm result. It might be due to a lower VDD.
Area: The area is evidently reduced due to smaller feature size.

	Unit	90nm	32bit	32nm	Chisel
Post Syn Crit Path Length	ns	0.81	0.81	0.71	0.82
Post Syn Area	um^2	3380.43	7770.93	800.05	3946.29
Post Syn Power	mW	0.6093	1.69	0.179	1.190
Post PaR Crit Path Length	ns	0.64	0.83	0.84	0.78
Post PaR Area	um^2	4352.90	10256.84	1084.12	5335.92
Post PaR Power	mW	0.996	2.65	0.215	1.67
Avg Power (max)	mW	0.267	0.626	0.228	0.251
Peak Power (max)	mW	190	266	7.3	44.5
Total Cell Count		411	991	228	591
DFF* Cell Count		34	66	34	34