Lab2 writeup Pi-Feng Chiu

Area		RVT	Multi-VT	SRAM
Window Buffer	um^2	23306.02	21283.8	4177.41
Median Sorter	um^2	1858.81	2477.4	2508.66
Total	um^2	25785.2	24229.84	7124.72
Cell Count	SVT	0	198	12
Cell Count	RVT	5884	207	83
Cell Count	HVT	0	5811	1459

Power		RVT	Multi-VT	SRAM
Entire Design				
Leakage	uW	3390	706	191
Total	uW	6940	3120	2200
Window Buffer				
Leakage	uW	3200	567	16.5
Total	uW	5790	2020	943
Median Sorter				
Leakage	uW	115	44.3	20.1
Total	uW	753	766	927

Questions: Multiple VT Flow

1. What impact does switching from a single VT to a multi-VT flow have on area? Does this agree with your expectations?

The Median Sorter area in Multi-VT is slightly larger while Window Buffer area in Multi-VT is smaller, which results to a smaller area in total. I expected the area would be larger in Multi-VT since Multi-VT design would use much more gates to do both leakage control and driving output.

2. What effect does switching to a multi-VT have on the power consumption of your design? How much does it reduce leakage power?

The power consumption is reduced evidently when switching to multi-VT design, since the leakage power in entire design is reduced by 77.58%.

3. Can you think of a reason why you wouldn't want to use multiple VT cells to implement a design?

Although switching to multi-VT contributes to smaller area and tremendous leakage reduction in this design, the process of multiple VT CMOS manufacture is much more complicate than the single VT one, and that leads to increasing cost in production.

4. What portion of the cells used in the multi-VT version of your design are regular or low VT?

The portion of regular VT cells is 3.2% and low VT is 3.33%.

5. Where in your design do they appear and why?

They appear in some output stages to increase driving ability.

Questions: SRAM

1. How much area do you save by using an SRAM instead of registers to implement storage for your window buffer?

Using SRAM instead of registers saves 17106.39 um2 (80.37%) area for window buffer.

2. What is the area of the SRAM macro?

3332.89 um^2

3. Assuming that the individual bitcells have an area of 0.595 um2, what is the efficiency (area used for bitcells over total area) of this SRAM macro?

(0.595*128*16)/3332.89=36.56 %

4. Would you expect this SRAM to use 6T or 8T bitcells, and why?

I would expect this SRAM to use 8T bitcells since this is an one-read AND one-write SRAM, it requires two ports to access to the data and that would be two additional transistors.

5. What are the other components of an SRAM, besides the bitcells?

In an SRAM, there would be peripheral circuits including row/column decoders, passgates, control circuits, and sense amplifiers.

Questions: Power and Performance

1. Assuming a clock frequency of 250 MHz, calculate the amount of energy (in Joules) used to compute a single output pixel and an entire image for all three versions of your design.

Energy=Power * Time; Cycle time=1/250MHz=4ns

RVT:	Energy(single output pixel)=6940uW*4ns=27.76 pJ
	Energy(entire image)=6940uW*4ns*16384=454.82 nJ
Multi-Vt:	Energy(single output pixel)=3120uW*4ns=12.48 pJ
	Energy(entire image)=3120uW*4ns*16384=204.472 nJ
SRAM:	Energy(single output pixel)=2200uW*4ns=8.8 pJ
	Energy(entire image)=2200uW*4ns*16384=147.13 nJ

2. How would pipelining your median sorting module change the timing (critical path) and area of your design? How can pipelining improve performance, and how does it effect latency and throughput? What effect would you expect pipelining to have on energy efficiency?

Pipelining in median sorting module would increase area due to inserted register for every output of pipeline stages. Also, the critical timing would also be increased due to additional delay of the inserted register. However, the performance could be improved by reducing cycle time (higher operating frequency) because the latency would be 1 three element network operating time plus pipeline register delay instead of 3 three element network operating time. Therefore, throughput is increased about three times. I would expect pipelining improves energy efficiency since the function blocks would not be in an idle state and consume leakage current.