Table 9. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TTa	3.3 V tolerant I/O directly connected to ADC
	B	Dedicated BOOT pin
	RST	Bidirectional reset pin with weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
1	1	A2	1	1	A3	E10	1	1	A3	PE2	I/O	FT	-	TRACECLK, SPI4_SCK, SAI1_MCLK_A, QUADSPI_BK1_IO2, ETH_MII_TXD3, FMC_A23, EVENTOUT	-
2	2	A1	2	2	A2	F10	2	2	A2	PE3	I/O	FT	-	TRACED0, SAI1_SD_B, FMC_A19, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
3	3	B1	3	3	A1	C12	3	3	A1	PE4	I/O	FT	-	TRACED1, SPI4_NSS, SAI1_FS_A, DFSDM1_DATIN3, FMC_A20, DCMI_D4, LCD_B0, EVENTOUT	-
4	4	B2	4	4	B1	D12	4	4	B1	PE5	I/O	FT	-	TRACED2, TIM9_CH1, SPI4_MISO, SAI1_SCK_A, DFSDM1_CKIN3, FMC_A21, DCMI_D6, LCD_G0, EVENTOUT	-
5	5	B3	5	5	B2	E11	5	5	B2	PE6	I/O	FT	-	TRACED3, TIM1_BKIN2, TIM9_CH2, SPI4_MOSI, SAI1_SD_A, SAI2_MCLK_B, FMC_A22, DCMI_D7, LCD_G1, EVENTOUT	-
-	-	-	-	-	G6	-	-	-	G6	VSS	S	-	-	-	-
-	-	-	-	-	F5	-	-	-	F5	VDD	S	-	-	-	-
6	6	C1	6	6	C1	C13	6	6	C1	VBAT	S	-	-	-	-
-	-	D2	7	7	C2	NC	7	7	C2	PI8	I/O	FT	(2)	EVENTOUT	RTC_TAMP2/RTC_TS/ WKUP5
7	7	D1	8	8	D1	D13	8	8	D1	PC13	I/O	FT	(2)	EVENTOUT	RTC_TAMP1/RTC_TS/ RTC_OUT/ WKUP4
8	8	E1	9	9	E1	E12	9	9	E1	PC14-OSC32_IN	I/O	FT	(2) (3)	EVENTOUT	OSC32_IN
9	9	F1	10	10	F1	E13	10	10	F1	PC15-OSC32_OUT	I/O	FT	(2) (3)	EVENTOUT	OSC32_OUT
-	-	-	-	-	G5	-	-	-	G5	VDD	S	-	-	-	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	-	D3	11	11	E4	G10	11	11	E4	PI9	I/O	FT	-	UART4_RX, CAN1_RX, FMC_D30, LCD_VSYNC, EVENTOUT	-
-	-	E3	12	12	D5	H10	12	12	D5	PI10	I/O	FT	-	ETH_MII_RX_ER, FMC_D31, LCD_HSYNC, EVENTOUT	-
-	-	E4	13	13	F3	F11	13	13	F3	PI11	I/O	FT	-	LCD_G6, OTG_HS_ULPI_DIR, EVENTOUT	WKUP6
-	-	F2	14	14	F2	F13	14	14	F2	VSS	S	-	-	-	-
-	-	F3	15	15	F4	F12	15	15	F4	VDD	S	-	-	-	-
-	10	E2	16	16	D2	G11	16	16	D2	PF0	I/O	FT	-	I2C2_SDA, FMC_A0, EVENTOUT	-
-	11	H3	17	17	E2	G12	17	17	E2	PF1	I/O	FT	-	I2C2_SCL, FMC_A1, EVENTOUT	-
-	12	H2	18	18	G2	G13	18	18	G2	PF2	I/O	FT	-	I2C2_SMBA, FMC_A2, EVENTOUT	-
-	-	-	-	19	E3	NC	-	19	E3	PI12	I/O	FT	-	LCD_HSYNC, EVENTOUT	-
-	-	-	-	20	G3	NC	-	20	G3	PI13	I/O	FT	-	LCD_VSYNC, EVENTOUT	-
-	-	-	-	21	H3	NC	-	21	H3	PI14	I/O	FT	-	LCD_CLK, EVENTOUT	-
-	13	J2	19	22	H2	H11	19	22	H2	PF3	I/O	FT	-	FMC_A3, EVENTOUT	ADC3_IN9
-	14	J3	20	23	J2	H12	20	23	J2	PF4	I/O	FT	-	FMC_A4, EVENTOUT	ADC3_IN14
-	15	K3	21	24	K3	H13	21	24	K3	PF5	I/O	FT	-	FMC_A5, EVENTOUT	ADC3_IN15
10	16	G2	22	25	H6	J13	22	25	H6	VSS	S	-	-	-	-
11	17	G3	23	26	H5	J12	23	26	H5	VDD	S	-	-	-	-
-	18	K2	24	27	K2	NC	24	27	K2	PF6	I/O	FT	-	TIM10_CH1, SPI5_NSS, SAI1_SD_B, UART7_RX, QUADSPI_BK1_IO3, EVENTOUT	ADC3_IN4

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	19	K1	25	28	K1	NC	25	28	K1	PF7	I/O	FT	-	TIM11_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_TX, QUADSPI_BK1_IO2, EVENTOUT	ADC3_IN5
-	20	L3	26	29	L3	NC	26	29	L3	PF8	I/O	FT	-	SPI5_MISO, SAI1_SCK_B, UART7_RTS, TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT	ADC3_IN6
-	21	L2	27	30	L2	NC	27	30	L2	PF9	I/O	FT	-	SPI5_MOSI, SAI1_FS_B, UART7_CTS, TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT	ADC3_IN7
-	22	L1	28	31	L1	K11	28	31	L1	PF10	I/O	FT	-	QUADSPI_CLK, DCMI_D11, LCD_DE, EVENTOUT	ADC3_IN8
12	23	G1	29	32	G1	K12	29	32	G1	PH0-OSC_IN	I/O	FT	(3)	EVENTOUT	OSC_IN
13	24	H1	30	33	H1	K13	30	33	H1	PH1-OSC_OUT	I/O	FT	(3)	EVENTOUT	OSC_OUT
14	25	J1	31	34	J1	L11	31	34	J1	NRST	I/O	RST	-	-	-
15	26	M2	32	35	M2	L12	32	35	M2	PC0	I/O	FT	-	DFSDM1_CKIN0, DFSDM1_DATIN4, SAI2_FS_B, OTG_HS_ULPI_STP, FMC_SDNWE, LCD_R5, EVENTOUT	ADC1_IN10, ADC2_IN10, ADC3_IN10
16	27	M3	33	36	M3	L13	33	36	M3	PC1	I/O	FT	-	TRACED0, DFSDM1_DATIN0, SPI2_MOSI/I2S2_SD, SAI1_SD_A, DFSDM1_CKIN4, ETH_MDC, MDIOS_MDC, EVENTOUT	ADC1_IN11, ADC2_IN11, ADC3_IN11, RTC_TAMP3/WKUP3

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
17	28	M4	34	37	M4	NC	34	37	M4	PC2	I/O	FT	-	DFSDM1_CKIN1, SPI2_MISO, DFSDM1_CKOUT, OTG_HS_ULPI_DIR, ETH_MII_TXD2, FMC_SDNE0, EVENTOUT	ADC1_IN12, ADC2_IN12, ADC3_IN12
18	29	M5	35	38	L4	NC	35	38	L4	PC3	I/O	FT	-	DFSDM1_DATIN1, SPI2_MOSI/I2S2_SD, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, FMC_SDCKE0, EVENTOUT	ADC1_IN13, ADC2_IN13, ADC3_IN13
-	30	-	36	39	J5	-	36	39	J5	VDD	S	-	-	-	-
-	-	-	-	-	J6	-	-	-	J6	VSS	S	-	-	-	-
19	31	M1	37	40	M1	M11	37	40	M1	VSSA	S	-	-	-	-
-	-	N1	-	-	N1	-	-	-	N1	VREF-	S	-	-	-	-
20	32	P1	38	41	P1	-	38	41	P1	VREF+	S	-	-	-	-
21	33	R1	39	42	R1	M12	39	42	R1	VDDA	S	-	-	-	-
22	34	N3	40	43	N3	M13	40	43	N3	PA0-WKUP	I/O	FT	(4)	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, SAI2_SD_B, ETH_MII_CRS, EVENTOUT	ADC1_IN0, ADC2_IN0, ADC3_IN0, WKUP1
23	35	N2	41	44	N2	J11	41	44	N2	PA1	I/O	FT	-	TIM2_CH2, TIM5_CH2, USART2_RTS, UART4_RX, QUADSPI_BK1_IO3, SAI2_MCLK_B, ETH_MII_RX_CLK/ETH_RMII_REF_CLK, LCD_R2, EVENTOUT	ADC1_IN1, ADC2_IN1, ADC3_IN1

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
24	36	P2	42	45	P2	J10	42	45	P2	PA2	I/O	FT	-	TIM2_CH3, TIM5_CH3, TIM9_CH1, USART2_TX, SAI2_SCK_B, ETH_MDIO, MDIOS_MDIO, LCD_R1, EVENTOUT	ADC1_IN2, ADC2_IN2, ADC3_IN2, WKUP2
-	-	F4	43	46	K4	L10	43	46	K4	PH2	I/O	FT	-	LPTIM1_IN2, QUADSPI_BK2_IO0, SAI2_SCK_B, ETH_MII_CRS, FMC_SDCKE0, LCD_R0, EVENTOUT	-
-	-	G4	44	47	J4	K10	44	47	J4	PH3	I/O	FT	-	QUADSPI_BK2_IO1, SAI2_MCLK_B, ETH_MII_COL, FMC_SDNE0, LCD_R1, EVENTOUT	-
-	-	H4	45	48	H4	N12	45	48	H4	PH4	I/O	FT	-	I2C2_SCL, LCD_G5, OTG_HS_ULPI_NXT, LCD_G4, EVENTOUT	-
-	-	J4	46	49	J3	N11	46	49	J3	PH5	I/O	FT	-	I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT	-
25	37	R2	47	50	R2	M10	47	50	R2	PA3	I/O	FT	-	TIM2_CH4, TIM5_CH4, TIM9_CH2, USART2_RX, LCD_B2, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT	ADC1_IN3, ADC2_IN3, ADC3_IN3
26	38	-	-	51	K6	J9	-	51	K6	VSS	S	-	-	-	-
-	-	L4	48	-	L5	-[5]	48	-	L5	BYPASS_REG	I	FT	-	-	-
27	39	K4	49	52	K5	K9	49	52	K5	VDD	S	-	-	-	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
28	40	N4	50	53	N4	L9	50	53	N4	PA4	I/O	TT a	-	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, SPI6_NSS, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC1_IN4, ADC2_IN4, DAC_OUT1
29	41	P4	51	54	P4	P11	51	54	P4	PA5	I/O	TT a	-	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, SPI6_SCK, OTG_HS_ULPI_CK, LCD_R4, EVENTOUT	ADC1_IN5, ADC2_IN5, DAC_OUT2
30	42	P3	52	55	P3	N10	52	55	P3	PA6	I/O	FT	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, SPI6_MISO, TIM13_CH1, MDIOS_MDC, DCMI_PIXCLK, LCD_G2, EVENTOUT	ADC1_IN6, ADC2_IN6
31	43	R3	53	56	R3	M9	53	56	R3	PA7	I/O	FT	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SD, SPI6_MOSI, TIM14_CH1, ETH_MII_RX_DV/ETH_RMII_CRS_DV, FMC_SDNWE, EVENTOUT	ADC1_IN7, ADC2_IN7
32	44	N5	54	57	N5	NC	54	57	N5	PC4	I/O	FT	-	DFSDM1_CKIN2, I2S1_MCK, SPDIF_RX2, ETH_MII_RXD0/ETH_RMII_RXD0, FMC_SDNE0, EVENTOUT	ADC1_IN14, ADC2_IN14
33	45	P5	55	58	P5	NC	55	58	P5	PC5	I/O	FT	-	DFSDM1_DATIN2, SPDIF_RX3, ETH_MII_RXD1/ETH_RMII_RXD1, FMC_SDCKE0, EVENTOUT	ADC1_IN15, ADC2_IN15
-	-	-	-	59	L7	-	-	59	L7	VDD	S	-	-	-	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	-	-	-	60	L6	-	-	60	L6	VSS	S	-	-	-	-
34	46	R5	56	61	R5	P10	56	61	R5	PB0	I/O	FT	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, DFSDM1_CKOUT, UART4_CTS, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, LCD_G1, EVENTOUT	ADC1_IN8, ADC2_IN8
35	47	R4	57	62	R4	J8	57	62	R4	PB1	I/O	FT	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM1_DATIN1, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, LCD_G0, EVENTOUT	ADC1_IN9, ADC2_IN9
36	48	M6	58	63	M5	J7	58	63	M5	PB2	I/O	FT	-	SAI1_SD_A, SPI3_MOSI/I2S3_SD, QUADSPI_CLK, DFSDM1_CKIN1, EVENTOUT	-
-	-	-	-	64	G4	NC	-	64	G4	PI15	I/O	FT	-	LCD_G2, LCD_R0, EVENTOUT	-
-	-	-	-	65	R6	NC	-	65	R6	PJ0	I/O	FT	-	LCD_R7, LCD_R1, EVENTOUT	-
-	-	-	-	66	R7	NC	-	66	R7	PJ1	I/O	FT	-	LCD_R2, EVENTOUT	-
-	-	-	-	67	P7	NC	-	67	P7	PJ2	I/O	FT	-	DSI_TE, LCD_R3, EVENTOUT	-
-	-	-	-	68	N8	NC	-	68	N8	PJ3	I/O	FT	-	LCD_R4, EVENTOUT	-
-	-	-	-	69	M9	NC	-	69	M9	PJ4	I/O	FT	-	LCD_R5, EVENTOUT	-
-	49	R6	59	70	P8	N9	59	70	P8	PF11	I/O	FT	-	SPI5_MOSI, SAI2_SD_B, FMC_SDNRAS, DCMI_D12, EVENTOUT	-
-	50	P6	60	71	M6	K7	60	71	M6	PF12	I/O	FT	-	FMC_A6, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	51	M8	61	72	K7	P9	61	72	K7	VSS	S		-	-	-
-	52	N8	62	73	L8	M8	62	73	L8	VDD	S		-	-	-
-	53	N6	63	74	N6	L8	63	74	N6	PF13	I/O	FT	-	I2C4_SMBA, DFSDM1_DATIN6, FMC_A7, EVENTOUT	-
-	54	R7	64	75	P6	K8	64	75	P6	PF14	I/O	FT	-	I2C4_SCL, DFSDM1_CKIN6, FMC_A8, EVENTOUT	-
-	55	P7	65	76	M8	P8	65	76	M8	PF15	I/O	FT	-	I2C4_SDA, FMC_A9, EVENTOUT	-
-	56	N7	66	77	N7	N8	66	77	N7	PG0	I/O	FT	-	FMC_A10, EVENTOUT	-
-	57	M7	67	78	M7	L7	67	78	M7	PG1	I/O	FT	-	FMC_A11, EVENTOUT	-
37	58	R8	68	79	R8	M7	68	79	R8	PE7	I/O	FT	-	TIM1_ETR, DFSDM1_DATIN2, UART7_RX, QUADSPI_BK2_IO0, FMC_D4, EVENTOUT	-
38	59	P8	69	80	N9	N7	69	80	N9	PE8	I/O	FT	-	TIM1_CH1N, DFSDM1_CKIN2, UART7_TX, QUADSPI_BK2_IO1, FMC_D5, EVENTOUT	-
39	60	P9	70	81	P9	P7	70	81	P9	PE9	I/O	FT	-	TIM1_CH1, DFSDM1_CKOUT, UART7_RTS, QUADSPI_BK2_IO2, FMC_D6, EVENTOUT	-
-	61	M9	71	82	K8	-	71	82	K8	VSS	S	-	-	-	-
-	62	N9	72	83	L9	-	72	83	L9	VDD	S	-	-	-	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
40	63	R9	73	84	R9	J6	73	84	R9	PE10	I/O	FT	-	TIM1_CH2N, DFSDM1_DATIN4, UART7_CTS, QUADSPI_BK2_IO3, FMC_D7, EVENTOUT	-
41	64	P10	74	85	P10	K6	74	85	P10	PE11	I/O	FT	-	TIM1_CH2, SPI4_NSS, DFSDM1_CKIN4, SAI2_SD_B, FMC_D8, LCD_G3, EVENTOUT	-
42	65	R10	75	86	R10	L6	75	86	R10	PE12	I/O	FT	-	TIM1_CH3N, SPI4_SCK, DFSDM1_DATIN5, SAI2_SCK_B, FMC_D9, LCD_B4, EVENTOUT	-
43	66	N11	76	87	R12	P6	76	87	R12	PE13	I/O	FT	-	TIM1_CH3, SPI4_MISO, DFSDM1_CKIN5, SAI2_FS_B, FMC_D10, LCD_DE, EVENTOUT	-
44	67	P11	77	88	P11	N6	77	88	P11	PE14	I/O	FT	-	TIM1_CH4, SPI4_MOSI, SAI2_MCLK_B, FMC_D11, LCD_CLK, EVENTOUT	-
45	68	R11	78	89	R11	M6	78	89	R11	PE15	I/O	FT	-	TIM1_BKIN, FMC_D12, LCD_R7, EVENTOUT	-
46	69	R12	79	90	P12	K5	79	90	P12	PB10	I/O	FT	-	TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, DFSDM1_DATIN7, USART3_TX, QUADSPI_BK1_NCS, OTG_HS_ULPI_D3, ETH_MII_RX_ER, LCD_G4, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
47	70	R13	80	91	R13	L5	80	91	R13	PB11	I/O	FT	-	TIM2_CH4, I2C2_SDA, DFSDM1_CKIN7, USART3_RX, OTG_HS_ULPI_D4, ETH_MII_TX_EN/ETH_RMII_TX_EN, DSI_TE, LCD_G5, EVENTOUT	-
48	71	M10	81	92	L11	P5	81	92	L11	VCAP_1	S	-	-	-	-
49	-	-	-	93	K9	N5	-	93	K9	VSS	S	-	-	-	-
50	72	N10	82	94	L10	P4	82	94	L10	VDD	S	-	-	-	-
-	-	-	-	95	M14	NC	-	95	M14	PJ5	I/O	FT	-	LCD_R6, EVENTOUT	-
-	-	M11	83	96	P13	NC	83	96	P13	PH6	I/O	FT	-	I2C2_SMBA, SPI5_SCK, TIM12_CH1, ETH_MII_RXD2, FMC_SDNE1, DCMI_D8, EVENTOUT	-
-	-	N12	84	97	N13	NC	84	97	N13	PH7	I/O	FT	-	I2C3_SCL, SPI5_MISO, ETH_MII_RXD3, FMC_SDCKE1, DCMI_D9, EVENTOUT	-
-	-	M12	85	98	P14	M5	-	98	P14	PH8	I/O	FT	-	I2C3_SDA, FMC_D16, DCMI_HSYNC, LCD_R2, EVENTOUT	-
-	-	M13	86	99	N14	K4	-	99	N14	PH9	I/O	FT	-	I2C3_SMBA, TIM12_CH2, FMC_D17, DCMI_D0, LCD_R3, EVENTOUT	-
-	-	L13	87	100	P15	L4	-	100	P15	PH10	I/O	FT	-	TIM5_CH1, I2C4_SMBA, FMC_D18, DCMI_D1, LCD_R4, EVENTOUT	-
-	-	L12	88	101	N15	M4	-	101	N15	PH11	I/O	FT	-	TIM5_CH2, I2C4_SCL, FMC_D19, DCMI_D2, LCD_R5, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	-	K12	89	102	M15	P3	-	102	M15	PH12	I/O	FT	-	TIM5_CH3, I2C4_SDA, FMC_D20, DCMI_D3, LCD_R6, EVENTOUT	-
-	-	H12	90	-	K10	N4	-	-	K10	VSS	S		-	-	-
-	-	J12	91	103	K11	-	-	103	K11	VDD	S		-	-	-
51	73	P12	92	104	L13	H8	85	104	L13	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, DFSDM1_DATIN1, USART3_CK, UART5_RX, CAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ETH_RMII_TXD0, OTG_HS_ID, EVENTOUT	-
52	74	P13	93	105	K14	J5	86	105	K14	PB13	I/O	FT	-	TIM1_CH1N, SPI2_SCK/I2S2_CK, DFSDM1_CKIN1, USART3_CTS, UART5_TX, CAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_RMII_TXD1, EVENTOUT	OTG_HS_VBUS
53	75	R14	94	106	R14	N3	87	106	R14	PB14	I/O	FT	-	TIM1_CH2N, TIM8_CH2N, USART1_TX, SPI2_MISO, DFSDM1_DATIN2, USART3_RTS, UART4_RTS, TIM12_CH1, SDMMC2_D0, OTG_HS_DM, EVENTOUT	-
54	76	R15	95	107	R15	N2	88	107	R15	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, USART1_RX, SPI2_MOSI/I2S2_SD, DFSDM1_CKIN2, UART4_CTS, TIM12_CH2, SDMMC2_D1, OTG_HS_DP, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
55	77	P15	96	108	L15	M3	89	108	L15	PD8	I/O	FT	-	DFSDM1_CKIN3, USART3_TX, SPDIF_RX1, FMC_D13, EVENTOUT	-
56	78	P14	97	109	L14	L3	90	109	L14	PD9	I/O	FT	-	DFSDM1_DATIN3, USART3_RX, FMC_D14, EVENTOUT	-
57	79	N15	98	110	K15	M2	91	110	K15	PD10	I/O	FT	-	DFSDM1_CKOUT, USART3_CK, FMC_D15, LCD_B3, EVENTOUT	-
58	80	N14	99	111	N10	K3	92	111	N10	PD11	I/O	FT	-	I2C4_SMBA, USART3_CTS, QUADSPI_BK1_IO0, SAI2_SD_A, FMC_A16/FMC_CLE, EVENTOUT	-
59	81	N13	100	112	M10	J4	93	112	M10	PD12	I/O	FT	-	TIM4_CH1, LPTIM1_IN1, I2C4_SCL, USART3_RTS, QUADSPI_BK1_IO1, SAI2_FS_A, FMC_A17/FMC_ALE, EVENTOUT	-
60	82	M15	101	113	M11	L2	94	113	M11	PD13	I/O	FT	-	TIM4_CH2, LPTIM1_OUT, I2C4_SDA, QUADSPI_BK1_IO3, SAI2_SCK_A, FMC_A18, EVENTOUT	-
-	83	-	102	114	J10	M1	95	114	J10	VSS	S		-	-	-
-	84	J13	103	115	J11	-	96	115	J11	VDD	S		-	-	-
61	85	M14	104	116	L12	L1	97	116	L12	PD14	I/O	FT	-	TIM4_CH3, UART8_CTS, FMC_D0, EVENTOUT	-
62	86	L14	105	117	K13	K2	98	117	K13	PD15	I/O	FT	-	TIM4_CH4, UART8_RTS, FMC_D1, EVENTOUT	-
-	-	-	-	118	K12	-	-	-	-	PJ6	I/O	FT	-	LCD_R7, EVENTOUT	-
-	-	-	-	119	J12	-	-	-	-	PJ7	I/O	FT	-	LCD_G0, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	-	-	-	120	H12	-	-	-	-	PJ8	I/O	FT	-	LCD_G1, EVENTOUT	-
-	-	-	-	121	J13	-	-	-	-	PJ9	I/O	FT	-	LCD_G2, EVENTOUT	-
-	-	-	-	122	H13	-	-	-	-	PJ10	I/O	FT	-	LCD_G3, EVENTOUT	-
-	-	-	-	123	G12	-	-	-	-	PJ11	I/O	FT	-	LCD_G4, EVENTOUT	-
-	-	-	-	124	H11	-	-	-	-	VDD	S	-	-	-	-
-	-	-	-	-	-	K1	99	118	H11	VDDDSI	S	-	-	-	-
-	-	-	-	125	H10	-	-	-	H10	VSS	S	-	-	-	-
-	-	-	-	-	-	H6	100	119	K12	VCAPDSI	S	-	-	-	-
-	-	-	-	-	-	J3	-	-	G13	VDD12DSI	S	-	-	-	-
-	-	-	-	-	-	J1	101	120	J12	DSI_D0P	I/O	-	-	-	-
-	-	-	-	-	-	J2	102	121	J13	DSI_D0N	I/O	-	-	-	-
-	-	-	-	-	-	H5	103	122	G12	VSSDSI	S	-	-	-	-
-	-	-	-	-	-	H4	104	123	H12	DSI_CKP	I/O	-	-	-	-
-	-	-	-	-	-	H3	105	124	H13	DSI_CKN	I/O	-	-	-	-
-	-	-	-	-	-	-	106	125	-	VDD12DSI	S			-	-
-	-	-	-	-	-	H1	107	126	F12	DSI_D1P	I/O		-	-	-
-	-	-	-	-	-	H2	108	127	F13	DSI_D1N	I/O		-	-	-
-	-	-	-	-	-	-	109	128	-	VSSDSI	S		-	-	-
-	-	-	-	126	G13	-	-	-	-	PK0	I/O	FT	-	LCD_G5, EVENTOUT	-
-	-	-	-	127	F12	-	-	-	-	PK1	I/O	FT	-	LCD_G6, EVENTOUT	-
-	-	-	-	128	F13	-	-	-	-	PK2	I/O	FT	-	LCD_G7, EVENTOUT	-
-	87	L15	106	129	M13	H9	110	129	M13	PG2	I/O	FT	-	FMC_A12, EVENTOUT	-
-	88	K15	107	130	M12	G9	111	130	M12	PG3	I/O	FT	-	FMC_A13, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	89	K14	108	131	N12	G1	112	131	N12	PG4	I/O	FT	-	FMC_A14/FMC_BA0, EVENTOUT	-
-	90	K13	109	132	N11	G2	113	132	N11	PG5	I/O	FT	-	FMC_A15/FMC_BA1, EVENTOUT	-
-	91	J15	110	133	J15	G3	114	133	J15	PG6	I/O	FT	-	FMC_NE3, DCMI_D12, LCD_R7, EVENTOUT	-
-	92	J14	111	134	J14	G4	115	134	J14	PG7	I/O	FT	-	SAI1_MCLK_A, USART6_CK, FMC_INT, DCMI_D13, LCD_CLK, EVENTOUT	-
-	93	H14	112	135	H14	G5	116	135	H14	PG8	I/O	FT	-	SPI6_NSS, SPDIF_RX2, USART6_RTS, ETH_PPS_OUT, FMC_SDCLK, LCD_G7, EVENTOUT	-
-	94	G12	113	136	G10	F1	117	136	G10	VSS	S		-	-	-
-	95	H13	114	137	G11	F2	118	137	G11	VDDUSB	S		-	-	-
63	96	H15	115	138	H15	G6	119	138	H15	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, I2S2_MCK, DFSDM1_CKIN3, USART6_TX, FMC_NWAIT, SDMMC2_D6, SDMMC1_D6, DCMI_D0, LCD_HSYNC, EVENTOUT	-
64	97	G15	116	139	G15	F3	120	139	G15	PC7	I/O	FT	-	TIM3_CH2, TIM8_CH2, I2S3_MCK, DFSDM1_DATIN3, USART6_RX, FMC_NE1, SDMMC2_D7, SDMMC1_D7, DCMI_D1, LCD_G6, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
65	98	G14	117	140	G14	G8	121	140	G14	PC8	I/O	FT	-	TRACED1, TIM3_CH3, TIM8_CH3, UART5_RTS, USART6_CK, FMC_NE2/FMC_NCE, SDMMC1_D0, DCMI_D2, EVENTOUT	
66	99	F14	118	141	F14	E1	122	141	F14	PC9	I/O	FT	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, LCD_G3, SDMMC1_D1, DCMI_D3, LCD_B2, EVENTOUT	--
67	100	F15	119	142	F15	E2	123	142	F15	PA8	I/O	FT	-	MCO1, TIM1_CH1, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_FS_SOF, CAN3_RX, UART7_RX, LCD_B3, LCD_R6, EVENTOUT	-
68	101	E15	120	143	E15	F4	124	143	E15	PA9	I/O	FT	-	TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, DCMI_D0, LCD_R5, EVENTOUT	OTG_FS_VBUS
69	102	D15	121	144	D15	F5	125	144	D15	PA10	I/O	FT	-	TIM1_CH3, USART1_RX, LCD_B4, OTG_FS_ID, MDIOS_MDIO, DCMI_D1, LCD_B1, EVENTOUT	-
70	103	C15	122	145	C15	E3	126	145	C15	PA11	I/O	FT	-	TIM1_CH4, SPI2_NSS/I2S2_WS, UART4_RX, USART1_CTS, CAN1_RX, OTG_FS_DM, LCD_R4, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
71	104	B15	123	146	B15	D1	127	146	B15	PA12	I/O	FT	-	TIM1_ETR, SPI2_SCK/I2S2_CK, UART4_TX, USART1_RTS, SAI2_FS_B, CAN1_TX, OTG_FS_DP, LCD_R5, EVENTOUT	-
72	105	A15	124	147	A15	D2	128	147	A15	PA13(JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
73	106	F13	125	148	E11	C1	129	148	E11	VCAP_2	S	-	-	-	-
74	107	F12	126	149	F10	C2	130	149	F10	VSS	S	-	-	-	-
75	108	G13	127	150	F11	B2	131	150	F11	VDD	S	-	-	-	-
-	-	E12	128	151	E12	F6	-	151	E12	PH13	I/O	FT	-	TIM8_CH1N, UART4_TX, CAN1_TX, FMC_D21, LCD_G2, EVENTOUT	-
-	-	E13	129	152	E13	F7	-	152	E13	PH14	I/O	FT	-	TIM8_CH2N, UART4_RX, CAN1_RX, FMC_D22, DCMI_D4, LCD_G3, EVENTOUT	-
-	-	D13	130	153	D13	E5	-	153	D13	PH15	I/O	FT	-	TIM8_CH3N, FMC_D23, DCMI_D11, LCD_G4, EVENTOUT	-
-	-	E14	131	154	E14	E4	132	154	E14	PI0	I/O	FT	-	TIM5_CH4, SPI2_NSS/I2S2_WS, FMC_D24, DCMI_D13, LCD_G5, EVENTOUT	-
-	-	D14	132	155	D14	B3	133	155	D14	PI1	I/O	FT	-	TIM8_BKIN2, SPI2_SCK/I2S2_CK, FMC_D25, DCMI_D8, LCD_G6, EVENTOUT	-
-	-	C14	133	156	C14	C3	-	156	C14	PI2	I/O	FT	-	TIM8_CH4, SPI2_MISO, FMC_D26, DCMI_D9, LCD_G7, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	-	C13	134	157	C13	D3	134	157	C13	PI3	I/O	FT	-	TIM8_ETR, SPI2_MOSI/I2S2_SD, FMC_D27, DCMI_D10, EVENTOUT	-
-	-	D9	135	-	F9	-	135	-	F9	VSS	S	-	-	-	
-	-	C9	136	158	E10	-	136	158	E10	VDD	S	-	-	-	--
76	109	A14	137	159	A14	A3	137	159	A14	PA14(JTCK-SWCLK)	I/O	FT	-	JTCK-SWCLK, EVENTOUT	-
77	110	A13	138	160	A13	F8	138	160	A13	PA15(JTDI)	I/O	FT	-	JTDI, TIM2_CH1/TIM2_ETR, HDMI_CEC, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, SPI6_NSS, UART4_RTS, CAN3_TX, UART7_TX, EVENTOUT	-
78	111	B14	139	161	B14	B4	139	161	B14	PC10	I/O	FT	-	DFSDM1_CKIN5, SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, QUADSPI_BK1_IO1, SDMMC1_D2, DCMI_D8, LCD_R2, EVENTOUT	-
79	112	B13	140	162	B13	C4	140	162	B13	PC11	I/O	FT	-	DFSDM1_DATIN5, SPI3_MISO, USART3_RX, UART4_RX, QUADSPI_BK2_NCS, SDMMC1_D3, DCMI_D4, EVENTOUT	-
80	113	A12	141	163	A12	D4	141	163	A12	PC12	I/O	FT	-	TRACED3, SPI3_MOSI/I2S3_SD, USART3_CK, UART5_TX, SDMMC1_CK, DCMI_D9, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
81	114	B12	142	164	B12	A4	142	164	B12	PD0	I/O	FT	-	DFSDM1_CKIN6, DFSDM1_DATIN7, UART4_RX, CAN1_RX, FMC_D2, EVENTOUT	-
82	115	C12	143	165	C12	D5	143	165	C12	PD1	I/O	FT	-	DFSDM1_DATIN6, DFSDM1_CKIN7, UART4_TX, CAN1_TX, FMC_D3, EVENTOUT	--
83	116	D12	144	166	D12	D6	144	166	D12	PD2	I/O	FT	-	TRACED2, TIM3_ETR, UART5_RX, SDMMC1_CMD, DCMI_D11, EVENTOUT	-
84	117	D11	145	167	C11	B5	145	167	C11	PD3	I/O	FT	-	DFSDM1_CKOUT, SPI2_SCK/I2S2_CK, DFSDM1_DATIN0, USART2_CTS, FMC_CLK, DCMI_D5, LCD_G7, EVENTOUT	-
85	118	D10	146	168	D11	A5	146	168	D11	PD4	I/O	FT	-	DFSDM1_CKIN0, USART2_RTS, FMC_NOE, EVENTOUT	-
86	119	C11	147	169	C10	C5	147	169	C10	PD5	I/O	FT	-	USART2_TX, FMC_NWE, EVENTOUT	-
-	120	D8	148	170	F8	B6	148	170	F8	VSS	S	-	-	-	-
-	121	C8	149	171	E9	A6	149	171	E9	VDDSDMMC	S	-	-	-	-
87	122	B11	150	172	B11	E6	150	172	B11	PD6	I/O	FT	-	DFSDM1_CKIN4, SPI3_MOSI/I2S3_SD, SAI1_SD_A, USART2_RX, DFSDM1_DATIN1, SDMMC2_CK, FMC_NWAIT, DCMI_D10, LCD_B2, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
88	123	A11	151	173	A11	E7	151	173	A11	PD7	I/O	FT	-	DFSDM1_DATIN4, SPI1_MOSI/I2S1_SD, DFSDM1_CKIN1, USART2_CK, SPDIF_RX0, SDMMC2_CMD, FMC_NE1, EVENTOUT	-
-	-	-	-	174	B10	NC	-	174	B10	PJ12	I/O	FT	-	LCD_G3, LCD_B0, EVENTOUT	-
-	-	-	-	175	B9	NC	-	175	B9	PJ13	I/O	FT	-	LCD_G4, LCD_B1, EVENTOUT	-
-	-	-	-	176	C9	NC	-	176	C9	PJ14	I/O	FT	-	LCD_B2, EVENTOUT	-
-	-	-	-	177	D10	-	-	177	D10	PJ15	I/O	FT	-	LCD_B3, EVENTOUT	-
-	124	C10	152	178	D9	C6	152	178	D9	PG9	I/O	FT	-	SPI1_MISO, SPDIF_RX3, USART6_RX, QUADSPI_BK2_IO2, SAI2_FS_B, SDMMC2_D0, FMC_NE2/FMC_NCE, DCMI_VSYNC, EVENTOUT	-
-	125	B10	153	179	C8	A7	153	179	C8	PG10	I/O	FT	-	SPI1_NSS/I2S1_WS, LCD_G3, SAI2_SD_B, SDMMC2_D1, FMC_NE3, DCMI_D2, LCD_B2, EVENTOUT	-
-	126	B9	154	180	B8	B7	154	180	B8	PG11	I/O	FT	-	SPI1_SCK/I2S1_CK, SPDIF_RX0, SDMMC2_D2, ETH_MII_TX_EN/ETH_RMII_TX_EN, DCMI_D3, LCD_B3, EVENTOUT	-
-	127	B8	155	181	C7	D7	155	181	C7	PG12	I/O	FT	-	LPTIM1_IN1, SPI6_MISO, SPDIF_RX1, USART6_RTS, LCD_B4, SDMMC2_D3, FMC_NE4, LCD_B1, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
-	128	A8	156	182	B3	C7	156	182	B3	PG13	I/O	FT	-	TRACED0, LPTIM1_OUT, SPI6_SCK, USART6_CTS, ETH_MII_TXD0/ETH_RMII_TXD0, FMC_A24, LCD_R0, EVENTOUT	-
-	129	A7	157	183	A4	NC	157	183	A4	PG14	I/O	FT	-	TRACED1, LPTIM1_ETR, SPI6_MOSI, USART6_TX, QUADSPI_BK2_IO3, ETH_MII_TXD1/ETH_RMII_TXD1, FMC_A25, LCD_B0, EVENTOUT	-
-	130	D7	158	184	F7	A8	158	184	F7	VSS	S	-	-	-	-
-	131	C7	159	185	E8	B8	159	185	E8	VDD	S	-	-	-	-
-	-	-	-	186	D8	NC	-	186	D8	PK3	I/O	FT	-	LCD_B4, EVENTOUT	-
-	-	-	-	187	D7	NC	-	187	D7	PK4	I/O	FT	-	LCD_B5, EVENTOUT	-
-	-	-	-	188	C6	NC	-	188	C6	PK5	I/O	FT	-	LCD_B6, EVENTOUT	-
-	-	-	-	189	C5	NC	-	189	C5	PK6	I/O	FT	-	LCD_B7, EVENTOUT	-
-	-	-	-	190	C4	NC	-	190	C4	PK7	I/O	FT	-	LCD_DE, EVENTOUT	-
-	132	B7	160	191	B7	F9	160	191	B7	PG15	I/O	FT	-	USART6_CTS, FMC_SDNCAS, DCMI_D13, EVENTOUT	-
89	133	A10	161	192	A10	E8	161	192	A10	PB3 (JTDO/ TRACESWO)	I/O	FT	-	JTDO/TRACESWO, TIM2_CH2, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, SPI6_SCK, SDMMC2_D2, CAN3_RX, UART7_RX, EVENTOUT	-
90	134	A9	162	193	A9	D8	162	193	A9	PB4(NJTRST)	I/O	FT	-	NJTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, SPI2_NSS/I2S2_WS, SPI6_MISO, SDMMC2_D3, CAN3_TX, UART7_TX, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
91	135	A6	163	194	A8	A9	163	194	A8	PB5	I/O	FT	-	UART5_RX, TIM3_CH2, I2C1_SMBA, SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, SPI6_MOSI, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, FMC_SDCKE1, DCMI_D10, LCD_G7, EVENTOUT	-
92	136	B6	164	195	B6	B9	164	195	B6	PB6	I/O	FT	-	UART5_TX, TIM4_CH1, HDMI_CEC, I2C1_SCL, DFSDM1_DATIN5, USART1_TX, CAN2_TX, QUADSPI_BK1_NCS, I2C4_SCL, FMC_SDNE1, DCMI_D5, EVENTOUT	-
93	137	B5	165	196	B5	C8	165	196	B5	PB7	I/O	FT	-	TIM4_CH2, I2C1_SDA, DFSDM1_CKIN5, USART1_RX, I2C4_SDA, FMC_NL, DCMI_VSYNC, EVENTOUT	-
94	138	D6	166	197	E6	A10	166	197	E6	BOOT0	I	B	-	-	VPP
95	139	A5	167	198	A7	E9	167	198	A7	PB8	I/O	FT	-	I2C4_SCL, TIM4_CH3, TIM10_CH1, I2C1_SCL, DFSDM1_CKIN7, UART5_RX, CAN1_RX, SDMMC2_D4, ETH_MII_TXD3, SDMMC1_D4, DCMI_D6, LCD_B6, EVENTOUT	-

Table 10. STM32F765xx, STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F765xx STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180[1]	LQFP176	LQFP208	TFBGA216						
96	140	B4	168	199	B4	D9	168	199	B4	PB9	I/O	FT	-	I2C4_SDA, TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, DFSDM1_DATIN7, UART5_TX, CAN1_TX, SDMMC2_D5, I2C4_SMBA, SDMMC1_D5, DCMI_D7, LCD_B7, EVENTOUT	-
97	141	A4	169	200	A6	C9	169	200	A6	PE0	I/O	FT	-	TIM4_ETR, LPTIM1_ETR, UART8_RX, SAI2_MCLK_A, FMC_NBL0, DCMI_D2, EVENTOUT	-
98	142	A3	170	201	A5	B10	170	201	A5	PE1	I/O	FT	-	LPTIM1_IN2, UART8_TX, FMC_NBL1, DCMI_D3, EVENTOUT	-
99	-	D5	-	202	F6	A11	-	202	F6	VSS	S	-	-	-	-
-	143	C6	171	203	E5	C10	171	203	E5	PDR_ON	S	-	-	-	-
100	144	C5	172	204	E7	B11	172	204	E7	VDD	S	-	-	-	-
-	-	D4	173	205	C3	D10	173	205	C3	PI4	I/O	FT	-	TIM8_BKIN, SAI2_MCLK_A, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT	-
-	-	C4	174	206	D3	D11	174	206	D3	PI5	I/O	FT	-	TIM8_CH1, SAI2_SCK_A, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT	-
-	-	C3	175	207	D6	C11	175	207	D6	PI6	I/O	FT	-	TIM8_CH2, SAI2_SD_A, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT	-
-	-	C2	176	208	D4	B12	176	208	D4	PI7	I/O	FT	-	TIM8_CH3, SAI2_FS_A, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT	-