Improving Flash Write Performance by Using Strong ECC Scheme

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***Abstract*—The adoption of smaller geometries and multi-level cell (MLC) technologies significantly expands the capacity and drops the price of flash memory, which, at the same time, noticeably degrades the performance and reliability of the devices. As incremental-step pulse programming (ISPP) scheme is used to increase the program accuracy for MLC cells, there is a trade-off between the SSD write speed and raw storage reliability. What's more, ECC are widely used in SSDs to provide error-tolerance ability. Therefore, if we could use stronger ECC to increase error correction strength, a coarser step size could be applied in the ISPP scheme to promote the write performance. However, stronger ECC scheme may hurt the read performance due to the increased decoding complexity and latency.**

In this paper, we propose an operation-aware differentiated ECC scheme to improve the SSD write performance without any sacrifice of the read performance. The main idea is to dynamically classify the logical pages into three categories: pure write, pure read, and overlapped part. For pure write logical pages, a faster write scheme that uses coarser step size will be applied to increase the write speed with a stronger ECC scheme to guarantee the reliability. For a pure read logical page encoded with a stronger ECC, we will rewrite it with the normal ISPP and ECC scheme if its hotness exceed a pre-defined threshold. While for the overlapped part, the faster write scheme will be selectively used based on the relative read and write hotness of the logical pages. Our evaluation shows that our operation-aware differentiated ECC scheme could improve the write performance by x% on average.

I. Introduction

NAND Flash-based Solid State Disk (SSD) has been widely deployed in various environments because of its high performance, nonvolatile property, and low power consumption. To continuously increase the capacity and reduce the bit cost, manufactures are aggressively scaling down the geometries and storing more bits information per flash cell [**?**].

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II. Background and Motivation

III. Conclusion

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References