EN.520.216 Homework 2

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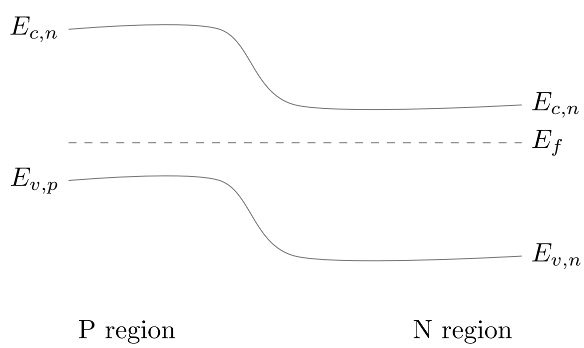
Problem 1 1. First notice that the voltage at the anode of D4 is 0.6V (0V ground+dropoff voltage), and likewise the voltages at the anodes of D1, D2, and D3 are 1.2V, 0.9V, and 0.9V respectively. This is when we use the first-order model where a diode is considered to be a source with the positive terminal on the side opposing current flow. Because the supply voltage is maintained at 18V, it follows that the respective currents are $I_1 = \frac{18-1.2}{2200} = 7.63mA$, $I_2 = \frac{18-0.9}{2700} = 6.33mA$, and $I_3 = \frac{18-0.9}{1000} = 17.1mA$. By Kirchoff's law the current through the source is then 31.06mA.

2. All of the diodes are forward-biased, since the voltage at the anode is lower than the voltage at the cathode.

3. The power absorbed by D4 can be computed from $P = IV$ where I and V are the current and voltage through the component. Using I_d and 0.6V we get $P = 18.636mW$.

Problem 2 1.



2. We consider that the valence level in the n-type region opposing the junction has 0 energy relative to the rest of the system, and thus an intrinsic fermi level of $\frac{1}{2}(1.1) = 0.55$ eV. We can then use a straight application of the formula $\ln(\frac{n_i}{n_d}) = \frac{-\Delta E}{kT}$ with $n \approx N_D = 8 \times 10^{16}$ to find the shift of the fermi energy relative to that intrinsic fermi level. We find this to be 0.38eV. The fermi level is then at 0.93eV.

3. The contact potential is given by $\Phi \ln \frac{N_A N_D}{n_i^2}$ where $\Phi = \frac{kT}{q} \approx 26mV$ at 300K. This means that V_o for this particular junction is about 0.837V.

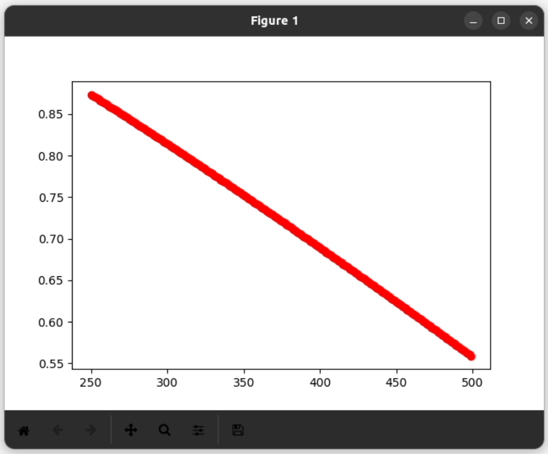


Figure 1: Temperature vs. built-in voltage

Problem 3

1. No, the diode is not always forward biased. For example, when the sinusoid goes negative, the diode is always going to be reversed biased.

2. The diode makes sure that only current in the positive direction goes through the load. The capacitor makes sure that a positive voltage is at least partially maintained through the load even when the source tries to pull current the other way (where usually there would be no current through the resistor thanks to the diode).

3. We first note that the saturation current of this diode vastly diverges from the one we would expect from a silicon diode so we can't make a direct assumption about its voltage drop (e.g 0.7V).
Instead we find the value of R in terms of the abstract V_{DOn} variable and estimate its value with a simple model.
The circuit can be partitioned in two periods of operation: a) while the diode is in forward conduction (mostly on the rising of the voltage source) and b) when the diode is reversed biased.
The latter happens not only when the voltage source is in the negative region but also right after it reaches its peak, since the capacitor would have already been charged and discharges through the resistor more slowly than the voltage on the voltage source decreases back down (otherwise, there would be no ripple, just a half-rectified wave).
Hence, the time period that the capacitor discharges through the load resistor (with no help from the voltage source) is $[\frac{1}{4}T, t_1]$, where T is the period of the sinusoid and t_1 is the timestamp at which the diode is back

in forward conduction.
We know t_1 to satisfy $\sin 20\pi t_1 = V_{DOn}$, and if we limit ourselves to its first instance we have $t_1 = \frac{1}{20\pi}\sin^{-1}(V_{DOn}) + \frac{1}{10}$. (adding the length of one period). We want to make sure that during that known amount of time, the voltage across the load does not decrease more than $1 - V_{DOn} - 0.5$, from its original value of $1 - V_{DOn}$. Within this time period, the load is just looking at a capacitor, and we know the equation of this setup to be

$$\int_{t=\frac{1}{4}T}^{\frac{1}{20\pi}\sin^{-1}(V_{DOn})+\frac{1}{10}} \frac{1}{RC}dt = \int_{1-V_{DOn}-0.5}^{1-V_{DOn}} \frac{1}{V_c(t)}dV_c(t)$$

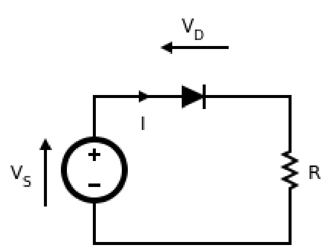
$$\therefore R = \frac{\frac{1}{20\pi}\sin^{-1}(V_{DOn}) + \frac{3}{40}}{10 \times 10^{-6}\ln\left(\frac{1-V_{DOn}}{1-V_{DOn}-0.5}\right)}$$

Just as we did to obtain the 0.7V estimation of the silicon diode, we can set up a voltage source, diode, and resistor in series and solve under the exponential model to get V_{DOn} (see figure below). With a 1V source and 10kΩ resistor, we have $1 - V_{DOn} - 1.8 \times 10^{-2}(e^{V_{DOn}/\Phi_T} - 1) = 0$, which gives a V_{DOn} value of 0.103V. Choosing other values of V and R as well neighbors this value.

Putting this back in the equation, we get $R \approx 9402\Omega$, our final answer.

4. The maximum output voltage under the constant drop model is given by the max source voltage minus one voltage drop, or about 0.897V

5.



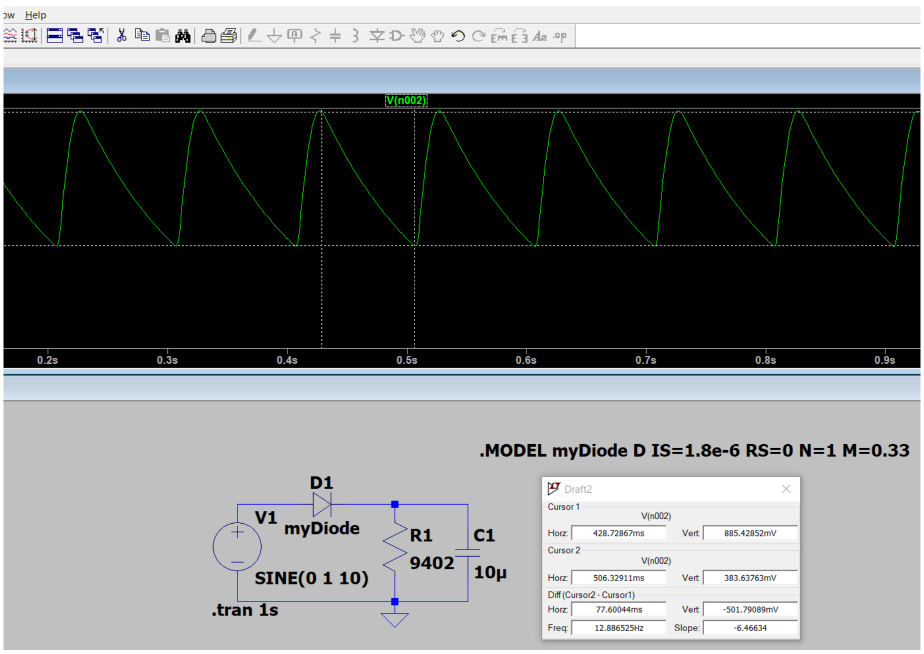


Figure 2: LTSpice Simulation