Cadence Homework 0

LJ Gonzales

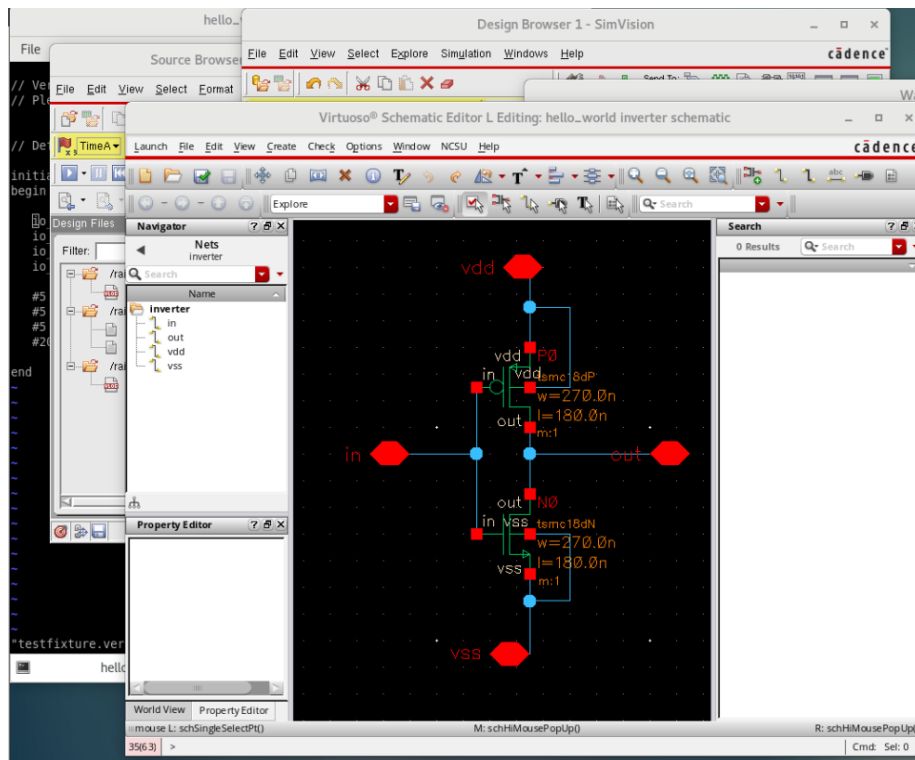## March 2023

Figure 1: Creating a cell
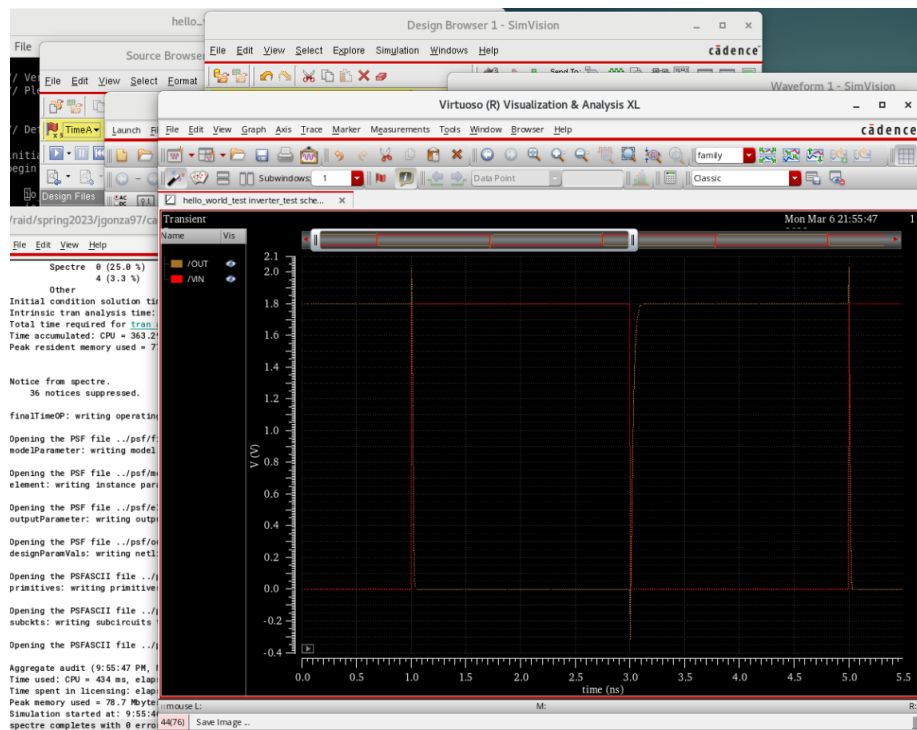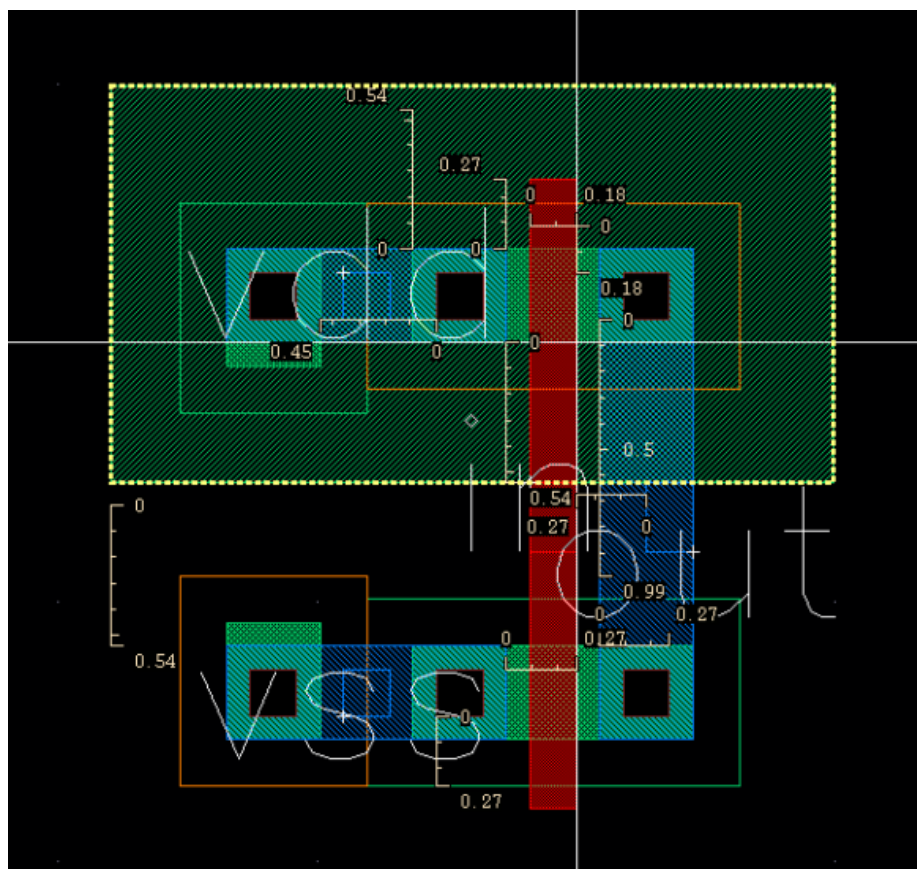
Figure 2: Creating symbol

Figure 3: Schematic DC Sweep

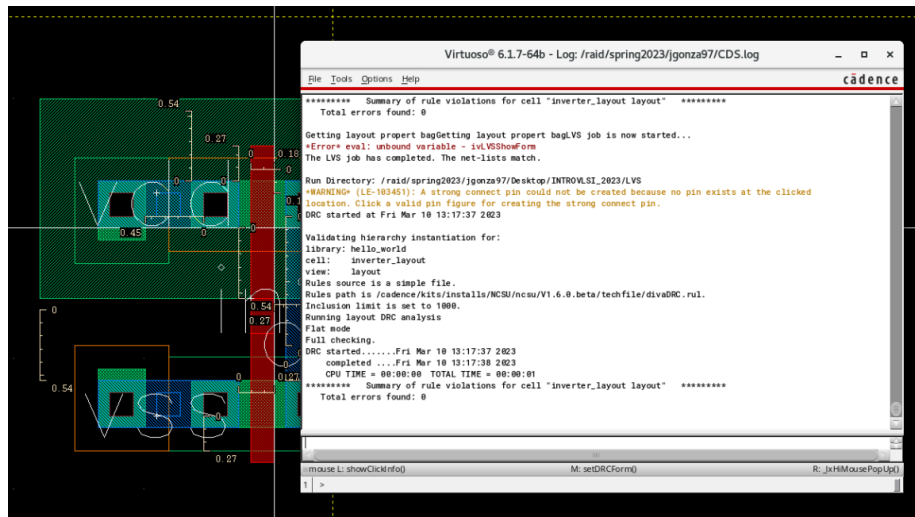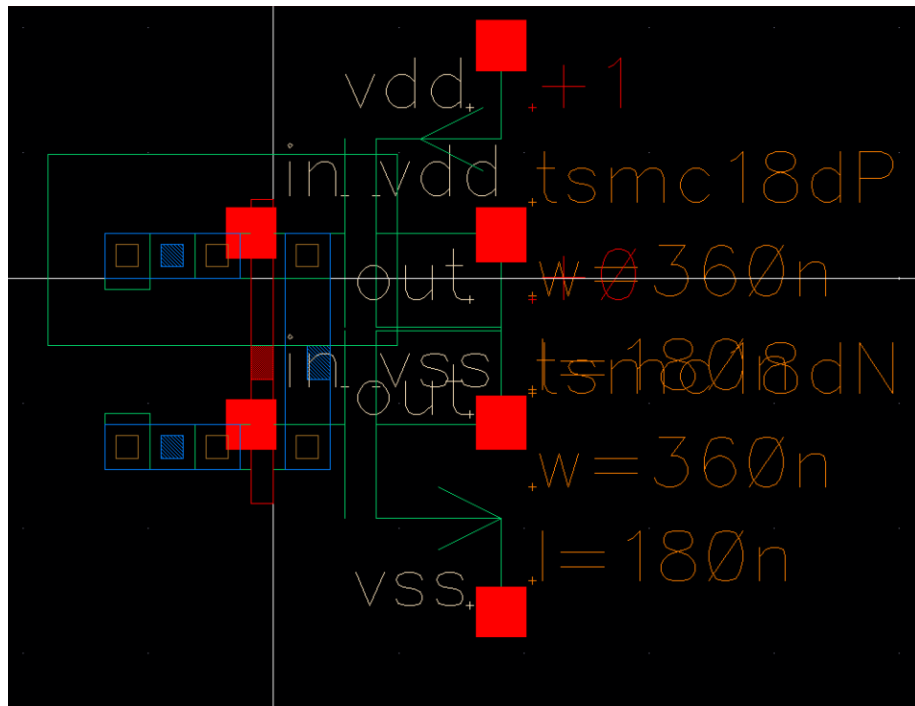Figure 4: Transient Analysis

Figure 5: Layout

Figure 6: Layout DRC Check

Figure 7: Extracted
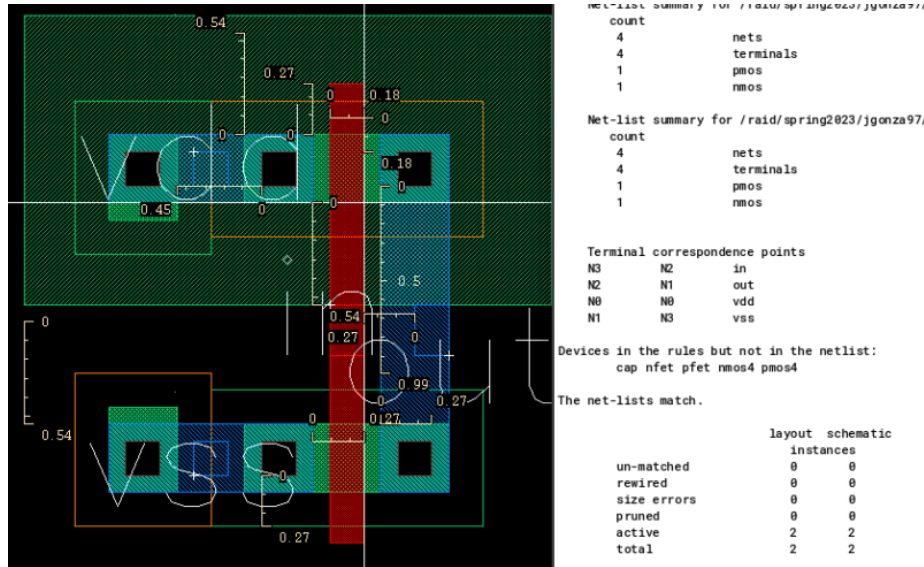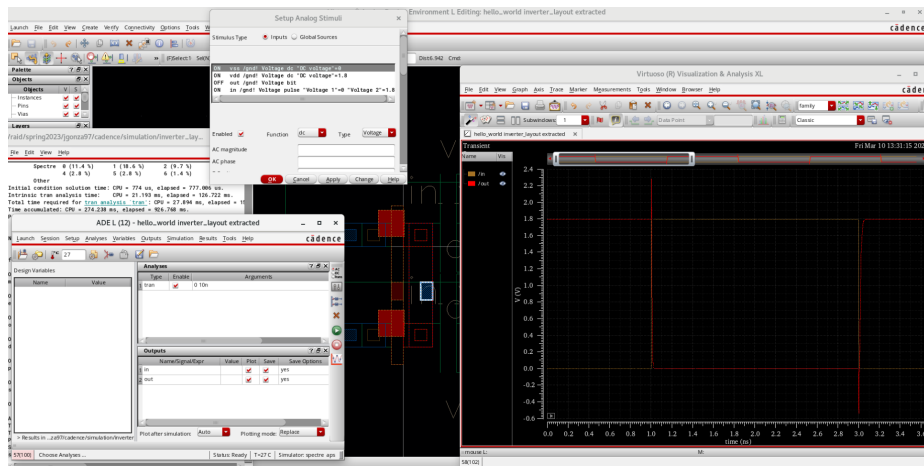
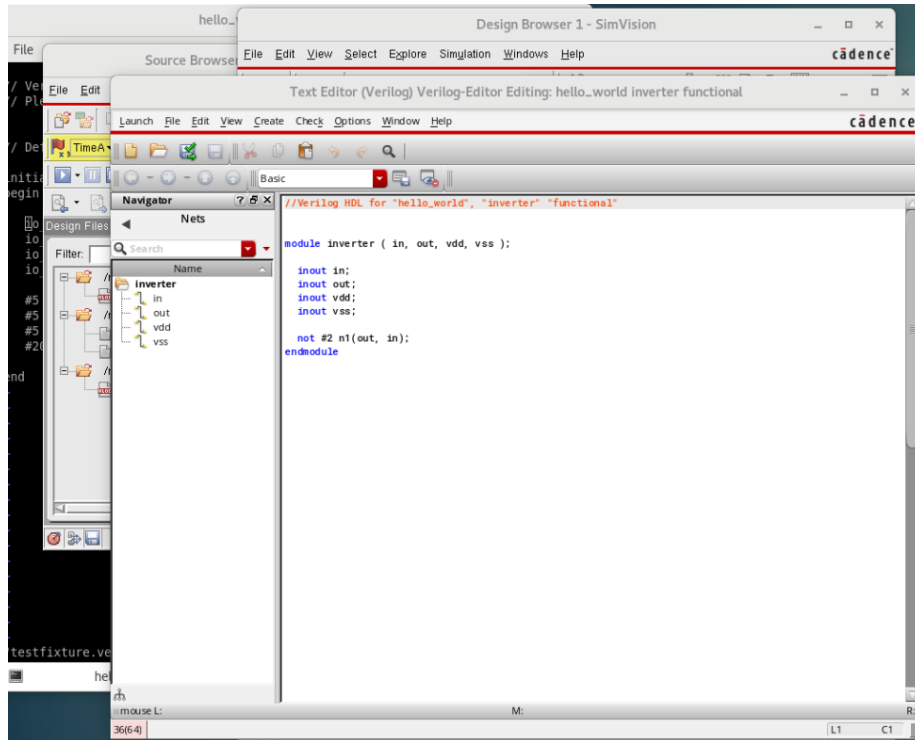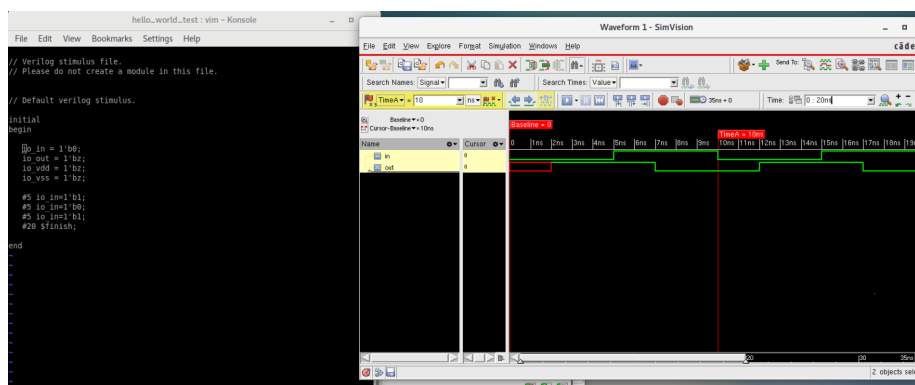Figure 8: LVS Check

Figure 9: Extracted transient analysis

Figure 10: Functional

Figure 11: Verilog .txt and Waveform output