Cycle	Reset	PC	Instr	(FSM) state	Src A	SrcB	ALUResult	Zero	Control Word
1	1	00	0	0	00	04	04	0	5010
2	0	04	addi 200200	05 1	04	Х	X	0	0030
3	0	04	addi 200200	05 9	00	05	05	0	0420
4	0	04	addi 200200		Х	X	X	0	0800
5	0	04	addi 200200	05 0	04	04	08	0	5010
6	0	08	addi 200300	0c 1	08	Х	Х	0	0030
7	0	08	addi 200300	0c 9	00	0c	0c	0	0420
8	0	08	addi 200300	0c 10	Х	Х	Х	0	0800
9	0	08	addi 200300	0c 0	08	0c	0c	0	5010
10	0	0c	addi 2067ff	f7 1	0c	Х	х	0	0030
11	0	0c	addi 2067ff	f7 9	0c	-9	03	0	0420
12	0	0c	addi 2067ff	f7 10	X	X	Х	0	0800
13	0	0c	addi 2067ff	f7 0	0c	10	10	0	5010
14	0	10	or 00e220		10	X	X	0	0030
15	0	10	or 00e220		03	05	07	0	0402
16	0	10	or 00e220		X	X	X	0	0840
17	0	10	or 00e220		10	04	14	0	5010
18	0	14	and 006428		14	X	X	0	0030
19	0	14	and 006428		0C	07	04	0	0402
20	0	14	and 006428				X X	0	0840
21	0	14	and 006428		14	04	18	0	5010
22	0	18			18	_		0	0030
	_		add 00a428			X	X	_	
23	0	18	add 00a428		04	07	0b	0	0402
24	0	18	add 00a428		X	X	X	0	0840
25	0	18	add 00a428		18	04	1c	0	5010
26	0	1c	Beq 10a700		1c	X	X	0	0030
27	0	1c	Beq 10a700		0b	03	08	0	0605
28	0	1c	Beq 10a700		1c	04	20	0	5010
29	0	20	Slt 006420	2a   1	20	X	X	0	0030
30	0	20	Slt 006420	2a 6	0c	07	00	0	0402
31	0	20	Slt 006420	2a 7	Х	Х	Х	0	0840
32	0	20	Slt 006420	2a 0	20	28	28	0	5010
33	0	28	Beq 108000	01 1	28	Х	х	1	0030
34	0	28	Beg 108000	01 8	00	00	00	1	0605
35	0	28	Beg 108000		28	04	2c	1	5010
36	0	2c	Slt 00e220		2c	X	X	0	0030
37	0	2c	Slt 00e220		03	05	01	0	0402
38	0	2c	Slt 00e220		X	X	X	0	0840
39	0	2c		= 4	2c	04	30	0	5010
	_			= 4					
40	0	30	add 008538		30	X	X	0	0030
41	0	30	add 008538		01	0b	0c	0	0402
42	0	30	add 008538		X	X	X	0	0840
43	0	30	add 008538		30	04	34	0	5010
44	0	34	sub 00e238	_	34	X	X	0	0030
45	0	34	sub 00e238		0c	05	07	0	0402
46	0	34	sub 00e238		X	X	X	0	0840
47	0	34	sub 00e238		34	04	38	0	5010
48	0	38	sw ac6700		38	X	Х	0	0030
49	0	38	sw ac6700		0c	44	50	0	0420
50	0	38	sw ac6700		Х	Х	Х	0	2100
51	0	38	sw ac6700		38	04	3c	0	5010
52	0	3c	lw 8c0200		3c	Х	Х	0	0030
53	0	3c	lw 8c0200	50 2	00	50	50	0	0420
54	0	3c	lw 8c0200	50 3	Х	Х	Х	0	0100
55	0	3c	lw 8c0200	50 4	Х	Х	Х	0	0880
56	0	3c	lw 8c0200		3c	04	40	0	5010
57	0	40	J 080000		40	X	X	0	0030
58	0	40	J 080000		X	X	X	0	4008
59	0	40	J 080000		40	48	48	0	5010
60	0	48	Sw ac0200		48	X	X	0	0030
61	0	48	Sw ac0200		00	54	54		0420
							<del>                                     </del>	0	
62	0	48	Sw ac0200		X	X	X	0	2100

**Table 1. Expected Instruction Trace**