

Zainab Hussein

Lab 8 Prelab

Table 1. Main Decoder Control Output

State (Name)	PCWrite	MemWrite	IRWrite	RegWrite	ALUSrcA	Branch	IOrd	MemtoReg	RegDst	ALUSrcB[1:0]	PCRsc[1:0]	ALUOp[1:0]	FSM Control Word
0 (Fetch)	1	0	1	0	0	0	0	0	0	01	00	00	0x5010
1 (Decode)	0	0	0	0	0	0	0	0	0	11	00	00	0x0030
2 (MemAdr)	0	0	0	0	1	0	0	0	0	10	00	00	0x0420
3 (MemRd)	0	0	0	0	1	0	1	0	0	10	00	00	0x0520
4 (MemWB)	0	0	0	1	1	0	1	1	0	10	00	00	0x0DA0
5 (MemWr)	0	1	0	0	1	0	1	0	0	10	00	00	0x2520
6 (RtypeEx)	0	0	0	0	1	0	0	0	0	00	00	10	0x0402
7 (RtypeWB)	0	0	0	1	1	0	0	0	1	00	00	10	0x0C42
8 (BeqEx)	0	0	0	0	1	1	0	0	0	00	01	01	0x0605
9 (AddiEx)	0	0	0	0	1	0	0	0	0	10	00	00	0x0420
10 (AddiWB)	0	0	0	1	1	0	0	0	0	10	00	00	0x0C20
11 (JEx)	1	0	0	0	0	0	0	0	0	11	10	00	0x4038