Cycle	Reset	IF	ID	EX	MEM	WB
1	1	addi $2, $0, 5	nop	nop	nop	nop
2	0	addi $3, $0, 12	addi $2, $0, 5	nop	nop	nop
3	0	addi $7, $3, -9	addi $3, $0, 12	addi $2, $0, 5	nop	nop
4	0	or $4, $7, $2	addi $7, $3, -9	addi $3, $0, 12	addi $2, $0, 5	nop
5	0	and $5, $3, $4	or $4, $7, $2	addi $7, $3, -9	addi $3, $0, 12	addi $2, $0, 5
6	0	add $5, $5, $4	and $5, $3, $4	or $4, $7, $2	addi $7, $3, -9	addi $3, $0, 12
7	0	beq $5, $7, end	add $5, $5, $4	and $5, $3, $4	or $4, $7, $2	addi $7, $3, -9
8	0	slt $4, $3, $4	beq $5, $7, end	add $5, $5, $4	and $5, $3, $4	or $4, $7, $2
9	0	slt $4, $3, $4	beq $5, $7, end	*nop*	add $5, $5, $4	and $5, $3, $4
10	0	beq $4, $0, around	slt $4, $3, $4	beq $5, $7, end	nop	add $5, $5, $4
11	0	addi $5, $0, 0	beq $4, $0, around	slt $4, $3, $4	beq $5, $7, end	nop
12	0	addi $5, $0, 0	beq $4, $0, around	nop	slt $4, $3, $4	beq $5, $7, end
13	0	slt $4, $7, $2	nop	beq $4, $0, around	nop	slt $4, $3, $4
14	0	add $7, $4, $5	slt $4, $7, $2	nop	beq $4, $0, around	nop
15	0	sub $7, $7, $2	add $7, $4, $5	slt $4, $7, $2	nop	beq $4, $0, around
16	0	sw $7, 68($3)	sub $7, $7, $2	add $7, $4, $5	slt $4, $7, $2	nop
17	0	lw 42, 80($0)	sw $7, 68($3)	sub $7, $7, $2	add $7, $4, $5	slt $4, $7, $2
18	0	j end	lw 42, 80($0)	sw $7, 68($3)	sub $7, $7, $2	add $7, $4, $5
19	0	addi $2, $0, 1	j end	lw 42, 80($0)	sw $7, 68($3)	sub $7, $7, $2
20	0	sw $2, 84($0)	nop	j end	lw 42, 80($0)	sw $7, 68($3)
21	0		sw $2, 84($0)	nop	j end	lw 42, 80($0)
22	0			sw $2, 84($0)	nop	j end
23	0				sw $2, 84($0)	nop
24	0					sw $2, 84($0)

Table 1. Expected Instruction Trace

Note: The number of included cycles is not necessarily the number of expected cycles

Cycle	Reset	PCF	brjflush	forwardAE	forwardBE	forwardAD	forwardBD	branchstall	lwstall
1	1	0x00	0	00	00	0	0	0	0
2	0	0x04	0	00	00	0	0	0	0
3	0	0x08	0	00	00	0	0	0	0
4	0	0x0C	0	00	00	0	0	0	0
5	0	0x10	0	10	00	0	0	0	0
6	0	0x14	0	10	00	0	0	0	0
7	0	0x18	0	00	10	0	0	0	0
8	0	0x1C	0	10	01	1	0	1	0
9	0	0x1C	0	00	00	1	0	0	0
10	0	0x20	0	00	00	0	0	0	0
11	0	0x24	0	00	00	0	0	1	0
12	0	0x24	1	00	00	1	0	0	0
13	0	0x28	0	00	00	0	0	0	0
14	0	0x2C	0	00	00	0	0	0	0
15	0	0x30	0	00	00	0	0	0	0
16	0	0x34	0	10	00	0	0	0	0
17	0	0x38	0	10	00	0	0	0	0
18	0	0x3C	0	10	00	0	0	0	0
19	0	0x40	1	00	00	0	0	0	0
20	0	0x44	0	00	00	0	0	0	0
21	0	0x48	0	00	00	0	0	0	0
22	0	0x4C	0	00	00	0	0	0	0
23	0	0x50	0	00	00	0	0	0	0
24	0	0x54	0	00	00	0	0	0	0

Table 2. Expected Forward and Stall Signal