Clock gating

Clock gating is a power-saving technique used in digital design and integrated circuits to reduce power consumption when certain parts of a circuit are not in use. It involves controlling the clock signal to specific parts of a circuit so that they only receive clock pulses when needed, as opposed to receiving a constant clock signal.

Here's how clock gating works:

1. Clock Signal: In most digital circuits, there is a central clock signal that synchronizes the operation of various components. This clock signal usually runs continuously at a fixed frequency.

2. Gating Logic: Clock gating involves the use of gating logic to control whether the clock signal is allowed to pass through to specific elements of the circuit or not.

3. Enable Signal: The gating logic generates an "enable" signal based on certain conditions or control inputs. When this enable signal is active (usually high), it allows the clock signal to pass through to the associated circuit elements.

4. Power Saving: When the enable signal is inactive (usually low), the clock signal is effectively blocked or gated, preventing it from reaching the components it controls. This means that these components do not consume power by toggling or switching states when they are not in use.

Clock gating is particularly useful in situations where parts of a digital circuit are not active all the time, such as in microprocessors and other integrated circuits. For example, when a CPU is executing a simple instruction, some functional units within the CPU may not be needed. By gating the clock signal to these unused functional units, power consumption can be significantly reduced.

Normal clock gating using an AND gate can produce glitches because of the differences in propagation delays between the clock enable signal and the original clock signal. This happens due to the fundamental nature of digital logic gates and the fact that they have finite propagation delays.

1. Original Clock Signal (CLK): This is the main clock signal that drives the entire circuit.

2. Clock Enable Signal (EN): This signal is generated by the gating logic (typically an AND gate) and determines whether the clock signal should pass through or be blocked.

3. Glitch Scenario:

- Initially, EN is low (0), meaning the clock gating logic is blocking the clock signal (CLK).
- At some point, the control signal that determines EN transitions from low (0) to high (1), indicating that the clock should be allowed to pass through.
- Due to the finite propagation delay of the AND gate (or any other logic gate used in the clock gating), there is a slight delay before EN transitions from 0 to 1.
- During this delay, CLK may still be high because it has not yet propagated through the AND gate, but EN is transitioning to high.
- This results in a brief period where CLK is high, but EN is also transitioning to high. This brief overlap creates a glitch, where the clock signal briefly turns on when it should have been off.

Integrated clock gating

Integrated clock gating is a design technique used in modern integrated circuits (ICs) to reduce power consumption by controlling the clock signal to specific blocks or components within the chip. It's a more advanced and efficient form of clock gating compared to traditional methods. Integrated clock gating is especially crucial in power-sensitive devices like mobile devices and battery-powered systems.

1. Local Clock Gating: Integrated clock gating involves adding clock gating logic within individual functional blocks or modules of an IC. Instead of gating the clock signal at a global level, it is done locally within the specific block where it is needed. This enables fine-grained control over power consumption.

2. Automatic Generation: Many modern digital design tools and methodologies include automated clock gating insertion. The tools analyse the design and identify opportunities for clock gating based on user-defined constraints and power-saving goals. The gating logic is then automatically generated and inserted into the design.

3. Dynamic Control: Integrated clock gating often includes dynamic control mechanisms. This means that the gating logic can be activated or deactivated based on the actual activity or usage of a particular block. If a block is idle or not in use, the clock gating logic can turn off the clock signal to that block, reducing power consumption.

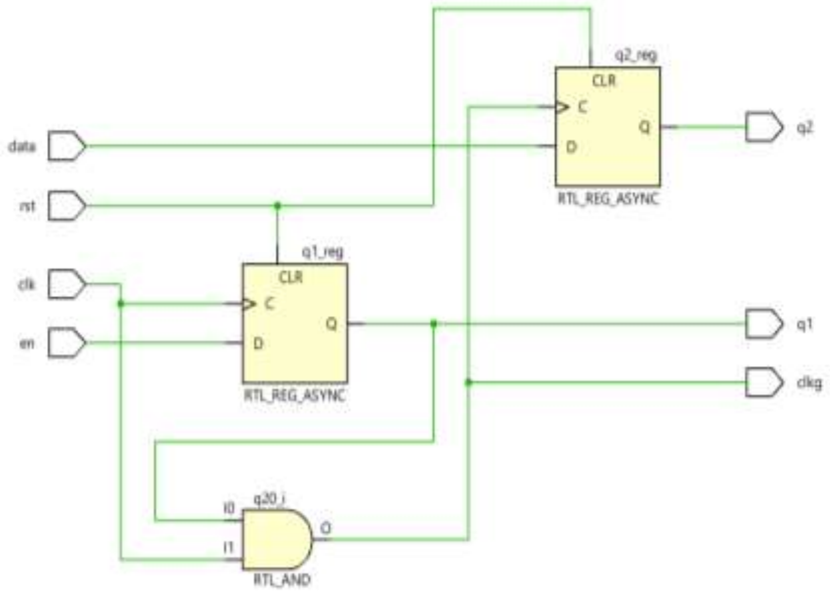
4. Glitch-Free Operation: Integrated clock gating solutions are designed to minimize or eliminate glitches that might occur during clock gating transitions. Specialized synchronization techniques and circuitry are used to ensure that clock signals are gated without introducing timing issues or unexpected behaviour.

5. Power Savings: By using integrated clock gating, ICs can significantly reduce dynamic power consumption. When functional blocks are not actively processing data or performing tasks, their clock signals are gated, preventing unnecessary power dissipation in switching logic.

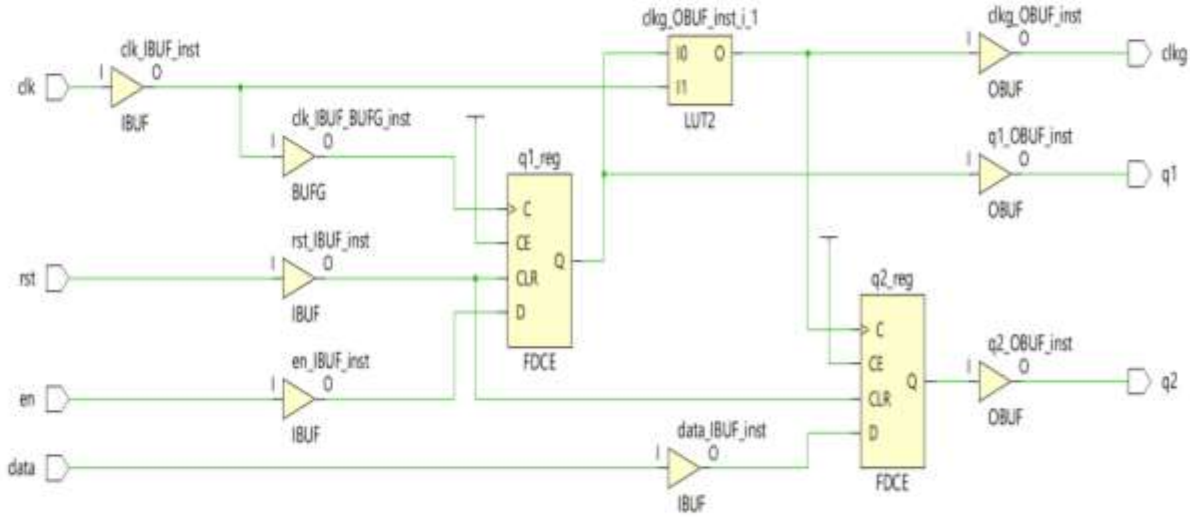
6. Performance Trade-offs: While integrated clock gating is highly effective at reducing power consumption, it can introduce some latency when re-enabling clock signals. Designers need to carefully consider the trade-offs between power savings and performance when implementing clock gating.

7. Clock Domain Isolation: Integrated clock gating is often used in conjunction with clock domain isolation techniques. Different functional blocks may operate on different clock domains, and clock gating ensures that only the necessary clock domains are active at any given time.

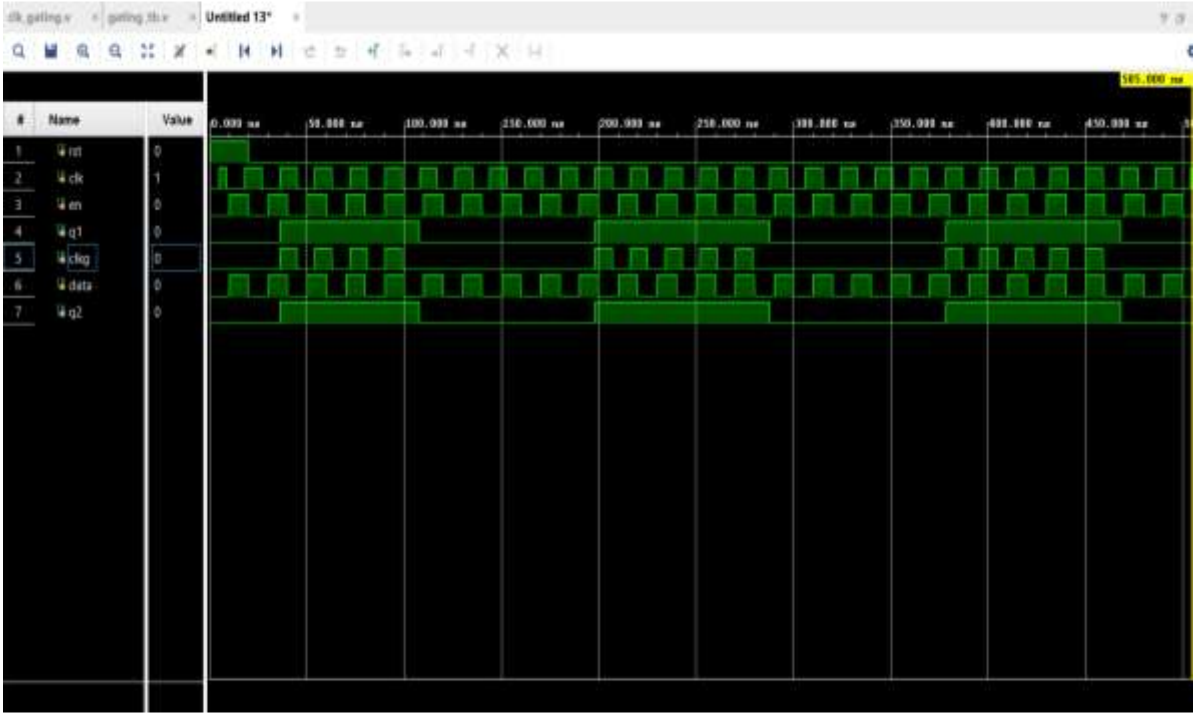
Elaborated design



Implemented design



Behavioural design



ICG cell basically stops the clock propagation through it when we apply a low clock enable signal on it. This phenomenon is termed clock gating. We use the ICG cell to stop the clock signal propagation to a big group of logic cells when the group is not required to operate. This is done through a clock enable signal generated internally in the block and applied to the EN pin of the ICG cell. We know that the total power consumption of an SoC is the sum of dynamic power and static power. The clock tree is a major contributor to dynamic power as the clock signal has maximum switching activities. The ICG cell allows to stop the clock signal propagation beyond it and it helps to reduce dynamic power consumption in the design.

Prevention of glitches is one of the qualities of ICG cells. The latch-and gate based ICG cell is good on that front and that’s why this architecture of clock gating circuit is used widely. There are various architectures of ICG cells but we are limiting our discussion to only this architecture in this article.

In the above wave form we can see the glitch free output.