

Tutorial 3: Simulation of Post-Translate, Post-Mapping and Post-Place and Route

This process helps to analyze and understand the timing of the final architecture, and also test if a certain code is being interpreted correctly by the tool. The entire process of transforming a VHDL code into a bitstream for FPGA can be summed up to:

1. Synthesis
2. Implementing
 - (a) Translate
 - (b) Mapping
 - (c) Place and Route

The Xilinx ISE tool can generate simulation code in all 4 process. However the Synthesis output is more difficult to obtain, so I suggest to simulate the Translate process first, and if it works, do the Place and Route. If the design pass both tests, then it is possible to put on the FPGA board for a final test.

The procedure is described here, with some showing figures:

1. Run the Synthesis process for the given architecture.
2. Verify if there are errors and/or warnings, if there are try to understand and correct.
3. Run the Implementing option.
4. Verify if there are errors and/or warnings, if there are try to understand and correct.
5. Open the Translate inside the Implementing, and then run the option to generate the simulation code.
6. Verify if it is okay, then open the Simulation tab.
7. Inside the Simulation tab, change from Behavioral to Post-Translate.
8. Do the simulation and verify if everything went as expected.
9. Repeat steps for Place and Route and then prepare to do it on the FPGA.

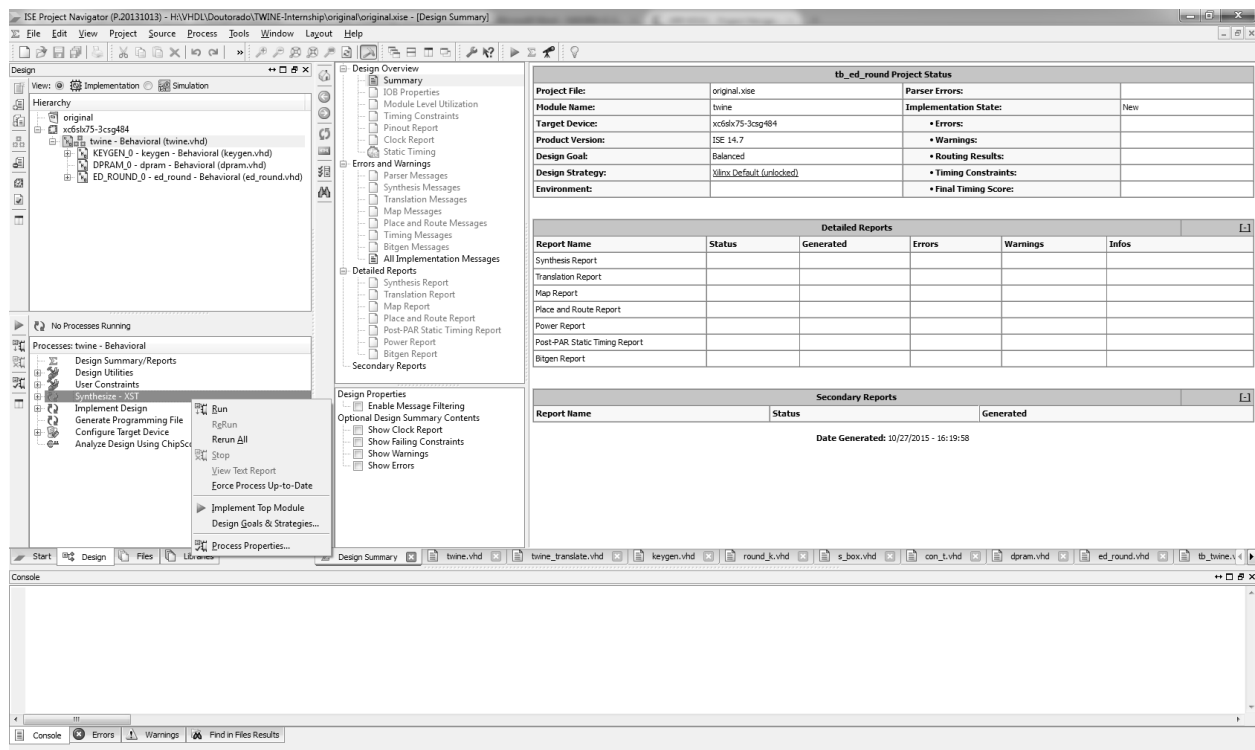


Figure 1: First click on the “Synthesis - XST” option with the right button and then the run option.

The screenshot shows the Xilinx ISE Project Navigator interface. The main window is titled "th_ed_round Project Status (10/27/2015 - 16:23:24)". It displays the following information:

Project File: original_xise
Module Name: twine
Target Device: xc6slx75-3csg484
Product Version: ISE 14.7
Design Goal: Balanced
Design Strategy: Vttrn_Default (Unlocked)
Environment: System Settings

Parser Errors: Synthesized
Implementation State: No Errors
Warnings: 1 Warning (1 new)
Routing Results:
Timing Constraints:
Final Timing Score:

Device Utilization Summary (estimated values)

Logic Utilization	Used	Available	Utilization
Number of Slice Registers	203	93296	0%
Number of Slice LUTs	255	46648	0%
Number of fully used LUT-FF pairs	164	294	55%
Number of bonded IOBs	212	328	64%
Number of Block RAM/PRFQ	1	172	0%
Number of BUFQ/BUFCTRLS	1	16	6%

Detailed Reports

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Tue 27, Oct 16:23:23 2015	0	1 Warning (1 new)	28 Infos (28 new)
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PRR Static Timing Report					
Bitgen Report					

Console

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Minimum period: 4.821ns (Maximum Frequency: 207.437MHz)
Minimum input arrival time before clock: 5.655ns
Maximum output required time after clock: 6.973ns
Maximum combinational path delay: No path found

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Process "Synthesize - XST" completed successfully

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Figure 2: This are the possible output: Green sign = no Warning or Errors, Yellow sign = Only Warnings, Red sign = Errors and/or Warnings.

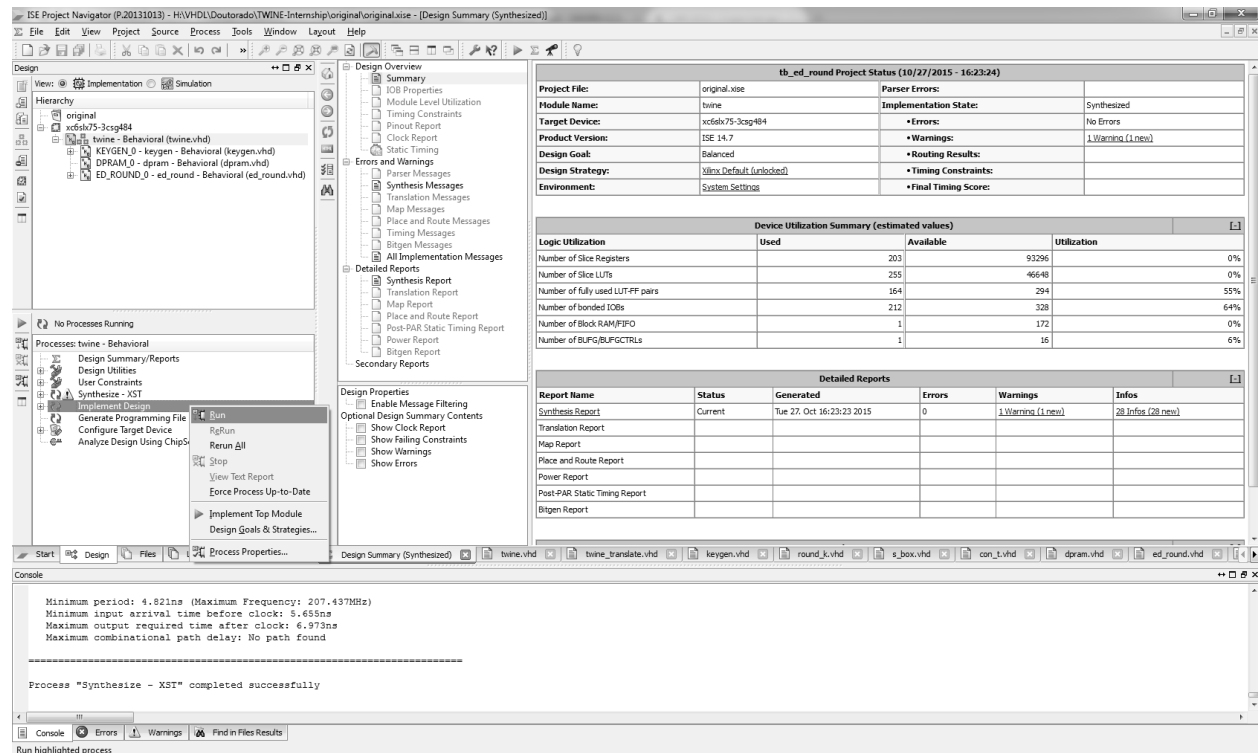


Figure 3: Do the same in the “Implement Design” option.

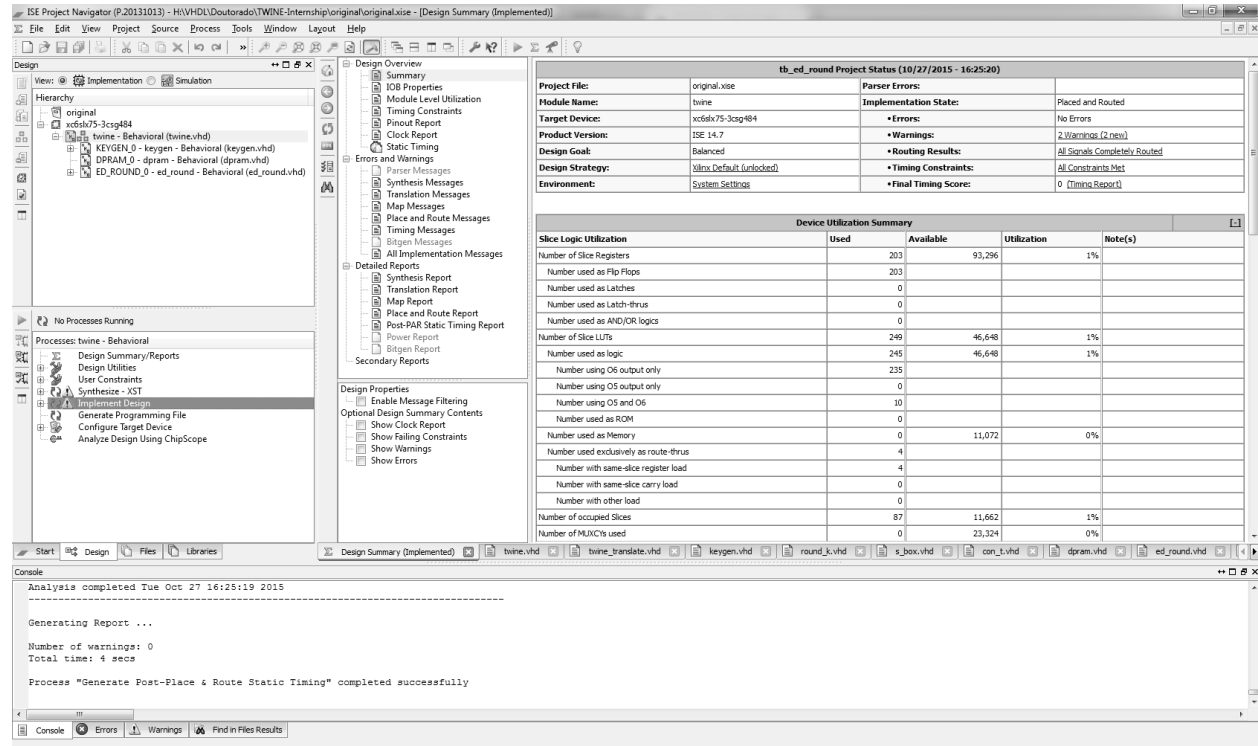


Figure 4: After execution it employs the same sign system as “Synthesis - XST”.

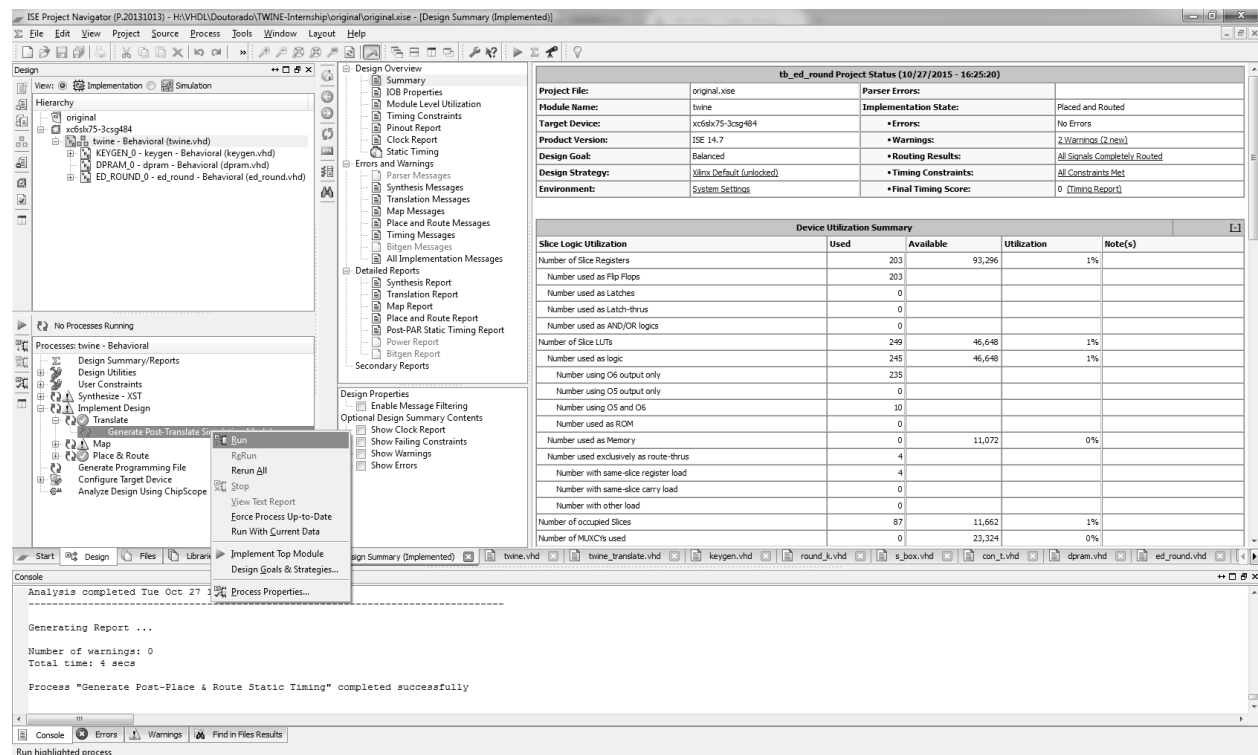


Figure 5: Click on the plus sign at the right of “Implement Design”. It should open 3 options: “Translate”, “Map” and “Place & Route”. Click on “Translate” plus sign and open the option :“Generate Post-Translate Simulation model” and run.

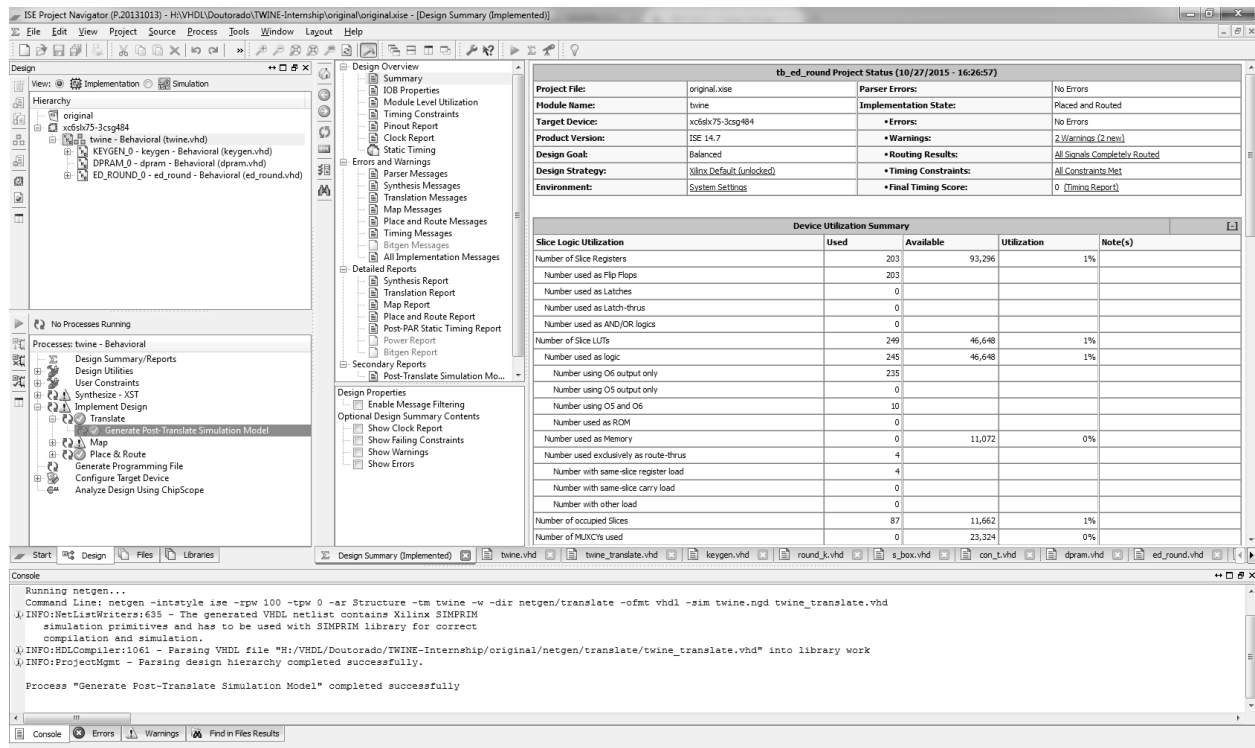


Figure 6: It should give a green sign if everything went okay.

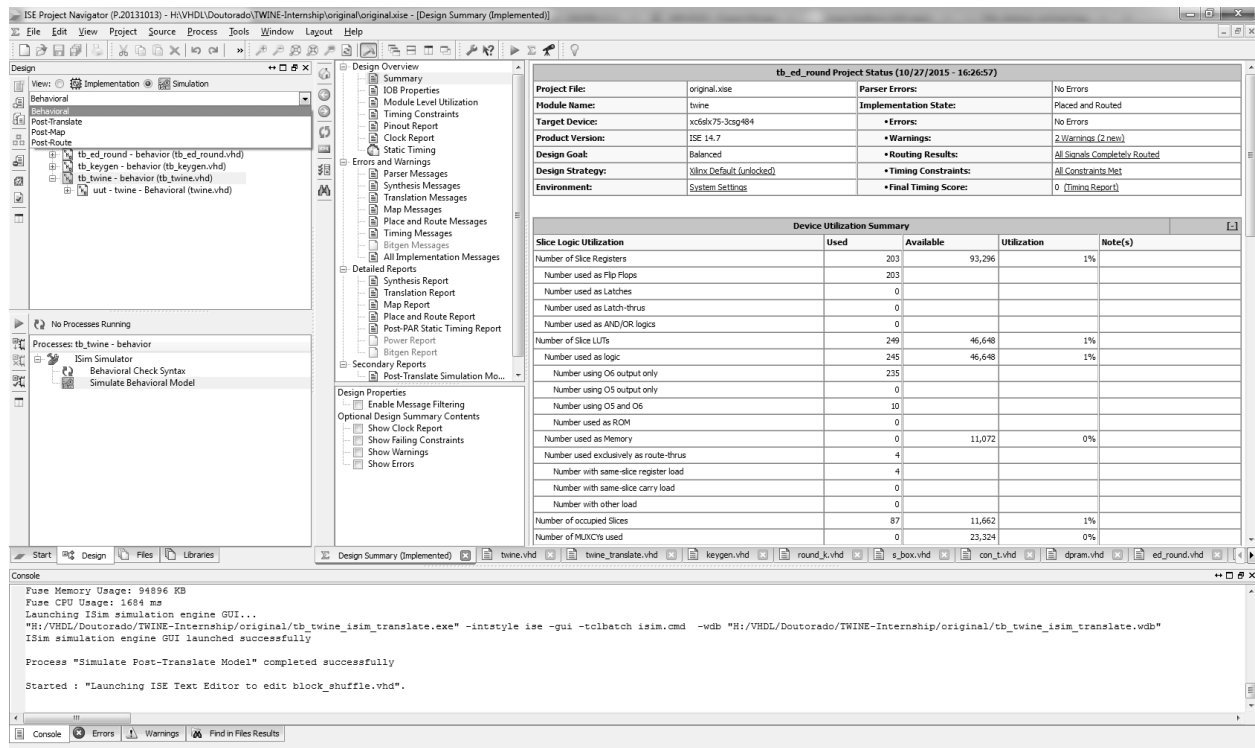


Figure 7: Now on the Simulation tab. Click on the arrow down in the Behavioral model and select “Post-Translate”

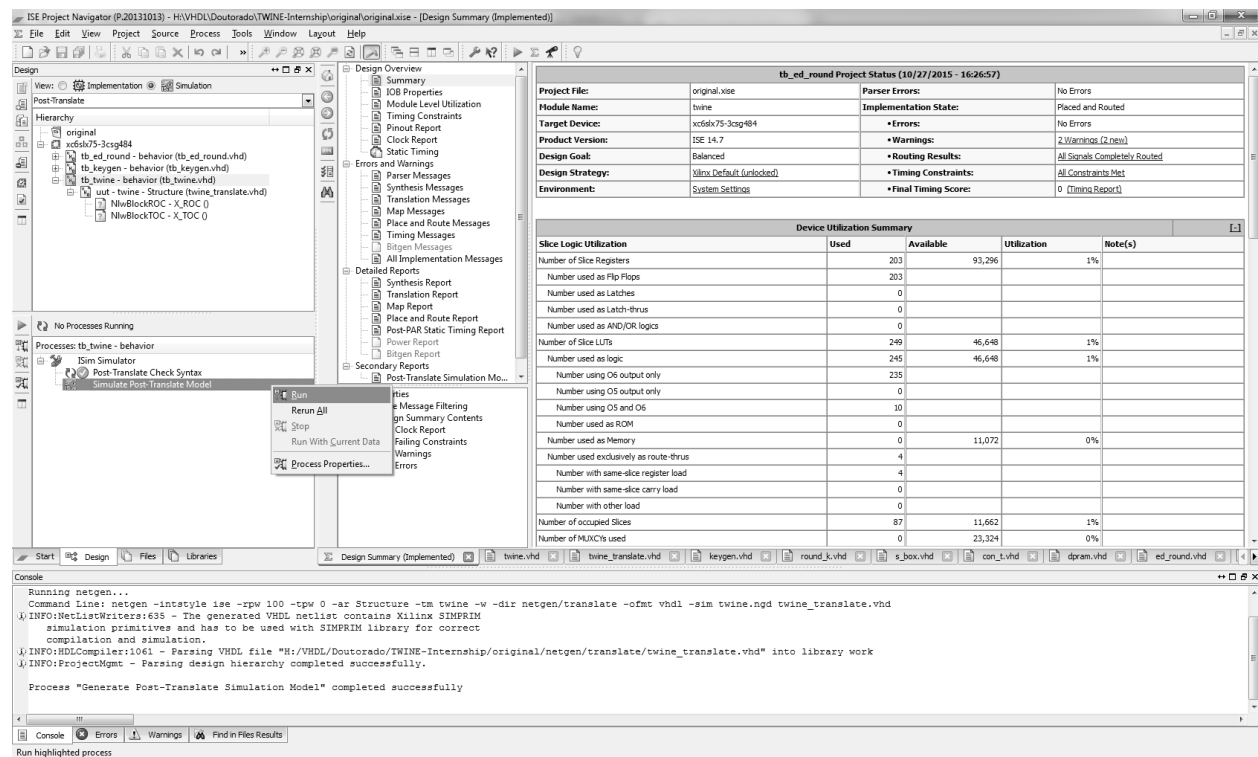


Figure 8: Finally select the respective test bench and begin simulation process by choosing “Simulate Post-Translate Model”.

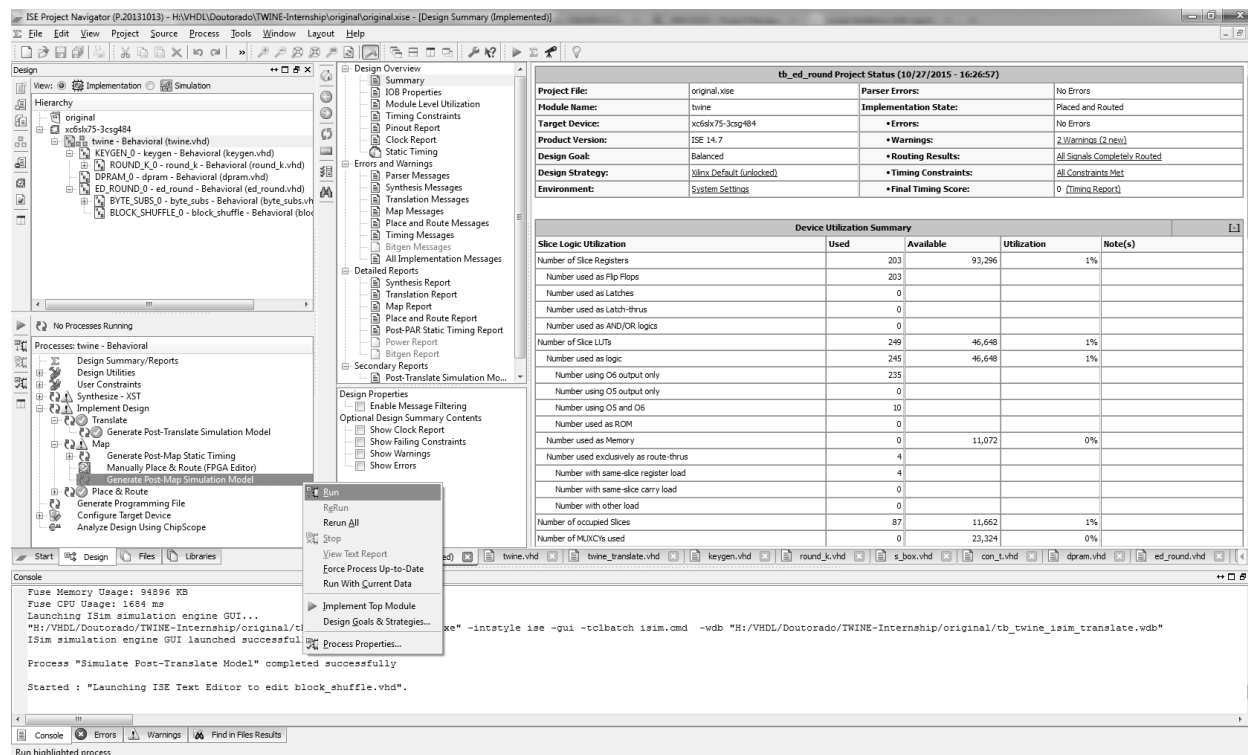


Figure 9: You can do the same process with “Post-Map”.

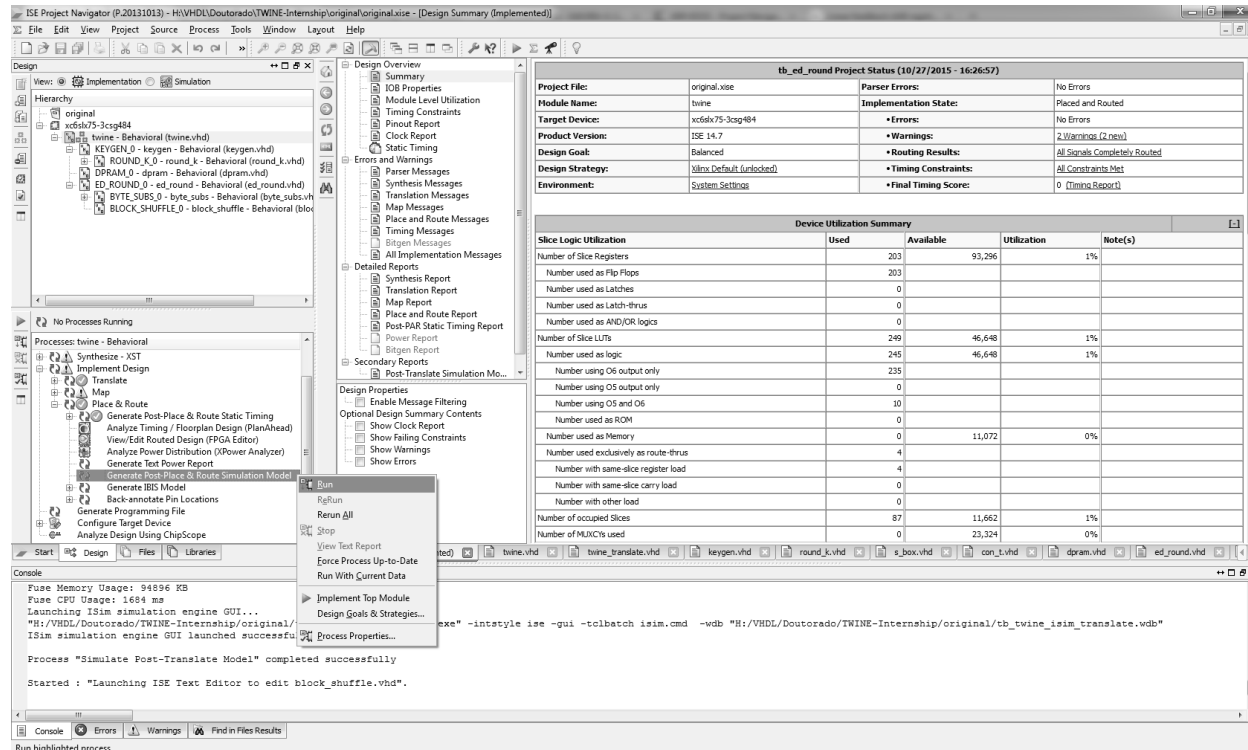


Figure 10: And “Post-Place & Route”.