



## Original Article

# A Review on Electronic Design Automation for Electromagnetic Interference and Signal Integrity of Artificial Intelligence Neuromorphic Chips

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Received March 22, 2022; Accepted March 22, 2022; Published March 22, 2022.

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**Abstract**— The emergence of artificial intelligence has shown a huge promise in solving a wide range of complex problems. However, traditional general-purpose chips based on von Neumann architecture face the "memory wall" problem when applied in artificial intelligence applications. Based on the efficiency of the human brain, many intelligent neuromorphic chips have been proposed to emulate its working mechanism and neuron-synapse structure. With the emergence of spiking-based neuromorphic chips, the computation and energy efficiency could be enhanced by integrating a variety of features inspired by the biological brain. Aligning with the rapid development of neuromorphic chips, it is of great importance to investigate the electromagnetic interference and signal integrity issues in neuromorphic chips for both CMOS-based and memristor-based circuits. Here, we review neuromorphic circuits design, algorithms and applications. With focus on signal integrity issues, modeling, and optimization. Moreover, the heterogeneous structures of neuromorphic circuits and other circuits such as memory arrays, sensors using different integration technologies is also reviewed, and locations where signal integrity might be compromised is exposed. Finally, we provide signal integrity future trends and prospects in neuromorphic devices.

**Keywords**— Signal integrity, Neuromorphic chips, Spiking neural networks, Heterogeneous integration.

## I. Introduction

Artificial intelligence (AI), which was formally proposed at 1956 Dartmouth Conference [1], is a technology that imitates and expands human intelligence and is currently in the third wave of development. The emergence of AI has shown a huge promise in solving a wide range of complex problems ranging from science, finance, security, education, transportation, and logistics, to name a few. In recent years, global digital innovation has revived a new upsurge in AI research and applications. Based on the efficiency of the human brain, which consists of more than  $10^{11}$  neurons and  $10^{15}$  synapses, and consumes only 20 watts, many neuro-inspired computing chips have been proposed to emulate the working mechanism and the neuron-synapse structure of the brain [2]. These neuro-

morphic chips are expected to provide better performances in terms of energy efficiency and computing capabilities when performing AI tasks.

Traditional general-purpose chips mostly use the architecture of computing unit and storage unit separated from each other, namely von Neumann architecture. In such architecture, computing units need to frequently access a large amount of data in the storage unit to perform AI operations based on big data, of which the operation speed is often limited by the memory read and write speed, resulting in a "memory wall" [3]. Hence, the computation and storage demand of these complex algorithms exceed the capabilities of central processing unit (CPU)-based platforms. On the other hand, graphical processing unit (GPU), field programmable

gate array (FPGA) and application specific integrated circuit (ASIC) demonstrated superior capabilities in many areas. However, they face serious challenges due to the conventional von Neumann architecture. Especially, in typical sensor-rich designs (such as autonomous vehicles, robotics, and wearable electronics) and low-delay requirement designs (such as real time applications). Therefore, the research and development of neuromorphic chips has become the research focus and future layout of more and more leading scientific research institutions and companies in the world.

Most of the existing neuromorphic chips aim at accelerating AI algorithms, however, only partially realize the biological characteristics of the human brain neural network [4]. In order to further improve the computational efficiency of neuromorphic chips and reduce power consumption, it will be necessary to more deeply imitate the behavior of human brain neural networks in the future, including the imitation of human brain neural signals and neural network architecture. Spiking neural networks (SNNs), which are considered as the third generation of neural network [5], take further steps in emulating the human brain by using spikes to exchange the information between neurons, and adapting neurons to work on event-driven networks i.e., when potential of a neuron reaches a threshold, it emits a spike, while other neurons remain idle. This concept of spatio-temporal event representation contributes to energy efficiency in SNN-based applications, based on which there have been preliminary explorations in hardware implementation, that is, spiking neuromorphic chips [6]. Spiking neuromorphic chips have the characteristics of low power consumption, low latency, high-speed processing, and space-time integration. It represents a promising long-term development direction of the neuromorphic chip.

With the future direction for high-speed circuits, and the development of spiking-based neuromorphic chips, electromagnetic interference (EMI) and signal integrity (SI) issues such as crosstalk and noise pose a great challenge in the early stage of circuit. This will promote the development of neuromorphic chips towards high speed, high integration and high intelligence, which has important scientific value and industrial application prospect. To the best of our knowledge, this is the first work to address and summary the SI issues in neuromorphic chips. Moreover, neuromorphic chips based on emergent devices such as memristor are also considered.

The remaining of this paper is organized as follows: Section 2 reviews the circuits design and applications of neuromorphic chips while Section 3 illustrates the EMI and SI issues in neuromorphic chips based on CMOS and memristor devices. Section 4 explains the design of different heterogeneous integration structures of neuromorphic and other chips and analyzes the SI issues. In Section 5, we discuss various techniques for SI improvement and optimization. Finally, this paper is concluded in Section 6.

## II. Review of Neuromorphic Circuits Design and Application

To ensure that the functional chip can still work properly in a complex electromagnetic environment, its immunity to SI and electromagnetic interference (EMI) issues are essential indicators [7–9]. Due to the unique hardware architecture and bionic design concept, the neuromorphic chip is considered to have high parallelism, low power consumption, and robustness, making it also an emerging technology of interest in the future of computing [10]. While von Neumann computers encode information as numerical values represented by binary values, neuromorphic chips use spike sequences as input and output. Much work has been done to optimize the hardware architecture of neuromorphic chips with different designs to fit their characteristics better [11–14]. Here, we briefly review the design aspects of large-scale neuromorphic chips and RRAM devices, and its computation algorithms and applications. Moreover, we highlight the potential advantages of neuromorphic chips in different applications.

### 1. Circuit Design

The realization of neuromorphic chips can be achieved through digital implementation, or mixed analog-digital implementation. The effort of neuromorphic hardware design was initiated by many research institutions, followed by partnerships with the industry as shown in Fig. 1. University of Manchester came up with a purely digital neuromorphic chip called SpiNNaker [15] with two versions (SpiNNaker and SpiNNaker2). Similarly, Zhejiang University and Zhejiang Lab developed Darwin Neuromorphic Processing Unit (NPU) [12], a digital chip with an off-chip memory to store synapse information. IBM and Intel also developed two digital neuromorphic chips known as TrueNorth [16] and Loihi [17], respectively. Stanford University's Neurogrid [18] and Braindrop [19] are examples of mixed-analog-digital system and the neurons are designed using analog circuits. Another mixed-analog-digital design is BrainScaleS [20], from University of Heidelberg and Technische Universitat Dresden. In 2019, Tsinghua University introduced a cross-paradigm neuromorphic digital chip called Tianjic, which integrates artificial neural network (ANN) and SNN into hybrid neural networks (HNNs) [4].

Resistive random-access memory (RRAM) devices have experienced fast development in the last two decades. As can be seen from Fig. 2, RRAM is first proposed in 2008 as the missing fundamental element in Berkeley[**References**]. Then, many researchers attempted to fabricate real RRAM devices as well as developing underlying physical principal. From 2016 to 2020, large companies such as IBM, Intel and foundry like TSMC start to tape out some RRAM samples compatible with CMOS process node. At the same time, many researchers start to develop RRAM Macro [21] and system integration. During the past two years, 3-dimension inte-

gration of 3D-RRAM [22], programmable RRAM chip and SoC [23, 24] with RRAM are taped out with impressive energy and area efficiency. Some start-ups also announced to release their commercial products based on RRAM at the end of 2023. The trend of the future five years development of RRAM chips may focus on related tool chain and compilers, efficient soc design as well as 3D integration compatibility. Fig. 3 shows typical neuromorphic chips layout and their architectures.

## 2. Algorithm and Applications

**Neural Coding** Fig.4 describes the key attributes of biological and silicon-based computing frameworks [29]. As mentioned earlier, using spike sequences as input and output is an essential feature of neuromorphic computation. Therefore, implementing a numerical-to-pulse sequence encoder and decoder is a fundamental module for deploying neuromorphic algorithms to a given task. There are two mainstream ways to encode spikes: rate encoding, which carries information through the frequency of spike issuance within a certain length of the time window, and temporal encoding, which describes the time point of spike issuance [30]. One of literature's most widely used frequency coding methods is Poisson coding, which encodes the normalized numerical information as a spike sequence with the number of spike releases conforming to the Poisson process. Due to the concept of randomness inherent in such encoders, when noise affects a single spike, the whole computing system has a natural robustness advantage. A typical approach to temporal coding would be to characterize the information using the exact moment when the spikes are issued in a time window. In addition, various coding methods, such as differential and phase coding, have been further proposed to improve the encoder's performance by incorporating communication modulation theory.

The decoding method of spikes generally corresponds to the encoding method, for example, by counting the spike delivery rate over some time to obtain the rate encoding information or by locating the exact time of spike delivery to restore the original information of the temporal encoding. However, it is also worth mentioning that in practical application scenarios, the neuromorphic chip may receive spike input directly, for example, when a dynamic vision sensor is used as signal input instead of a conventional optical camera [31, 32]. In this case, the spike signal contains more spatio-temporal information, and the decoder needs to be further discussed and selected in combination with the neuromorphic computing algorithm used.

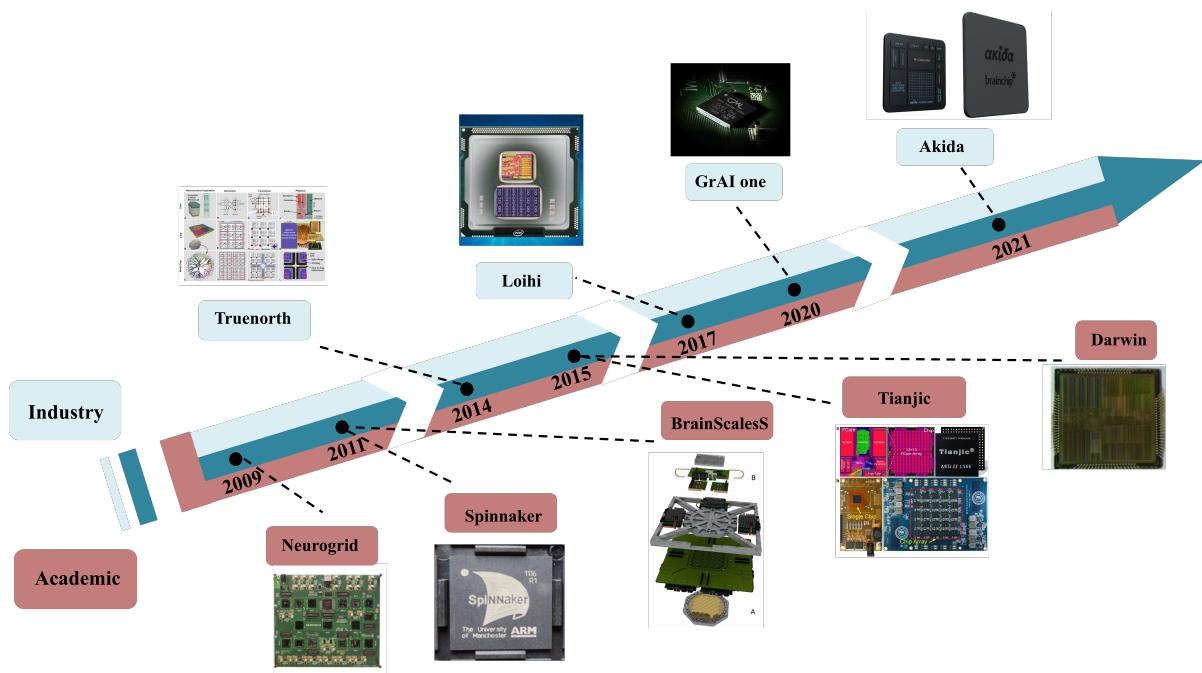
The low power consumption characteristics of the neuromorphic chip are also related to its use of spike sequences as data streams. Similar to how the human brain works, the event-driven nature allows the circuitry of the neuromorphic chip to be silent most of the time due to not receiving new spikes from the previous synapses. In addition, due to the duality of the spikes, the corresponding neural computation al-

gorithm reduces a large number of multiplication operations, which can further reduce the computational overhead. The low-power effects also make the neuromorphic chip expected to mitigate EMI problems better.

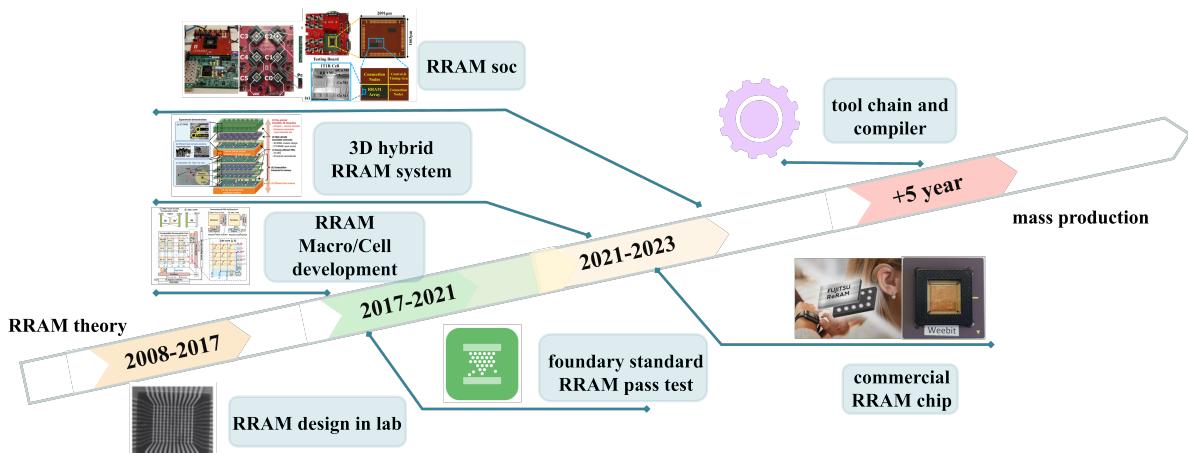
**Neuronal Dynamics** In recent years, the development of machine learning, especially ANNs, and the landing of many applications are important reasons for the surge in demand for chip computing power. For the application of the natural language processing model, the parameter quantity of the neural network model has reached 100 billion [33]. Another more serious challenge is how to train such a large-scale neural network. Even after addressing the equipment requirements and energy overhead required for training, there is still a need to ensure good parallelism among thousands of GPUs to enable the load to be efficient and scalable at both the memory and compute levels.

Research in the field of neuromorphic computing is expected to be inspired by the human brain to develop next-generation computers. The mainstream algorithmic framework in neuromorphic computing is the SNNs, which originated from the theoretical foundation of neuroscience and is also called the third generation of neural networks [34]. Fig. 5 shows some similarities and differences between ANN and SNN when simulating biological neurons. Compared with ANN, SNN uses a spike encoder and decoder at the input and output ends. Its internal computing unit is modeled on the neuron structure and reproduces the unique neuronal dynamics. When dealing with the complex relationship between input and output, ANN neurons are nonlinear fitting with the help of activation functions such as ReLU. At the same time, SNN is based on biological neurology and introduces dynamic characteristics such as membrane potential accumulation, leakage, and fire. The neuronal dynamics of SNN is also an adaptive result because the information density of the spike data stream is not as high as that of ANN, so it is usually necessary to rearrange and analyze the spike sequences within a certain time window to achieve similar functions [35]. In addition, it is precisely this neuron dynamics that makes the activity of each neuron depend on its membrane potential and spike fire rules, so the whole network is well parallelized in its deployment. At the same time, each neuron has its unit to store the state of the membrane potential, thus presenting a storage and computational integration throughout the computational model to break the computational performance bottleneck.

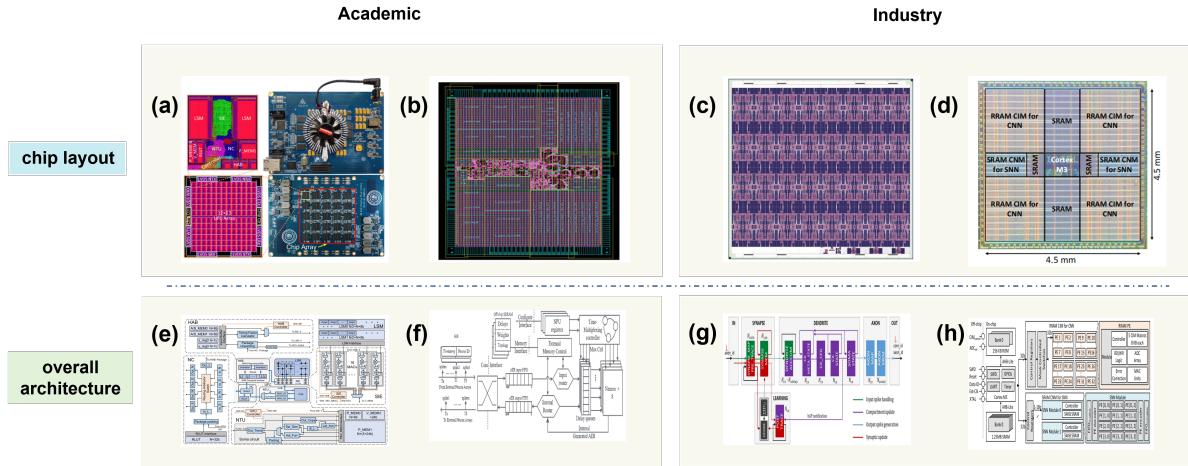
There are various neural dynamics of SNNs currently available, ranging from the simpler integrate-and-fire model (IF) and leaky-integrate-and-fired (LIF) model to the more complex Hodgkin-Huxley (HH) models from biology [11, 12]. However, considering the hardware deployment of SNNs, discrete equations are generally used to describe the spiking neurons. Combining a variety of neuronal dynamics



**Figure 1** During the last four decades of the neuromorphic field, several neuromorphic chips have been developed. Popular large-scale neuromorphic chips and their first reported years: as early as 2009, Stanford University released Neurogrid [18] neuromorphic chip. In 2011, the first versions of Spinnaker [15] and BrainScaleS [25] were released for the first time by University of Manchester and Heidelberg University, respectively. In 2014, IBM released its neuromorphic chip, TrueNorth, which has 4096 neurosynaptic cores, with 1 million neurons and 256 million synapses [11]. A year later in 2015, the first generation of Tianjic chip, which was the first hybrid chip that can use both ANN and SNN, was developed by Tsinghua University [4]. At the same year, the first generation of Darwin NPU was developed by Zhejiang university and Zhejiang Lab [12]. In 2017, Intel Labs developed first generation of Loihi chips with 130 thousand neurons and 130 million synapses [17]. In 2020, GrAI Matter Labs presented GrAIOne chip [26] that is capable of accelerating both ANN and SNN. BrainChip's Akida is the first commercial neuromorphic chip in 2021 [27].



**Figure 2** RRAM devices development in a nutshell: in 2008, first RRAM was proposed. From 2017 - 2021, many companies started to RRAM devices compatible with the CMOS technology [21]. Recently, 3D-RRAM found was realized which improved the energy and energy efficiency dramatically [22]. In the next few years, the focus is expected to be on the related tool chain and compilers, efficient soc design as well as 3D integration compatibility.



**Figure 3** Typical neuromorphic chips by academic and industrial communities. (a)(e) Tianjic neuromorphic chip for SNN/DNN workload;(b)(f) Darwin neuromorphic chip.(c)(g) Intel's Loihi for SNN and (d)(h) ReRAM/SRAM hybrid CIM for SNN/DNN by TSMC[28].

models, the description of a typical neuron mainly includes three behaviors of accumulation, fire, and reset, which correspond to the following three equations

$$H(t) = f(V(t-1), X(t)) \quad (1)$$

$$S(t) = \theta(H(t) - V_{th}) \quad (2)$$

$$V(t) = H(t).(1 - S(t) + V_{reset}.S(t)) \quad (3)$$

where  $t$  is the time stamp,  $V(t)$  and  $V(t-1)$  represent the membrane potential at the current and last time, respectively, which are the most important hidden variables in neuronal dynamics.  $X(t)$  represents the input at the current moment, which is generally the potential increment caused by presynaptic.  $H(t)$  represents the instantaneous membrane potential before the spike is released at the current moment.  $V_{th}$  represents the threshold potential of the neuron. Here, the step function  $\theta$  is used to indicate whether the current spike sends out the spike signal  $S(t)$ . The two main differences between neuronal dynamics are the state update equation  $f$  and the reset of neurons. Currently more widely used in neuromorphic computing are LIF neurons, whose discrete form of neuron state update equation is described as:

$$f(V(t-1), X(t)) = V(t-1) + \frac{1}{\tau_m}(-(V(t-1)) - V_{reset}) + X(t) \quad (4)$$

where  $\tau_m$  is the time constant describing the decay of the membrane potential, also known as the discount factor.

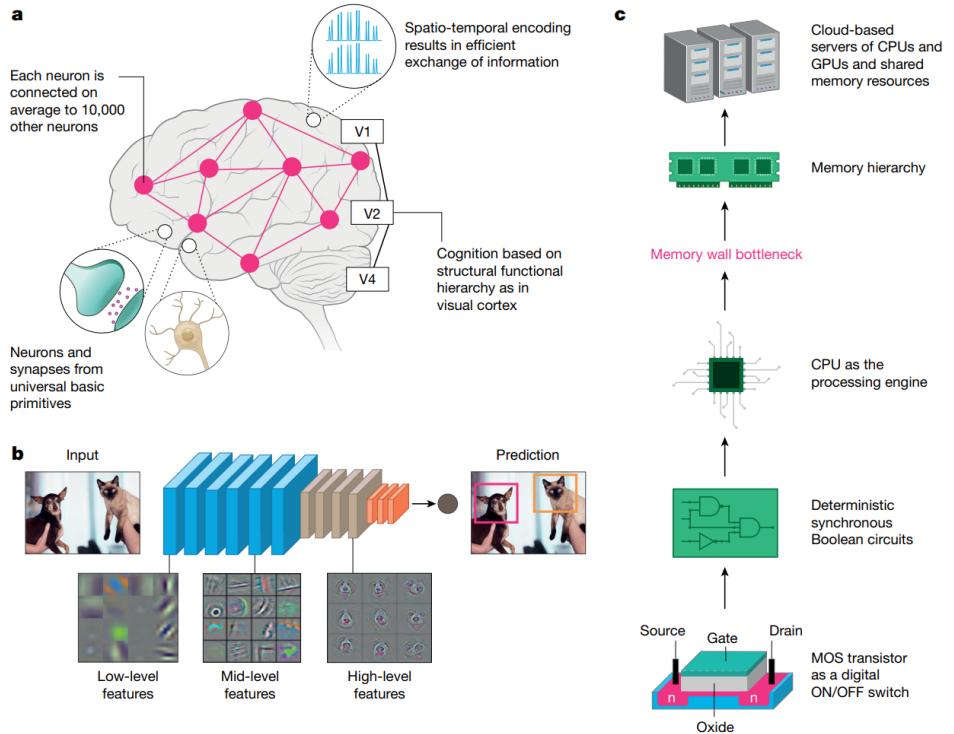
LIF neurons are relatively simple, but their neuronal dynamics still have reasonable biological plausibility and have been proven to perform well in most computing task scenarios.

Due to the presence of neuronal dynamics, the behavior of neurons is continuously influenced by a certain time window. Therefore, neuromorphic computing presents better ro-

bustness to transient disturbances when deployed for applications. In addition, some studies have combined anatomical studies of biological neurons to enhance the ability of neurons to integrate temporal spikes and thus maintain a more stable performance by introducing mechanisms such as adaptive release thresholds [35, 36]. Neuronal dynamics of SNNs are evolving under the influence of both computational applications and bionic inspiration.

**SNN learning** An essential application of neuromorphic computing is to solve deep learning tasks. Fig. 6 illustrates the timeline of major discoveries and advances in intelligent computing, from the 1940s to the present [29]. For decades, ANNs have achieved outstanding results in natural language processing, image processing, robot control, and many other fields. Although SNNs can theoretically achieve the exact fitting of nonlinear systems as ANNs by introducing impulse codes and neuronal dynamics, their practical performance needs further discussion.

A deep neural network requires inference and, more importantly, a well-developed training method. ANNs currently adjust network parameters based on gradient information by building loss functions and performing backpropagation of errors. However, since SNNs propagate data through impulse signals based on neuronal dynamics, it is challenging to learn similarly from gradient information. Therefore, a common practice is to guarantee training through custom backward gradient propagation rules, also referred to as surrogate gradients [37]. However, surrogate gradients are relatively ambiguous, and thus the ultimate performance of SNNs becomes challenging to surpass that of ANNs with such training methods. Recent research advances have focused very much on training methods for SNNs, including synthetic gradients or three-factor learning from a biological perspective [38–40].



**Figure 4** Key attributes of biological and silicon-based computing frameworks [29]. (a) A schematic of the organizational principles of the brain. (b) A deep convolutional neural network performing objection detection on an image. (c) A state-of-the-art silicon computing ecosystem.

In addition, due to the nature of neuromorphic computing chip storage and computation, some research focusing on hardware-friendly on-chip training methods, such as e-prop, also has good application prospects [41–43].

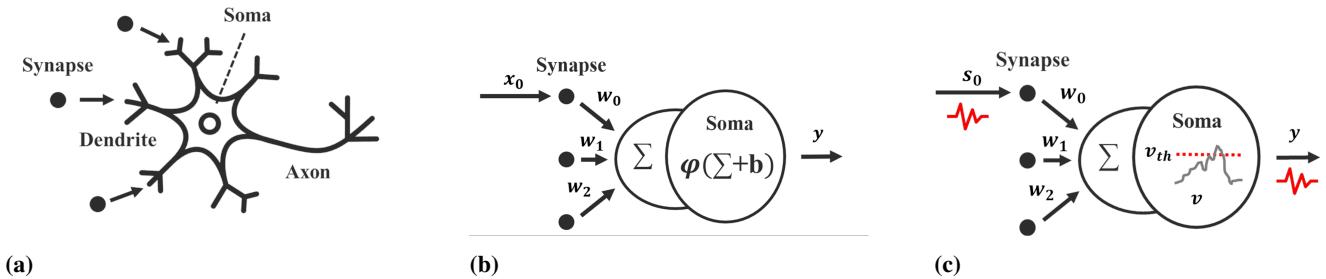
Although there are some challenges in the training of SNNs, given the unique advantages of neuromorphic computing and its hardware, deploying SNN to replace ANN to achieve some more complex tasks is still a very promising application. Thus, another important field for SNNs is the desire to establish their relationship with well-trained ANNs. The transformation method focuses on converting an ANN whose parameters have been trained into an effective SNN that can be deployed on a neuromorphic chip [44, 45]. Through the transformation method, ANN training techniques are also applied, thus avoiding the training problem of deeper SNNs, and these SNNs obtained by the transformation method also show higher performance than the direct training method in many task scenarios.

However, since one of the starting points of the transformation method is the statistical approximation of the spike, the SNNs obtained from the transformation often use frequency encoding and require a relatively long-time window, which increases the computational latency to some extent [46]. Subsequent studies include combining the conversion method with the direct training method, which effectively

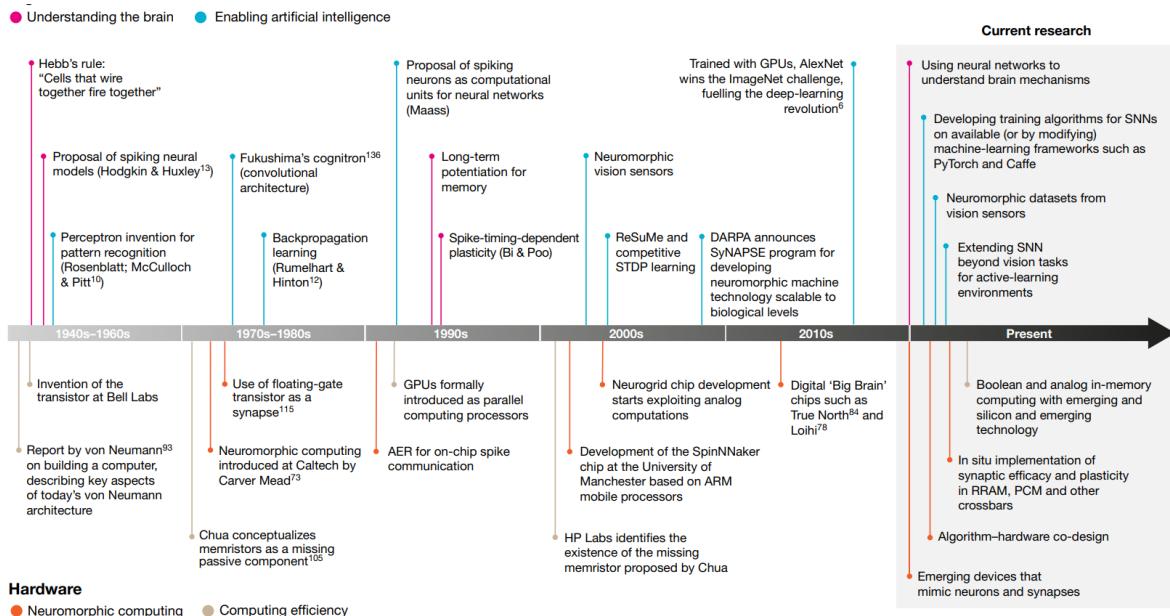
shortens the time window and achieves a good performance [47]. Since task accuracy is the most concerned metric, this series of techniques based on the conversion method, linking SNN with ANN, is the mainstream and the focus of the research field in the near future.

**Application Scenario** Due to their respective strengths, ANN and SNN will be positioned in different deep learning application scenarios [48]. Specifically, ANN is highly abstract in its description of neural systems and shows better accuracy and performance in deep learning. However, due to the memory wall problem of von Neumann architecture, its power and cost are higher, so it is more suitable for cloud and strong edge-end application scenarios. On the other hand, SNN is a more bionic description of the neural system, which has the advantage of relatively lower power and cost and better robustness and thus has great potential in edge computing.

In addition, ANN is more adept at static data pair processing, while SNN processes dynamic information due to neuronal dynamics. For example, ANN is considered relatively more suitable for image and video processing applications, while SNN has unique advantages in areas such as detection and control. Therefore, ANN and SNN will continue to be developed in the near future and are not a substitute for each other. In addition to the division of labor between ANN



**Figure 5** (a) Schematic diagram of biological neuron. (b) Schematic diagram of ANN neuron. (c) Schematic diagram of SNN neuron.



**Figure 6** Timeline of major discoveries and advances in intelligent computing, from the 1940s to the present [29]

and SNN from cloud to edge, combining their advantages in the same task also requires continuous research and breakthroughs in algorithms and hardware.

### III. Electromagnetic Interference and Signal Integrity in Neuromorphic Chips

The advantage of the working mechanism of the human brain neural network lies in the low-frequency spike signals and low power consumption. Correspondingly, the neuromorphic chips that have been manufactured so far all adopt low-frequency transmission signals. However, as the development of neuromorphic chip, the frequency of the transmission signals tends to be higher and higher. And the neuromorphic chip is supposed to operate in complex electromagnetic environment. It is necessary to conduct research about signal integrity theory of the neuromorphic chip in advance because it has non-von Neumann architecture with novel neurological devices whose SI analysis methods should be different from

traditional semiconductor chip.

There are roughly two kinds of neuromorphic chips: neuromorphic chips based on CMOS technology, and neuromorphic chips based on memristors. This section mainly focuses on the SI analysis of the memristor-based neuromorphic crossbar array because its circuit structure deeply imitates the neural network of human brain and is totally different from traditional CMOS-based chip. The SI analysis of the crossbar array is considered to be more unique and challenging.

#### 1. EMI and SI in CMOS-based Neuromorphic Chips

Similar with traditional chips, CMOS-based neuromorphic chips suffer from lots of SI issues, including crosstalk reflection, impedance mismatch, inter-board resonance, etc. The SI problems of CMOS-based neuromorphic chips can be mainly attributed to the following aspects: 1) The steep rising edge of the signal leads to the excessively high working frequency, which leads to the transmission line effect such as reflection,

crosstalk and dispersion; 2) The reduced chip operating voltage makes the signal easy to be interfered, resulting in the higher bit error rate; 3) The higher system integration and narrowed wiring distance cause serious parasitic effects of interconnection and packaging, signal crosstalk intensification, etc. The key research of SI in CMOS-based Neuromorphic Chips is to clarify various factors affecting signal performance and adopt a series of measures to solve or suppress them, so that the received signals can maintain corresponding characteristics in time domain and frequency domain.

## 2. EMI and SI in Memristor-based Neuromorphic Chips

Memristor-based neuromorphic crossbar array as shown in Fig.7 occupies a smaller area with lower power consumption compared with neuromorphic hardware based on traditional devices. However, the reliability of neuromorphic crossbar array is still poor due to unstable device performance, special circuit structure, and high integration. Fig.8 describes several typical EMI and SI in memristor-based neuromorphic chips, e.g. crosstalk, sneak path, etc. At present, the EMI and SI issues of crossbar array that have been widely concerned and explored can be roughly divided into two parts [49–54]: one is the impact of variation and non-linearity of memristor at the device level, the other is the parasitic effects caused by interconnect at the circuit level.

The emerging memristor [56, 57] is believed to be an excellent alternative for the artificial synapse. It can achieve the weight update process in the neural network with the resistive switching behavior. The variability of the memristor performance is a major barrier to manufacture large-scale crossbar array. Like other nano devices, it suffers from process variations (device to device) which may cause non-linear effects in the resistance adjustment region. Further, it also suffers from temporal variations (cycle to cycle) caused by the stochastic intrinsic characteristics of memristor switching dynamics.

The most commonly used memristor array architecture in neuromorphic hardware is the one-transistor and one-resistor (1T1R) array. Transistors in series with memristors make it easier to design neuromorphic chip. Firstly, the transistor gate voltage sets the current compliance so that it can suppress the overshoot and feedback effects. Secondly, the transistor size is much larger than the memristor which provides a good isolation between cells and minimizes the crosstalk issue. Thirdly, the transistor also helps eliminate the sneak path in the large-scale memristor array.

The 1T1R array has good performance and reliability, but the transistor occupies too much area. To achieve higher integration density, the transistor can be replaced by a two-terminal selector (1S1R) or be removed from the array (1R). However, higher density can cause severe electromagnetic problems, so it is more difficult to design a large-scale neuromorphic circuit based on 1S1R or 1R [58] structure than 1T1R structure. The crossbar (1R) array, shown in Fig. ??, will be further illustrated in this section.

When the wire width is of nanoscale, the effects of interconnect capacitance and inductance can be ignored and there are two typical signal integrity problems of the crossbar array: IR-drop and sneak-path problems. IR-drop is caused by interconnect resistance. For a large array, the interconnect resistance is comparable to the memristor resistance so that the write voltage will drop on the wire. Besides, the sneak-path problem happens in the read process of the crossbar array is shown in Fig. ???. When a memristor cell is selected in the array, the other cells on the same row and column are also half-selected. So there will be sneak-path currents through those half-selected cells and the read-out current will be higher than the ideal current.

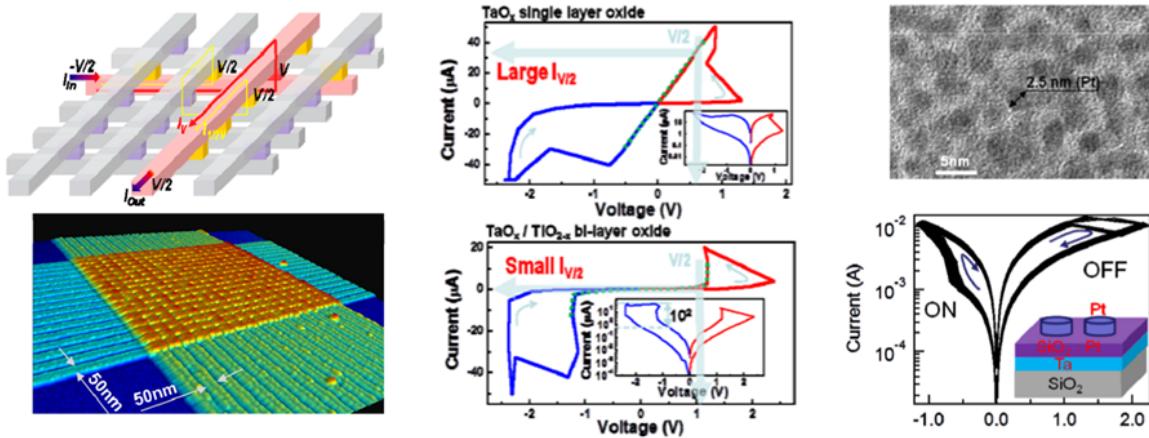
When the wire width is larger and of micron-scale, the influence of interconnect resistance decreases and the parasitic effects in the crossbar array are mainly caused by interconnect inductance and capacitance. The parasitic effects involve voltage degradation, time delay, overshoot, crosstalk and coupling which may have a strong influence on the performance of the neuromorphic chip.

## 3. EMI and SI Modeling Methods for Neuromorphic Chips

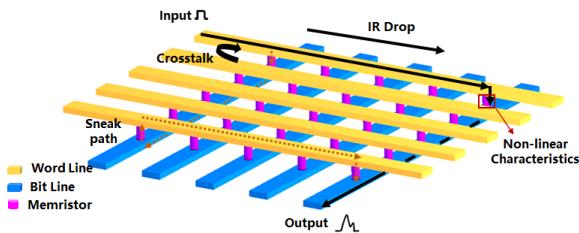
Accurate circuit modeling of crossbar array is the foundation of signal integrity analysis. The crossbar model consists of the memristor model and the interconnect model.

Weber distribution is commonly used for statistical analysis [59, 60], but this kind of method does not consider the continuity and high dependence of the random process of memristors. Kinetic Monte-Carlo (KMC) is a powerful method for the numerical modeling of memristor's intrinsic stochastic switching process [61–63]. It can physically describe the forming and rupturing process of the conductive filaments in the memristor. Time series statistical analysis method is also proposed to predict and model the randomness of memristors under continuous periods [64, 65]. However, these methods are very computationally complex and is not suitable for large-scale crossbar array simulation. The compact memristor models for spice simulation have received more attention [66–70]. The formation and rupture of the conductive filaments are described by simplified mechanisms.

The crossbar array is usually divided into unit cells for modeling because it has a periodic structure. If the crossbar array is of nanoscale, the interconnect wire is simply modeled as resistance. Otherwise, the parasitic inductance and capacitance should also be considered [71–77]. Commercial software (e.g. ANSYS Q3D Extractor) can be utilized to extract these parasitic parameters for crossbar array circuits [73]. Meanwhile, calculating parasitic inductance and capacitance by numerical method can be treated as an alternative method for fast analysis. Partial element equivalent circuit (PEEC) method is one of the most common numerical calculation method to analysis parasitic effects of interconnect wires [71, 77]. Fig. 9 illustrates the circuit model of the unit



**Figure 7** An example of memristor based neuromorphic chip [55]



**Figure 8** EMI and SI issues in memristor-based neuromorphic chips

cell of crossbar array including parasitic inductance, capacitance and resistance [71]. Because the neural network is realized in time domain, only time-domain simulation of the crossbar array is discussed. The whole circuit simulation can be conducted in SPICE simulators, but it is not convenient to simulate a large-scale crossbar array or to implement neural network simulation on the crossbar array. So it is more recommended to conduct simulations by solving circuit matrix functions in programming software such as Matlab or Python in which array size and time loop can be easily modified.

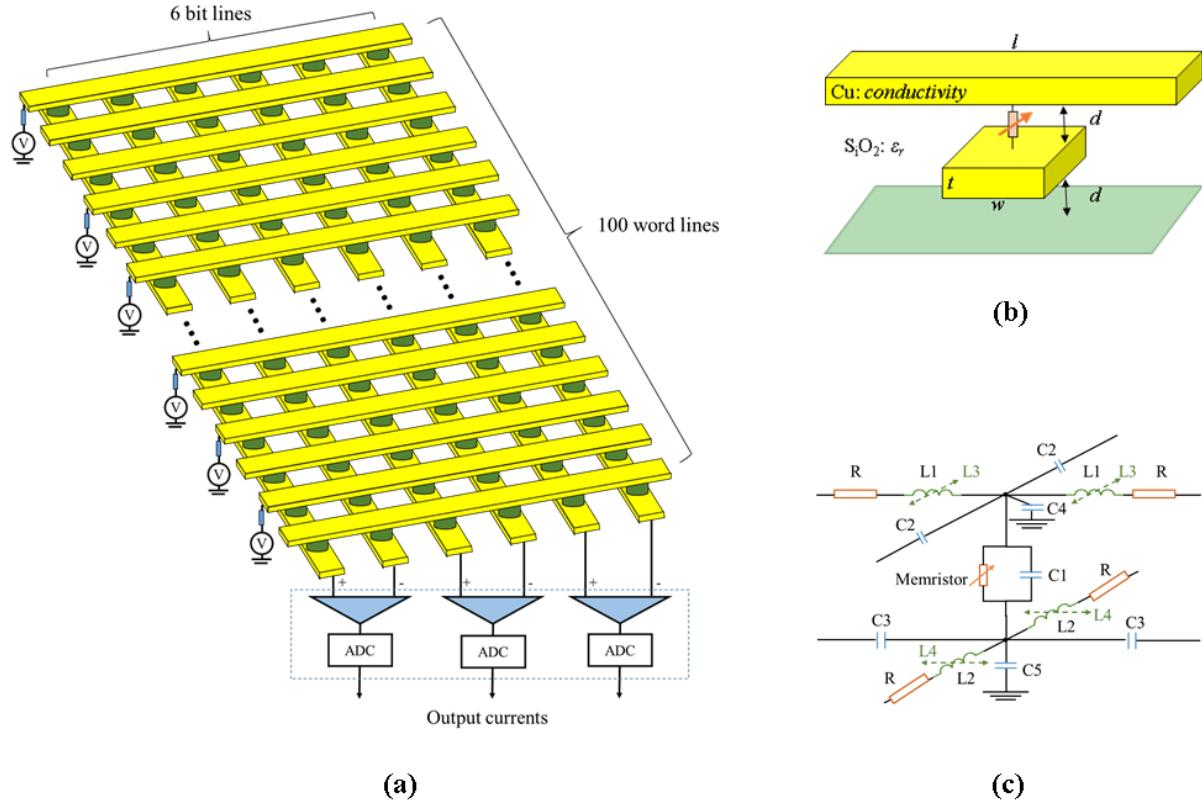
#### IV. Electromagnetic Interference and Signal Integrity in Heterogeneous Neuromorphic Structures

The term heterogeneous integration (HI) originally was used to describe the integration of multi-functional chips in the same location [78]. HI allows stacking of dissimilar components with different feature size, functions, materials, and foundries. This gives an advantage over other technologies such as system-on-chip (SoC). HI can be achieved through different techniques such as 2D, 2.5D and 3D or other packaging technologies.

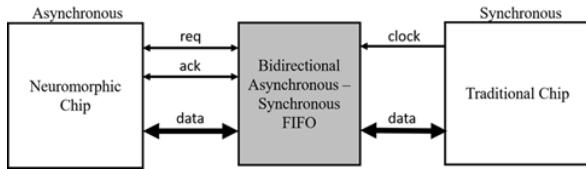
The asynchronous nature of neuromorphic chips benefits real-time and event-based sensory processing, featur-

ing low power and latency. In terms of signal processing, the event-driven architecture uses asynchronous design for inter/intra-chip networking [16, 17]. However, clock-domain crossing is inevitable when dealing with synchronous circuit within the neuromorphic chip as in [16, 79], where the neuron computation unit is implemented in a synchronous design style. In such cases, asynchronous-synchronous interface [80] is required to translate the asynchronous signal to synchronous signal and vice-versa. A bidirectional interface between asynchronous and synchronous domains is also required when neuromorphic chip is integrated with traditional chip based on synchronous designs as shown in Fig. 10. Heterogeneous integration between neuromorphic circuits and sensors could be achieved using address event representation (AER) as in [81], where neuromorphic binaural auditory sensor was implemented using FPGA. Similarly, motion detection (MD) vision sensor using processing-in-sensor technique yielding high-frame-rate and low-power consumption [82]. In this type of interface, the analogue auditory and visual signals are converted into event-based spikes using spike coding schemes, and then sent to the AER bus.

The HI of neuromorphic circuits and other elements such as memory arrays and sensors were achieved through different packaging technologies. For instance, a CMOS image sensor (CIS) and CMOS neurons were fabricated in a single  $0.18 - \mu\text{m}$  process chip [83], and the chip was integrated with memristor array through printed circuit board (PCB) packaging technology, as shown in Fig. 11a. Although PCB was successful in integrating neuromorphic and sensor circuits, its relatively greater trace length and lower integration density pose significant challenges for modern hardware architectures. In [84], Hartmann *et al.* presented a packet-based AER communication infrastructure to avoid the parallel AER bottleneck. However, Field Programmable Gate Arrays - Digital Network Chip (FPGA-DNC) connections still susceptible to signal distortion due to the high routing density required by



**Figure 9** Circuit modeling method for memristor-based neuromorphic chips [71]. (a) memristor-based neuromorphic chip; (b) and (c) unit cell and equivalent circuit model based on PEEC



**Figure 10** Bidirectional FIFO interface between asynchronous and synchronous domains[80].

the compact board design. Signal integrity in PCB structures relies on several factors such as the quality of the PCB trace, wires, connectors, and frequency mismatch. An example of the signal integrity of multi-tile neuromorphic system integrated in PCB [85], where eye-diagram and bath-tube measurements were conducted to evaluate signal integrity of the links.

Other type of packaging technology such as system-on-chip (SoC) was also used for heterogeneously integrating neuromorphic circuits with different sensors [86, 87]. For odor classification task, a neuromorphic spiking neural network chip was integrated with an odor sensor. Fig. 11b show olfaction chip with a die area of  $50 \text{ mm}^2$ . The chip consists of neuromorphic circuit with spike timing-dependent plasticity

(STDP) learning and an on-chip chemosensor, with an on-chip sensor interface for signal cancellation, amplification, and filtering. SoC and AER allow the design of large-scale neuromorphic computing systems [11]. However, scaling-up the number of neurons and synapses to billion level faces many challenges such as the signal propagation delay, which ultimately degrade the computing speed at the system level. Fig. 11c shows a heterogeneous system of Darwin chip[12] and traditional digital chips in 2.5-D integration structure. The system consists of: encoding, neuromorphic chip, and decoding subsystems. Compared to the PCB, 2.5-D integration shows less signal loss and jitter[88]. Moreover, novel signal integrity analysis and design methods such as the usage of two-eye approach could lead to better signal integrity across the link in 2.5-D structure as shown in Fig. 11d[88].

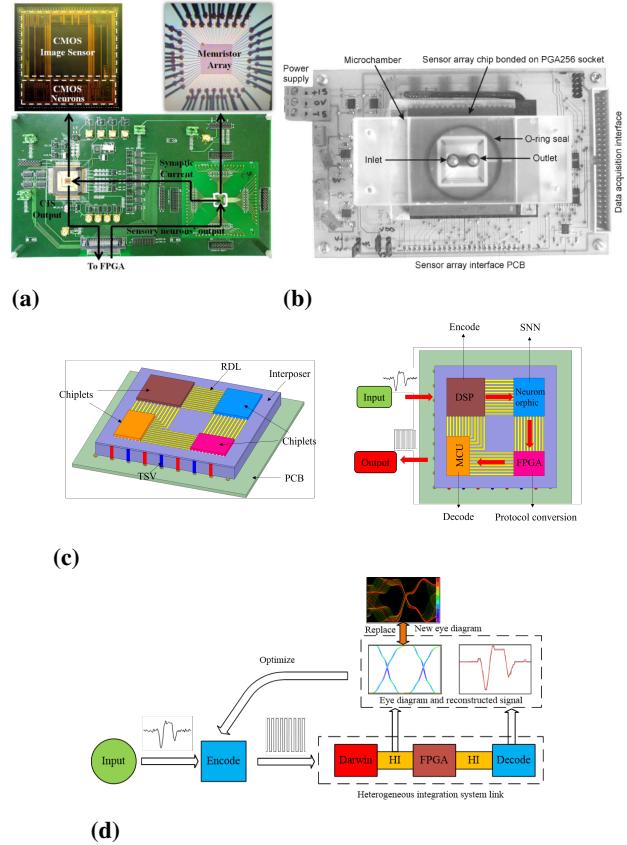
Due to the complexity of neural systems i.e., high connectivity densities and massive parallelism, 3D heterogeneous integration has been exploited in neuromorphic chips. In one hand, shorter connections can lower both the energy consumption and the latency. On the other hand, 3D stacking offers more connection lines, resulting in enhancing the bandwidth between the layers. 3D HI can take advantage of synaptic crossbar to allow high density connections, as well as

storage of internal information. Belhadj *et al.* [89] integrated a CMOS vision sensor into a neuromorphic accelerator using 130 nm technology. The sensor is composed of micro-block that issue spikes to the neurons using temporal coding [90]. The spikes are passed to the first layer through synaptic weights. The second layer works as fully-connected output classifier layer, as a feature of the parallel connections between the stacked layer in 3D structure. Copper-to-copper microbumps were used for the inter-layer connections with surface area of  $5 \times 5 \mu\text{m}^2$ . Ehsan *et al.* [91] explained proposed a neuromorphic 3D IC with Through Silicon Vias (TSVs) interconnects. As shown in Fig. 12a, each chip in the 3D structure represents a functional unit. At the bottom, CMOS layer represents the neurons, while synapses, axons/dendrites are represented by crossbar and nanowires, respectively. The usage of TSVs can be extended to other configurations as explained by Ehsan *et al.* [92]. Especially, redundant and superfluous dummy TSVs [93], where they were used as membrane capacitors (Fig. 12b) [94]. Such configurations can enhance the performance without increasing additional silicon area. The massive parallelism between the adjacent layers in 3D structure due to the abundant TSVs imposes electromagnetic interference issues such as crosstalk and electromagnetic coupling. For instance, the presence of adjacent signal TSVs imposes electromagnetic field coupling as a result of the strong mutual capacitance and inductance between the TSVs as shown in Fig. 12c [95]. Moreover, the discontinuous structure (Fig. 12d) and the bump formed at the interconnection of the TSV and redistribution layer (RDL) may lead to signal loss [96]. In fact, this type of discontinuity was found to contribute a great loss to the signal and hence compromise the signal integrity.

Recently, Choi *et al.* [97] reported a Lego-like 3D heterogeneous structure of multi-stacked neuromorphic chips. Chip-to-chip communication is achieved by optoelectronic device arrays, which not only allows stackability, but allows replaceability of sensors depending on the input. Fig. 13a shows a schematic of how the eye layer (input layer) sends the light to the next layer. Each layer has an optoelectronic device of LED and PD stacks to send and receive the light, respectively (Fig. 13b). Moreover, a library of sensors, processors, and noise-reducing processors is designed to ensure the modular reconfigurable design.

## V. Discussion and future prospects

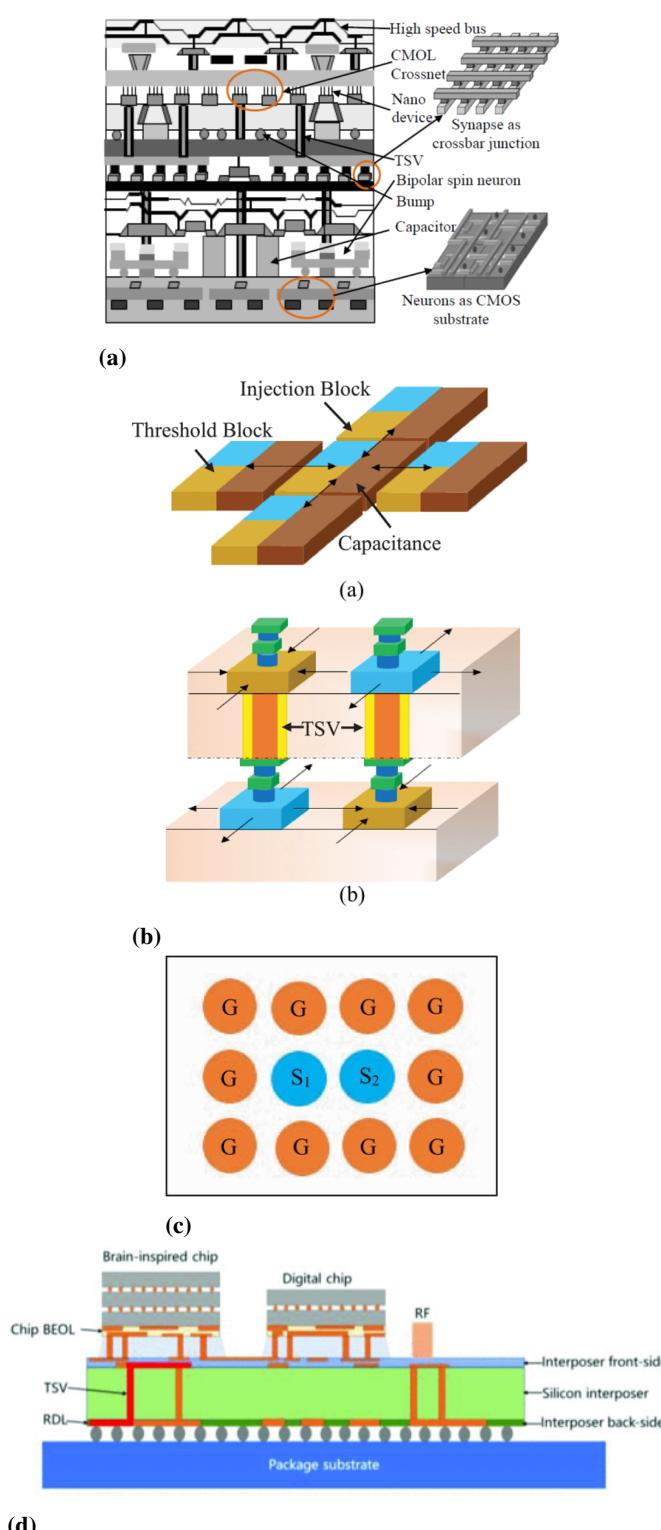
Conventional techniques for circuit prediction and optimization such as Monte Carlo (MC) [98], worst-case [99], parametric macromodeling [100, 101] and statistics-based methods suffer to provide ultimate efficiency with accurate analysis. Emergent prediction and optimization methods such as machine learning (ML) were used in many engineering fields related to CMOS technology. Using ML methods could help to alleviate difficulties related to traditional methods



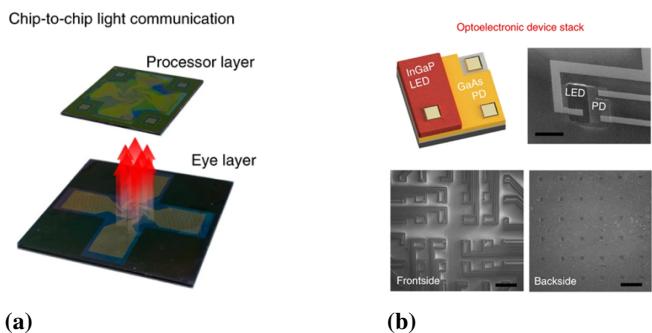
**Figure 11** Different types of HI of neuromorphic chips. (a) Neuromorphic system for visual pattern recognition implemented in PCB [83]. (b) The olfaction chip with the chemosensor array [86, 87]. Signal link in the heterogeneous system. (c) 2.5-D Heterogeneous Integrated Structure. Initially, the signal is fed to the first subsystem, which mainly comprises a DSP chip for chip coding. The coded signal is then fed to the second subsystem, consisting of the Darwin and FPGA chips, which perform SNN operations and data protocol conversion. Finally, the MCU chip outputs the signals. (d) Flow of a novel method for link analysis and result optimization of heterogeneous integration links[88].

such as electromagnetic solvers [102] and circuit simulators [103]. Although there were efforts in enhancing SI analysis [104, 105], traditional methods still face many challenges [106]. For IC design and advanced packaging, deep learning was used to predict SI performance by using the circuit parameter [107–109]. Resulting in huge time saving for electronic design automation (EDA) simulations. Fig. 14 shows an example of SI prediction for chip-to-chip using neural network [109]. Deep learning methods could be used in both ways, i.e., by having a measurement such as an eye diagram, one could identify or classify the circuit defect that causes signal loss or crosstalk [110]. Additionally, SI optimization could also be achieved as in [111], where a deep genetic algorithm (GA) was proposed to optimize a high-speed channel.

In memristor-based neuromorphic circuits, different opti-



**Figure 12** Signal integrity in 3D HI structure. (a) TSV arrangements between neuron cell layers. (b) TSV and RDL in 3D HI structure. (c) TSV based 3D neuromorphic IC [91], (d) Usage of TSV as capacitor [94].

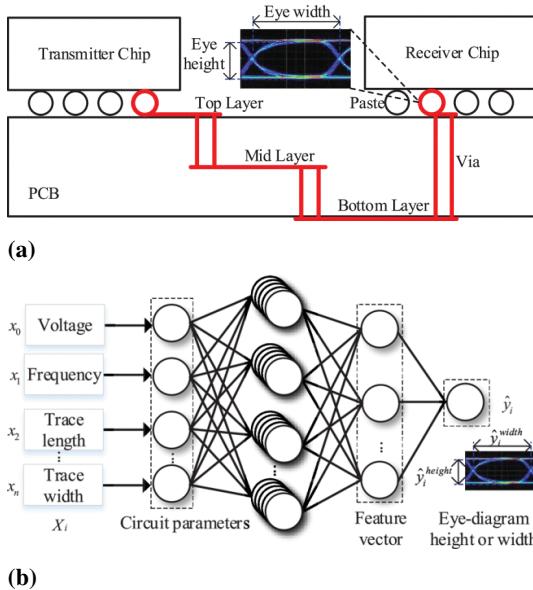


**Figure 13** Optoelectronic devices in 3D HI structure. (a) Optical photograph of the eye layer and processor layer. (b) SEM images of an optoelectronic device stack [97].

mization methods are proposed recently from three aspects: memristor device, crossbar circuit and neuromorphic computing algorithm. Firstly, the performance of the memristor device should be improved. The adjustment of memristor conductance is preferably stable and linear by adopting special material and process technology [112]. Secondly, the parameters of the interconnect wire can be modified to decrease the parasitic effects. The cross array segmentation method is proposed to flexibly create a combination of various array sizes, so as to design a memristor cross array circuit closer to the desired ideal size and reduce the calculation error [113]. Also it is necessary to develop multi-parameter optimization methods under the consideration of circuit uncertainties [114]. Thirdly, It is very necessary to design and improve the brain-like algorithm according to the SI properties of the neuromorphic chip. A novel proposed sensing training scheme (Vortex) actively compensates for the influence of device changes, thus ensuring the reasoning accuracy and enhancing the training robustness of memristor-based neuromorphic circuits [115]. An improved spiking neural network algorithm considering circuit parasitic effect is also helpful to improve the calculation accuracy and efficiency of the whole circuit [116]. In the future, the co-design of the neural network algorithm and the crossbar array structure would be very helpful. Suitable algorithms may achieve better hardware performance.

Aligning with the post-Moore era, 3D HI is expected to gain more attention to meet the urgent demands for multi-functional neuromorphic chips. Therefore, it is great importance to develop approaches to neuromorphic computing that function as close as possible to sensors, with inter-layer connection that allows module versatility, and complying with the energy and performance requirements.

In HI of stackable chips using light communication, the accurate alignment between the front- and backside of the LED/PD stacks is very crucial to ensure SI. In chip-to-chip light communication [97], the alignment of the chips is achieved by using micro-manipulators, together with the deep reactive-ion etching technique for the patterning.



**Figure 14** A hybrid neural network (HNN) used to predict the eye-diagram metrics. (a) The structure of chip-to-chip connections. (b) The structure of DNN network [109]. The network takes  $n$  channel parameters such as voltage and frequency as inputs and gives eye-diagram parameters such as the eye height and width as outputs.

To cope with the huge potential of AI in enhancing signal integrity performance in neuromorphic chips, we believe that both academic and industry institutions will keep pushing the silicon industry towards AI-driven EDA tools. The merge of AI techniques into EDA tools is expected to make SI design more simple and less time-consuming. An example of such innovation is Synopsys's new EDA suite: Synopsys.ai, which was recently unveiled as Industry's first full-stack, AI-driven EDA suite for Chipmakers [117]. Other EDA companies are expected to explore in the same direction, with more focus on the 3D-HI, enhanced chip-to-chip communication, and memristor-based devices.

## VI. Conclusion

Neuromorphic chips present a promising solutions towards the realization of efficient and robust systems that is motivated by the neurobiological system of the brain. SI in neuromorphic chips plays a crucial role in determining their performance. This paper reviews the SI issues in both neuromorphic chips, and their heterogeneous structures. First, neuromorphic chips are briefly reviewed, considering their design, algorithms, and applications. Due to the difference in nature, SI issues in memristor-based chips are discussed separately to account for the various memristor-based architectures. HI of multi-functional chips becomes inevitable due to the continuous decrease of chip size. Therefore, SI in various heterogeneous structures such as PCB, SoC, 3-D, and light connec-

tions are reviewed. Different optimization techniques to enhance the SI performance are also reviewed. Including emergent prediction and optimization methods such as ML methods. Finally, future prospects of SI optimization methods are reported.

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