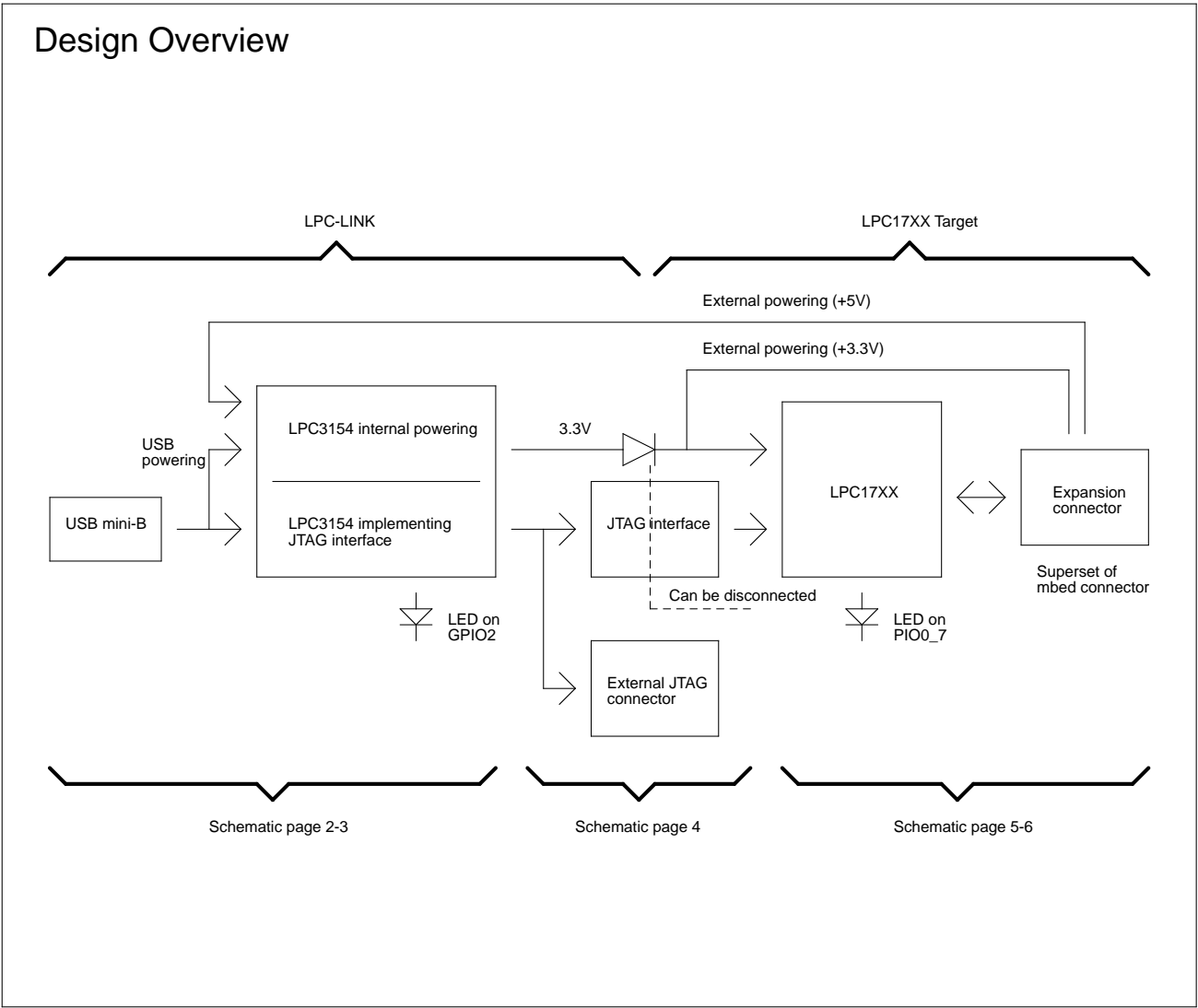


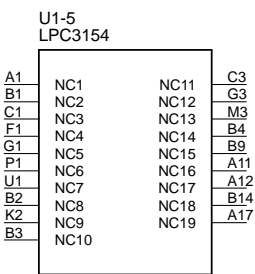
Page 2	LPC3154 Powering and Unused parts
Page 3	LPC3154 Digital I/O
Page 4	JTAG Interface
Page 5	LPC17XX with Expansion connector
Page 6	LPC17XX



UL = UnLoaded = normally not mounted component.

Default jumper settings are indicated in the schematic.  
However, always check jumper positions on actual boards  
since there is no guarantee that all jumpers are in default place.

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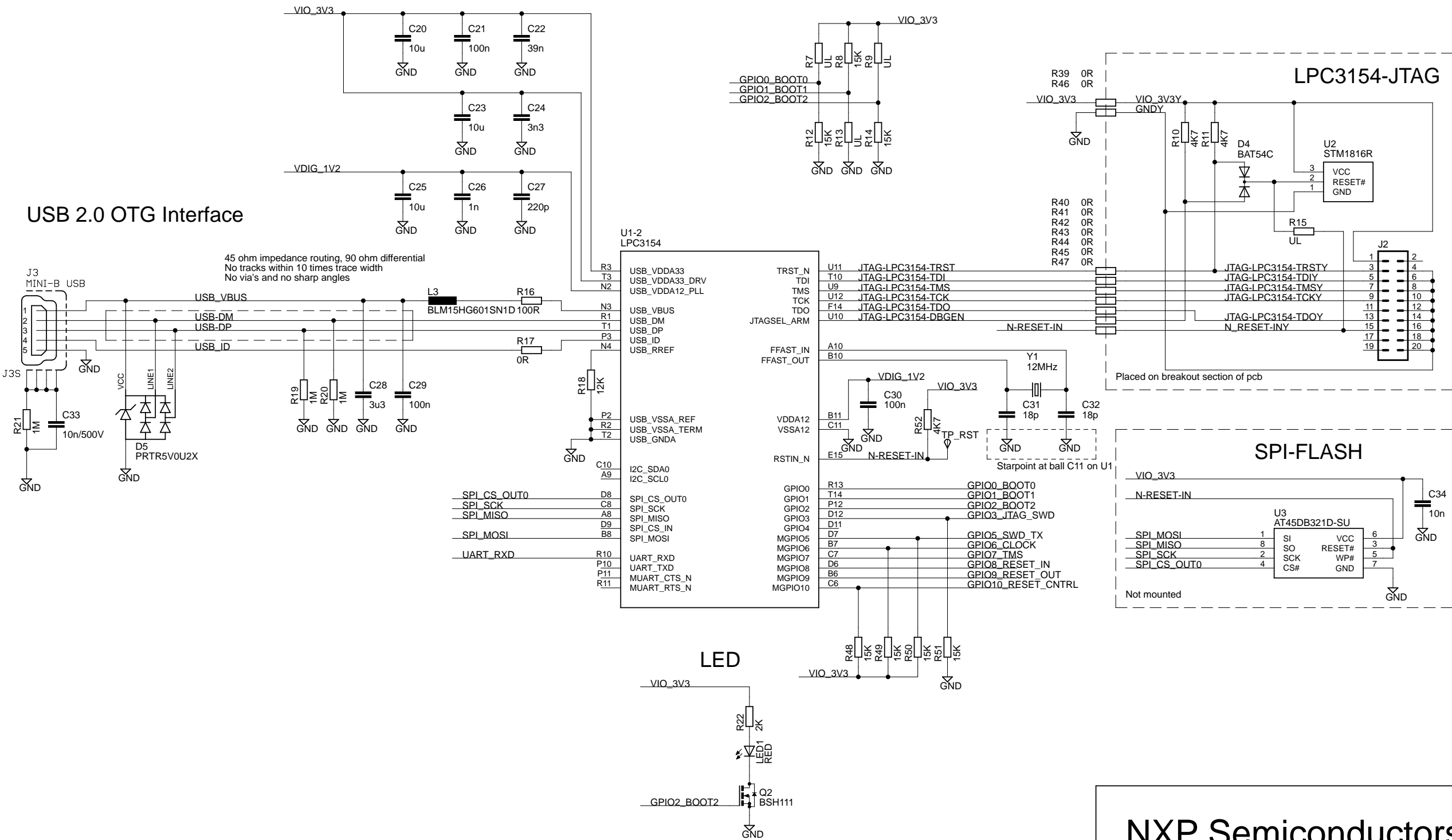
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Boot mode - USB via DFU class



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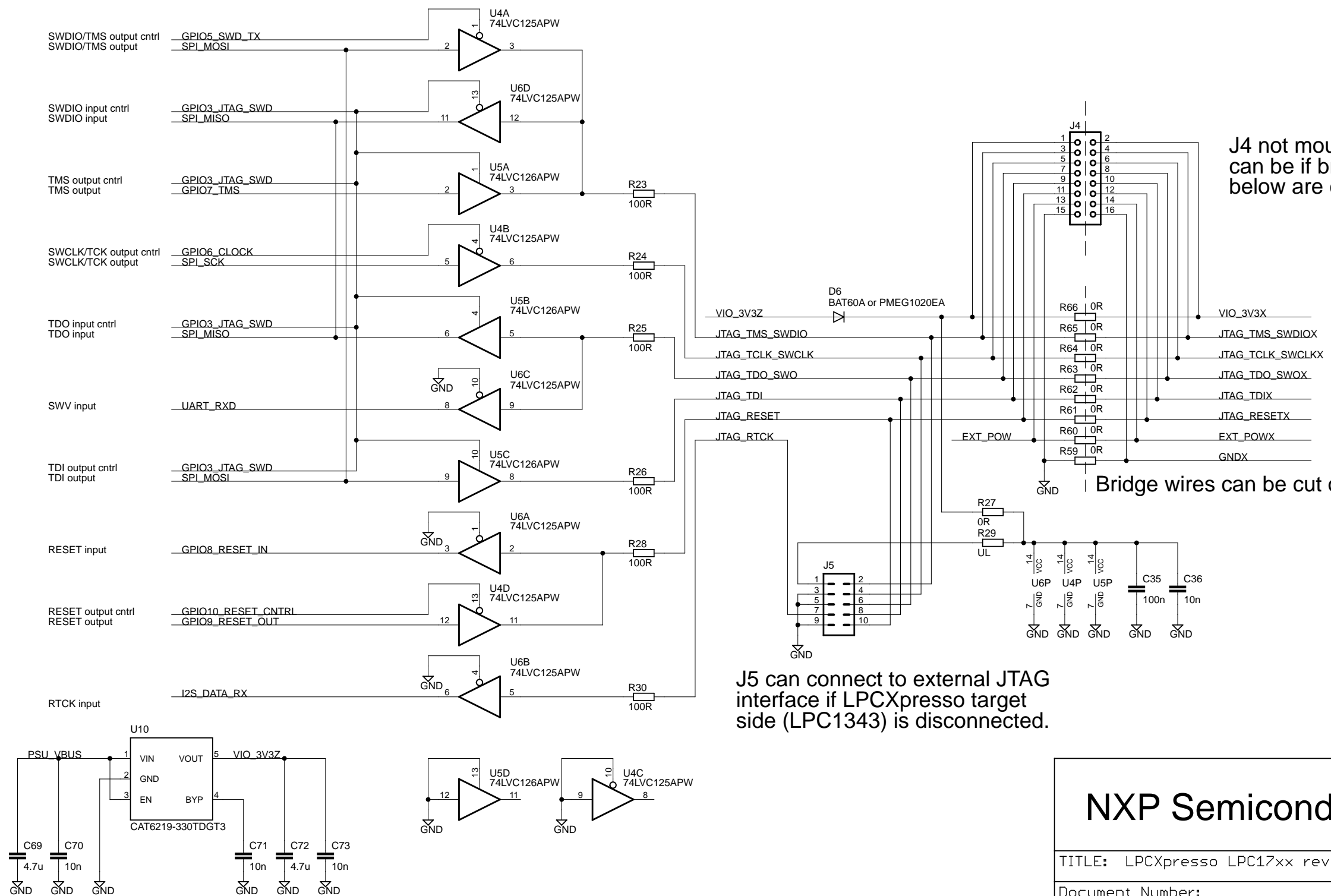
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## JTAG Interface



J4 not mounted, but  
can be if bridge wires  
below are cut.

Bridge wires can be cut on pcb

J5 can connect to external JTAG interface if LPCXpresso target side (LPC1343) is disconnected.

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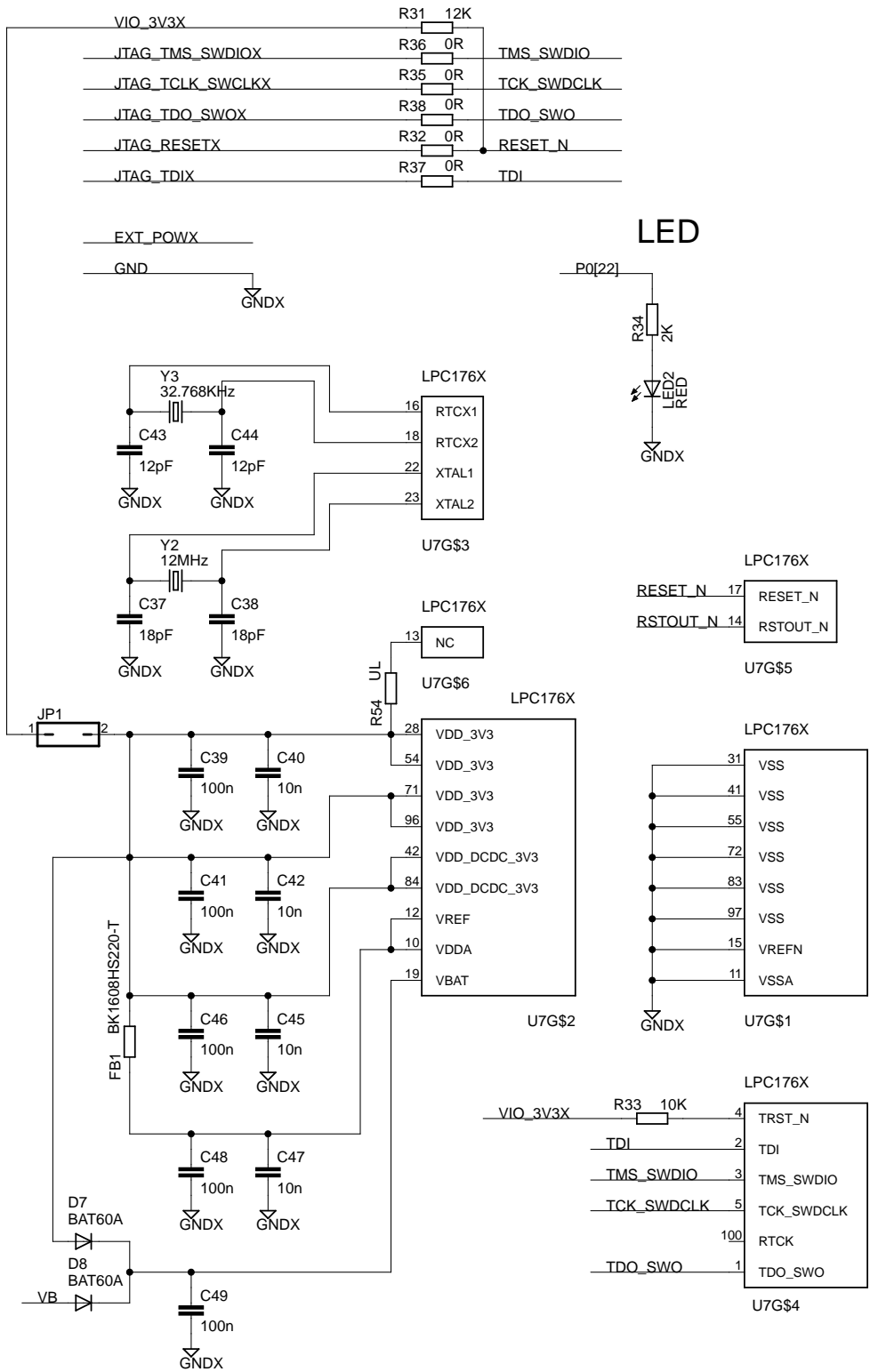
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From LPC-LINK Side



LPC1XXX Target Side

mbed	LPCXpresso
GND	GND
VIN (4.5-14V)	VIN (4.5-5.5V)
VB (battery supply)	VB (battery supply)
nR (reset)	RESET_N
SPI1-MOSI	P0.9 MOSI1
SPI1-MISO	P0.8 MISO1
SPI1-SCK	P0.7 SCK1
GPIO	P0.6 SSEL1
UART1-TX / I2C1-SDA	P0.0 TXD3/SDA1
UART1-RX / I2C1-SCL	P0.1 RXD3/SCL1
SPI2-MOSI	P0.18 MOSI0
SPI2-MISO	P0.17 MISO0
SPI2-SCL / UART2-TX	P0.15 TXD1/SCK0
UART2-RX	P0.16 RXD1/SSEL0
AIN0	P0.23 AD0.0
AIN1	P0.24 AD0.1
AIN2	P0.25 AD0.2
AIN3 / AOUT	P0.26 AD0.3/AOUT
AIN4	P1.30 AD0.4
AIN5	P1.31 AD0.5
	P0.2
	P0.3
	P0.21
	P0.22
	P0.27
	P0.28
	P2.13

Expansion Connector  
(superset of mbed pinning)

Dual row holes (2x27), 100 mil spacing	
GNDX	J6-1
EXT_POWX	J6-2
VB	J6-3
RESET_N	J6-4
P0[9]	J6-5
P0[8]	J6-6
P0[7]	J6-7
P0[6]	J6-8
P0[0]	J6-9
P0[1]	J6-10
P0[18]	J6-11
P0[17]	J6-12
P0[15]	J6-13
P0[16]	J6-14
P0[23]	J6-15
P0[24]	J6-16
P0[25]	J6-17
P0[26]	J6-18
P1[30]	J6-19
P1[31]	J6-20
P0[2]	J6-21
P0[3]	J6-22
P0[21]	J6-23
P0[22]	J6-24
P0[27]	J6-25
P0[28]	J6-26
P2[13]	J6-27

LPCXpresso	mbed
VOUT (+3.3V out) if self powered, else +3.3V input	VOUT (3.3V out)
not used	VU (5.0V USB out)
not used	IF+
not used	IF-
RD-	RD- (Ethernet)
RD+	RD+ (Ethernet)
TD-	TD- (Ethernet)
TD+	TD+ (Ethernet)
USB-D-	D- (USB)
USB-D+	D+ (USB)
P0.4 CAN_RX2	CAN-RD
P0.5 CAN_TX2	CAN-TD
P0.10 TXD2/SDA2	UART3-TX / I2C2-SDA
P0.11 RXD2/SCL2	UART3-RX / I2C2-SCL
P2.0 PWM1.1	PWMOUT0
P2.1 PWM1.2	PWMOUT1
P2.2 PWM1.3	PWMOUT2
P2.3 PWM1.4	PWMOUT3
P2.4 PWM1.5	PWMOUT4
P2.5 PWM1.6	PWMOUT5
P2.6	
P2.7	
P2.8	
P2.10	
P2.11	
P2.12	
GND	

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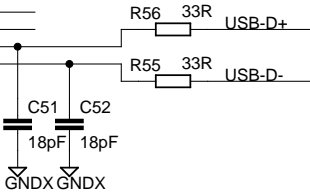
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P0_0_RD1_TXD3_SDA1	46	P0[0]
P0_1_TD1_RXD3_SCL1	47	P0[1]
P0_2_TXD0_AD0.7	98	P0[2]
P0_3_RXD0_AD0.6	99	P0[3]
P0_4_I2SRX-CLK_RD2_CAP2.0	81	P0[4]
P0_5_I2SRX-WS_TD2_CAP2.1	80	P0[5]
P0_6_I2SRX-SDA_SSEL1_MAT2.0	79	P0[6]
P0_7_I2STX-CLK_SCK1_MAT2.1	78	P0[7]
P0_8_I2STX-WS_MISO1_MAT2.2	77	P0[8]
P0_9_I2STX-SDA_MOSI1_MAT2.3	76	P0[9]
P0_10_TXD2_SDA2_MAT3.0	48	P0[10]
P0_11_RXD2_SCL2_MAT3.1	49	P0[11]
P0_15_TXD1_SCK0_SCK	62	P0[15]
P0_16_RXD1_SSEL0_SSEL	63	P0[16]
P0_17_CTS1_MISO0_MISO	61	P0[17]
P0_18_DCD1_MOSI0_MOSI	60	P0[18]
P0_19_DSR1_SDA1	59	P0[19]
P0_20_DTR1_SCL1	58	P0[20]
P0_21_RI1_RD1	57	P0[21]
P0_22_RTS1_TD1	56	P0[22]
P0_23_AD0.0_I2SRX-CLK_CAP3.0	9	P0[23]
P0_24_AD0.1_I2SRX-WS_CAP3.1	8	P0[24]
P0_25_AD0.2_I2SRX-SDA_TXD3	7	P0[25]
P0_26_AD0.3_AOUT_RXD3	6	P0[26]
P0_27_SDA0_USB-SDA1	25	P0[27]
P0_28_SCL0_USB-SCL1	24	P0[28]
P0_29_USB-D+	29	P0[29]
P0_30_USB-D-	30	P0[30]

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LPC176X

P1_0_ENET-TXD0	95	P1[0]
P1_1_ENET-TXD1	94	P1[1]
P1_4_ENET-TX_EN	93	P1[4]
P1_8_ENET-CRS	92	P1[8]
P1_9_ENET-RXD0	91	P1[9]
P1_10_ENET-RXD1	90	P1[10]
P1_14_ENET-RX_ER	89	P1[14]
P1_15_ENET-REF_CLK	88	P1[15]
P1_16_ENET-MDC	87	P1[16]
P1_17_ENET-MDIO	86	P1[17]
P1_18_USB-UP-LED_PWM1.1_CAP1.0	32	P1[18]
P1_19_MCOA_USB-PPWR-N_CAP1.1	33	P1[19]
P1_20_MCFB0_PWM1.2_SCK0	34	P1[20]
P1_21_MCABORT_PWM1.3_SSEL0	35	P1[21]
P1_22_MCOB_USB-PWRD_MAT1.0	36	P1[22]
P1_23_MCFB1_PWM1.4_MISO0	37	P1[23]
P1_24_MCFB2_PWM1.5_MOSI0	38	P1[24]
P1_25_MC1A_MAT1.1	39	P1[25]
P1_26_MC1B_PWM1.6_CAP0.0	40	P1[26]
P1_27_CLKOUT_USB-OVRCR-N_CAP0.1	43	P1[27]
P1_28_MC2A_PCAP1.0_MAT0.0	44	P1[28]
P1_29_MC2B_PCAP1.1_MAT0.1	45	P1[29]
P1_30_VBUS_AD0.4	21	P1[30]
P1_31_SCK1_AD0.5	20	P1[31]

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LPC176X

P2_0_PWM1.1_TXD1	75	P2[0]
P2_1_PWM1.2_RXD1	74	P2[1]
P2.2_PWM1.3_CTS1_TRACEDATA[3]	73	P2[2]
P2.3_PWM1.4_DCD1_TRACEDATA[2]	70	P2[3]
P2.4_PWM1.5_DSR1_TRACEDATA[1]	69	P2[4]
P2.5_PWM1.6_DTR1_TRACEDATA[0]	68	P2[5]
P2.6_PCAP1.0_RI1_TRACECLK	67	P2[6]
P2.7_RD2_RTS1	66	P2[7]
P2.8_TD2_TXD2	65	P2[8]
P2.9_USB-CONNECT_RXD2	64	P2[9]
P2.10_EINT0-N_NMI	53	P2[10]
P2.11_EINT1-N_I2STX-CLK	52	P2[11]
P2.12_EINT2-N_I2STX-WS	51	P2[12]
P2.13_EINT3-N_I2STX-SDA	50	P2[13]

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LPC176X

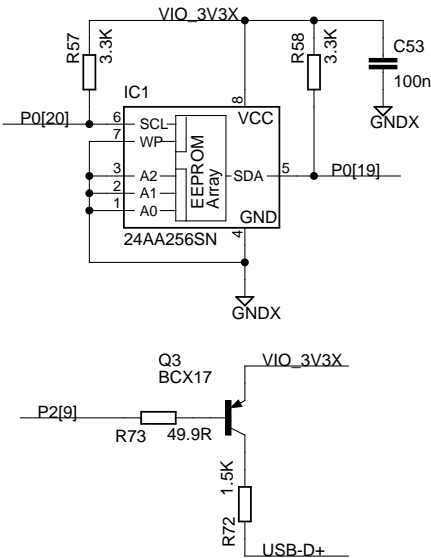
P3.25_MAT0.0_PWM1.2	27	P3[25]
P3.26_STCLK_MAT0.1_PWM1.3	26	P3[26]

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P4.28_RX-MCLK_MAT2.0_TXD3	82	P4[28]
P4.29_TX-MCLK_MAT2.1_RXD3	85	P4[29]

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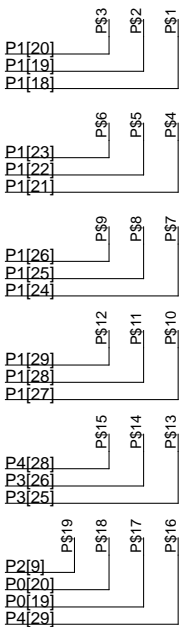
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