Homework 9

● Graded

Student

Ashley Leora Cain

Total Points

98 / 100 pts

Question 1

Test-and-Set

6 / 6 pts

✔ **– 0 pts** Correct

– 6 pts Incorrect

– 8 pts Did not identify test-and-set as being used for mutual exclusion/locks/etc. (a synchronization primitive)

– 6 pts Did not explain why test-and-set is needed for a lock implementation (atomic test-and-set to ensure no data race/consistency/etc.)

– 14 pts Blank/no answer

Question 2

Cache Addressing **24** / 24 pts

2.1 **Offset size** **8** / 8 pts

✔ **– 0 pts** Correct

– 8 pts Incorrect

– 6 pts Incorrect offset bit size (8)

– 2 pts Incorrect cache address offset (11100100; accept follow through from bit size)

– 8 pts Blank/no answer/incorrect

2.2 **Index** **8** / 8 pts

– 8 pts Incorrect

✔ **– 0 pts** Correct (9)

– 2 pts Did not use set associativity while collecting bit size (did not divide by 4)

– 2 pts Used words/block instead of bytes/block when calculating bit size (divided by 64 instead of 64 * 4 = 256)

– 6 pts Incorrect index bit size for other/unknown reason (8)

– 2 pts Incorrect cache address index (010010011; accept follow through from bit size and previous parts)

– 8 pts Blank/no answer/incorrect

2.3 **Tag** **8** / 8 pts

✔ **– 0 pts** Correct (15)

– 8 pts Incorrect

– 0 pts Incorrect bit size due to follow-through from a previous part

– 6 pts Incorrect tag bit size for other/unknown reason (15)

– 2 pts Incorrect cache address tag (011001001101001; accept follow through from bit size and previous parts)

– 8 pts Blank/no answer/incorrect

2.4 **Work (Optional)** **0** / 0 pts

✔ **+ 0 pts** Correct

Question 3

Effective Memory Access Time **22** / 24 pts

3.1 **Memory 1 EMAT** **8** / 10 pts

- **– 0 pts** Correct (10.53)
- **– 0 pts** Correct
- **– 10 pts** Incorrect
- ✔ **– 2 pts** Incorrect rounding
- **– 5 pts** Set missed rate equal to hit rate (i.e used m = (1 - .24)) (55.12)
- **– 4 pts** Did not consider access time at each level if it was a miss (i.e. did not include L1 access time if it was an L2 hit) (59.69)
- **– 6 pts** Only considered the miss rate * hit time of the lower level as the EMAT at all levels (10.13/15.13)
- **– 10 pts** Other incorrect/blank/no answer

3.2 **Memory 2 EMAT** **10** / 10 pts

- ✔ **– 0 pts** Correct (16.87)
- **– 0 pts** Correct
- **– 10 pts** Incorrect
- **– 2 pts** Incorrect rounding
- **– 5 pts** Set missed rate equal to hit rate (i.e. used m = (1 - .31)) (27.13)
- **– 4 pts** Did not consider access time at each level if it was a miss (i.e. did not include L1 access time if it was an L2 hit) (11.72)
- **– 6 pts** Only considered total miss times at all levels (25.24)
- **– 10 pts** Other incorrect/blank/no answer

3.3 **EMAT Comparison** **4** / 4 pts

- ✔ **– 0 pts** Correct
- **– 0 pts** Correct (follow through)
- **– 4 pts** Incorrect

3.4 **Work (Optional)** **0** / 0 pts

- ✔ **+ 0 pts** Correct

Question 4

Effective CPI **34** / 34 pts

4.1 **Cost of instruction misses** **8** / 8 pts

✔ **+ 8 pts** Correct (1.2)

+ 0 pts Incorrect

4.2 **Cost of data read misses** **8** / 8 pts

+ 0 pts Incorrect

✔ **+ 8 pts** Correct (0.112)

4.3 **Cost of data write misses** **8** / 8 pts

✔ **+ 8 pts** Correct (0.0084)

+ 0 pts Incorrect

4.4 **Effective CPI** **10** / 10 pts

✔ **+ 10 pts** Correct (3.2204)

+ 10 pts Incorrect final result owing to incorrect previous steps

+ 8 pts Minor Mistake

+ 0 pts Incorrect

Question 5

Page Coloring **12** / 12 pts

5.1 **Overlapping Bits** **6** / 6 pts

✔ **+ 6 pts** Correct (4)

+ 0 pts Incorrect

5.2 **Overlap in Cache Address** **6** / 6 pts

✔ **+ 6 pts** Correct

+ 0 pts Incorrect

5.3 **Work (Optional)** **0** / 0 pts

✔ **+ 0 pts** Correct

Q1 Test-and-Set
6 Points

In order to support synchronization between multiple processes, why do we need a test-and-set (T&S) instruction instead of just using existing load, store, and branch-if-zero instructions?

- ○ processor speed
- ○ efficiency
- ◉ atomicity
- ○ energy saving
- ○ reduction in CPI

Q2 Cache Addressing

24 Points

Listed below are the cache parameters that describe the cache layout for a byte-addressable memory system:

- 4 way set associative
- 32 bit address
- block size of 64 words
- word size of 4 bytes
- total cache size of 128K words (512 KB)

Use these parameters to evaluate how this cache will interpret an address and the sizes of each part of the address. (Also, use 1 KB = 1024 B = 2^10 B)

Q2.1 Offset size

8 Points

What is the size (in bits) of the offset?

8

Given the following cache address, what is the offset (in binary)? Assume the cache address follows the format *tag* | *index* | *offset*.

Cache address = $01100100110100101001001111100100$

11100100

Q2.2 Index
8 Points

What is the size (in bits) of the index?

9

Given the following cache address, what is the index (in binary)? Assume the cache address follows the format *tag* | *index* | *offset*.

Cache address = 01100100110100101001001111100100

010010011

Q2.3 Tag
8 Points

What is the size (in bits) of the tag?

15

Given the following cache address, what is the tag (in binary)? Assume the cache address follows the format *tag* | *index* | *offset*.

Cache address = 01100100110100101001001111100100

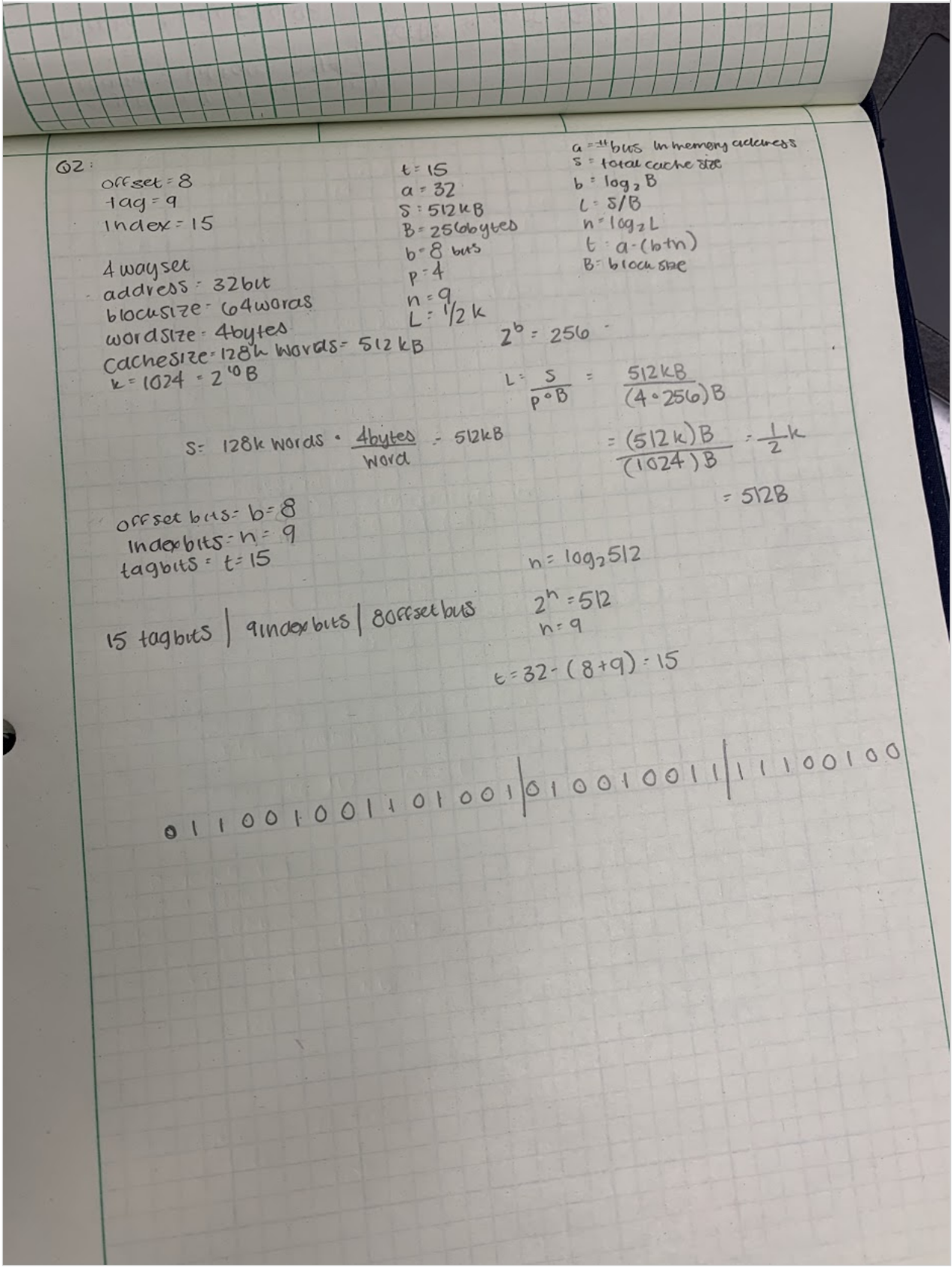
011001001101001

Q2.4 Work (Optional)
0 Points

For partial credit, show your work in the field below or attach it as a file.

HW 9 Q2.jpg

Download



Q3 Effective Memory Access Time

24 Points

Say we have two setups for hierarchical memory with the following miss rates and hit times:

Memory 1

Hardware	Miss Rate	Hit Time
L1 Cache	0.24	5 ns
L2 Cache	0.11	17 ns
Main Memory	0	55 ns

Memory 2

Hardware	Miss Rate	Hit Time
L1 Cache	0.50	5 ns
L2 Cache	0.31	7 ns
Main Memory	0	54 ns

Q3.1 Memory 1 EMAT

10 Points

What is the EMAT (effective memory access time) for Memory 1 in ns? Round your answer to 2 decimal places.

10.532

Q3.2 Memory 2 EMAT
10 Points

What is the EMAT (effective memory access time) for Memory 2 in ns? Round your answer to 2 decimal places.

16.87

Q3.3 EMAT Comparison
4 Points

Which setup has a better EMAT?

- (●) Memory 1
- ( ) Memory 2

Q3.4 Work (Optional)
0 Points

If you would like partial credit in case of an incorrect answer on the previous parts, show your work in the field below or attach it as a file:

No files uploaded

Q4 Effective CPI

34 Points

Consider a pipelined processor that has an average CPI of 1.9 without accounting for memory stalls. It has separate instruction and data caches.

- I-Cache has a hit rate of 94%
- D-Cache has a hit rate of 98%.

Assume that memory reference instructions account for 35% of all the instructions executed.

- 80% are loads
- 20% are stores

On average for both caches

- read-miss penalty is 20 cycles.
- write-miss penalty is 6 cycles.

Q4.1 Cost of instruction misses

8 Points

What is the cost of instruction cache misses in CPI?

1.2

Q4.2 Cost of data read misses

8 Points

What is the cost of data read misses in CPI?

0.112

Q4.3 Cost of data write misses

8 Points

What is the cost of data write misses in CPI?

0.0084

Q4.4 Effective CPI
10 Points

Compute the effective CPI of the processor accounting for the memory stalls.

3.2204

Q5 Page Coloring

12 Points

Page coloring is used to make sure that a few least significant bits of the virtual page number (VPN) and physical frame number (PFN) remain unchanged during address translation.

Imagine the following memory hierarchy:

- 64-bit virtual address
- 32-bit physical address
- Virtually-indexed, physically-tagged, 2-way set associative cache
- Page size of 8 KB
- Memory is byte-addressable
- Total Cache Size of 256 KB
- Cache block size of 128 bytes

Assume K = 1024 and M = 1024 * 1024.

Q5.1 Overlapping Bits

6 Points

How many of the least significant bits of the VPN must remain unchanged in the VPN-PFN translation?

4

Q5.2 Overlap in Cache Address

6 Points

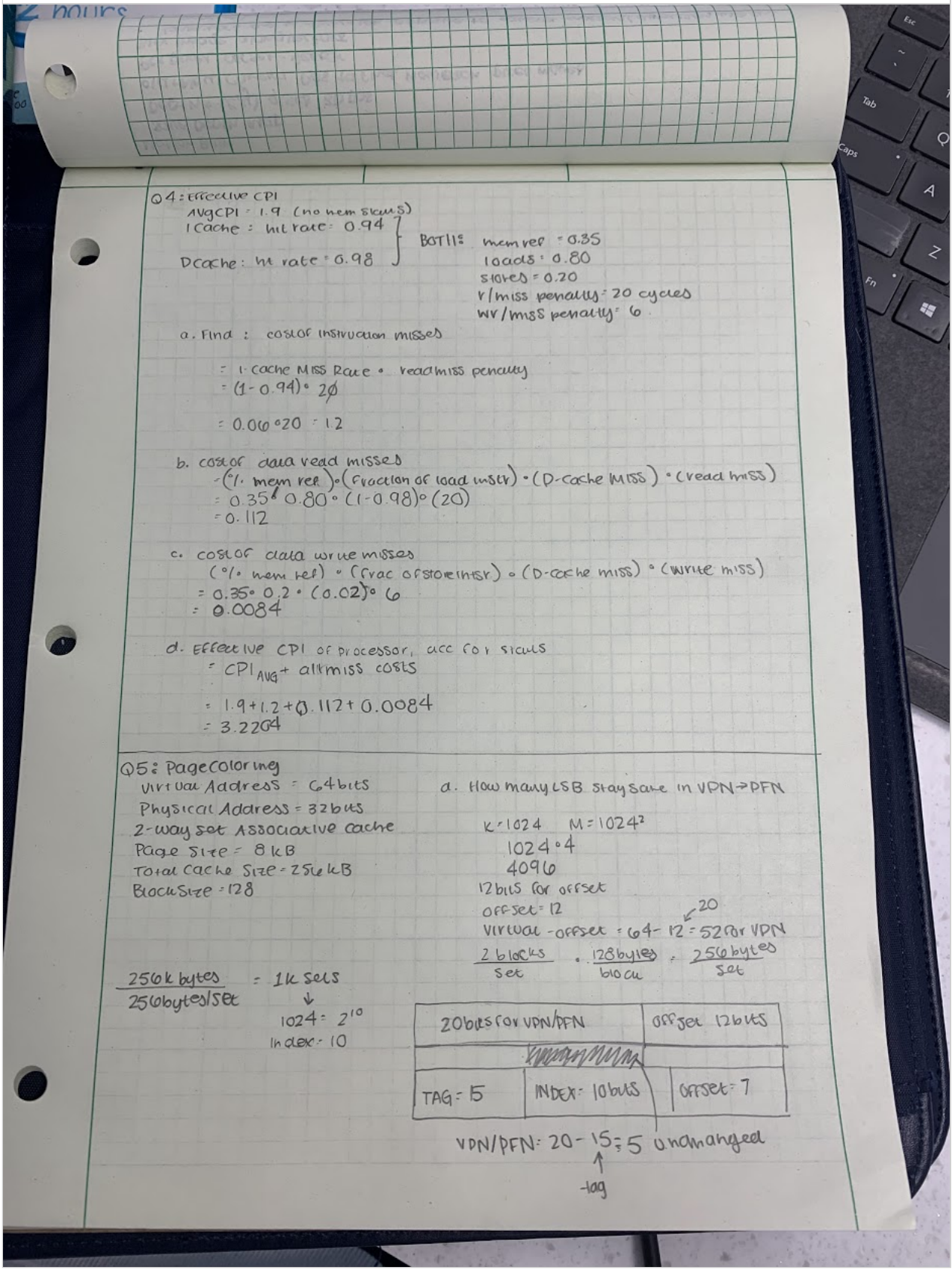
Where in the cache address are the overlapping bits present? (End describes positions touching MSB, and beginning describes positions touching LSB)

- ○ End of the tag
- ○ Beginning of the index
- ○ Middle of the index
- ◉ End of the index
- ○ Beginning of the offset

Q5.3 Work (Optional)
0 Points

If you would like partial credit in case of an incorrect answer on the previous parts, show your work in the field below or attach it as a file:

HW 9 Q4 and Q5.jpg Download



I also attached the work for q4
I assumed the "end of index" was referring to the MSB of that portion of the

portion