Homework 7

Graded

Student

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Total Points

94 / 100 pts

Question 1

Virtual Memory Concepts — **32** / 32 pts

1.1 **Memory Compaction** — **8** / 8 pts

✔ **– 0 pts** Correct (False)

– 2 pts Did not mark False

– 6 pts Incorrect justification (bounds registers supports static relocation or equivalent)

– 8 pts Blank/no answer

1.2 **Paging and Segmentation** — **8** / 8 pts

✔ **– 0 pts** Correct (True)

– 2 pts Did not mark True

– 6 pts Incorrect justification (Fails to discuss how segmentation can have segments of different sizes while paging has pages of the same size. Other correct justifications also accepted)

– 8 pts Blank/no answer

1.3 **Base and Limit Register** — **8** / 8 pts

✔ **– 0 pts** Correct (false)

– 2 pts Did not mark False

– 6 pts Incorrect justification (Does not discuss how base and limit solution can have the memory manager decide the memory location, etc.)

– 4 pts Incomplete justification

– 8 pts Blank/no answer

1.4 **External Fragmentation** — **8** / 8 pts

✔ **– 0 pts** Correct (true)

– 2 pts Did not mark true

– 6 pts Incorrect justification (Fails to discuss how pages are the same size)

– 8 pts Blank/no answer

Question 2

Addresses and Page Tables **28** / 28 pts

2.1 Virtual Address Layout **8** / 8 pts

- ✔ **– 0 pts** Correct
- **– 8 pts** Incorrect
- **– 2 pts** Incorrect | Label 1 | (VPN)
- **– 2 pts** Incorrect | Label 2 | (Offset)
- **– 2 pts** Incorrect | Label 1 | bit size (18)
- **– 2 pts** Incorrect | Label 2 | bit size (14)
- **– 8 pts** Blank/no answer

2.2 Physical Address Layout **8** / 8 pts

- ✔ **– 0 pts** Correct
- **– 8 pts** Incorrect
- **– 2 pts** Incorrect | Label 1 | (PFN)
- **– 2 pts** Incorrect | Label 2 | (Offset)
- **– 2 pts** Incorrect | Label 1 | bit size (10)
- **– 2 pts** Incorrect | Label 2 | bit size (14)
- **– 8 pts** Blank/no answer

2.3 Page Table Entries **6** / 6 pts

- ✔ **– 0 pts** Correct (262144)
- **– 0 pts** Correct
- **– 6 pts** Incorrect
- **– 2 pts** Partial credit: right power of two (2^18) but wrong answer submitted
- **– 4 pts** Calculated page size instead (16384)
- **– 6 pts** Incorrect/blank/no answer

2.4 **Page Frames** **6** / 6 pts

✔ **– 0 pts** Correct (1024)

– 0 pts Correct

– 6 pts Incorrect

– 4 pts Partial credit: Correct calculation but incorrect number of bits for PFN

– 2 pts Partial credit: right power of two (2^10) but wrong answer submitted

– 6 pts Incorrect/blank/no answer

2.5 **Work** **0** / 0 pts

✔ **+ 0 pts** Correct

Question 3

Page Faults **16** / 16 pts

3.1 **Offset Bits** **4** / 4 pts

✔ **– 0 pts** Correct

– 4 pts Incorrect

3.2 **Address Translation** **8** / 8 pts

✔ **– 0 pts** Correct (0xCAFEA30)

– 8 pts Incorrect

– 0 pts Correct

– 4 pts Incorrect offset portion (A30, last three numbers; or wrong size)

– 4 pts Incorrect PFN portion (CAFE, first four numbers; or wrong size)

– 8 pts Blank/no answer

3.3 **Page Fault** **4** / 4 pts

✔ **– 0 pts** Correct

– 4 pts Incorrect

Question 4

Second Chance Replacement **18** / 24 pts

4.1 **Structures Needed** **2** / 8 pts

- **– 0 pts** Correct
- **– 3 pts** Did not mention circular queue/circular queue-like function/FIFO (just need to mention one)

  Ex: frame table or separate queue
- **– 3 pts** Did not mention referenced bit
- ✔ **– 3 pts** Did not mention clearing referenced bit while going through queue
- ✔ **– 3 pts** Did not mention selecting the first victim without a referenced bit set
- **– 12 pts** Blank/no answer

4.2 **Advantages over FIFO** **8** / 8 pts

- ✔ **– 0 pts** Correct
- **– 4 pts** Does not explain that referenced allows pages accessed more frequently recently to not be evicted (therefore less page faults).

4.3 **Degenerates to FIFO** **8** / 8 pts

- ✔ **– 0 pts** Correct
- **– 6 pts** Did not mention Second Chance Replacement uses a FIFO ordering for frames (can imply this)
- **– 6 pts** Did not mention all referenced bits being set to the same value (0 or 1) causes FIFO degeneration; only one example needed
- **– 12 pts** Blank/no answer

Q1 Virtual Memory Concepts
32 Points

For the questions below, answer true/false and justify your choice.

Q1.1 Memory Compaction
8 Points

Memory compaction is usually used with fixed-size partition memory allocation scheme.

- ○ True
- ◉ False

Why is this statement true/false?

Compaction is used in variable memory partition memory allocation, since fixed size allocation must use the same sized memory and can't be modified. Also this helps eliminate external fragmentation.

Q1.2 Paging and Segmentation
8 Points

Paging and Segmentation both use a table for virtual to physical mapping since they work in a similar way.

- ◉ True
- ○ False

Why is this statement true/false?

Paging process uses a page table to convert partial virtual memory portions to physical pages at broken up sections of physical mem. Segmentation is similar mapping technique since it takes a large-scale program and its components to dedicate address spaces (segments) to the storage of different functional components in memory.

Q1.3 Base and Limit Register
8 Points

There is no special advantage for the base and limit register solution over the bounds register solution for memory management.

- ○ True
- ◉ False

Why is this statement true/false?

Base + limit registers are needed to support dynamic relocation on LC-2200

Q1.4 External Fragmentation
8 Points

Paged virtual memory can eliminate external fragmentation.

- ◉ True
- ○ False

Why is this statement true/false?

Paged segmented memory systems can have internal fragmentation, but not external. Since distinct pages don't need to be mapped contiguously in physical memory, the technique will eliminate external fragmentation. This is also aided by the fact that page sizes can be smaller than the allocated space in their associated memory segment.

Q2 Addresses and Page Tables

28 Points

Our operating system uses 32-bit virtual addresses, 24-bit physical addresses, and page sizes of 16KB.

For Q2.1 and Q2.2, complete the layout of the virtual and physical addresses by labelling each field with the correct value, as well as denoting the bit size for each field.

Q2.1 Virtual Address Layout

8 Points

Fill in the layout below with the appropriate fields for the **VIRTUAL address**.

Label 1	Label 2

What part of the virtual address is `Label 1`?

Virtual Page Number

What part of the virtual address is `Label 2`?

Page Offset

What is the bit size of `Label 1`?

18

What is the bit size of `Label 2`?

14

Q2.2 Physical Address Layout
8 Points

Fill in the layout below with the appropriate fields for the **PHYSICAL address**.

Label 1	Label 2

What part of the physical address is `Label 1`?

Page Frame Number

What part of the physical address is `Label 2`?

Page Offset

What is the bit size of `Label 1`?

10

What is the bit size of `Label 2`?

14

Q2.3 Page Table Entries
6 Points

How many entries are there in the page table? Format your answer as a base 10 number (standard number). So if your answer is 2^4, write "16".

262144

Q2.4 Page Frames
6 Points

How many page frames does the memory system have? (assume there are no hardware limitations) Again, format your answer as a base 10 number (standard number).

1024

Q2.5 Work
0 Points

In order to receive partial credit for an incorrect answer for Q2.3 and Q2.4, please show your work and attach it below. **Incorrect answers with no work shown will receive 0 points.**

No files uploaded

Q3 Page Faults
16 Points

Say we have virtual addresses of 32 bits, physical addresses of 28 bits, and a page size of 4KB. Given the following page table entries from the process' page table, answer the following questions.

VPN	PFN	Valid?
35FCA	2A2F	V
47F99	CAFE	V
4ECD5	BEEF	I
50AAC	223D	V

Q3.1 Offset Bits
4 Points

How many bits does the offset in an address have?

12

Q3.2 Address Translation
8 Points

You are given a virtual address of 0x47F99A30. According to the table above, what is its corresponding physical address?

0xCAFEA30

Q3.3 Page Fault
4 Points

Which of the following VPNs is held by a Page Table Entry that may lead to a page fault?

- ○ 35FCA
- ○ 47F99
- ◉ 4ECD5
- ○ 50AAC
- ○ None of the above

Q4 Second Chance Replacement

24 Points

Provide short answers to the following questions on the Second Chance page replacement algorithm.

Q4.1 Structures Needed

8 Points

What data structures and bookkeeping features are needed to implement Second Chance replacement algorithm? Explain how the algorithm selects a page for eviction.

reference bit: if frame has been used recently, then the associated reference bit will be 1. This will help to reduce amount of physical memory used so that the least recently used pages will be removed
circular queue: this is the main data structure that holds all of the pages and implement the frame table. This allows for all pages and reference bits to be iterated through for deletion or changes in reference bit.

Q4.2 Advantages over FIFO

8 Points

What are the advantages of Second Chance Replacement algorithm over FIFO? Explain why it performs better in most cases.

Second chance replacement will have better expected performance than FIFO since frames used in more frequency will remain in the frame table for longer. This algorithm's better performance is aided by the idea that recently used processes are more likely to be used in higher frequency in the near future of execution.

Q4.3 Degenerates to FIFO
8 Points

Second Chance replacement algorithm can degenerate to FIFO. Explain the circumstances in which this might occur.

This would occur when the final frame in the table is the one to be removed, then all the reference bits in page table are 0, so the algorithm will remove the first added bit to the table because the first reference bit is 0. This will continue in a FIFO order since all of the other bits are also 0. Also if all bits are set, then you would change first bit to 0 and iterate through all of the rest and then you would return to and remove the first one since that is the only 0 bit.