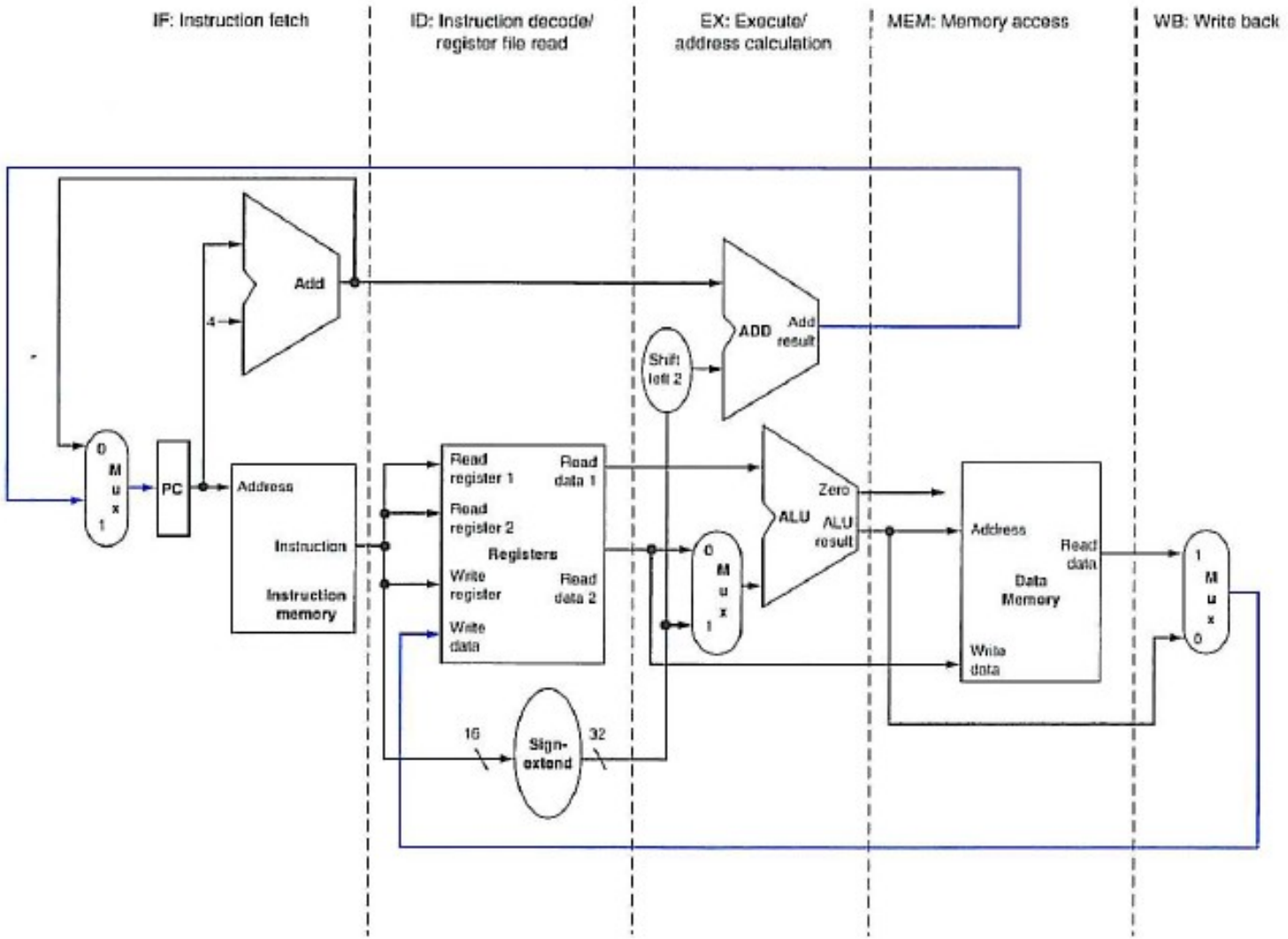
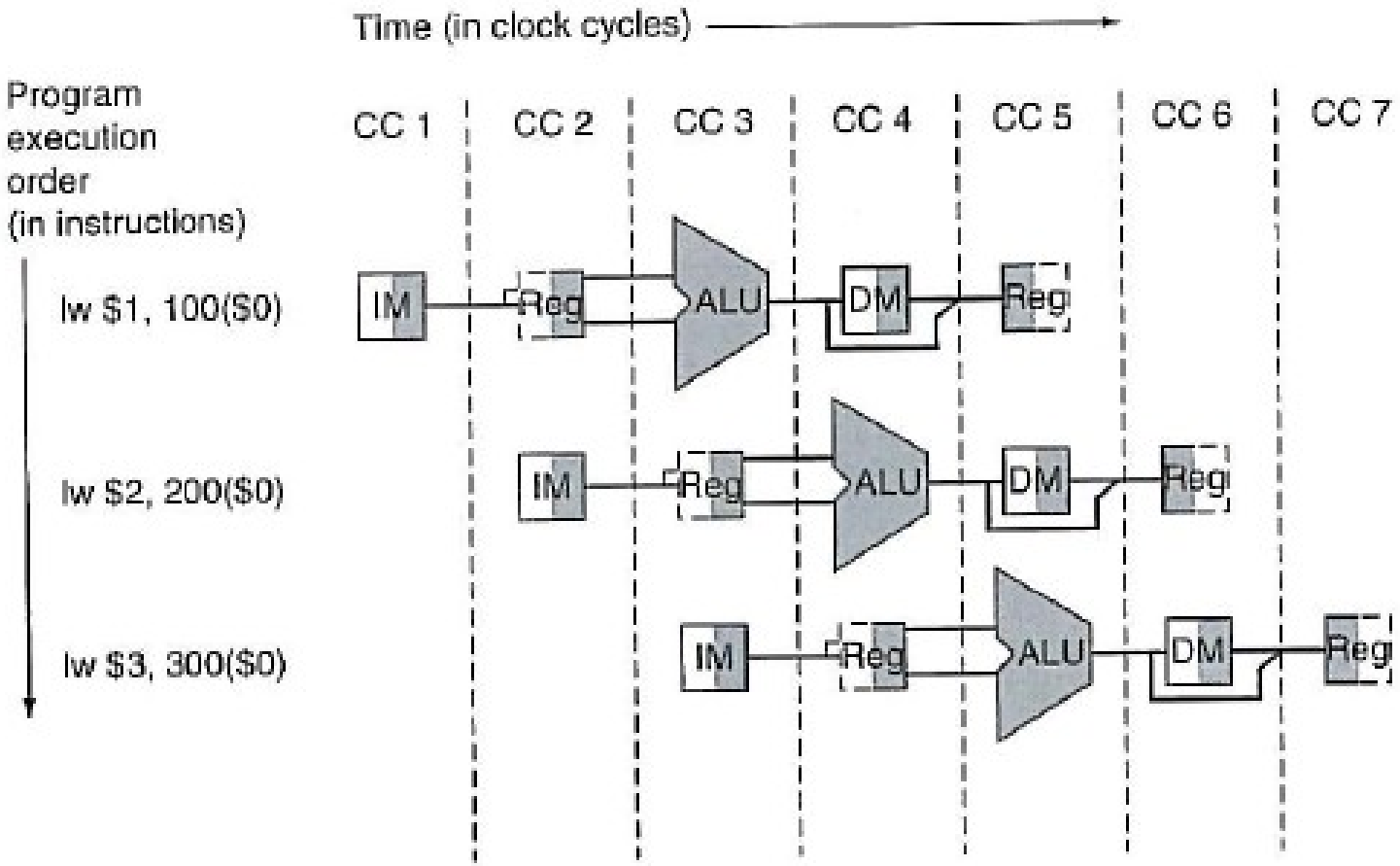
DATA PATH Y CONTROL DEL PIPELINE 1/26
DATA PATH



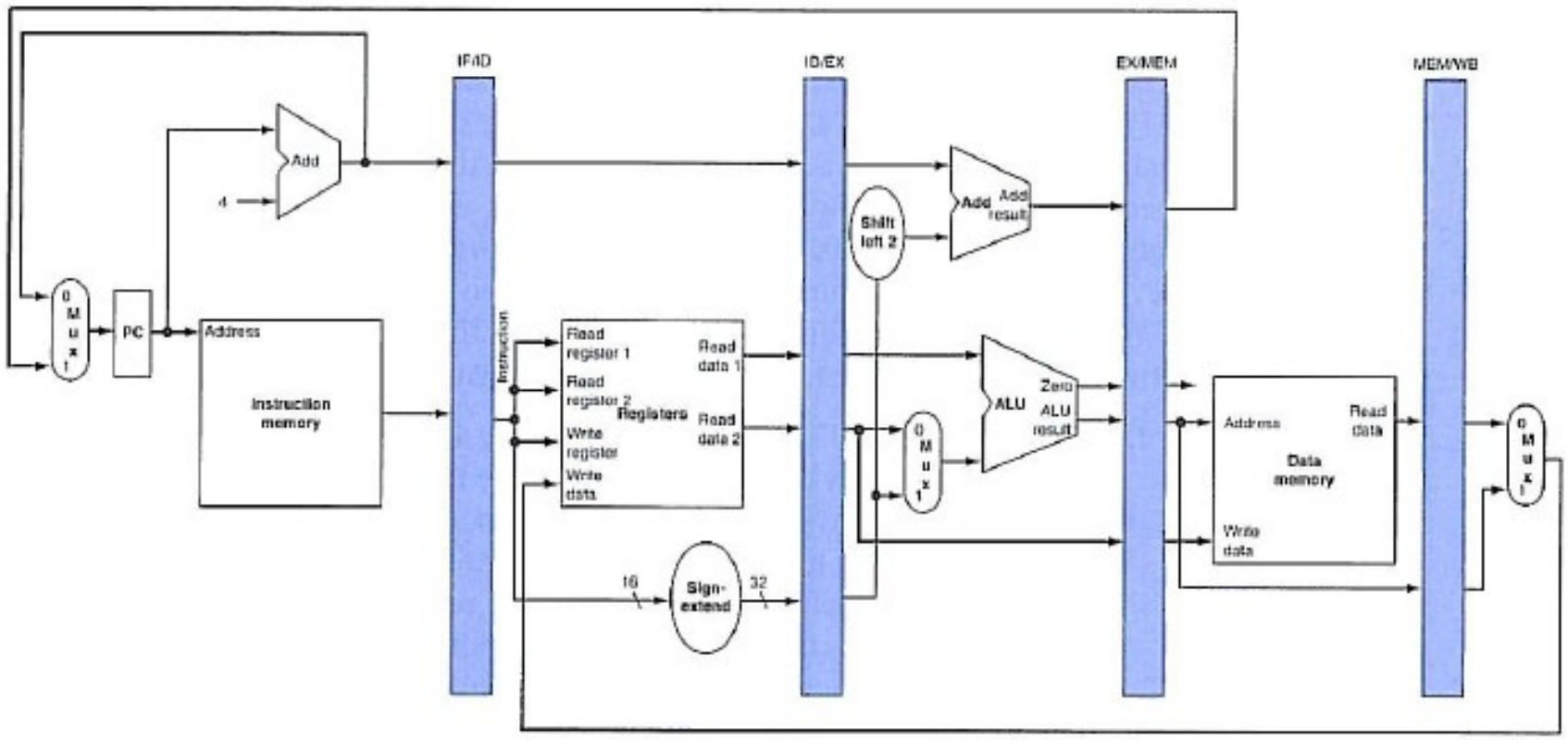
DATA PATH Y CONTROL DEL PIPELINE 2/26
DATA PATH

1. IF: Instruction fetch
2. ID: Instruction decode and register file read
3. EX: Execution or address calculation
4. MEM: Data memory access
5. WB: Write back

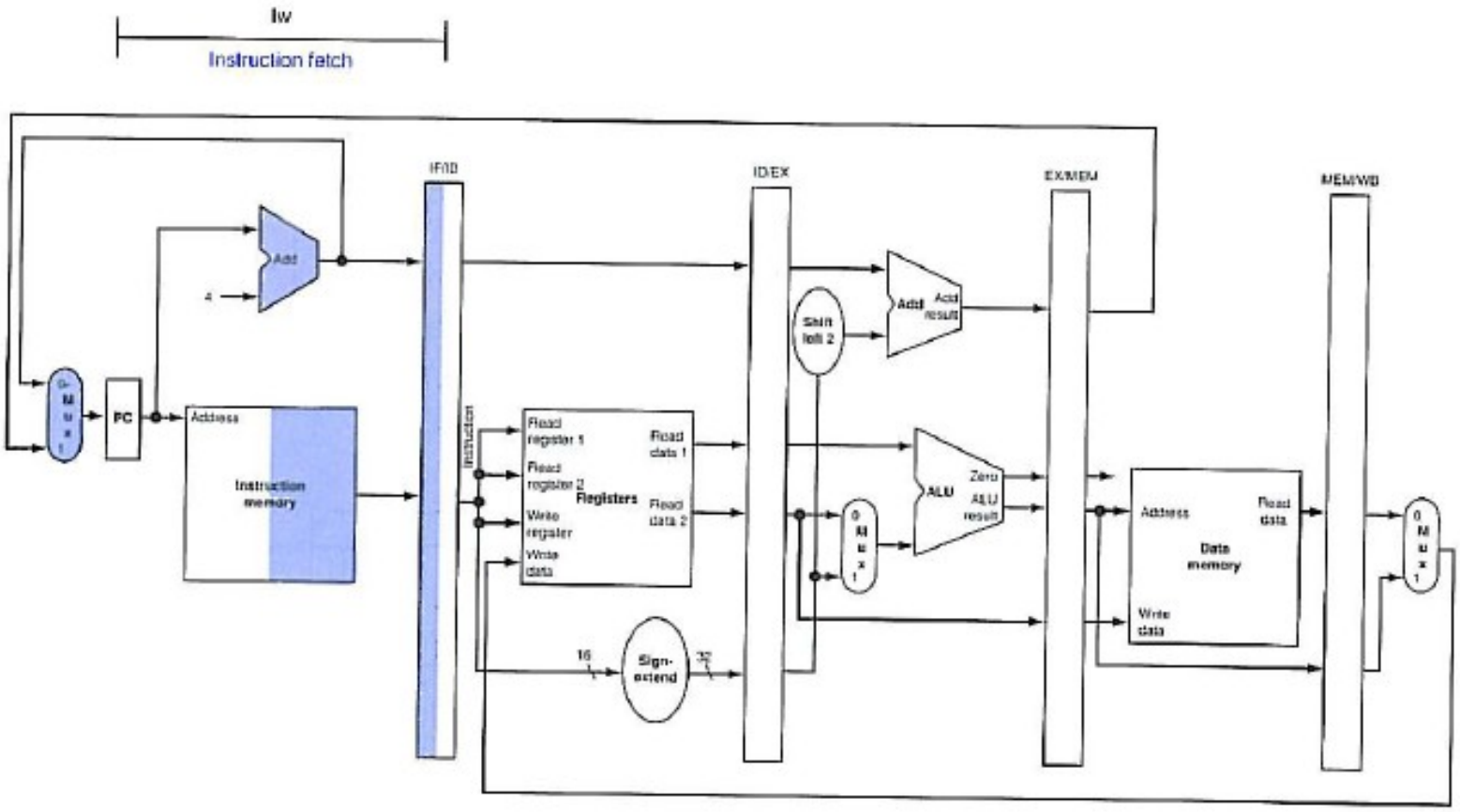
DATA PATH Y CONTROL DEL PIPELINE 3/26
DATA PATH



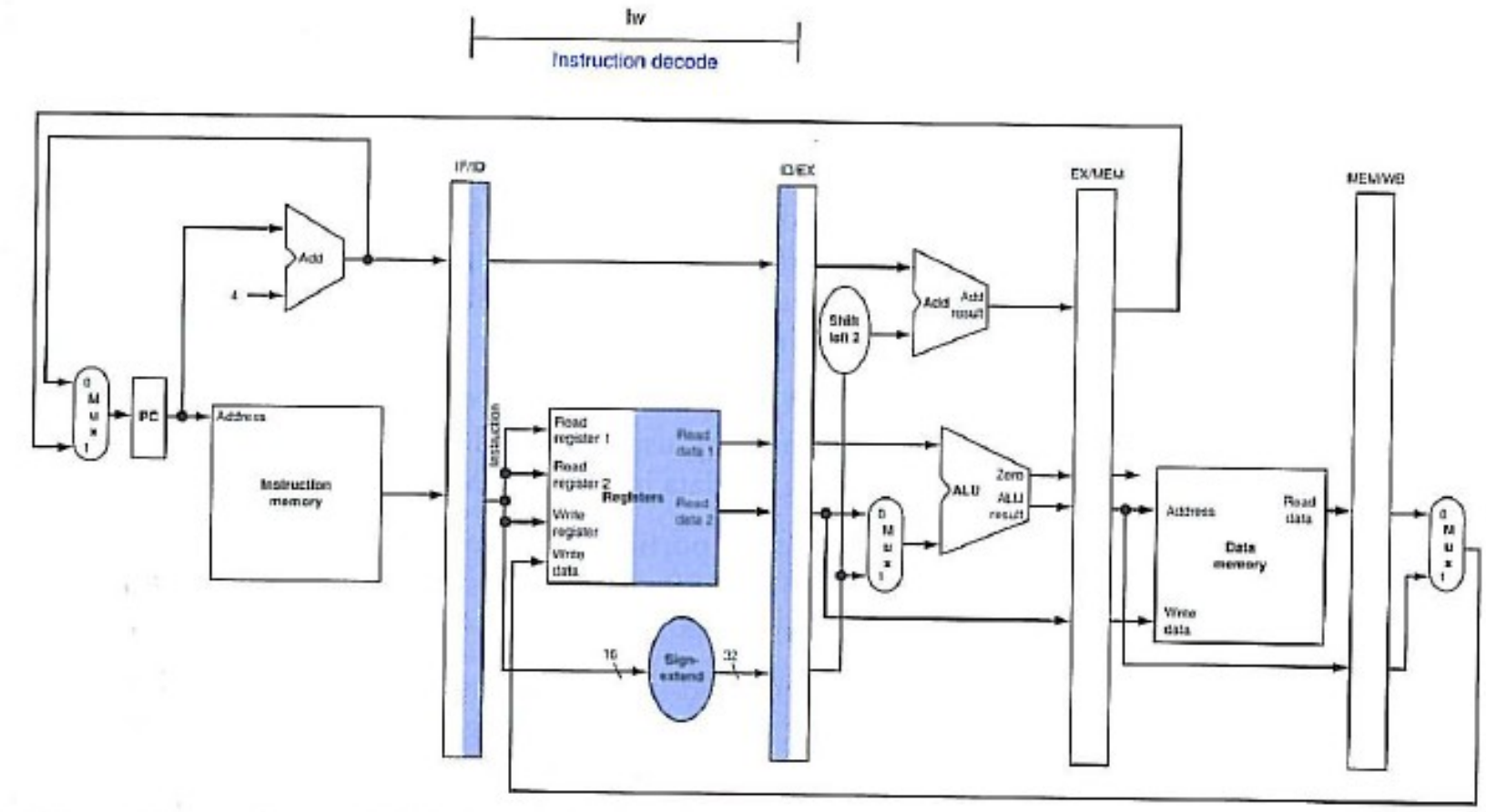
DATA PATH Y CONTROL DEL PIPELINE 4/26
DATA PATH



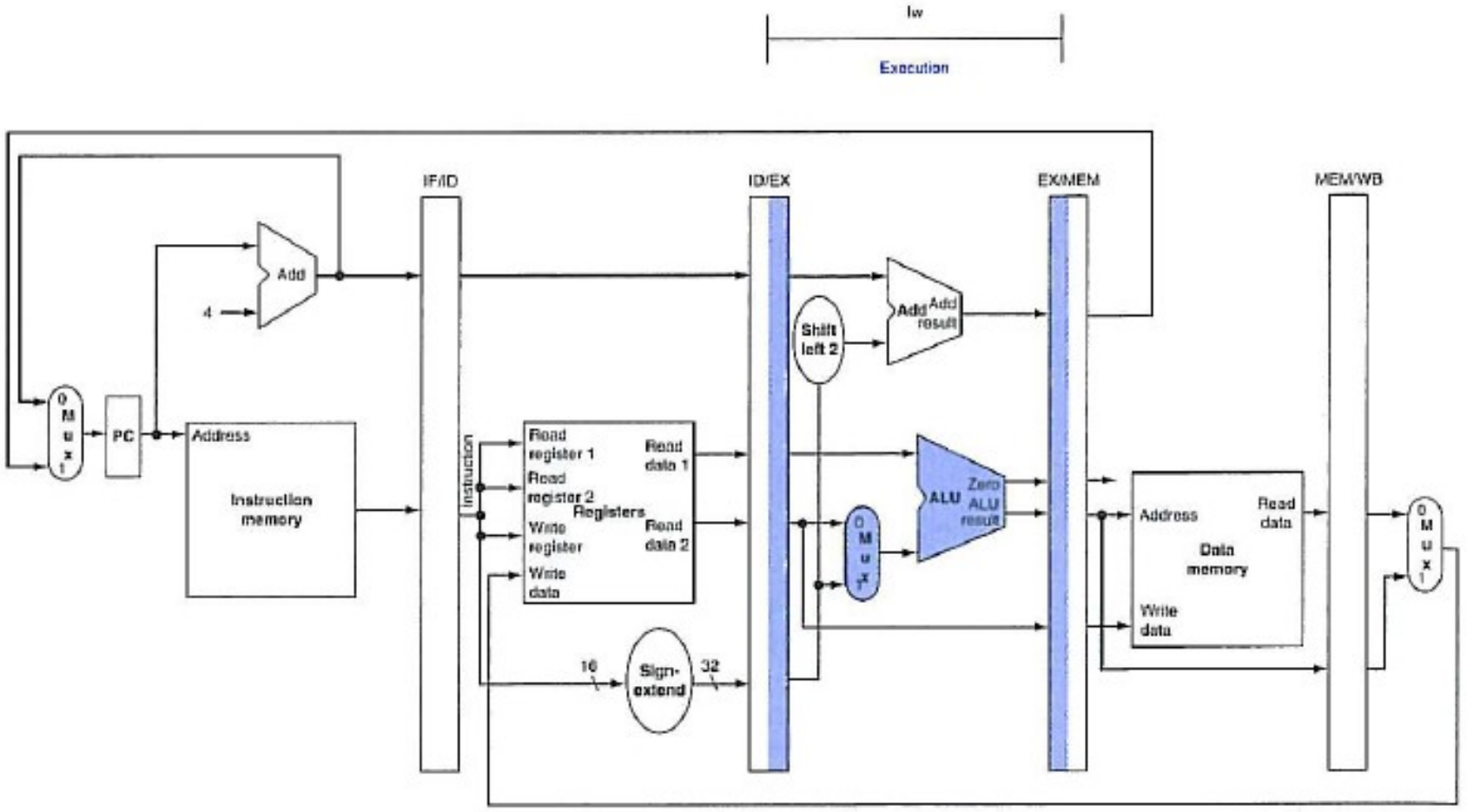
DATA PATH Y CONTROL DEL PIPELINE 5/26
DATA PATH



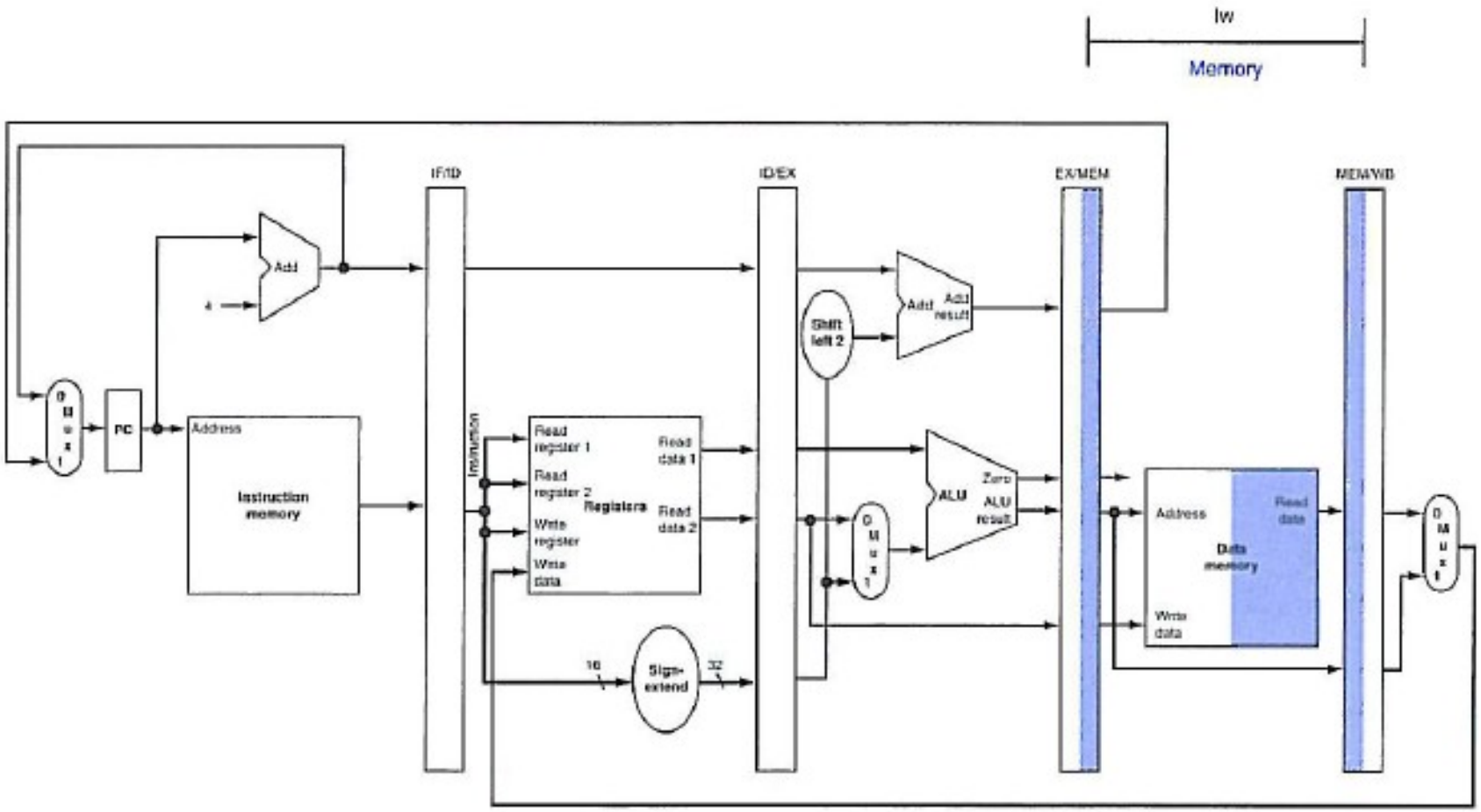
DATA PATH Y CONTROL DEL PIPELINE 6/26
DATA PATH



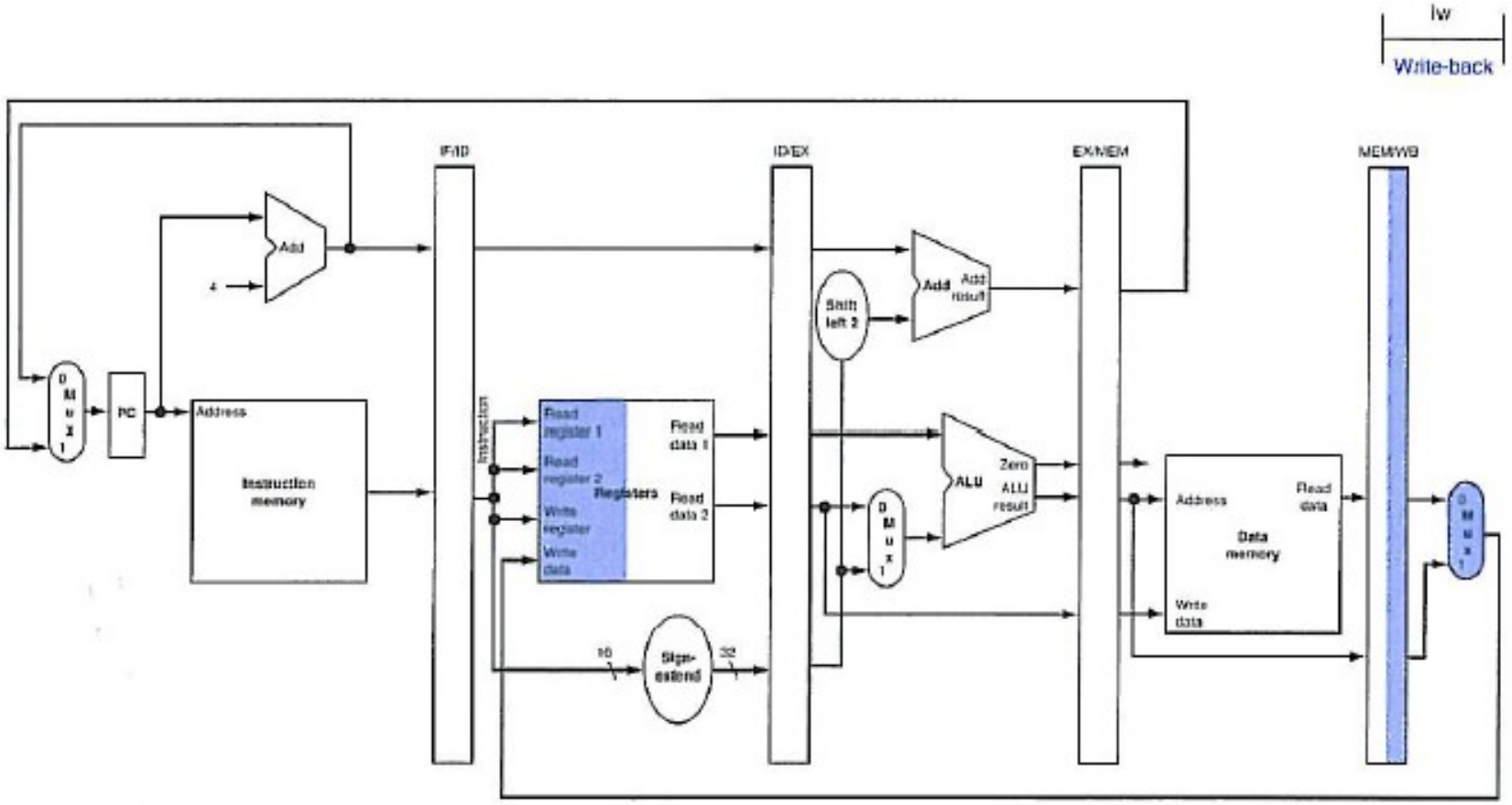
DATA PATH Y CONTROL DEL PIPELINE 7/26
DATA PATH



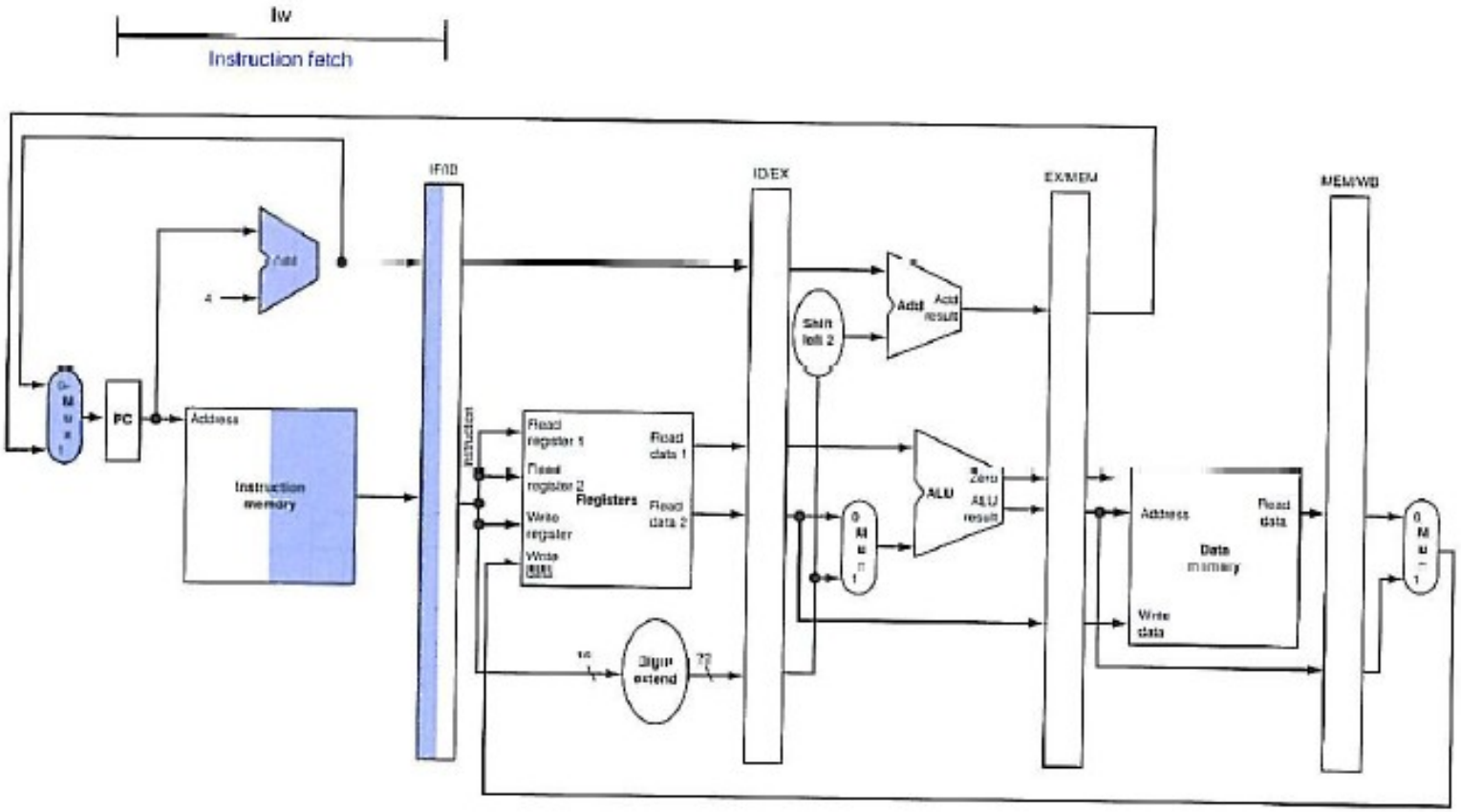
DATA PATH Y CONTROL DEL PIPELINE 8/26
DATA PATH



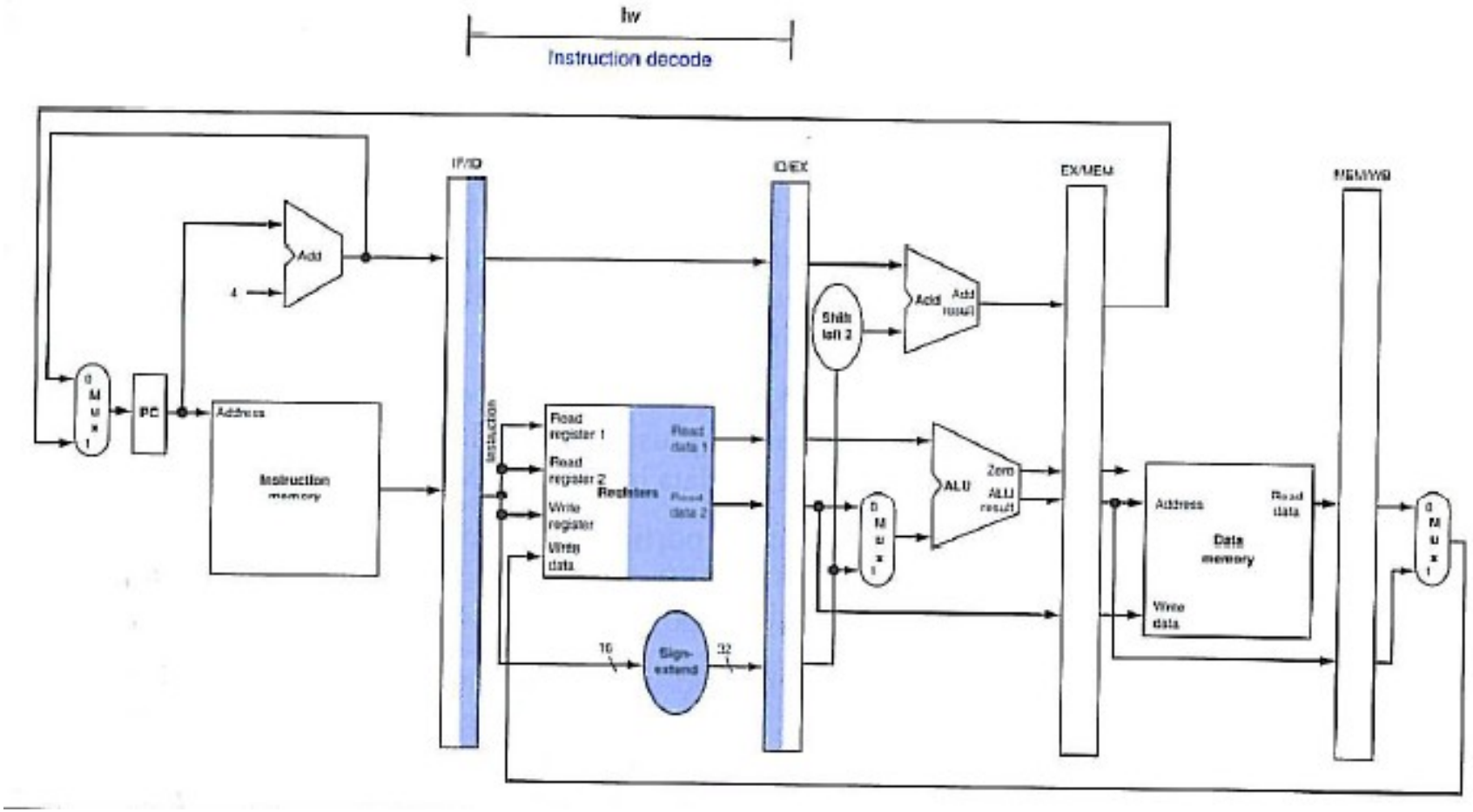
DATA PATH Y CONTROL DEL PIPELINE 9/26
DATA PATH



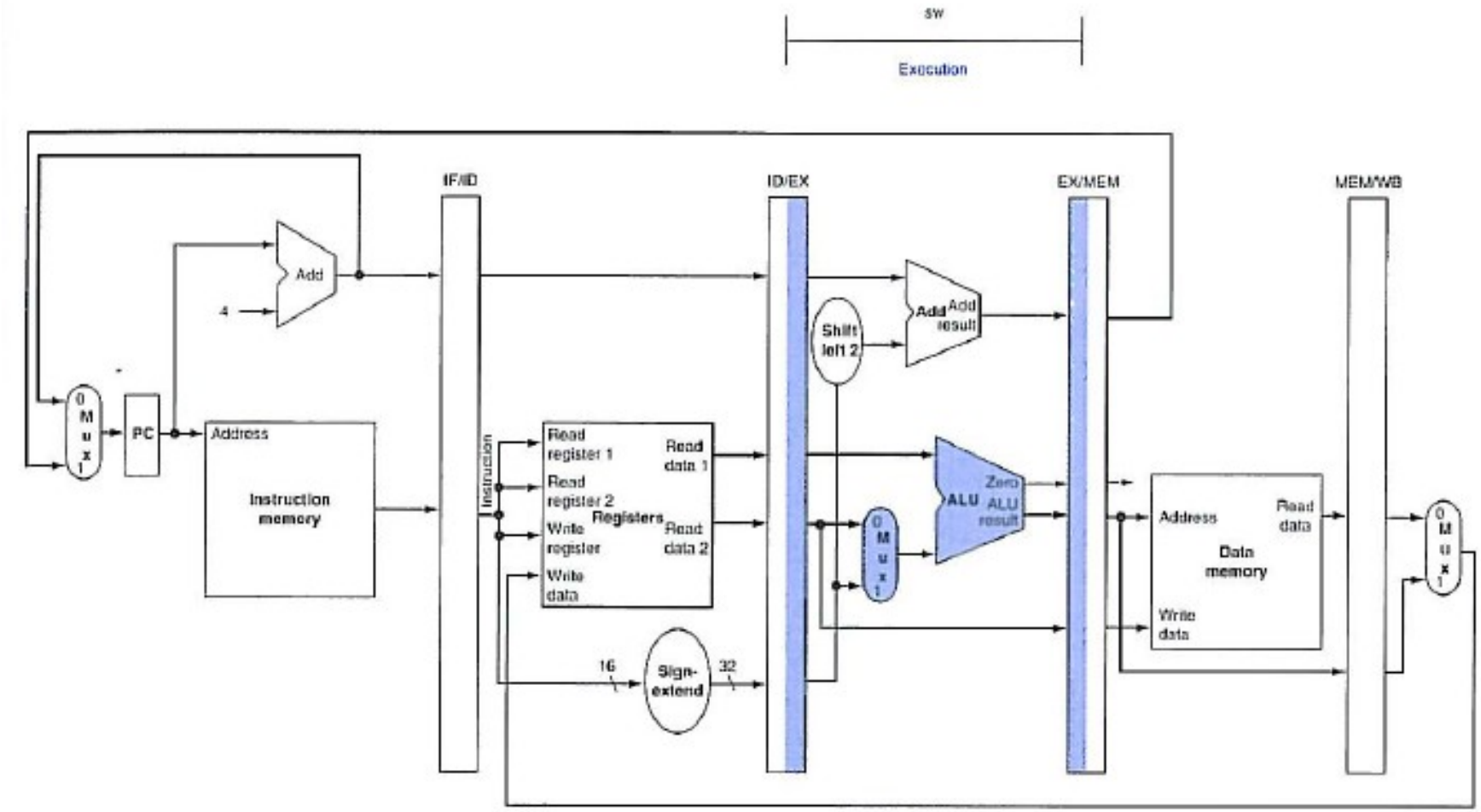
DATA PATH Y CONTROL DEL PIPELINE 10/26
DATA PATH



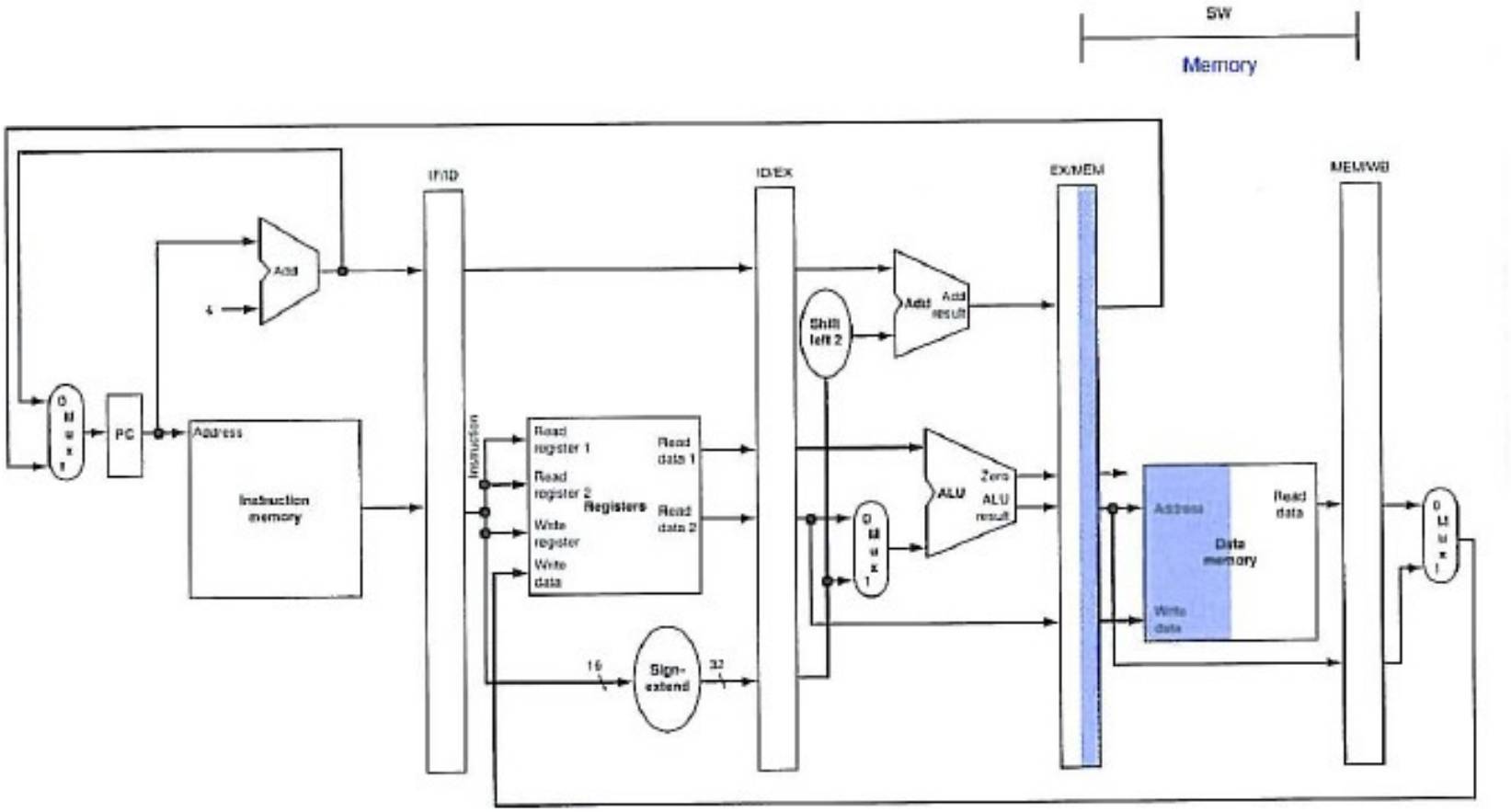
DATA PATH Y CONTROL DEL PIPELINE 11/26
DATA PATH



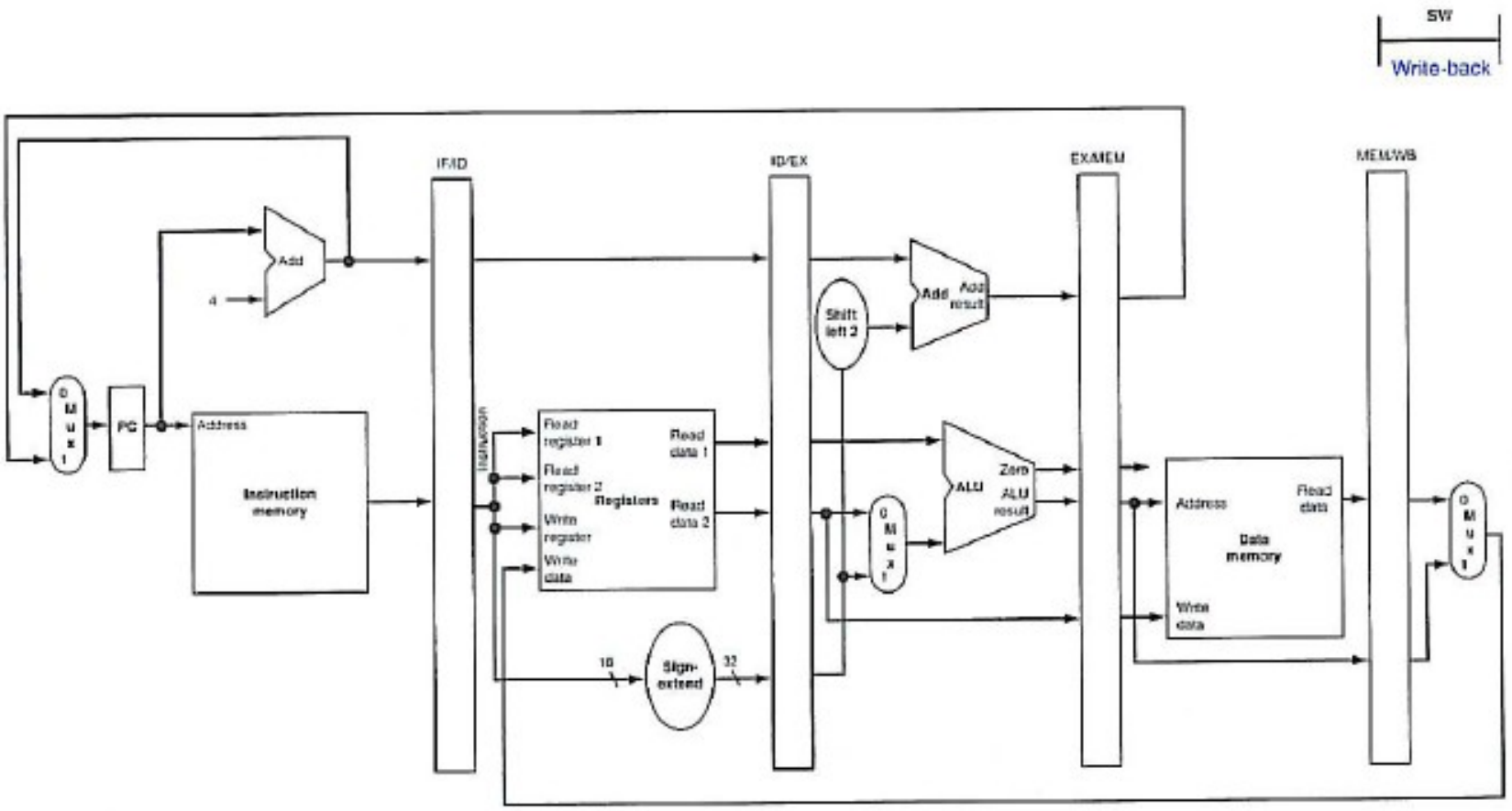
DATA PATH Y CONTROL DEL PIPELINE 12/26
DATA PATH



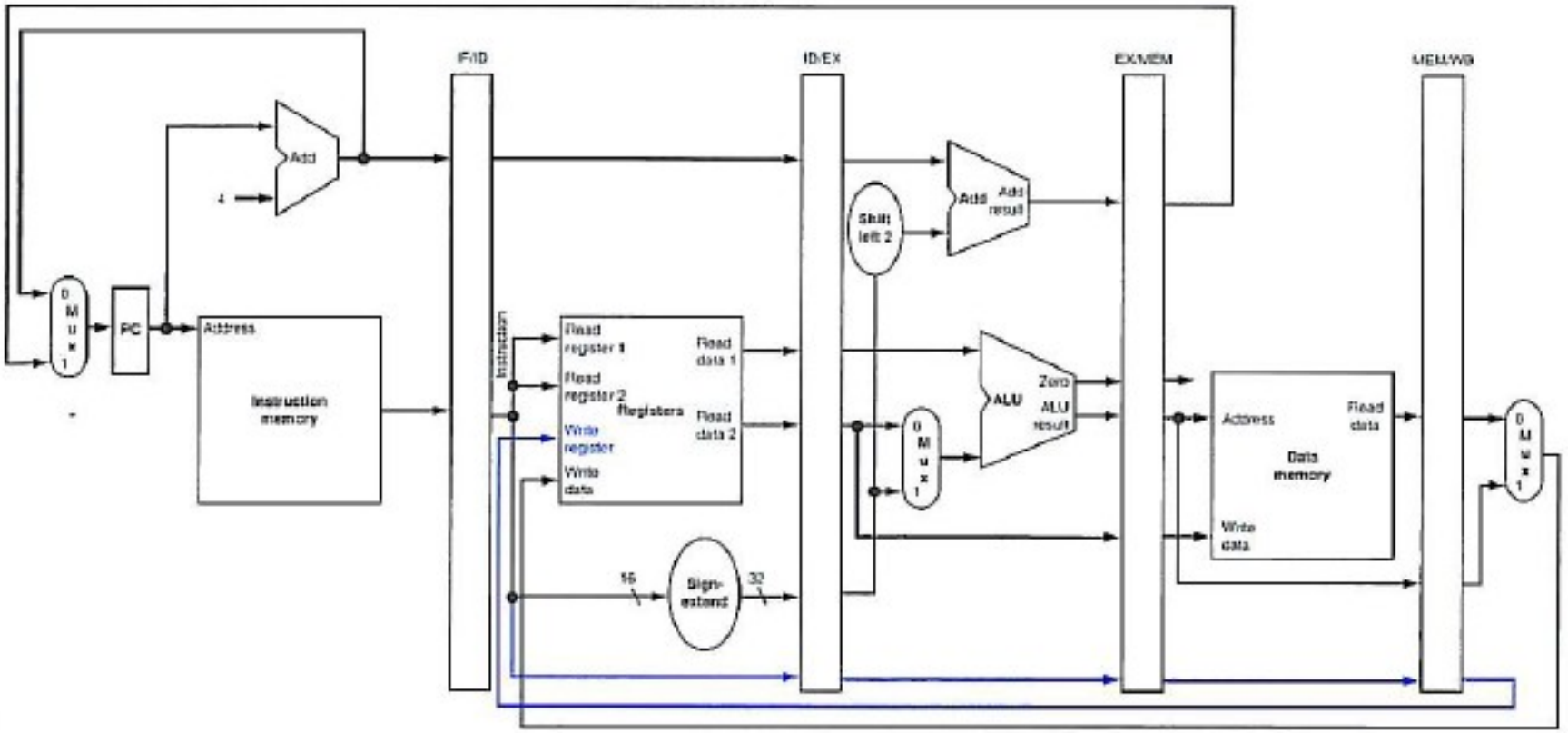
DATA PATH Y CONTROL DEL PIPELINE 13/26
DATA PATH



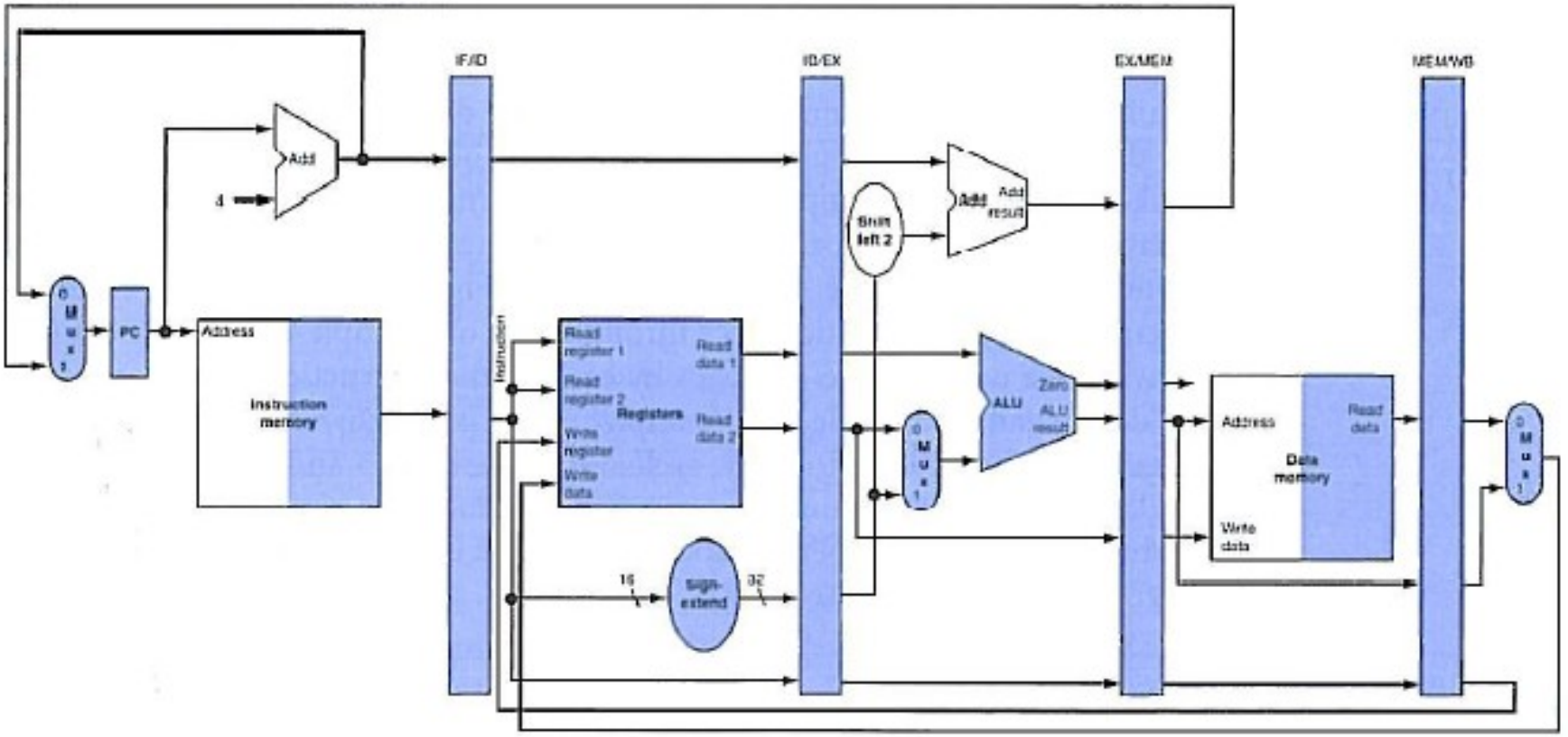
DATA PATH Y CONTROL DEL PIPELINE 14/26
DATA PATH



DATA PATH Y CONTROL DEL PIPELINE 15/26
DATA PATH CORRECTO



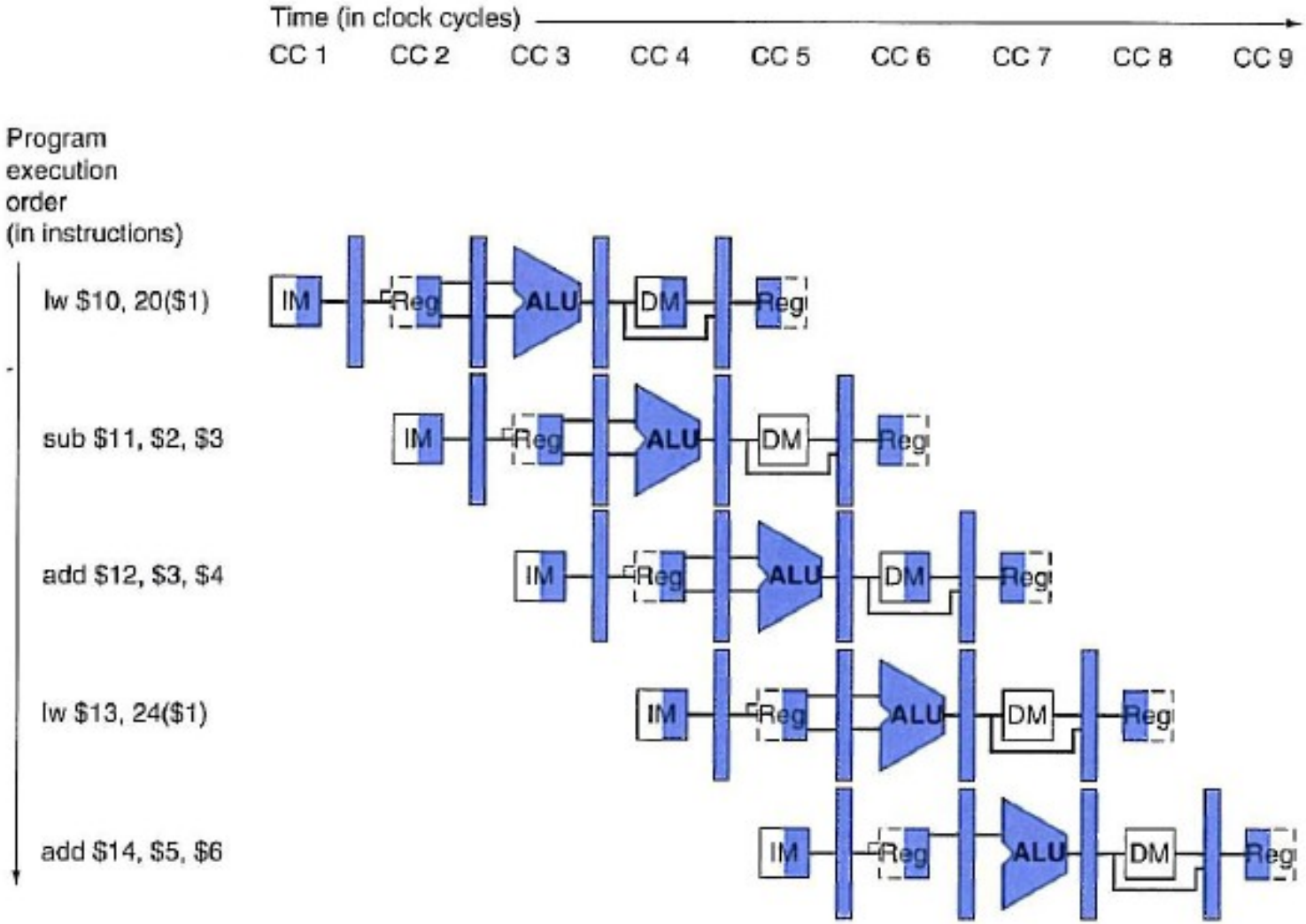
DATA PATH Y CONTROL DEL PIPELINE 16/26
DATA PATH



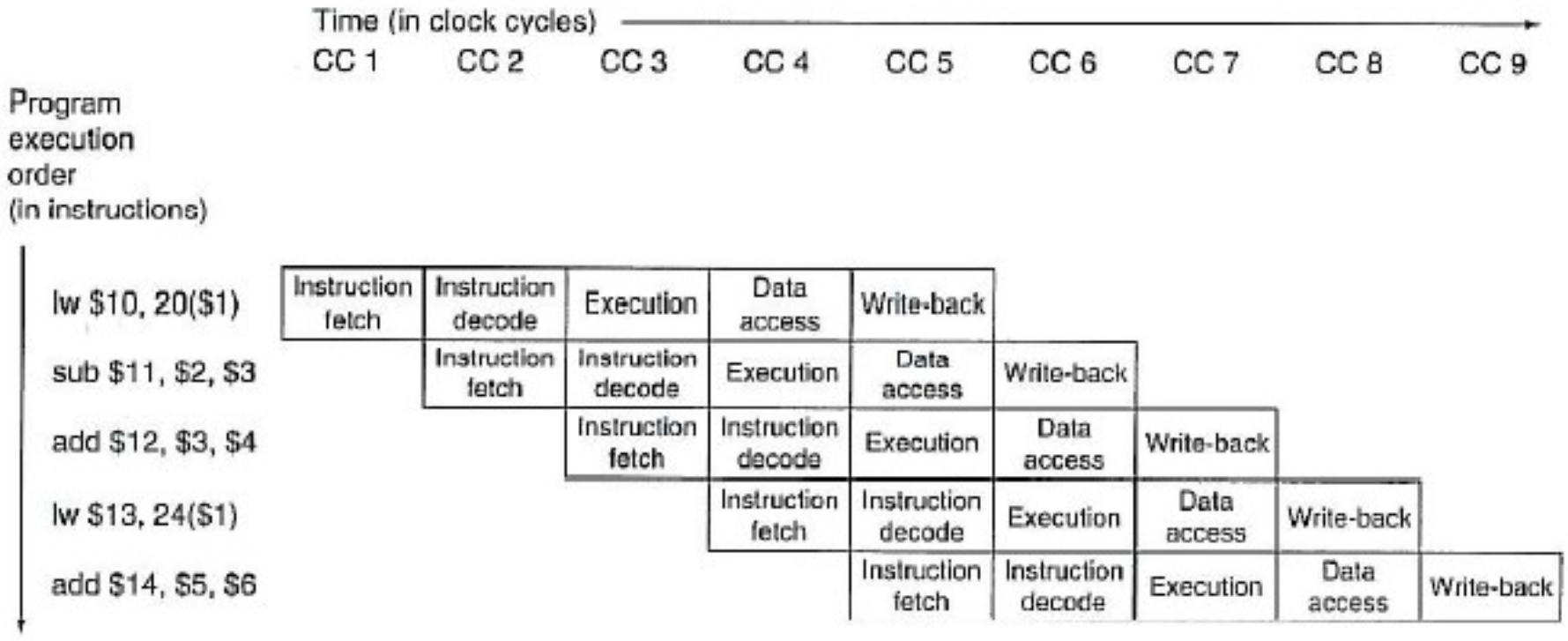
DATA PATH Y CONTROL DEL PIPELINE 17/26
REPRESENTACIÓN GRÁFICA

```
lw      $10, 20($1)
sub     $11, $2, $3
add     $12, $3, $4
lw      $13, 24($1)
add     $14, $5, $6
```

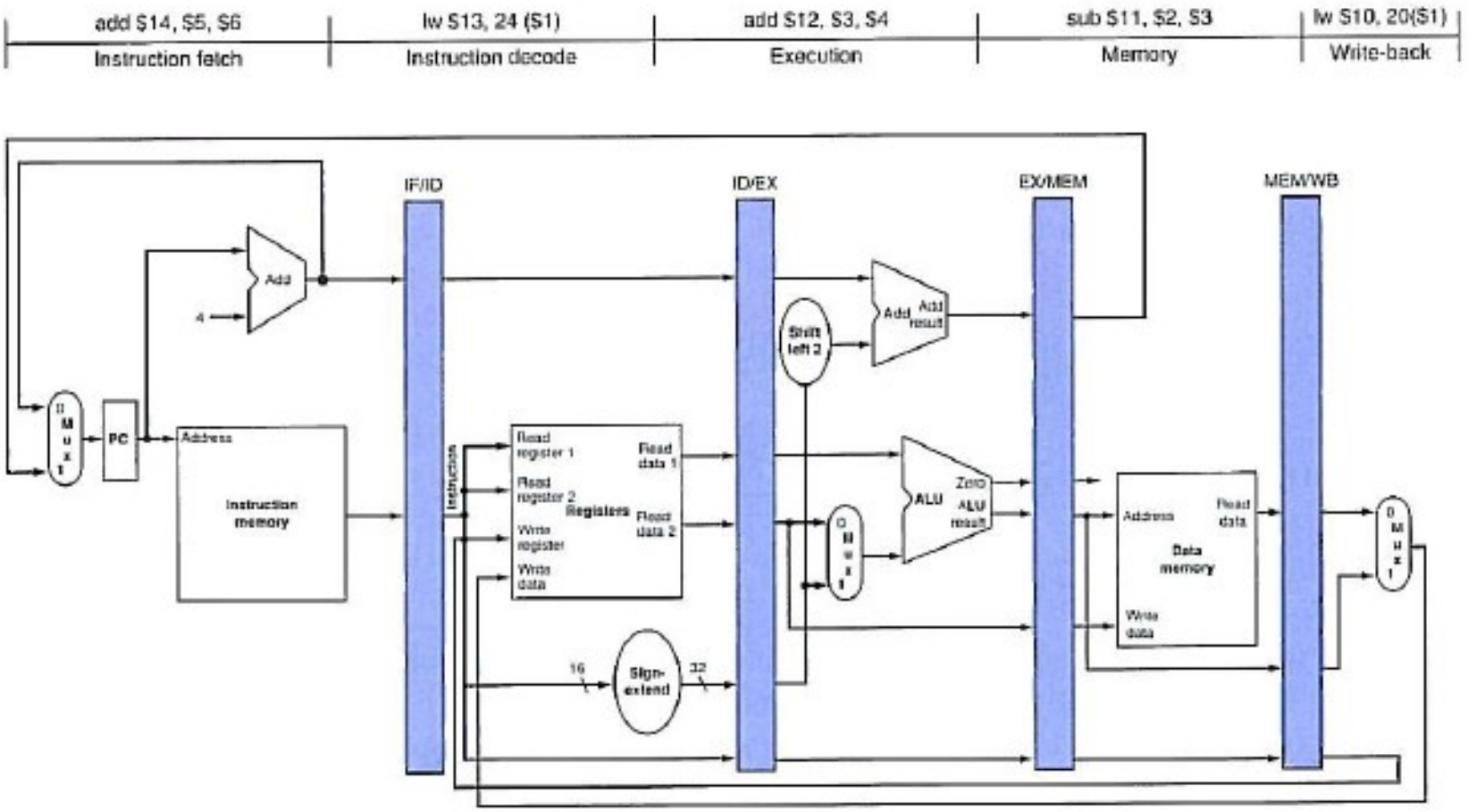
DATA PATH Y CONTROL DEL PIPELINE 18/26
REPRESENTACIÓN GRÁFICA



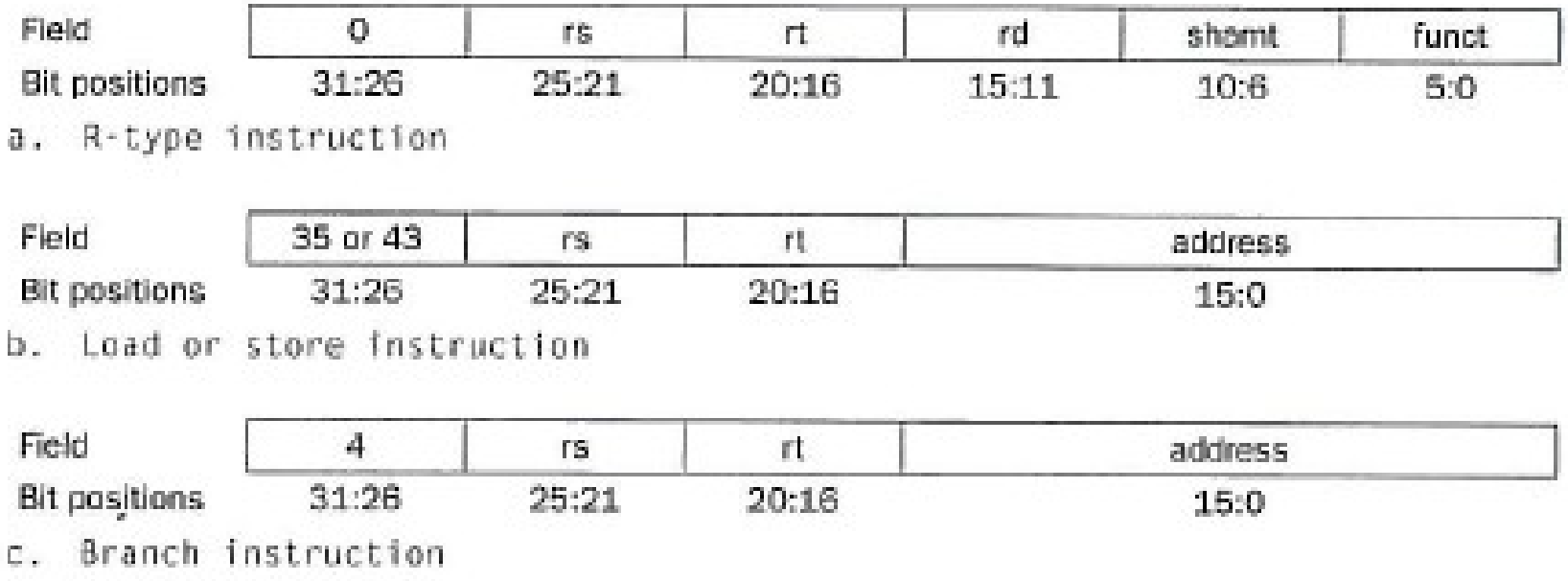
DATA PATH Y CONTROL DEL PIPELINE 19/26
REPRESENTACIÓN GRÁFICA



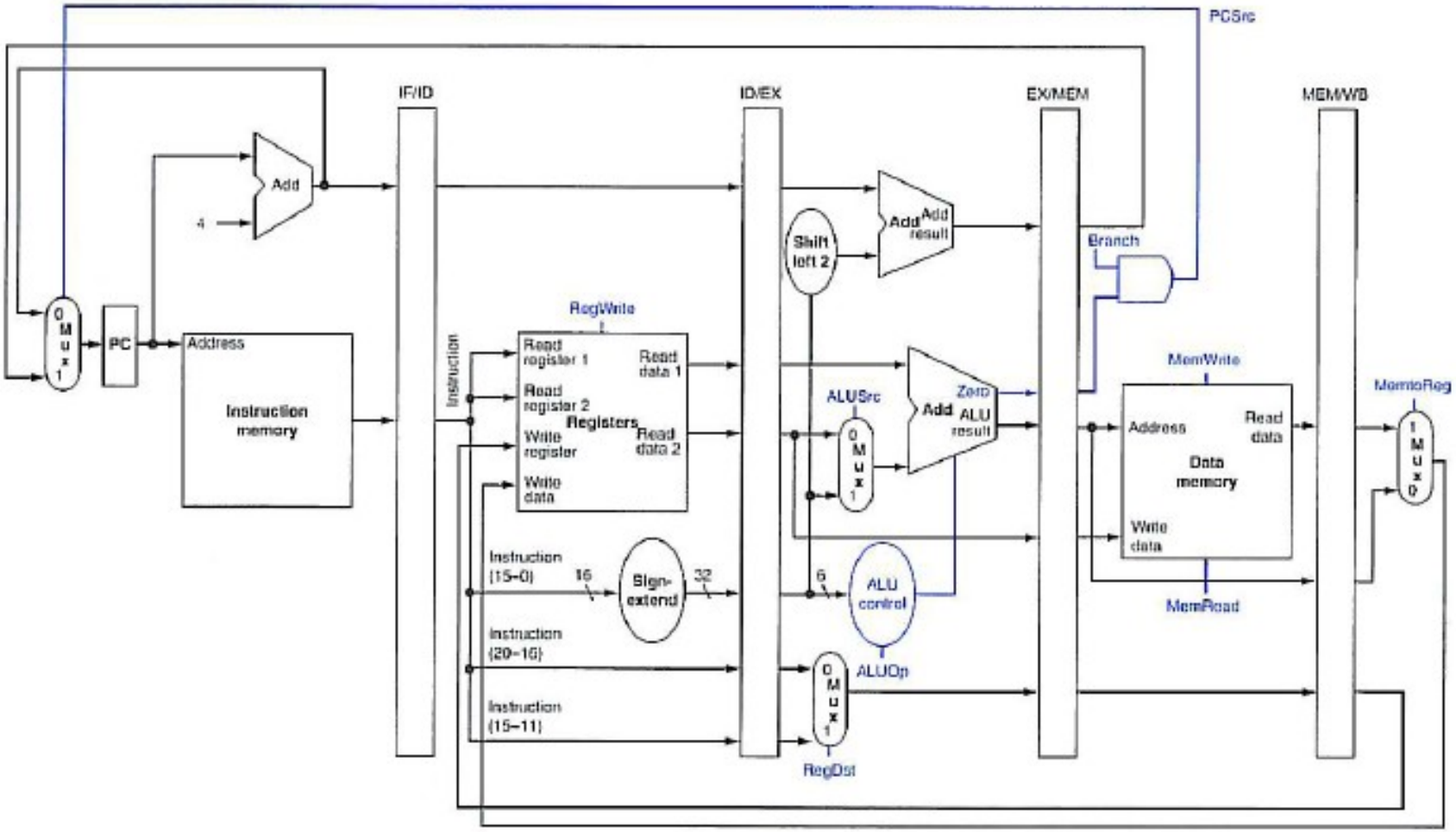
DATA PATH Y CONTROL DEL PIPELINE 20/26 REPRESENTACIÓN GRÁFICA



DATA PATH Y CONTROL DEL PIPELINE 20/26
CONTROL DEL PIPELINE



DATA PATH Y CONTROL DEL PIPELINE 20/26
CONTROL DEL PIPELINE



DATA PATH Y CONTROL DEL PIPELINE 21/26
CONTROL DEL PIPELINE

Instruction opcode	ALUOp	Instruction operation	Function code	Desired ALU action	ALU control input
LW	00	load word	XXXXXX	add	0010
SW	00	store word	XXXXXX	add	0010
Branch equal	01	branch equal	XXXXXX	subtract	0110
R-type	10	add	100000	add	0010
R-type	10	subtract	100010	subtract	0110
R-type	10	AND	100100	AND	0000
R-type	10	OR	100101	OR	0001
R-type	10	set on less than	101010	set on less than	0111

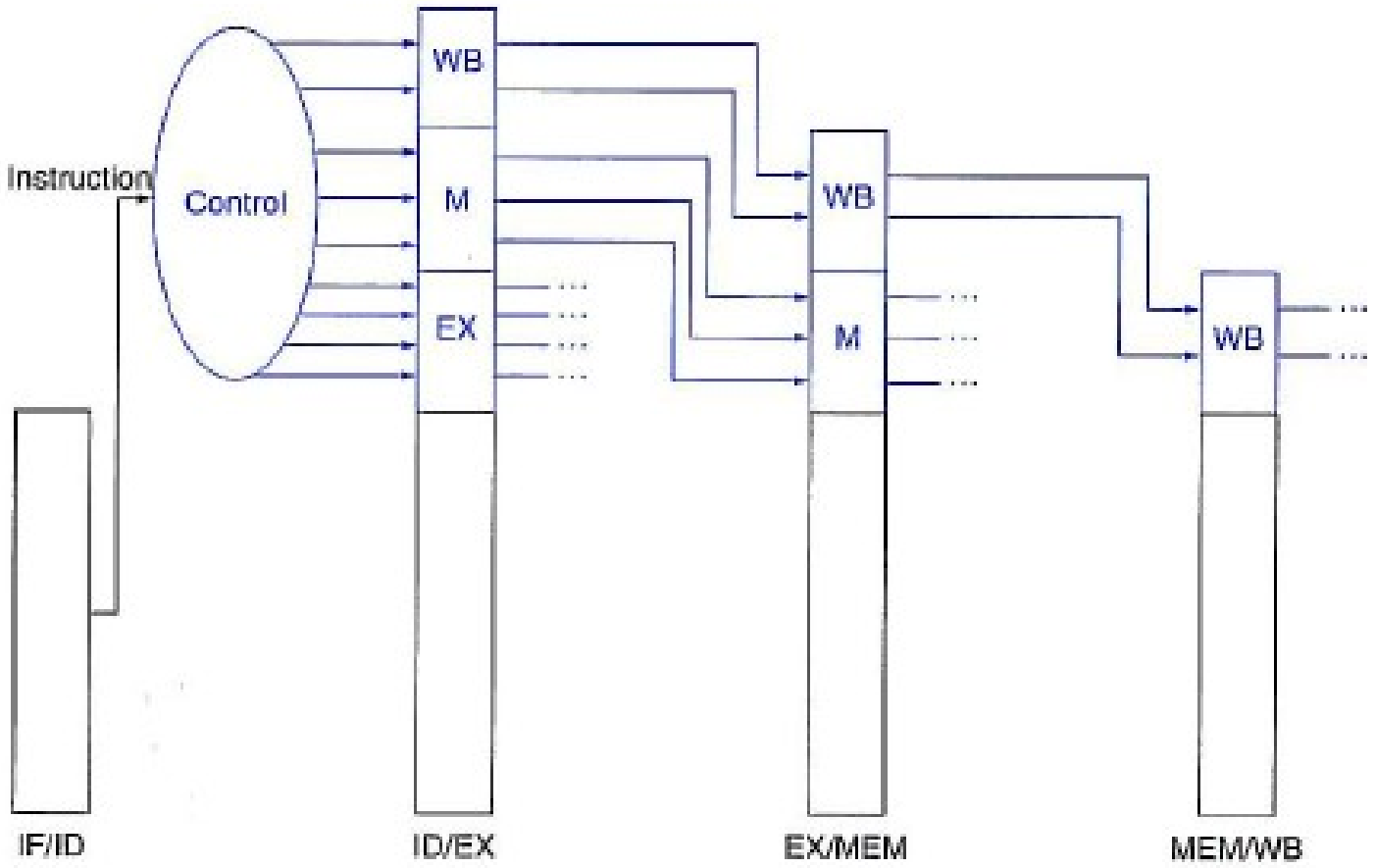
DATA PATH Y CONTROL DEL PIPELINE 22/26
CONTROL DEL PIPELINE

Signal name	Effect when deasserted (0)	Effect when asserted (1)
RegDst	The register destination number for the Write register comes from the rt field (bits 20:16).	The register destination number for the Write register comes from the rd field (bits 15:11).
RegWrite	None.	The register on the Write register input is written with the value on the Write data input.
ALUSrc	The second ALU operand comes from the second register file output (Read data 2).	The second ALU operand is the sign-extended, lower 16 bits of the instruction.
PCSrc	The PC is replaced by the output of the adder that computes the value of PC + 4.	The PC is replaced by the output of the adder that computes the branch target.
MemRead	None.	Data memory contents designated by the address input are put on the Read data output.
MemWrite	None.	Data memory contents designated by the address input are replaced by the value on the Write data input.
MemtoReg	The value fed to the register Write data input comes from the ALU.	The value fed to the register Write data input comes from the data memory.

DATA PATH Y CONTROL DEL PIPELINE 23/26
CONTROL DEL PIPELINE

Instruction	Execution/address calculation stage control lines				Memory access stage control lines			Write-back stage control lines	
	RegDst	ALUOp1	ALUOp0	ALUSrc	Branch	Mem-Read	Mem-Write	Reg-Write	Memto-Reg
R-format	1	1	0	0	0	0	0	1	0
lw	0	0	0	1	0	1	0	1	1
sw	X	0	0	1	0	0	1	0	X
beq	X	0	1	0	1	0	0	0	X

DATA PATH Y CONTROL DEL PIPELINE 24/26
CONTROL DEL PIPELINE



DATA PATH Y CONTROL DEL PIPELINE 25/26
CONTROL DEL PIPELINE