Lab 3

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Summary

In this lab, I learned how to do parasitic extractions of layouts by running LPE on Custom Designer. I also learned how to design a ring oscillator using hierarchical design. I learned how to connect the inverters to create the ring oscillator and gained more familiarity with running DRC and LVS to verify layouts. Next, I learned how to create a layout from a schematic and designed a layout for a 1-bit full adder and then a 4-bit full adder using hierarchical design. A large part of this lab was practicing debugging with the DRC and LVS as well.

Checkoff Video

Week 1: https://youtu.be/SzEygGEC7ds
Week 2&3: https://youtu.be/3hqnZoSdNoU

Images

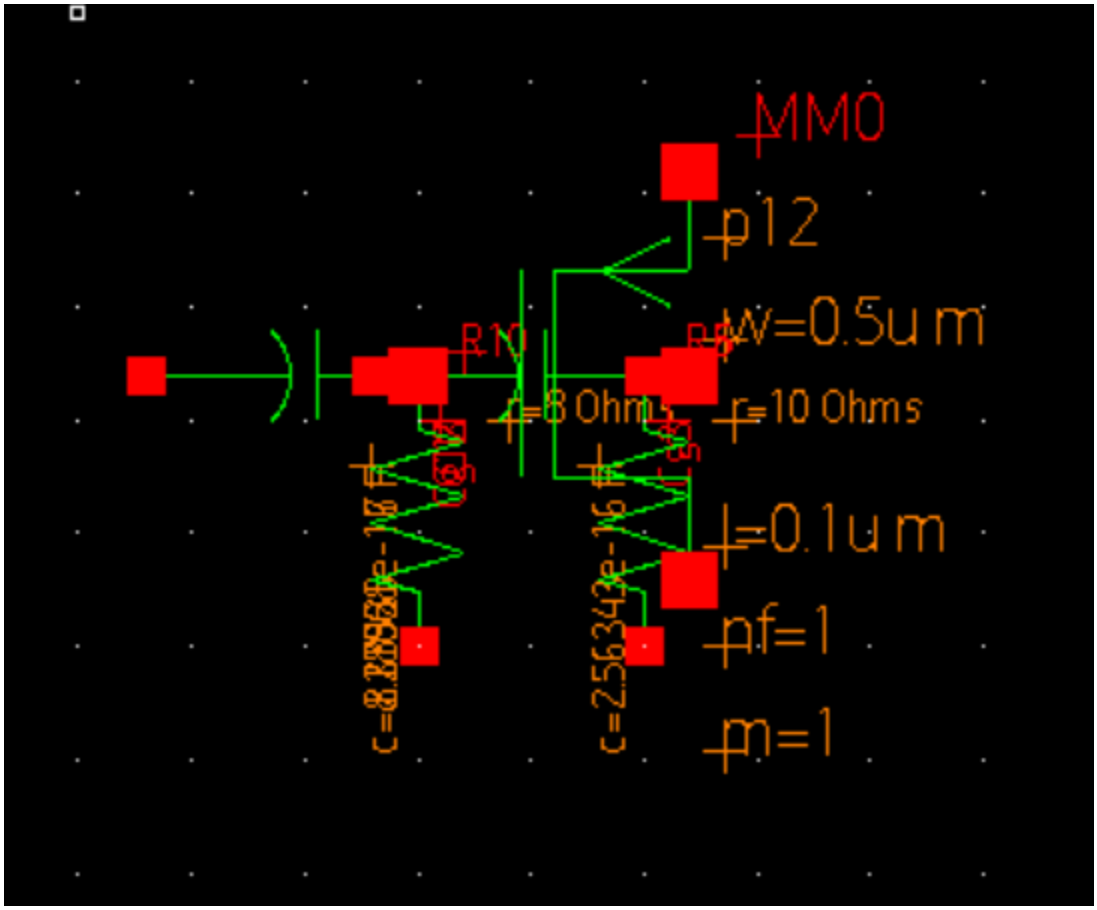

Figure 1. Inverter parasitic view

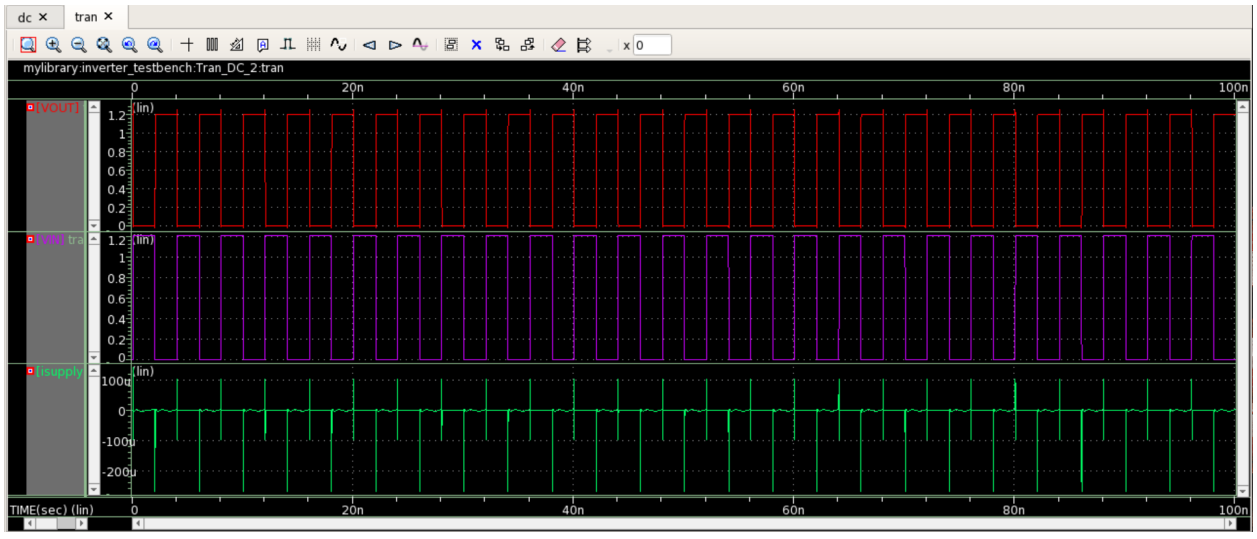

Figure 2. Your post simulation result

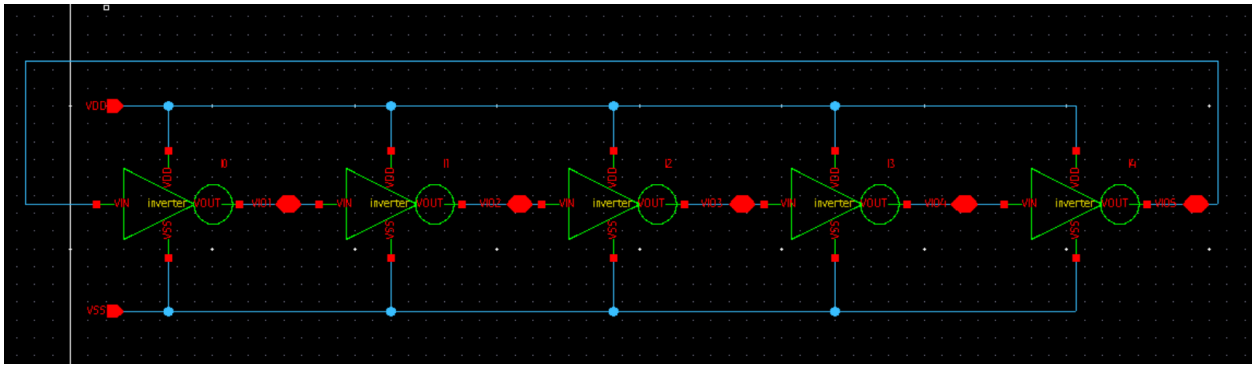

Figure 3. Ring oscillator with Hierarchical design

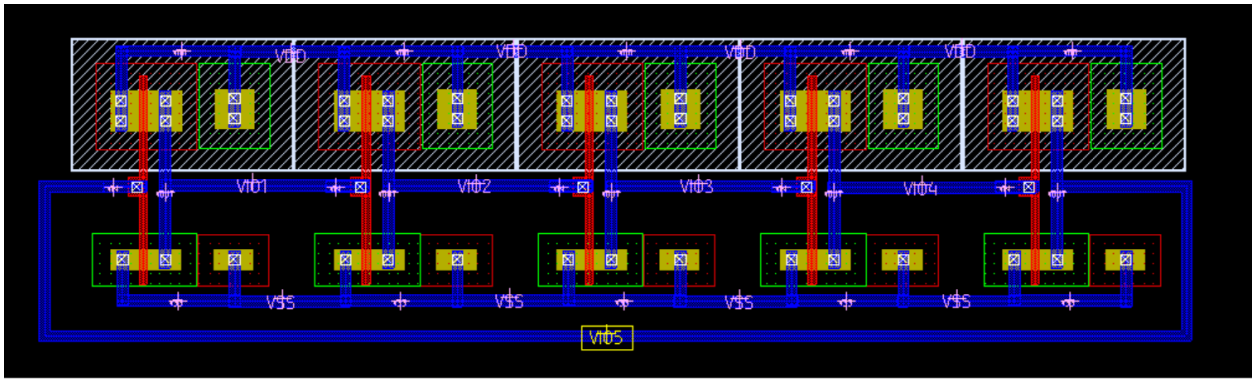

Figure 4. Ring oscillator layout

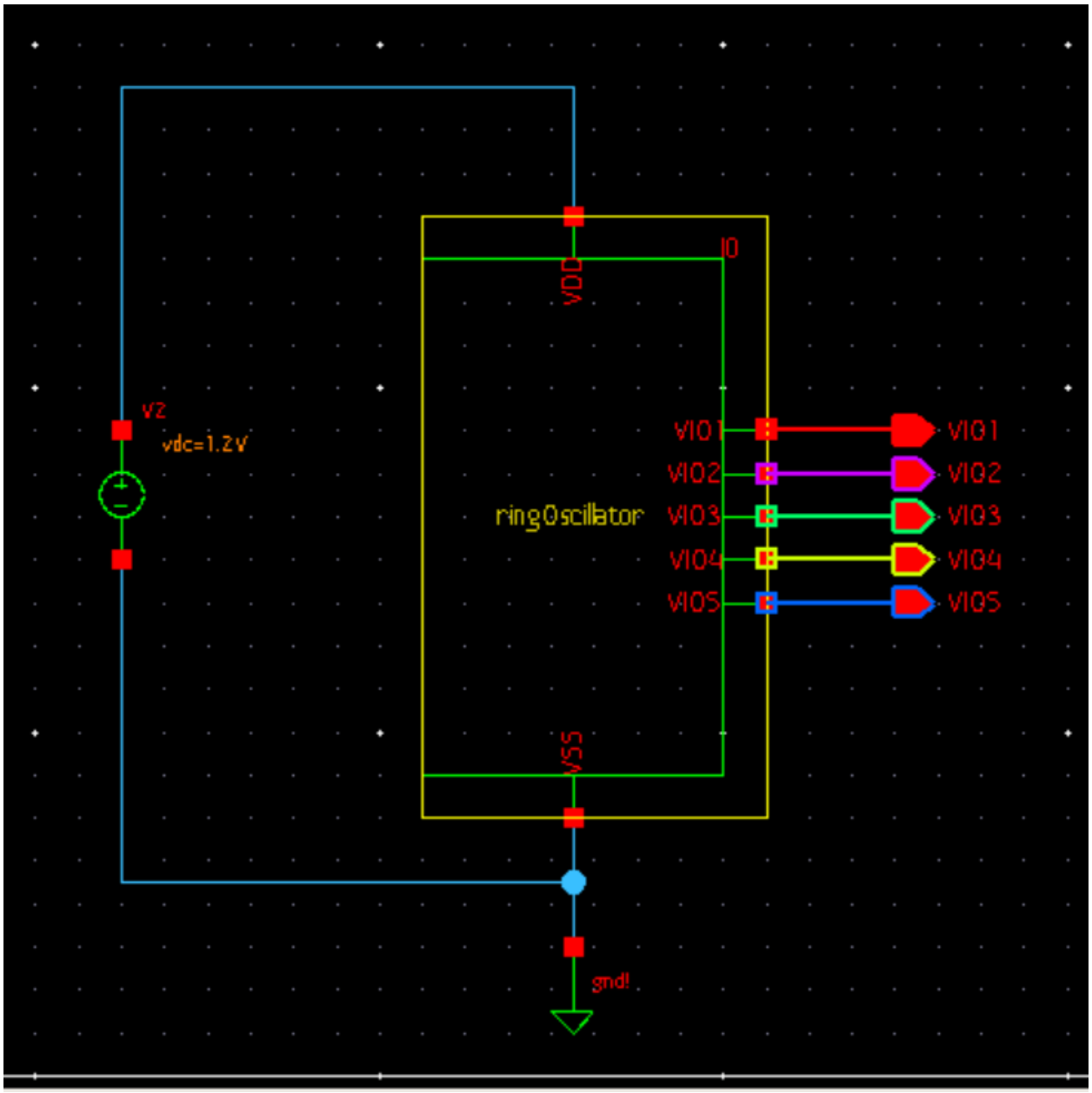

Figure 5. Ring Oscillator Testbench

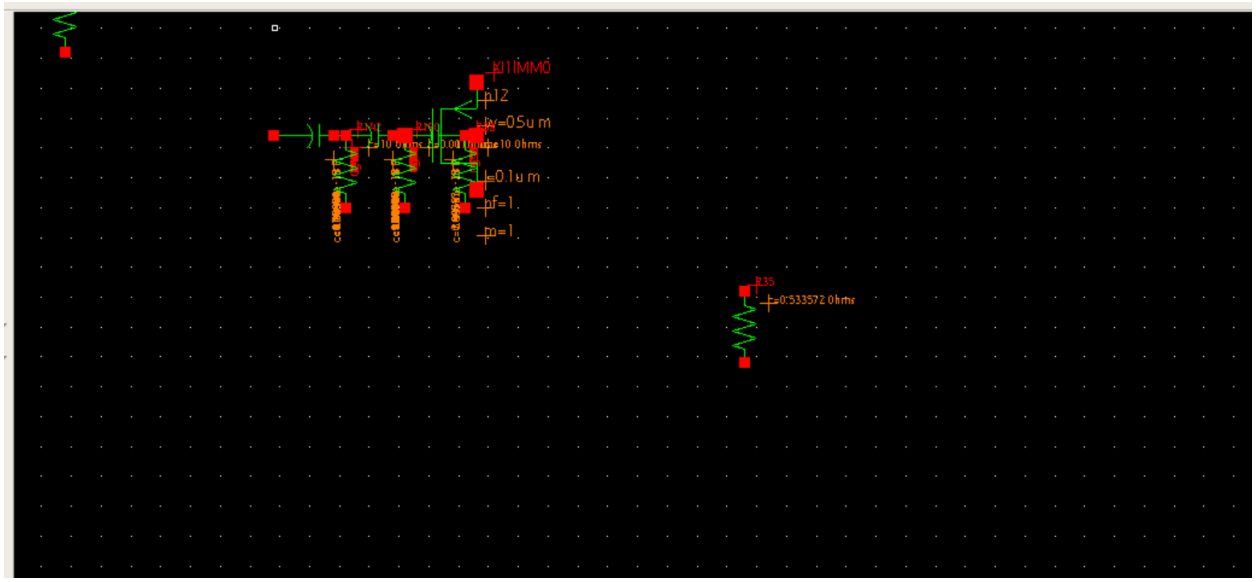

Figure 6. Parasitic Extraction of Ring Oscillator

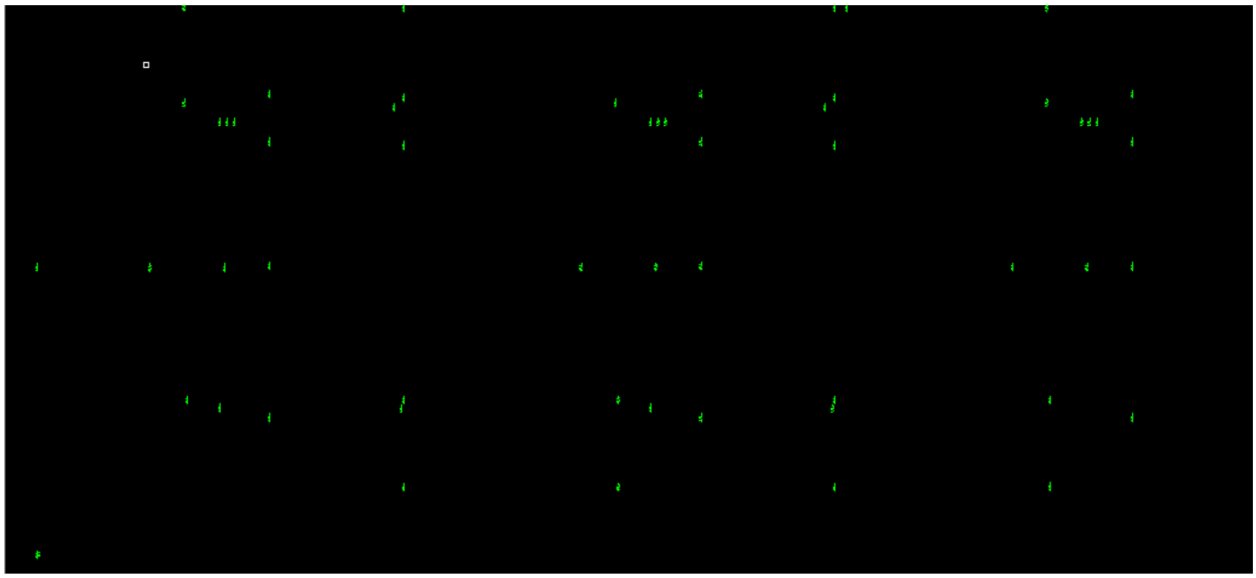

Figure 7. Parasitic Extraction of Ring Oscillator

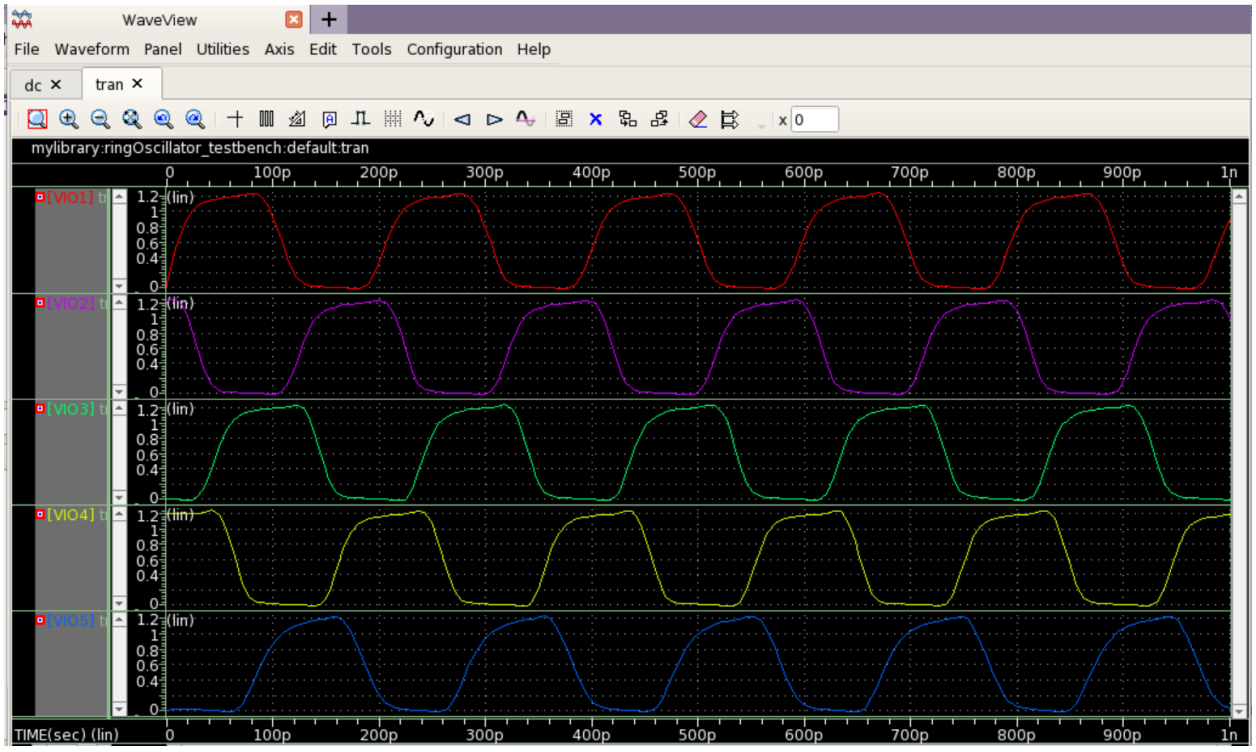

Figure 8. Ring oscillator POST (Layout) SIMULATION result (with parasitic extraction)

Week 2

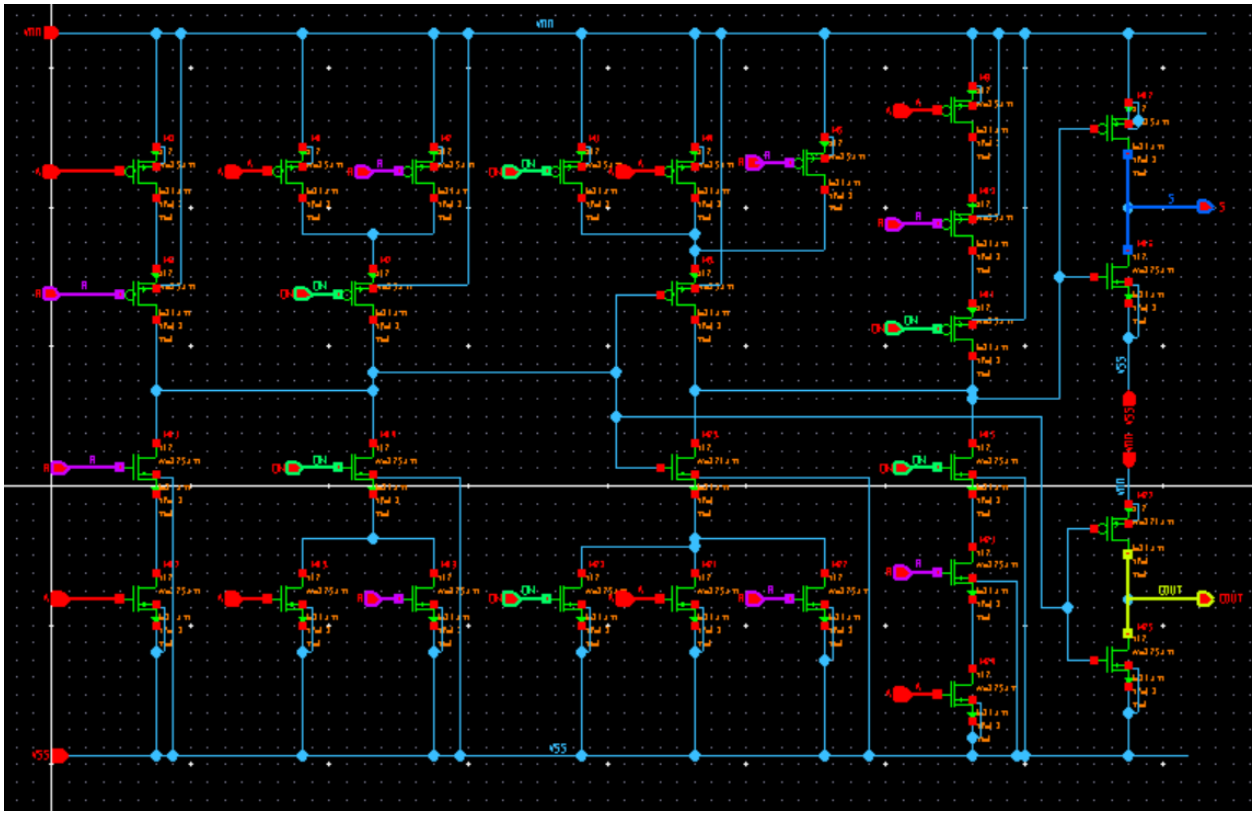

Fig. 9: 1-bit full adder schematic

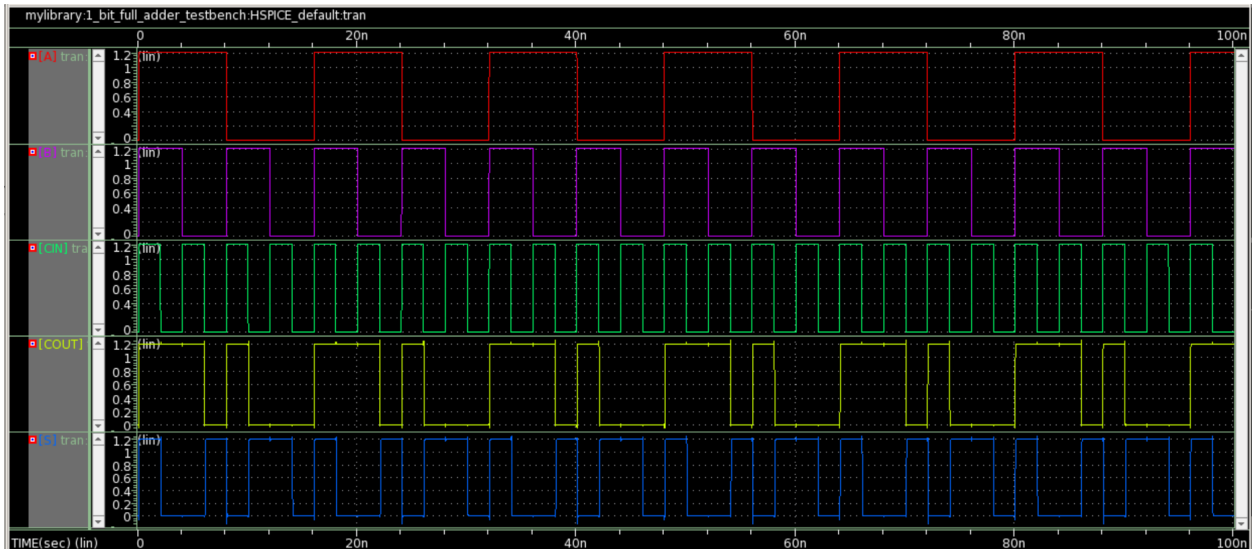

Fig. 10: 1 bit full adder simulation

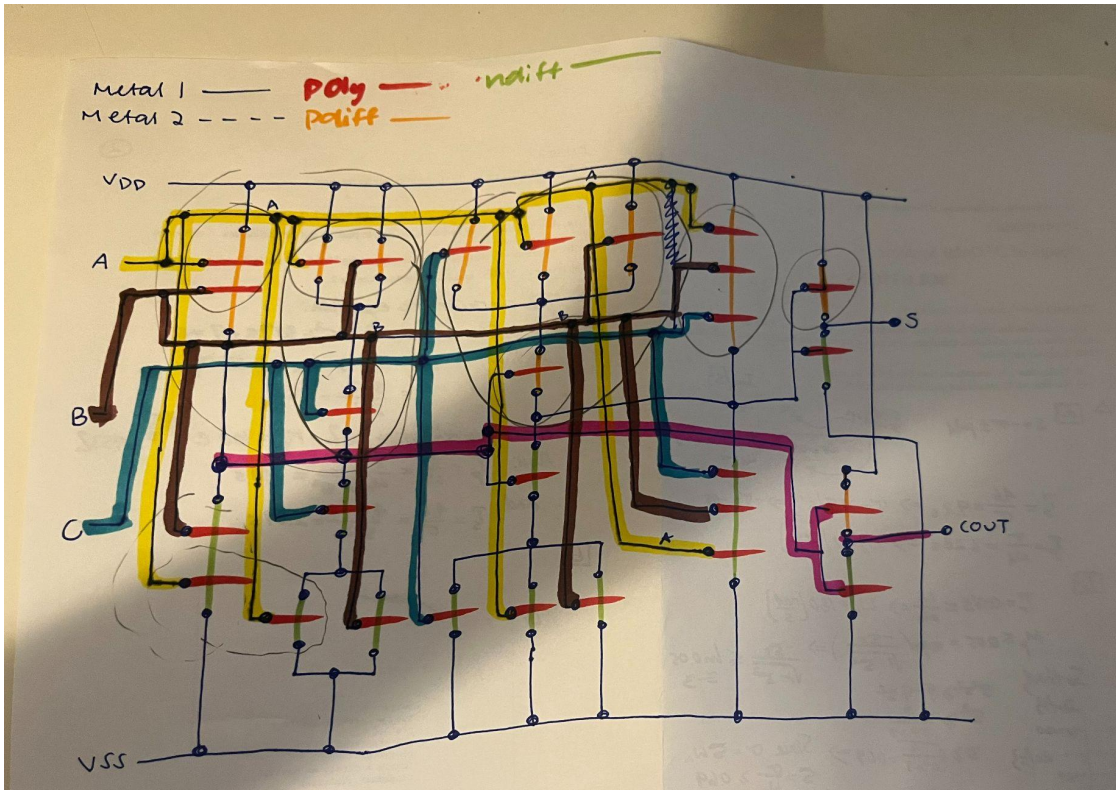

Fig. 11: 1-bit full adder stick diagram

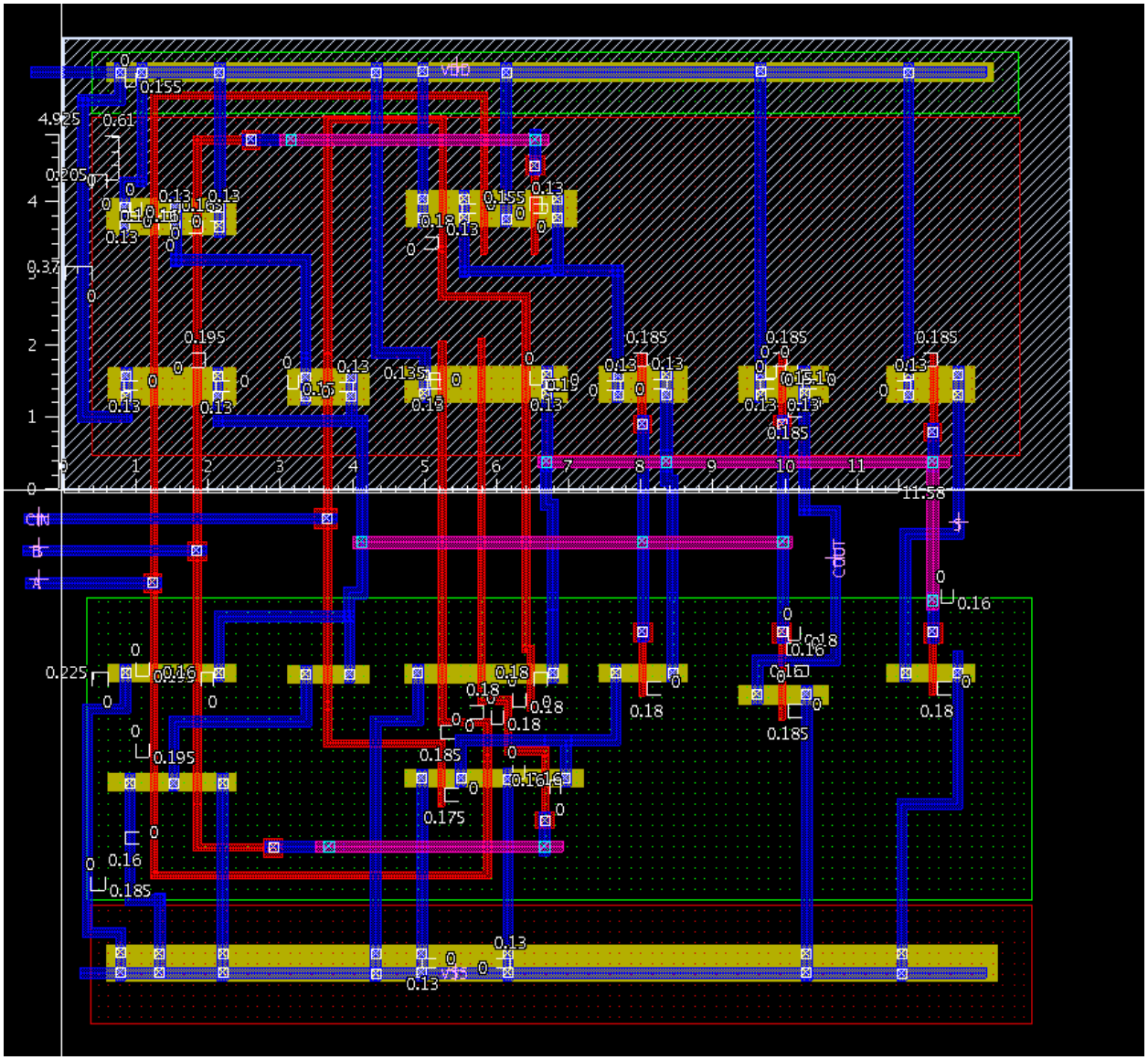

Fig. 12: 1-bit full adder layout

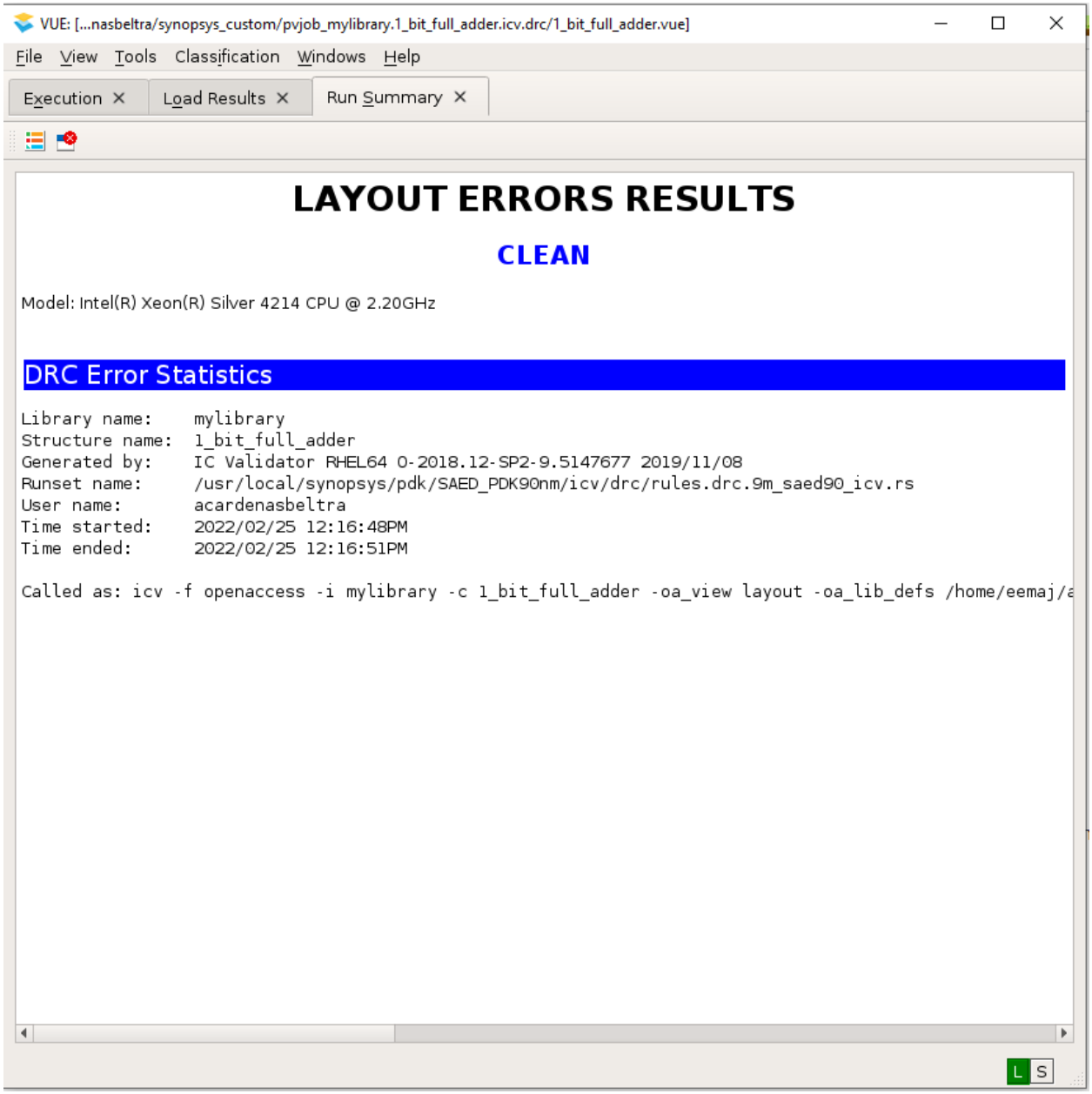

Fig. 13: DRC Result with CLEAN for 1-bit full adder

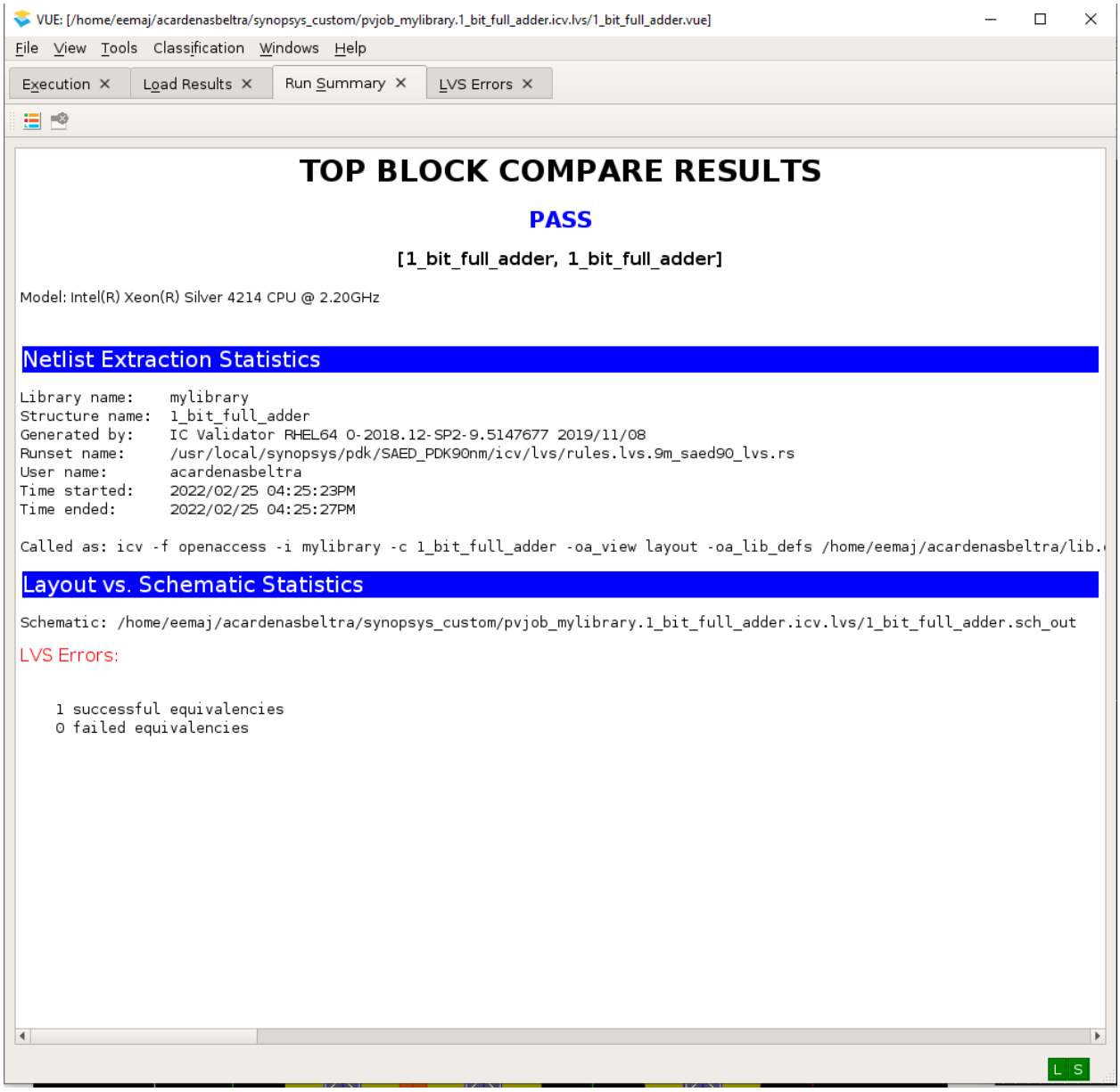

Fig. 14: LVS Result with PASS for 1-bit full adder

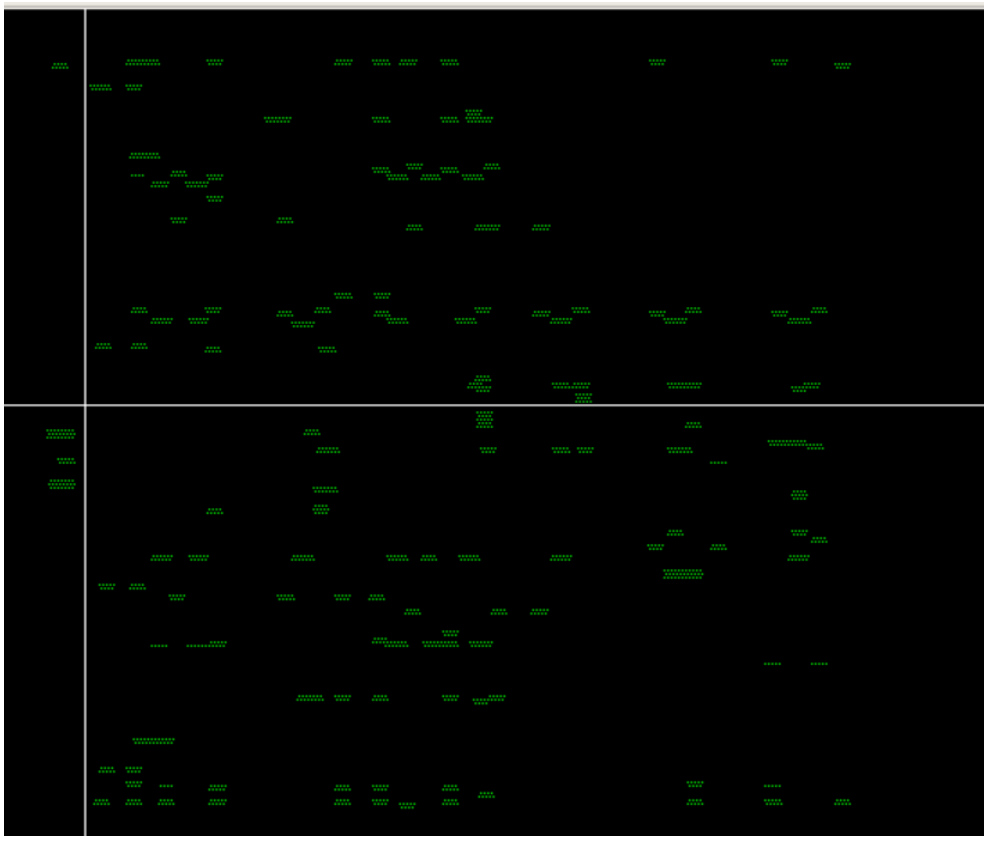

Fig. 15: Parasitic Extraction

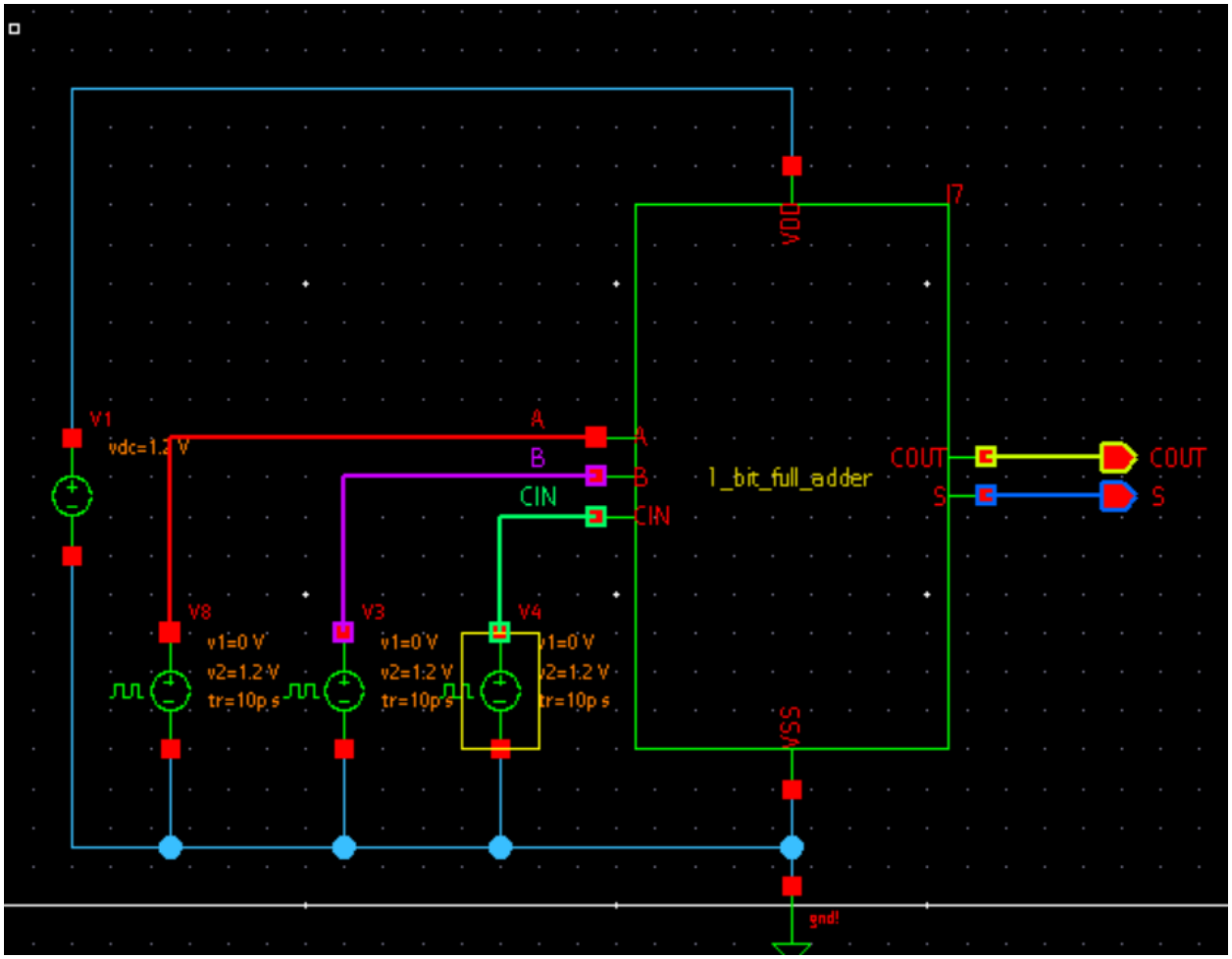

Fig. 16: Fig. 15: 1-bit full adder Post (Layout) Simulation testbench with parasitic extraction

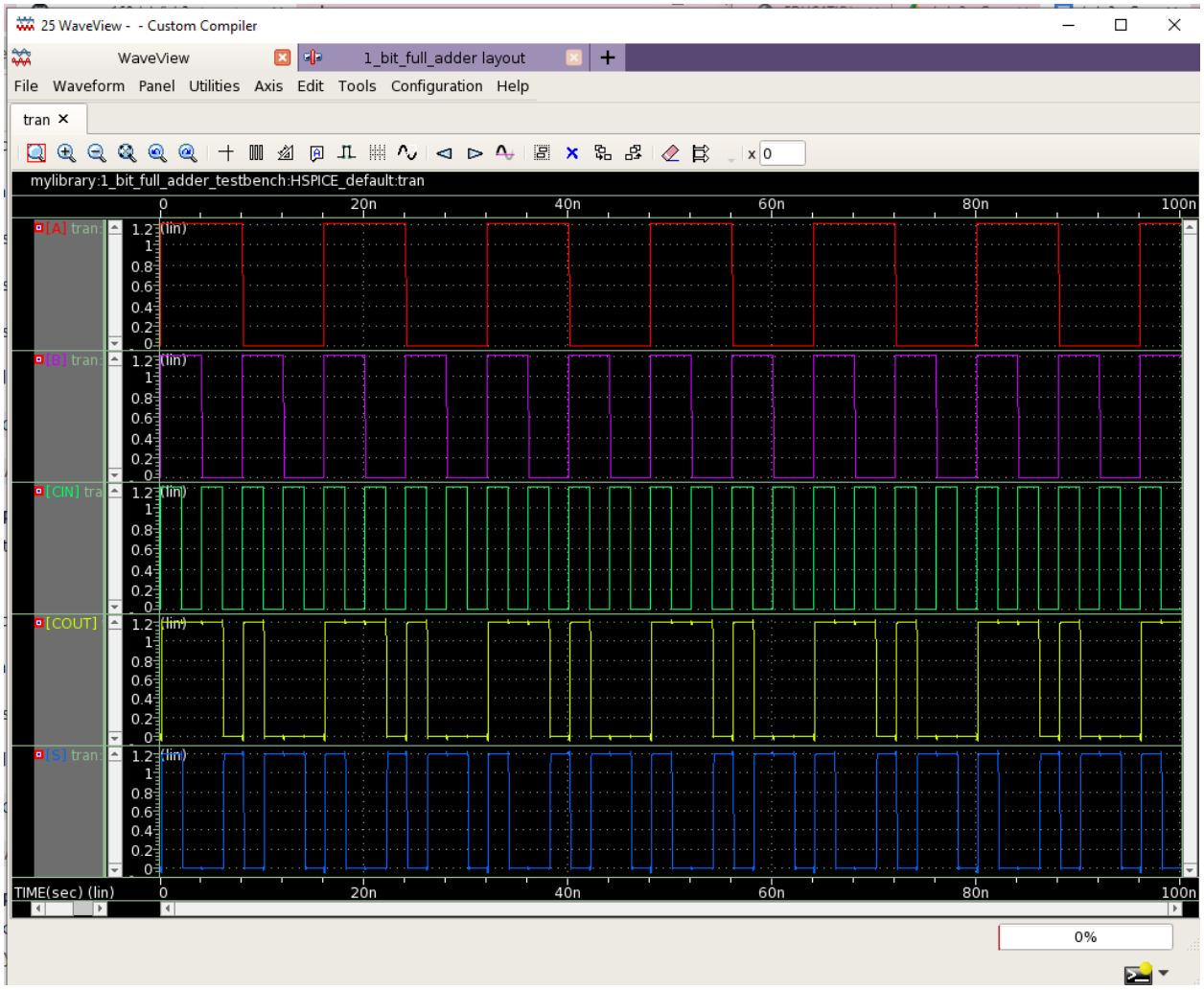

Fig. 17: 1-bit full adder Post (Layout) Simulation result with parasitic extraction

Week 3

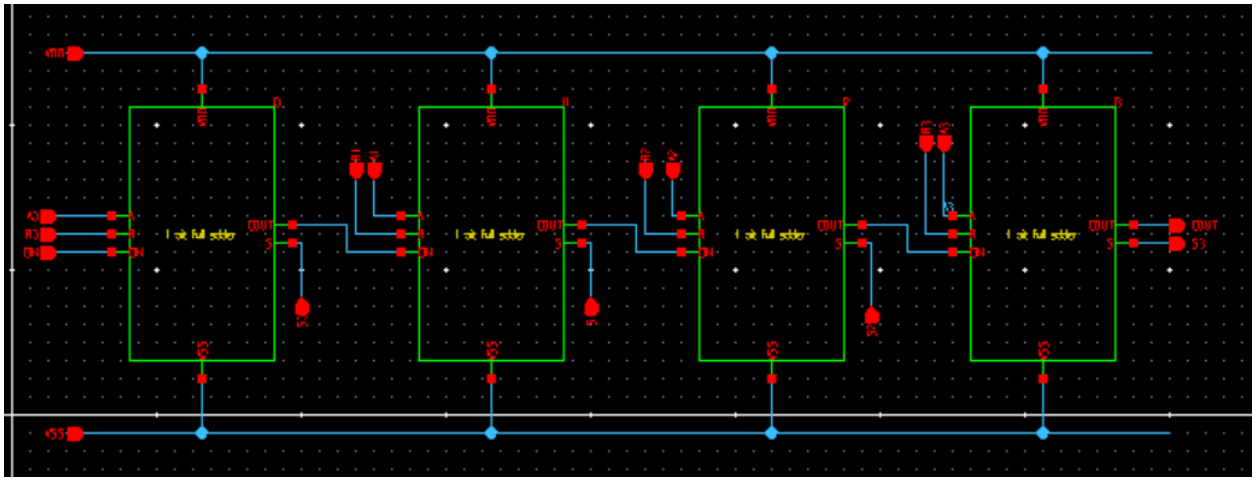

Fig. 18: 4-bit full adder schematic

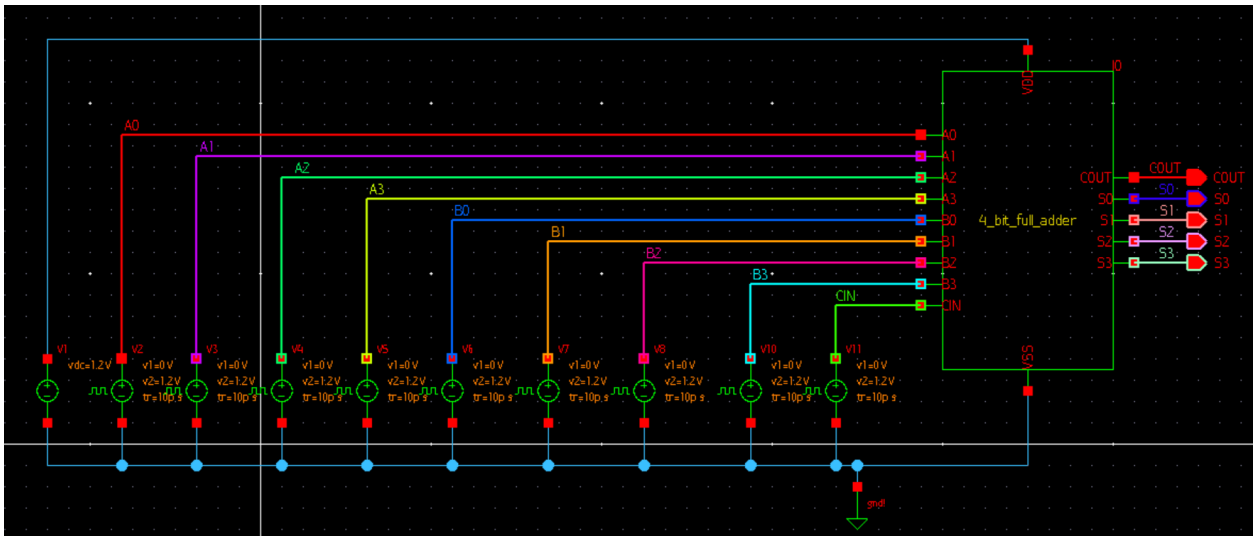

Fig. 19: 4-bit full adder testbench

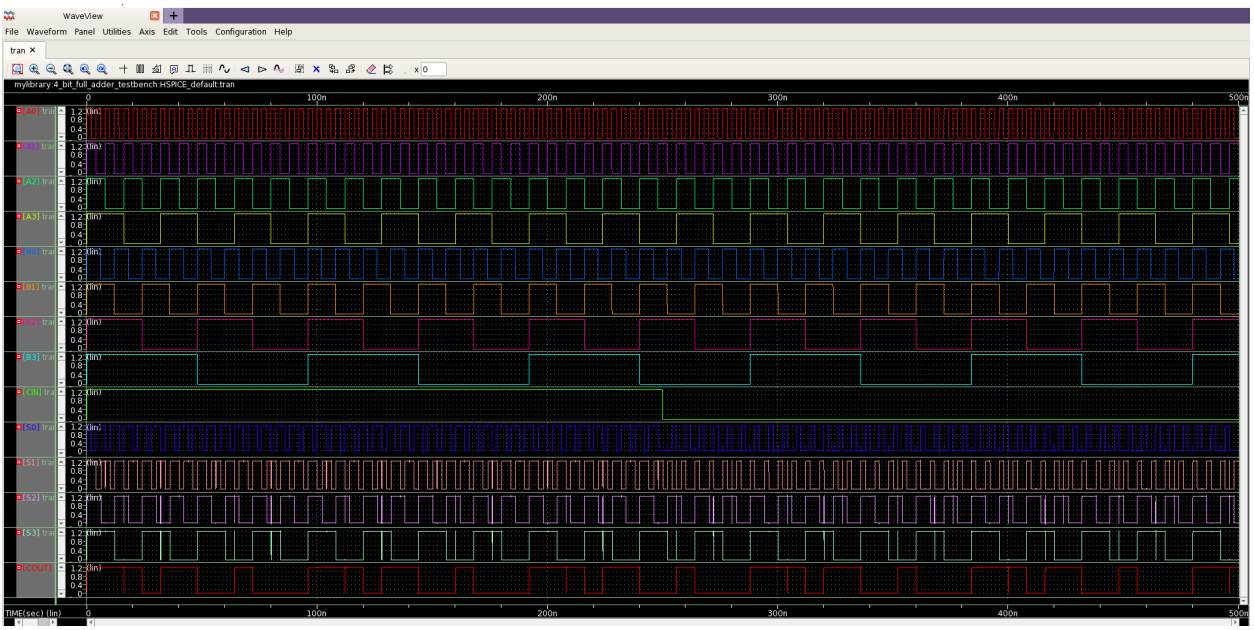

Fig. 19: 4-bit full adder schematic Simulation result

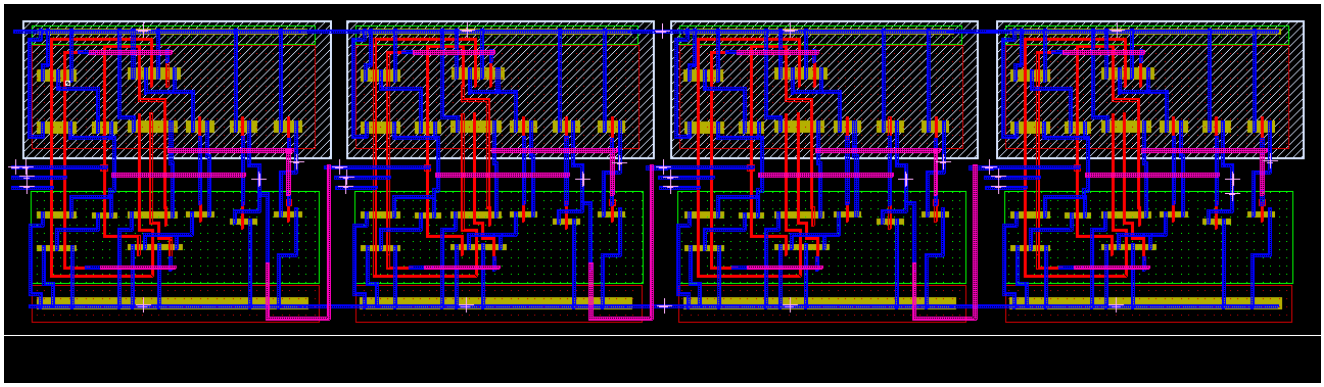

Fig. 20: 4 bit full adder layout

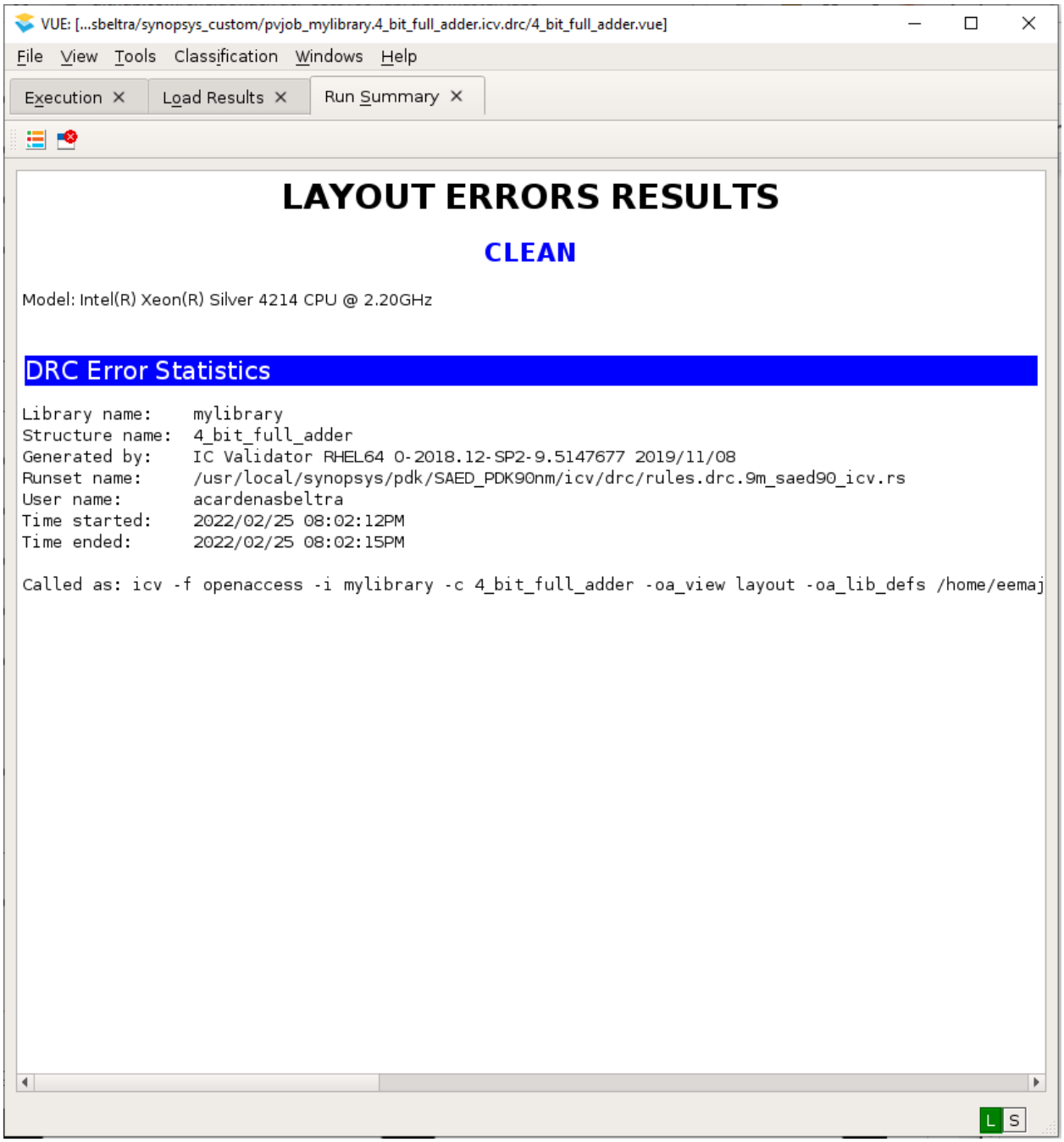

Fig. 21: 4-bit full adder DRC Result

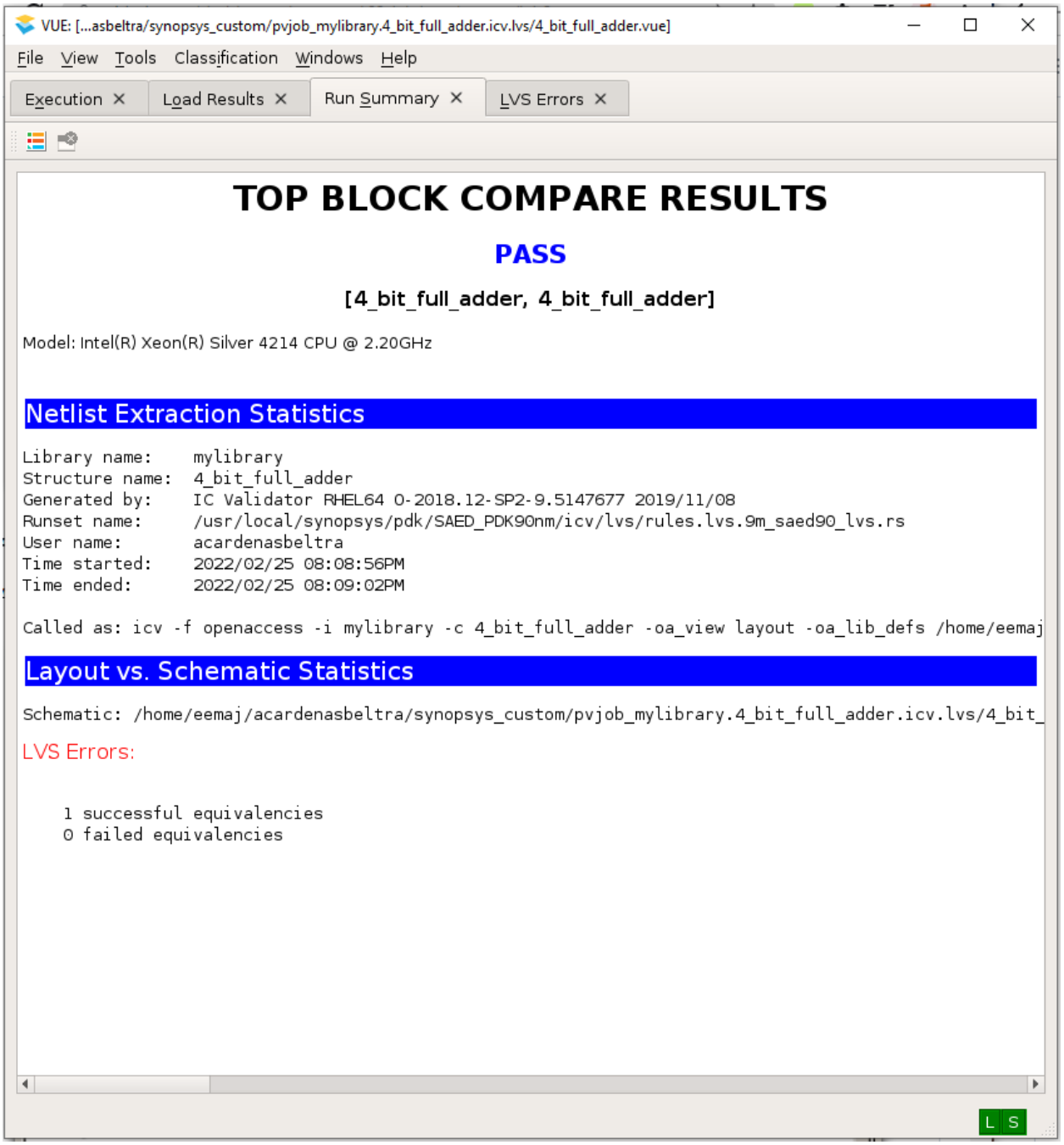

Fig. 22: 4-bit full adder LVS Result

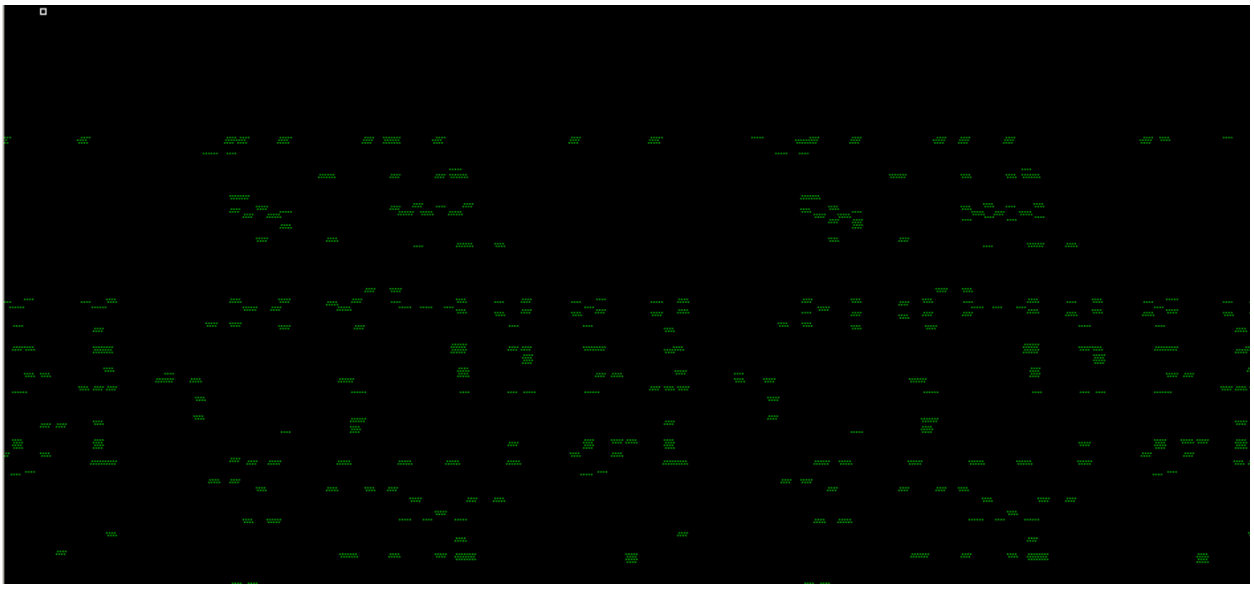

Fig. 23: 4-bit full adder Parasitic Extraction

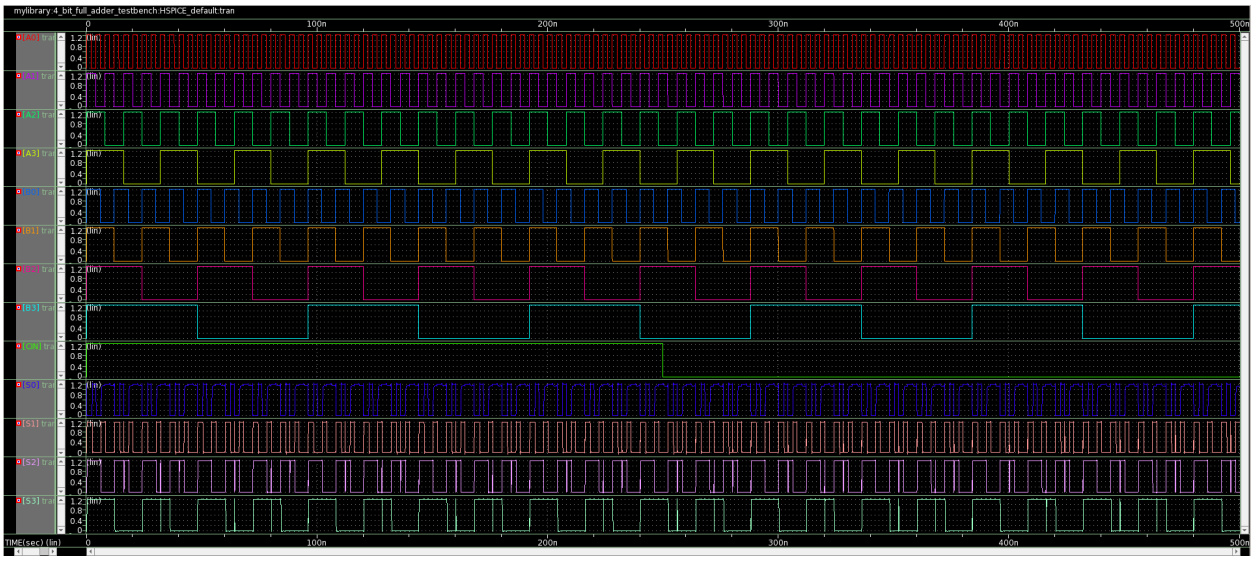

Fig. 23: 4-bit full adder Simulation Result with Parasitic Extraction

Issues

I had many issues in designing the layout for the 1-bit full adder. I was having trouble visualizing the layout from the circuit schematic. What I did was that in addition to the stick diagram, I drew the layout out on paper. After I had completed my layout, I had many problems with the LVS. One was that I had forgotten to add contacts to the metal of the body of the circuit. Also, My connections for S were separate so I was receiving unmatched errors. After my layout was fully verified, the rest of the lab was fairly simple, but I did spend many hours only on the layout of the 1-bit full adder portion of the lab.