Lab 2

Ana Cardenas Beltran

SID: 862158699

Section 23

ENGR ID: acardenasbeltra

UCR NetID: acard079

Summary

In this lab, we learned how to create layouts for an inverter and a NAND Gate using Custom Designer. We also learned how to validate our designs using DRC and LVS. After studying the layout of transistors, I was able to create layouts for the schematics I had made for the two circuits. I also found myself referring back to the SAED 90nm Design Rules Document, so I became very familiar with it and the specifications for designing layouts.

Checkoff Video

Lab 2 Checkoff Video

Part 1. Inverter

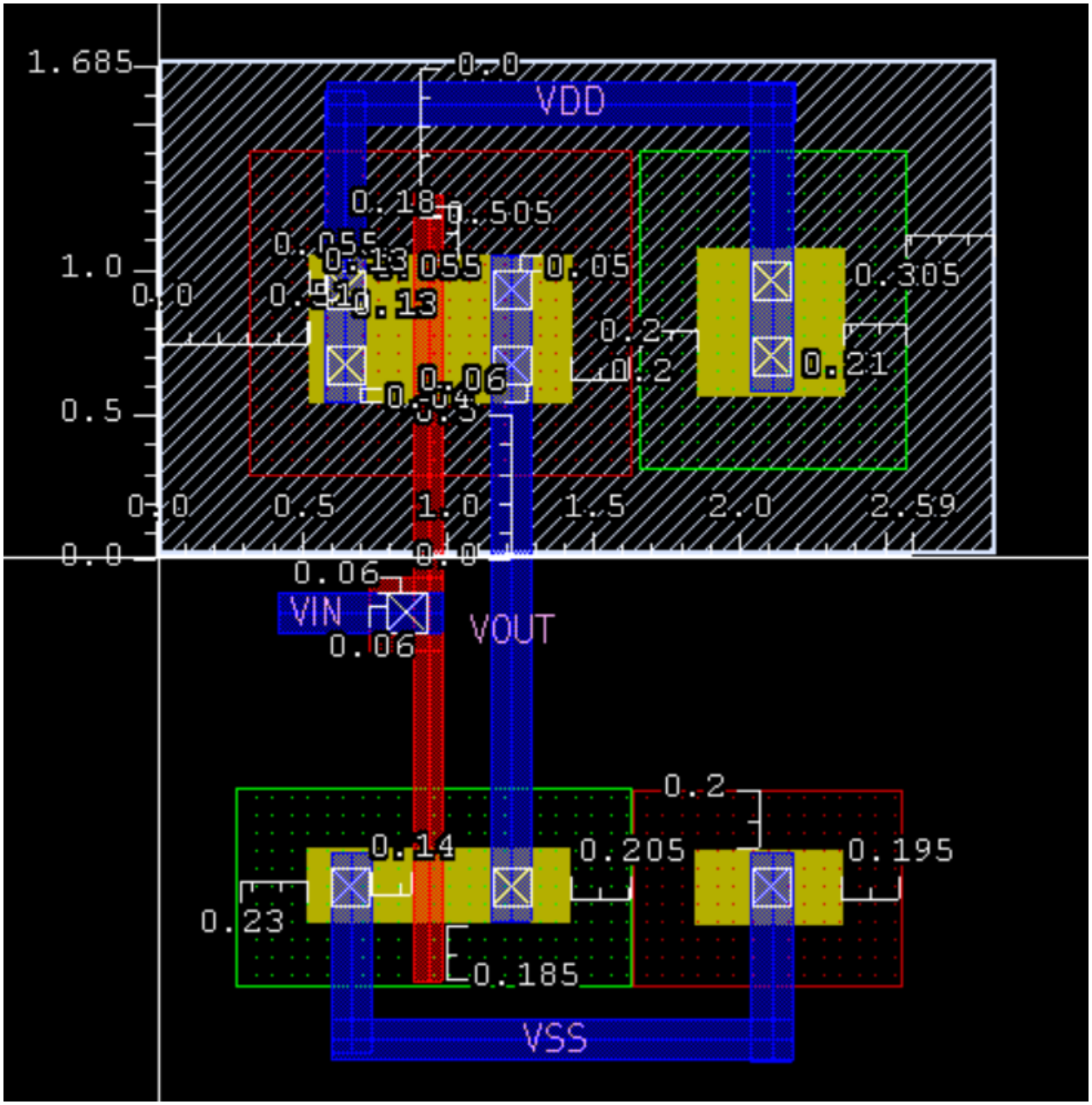

Fig. 1: Inverter layout

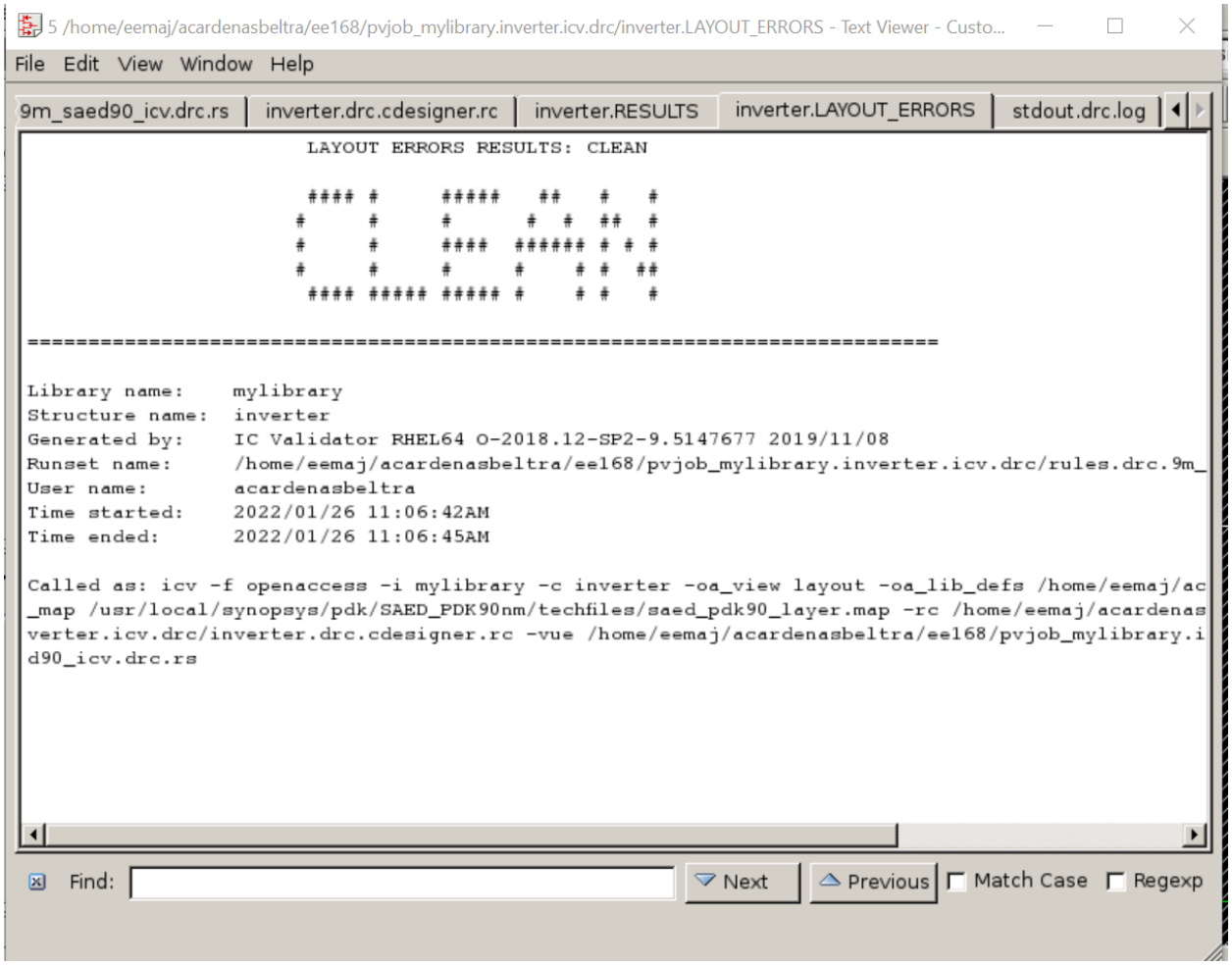

Fig 2. DRC Result with CLEAN for Inverter Layout

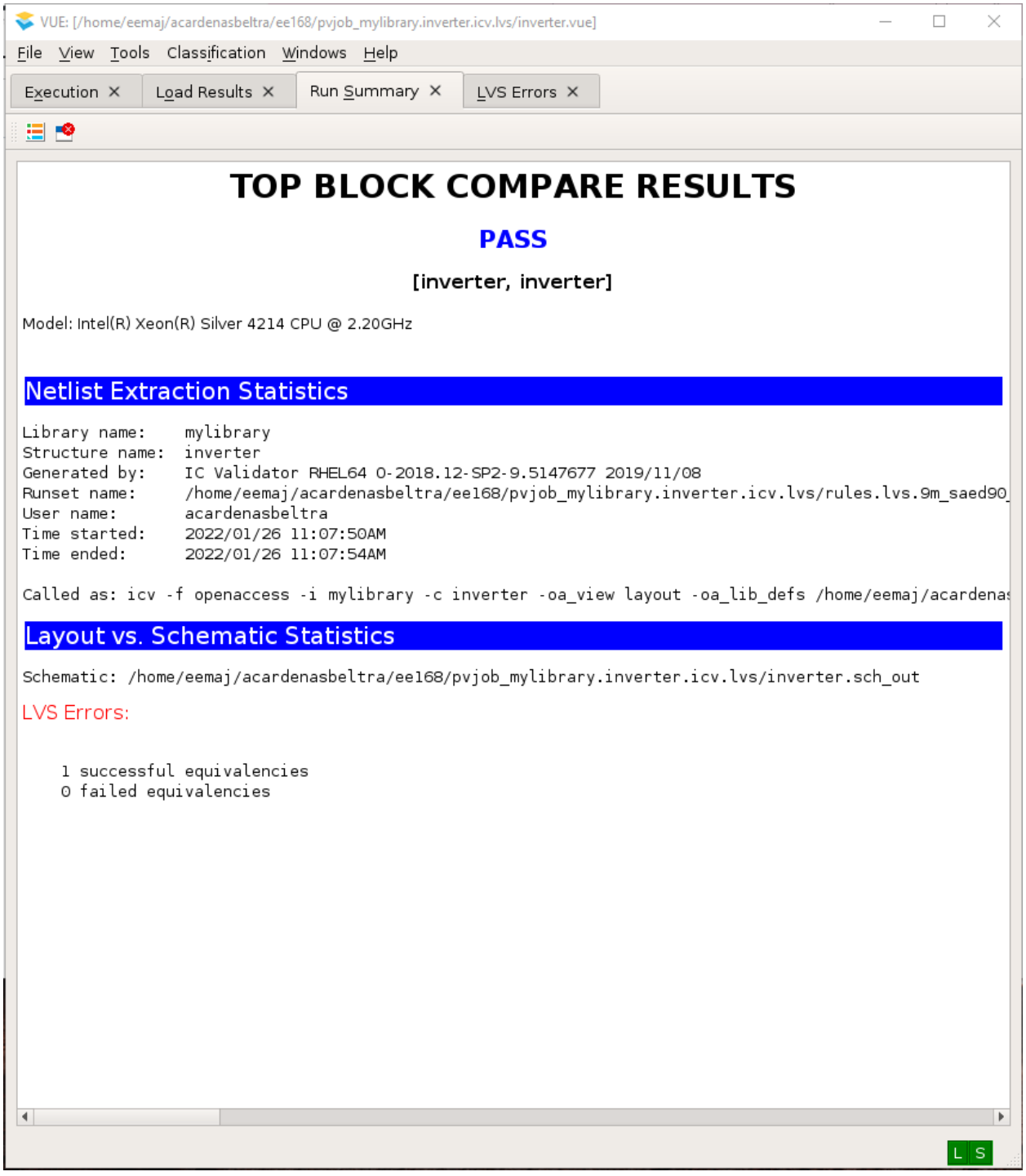

Fig 3. LVS Result with PASS for Inverter Layout

Part 2. NAND Gate

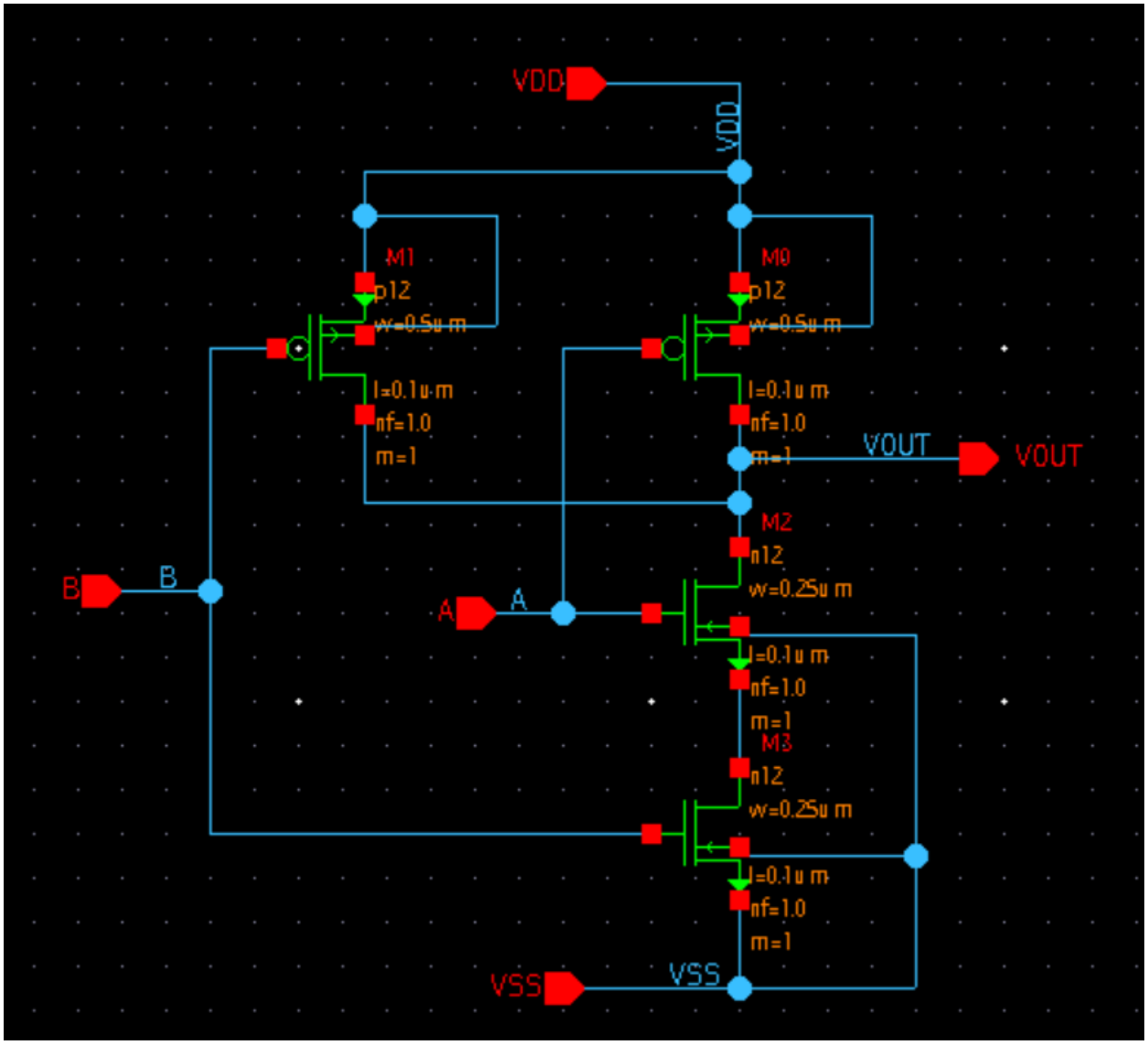

Fig. 4: NAND Gate Schematic

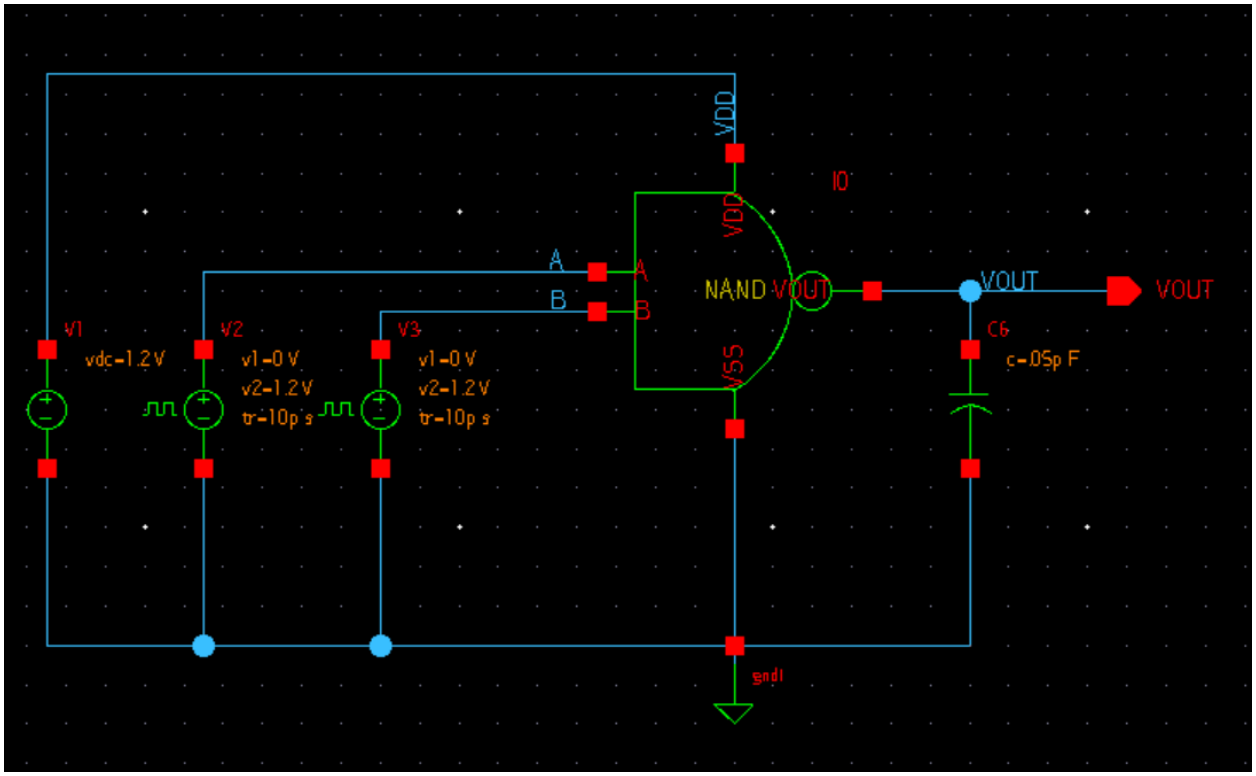

Fig. 5: NAND Gate test bench schematic

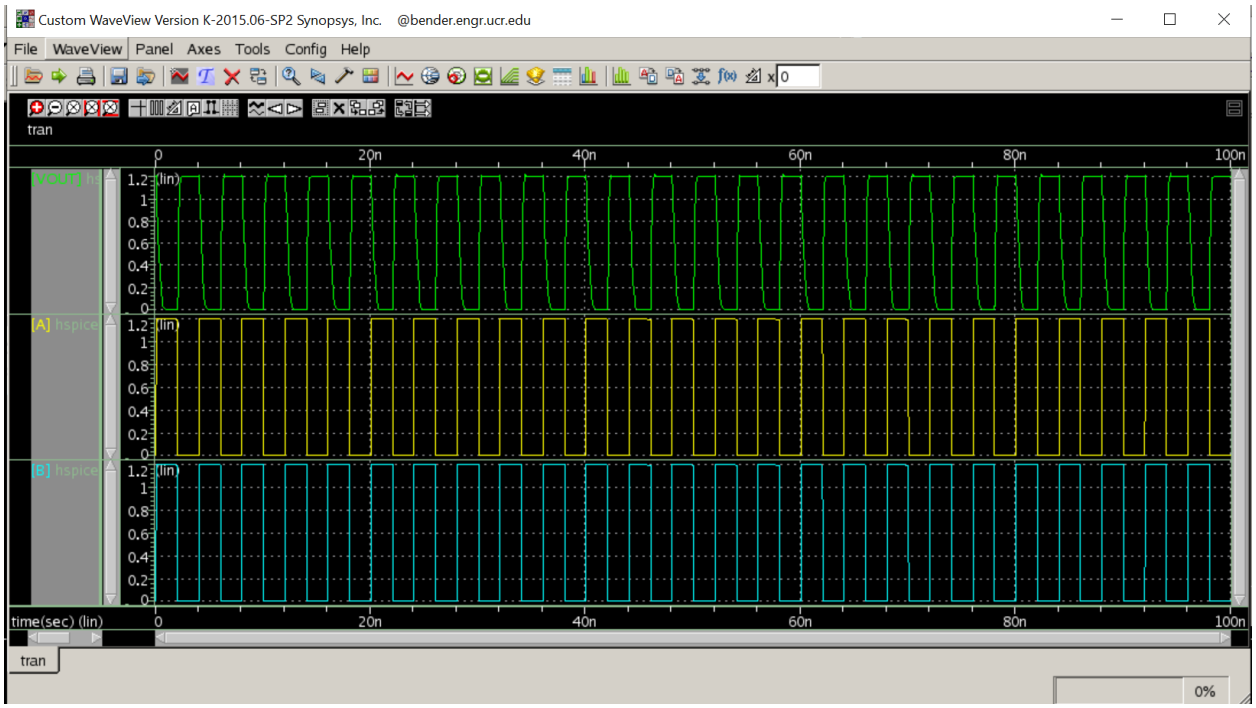

Fig. 6: NAND Gate Testbench Results

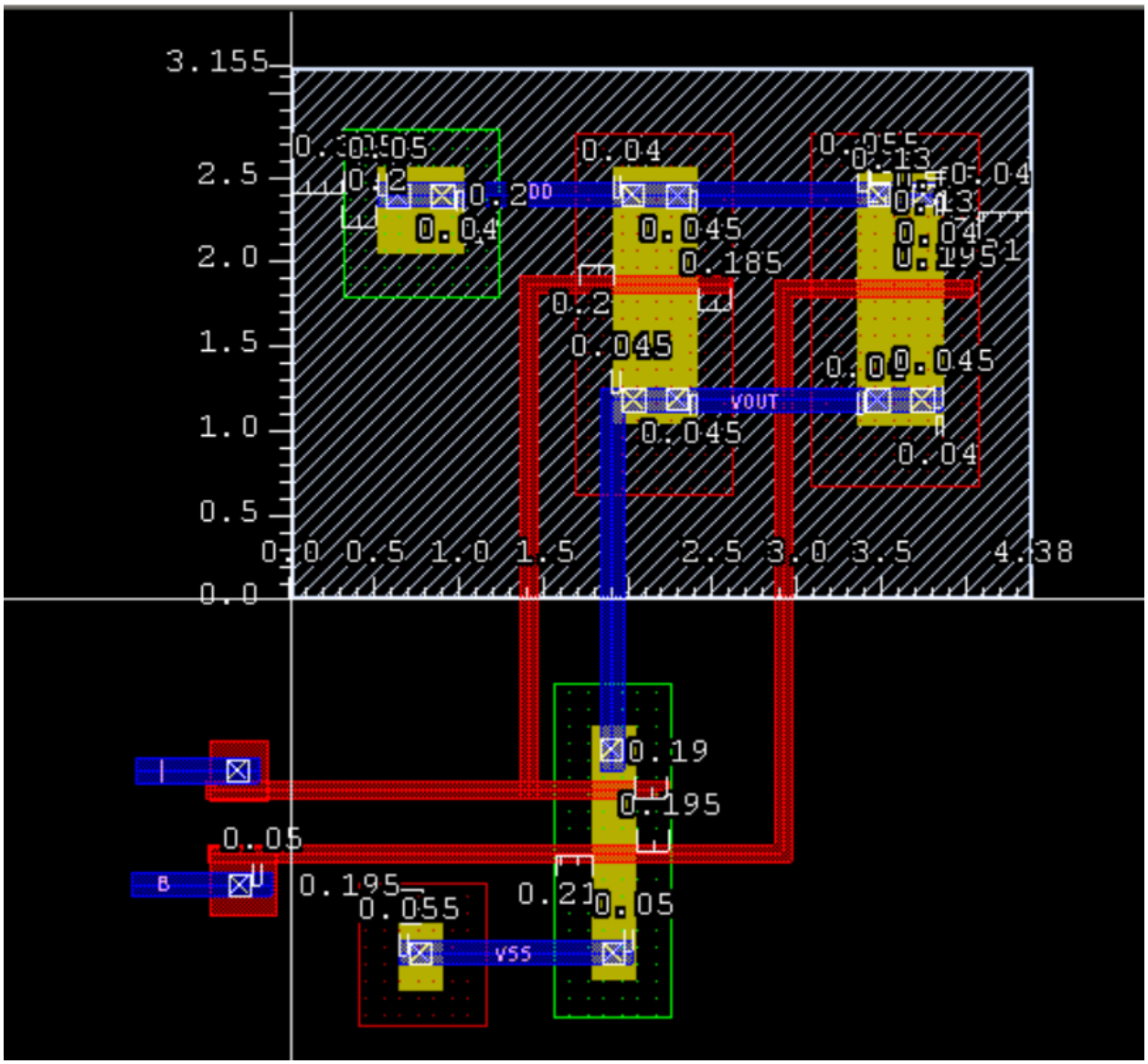

Fig. 7: NAND Gate Layout

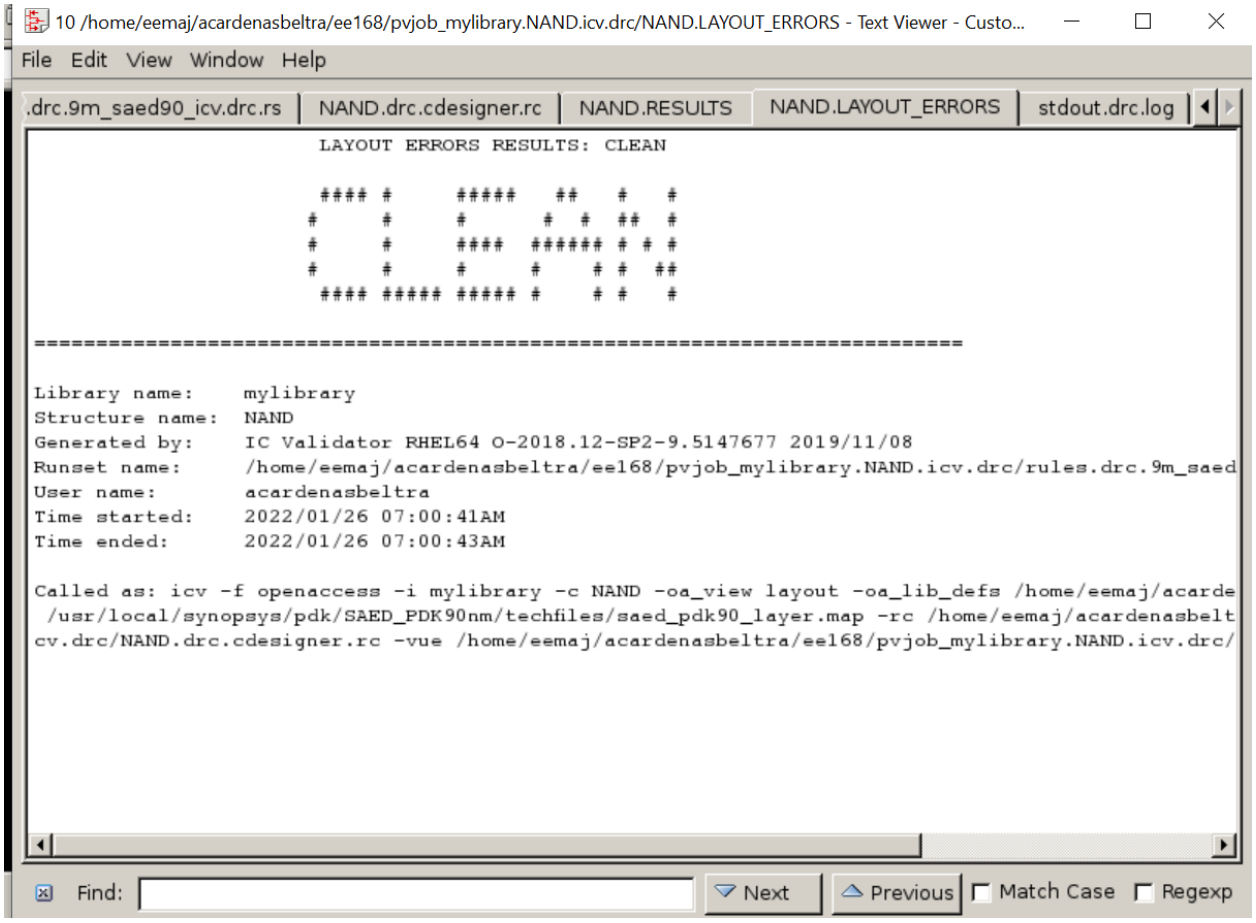

Fig. 8: DRC Result with CLEAN for NAND Gate layout

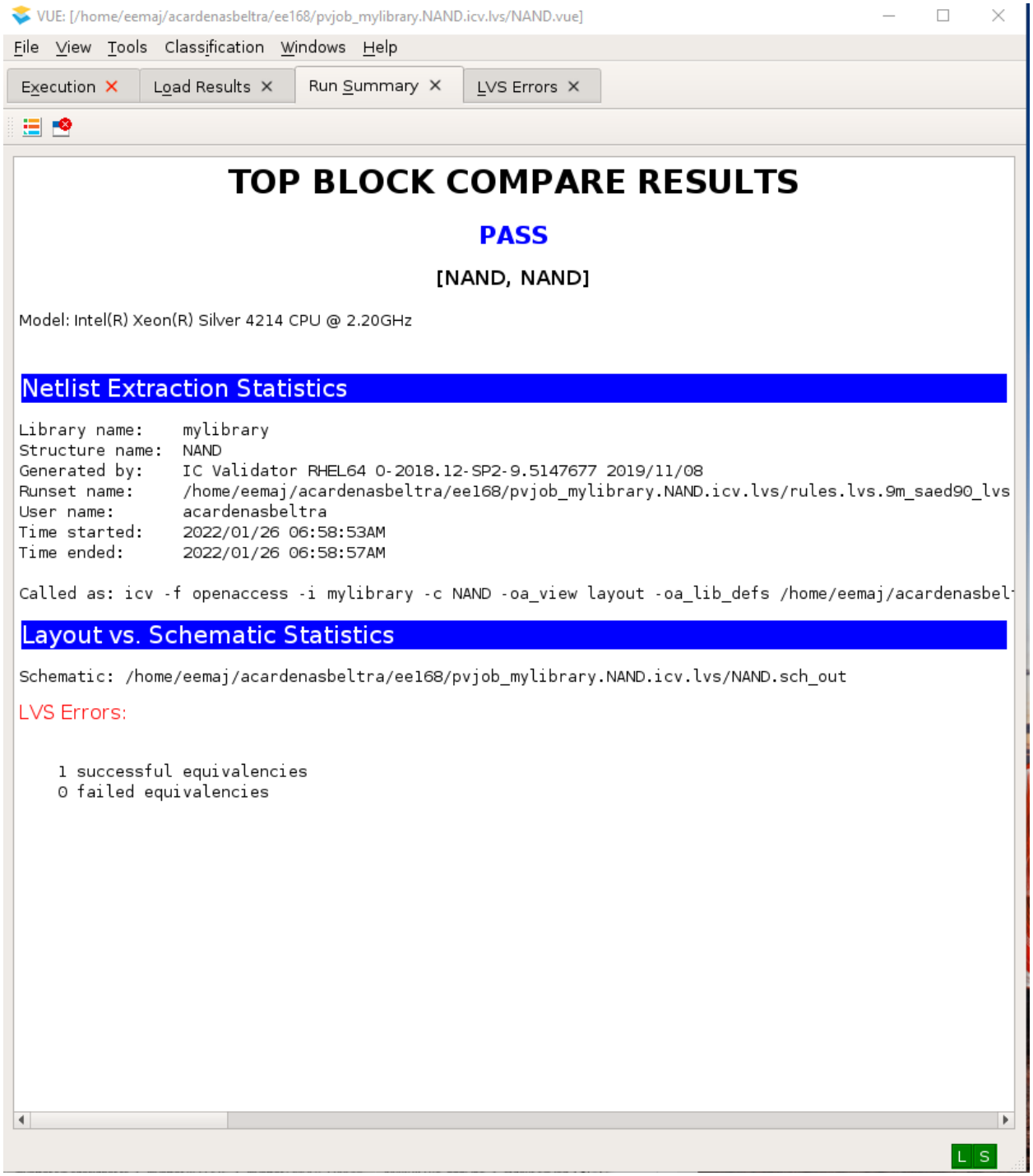

Fig. 9: LVS Result with PASS for NAND Gate Layout

Issues Encountered

One of the issues I had with this lab was it was very tedious and time consuming to make sure all the layers met the required specifications. However, with time, I got used to referring

back to the SAED 90nm Design Rules Document to make sure specifications were being met. A big issue I had was that once I had almost finished my NAND Gate Layout, my internet crashed and synopsis closed and “locked” my design so I could no longer edit it. I had to delete the file and start over.