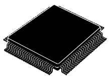
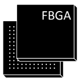
STM32H7A3xI/G

Datasheet

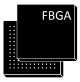
32-bit Arm® Cortex®-M7 280 MHz MCUs, up to 2-Mbyte Flash memory, 1.4-Mbyte RAM, 46 com. and analog interfaces, SMPS



LQFP64
(10 x 10 mm)
LQFP100
(14 x 14 mm)
LQFP144
(20x20 mm)
LQFP176
(24 x 24 mm)



TFBGA100
(8 x 8 mm)
TFBGA216
(13x13 mm)
TFBGA225
(13x13 mm)



UFBGA169
(7 x 7 mm)
UFBGA176+25
(10x10 mm)

WLCSP132
(4.57 X 4.37 mm)

Product summary	
STM32H7A3xI	STM32H7A3RI, STM32H7A3VI, STM32H7A3QI, STM32H7A3ZI, STM32H7A3AI, STM32H7A3II, STM32H7A3NI, STM32H7A3LI
STM32H7A3xG	STM32H7A3RG, STM32H7A3VG, STM32H7A3ZG, STM32H7A3AG, STM32H7A3IG, STM32H7A3NG, STM32H7A3LG

Features

Includes ST state-of-the-art patented technology

Core

- 32-bit Arm® Cortex®-M7 core with double-precision FPU and L1 cache: 16 Kbytes of data and 16 Kbytes of instruction cache allowing to fill one cache line in a single access from the 128-bit embedded flash memory; frequency up to 280 MHz, MPU, 599 DMIPS/ 2.14 DMIPS/MHz (Dhrystone 2.1), and DSP instructions

Memories

- Up to 2 Mbytes of flash memory with read while write support, plus 1 Kbyte of OTP memory
- ~1.4 Mbytes of RAM: 192 Kbytes of TCM RAM (inc. 64 Kbytes of ITCM RAM + 128 Kbytes of DTCM RAM for time critical routines), 1.18 Mbytes of user SRAM, and 4 Kbytes of SRAM in Backup domain
- 2x Octo-SPI memory interfaces, I/O multiplexing and support for serial PSRAM/ NOR, Hyper RAM/flash frame formats, running up to 140 MHz in SRD mode and up to 110 MHz in DTR mode
- Flexible external memory controller with up to 32-bit data bus:
  - SRAM, PSRAM, NOR flash memory clocked up to 125 MHz in Synchronous mode
  - SDRAM/LPSDR SDRAM
  - 8/16-bit NAND flash memories
- CRC calculation unit

Security

- ROP, PC-ROP, active tamper, secure firmware upgrade support

General-purpose input/outputs

- Up to 168 I/O ports with interrupt capability
  - Fast I/Os capable of up to 133 MHz
  - Up to 164 5-V-tolerant I/Os

Low-power consumption

- Stop: down to 32 µA with full RAM retention
- Standby: 2.8 µA (Backup SRAM OFF, RTC/LSE ON, PDR OFF)
- V_{BAT}: 0.8 µA (RTC and LSE ON)

Clock management

- Internal oscillators: 64 MHz HSI, 48 MHz HSI48, 4 MHz CSI, 32 kHz LSI
- External oscillators: 4-50 MHz HSE, 32.768 kHz LSE
- 3× PLLs (1 for the system clock, 2 for kernel clocks) with fractional mode

Reset and power management

- 2 separate power domains, which can be independently clock gated to maximize power efficiency:
  - CPU domain (CD) for Arm® Cortex® core and its peripherals, which can be independently switched in Retention mode
  - Smart run domain (SRD) for reset and clock control, power management and some peripherals
- 1.62 to 3.6 V application supply and I/Os
- POR, PDR, PVD and BOR
- Dedicated USB power embedding a 3.3 V internal regulator to supply the internal PHYs
- Dedicated SDMMC power supply
- High power efficiency SMPS step-down converter regulator to directly supply V_{CORE} or an external circuitry
- Embedded regulator (LDO) with configurable scalable output to supply the digital circuitry
- Voltage scaling in Run and Stop mode
- Backup regulator (~0.9 V)
- Low-power modes: Sleep, Stop and Standby
- V_{BAT} battery operating mode with charging capability
- CPU and domain power state monitoring pins

Interconnect matrix

- 3 bus matrices (1 AXI and 2 AHB)
- Bridges (5× AHB2APB, 3× AXI2AHB)

5 DMA controllers to unload the CPU

- 1× high-speed general-purpose master direct memory access controller (MDMA)
- 2× dual-port DMAs with FIFO and request router capabilities
- 1× basic DMA with request router capabilities
- 1x basic DMA dedicated to DFSDM

Up to 35 communication peripherals

- 4× I2C FM+ interfaces (SMBus/PMBus)
- 5× USART/5x UARTs (ISO7816 interface, LIN, IrDA, modem control) and 1x LPUART
- 6× SPIs, including 4 with muxed full-duplex I2S audio class accuracy via internal audio PLL or external clock and 1 x SPI/I2S in LP domain (up to 125 MHz)
- 2x SAIs (serial audio interface)
- SPDIFRX interface
- SWPMI single-wire protocol master interface
- MDIO Slave interface
- 2× SD/SDIO/MMC interfaces (up to 133 MHz)
- 2× CAN controllers: 2 with CAN FD, 1 with time-triggered CAN (TT-CAN)
- 1× USB OTG interfaces (1HS/FS)
- HDMI-CEC
- 8- to 14-bit camera interface up to 80 MHz
- 8-/16-bit parallel synchronous data input/output slave interface (PSSI)

11 analog peripherals

- 2× ADCs with 16-bit max. resolution (up to 24 channels, up to 3.6 MSPS)
- 1× analog and 1x digital temperature sensors
- 1× 12-bit single-channel DAC (in SRD domain) + 1× 12-bit dual-channel DAC
- 2× ultra-low-power comparators
- 2× operational amplifiers (8 MHz bandwidth)
- 2× digital filters for sigma delta modulator (DFSDM), 1x with 8 channels/8 filters and 1x in SRD domain with 2 channels/1 filter

Graphics

- LCD-TFT controller up to XGA resolution
- Chrom-ART graphical hardware Accelerator (DMA2D) to reduce CPU load
- Hardware JPEG Codec
- Chrom-GRC™ (GFXMMU)

Up to 19 timers and 2 watchdogs

- 2× 32-bit timers with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input (up to 280 MHz)
- 2× 16-bit advanced motor control timers (up to 280 MHz)
- 10× 16-bit general-purpose timers (up to 280 MHz)
- 3× 16-bit low-power timers (up to 280 MHz)
- 2× watchdogs (independent and window)
- 1× SysTick timer
- RTC with sub-second accuracy and hardware calendar

Debug mode

- SWD and JTAG interfaces
- 4 KB Embedded Trace Buffer

1x 32-bit, NIST SP 800-90B compliant, true random generator

96-bit unique ID

All packages are ECOPACK2 compliant

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32H7A3xI/G microcontrollers.

This document should be read in conjunction with the STM32H7A3xI/G reference manual (RM0455). The reference manual is available from the STMicroelectronics website .

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32H7A3xI/G errata sheet (ES0478), available on the STMicroelectronics website .

For information on the Arm® Cortex®-M7 core, refer to the Cortex®-M7 Technical Reference Manual, available from the www.arm.com website

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Description

STM32H7A3xI/G devices are based on the high-performance Arm® Cortex®-M7 32-bit RISC core operating at up to 280 MHz. The Cortex® -M7 core features a floating point unit (FPU) which supports Arm® double-precision (IEEE 754 compliant) and single-precision data-processing instructions and data types. STM32H7A3xI/G devices support a full set of DSP instructions and a memory protection unit (MPU) to enhance application security.

STM32H7A3xI/G devices incorporate high-speed embedded memories with a dual-bank flash memory of up to 2 Mbytes, around 1.4 Mbyte of RAM (including 192 Kbytes of TCM RAM, 1.18 Mbytes of user SRAM and 4 Kbytes of backup SRAM), as well as an extensive range of enhanced I/Os and peripherals connected to four APB buses, three AHB buses, a 32-bit multi-AHB bus matrix and a multi layer AXI interconnect supporting internal and external memory access.

All the devices offer two ADCs, two DACs (one dual and one single DAC), two ultra-low power comparators, a low-power RTC, 12 general-purpose 16-bit timers, two PWM timers for motor control, three low-power timers, a true random number generator (RNG). The devices support nine digital filters for external sigma delta modulators (DFSDM). They also feature standard and advanced communication interfaces.

- Standard peripherals
  - Four I2Cs
  - Five USARTs, five UARTs and one LPUART
  - Six SPIs, four I2Ss in full-duplex mode. To achieve audio class accuracy, the I^2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
  - Two SAI serial audio interfaces, out of which one with PDM
  - One SPDIFRX interface
  - One single wire protocol master interface (SWPMI)
  - One 16-bit parallel synchronous slave interface (PSSI) sharing the same interface as the digital camera)
  - Management Data Input/Output (MDIO) slaves
  - Two SDMMC interfaces (one can be supplied from a supply voltage separate from that of all other I/Os)
  - A USB OTG high-speed with full-speed capability (with the ULPI)
  - One FDCAN plus one TT-CAN interface
  - Chrom-ART Accelerator
  - HDMI-CEC
- Advanced peripherals including
  - A flexible memory control (FMC) interface
  - Two octo-SPI memory interface
  - A digital camera interface for CMOS sensors (DCMI)
  - A graphic memory management unit (GFXMMU)
  - An LCD-TFT display controller (LTDC)
  - A JPEG hardware compressor/decompressor

Refer to Table 1. STM32H7A3xI/G features and peripheral counts for the list of peripherals available on each part number.

STM32H7A3xI/G devices operate in the –40 to +85 °C ambient temperature range from a 1.62 to 3.6 V power supply. The supply voltage can drop down to 1.62 V by using an external power supervisor (see Section 3.5.2 Power supply supervisor) and connecting the PDR_ON pin to V_{SS}. Otherwise the supply voltage must stay above 1.71 V with the embedded power voltage detector enabled.

The USB OTG_HS/FS interfaces can be supplied either by the integrated USB regulator or through a separate supply input.

A dedicated supply input is available for one of the SDMMC interface for package with more than 100 pins. It allows running from a different voltage level than all other I/Os.

A comprehensive set of power-saving mode allows the design of low-power applications.

The CPU and domain states can be directly monitored on some GPIOs configured as alternate functions.

STM32H7A3xI/G devices are offers in several packages ranging from 64 pins to 225 pins/balls. The set of included peripherals changes with the device chosen.

These features make the STM32H7A3xI/G microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile applications, Internet of Things
- Wearable devices: smart watches.

Figure 1. STM32H7A3xI/G block diagram shows the general block diagram of the device family.

Table 1. STM32H7A3xI/G features and peripheral counts

Peripherals		SMPS [1]								no-SMPS						
		STM32H7A3LIH/LGH	STM32H7A3IIK/IGK	STM32H7A3IIT/IGT	STM32H7A3AII/AGI	STM32H7A3ZIT/ZGT	STM32H7A3QIY	STM32H7A3VIH/VGH	STM32H7A3VIT/VGT	STM32H7A3NIH/NGH	STM32H7A3IIK/IGK	STM32H7A3IIT/IGT	STM32H7A3ZIT/ZGT	STM32H7A3VIH/VGH	STM32H7A3VIT/VGT	STM32H7A3RIT/RGT
Flash memory (Kbytes)		1024 (STM32H7A3xGx)/2048 (STM32H7A3xIx),														
SRAM in Kbytes	SRAM on AXI	1024														
	SRAM on AHB (CD domain)	128														
	SRAM on AHB (SRD domain)	32														
TCM RAM in Kbytes	ITCM RAM (instruction)	64														
	DTCM RAM (data)	128														
Backup SRAM (Kbytes)		4														
FMC	Interface	1														
	NOR Flash memory/RAM controller	x	x [2]			-	x[2]	-		x			x[2]	-		
	Multiplexed I/O NOR Flash memory	x					x[2]			x				x[2]		-
	16-bit NAND Flash memory	x					x[2]		-	x				x[2]		-
	SDRAM controller	x	x[2]			-				x			x[2]	-		
Octo-SPI interfaces[3]		2	2[4]			2 [5]		1	1 Quad-SPI	2			2[4]	1		1 Quad-SPI
Timers	General-purpose	10														
	Advanced-control (PWM)	2														
	Basic	2														
	Low-power	3														

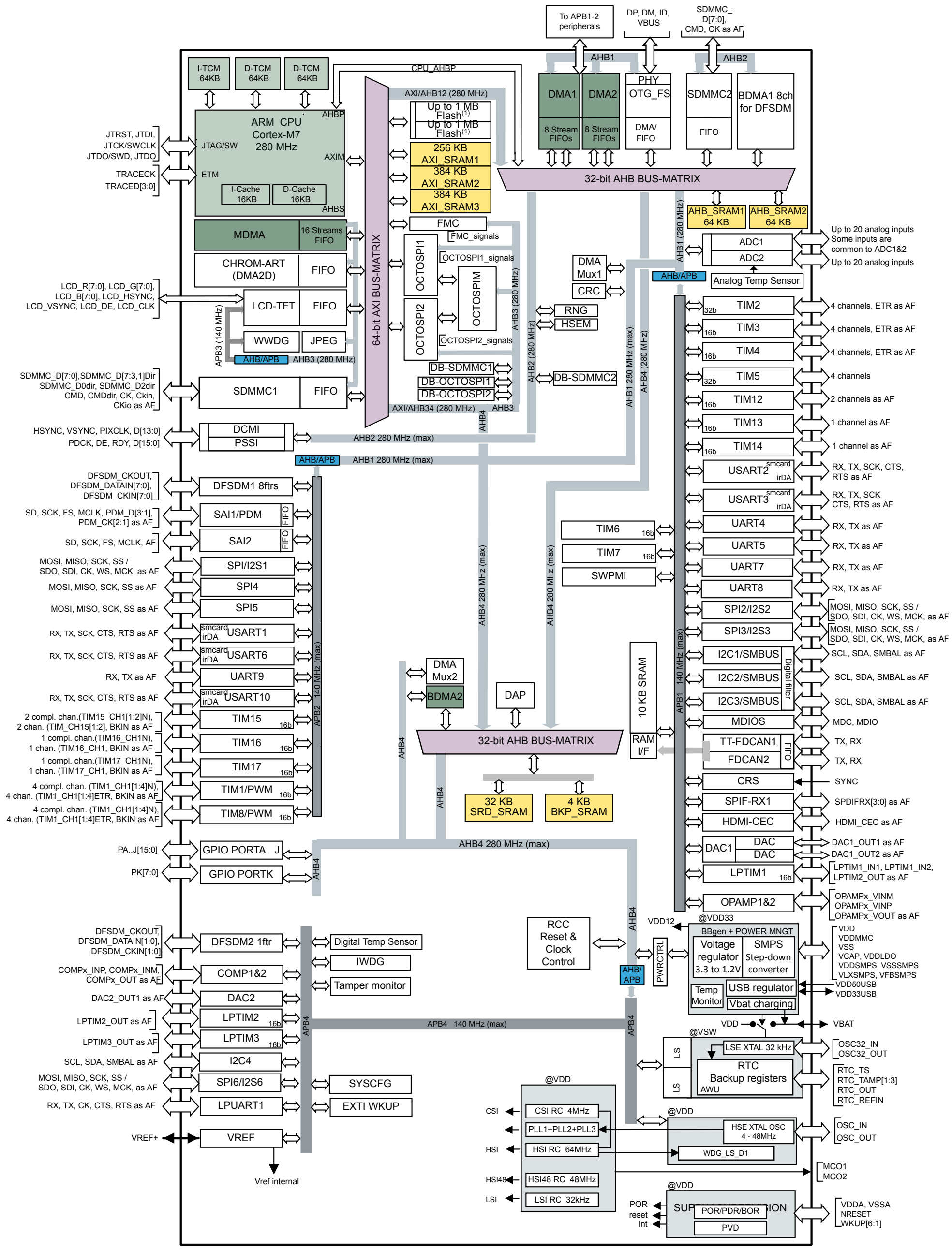
Peripherals		SMPS [1]								no-SMPS						
		STM32H7A3LIH/LGH	STM32H7A3IIK/IGK	STM32H7A3IIT/IGT	STM32H7A3AII/AGI	STM32H7A3ZIT/ZGT	STM32H7A3QIY	STM32H7A3VIH/VGH	STM32H7A3VIT/VGT	STM32H7A3NIH/NGH	STM32H7A3IIK/IGK	STM32H7A3IIT/IGT	STM32H7A3ZIT/ZGT	STM32H7A3VIH/VGH	STM32H7A3VIT/VGT	STM32H7A3RIT/RGT
Window watchdog / independent watchdog		1/1														
Real-time Clock (RTC)		1														
Tamper pins [6]	Passive	3	2							3			2			
	Active	2	1							2			1			
Random number generator		1														
Communi-cation interfaces	SPI/I2S [7]	6/4					5/4		5[2]/4	6/4				5/4		4/4
	I2C	4														3
	USART/UART /LPUART	5/5 /1					5[2]/5[2] /1	5[2]/5 /1	4[2]/5[2] /1	5/5 /1				5[2]/5 /1		4[2]/3[2] /1
	SAI/PDM	2/1					2[2]/1[2]	2[2]/1		2/1				2[2]/1		1[2]/-
	SPDIFRX	4 inputs							-	4 inputs						
	SWPMI	1														
	MDIOS	1														
	SDMMC	2						2 [8]		2				2[8]		
	FDCAN/TT-CAN	1/1														1/1[2]
	USB OTG_HS ULPI, OTG_FS PHY	1		1[9]	1	1[9]	1	1[9]		1			1			1 [10]
Digital camera interface/PSSI [11]		1/1														1/1[2]
LCD-TFT display controller		1														
JPEG Codec		1														
Chrom-ART Accelerator (DMA2D)		1														
Graphic memory management unit (GFXMMU)		1														
HDMI CEC		1														
DFSDM		2														

Peripherals		SMPS [1]								no-SMPS						
		STM32H7A3LIH/LGH	STM32H7A3IIK/IGK	STM32H7A3IIT/IGT	STM32H7A3AII/AGI	STM32H7A3ZIT/ZGT	STM32H7A3QIY	STM32H7A3VIH/VGH	STM32H7A3VIT/VGT	STM32H7A3NIH/NGH	STM32H7A3IIK/IGK	STM32H7A3IIT/IGT	STM32H7A3ZIT/ZGT	STM32H7A3VIH/VGH	STM32H7A3VIT/VGT	STM32H7A3RIT/RGT
Number of filters for DFSDM1/ DFSDM2		8/1							7/1	8/1						7/1
ADCs	8 to 16 bits	2														
	Number of channels	24	24	20 [12]	24	18[12]	17[12]	16[12]		20[12]				16[12]		
DACs	12 bits	2														
	Number of channels	3 (1 single channel + 1 dual-channel interfaces)														
Comparators		2							2[2]	2						1
Operational amplifier		2							2[2]	2						1
GPIOs		168	128	119	121	97	87	75	68	166	138	138	112	80	80	49
	Wakeup pins	6	4							6			4			
Maximum CPU frequency (MHz)		280														
SMPS step-down converter		1								-						
USB internal regulator		1							-	-						
USB separate supply pad		1													-	
VDDMMC separate supply pad		1						-		1				-		
VREF+ separate pad and internal buffer		1								1				-	1	-
Operating voltage		1.62 to 3.6 V [13]														
Operating temperatures		Ambient temperature range: −40 to 85 °C														
		Junction temperature range: −40 to 130 °C[14]														
Packages		TFBGA 225	UFBGA 176+25	LQFP 176	UFBGA 169	LQFP 144	WLCSP 132	TFBGA 100	LQFP 100	TFBGA 216	UFBGA 176+25	LQFP 176	LQFP 144	TFBGA 100	LQFP 100	LQFP64
Bootloader		USART, I2C, SPI, USB-DFU, FDCAN		USART, I2C, SPI, USB-DFU	USART, I2C, SPI, USB-DFU, FDCAN	USART, I2C, SPI, USB-DFU				USART, I2C, SPI, USB-DFU, FDCAN			USART, I2C, SPI, USB-DFU			

1. *The devices with SMPS correspond to commercial code STM32H7A3xIxxQ and STM32H7A3xGxxQ.*

2. For limitations on peripheral features depending on packages, check the available pins/balls in Table 7. STM32H7A3xI/G pin/ball definition.
3. To maximize the performance, the I/O high-speed at low-voltage feature (HSLV) must be activated when V_{DD} < 2.7 V. This feature is not available on all I/Os (see Table 90. OCTOSPI characteristics in SDR mode, and Table 91. OCTOSPI characteristics in DTR mode (with DQS)/Octal and Hyperbus).
4. The I/O high-speed at low-voltage feature (HSLV) at V_{DD} < 2.7 V is not available for OCTOSPIM_P2.
5. The two OCTOSPIs are available only in Muxed mode.
6. A tamper pin can be configured either as passive or active (not both).
7. SPI1, SPI2, SPI3 and SPI6 interfaces give the flexibility to work in an exclusive way in either SPI mode or I2S audio mode.
8. Dedicated I/O supply pad (VDDMMC) or external level shifter are not supported.
9. The ULPI interface is supported. PC2 and PC3 are available on PC2_C and PC3_C, respectively, by closing the internal analog switch (see Table 7. STM32H7A3xI/G pin/ball definition).
10. The ULPI interface is not supported.
11. DCMI and PSSI cannot be used simultaneously since they share the same circuitry.
12. For limitations on fast pads or channels depending on packages, check to the available pins/balls in Table 7. STM32H7A3xI/G pin/ball definition.
13. V_{DD}/V_{DDA} can drop down to 1.62 V by using an external power supervisor (see Section 3.5.2 Power supply supervisor) and connecting PDR_ON pin to V_{SS}. Otherwise the supply voltage must stay above 1.71 V with the embedded power voltage detector enabled.
14. The junction temperature is limited to 105 °C in VOS0 voltage range.

Figure 1. STM32H7A3xI/G block diagram



1. STM32H7AxGx devices feature two Flash memory banks of 512 Kbytes each.

3 Functional overview

3.1 Arm® Cortex®-M7 with FPU

The Arm® Cortex®-M7 with double-precision FPU processor is the latest generation of Arm processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and optimized power consumption, while delivering outstanding computational performance and low interrupt latency.

The Cortex®-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard architecture with L1 caches (16 Kbytes of I-cache and 16 Kbytes of D-cache)
- 64-bit AXI4 interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The following memory interfaces are supported:

- Separate Instruction and Data buses (Harvard Architecture) to optimize CPU latency
- Tightly Coupled Memory (TCM) interface designed for fast and deterministic SRAM accesses
- AXI Bus interface to optimize Burst transfers
- Dedicated low-latency AHB-Lite peripheral bus (AHBP) to connect to peripherals.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

It also supports single and double precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

Refer to Figure 1. STM32H7A3xI/G block diagram for the general block diagram of the STM32H7A3xI/G family.

Note: Cortex®-M7 with FPU core is binary compatible with the Cortex®-M4 core.

3.2 Memory protection unit (MPU)

The memory protection unit (MPU) manages the CPU access rights and the attributes of the system resources. It has to be programmed and enabled before use. Its main purposes are to prevent an untrusted user program to accidentally corrupt data used by the OS and/or by a privileged task, but also to protect data processes or read-protect memory regions.

The MPU defines access rules for privileged accesses and user program accesses. It allows defining up to 16 protected regions that can in turn be divided into up to 8 independent subregions, where region address, size, and attributes can be configured. The protection area ranges from 32 bytes to 4 Gbytes of addressable memory.

When an unauthorized access is performed, a memory management exception is generated.

3.3 Memories

3.3.1 Embedded flash memory

The STM32H7A3xI/G devices embed up to up to 2 Mbytes of flash memory that can be used for storing programs and data.

The flash memory is organized as 137-bit flash words memory that can be used for storing both code and data constants. Each word consists of:

- One flash word (4 words, 16 bytes or 128 bits)
- 9 ECC bits.

The Flash memory is organized as follows:

- For STM32H7AxI: two independent 1 Mbyte banks of user Flash memory, each one containing 128 user sectors of 8 Kbytes each.
  For STM32H7AxG: two independent 512 Kbyte banks of user Flash memory, each one containing 64 user sectors of 8 Kbytes each.
- 128 Kbytes of System Flash memory from which the device can boot.
- 1 Kbyte of OTP (one-time programmable) memory containing option bytes for user configuration.

3.3.2 Embedded SRAM

All devices feature:

- 1 Mbyte of AXI-SRAM mapped onto AXI bus matrix in CPU domain (CD) split into:
  - AXI-SRAM1: 256 Kbytes
  - AXI-SRAM2: 384 Kbytes
  - AXI-SRAM3: 384 Kbytes
- 128 Kbytes of AHB-RAM mapped onto AHB bus matrix in CPU domain (CD) split into:
  - AHB-SRAM1: 64 Kbytes
  - AHB-SRAM2: 64 Kbytes
- 32 Kbytes of SRD-SRAM mapped in Smart Run Domain (SRD)
- 4 Kbytes of backup SRAM

The content of this area is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.

- RAM mapped to TCM interface (ITCM and DTCM):

Both ITCM and DTCM RAMs are 0 wait state memories that are accessible from the CPU or the MDMA (even in Sleep mode) through a specific AHB slave of the CPU(AHBP).

- 64 Kbytes of ITCM-RAM (instruction RAM)

This RAM is connected to ITCM 64-bit interface designed for execution of critical real-times routines by the CPU.

- 128 Kbytes of DTCM-RAM (2x 64 Kbyte DTCM-RAMs on 2x32-bit DTCM ports)

The DTCM-RAM could be used for critical real-time data, such as interrupt service routines or stack/heap memory. Both DTCM-RAMs can be used in parallel (for load/store operations) thanks to the Cortex®-M7 dual issue capability.

3.4 Boot modes

At startup, the boot memory space is selected by the BOOT pin and BOOT_ADDx option bytes, allowing to program any boot memory address from 0x0000 0000 to 0x3FFF FFFF which includes:

- All flash address space
- All RAM address space: ITCM, DTCM RAMs and SRAMs
- The system memory bootloader

The boot loader is located in non-user System memory. It is used to reprogram the flash memory through a serial interface (USART, I2C, SPI, USB-DFU, FDCAN). Refer to *STM32 microcontroller system memory boot mode application note* (AN2606) for details.

3.5 Power supply management

3.5.1 Power supply scheme

- V_{DD} = 1.62 to 3.6 V: external power supply for I/Os, provided externally through V_{DD} pins.
- V_{DDLDO} = 1.62 to 3.6 V: supply voltage for the internal regulator supplying V_{CORE}
- V_{DDA} = 1.62 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL.
- $V_{DD33USB}$ and $V_{DD50USB}$:

$V_{DD50USB}$ can be supplied through the USB cable to generate the $V_{DD33USB}$ via the USB internal regulator. This allows supporting a V_{DD} supply different from 3.3 V.

The USB regulator can be bypassed to supply directly $V_{DD33USB}$ if V_{DD} = 3.3 V.

- V_{DDMMC} = 1.62 to 3.6 V external power supply for independent I/Os. V_{DDMMC} can be higher than V_{DD}. VDDMMC pin should be tied to VDD when it is not used.
- V_{BAT} = 1.2 to 3.6 V: power supply for the V_{SW} domain when V_{DD} is not present.
- V_{CAP}: V_{CORE} supply, which value depends on voltage scaling (0.74 V, 0.9 V, 1.0 V, 1.1 V, 1.2 V or 1.3 V). It is configured through VOS bits in PWR_CR3 register. The V_{CORE} domain is split into two domains the CPU domain (CD) and the Smart Run Domain (SRD).
  - CD domain containing most of the peripherals and the Arm® Cortex®-M7 core
  - SRD domain containing some peripherals and the system control.
- V_{DDSMPS} = 1.62 to 3.6 V: step-down converter power supply
- V_{LXSMPS} = V_{CORE} or 1.8 to 2.5 V: external regulated step-down converter output
- V_{FBSMPS} = V_{CORE} or 1.8 to 2.5 V: external step-down converter feedback voltage sense input

Note: For I/O speed optimization at low V_{DD} supply, refer to Section 3.8 General-purpose input/outputs (GPIOs).

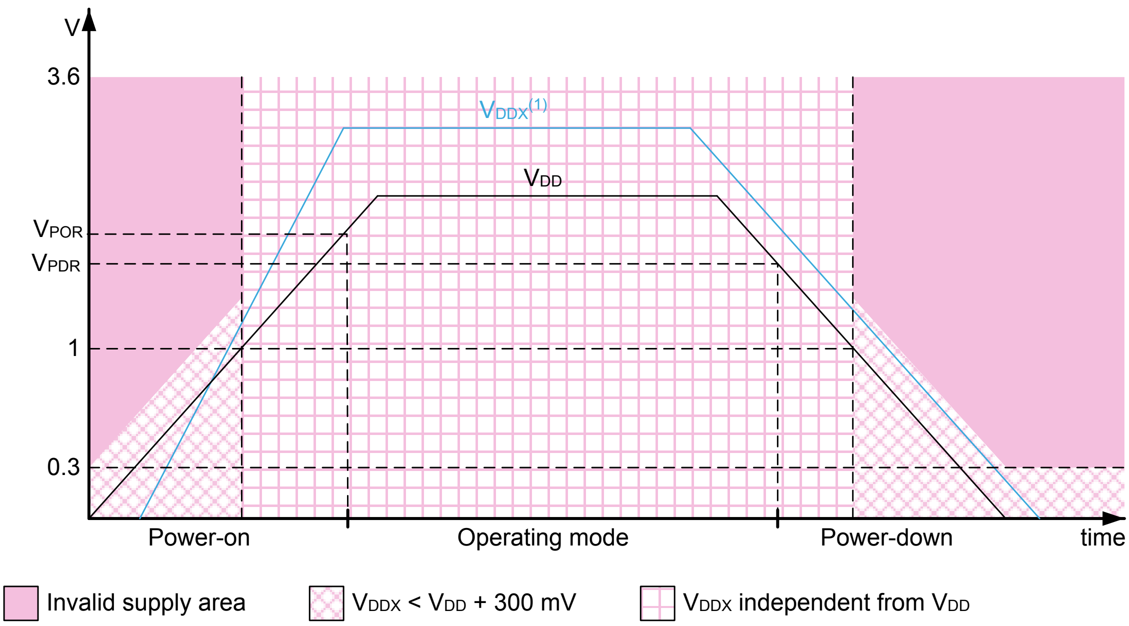
The features available on the device depend on the package (refer to Table 1. STM32H7A3xI/G features and peripheral counts).

During power-up and power-down phases, the following power sequence requirements must be respected (see Figure 2. Power-up/power-down sequence):

- When V_{DD} is below 1 V, other power supplies (V_{DDA}, $V_{DD33USB}$ and $V_{DD50USB}$) must remain below V_{DD} + 300 mV.
- When V_{DD} is above 1 V, all power supplies are independent (except for V_{DDSMPS}, which must remain at the same level as V_{DD}).

During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the microcontroller remains below 1 mJ. This allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

Figure 2. Power-up/power-down sequence



1. V_{DDx} refers to any power supply among V_{DDA}, $V_{DD33USB}$ and $V_{DD50USB}$.
2. V_{DD} and V_{DDSMPS} must be wired together into order to follow the same voltage sequence.

3.5.2 Power supply supervisor

The devices have an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry:

- Power-on reset (POR)
  The POR supervisor monitors V_{DD} power supply and compares it to a fixed threshold. The devices remain in reset mode when V_{DD} is below this threshold,
- Power-down reset (PDR)
  The PDR supervisor monitors V_{DD} power supply. A reset is generated when V_{DD} drops below a fixed threshold.
  The PDR supervisor can be enabled/disabled through PDR_ON pin.
- Brownout reset (BOR)
  The BOR supervisor monitors V_{DD} power supply. Three BOR thresholds (from 2.1 to 2.7 V) can be configured through option bytes. A reset is generated when V_{DD} drops below this threshold.
- Programmable voltage detector (PVD)
  The PVD monitors the V_{DD} power supply by comparing it with a threshold selected from a set of predefined values.
  It can also monitor the voltage level of the PVD_IN pin by comparing it with an internal V_{REFINT} voltage reference level.
- Analog voltage detector (AVD)
  The AVD monitors the V_{DDA} power supply by comparing it with a threshold selected from a set of predefined values.
- V_{BAT} threshold
  The V_{BAT} battery voltage level can be monitored by comparing it with two thresholds levels.
- Temperature threshold
  A dedicated temperature sensor monitors the junction temperature and compare it with two threshold levels.

3.5.3 Voltage regulator

The same voltage regulator supplies the two power domains (CD and SRD). The CD domain can be independently switched off.

Voltage regulator output can be adjusted according to application needs through six power supply levels:

- Run mode (VOS0 to VOS3)
  – Scale 0 and scale 1: high performance
  – Scale 2: medium performance and consumption
  – Scale 3: optimized performance and low-power consumption
- Stop mode (SVOS3 to SVOS5)
  – Scale 3: peripheral with wakeup from stop mode capabilities (UART, SPI, I2C, LPTIM) are operational
  – Scale 4 and 5 where the peripheral with wakeup from Stop mode is disabled
  The peripheral functionality is disabled but wakeup from Stop mode is possible through GPIO or asynchronous interrupt.

3.5.4 SMPS step-down converter

The built-in SMPS step-down converter is a highly power-efficient DC/DC non-linear switching regulator that provides lower power consumption than a conventional voltage regulator (LDO).

The step-down converter can be used to:

- Directly supply the V_{CORE} domain
  – the SMPS step-down converter operating modes follow the device system operating modes (Run, Stop, Standby).
  – the SMPS step-down converter output voltage are set according to the selected VOS and SVOS bits (voltage scaling)

- Provide intermediate voltage level to supply the internal voltage regulator (LDO)
  - The SMPS step-down converter operating modes follow the device system operating modes (Run, Stop, Standby).
  - The SMPS step-down converter output equals 1.8 V or 2.5 V according to the selected step-down level
- Provide an external supply
  - The SMPS step-down converter is forced to external operating mode
  - The SMPS step-down converter output equals 1.8 V or 2.5 V according to the selected step-down level

The 1.8 V or 2.5 V SMPS step-down converter output voltage imposes a minimum V_{DDSMPS} supply of 2.5 V or 3.3 V, respectively. It defines indirectly the minimum V_{DD} supply and I/O level.

3.6 Low-power modes

There are several ways to reduce power consumption on STM32H7A3xI/G:

- Decrease dynamic power consumption by slowing down the system clocks even in Run mode and individually clock gating the peripherals that are not used.
- Save power consumption when the CPU is idle, by selecting among the available low-power mode according to the user application needs. This allows achieving the best compromise between short startup time, low-power consumption, as well as available wakeup sources.

The devices feature several low-power modes:

- System Run with CSleep (CPU clock stopped)
- Autonomous with CD domain in DStop (CPU and CPU Domain bus matrix clocks stopped)
- Autonomous with CD domain in DStop2 (CPU and CPU Domain bus matrix clocks stopped, CPU domain in retention mode)
- System Stop (SRD domain clocks stopped) and CD domain in DStop (CPU and CPU Domain bus matrix clocks stopped)
- System Stop (SRD domain clocks stopped) and CD domain in DStop2 (CPU and CPU Domain bus matrix clocks stopped, CPU domain in retention mode)
- Standby (System, CD and SRD domains powered down)

CSleep and CStop low-power modes are entered by the MCU when executing the WFI (Wait for Interrupt) or WFE (Wait for Event) instructions, or when the SLEEPONEXIT bit of the Cortex®-M7 core is set after returning from an interrupt service routine.

The CPU domain can enter low-power mode (DStop or DStop2) when the processor, its subsystem and the peripherals allocated in the domain enter low-power mode.

If part of the domain is not in low-power mode, the domain remains in the current mode.

Finally the system can enter Stop or Standby when all EXTI wakeup sources are cleared and the power domains are in DStop or DStop2 mode.

Table 2. System vs domain low-power mode

System power mode	CD domain power mode	SRD domain power mode
Run	DRun/DStop/DStop2	DRun
Stop	DStop/DStop2	DStop
Standby	Standby	Standby

Some GPIO pins can be used to monitor CPU and domain power states:

Table 3. Overview of low-power mode monitoring pins

Power state monitoring pins	Description
PWR_CSLEEP	CPU clock OFF
PWR_CSTOP	CPU domain in low-power mode
PWR_NDSTOP2	CPU domain retention mode selection

3.7 Reset and clock controller (RCC)

The clock and reset controller is located in the SRD domain. The RCC manages the generation of all the clocks, as well as the clock gating and the control of the system and peripheral resets. It provides a high flexibility in the choice of clock sources and allows to apply clock ratios to improve the power consumption. In addition, on some communication peripherals that are capable to work with two different clock domains (either a bus interface clock or a kernel peripheral clock), the system frequency can be changed without modifying the baud rate.

3.7.1 Clock management

The devices embed four internal oscillators, two oscillators with external crystal or resonator, two internal oscillators with fast startup time and three PLLs.

The RCC receives the following clock source inputs:

- Internal oscillators:
  - 64 MHz HSI clock (1% accuracy)
  - 48 MHz RC oscillator
  - 4 MHz CSI clock
  - 32 kHz LSI clock
- External oscillators:
  - 4-50 MHz HSE clock
  - 32.768 kHz LSE clock

The RCC provides three PLLs: one for system clock, two for kernel clocks.

The system starts on the HSI clock. The user application can then select the clock configuration.

A high precision can be achieved for the 48 MHz clock by using the embedded clock recovery system (CRS). It uses the USB SOF signal, the LSE or an external signal (SYNC) to fine tune the oscillator frequency on-the- fly.

3.7.2 System reset sources

Power-on reset initializes all registers while system reset reinitializes the system except for the debug, part of the RCC and power controller status registers, as well as the backup power domain.

A system reset is generated in the following cases:

- Power-on reset (pwr_por_rst)
- Brownout reset
- Low level on NRST pin (external reset)
- Window watchdog
- Independent watchdog
- Software reset
- Low-power mode security reset
- Exit from Standby

3.8 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

After reset, all GPIOs are in Analog mode to reduce power consumption.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

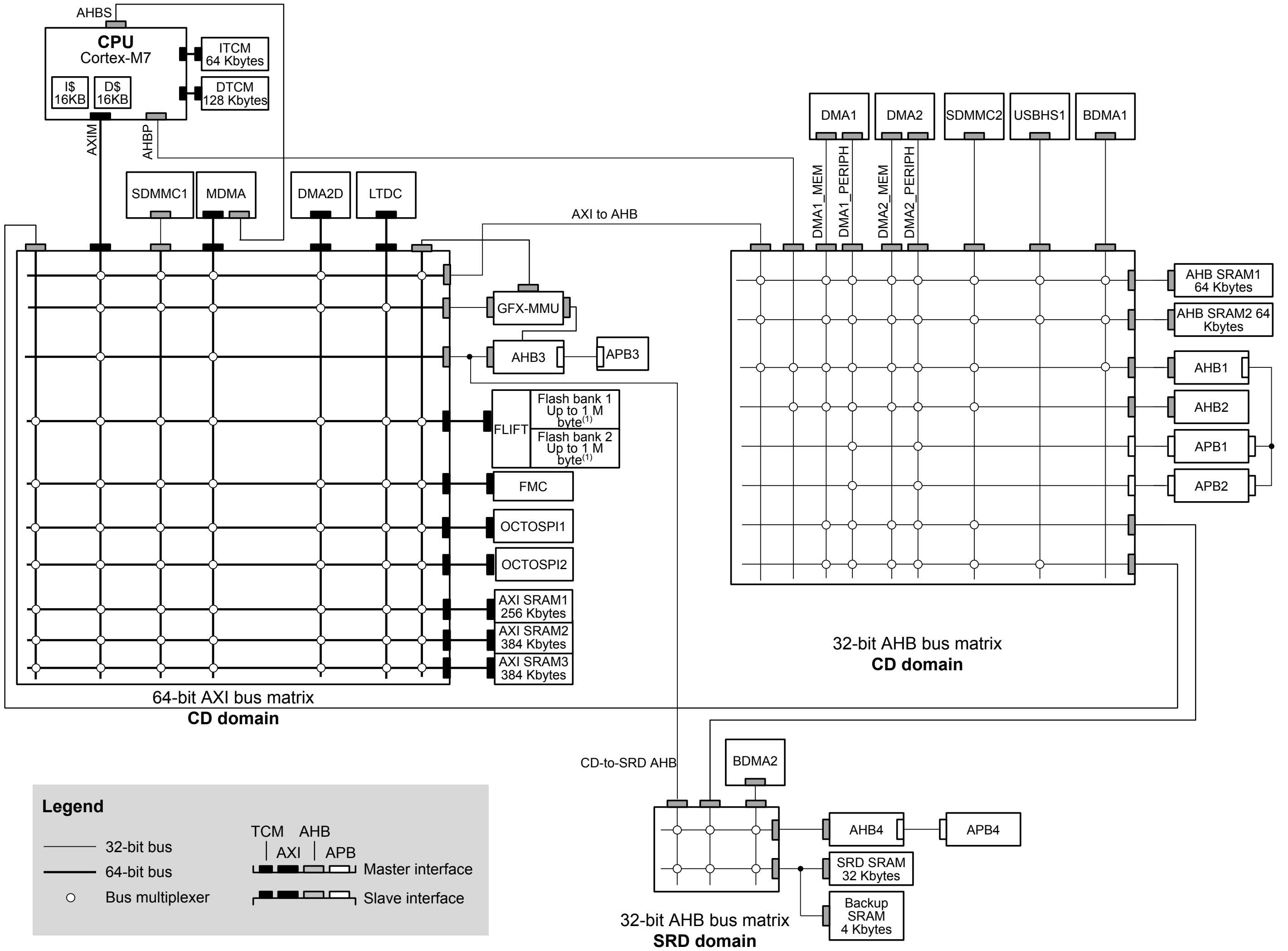
To maximize the performance, the I/O high-speed feature, HSLV, must be activated at low device supply voltage. This is needed to achieve the performance required for peripherals such as the SDMMC, FMC and OCTOSPI. The GPIOs are divided into four groups which can be optimized separately (refer to the description of HSLVx bits of SYSCFG_CCCSR register in RM0455).

The I/O high-speed feature must be used only when V_{DD} is lower than 2.7 V, and both the HSLV user option bits (VDDIO_HSLV and VDDMMC_HSLV) and HSLVx bits must be set to enable it (refer to RM0455 for details).

3.9 Bus-interconnect matrix

The devices feature an AXI bus matrix, two AHB bus matrices and bus bridges that allow interconnecting bus masters with bus slaves (see Figure 3. STM32H7A3xI/G bus matrix).

Figure 3. **STM32H7A3xI/G bus matrix**



1. STM32H7A3xI and STM32H7A3xG devices feature two banks of 1 Mbyte and 512 Kbytes each, respectively.

3.10 DMA controllers

The devices feature five DMA instances to unload CPU activity:

- A master direct memory access (MDMA)

The MDMA is a high-speed DMA controller, which is in charge of all types of memory transfers (peripheral to memory, memory to memory, memory to peripheral), without any CPU action. It features a master AXI interface and a dedicated AHB interface to access Cortex®-M7 TCM memories.

The MDMA is located in the CD domain. It is able to interface with the other DMA controllers located in this domain to extend the standard DMA capabilities, or can manage peripheral DMA requests directly.

Each of the 16 channels can perform single block transfers, repeated block transfers and linked list transfers.

- Two dual-port DMAs (DMA1, DMA2) located in the CD domain and connected to the AHB matrix, with FIFO and request router capabilities.
- One basic DMA (BDMA1) located in the CD domain and connected to the AHB matrix. This DMA is dedicated to the DFSDM (see Section 3.26 Digital filter for sigma-delta modulators (DFSDM))
- One basic DMA (BDMA2) located in the SRD domain, with request router capabilities.

The DMA request router could be considered as an extension of the DMA controller. It routes the DMA peripheral requests to the DMA controller itself. This allowing managing the DMA requests with a high flexibility, maximizing the number of DMA requests that run concurrently, as well as generating DMA requests from peripheral output trigger or DMA event.

3.11 Chrom-ART Accelerator (DMA2D)

The Chrom-Art Accelerator (DMA2D) is a graphical accelerator which offers advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion

Various image format coding are supported, from indirect 4bpp color mode up to 32bpp direct color. It embeds dedicated memory to store color lookup tables. The DMA2D also supports block based YCbCr to handle JPEG decoder output.

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

3.12 Chrom-GRC™ (GFXMMU)

The Chrom-GRC™ is a graphical oriented memory management unit aimed at:

- Optimizing memory usage according to the display shape
- Manage cache linear accesses to the frame buffer
- Prefetch data

The display shape is programmable to store only the visible image pixels.

A virtual memory space is provided which is seen by all system masters and can be physically mapped to any system memory.

An interrupt can be generated in case of buffer overflow or memory transfer error.

3.13 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller which is able to manage 16 priority levels, and handle up to 150 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M7 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor context automatically saved

- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.14 Extended interrupt and event controller (EXTI)

The EXTI controller performs interrupt and event management. In addition, it can wake up the processor, power domains and/or SRD domain from Stop mode.

The EXTI handles up to 89 independent event/interrupt lines split into 28 configurable events and 61 direct events.

Configurable events have dedicated pending flags, active edge selection, and software trigger capable.

Direct events provide interrupts or events from peripherals having a status flag.

3.15 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a programmable polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.16 Flexible memory controller (FMC)

The FMC controller main features are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR flash memory/OneNAND flash memory
  - PSRAM (4 memory banks)
  - NAND flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) memories
- 8-,16-,32-bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- Read FIFO for SDRAM controller
- The maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is the FMC kernel clock divided by 2.

3.17 Octo-SPI memory interface (OCTOSPI)

The OCTOSPI is a specialized communication interface targeting single, dual, quad or octal SPI memories.

The STM32H7A3xI/G embeds two separate Octo-SPI interfaces.

Each OCTOSPI instance supports single/dual/quad/octal SPI formats.

Multiplex of single/dual/quad/octal SPI over the same bus can be achieved using the integrated I/O manager.

The OCTOSPI can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the OCTOSPI registers
- Status-polling mode: the external memory status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external memory is memory mapped and it is seen by the system as if it was an internal memory supporting both read and write operations.

The OCTOSPI support two frame formats supported by most external serial memories such as serial PSRAMs, serial NOR flash memories, Hyper RAMs and Hyper flash memories:

- The classical frame format with the command, address, alternate byte, dummy cycles and data phase
- The HyperBus™ frame format.

Multichip package (MCP) combining any of the above mentioned memory types can also be supported.

3.18 Analog-to-digital converters (ADCs)

The STM32H7A3xI/G devices embed two analog-to-digital converters, whose resolution can be configured to 16, 14, 12, 10 or 8 bits. Each ADC shares up to 24 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller, thus allowing to automatically transfer ADC converted values to a destination location without any software action.

In addition, an analog watchdog feature can accurately monitor the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM6, TIM8, TIM15, and LPTIM1 timers.

3.19 Analog temperature sensor

The STM32H7A3xI/G embeds an analog temperature sensor that generates a voltage (V_{TS}) that varies linearly with the temperature. This temperature sensor is internally connected to ADC2_IN18. The conversion range is between 1.7 V and 3.6 V. It can measure the device junction temperature ranging from −40 to +125 °C.

The temperature sensor have a good linearity, but it has to be calibrated to obtain a good overall accuracy of the temperature measurement. As the temperature sensor offset varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only. To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the System memory area, which is accessible in read-only mode.

3.20 Digital temperature sensor (DTS)

The STM32H7A3xI/G embeds a sensor that converts the temperature into a square wave which frequency is proportional to the temperature. The PCLK or the LSE clock can be used as reference clock for the measurements. A formula given in the product reference manual (RM0455) allows to calculate the temperature according to the measured frequency stored in the DTS_DR register.

3.21 V_{BAT} operation

The V_{BAT} power domain contains the RTC, the backup registers and the backup SRAM.

To optimize battery duration, this power domain is supplied by V_{DD} when available or by the voltage applied on VBAT pin (when V_{DD} supply is not present). V_{BAT} power is switched when the PDR detects that V_{DD} dropped below the PDR level.

The voltage on the VBAT pin could be provided by an external battery, a supercapacitor or directly by V_{DD}, in which case, the V_{DD} mode is not functional.

V_{BAT} operation is activated when V_{DD} is not present.

The VBAT pin supplies the RTC, the backup registers and the backup SRAM.

The devices embed an internal V_{BAT} battery charging circuitry that can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from V_{BAT}, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

When PDR_ON pin is connected to V_{SS} (Internal Reset OFF), the V_{BAT} functionality is no more available and V_{BAT} pin should be connected to VDD.

3.22 Digital-to-analog converters (DAC)

The devices features one dual-channel DAC (DAC1), located in the CD domain, plus one single-channel DAC (DAC2), located in the SRD domain.

The three 12-bit buffered DAC channels can be used to convert three digital signals into three analog voltage signal outputs.

The following feature are supported:

- three DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- Triple DAC channel independent or simultaneous conversions
- DMA capability for each channel including DMA underrun error detection
- external triggers for conversion
- input voltage reference V_{REF+} or internal VREFBUF reference.

The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

3.23 Voltage reference buffer (VREFBUF)

The built-in voltage reference buffer can be used as voltage reference for ADCs and DACs, as well as voltage reference for external components through the VREF+ pin.

Five different voltages are supported (refer to the reference manual for details).

3.24 Ultra-low-power comparators (COMP)

The STM32H7A3xI/G devices embed two rail-to-rail comparators (COMP1 and COMP2). They feature programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) as well as selectable output polarity.

The reference voltage can be one of the following:

- An external I/O
- A DAC output channel
- An internal reference voltage or submultiple (1/4, 1/2, 3/4)
- The analog temperature sensor
- The V_{BAT}/4 supply.

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers, and be combined into a window comparator.

3.25 Operational amplifiers (OPAMP)

The STM32H7A3xI/G devices embed two rail-to-rail operational amplifiers (OPAMP1 and OPAMP2) with external or internal follower routing and PGA capability, and two inputs and one output each. These three I/Os can be connected to the external pins, thus enabling any type of external interconnections. The operational amplifiers can be configured internally as a follower, as an amplifier with a non-inverting gain ranging from 2 to 16 or with inverting gain ranging from -1 to -15.

The operational amplifier main features are:

- PGA with a non-inverting gain ranging of 2, 4, 8 or 16 or inverting gain ranging of -1, -3, -7 or -15
- Up to two positive inputs connected to DAC
- Output connected to internal ADC
- Low input bias current down to 1 nA
- Low input offset voltage down to 1.5 mV
- Gain bandwidth up to 8 MHz

The devices embed two operational amplifiers (OPMAP1 and OPAMP2) with two inputs and one output each. These three I/Os can be connected to the external pins, thus enabling any type of external interconnections. The operational amplifiers can be configured internally as a follower, as an amplifier with a non-inverting gain ranging from 2 to 16 or with inverting gain ranging from -1 to -15.

3.26 Digital filter for sigma-delta modulators (DFSDM)

The device embeds two DFSDM interfaces:

- DSFDM1

  It is located in the CD domain and features eight external digital serial interfaces (channels) and eight digital filters, or alternately eight internal parallel inputs.
- DSFDM2

  It is located in the SRD domain. DFSDM2 is a lite version including two external digital serial interfaces (channels) and one digital filters.

The DFSDM peripherals interface the external ΣΔ modulators to microcontroller and then perform digital filtering of the received data streams (which represent analog value on ΣΔ modulators inputs). DFSDMs can also interface PDM (Pulse Density Modulation) microphones and perform PDM to PCM conversion and filtering in hardware. The DFSDMs feature optional parallel data stream inputs from internal ADC peripherals or microcontroller memory (through DMA/CPU transfers into DFSDM).

DFSDM transceivers support several serial interface formats (to support various ΣΔ modulators). DFSDM digital filter modules perform digital processing according user selected filter parameters with up to 24-bit final ADC resolution.

The DFSDM peripherals support:

- Multiplexed input digital serial channels:
  - configurable SPI interface to connect various SD modulator(s)
  - configurable Manchester coded 1 wire interface support
  - PDM (Pulse Density Modulation) microphone input support
  - maximum input clock frequency up to 20 MHz (10 MHz for Manchester coding)
  - clock output for SD modulator(s): 0..20 MHz
- Alternative inputs from eight internal digital parallel channels (up to 16 bit input resolution):
  - internal sources: ADC data or memory data streams (DMA)
- Digital filter modules with adjustable digital signal processing:
  - $Sinc^x$ filter: filter order/type (1..5), oversampling ratio (up to 1..1024)
  - integrator: oversampling ratio (1..256)
- Up to 24-bit output data resolution, signed output data format
- Automatic data offset correction (offset stored in register by user)
- Continuous or single conversion
- Start-of-conversion triggered by:
  - software trigger
  - internal timers
  - external events
  - start-of-conversion synchronously with first digital filter module (DFSDM0)
- Analog watchdog feature:
  - low value and high value data threshold registers
  - dedicated configurable Sincx digital filter (order = 1..3, oversampling ratio = 1..32)
  - input from final output data or from selected input digital serial channels
  - continuous monitoring independently from standard conversion
- Short circuit detector to detect saturated analog input values (bottom and top range):
  - up to 8-bit counter to detect 1..256 consecutive 0's or 1's on serial data stream
  - monitoring continuously each input serial channel
- Break signal generation on analog watchdog event or on short circuit detector event
- Extremes detector:
  - storage of minimum and maximum values of final conversion data
  - refreshed by software
- DMA capability to read the final conversion data
- Interrupts: end of conversion, overrun, analog watchdog, short circuit, input serial channel clock absence

- “Regular” or “injected” conversions:
  - “regular” conversions can be requested at any time or even in continuous mode without having any impact on the timing of “injected” conversions
  - “injected” conversions for precise timing and with high conversion priority

3.27 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can achieve a data transfer rate up to 140 Mbyte/s using a 80 MHz pixel clock. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

3.28 Parallel synchronous slave interface (PSSI)

The PSSI is a generic synchronous 8-/16-bit parallel data input/output slave interface. It allows the transmitter to send a data valid signal to indicate when the data is valid, and the receiver to output a flow control signal to indicate when it is ready to sample the data.

The PSSI main features are:

- Slave mode operation
- 8- or 16-bit parallel data input or output
- 8-word (32-byte) FIFO
- Data enable (DE) alternate function input and Ready (RDY) alternate function output.

When enabled, these signals can either allow the transmitter to indicate when the data is valid or the receiver to indicate when it is ready to sample the data, or both.

The PSSI shares most of the circuitry with the digital camera interface (DCMI). It thus cannot be used simultaneously with the DCMI.

3.29 LCD-TFT display controller (LTDC)

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 display layers with dedicated FIFO (64x32-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events
- AXI master interface with burst of 16 words

3.30 JPEG codec (JPEG)

The JPEG codec can encode and decode a JPEG stream as defined in the

ISO/IEC10918-1 specification. It provides an fast and simple hardware compressor and decompressor of JPEG images with full management of JPEG headers.

The JPEG codec main features are as follows:

- 8-bit/channel pixel depths
- Single clock per pixel encoding and decoding
- Support for JPEG header generation and parsing

- Up to four programmable quantization tables
- Fully programmable Huffman tables (two AC and two DC)
- Fully programmable minimum coded unit (MCU)
- Encode/decode support (non simultaneous)
- Single clock Huffman coding and decoding
- Two-channel interface: Pixel/Compress In, Pixel/Compressed Out
- Stallable design
- Support for single greyscale component
- Ability to enable/disable header processing
- Internal register interface
- Fully synchronous design
- Configuration for high-speed decode mode

3.31 True random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit. The RNG is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

3.32 Timers and watchdogs

The devices include two advanced-control timers, ten general-purpose timers, two basic timers, three low-power timers, two watchdogs and a SysTick timer.

All timer counters can be frozen in Debug mode.

Table 4. Timer feature comparison compares the features of the advanced-control, general-purpose and basic timers.

Table 4. **Timer feature comparison**

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary output	Max interface clock (MHz)	Max timer clock (MHz) (1)
Advanced-control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	140	280
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	140	280
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	140	280
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	140	280
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	140	280
	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1	140	280
	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1	140	280
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	140	280
Low-power timer	LPTIM1, LPTIM2, LPTIM3	16-bit	Up	1, 2, 4, 8, 16, 32, 64, 128	No	0	No	140	280

1. *The maximum timer clock is up to 280 MHz depending on TIMPRE bit in the RCC_CFGR register and CDPRE1/2 bits in RCC_CDCFGR register.*

3.32.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

The advanced-control timers support independent DMA request generation.

3.32.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32H7A3xI/G devices (see Table 4. Timer feature comparison for differences).

- **TIM2, TIM3, TIM4 and TIM5**

  The devices include 4 full-featured general-purpose timers: TIM2, TIM3, TIM4 and TIM5. TIM2 and TIM5 are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler while TIM3 and TIM4 are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. All timers feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

  TIM2, TIM3, TIM4 and TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers (TIM1, TIM8) via the Timer Link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM outputs.

  TIM2, TIM3, TIM4 and TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM12, TIM13, TIM14, TIM15, TIM16 and TIM17**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM13, TIM14, TIM16 and TIM17 feature one independent channel, whereas TIM12 and TIM15 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4 and TIM5 full-featured general-purpose timers or used as simple time bases.

3.32.3 Basic timers (TIM6 and TIM7)

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

3.32.4 Low-power timers (LPTIM1, LPTIM2, LPTIM3)

The low-power timers feature an independent clock and are running also in Stop mode if they are clocked by LSE, LSI or an external clock. The low-power timers are able to wakeup the devices from Stop mode.

The low-power timers support the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one-shot mode
- Selectable software / hardware input trigger
- Selectable clock source:
- Internal clock source: LSE, LSI, HSI or APB clock
- External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

3.32.5 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

3.32.6 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.32.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

3.33 Real-time clock (RTC)

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to V_{BAT} mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC is supplied through a switch that takes power either from the V_{DD} supply when present or from the V_{BAT} pin.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32.

The RTC is functional in V_{BAT} mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in V_{BAT} mode, but is functional in all low-power modes.

All RTC events (Alarm, Wakeup Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

3.34 Tamper and backup registers (TAMP)

The TAMP main features are the following:

- 32 backup registers:
  – The backup registers (TAMP_BKPxR) are implemented in the RTC domain that remains powered-on by V_{BAT} when the V_{DD} power is switched off.
- Three external tamper detection events
  – Each external event can be configured to be active or passive
  – External passive tampers with configurable filter and internal pull-up
- Seven internal tamper events
- Any tamper detection can generate an RTC timestamp event
- Any tamper detection can erase the RTC backup registers and the backup SRAM
- Monotonic counter

3.35 Inter-integrated circuit interface (I^2C)

The STM32H7A3xI/G embed four I^2C interfaces.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bit rate up to 100 kbit/s
  - Fast-mode (Fm), with a bit rate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System management bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus®) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming.
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

3.36 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32H7A3xI/G devices have five embedded universal synchronous receiver transmitters (USART1, USART2, USART3, USART6 and USART10) and five universal asynchronous receiver transmitters (UART4, UART5, UART7, UART8 and UART9). Refer to the table below for a summary of USARTx and UARTx features.

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. They provide hardware management of the CTS and RTS signals, and RS485 Driver Enable. They are able to communicate at speeds of up to 10Mbit/s.

USART1, USART2, USART3, USART6 and USART10 also provide Smartcard mode (ISO 7816 compliant) and SPI-like communication capability.

The USARTs embed a Transmit FIFO (TXFIFO) and a Receive FIFO (RXFIFO). FIFO mode is enabled by software and is disabled by default.

All USART have a clock domain independent from the CPU clock, allowing the USARTx to wake up the MCU from Stop mode.The wakeup from Stop mode are programmable and can be done on:

- Start bit detection
- Any received data frame
- A specific programmed data frame
- Specific TXFIFO/RXFIFO status when FIFO mode is enabled.

All USART interfaces can be served by the DMA controller.

Table 5. USART features

X = supported.

USART modes/features	USART1/2/3/6/10	UART4/5/7/8/9
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode (Master/Slave)	X	-
Smartcard mode	X	-
Single-wire Half-duplex communication	X	X
IrDA SIR ENDEC block	X	X

USART modes/features	USART1/2/3/6/10	UART4/5/7/8/9
LIN mode	X	X
Dual clock domain and wakeup from low power mode	X	X
Receiver timeout interrupt	X	X
Modbus communication	X	X
Auto baud rate detection	X	X
Driver Enable	X	X
USART data length	7, 8 and 9 bits	
Tx/Rx FIFO	X	X
Tx/Rx FIFO size	16	

3.37 Low-power universal asynchronous receiver transmitter (LPUART)

The device embeds one Low-power UART (LPUART1). The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART embeds a Transmit FIFO (TXFIFO) and a Receive FIFO (RXFIFO). FIFO mode is enabled by software and is disabled by default.

The LPUART has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode. The wakeup from Stop mode are programmable and can be done on:

- Start bit detection
- Any received data frame
- A specific programmed data frame
- Specific TXFIFO/RXFIFO status when FIFO mode is enabled.

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baud rates.

LPUART interface can be served by the DMA controller.

3.38 Serial peripheral interfaces (SPI)/integrated interchip sound interfaces (I2S)

The devices feature up to six SPIs (SPI1/I2S1, SPI2/I2S2, SPI3/I2S3, SPI6/I2S6 and SPI4, SPI5) that allow communicating up to 125 Mbits/s in master and slave modes, in half-duplex, full-duplex and simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable from 4 to 32 bits for SPI1/I2S1, SPI2/I2S2, SPI3/I2S3, from 4 to 16 bits for the others. All SPI interfaces support SS pulse mode, TI mode, Hardware CRC calculation, and 16x 8-bit embedded Rx and Tx FIFOs (SPI1/I2S1, SPI2/I2S2, SPI3/I2S3) or 8x 8-bit embedded Rx and Tx FIFOs (SPI4, SPI5, SPI6/I2S6), all with DMA capability. .

Four standard I^{2}S interfaces (multiplexed with SPI1, SPI2, SPI3, SPI6) are available. They can be operated in master or slave mode, in simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When one or all I^{2}S interfaces is/are configured in master mode, the master clock can be output to the external DAC/codec at 256 times the sampling frequency. All I^{2}S interfaces support 16x 8-bit embedded Rx and Tx FIFOs with DMA capability.

3.39 Serial audio interfaces (SAI)

The devices embed two SAIs (SAI1, SAI2) that allow designing many stereo or mono audio protocols such as I2S, LSB or MSB-justified, PCM/DSP, TDM or AC’97. An SPDIF output is available when the audio block is configured as a transmitter. To bring this level of flexibility and reconfigurability, the SAI contains two independent audio sub-blocks. Each block has it own clock generator and I/O line controller.

Audio sampling frequencies up to 192 kHz are supported.

One of the SAI supports up to 8 microphones thanks to an embedded PDM interface.

The SAI can work in master or slave configuration. The audio sub-blocks can be either receiver or transmitter and can work synchronously or asynchronously (with respect to the other one). The SAI can be connected with other SAIs to work synchronously.

3.40 SPDIFRX receiver interface (SPDIFRX)

The SPDIFRX peripheral is designed to receive an S/PDIF flow compliant with IEC-60958 and IEC-61937. These standards support simple stereo streams up to high sample rate, and compressed multi-channel surround sound, such as those defined by Dolby or DTS (up to 5.1).

The main SPDIFRX features are the following:

- Up to 4 inputs available
- Automatic symbol rate detection
- Maximum symbol rate: 12.288 MHz
- Stereo stream from 32 to 192 kHz supported
- Supports Audio IEC-60958 and IEC-61937, consumer applications
- Parity bit management
- Communication using DMA for audio samples
- Communication using DMA for control and user channel information
- Interrupt capabilities

The SPDIFRX receiver provides all the necessary features to detect the symbol rate, and decode the incoming data stream. The user can select the wanted SPDIF input, and when a valid signal will be available, the SPDIFRX will re-sample the incoming signal, decode the Manchester stream, recognize frames, sub-frames and blocks elements. It delivers to the CPU decoded data, and associated status flags.

The SPDIFRX also offers a signal named spdif_frame_sync, which toggles at the S/PDIF sub-frame rate that will be used to compute the exact sample rate for clock drift algorithms.

3.41 Single wire protocol master interface (SWPMI)

The single wire protocol master interface (SWPMI) is the master interface corresponding to the contactless frontend (CLF) defined in the ETSI TS 102 613 technical specification. The main features are:

- full-duplex communication mode
- automatic SWP bus state management (active, suspend, resume)
- configurable bit rate up to 2 Mbit/s
- automatic SOF, EOF and CRC handling

SWPMI can be served by the DMA controller.

3.42 Management data input/output (MDIO) slaves

The devices embed an MDIO slave interface it includes the following features:

- 32 MDIO register addresses, each of which is managed using separate input and output data registers:
  - 32 x 16-bit firmware read/write, MDIO read-only output data registers
  - 32 x 16-bit firmware read-only, MDIO write-only input data registers
- Configurable slave (port) address
- Independently maskable interrupts/events:
  - MDIO register write
  - MDIO register read
  - MDIO protocol error
- Able to operate in and wake up from STOP mode

3.43 SD/SDIO/MMC card host interfaces (SDMMC)

Two SDMMC host interfaces are available. They support *MultiMediaCard System Specification* version 4.51 in three different databus modes: 1 bit (default), 4 bits and 8 bits.

One of the SDMMC interface can be supplied through a separate V_{DDMMC} supply. If required, it can thus operate at a different voltage level than all other I/Os.

Both interfaces support the *SD memory card specifications* version 4.1. and the *SDIO card specification* version 4.0. in two different databus modes: 1 bit (default) and 4 bits.

Each SDMMC host interface supports only one SD/SDIO/MMC card at any one time and a stack of MMC Version 4.51 or previous.

The SDMMC host interface embeds a dedicated DMA controller allowing high-speed transfers between the interface and the SRAM.

3.44 Controller area network (FDCAN1, FDCAN2)

The controller area network (CAN) subsystem consists of two CAN modules, a shared message RAM memory and a clock calibration unit.

Both CAN modules (FDCAN1 and FDCAN2) are compliant with ISO 11898-1 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

FDCAN1 supports time triggered CAN (TTCAN) specified in ISO 11898-4, including event synchronized time-triggered communication, global system time, and clock drift compensation. FDCAN1 contains additional registers, specific to the time triggered feature. The CAN FD option can be used together with event-triggered and time-triggered CAN communication.

A 10 Kbyte message RAM memory implements filters, receive FIFOs, receive buffers, transmit event FIFOs, transmit buffers (and triggers for TTCAN). This message RAM is shared between the two FDCAN1 and FDCAN2 modules.

The common clock calibration unit is optional. It can be used to generate a calibrated clock for both FDCAN1 and FDCAN2 from the HSI internal RC oscillator and the PLL, by evaluating CAN messages received by the FDCAN1.

3.45 Universal serial bus on-the-go high-speed (OTG_HS)

The devices embed an USB OTG high-speed (up to 480 Mbit/s) device/host/OTG peripheral that supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 Mbit/s) and a UTMI low-pin interface (ULPI) for high-speed operation (480 Mbit/s). When using the USB OTG_HS interface in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG_HS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It features software-configurable endpoint setting and supports suspend/resume. The USB OTG_HS controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The main features are:

- Combined Rx and Tx FIFO size of 4 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 8 bidirectional endpoints
- 16 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Battery Charging Specification Revision 1.2 support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode

The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.

- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

3.46 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the consumer electronics control (CEC) protocol (supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI-CEC controller to wake up the MCU from Stop mode on data reception.

3.47 Debug infrastructure

The devices offer a comprehensive set of debug and trace features to support software development and system integration.

- Breakpoint debugging
- Code execution tracing
- Software instrumentation
- JTAG debug port
- Serial-wire debug port
- Trigger input and output
- Serial-wire trace port
- Trace port
- Arm® CoreSight™ debug and trace components

The debug can be controlled via a JTAG/Serial-wire debug access port, using industry standard debugging tools.

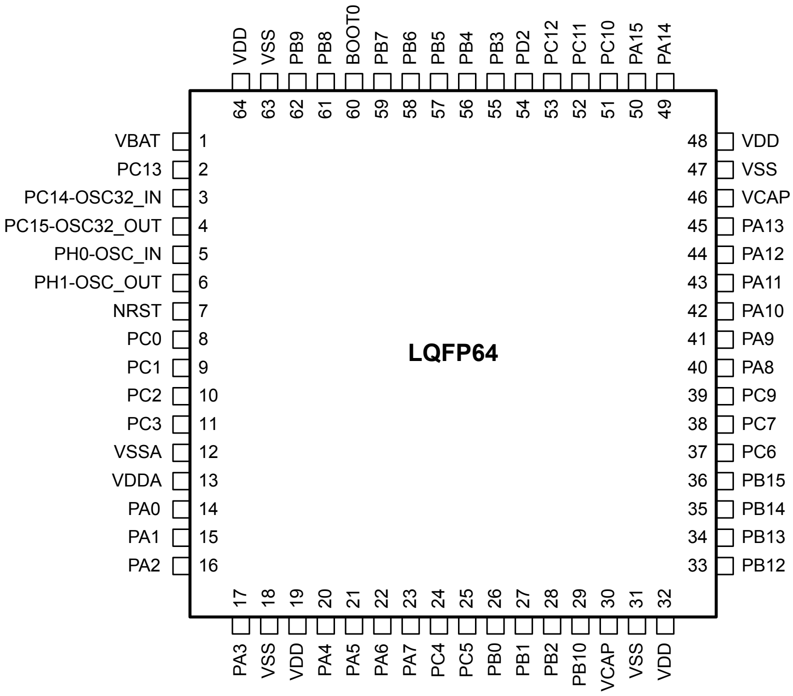
The trace port performs data capture for logging and analysis.

4 Memory mapping

Refer to the product line reference manual (RM0455) for details on the memory mapping as well as the boundary addresses for all peripherals.

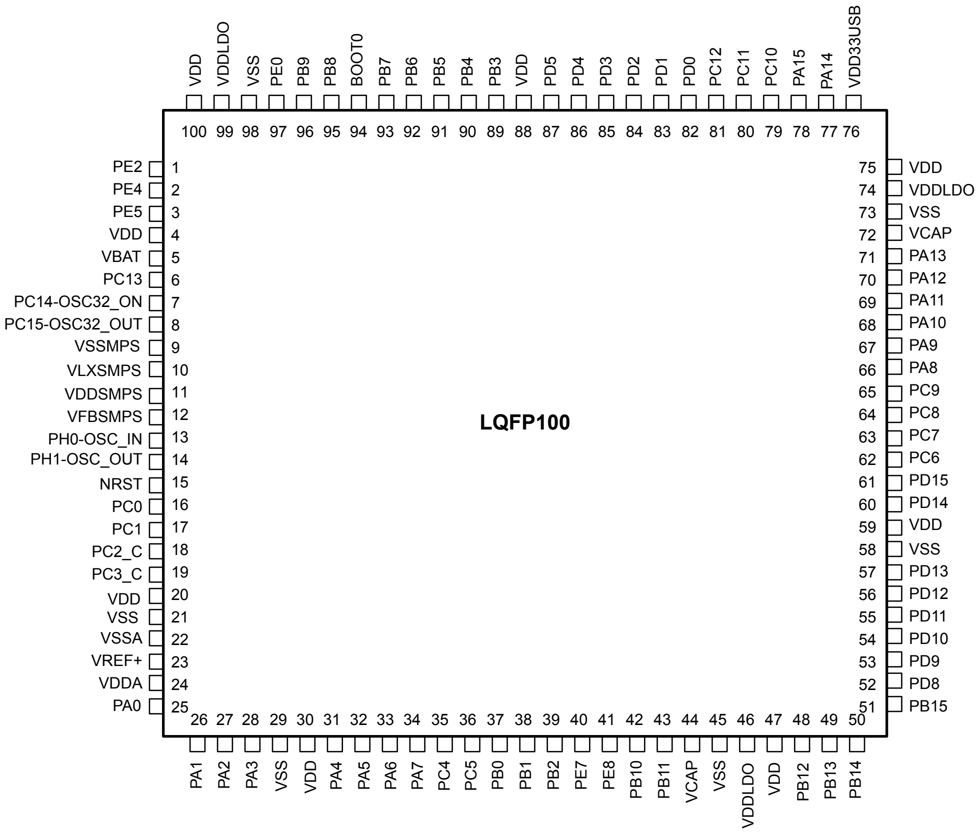
5 Pin descriptions

Figure 4. LQFP64 (STM32H7A3xI/G without SMPS) pinout



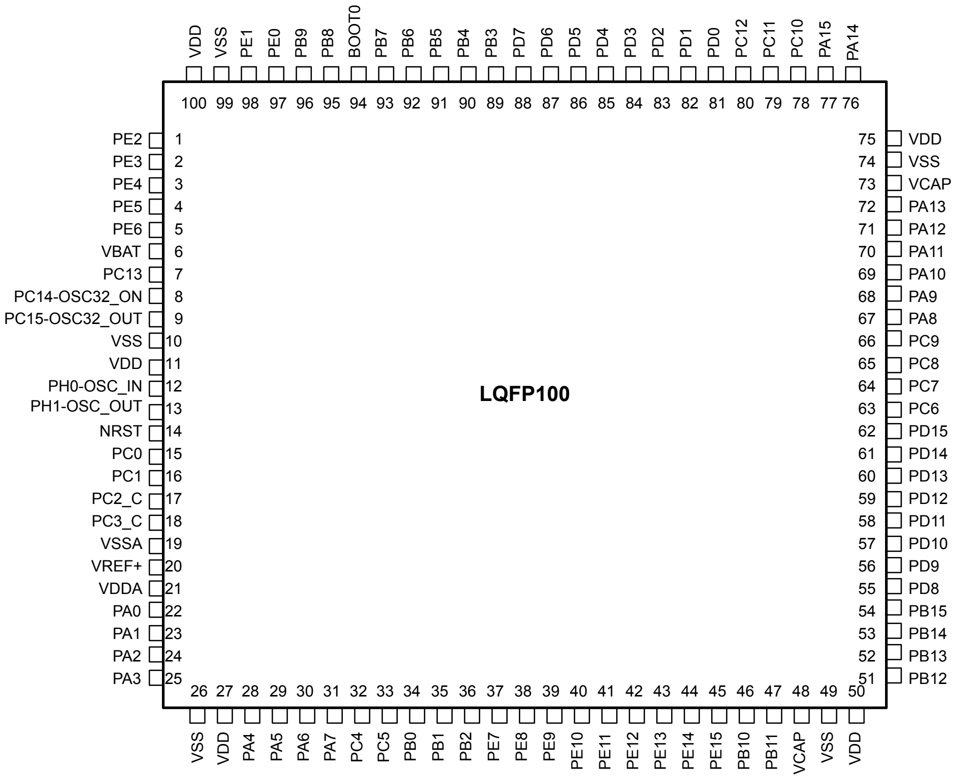
1. The above figure shows the package top view.

Figure 5. LQFP100 (STM32H7A3xI/G with SMPS) pinout



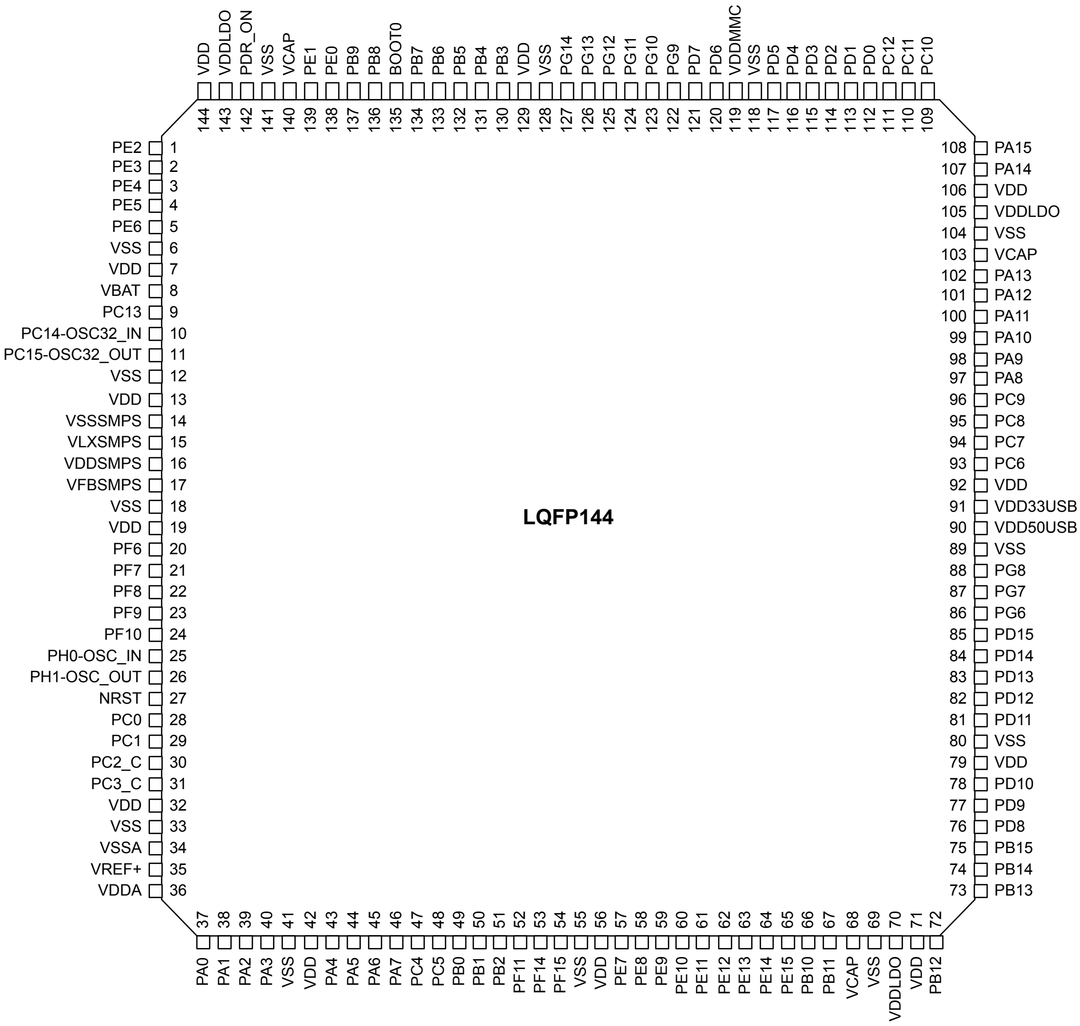
1. The above figure shows the package top view.
2. The devices with SMPS correspond to commercial codes STM32H7A3VIT6Q and STM32H7A3VGT6Q.

Figure 6. LQFP100 (STM32H7A3xI/G without SMPS) pinout



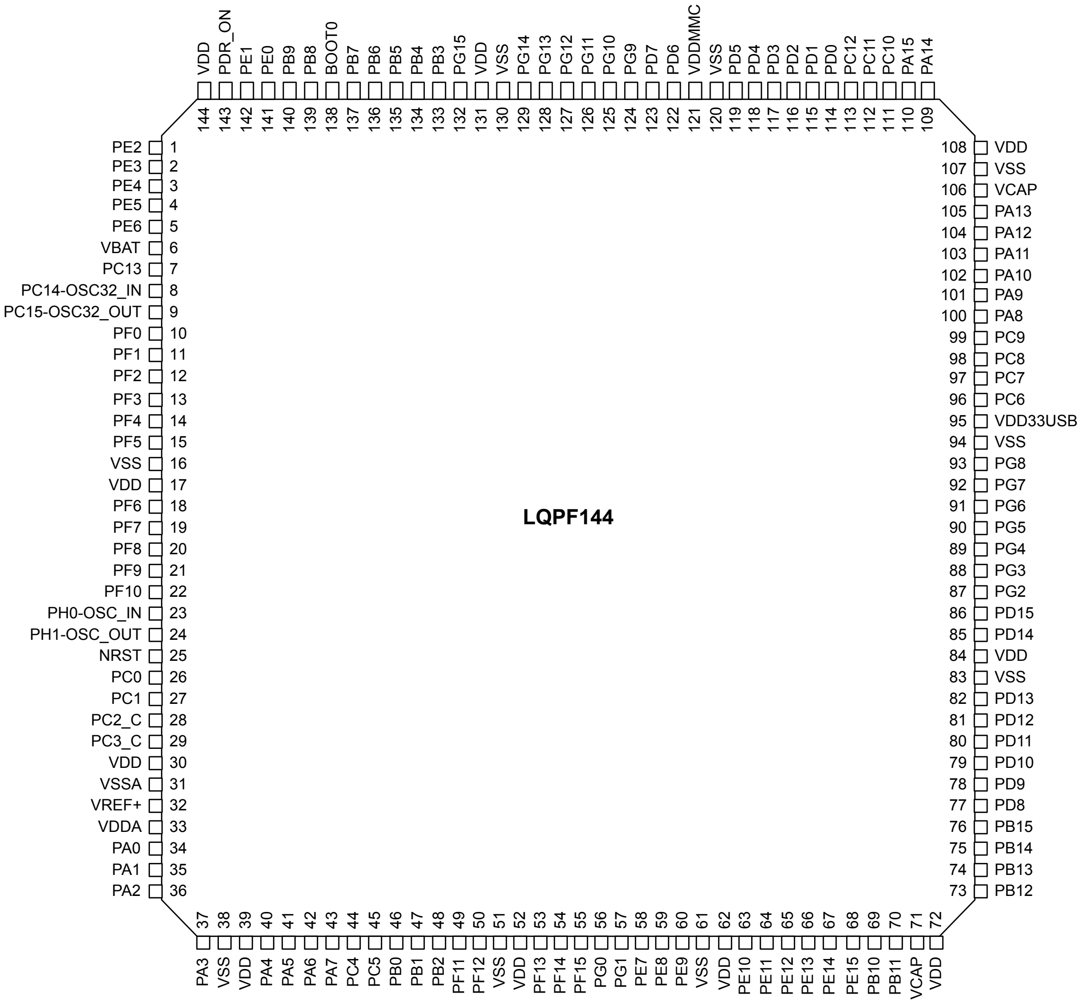
1. The above figure shows the package top view.

Figure 7. LQFP144 (STM32H7A3xI/G with SMPS) pinout



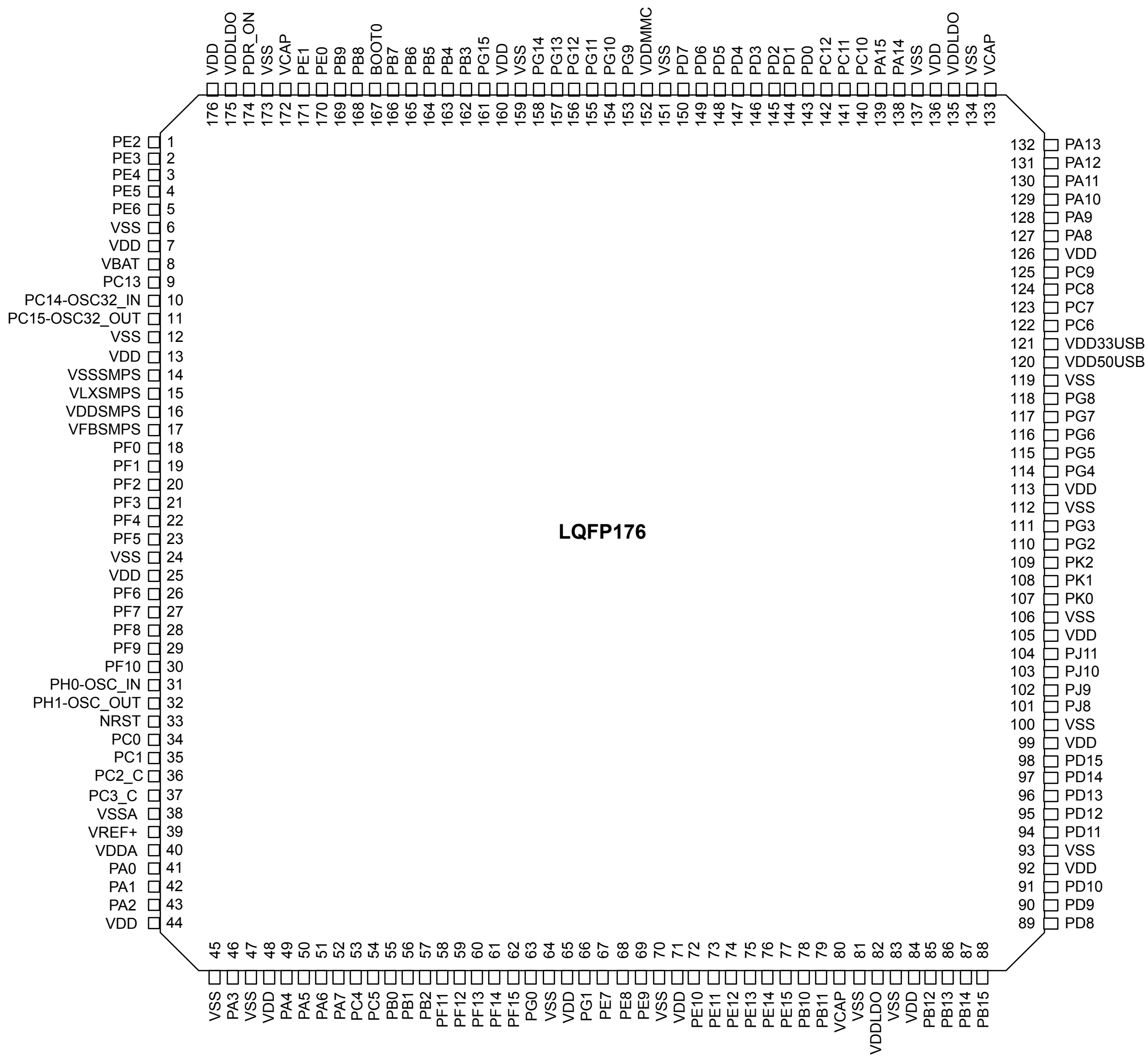
1. The above figure shows the package top view.
2. The devices with SMPS correspond to commercial codes STM32H7A3ZIT6Q and STM32H7A3ZGT6Q.

Figure 8. LQFP144 (STM32H7A3xI/G without SMPS) pinout



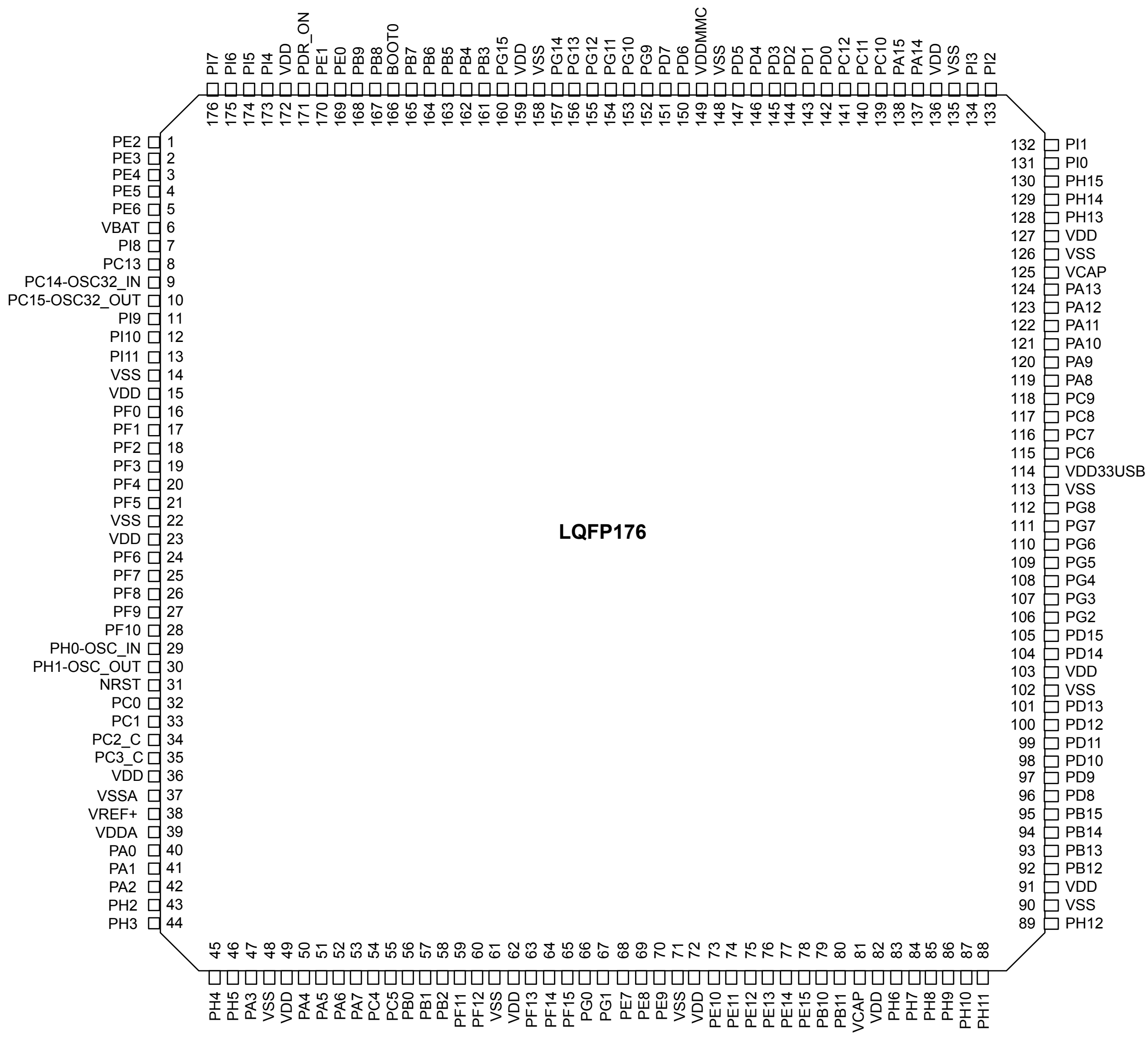
1. The above figure shows the package top view.

Figure 9. LQFP176 (STM32H7A3xI/G with SMPS) pinout



1. The above figure shows the package top view.
2. The devices with SMPS correspond to commercial codes STM32H7A3IIT6Q and STM32H7A3IGT6Q.

Figure 10. LQFP176 (STM32H7A3xI/G without SMPS) pinout



1. The above figure shows the package top view.

Figure 11. TFBGA100 (STM32H7A3xI/G with SMPS) pinout

	1	2	3	4	5	6	7	8	9	10
A	PE6	PE5	PE2	PB8	BOOT0	PB5	PD6	PD3	PD2	PC12
B	PC14-OSC32_IN	PC15-OSC32_OUT	PE3	PE0	PB7	PB3	PD4	PD1	PC11	PC10
C	VSS	VBAT	PE4	PE1	PB4	PD7	PD0	PA15	PA14	PA13
D	VSSSMPS	VLXSMPS	PDR_ON	PB6	VSS	VDD	PD5	VCAP	PA12	PA11
E	VDDSMPS	VFBSMPS	PB9	PC13	VDD	VDDLDO	VSS	VDD33 USB	PA9	PA10
F	PC1	NRST	PC0	PC2_C	VSS	VDD	VDD50 USB	PC6	PC9	PA8
G	PH0-OSC_IN	PH1-OSC_OUT	PA0	PC3_C	PA3	VCAP	PD14	PD15	PC7	PC8
H	VDDA	VSSA	PA2	PC4	PE7	PE10	PD11	PD9	PD12	PD13
J	VREF+	PA1	PA6	PC5	PB2	PE8	PB11	PB13	PD8	PD10
K	PA4	PA5	PA7	PB0	PB1	PE9	PB10	PB12	PB14	PB15

1. The above figure shows the package top view.
2. The devices with SMPS correspond to commercial codes STM32H7A3VIH6Q and STM32H7A3VGH6Q.

Figure 12. TFBGA100 (STM32H7A3xI/G without SMPS) pinout

	1	2	3	4	5	6	7	8	9	10
A	PC14-OSC32_IN	PC13	PE2	PB9	PB7	PB4	PB3	PA15	PA14	PA13
B	PC15-OSC32_OUT	VBAT	PE3	PB8	PB6	PD5	PD2	PC11	PC10	PA12
C	PH0-OSC_IN	VSS	PE4	PE1	PB5	PD6	PD3	PC12	PA9	PA11
D	PH1-OSC_OUT	VDD	PE5	PE0	BOOT0	PD7	PD4	PD0	PA8	PA10
E	NRST	PC2_C	PE6	VSS	VSS	VSS	VCAP	PD1	PC9	PC7
F	PC0	PC1	PC3_C	VDD	VDD	VDD33 USB	PDR_ON	VCAP	PC8	PC6
G	VSSA	PA0	PA4	PC4	PB2	PE10	PE14	PD15	PD11	PB15
H	VDDA	PA1	PA5	PC5	PE7	PE11	PE15	PD14	PD10	PB14
J	VSS	PA2	PA6	PB0	PE8	PE12	PB10	PB13	PD9	PD13
K	VDD	PA3	PA7	PB1	PE9	PE13	PB11	PB12	PD8	PD12

1. The above figure shows the package top view.

Figure 13. **TFBGA216 (STM32H7A3xI/G without SMPS) ballout**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	PE4	PE3	PE2	PG14	PE1	PE0	PB8	PB5	PB4	PB3	PD7	PC12	PA15	PA14	PA13
B	PE5	PE6	PG13	PB9	PB7	PB6	PG15	PG11	PJ13	PJ12	PD6	PD0	PC11	PC10	PA12
C	VBAT	PI8	PI4	PK7	PK6	PK5	PG12	PG10	PJ14	PD5	PD3	PD1	PI3	PI2	PA11
D	PC13	PF0	PI5	PI7	PI10	PI6	PK4	PK3	PG9	PJ15	PD4	PD2	PH15	PI1	PA10
E	PC14-OSC32_IN	PF1	PI12	PI9	PDR_ON	BOOT0	VDD	VDD	VDD MMC	VDD	VCAP	PH13	PH14	PI0	PA9
F	PC15-OSC32_OUT	VSS	PI11	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VDD	PK1	PK2	PC9	PA8
G	PH0-OSC_IN	PF2	PI13	PI15	VDD	VSS				VSS	VDD33 USB	PJ11	PK0	PC8	PC7
H	PH1-OSC_OUT	PF3	PI14	PH4	VDD	VSS				VSS	VDD	PJ8	PJ10	PG8	PC6
J	NRST	PF4	PH5	PH3	VDD	VSS				VSS	VDD	PJ7	PJ9	PG7	PG6
K	PF7	PF6	PF5	PH2	VDD	VSS	VSS	VSS	VSS	VSS	VDD	PJ6	PD15	PB13	PD10
L	PF10	PF9	PF8	PC3_C	VSS	VSS	VDD	VDD	VDD	VDD	VCAP	PD14	PB12	PD9	PD8
M	VSSA	PC0	PC1	PC2_C	PB2	PF12	PG1	PF15	PJ4	PD12	PD13	PG3	PG2	PJ5	PH12
N	VREF-	PA1	PA0	PA4	PC4	PF13	PG0	PJ3	PE8	PD11	PG5	PG4	PH7	PH9	PH11
P	VREF+	PA2	PA6	PA5	PC5	PF14	PJ2	PF11	PE9	PE11	PE14	PB10	PH6	PH8	PH10
R	VDDA	PA3	PA7	PB1	PB0	PJ0	PJ1	PE7	PE10	PE12	PE15	PE13	PB11	PB14	PB15

1. The above figure shows the package top view.

Figure 14. TFBGA225 (STM32H7A3xI/G with SMPS) ballout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	VSS	PI4	PB9	PB6	PG15	PK5	PG14	PG10	PG9	PD7	PD4	PD1	PC10	PI3	VSS
B	PE3	PI5	PE0	PB8	PB4	PK6	PK3	PG11	PJ15	PD6	PD2	PC12	PA14	PH15	PH14
C	PI8	PE4	PI6	PE1	BOOT0	PB3	PK4	PG12	PJ14	PD5	PD0	PA15	PI0	PA12	PA11
D	PC14-OSC32_IN	PC15-OSC32_OUT	PE5	PI7	PDR_ON	PB7	PK7	PG13	PJ13	PD3	PC11	PI2	PH13	VSS	VDD50 USB
E	VSS	VBAT	PI9	PE6	PE2	VCAP	PB5	VDD MMC	PJ12	VDDLDO	PI1	PA13	PA10	PC9	PC7
F	VLX SMPS	VFB SMPS	PI10	PC13	VDDLDO	VSS	VDD	VSS	VDD	VSS	VCAP	PA9	PC8	PC6	PG8
G	VDD SMPS	VSS SMPS	PF1	PF0	PI11	VDD	VDD	VSS	VDD	VDD	PA8	PG7	PG6	PG5	PG3
H	PF2	PI12	PF4	PI14	PI13	VSS	VSS	VSS	VSS	VSS	VDD33 USB	PG4	PG2	PK2	PK1
J	PF3	PF5	PF6	PF7	PC2	VDD	VDD	VSS	VDD	VDD	PJ11	PK0	PJ10	PJ9	PJ8
K	PF8	PF9	NRST	VREF-	VSSA	VSS	VDD	VSS	VDD	VSS	PD13	PD14	PD15	PJ6	PJ7
L	PH0-OSC_IN	PH1-OSC_OUT	PC0	VREF+	VDDA	PA4	PB1	VCAP	PE12	VDDLDO	PH12	PD8	PD10	PD11	PD12
M	VSS	PC1	PF10	PH2	PH4	PC4	PI15	PF13	PE7	PE13	PH6	PH10	PB13	PB14	PB15
N	PC2_C	PC3_C	PC3	PH3	PA5	PC5	PJ0	PF11	PF15	PE14	PE10	PJ5	PH9	PB12	PD9
P	PA0	PA1	PA0_C	PH5	PA6	PB0	PJ1	PJ4	PF14	PG1	PE9	PE15	PB11	PH8	PH11
R	VSS	PA2	PA1_C	PA3	PA7	PB2	PJ2	PJ3	PF12	PG0	PE8	PE11	PB10	PH7	VSS

1. The above figure shows the package top view.

Figure 15. UFBGA169 (STM32H7A3xI/G with SMPS) ballout

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	PE4	PE2	VDD	VCAP	PB6	VDDMMC	VDD	PG10	PD5	VDD	PC12	PC10	PH14
B	PC15-OSC32_OUT	PE3	VSS	VDDLDO	PB8	PB4	VSS	PG11	PD6	VSS	PC11	PA14	PH13
C	PC14-OSC32_IN	PE6	PE5	PDR_ON	PB9	PB5	PG14	PG9	PD4	PD1	PA15	VSS	VDD
D	VDD	VSS	PC13	PE1	PE0	PB7	PG13	PD7	PD3	PD0	PA13	VDDLDO	VCAP
E	VLXSMPS	VSSSMPS	VBAT	PF1	PF3	BOOT0	PG15	PG12	PD2	PA10	PA9	PA8	PA12
F	VDDSMPS	VFBSMPS	PF0	PF2	PF5	PF7	PB3	PG4	PC6	PC7	PC9	PC8	PA11
G	VDD	VSS	PF4	PF6	PF9	NRST	PF13	PE7	PG6	PG7	PG8	VDD50USB	VDD33USB
H	PH0-OSC_IN	PH1-OSC_OUT	PF10	PF8	PC2	PA4	PF14	PE8	PG2	PG3	PG5	VSS	VDD
J	PC0	PC1	VSSA	PC3	PA0	PA7	PF15	PE9	PE14	PD11	PD13	PD15	PD14
K	PC3_C	PC2_C	PA0_C	PA1	PA6	PC4	PG0	PE13	PH10	PH12	PD9	PD10	PD12
L	VDDA	VREF+	PA1_C	PA5	PB1	PB2	PG1	PE12	PB10	PH11	PB13	VSS	VDD
M	VDD	VSS	PH3	VSS	PB0	PF11	VSS	PE10	PB11	VDDLDO	VSS	PD8	PB15
N	PA2	PH2	PA3	VDD	PC5	PF12	VDD	PE11	PE15	VCAP	VDD	PB12	PB14

1. The above figure shows the package top view.

Figure 16. UFBGA176+25 (STM32H7A3xI/G with SMPS) ballout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	VSS	PB8	VDDLDO	VCAP	PB6	PB3	PG11	PG9	PD3	PD1	PA15	PA14	VDDLDO	VCAP	VSS
B	PE4	PE3	PB9	PE0	PB7	PB4	PG13	PD7	PD5	PD2	PC12	PH14	PA13	PA8	PA12
C	PC13	VSS	PE2	PE1	BOOT0	PB5	PG14	PG10	PD4	PD0	PC11	PC10	PH13	PA10	PA11
D	PC15-OSC32_OUT	PC14-OSC32_IN	PE5	PDR_ON	VDD MMC	VSS	PG15	PG12	PD6	VSS	VDD	PH15	PA9	PC8	PC7
E	VSS	VBAT	PE6	VDD								VDD	PC9	PC6	VDD50 USB
F	VLX SMPS	VSS SMPS	PF1	PF0		VSS	VSS	VSS	VSS	VSS		VSS	VDD33 USB	PG6	PG5
G	VDD SMPS	VFB SMPS	PF2	VDD		VSS	VSS	VSS	VSS	VSS		PG8	PG7	PG4	PG2
H	PF6	PF4	PF5	PF3		VSS	VSS	VSS	VSS	VSS		VDD	PG3	PD14	PD13
J	PH0-OSC_IN	PF8	PF7	PF9		VSS	VSS	VSS	VSS	VSS		PD15	PD11	VSS	PD12
K	PH1-OSC_OUT	VSS	PF10	VDD		VSS	VSS	VSS	VSS	VSS		VSS	PD9	PB15	PB14
L	NRST	PC0	PC1	VREF−								VDD	PD10	PD8	PB13
M	PC2	PC3	VREF+	VDDA	VDD	VSS	PC5	PB1	VDD	VSS	PH7	PE14	PH11	PH9	PB12
N	PC2_C	PC3_C	VSSA	PH2	PA3	PA7	PF11	PE8	PG1	PF15	PF13	PB10	PH8	PH10	PH12
P	PA0	PA1	PA1_C	PH4	PA4	PA5	PB2	PG0	PE7	PB11	PF12	PE12	PE13	PE15	PH6
R	VSS	PA2	PA0_C	PH3	PH5	PC4	PA6	PB0	PE10	PF14	PE9	PE11	VCAP	VDDLDO	VSS

1. The above figure shows the package top view.
2. The devices with SMPS correspond to commercial codes STM32H7A3IIK6Q and STM32H7A3IGK6Q.

Figure 17. UFBGA176+25 (STM32H7A3xI/G without SMPS) ballout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	PE3	PE2	PE1	PE0	PB8	PB5	PG14	PG13	PB4	PB3	PD7	PC12	PA15	PA14	PA13
B	PE4	PE5	PE6	PB9	PB7	PB6	PG15	PG12	PG11	PG10	PD6	PD0	PC11	PC10	PA12
C	VBAT	PI7	PI6	PI5	VDD	PDR_ON	VDD	VDD MMC	VDD	PG9	PD5	PD1	PI3	PI2	PA11
D	PC13	PI8	PI9	PI4	VSS	BOOT0	VSS	VSS	VSS	PD4	PD3	PD2	PH15	PI1	PA10
E	PC14-OSC32_IN	PF0	PI10	PI11								PH13	PH14	PI0	PA9
F	PC15-OSC32_OUT	VSS	VDD	PH2		VSS	VSS	VSS	VSS	VSS		VSS	VCAP	PC9	PA8
G	PH0-OSC_IN	VSS	VDD	PH3		VSS	VSS	VSS	VSS	VSS		VSS	VDD	PC8	PC7
H	PH1-OSC_OUT	PF2	PF1	PH4		VSS	VSS	VSS	VSS	VSS		VSS	VDD33 USB	PG8	PC6
J	NRST	PF3	PF4	PH5		VSS	VSS	VSS	VSS	VSS		VDD	VDD	PG7	PG6
K	PF7	PF6	PF5	VDD		VSS	VSS	VSS	VSS	VSS		PH12	PG5	PG4	PG3
L	PF10	PF9	PF8	VSS								PH11	PH10	PD15	PG2
M	VSSA	PC0	PC1	PC2_C	PC3_C	PB2	PG1	VSS	VSS	VCAP	PH6	PH8	PH9	PD14	PD13
N	VREF-	PA1	PA0	PA4	PC4	PF13	PG0	VDD	VDD	VDD	PE13	PH7	PD12	PD11	PD10
P	VREF+	PA2	PA6	PA5	PC5	PF12	PF15	PE8	PE9	PE11	PE14	PB12	PB13	PD9	PD8
R	VDDA	PA3	PA7	PB1	PB0	PF11	PF14	PE7	PE10	PE12	PE15	PB10	PB11	PB14	PB15

1. The above figure shows the package top view.

Figure 18. WLCSP132 (STM32H7A3xI with SMPS) ballout

	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS	VDD	PC10	PD3	VSS	PG10	VDD	PB3	BOOT0	VCAP	VDDLDO	VDD
B	VDDLDO	VSS	PC12	PD4	VDD MMC	PG11	VSS	VDDMMC	PB8	VSS	VDD	PC14-OSC32_IN
C	PA12	VCAP	PA15	PD0	PD5	PG12	PG14	PB6	PE1	PE6	PC15-OSC32_OUT	VSS
D	PA11	PA10	PA13	PC11	PD2	PG9	PG13	PB7	PDR_ON	PE5	VBAT	VSSSMPS
E	PC7	PC9	PA8	PA14	PD1	PD7	PB4	PB9	PE3	PC13	VFBSMPS	VLXSMPS
F	VDD33 USB	VDD50 USB	PC6	PA9	PB10	PD6	PB5	PE0	PE4	NRST	VSS	VDDSMPS
G	VDD	VSS	PD12	PD11	PE15	PE10	PA6	PA1	PC3	PC0	PH0-OSC_IN	VDD
H	PD15	PD13	PD8	PB15	PE14	PE8	PC4	PA2	VSS	VDD	PC1	PH1-OSC_OUT
J	PD14	PD9	PB14	PB11	PE11	PE9	PB1	PC5	PA3	VDDA	VREF+	PC2
K	PD10	PB13	VDDLDO	VSS	PE12	VSS	PF14	PB0	PA7	PA4	PA0	VSSA
L	VDD	PB12	VDD	VCAP	PE13	VDD	PE7	PB2	VSS	VDD	PA5	VSS

1. The above figure shows the package top view.

Table 6. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
	ANA	Analog-only Input
I/O structure	FT	5 V tolerant I/O
	TT	3.3 V tolerant I/O
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with embedded weak pull-up resistor
	Option for TT and FT I/Os	
	_f	I2C FM+ option
	_a	analog option (supplied by V_{DDA})
	_u	USB option (supplied by V_{DD33}USB)
	_h0 (1)	High-speed low voltage (mainly SDMMC2 on V_{DDMMC} power rail)
	_h1(1)	High-speed low voltage (mainly for OCTOSPI)
	_h2(1)	High-speed low voltage (mainly for FMC)
	_h3(1)	High-speed low voltage

Name		Abbreviation	Definition
I/O structure		_s	Secondary supply (supplied by V_{DDMMC}) (2)
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. Refer to SYSCFG_CCCSR register in the device reference manual for how to set a group of I/Os in High-speed low-voltage mode. Depending on the chosen I/Os (for example OCTOSPI), it can belong to several groups of I/Os and several HSLVx bits need to be set (refer to Table Pin/ball definition). Take care that the VDDIO_HSLV and/or VDDMMC_HSLV option bits must also be set.
2. Refer to the table Features and peripheral counts for the list of packages featuring a V_{DDMMC} separate supply pad.

Table 7. STM32H7A3xI/G pin/ball definition

Pin/ball name(1) (2)															Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
LQFP100 with SMPS	TFBGA100 with SMPS	LQFP144 with SMPS	WLCSP132 with SMPS	UFBGA169 with SMPS	UFBGA176+25 with SMPS	LQFP176 with SMPS	TFBGA225 with SMPS	LQFP64	TFBGA100	LQFP100	LQFP144	UFBGA176+25	LQFP176	TFBGA216					
1	A3	1	-	A2	C3	1	E5	-	A3	1	1	A2	1	A3	PE2	I/O	FT_h2	TRACECLK, SAI1_CK1, SPI4_SCK, SAI1_MCLK_A, OCTOSPIM_P1_IO2, USART10_RX, FMC_A23, EVENTOUT	-
-	B3	2	E9	B2	B2	2	B1	-	B3	2	2	A1	2	A2	PE3	I/O	FT_h2	TRACED0, TIM15_BKIN, SAI1_SD_B, USART10_TX, FMC_A19, EVENTOUT	-
2	C3	3	F9	A1	B1	3	C2	-	C3	3	3	B1	3	A1	PE4	I/O	FT_h2	TRACED1, SAI1_D2, DFSDM1_DATIN3, TIM15_CH1N, SPI4_SS, SAI1_FS_A, FMC_A20, DCMI_D4/ PSSI_D4, LCD_B0, EVENTOUT	-
3	A2	4	D10	C3	D3	4	D3	-	D3	4	4	B2	4	B1	PE5	I/O	FT_h2	TRACED2, SAI1_CK2, DFSDM1_CKIN3, TIM15_CH1, SPI4_MISO, SAI1_SCK_A, FMC_A21, DCMI_D6/ PSSI_D6, LCD_G0, EVENTOUT	-
-	A1	5	C10	C2	E3	5	E4	-	E3	5	5	B3	5	B2	PE6	I/O	FT_h2	TRACED3, TIM1_BKIN2, SAI1_D1, TIM15_CH2, SPI4_MOSI, SAI1_SD_A, SAI2_MCK_B, TIM1_BKIN2_COMP12, FMC_A22, DCMI_D7/ PSSI_D7, LCD_G1, EVENTOUT	-
-	-	6	-	B3	A1	6	F6	-	-	-	-	D5	-	G6	VSS	S	-	-	-
4	E5	7	B11	A3	-	7	F7	-	-	-	-	C5	-	F5	VDD	S	-	-	-
5	C2	8	D11	E3	E2	8	E2	1	B2	6	6	C1	6	C1	VBAT	S	-	-	-
-	C1	-	-	D2	A15	-	A15	-	-	-	-	-	-	-	VSS	S	-	-	-

Pin/ball name(1) (2)															Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
LQFP100 with SMPS	TFBGA100 with SMPS	LQFP144 with SMPS	WLCSP132 with SMPS	UFBGA169 with SMPS	UFBGA176+25 with SMPS	LQFP176 with SMPS	TFBGA225 with SMPS	LQFP64	TFBGA100	LQFP100	LQFP144	UFBGA176+25	LQFP176	TFBGA216					
-	-	-	-	-	-	-	C1	-	-	-	-	D2	7	C2	PI8	I/O	FT	EVENTOUT	TAMP_IN2/ TAMP_OUT3, RTC_OUT2, WKUP4
6	E4	9	E10	D3	C1	9	F4	2	A2	7	7	D1	8	D1	PC13	I/O	FT	EVENTOUT	TAMP_IN1/ TAMP_OUT2/ TAMP_OUT3, RTC_OUT1/ RTC_TS, WKUP3
-	-	-	C12	-	C2	-	A1	-	-	-	-	F7	-	-	VSS	S	-	-	-
7	B1	10	B12	C1	D2	10	D1	3	A1	8	8	E1	9	E1	PC14-OSC32_IN (OSC32_IN)	I/O	FT	EVENTOUT	OSC32_IN
8	B2	11	C11	B1	D1	11	D2	4	B1	9	9	F1	10	F1	PC15-OSC32_OUT (OSC32_OUT)	I/O	FT	EVENTOUT	OSC32_OUT
-	-	-	-	-	-	-	E3	-	-	-	-	D3	11	E4	PI9	I/O	FT_h2	OCTOSPIM_P2_IO0, UART4_RX, FDCAN1_RX, FMC_D30, LCD_VSYNC, EVENTOUT	-
-	-	-	-	-	-	-	F3	-	-	-	-	E3	12	D5	PI10	I/O	FT_h2	OCTOSPIM_P2_IO1, FMC_D31, PSSI_D14, LCD_HSYNC, EVENTOUT	-
-	-	-	-	-	-	-	G5	-	-	-	-	E4	13	F3	PI11	I/O	FT	OCTOSPIM_P2_IO2, LCD_G6, OTG_HS_ULPI_DIR, PSSI_D15, EVENTOUT	WKUP5
-	-	12	-	-	D10	12	E1	-	-	-	-	F2	14	F2	VSS	S	-	-	-
-	D6	13	G12	D1	D11	13	G6	-	-	-	-	F3	15	F4	VDD	S	-	-	-
9	D1	14	D12	E2	F2	14	G2	-	-	-	-	-	-	-	VSSSMPS	S	-	-	-
10	D2	15	E12	E1	F1	15	F1	-	-	-	-	-	-	-	VLXSMPS	S	-	-	-
11	E1	16	F12	F1	G1	16	G1	-	-	-	-	-	-	-	VDDSMPS	S	-	-	-
12	E2	17	E11	F2	G2	17	F2	-	-	-	-	-	-	-	VFBSMPS	S	-	-	-
-	-	-	-	F3	F4	18	G4	-	-	-	10	E2	16	D2	PF0	I/O	FT_f	I2C2_SDA, OCTOSPIM_P2_IO0, FMC_A0, EVENTOUT	-
-	-	-	-	E4	F3	19	G3	-	-	-	11	H3	17	E2	PF1	I/O	FT_f	I2C2_SCL, OCTOSPIM_P2_IO1, FMC_A1, EVENTOUT	-
-	-	-	-	F4	G3	20	H1	-	-	-	12	H2	18	G2	PF2	I/O	FT_h2	I2C2_SMBA, OCTOSPIM_P2_IO2, FMC_A2, EVENTOUT	-
-	-	-	-	-	-	-	H2	-	-	-	-	-	-	E3	PI12	I/O	FT_h1	OCTOSPIM_P2_IO3, LCD_HSYNC, EVENTOUT	-
-	-	-	-	-	-	-	H5	-	-	-	-	-	-	G3	PI13	I/O	FT_h1	OCTOSPIM_P2_CLK, LCD_VSYNC, EVENTOUT	-
-	-	-	-	-	-	-	H4	-	-	-	-	-	-	H3	PI14	I/O	FT_h1	OCTOSPIM_P2_NCLK, LCD_CLK, EVENTOUT	-
-	-	-	-	E5	H4	21	J1	-	-	-	13	J2	19	H2	PF3	I/O	FT_h2	OCTOSPIM_P2_IO3, FMC_A3, EVENTOUT	-

Pin/ball name(1) (2)															Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
LQFP100 with SMPS	TFBGA100 with SMPS	LQFP144 with SMPS	WLCSP132 with SMPS	UFBGA169 with SMPS	UFBGA176+25 with SMPS	LQFP176 with SMPS	TFBGA225 with SMPS	LQFP64	TFBGA100	LQFP100	LQFP144	UFBGA176+25	LQFP176	TFBGA216					
-	-	-	-	G3	H2	22	H3	-	-	-	14	J3	20	J2	PF4	I/O	FT_h2	OCTOSPIM_P2_CLK, FMC_A4, EVENTOUT	-
-	-	-	-	F5	H3	23	J2	-	-	-	15	K3	21	K3	PF5	I/O	FT_h2	OCTOSPIM_P2_NCLK, FMC_A5, EVENTOUT	-
-	F5	18	F11	B7	E1	24	H6	-	C2	10	16	G2	22	H6	VSS	S	-	-	-
-	F6	19	-	A7	E4	25	J6	-	D2	11	17	G3	23	H5	VDD	S	-	-	-
-	-	20	-	G4	H1	26	J3	-	-	-	18	K2	24	K2	PF6	I/O	FT_h1	TIM16_CH1, SPI5_SS, SAI1_SD_B, UART7_Rx, OCTOSPIM_P1_IO3, EVENTOUT	-
-	-	21	-	F6	J3	27	J4	-	-	-	19	K1	25	K1	PF7	I/O	FT_h1	TIM17_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_Tx, OCTOSPIM_P1_IO2, EVENTOUT	-
-	-	22	-	H4	J2	28	K1	-	-	-	20	L3	26	L3	PF8	I/O	FT_h1	TIM16_CH1N, SPI5_MISO, SAI1_SCK_B, UART7_RTS, TIM13_CH1, OCTOSPIM_P1_IO0, EVENTOUT	-
-	-	23	-	G5	J4	29	K2	-	-	-	21	L2	27	L2	PF9	I/O	FT_h1	TIM17_CH1N, SPI5_MOSI, SAI1_FS_B, UART7_CTS, TIM14_CH1, OCTOSPIM_P1_IO1, EVENTOUT	-
-	-	24	-	H3	K3	30	M3	-	-	-	22	L1	28	L1	PF10	I/O	FT_h1	TIM16_BKIN, SAI1_D3, PSSI_D15, OCTOSPIM_P1_CLK, DCMI_D11/PSSI_D11, LCD_DE, EVENTOUT	-
13	G1	25	G11	H1	J1	31	L1	5	C1	12	23	G1	29	G1	PH0-OSC_IN(PH0)	I/O	FT	EVENTOUT	OSC_IN
14	G2	26	H12	H2	K1	32	L2	6	D1	13	24	H1	30	H1	PH1-OSC_OUT (PH1)	I/O	FT	EVENTOUT	OSC_OUT
15	F2	27	F10	G6	L1	33	K3	7	E1	14	25	J1	31	J1	NRST	I/O	RST	-	-
16	F3	28	G10	J1	L2	34	L3	8	F1	15	26	M2	32	M2	PC0	I/O	FT_a	DFSDM1_CKIN0, DFSDM1_DATIN4, SAI2_FS_B, FMC_A25, OTG_HS_ULPI_STP, LCD_G2, FMC_SDNWE, LCD_R5, EVENTOUT	ADC12_INP10
17	F1	29	H11	J2	L3	35	M2	9	F2	16	27	M3	33	M3	PC1	I/O	FT_ah0	TRACED0, SAI1_D1, DFSDM1_DATIN0, DFSDM1_CKIN4, SPI2_MOSI/I2S2_SDO, SAI1_SD_A, SDMMC2_CK, OCTOSPIM_P1_IO4, MDIOS_MDC, LCD_G5, EVENTOUT	ADC12_INP11, ADC12_INN10, TAMP_IN3, WKUP6

Pin/ball name(1) (2)															Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
LQFP100 with SMPS	TFBGA100 with SMPS	LQFP144 with SMPS	WLCSP132 with SMPS	UFBGA169 with SMPS	UFBGA176+25 with SMPS	LQFP176 with SMPS	TFBGA225 with SMPS	LQFP64	TFBGA100	LQFP100	LQFP144	UFBGA176+25	LQFP176	TFBGA216					
-	-	-	J12	H5(3)	M1(3)	-	J5(3)	10	-	-	-	-	-	-	PC2	I/O	FT_a	PWR_CSTOP, DFSDM1_CKIN1, SPI2_MISO/I2S2_SDI, DFSDM1_CKOUT, OCTOSPIM_P1_IO2, OTG_HS_ULPI_DIR, OCTOSPIM_P1_IO5, FMC_SDNE0, EVENTOUT	ADC12_INP12, ADC12_INN11
18(4)	F4(4)	30(4)	-	K2(3)	N1(3)	36(4)	N1(3)	-	E2(4)	17(4)	28(4)	M4(4)	34(4)	M4(4)	PC2_C	ANA	TT_a	-	ADC2_INP0, ADC2_INN1
-	-	-	G9	J4(3)	M2(3)	-	N3(3)	11	-	-	-	-	-	-	PC3	I/O	FT_a	PWR_CSLEEP, DFSDM1_DATIN1, SPI2_MOSI/I2S2_SDO, OCTOSPIM_P1_IO0, OTG_HS_ULPI_NXT, OCTOSPIM_P1_IO6, FMC_SDCKE0, EVENTOUT	ADC12_INP13, ADC12_INN12
19(4)	G4(4)	31(4)	-	K1(3)	N2(3)	37(4)	N2(3)	-	F3(4)	18(4)	29(4)	M5(4)	35(4)	L4(4)	PC3_C	ANA	TT_a	-	ADC2_INP1
20	-	32	H10	G1	E12	-	K7	-	-	-	30	K4	36	J5	VDD	S		-	-
21	-	33	H9	G2	F6	-	R1	-	-	-	-	-	-	J6	VSS	S		-	-
22	H2	34	K12	J3	N3	38	K5	12	G1	19	31	M1	37	M1	VSSA	S		-	-
-	-	-	-	-	L4	-	K4	-	-	-	-	N1	-	N1	VREF-	S		-	-
23	J1	35	J11	L2	M3	39	L4	-	-	20	32	P1	38	P1	VREF+	S		-	-
24	H1	36	J10	L1	M4	40	L5	13	H1	21	33	R1	39	R1	VDDA	S		-	-
25	G3	37	K11	J5(3)	P1(3)	41	P1(3)	14	G2	22	34	N3	40	N3	PA0	I/O	FT_a	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, TIM15_BKIN, SPI6_SS/I2S6_WS, USART2_CTS/ USART2_NSS, UART4_TX, SDMMC2_CMD, SAI2_SD_B, EVENTOUT	ADC1_INP16, WKUP1
-	-	-	-	K3(3)	R3(3)	-	P3(3)	-	-	-	-	-	-	-	PA0_C	ANA	TT_a	-	ADC1_INP0, ADC1_INN1
26	J2	38	G8	K4(3)	P2(3)	42	P2(3)	15	H2	23	35	N2	41	N2	PA1	I/O	FT_ah1	TIM2_CH2, TIM5_CH2, LPTIM3_OUT, TIM15_CH1N, USART2_RTS, UART4_RX, OCTOSPIM_P1_IO3, SAI2_MCK_B, OCTOSPIM_P1_DQS, LCD_R2, EVENTOUT	ADC1_INP17, ADC1_INN16
-	-	-	-	L3(3)	P3(3)	-	R3(3)	-	-	-	-	-	-	-	PA1_C	ANA	TT_a	-	ADC1_INP1
27	H3	39	H8	N1	R2	43	R2	16	J2	24	36	P2	42	P2	PA2	I/O	FT_a	TIM2_CH3, TIM5_CH3, TIM15_CH1, DFSDM2_CKIN1, USART2_TX, SAI2_SCK_B, MDIOS_MDIO, LCD_R1, EVENTOUT	ADC1_INP14, WKUP2

Pin/ball name(1) (2)															Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
LQFP100 with SMPS	TFBGA100 with SMPS	LQFP144 with SMPS	WLCSP132 with SMPS	UFBGA169 with SMPS	UFBGA176+25 with SMPS	LQFP176 with SMPS	TFBGA225 with SMPS	LQFP64	TFBGA100	LQFP100	LQFP144	UFBGA176+25	LQFP176	TFBGA216					
-	-	-	-	N2	N4	-	M4	-	-	-	-	F4	43	K4	PH2	I/O	FT_h2	LPTIM1_IN2, OCTOSPIM_P1_IO4, SAI2_SCK_B, FMC_SDCKE0, LCD_R0, EVENTOUT	-
-	-	-	-	M1	G4	44	J7	-	-	-	-	-	-	-	VDD	S	-	-	-
-	-	-	L12	M2	F7	45	M1	-	J1	-	-	F6	-	K6	VSS	S	-	-	-
-	-	-	-	M3	R4	-	N4	-	-	-	-	G4	44	J4	PH3	I/O	FT_ah2	OCTOSPIM_P1_IO5, SAI2_MCK_B, FMC_SDNE0, LCD_R1, EVENTOUT	-
-	-	-	-	-	P4	-	M5	-	-	-	-	H4	45	H4	PH4	I/O	FT_fa	I2C2_SCL, LCD_G5, OTG_HS_ULPI_NXT, PSSI_D14, LCD_G4, EVENTOUT	-
-	-	-	-	-	R5	-	P4	-	-	-	-	J4	46	J3	PH5	I/O	FT_fa	I2C2_SDA, SPI5_SS, FMC_SDNWE, EVENTOUT	-
28	G5	40	J9	N3	N5	46	R4	17	K2	25	37	R2	47	R2	PA3	I/O	FT_ah1	TIM2_CH4, TIM5_CH4, OCTOSPIM_P1_CLK, TIM15_CH2, I2S6_MCK, USART2_RX, LCD_B2, OTG_HS_ULPI_D0, LCD_B5, EVENTOUT	ADC1_INP15
29	-	41	-	M4	F8	47	K6	18	E6	26	38	L4	48	L5	VSS	S	-	-	-
30	-	42	-	N4	H12	48	G7	19	K1	27	39	-	49	K5	VDD	S	-	-	-
31	K1	43	K10	H6	P5	49	L6	20	G3	28	40	N4	50	N4	PA4	I/O	TT_a	TIM5_ETR, SPI1_SS/I2S1_WS, SPI3_SS/I2S3_WS, USART2_CK, SPI6_SS/I2S6_WS, DCMI_HSYNC/ PSSI_DE, LCD_VSYNC, EVENTOUT	ADC1_INP18, DAC1_OUT1
32	K2	44	L11	L4	P6	50	N5	21	H3	29	41	P4	51	P4	PA5	I/O	TT_ah0	PWR_NDSTOP2, TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, SPI6_SCK/I2S6_CK, OTG_HS_ULPI_CK, PSSI_D14, LCD_R4, EVENTOUT	ADC1_INP19, ADC1_INN18, DAC1_OUT2
33	J3	45	G7	K5	R7	51	P5	22	J3	30	42	P3	52	P3	PA6	I/O	TT_ah1	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO/I2S1_SDI, OCTOSPIM_P1_IO3, SPI6_MISO/I2S6_SDI, TIM13_CH1, TIM8_BKIN_COMP12, MDIOS_MDC, TIM1_BKIN_COMP12, DCMI_PIXCLK/ PSSI_PDCK, LCD_G2, EVENTOUT	ADC12_INP3, DAC2_OUT1

Pin/ball name[1] [2]															Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
LQFP100 with SMPS	TFBGA100 with SMPS	LQFP144 with SMPS	WLCSP132 with SMPS	UFBGA169 with SMPS	UFBGA176+25 with SMPS	LQFP176 with SMPS	TFBGA225 with SMPS	LQFP64	TFBGA100	LQFP100	LQFP144	UFBGA176+25	LQFP176	TFBGA216					
34	K3	46	K9	J6	N6	52	R5	23	K3	31	43	R3	53	R3	PA7	I/O	FT_ah1	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, DFSDM2_DATIN1, SPI1_MOSI/I2S1_SDO, SPI6_MOSI/I2S6_SDO, TIM14_CH1, OCTOSPIM_P1_IO2, FMC_SDNWE, LCD_VSYNC, EVENTOUT	ADC12_INP7, ADC12_INN3, OPAMP1_VINM
35	H4	47	H7	K6	R6	53	M6	24	G4	32	44	N5	54	N5	PC4	I/O	FT_a	DFSDM1_CKIN2, I2S1_MCK, SPDIFRX1_IN2, FMC_SDNE0, LCD_R7, EVENTOUT	ADC12_INP4, OPAMP1_VOUT, COMP1_INM
36	J4	48	J8	N5	M7	54	N6	25	H4	33	45	P5	55	P5	PC5	I/O	FT_ah1	SAI1_D3, DFSDM1_DATIN2, PSSI_D15, SPDIFRX1_IN3, OCTOSPIM_P1_DQS, FMC_SDCKE0, COMP1_OUT, LCD_DE, EVENTOUT	ADC12_INP8, ADC12_INN4, OPAMP1_VINM
-	-	-	L10	N7	K4	-	-	-	-	-	-	-	-	L7	VDD	S	-	-	-
-	-	-	L9	M7	F9	-	-	-	-	-	-	M9	-	L6	VSS	S	-	-	-
37	K4	49	K8	M5	R8	55	P6	26	J4	34	46	R5	56	R5	PB0	I/O	FT_ah0	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, DFSDM2_CKOUT, DFSDM1_CKOUT, UART4_CTS, LCD_R3, OTG_HS_ULPI_D1, OCTOSPIM_P1_IO1, LCD_G1, EVENTOUT	ADC12_INP9, ADC12_INN5, OPAMP1_VINP, COMP1_INP
38	K5	50	J7	L5	M8	56	L7	27	K4	35	47	R4	57	R4	PB1	I/O	FT_ah0	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM1_DATIN1, LCD_R6, OTG_HS_ULPI_D2, OCTOSPIM_P1_IO0, LCD_G0, EVENTOUT	ADC12_INP5, COMP1_INM
39	J5	51	L8	L6	P7	57	R6	28	G5	36	48	M6	58	M5	PB2	I/O	FT_ah1	RTC_OUT2, SAI1_D1, DFSDM1_CKIN1, SAI1_SD_A, SPI3_MOSI/I2S3_SDO, OCTOSPIM_P1_CLK, OCTOSPIM_P1_DQS, EVENTOUT	COMP1_INP
-	-	-	-	-	-	-	M7	-	-	-	-	-	-	G4	PI15	I/O	FT	LCD_G2, LCD_R0, EVENTOUT	-
-	-	-	-	-	-	-	N7	-	-	-	-	-	-	R6	PJ0	I/O	FT	LCD_R7, LCD_R1, EVENTOUT	-
-	-	-	-	-	-	-	P7	-	-	-	-	-	-	R7	PJ1	I/O	FT_ah1	OCTOSPIM_P2_IO4, LCD_R2, EVENTOUT	-
-	-	-	-	-	-	-	R7	-	-	-	-	-	-	P7	PJ2	I/O	FT_ah1	OCTOSPIM_P2_IO5, LCD_R3, EVENTOUT	-
-	-	-	-	-	-	-	R8	-	-	-	-	-	-	N8	PJ3	I/O	FT	UART9_RTS, LCD_R4, EVENTOUT	-

Pin/ball name(1) (2)															Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
LQFP100 with SMPS	TFBGA100 with SMPS	LQFP144 with SMPS	WLCSP132 with SMPS	UFBGA169 with SMPS	UFBGA176+25 with SMPS	LQFP176 with SMPS	TFBGA225 with SMPS	LQFP64	TFBGA100	LQFP100	LQFP144	UFBGA176+25	LQFP176	TFBGA216					
-	-	-	-	-	-	-	P8	-	-	-	-	-	-	M9	PJ4	I/O	FT	UART9_CTS, LCD_R5, EVENTOUT	-
-	-	52	-	M6	N7	58	N8	-	-	-	49	R6	59	P8	PF11	I/O	FT_ah1	SPI5_MOSI, OCTOSPIM_P1_NCLK, SAI2_SD_B, FMC_SDNRAS, DCMI_D12/PSSI_D12, EVENTOUT	ADC1_INP2
-	-	-	-	N6	P11	59	R9	-	-	-	50	P6	60	M6	PF12	I/O	FT_ah2	OCTOSPIM_P2_DQS, FMC_A6, EVENTOUT	ADC1_INP6, ADC1_INN2
-	-	-	-	-	F10	-	K8	-	-	-	51	M8	61	K7	VSS	S	-	-	-
-	-	-	-	-	L12	-	K9	-	-	-	52	N8	62	L8	VDD	S	-	-	-
-	-	-	-	G7	N11	60	M8	-	-	-	53	N6	63	N6	PF13	I/O	FT_ah2	DFSDM1_DATIN6, I2C4_SMBA, FMC_A7, EVENTOUT	ADC2_INP2
-	-	53	K7	H7	R10	61	P9	-	-	-	54	R7	64	P6	PF14	I/O	FT_fah2	DFSDM1_CKIN6, I2C4_SCL, FMC_A8, EVENTOUT	ADC2_INP6, ADC2_INN2
-	-	54	-	J7	N10	62	N9	-	-	-	55	P7	65	M8	PF15	I/O	FT_fh2	I2C4_SDA, FMC_A9, EVENTOUT	-
-	-	-	-	K7	P8	63	R10	-	-	-	56	N7	66	N7	PG0	I/O	FT_h2	OCTOSPIM_P2_IO4, UART9_RX, FMC_A10, EVENTOUT	-
-	-	55	-	-	F12	64	-	-	-	-	-	K8	-	-	VSS	S	-	-	-
-	-	56	-	-	M5	65	-	-	-	-	-	N10	-	-	VDD	S	-	-	-
-	-	-	-	L7	N9	66	P10	-	-	-	57	M7	67	M7	PG1	I/O	FT_h2	OCTOSPIM_P2_IO5, UART9_TX, FMC_A11, EVENTOUT	OPAMP2_VINM
40	H5	57	L7	G8	P9	67	M9	-	H5	37	58	R8	68	R8	PE7	I/O	FT_ah2	TIM1_ETR, DFSDM1_DATIN2, UART7_Rx, OCTOSPIM_P1_IO4, FMC_D4/FMC_DA4, EVENTOUT	OPAMP2_VOUT, COMP2_INM
41	J6	58	H6	H8	N8	68	R11	-	J5	38	59	P8	69	N9	PE8	I/O	FT_ah2	TIM1_CH1N, DFSDM1_CKIN2, UART7_Tx, OCTOSPIM_P1_IO5, FMC_D5/FMC_DA5, COMP2_OUT, EVENTOUT	OPAMP2_VINM
-	K6	59	J6	J8	R11	69	P11	-	K5	39	60	P9	70	P9	PE9	I/O	FT_ah2	TIM1_CH1, DFSDM1_CKOUT, UART7_RTS, OCTOSPIM_P1_IO6, FMC_D6/FMC_DA6, EVENTOUT	OPAMP2_VINP, COMP2_INP
-	-	-	K6	M11	G6	70	K10	-	-	-	61	K9	71	K8	VSS	S	-	-	-
-	-	-	L6	N11	M9	71	J10	-	-	-	62	N9	72	L9	VDD	S	-	-	-
-	H6	60	G6	M8	R9	72	N11	-	G6	40	63	R9	73	R9	PE10	I/O	FT_ah2	TIM1_CH2N, DFSDM1_DATIN4, UART7_CTS, OCTOSPIM_P1_IO7, FMC_D7/FMC_DA7, EVENTOUT	COMP2_INM

Pin/ball name[1] [2]															Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
LQFP100 with SMPS	TFBGA100 with SMPS	LQFP144 with SMPS	WLCSP132 with SMPS	UFBGA169 with SMPS	UFBGA176+25 with SMPS	LQFP176 with SMPS	TFBGA225 with SMPS	LQFP64	TFBGA100	LQFP100	LQFP144	UFBGA176+25	LQFP176	TFBGA216					
-	-	61	J5	N8	R12	73	R12	-	H6	41	64	P10	74	P10	PE11	I/O	FT_ah2	TIM1_CH2, DFSDM1_CKIN4, SPI4_SS, SAI2_SD_B, OCTOSPIM_P1_NCS, FMC_D8/FMC_DA8, LCD_G3, EVENTOUT	COMP2_INP
-	-	62	K5	L8	P12	74	L9	-	J6	42	65	R10	75	R10	PE12	I/O	FT_h2	TIM1_CH3N, DFSDM1_DATIN5, SPI4_SCK, SAI2_SCK_B, FMC_D9/FMC_DA9, COMP1_OUT, LCD_B4, EVENTOUT	-
-	-	63	L5	K8	P13	75	M10	-	K6	43	66	N11	76	R12	PE13	I/O	FT_h2	TIM1_CH3, DFSDM1_CKIN5, SPI4_MISO, SAI2_FS_B, FMC_D10/FMC_DA10, COMP2_OUT, LCD_DE, EVENTOUT	-
-	-	64	H5	J9	M12	76	N10	-	G7	44	67	P11	77	P11	PE14	I/O	FT_h2	TIM1_CH4, SPI4_MOSI, SAI2_MCK_B, FMC_D11/FMC_DA11, LCD_CLK, EVENTOUT	-
-	-	65	G5	N9	P14	77	P12	-	H7	45	68	R11	78	R11	PE15	I/O	FT_h2	TIM1_BKIN, USART10_CK, FMC_D12/FMC_DA12, TIM1_BKIN_COMP12, LCD_R7, EVENTOUT	-
42	K7	66	F5	L9	N12	78	R13	29	J7	46	69	R12	79	P12	PB10	I/O	FT_f	TIM2_CH3, LPTIM2_IN1, I2C2_SCL, SPI2_SCK/I2S2_CK, DFSDM1_DATIN7, USART3_TX, OCTOSPIM_P1_NCS, OTG_HS_ULPI_D3, LCD_G4, EVENTOUT	-
43	J7	67	J4	M9	P10	79	P13	-	K7	47	70	R13	80	R13	PB11	I/O	FT_f	TIM2_CH4, LPTIM2_ETR, I2C2_SDA, DFSDM1_CKIN7, USART3_RX, OTG_HS_ULPI_D4, LCD_G5, EVENTOUT	-
44	G6	68	L4	N10	R13	80	L8	30	F8	48	71	M10	81	L11	VCAP	S	-	-	-
45	D5	69	K4	-	M10	81	-	31	-	49	-	-	-	K9	VSS	S	-	-	-
46	E6	70	K3	M10	R14	82	L10	-	-	-	-	-	-	-	VDDLDO	S	-	-	-
47	-	71	L1	-	-	-	-	32	-	50	72	J12	82	L10	VDD	S	-	-	-
-	-	-	-	-	-	-	N12	-	-	-	-	-	-	M14	PJ5	I/O	FT	LCD_R6, EVENTOUT	-
-	-	-	-	-	P15	-	M11	-	-	-	-	M11	83	P13	PH6	I/O	FT	TIM12_CH1, I2C2_SMBA, SPI5_SCK, FMC_SDNE1, DCMI_D8/PSSI_D8, EVENTOUT	-

Pin/ball name(1) (2)															Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
LQFP100 with SMPS	TFBGA100 with SMPS	LQFP144 with SMPS	WLCSP132 with SMPS	UFBGA169 with SMPS	UFBGA176+25 with SMPS	LQFP176 with SMPS	TFBGA225 with SMPS	LQFP64	TFBGA100	LQFP100	LQFP144	UFBGA176+25	LQFP176	TFBGA216					
-	-	-	-	-	M11	-	R14	-	-	-	-	N12	84	N13	PH7	I/O	FT_f	I2C3_SCL, SPI5_MISO, FMC_SDCKE1, DCMI_D9/PSSI_D9, EVENTOUT	-
-	-	-	-	-	N13	-	P14	-	-	-	-	M12	85	P14	PH8	I/O	FT_fh2	TIM5_ETR, I2C3_SDA, FMC_D16, DCMI_HSYNC/ PSSI_DE, LCD_R2, EVENTOUT	-
-	-	-	-	-	M14	-	N13	-	-	-	-	M13	86	N14	PH9	I/O	FT_h2	TIM12_CH2, I2C3_SMBA, FMC_D17, DCMI_D0/ PSSI_D0, LCD_R3, EVENTOUT	-
-	-	-	-	K9	N14	-	M12	-	-	-	-	L13	87	P15	PH10	I/O	FT_h2	TIM5_CH1, I2C4_SMBA, FMC_D18, DCMI_D1/ PSSI_D1, LCD_R4, EVENTOUT	-
-	-	-	-	L10	M13	-	P15	-	-	-	-	L12	88	N15	PH11	I/O	FT_fh2	TIM5_CH2, I2C4_SCL, FMC_D19, DCMI_D2/ PSSI_D2, LCD_R5, EVENTOUT	-
-	-	-	-	K10	N15	-	L11	-	-	-	-	K12	89	M15	PH12	I/O	FT_fh2	TIM5_CH3, I2C4_SDA, FMC_D20, DCMI_D3/ PSSI_D3, LCD_R6, EVENTOUT	-
-	E7	-	-	L12	G10	83	R15	-	-	-	-	H12	90	K10	VSS	S	-	-	-
-	-	-	L3	L13	-	84	-	-	-	-	-	G13	91	K11	VDD	S	-	-	-
48	K8	72	L2	N12	M15	85	N14	33	K8	51	73	P12	92	L13	PB12	I/O	FT_h1	TIM1_BKIN, OCTOSPIM_P1_NCLK, I2C2_SMBA, SPI2_SS/I2S2_WS, DFSDM1_DATIN1, USART3_CK, FDCAN2_RX, OTG_HS_ULPI_D5, DFSDM2_DATIN1, TIM1_BKIN_COMP12, UART5_RX, EVENTOUT	-
49	J8	73	K2	L11	L15	86	M13	34	J8	52	74	P13	93	K14	PB13	I/O	FT_h0	TIM1_CH1N, LPTIM2_OUT, DFSDM2_CKIN1, SPI2_SCK/I2S2_CK, DFSDM1_CKIN1, USART3_CTS/ USART3_NSS, FDCAN2_TX, OTG_HS_ULPI_D6, SDMMC1_D0, DCMI_D2/PSSI_D2, UART5_TX, EVENTOUT	-

Pin/ball name(1) (2)															Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
LQFP100 with SMPS	TFBGA100 with SMPS	LQFP144 with SMPS	WLCSP132 with SMPS	UFBGA169 with SMPS	UFBGA176+25 with SMPS	LQFP176 with SMPS	TFBGA225 with SMPS	LQFP64	TFBGA100	LQFP100	LQFP144	UFBGA176+25	LQFP176	TFBGA216					
50	K9	74	J3	N13	K15	87	M14	35	H10	53	75	R14	94	R14	PB14	I/O	FT_h0	TIM1_CH2N, TIM12_CH1, TIM8_CH2N, USART1_TX, SPI2_MISO/I2S2_SDI, DFSDM1_DATIN2, USART3_RTS, UART4_RTS, SDMMC2_D0, LCD_CLK, EVENTOUT	-
51	K10	75	H4	M13	K14	88	M15	36	G10	54	76	R15	95	R15	PB15	I/O	FT_h0	RTC_REFIN, TIM1_CH3N, TIM12_CH2, TIM8_CH3N, USART1_RX, SPI2_MOSI/I2S2_SDO, DFSDM1_CKIN2, UART4_CTS, SDMMC2_D1, LCD_G7, EVENTOUT	-
52	J9	76	H3	M12	L14	89	L12	-	K9	55	77	P15	96	L15	PD8	I/O	FT_h2	DFSDM1_CKIN3, USART3_TX, SPDIFRX1_IN1, FMC_D13/FMC_DA13, EVENTOUT	-
53	H8	77	J2	K11	K13	90	N15	-	J9	56	78	P14	97	L14	PD9	I/O	FT_h2	DFSDM1_DATIN3, USART3_RX, FMC_D14/FMC_DA14, EVENTOUT	-
54	J10	78	K1	K12	L13	91	L13	-	H9	57	79	N15	98	K15	PD10	I/O	FT_h2	DFSDM1_CKOUT, DFSDM2_CKOUT, USART3_CK, FMC_D15/FMC_DA15, LCD_B3, EVENTOUT	-
-	-	79	-	-	-	92	-	-	F4	-	-	-	-	-	VDD	S	-	-	-
-	-	80	-	-	H6	93	-	-	-	-	-	J10	-	-	VSS	S	-	-	-
55	H7	81	G4	J10	J13	94	L14	-	G9	58	80	N14	99	N10	PD11	I/O	FT_h2	LPTIM2_IN2, I2C4_SMBA, USART3_CTS/ USART3_NSS, OCTOSPIM_P1_IO0, SAI2_SD_A, FMC_A16/ FMC_CLE, EVENTOUT	-
56	H9	82	G3	K13	J15	95	L15	-	K10	59	81	N13	100	M10	PD12	I/O	FT_fh2	LPTIM1_IN1, TIM4_CH1, LPTIM2_IN1, I2C4_SCL, USART3_RTS, OCTOSPIM_P1_IO1, SAI2_FS_A, FMC_A17/ FMC_ALE, DCMI_D12/ PSSI_D12, EVENTOUT	-
57	H10	83	H2	J11	H15	96	K11	-	J10	60	82	M15	101	M11	PD13	I/O	FT_fh2	LPTIM1_OUT, TIM4_CH2, I2C4_SDA, OCTOSPIM_P1_IO3, SAI2_SCK_A, UART9_RTS, FMC_A18, DCMI_D13/ PSSI_D13, EVENTOUT	-
58	-	-	-	H12	R1	-	H7	-	-	-	83	J9	102	J10	VSS	S	-	-	-
59	-	-	-	H13	-	-	-	-	-	-	84	J13	103	J11	VDD	S	-	-	-

Pin/ball name(1) (2)															Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
LQFP100 with SMPS	TFBGA100 with SMPS	LQFP144 with SMPS	WLCSP132 with SMPS	UFBGA169 with SMPS	UFBGA176+25 with SMPS	LQFP176 with SMPS	TFBGA225 with SMPS	LQFP64	TFBGA100	LQFP100	LQFP144	UFBGA176+25	LQFP176	TFBGA216					
60	G7	84	J1	J13	H14	97	K12	-	H8	61	85	M14	104	L12	PD14	I/O	FT_h2	TIM4_CH3, UART8_CTS, UART9_RX, FMC_D0/ FMC_DA0, EVENTOUT	-
61	G8	85	H1	J12	J12	98	K13	-	G8	62	86	L14	105	K13	PD15	I/O	FT_h2	TIM4_CH4, UART8_RTS, UART9_TX, FMC_D1/ FMC_DA1, EVENTOUT	-
-	-	-	-	-	-	-	K14	-	-	-	-	-	-	K12	PJ6	I/O	FT	TIM8_CH2, LCD_R7, EVENTOUT	-
-	-	-	-	-	-	-	K15	-	-	-	-	-	-	J12	PJ7	I/O	FT	TRGIN, TIM8_CH2N, LCD_G0, EVENTOUT	-
-	-	-	G1	-	-	99	-	-	-	-	-	-	-	-	VDD	S	-	-	-
-	-	-	G2	-	D6	100	H10	-	-	-	-	-	-	-	VSS	S	-	-	-
-	-	-	-	-	-	101	J15	-	-	-	-	-	-	H12	PJ8	I/O	FT	TIM1_CH3N, TIM8_CH1, UART8_TX, LCD_G1, EVENTOUT	-
-	-	-	-	-	-	102	J14	-	-	-	-	-	-	J13	PJ9	I/O	FT	TIM1_CH3, TIM8_CH1N, UART8_RX, LCD_G2, EVENTOUT	-
-	-	-	-	-	-	103	J13	-	-	-	-	-	-	H13	PJ10	I/O	FT	TIM1_CH2N, TIM8_CH2, SPI5_MOSI, LCD_G3, EVENTOUT	-
-	-	-	-	-	-	104	J11	-	-	-	-	-	-	G12	PJ11	I/O	FT	TIM1_CH2, TIM8_CH2N, SPI5_MISO, LCD_G4, EVENTOUT	-
-	-	-	-	-	-	105	G9	-	-	-	-	-	-	H11	VDD	S	-	-	-
-	-	-	-	-	G7	106	H8	-	-	-	-	K10	-	H10	VSS	S	-	-	-
-	-	-	-	-	-	107	J12	-	-	-	-	-	-	G13	PK0	I/O	FT	TIM1_CH1N, TIM8_CH3, SPI5_SCK, LCD_G5, EVENTOUT	-
-	-	-	-	-	-	108	H15	-	-	-	-	-	-	F12	PK1	I/O	FT	TIM1_CH1, TIM8_CH3N, SPI5_SS, LCD_G6, EVENTOUT	-
-	-	-	-	-	-	109	H14	-	-	-	-	-	-	F13	PK2	I/O	FT	TIM1_BKIN, TIM8_BKIN, TIM8_BKIN_COMP12, TIM1_BKIN_COMP12, LCD_G7, EVENTOUT	-
-	-	-	-	H9	G15	110	H13	-	-	-	87	L15	106	M13	PG2	I/O	FT_h2	TIM8_BKIN, TIM8_BKIN_COMP12, FMC_A12, EVENTOUT	-
-	-	-	-	H10	H13	111	G15	-	-	-	88	K15	107	M12	PG3	I/O	FT_h2	TIM8_BKIN2, TIM8_BKIN2_COMP12, FMC_A13, EVENTOUT	-
-	-	-	-	C12	H10	112	J8	-	-	-	-	G10	-	-	VSS	S	-	-	-
-	-	-	-	C13	-	113	J9	-	-	-	-	-	-	-	VDD	S	-	-	-
-	-	-	-	F8	G14	114	H12	-	-	-	89	K14	108	N12	PG4	I/O	FT_h2	TIM1_BKIN2, TIM1_BKIN2_COMP12, FMC_A14/FMC_BA0, EVENTOUT	-

Pin/ball name(1) (2)															Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
LQFP100 with SMPS	TFBGA100 with SMPS	LQFP144 with SMPS	WLCSP132 with SMPS	UFBGA169 with SMPS	UFBGA176+25 with SMPS	LQFP176 with SMPS	TFBGA225 with SMPS	LQFP64	TFBGA100	LQFP100	LQFP144	UFBGA176+25	LQFP176	TFBGA216					
-	-	-	-	H11	F15	115	G14	-	-	-	90	K13	109	N11	PG5	I/O	FT_h2	TIM1_ETR, FMC_A15/ FMC_BA1, EVENTOUT	-
-	-	86	-	G9	F14	116	G13	-	-	-	91	J15	110	J15	PG6	I/O	FT_h2	TIM17_BKIN, OCTOSPIM_P1_NCS, FMC_NE3, DCMI_D12/ PSSI_D12, LCD_R7, EVENTOUT	-
-	-	87	-	G10	G13	117	G12	-	-	-	92	J14	111	J14	PG7	I/O	FT_h2	SAI1_MCLK_A, USART6_CK, OCTOSPIM_P2_DQS, FMC_INT, DCMI_D13/ PSSI_D13, LCD_CLK, EVENTOUT	-
-	-	88	-	G11	G12	118	F15	-	-	-	93	H14	112	H14	PG8	I/O	FT_h2	TIM8_ETR, SPI6_SS/I2S6_WS, USART6_RTS, SPDIFRX1_IN2, FMC_SDCLK, LCD_G7, EVENTOUT	-
-	-	89	-	-	J6	119	H9	-	-	-	94	H8	113	G10	VSS	S	-	-	-
-	F7	90	F2	G12	E15	120	D15	-	-	-	-	-	-	-	VDD50USB	S	-	-	-
-	E8	91	F1	G13	F13	121	H11	-	F6	-	95	H13	114	G11	VDD33USB	S	-	-	-
-	-	92	-	-	-	-	G10	-	-	-	-	-	-	-	VDD	S	-	-	-
62	F8	93	F3	F9	E14	122	F14	37	F10	63	96	H15	115	H15	PC6	I/O	FT_h0	TIM3_CH1, TIM8_CH1, DFSDM1_CKIN3, I2S2_MCK, USART6_TX, SDMMC1_D0DIR, FMC_NWAIT, SDMMC2_D6, SDMMC1_D6, DCMI_D0/PSSI_D0, LCD_HSYNC, EVENTOUT	SWPMI_IO
63	G9	94	E1	F10	D15	123	E15	38	E10	64	97	G15	116	G15	PC7	I/O	FT_h0	TRGIO, TIM3_CH2, TIM8_CH2, DFSDM1_DATIN3, I2S3_MCK, USART6_RX, SDMMC1_D123DIR, FMC_NE1, SDMMC2_D7, SWPMI_TX, SDMMC1_D7, DCMI_D1/PSSI_D1, LCD_G6, EVENTOUT	-
64	G10	95	-	F12	D14	124	F13	-	F9	65	98	G14	117	G14	PC8	I/O	FT_h0	TRACED1, TIM3_CH3, TIM8_CH3, USART6_CK, UART5_RTS, FMC_NE2/FMC_NCE, FMC_INT, SWPMI_RX, SDMMC1_D0, DCMI_D2/PSSI_D2, EVENTOUT	-

Pin/ball name(1) (2)															Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
LQFP100 with SMPS	TFBGA100 with SMPS	LQFP144 with SMPS	WLCSP132 with SMPS	UFBGA169 with SMPS	UFBGA176+25 with SMPS	LQFP176 with SMPS	TFBGA225 with SMPS	LQFP64	TFBGA100	LQFP100	LQFP144	UFBGA176+25	LQFP176	TFBGA216					
65	F9	96	E2	F11	E13	125	E14	39	E9	66	99	F14	118	F14	PC9	I/O	FT_fh0	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, OCTOSPIM_P1_IO0, LCD_G3, SWPMI_SUSPEND, SDMMC1_D1, DCMI_D3/PSSI_D3, LCD_B2, EVENTOUT	-
-	-	-	-	-	J7	-	D14	-	-	-	-	F10	-	-	VSS	S	-	-	-
-	-	-	-	-	-	126	-	-	-	-	-	-	-	-	VDD	S	-	-	-
66	F10	97	E3	E12	B14	127	G11	40	D9	67	100	F15	119	F15	PA8	I/O	FT_fh0	MCO1, TIM1_CH1, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_HS_SOF, UART7_RX, TIM8_BKIN2_COMP12, LCD_B3, LCD_R6, EVENTOUT	-
67	E9	98	F4	E11	D13	128	F12	41	C9	68	101	E15	120	E15	PA9	I/O	FT_u	TIM1_CH2, LPUART1_TX, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, DCMI_D0/PSSI_D0, LCD_R5, EVENTOUT	OTG_HS_VBUS
68	E10	99	D2	E10	C14	129	E13	42	D10	69	102	D15	121	D15	PA10	I/O	FT_u	TIM1_CH3, LPUART1_RX, USART1_RX, OTG_HS_ID, MDIOS_MDIO, LCD_B4, DCMI_D1/ PSSI_D1, LCD_B1, EVENTOUT	-
69	D10	100	D1	F13	C15	130	C15	43	C10	70	103	C15	122	C15	PA11	I/O	FT_u	TIM1_CH4, LPUART1_CTS, SPI2_SS/I2S2_WS, UART4_RX, USART1_CTS/ USART1_NSS, FDCAN1_RX, LCD_R4, EVENTOUT	OTG_HS_DM
70	D9	101	C1	E13	B15	131	C14	44	B10	71	104	B15	123	B15	PA12	I/O	FT_u	TIM1_ETR, LPUART1_RTS, SPI2_SCK/I2S2_CK, UART4_TX, USART1_RTS, SAI2_FS_B, FDCAN1_TX, LCD_R5, EVENTOUT	OTG_HS_DP
71	C10	102	D3	D11	B13	132	E12	45	A10	72	105	A15	124	A15	PA13(JTMS/ SWDIO)	I/O	FT	JTMS/SWDIO, EVENTOUT	-
72	D8	103	C2	D13	A14	133	F11	46	E7	73	106	F13	125	E11	VCAP	S	-	-	-
73	-	104	A1	B10	M6	134	F10	47	E5	74	107	F12	126	F10	VSS	S	-	-	-
74	-	105	B1	D12	A13	135	E10	-	-	-	-	-	-	-	VDDLDO	S	-	-	-
75	-	106	-	A10	-	136	F9	48	F5	75	108	-	127	F11	VDD	S	-	-	-
76	-	-	-	-	-	-	-	-	-	-	-	-	-	-	VDD33USB	S	-	-	-

Pin/ball name(1) (2)															Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
LQFP100 with SMPS	TFBGA100 with SMPS	LQFP144 with SMPS	WLCSP132 with SMPS	UFBGA169 with SMPS	UFBGA176+25 with SMPS	LQFP176 with SMPS	TFBGA225 with SMPS	LQFP64	TFBGA100	LQFP100	LQFP144	UFBGA176+25	LQFP176	TFBGA216					
-	-	-	-	B13	C13	-	D13	-	-	-	-	E12	128	E12	PH13	I/O	FT_h2	TIM8_CH1N, UART4_TX, FDCAN1_TX, FMC_D21, LCD_G2, EVENTOUT	-
-	-	-	-	A13	B12	-	B15	-	-	-	-	E13	129	E13	PH14	I/O	FT_h2	TIM8_CH2N, UART4_RX, FDCAN1_RX, FMC_D22, DCMI_D4/ PSSI_D4, LCD_G3, EVENTOUT	-
-	-	-	-	-	D12	-	B14	-	-	-	-	D13	130	D13	PH15	I/O	FT_h2	TIM8_CH3N, FMC_D23, DCMI_D11/ PSSI_D11, LCD_G4, EVENTOUT	-
-	-	-	-	-	-	-	C13	-	-	-	-	E14	131	E14	PI0	I/O	FT_h2	TIM5_CH4, SPI2_SS/ I2S2_WS, FMC_D24, DCMI_D13/PSSI_D13, LCD_G5, EVENTOUT	-
-	-	-	B2	-	J9	-	A15	-	-	-	-	G8	-	-	VSS	S	-	-	-
-	-	-	-	-	-	-	E11	-	-	-	-	D14	132	D14	PI1	I/O	FT_h2	TIM8_BKIN2, SPI2_SCK/I2S2_CK, TIM8_BKIN2_COMP12, FMC_D25, DCMI_D8/ PSSI_D8, LCD_G6, EVENTOUT	-
-	-	-	-	-	-	-	D12	-	-	-	-	C14	133	C14	PI2	I/O	FT_h2	TIM8_CH4, SPI2_MISO/I2S2_SDI, FMC_D26, DCMI_D9/ PSSI_D9, LCD_G7, EVENTOUT	-
-	-	-	-	-	-	-	A14	-	-	-	-	C13	134	C13	PI3	I/O	FT_h2	TIM8_ETR, SPI2_MOSI/I2S2_SDO, FMC_D27, DCMI_D10/ PSSI_D10, EVENTOUT	-
-	-	-	-	-	J10	137	F8	-	-	-	-	D9	135	F9	VSS	S	-	-	-
-	-	-	A2	-	-	-	-	-	-	-	-	C9	136	E10	VDD	S	-	-	-
77	C9	107	E4	B12	A12	138	B13	49	A9	76	109	A14	137	A14	PA14(JTCK/ SWCLK)	I/O	FT	JTCK/SWCLK, EVENTOUT	-
78	C8	108	C3	C11	A11	139	C12	50	A8	77	110	A13	138	A13	PA15(JTDI)	I/O	FT	JTDI, TIM2_CH1/ TIM2_ETR, HDMI_CEC, SPI1_SS/I2S1_WS, SPI3_SS/I2S3_WS, SPI6_SS/I2S6_WS, UART4_RTS, LCD_R3, UART7_TX, LCD_B6, EVENTOUT	-
79	B10	109	A3	A12	C12	140	A13	51	B9	78	111	B14	139	B14	PC10	I/O	FT_h0	DFSDM1_CKIN5, DFSDM2_CKIN0, SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, OCTOSPIM_P1_IO1, LCD_B1, SWPMI_RX, SDMMC1_D2, DCMI_D8/PSSI_D8, LCD_R2, EVENTOUT	-

Pin/ball name[1] [2]															Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
LQFP100 with SMPS	TFBGA100 with SMPS	LQFP144 with SMPS	WLCSP132 with SMPS	UFBGA169 with SMPS	UFBGA176+25 with SMPS	LQFP176 with SMPS	TFBGA225 with SMPS	LQFP64	TFBGA100	LQFP100	LQFP144	UFBGA176+25	LQFP176	TFBGA216					
80	B9	110	D4	B11	C11	141	D11	52	B8	79	112	B13	140	B13	PC11	I/O	FT_h0	DFSDM1_DATIN5, DFSDM2_DATIN0, SPI3_MISO/I2S3_SDI, USART3_RX, UART4_RX, OCTOSPIM_P1_NCS, SDMMC1_D3, DCMI_D4/PSSI_D4, LCD_B4, EVENTOUT	-
81	A10	111	B3	A11	B11	142	B12	53	C8	80	113	A12	141	A12	PC12	I/O	FT_h0	TRACED3, TIM15_CH1, DFSDM2_CKOUT, SPI6_SCK/I2S6_CK, SPI3_MOSI/I2S3_SDO, USART3_CK, UART5_TX, SDMMC1_CK, DCMI_D9/PSSI_D9, LCD_R6, EVENTOUT	-
-	-	-	-	-	J14	-	-	-	-	-	-	G7	-	-	VSS	S	-	-	-
82	C7	112	C4	D10	C10	143	C11	-	D8	81	114	B12	142	B12	PD0	I/O	FT_h2	DFSDM1_CKIN6, UART4_RX, FDCAN1_RX, UART9_CTS, FMC_D2/ FMC_DA2, LCD_B1, EVENTOUT	-
83	B8	113	E5	C10	A10	144	A12	-	E8	82	115	C12	143	C12	PD1	I/O	FT_h2	DFSDM1_DATIN6, UART4_TX, FDCAN1_TX, FMC_D3/ FMC_DA3, EVENTOUT	-
84	A9	114	D5	E9	B10	145	B11	54	B7	83	116	D12	144	D12	PD2	I/O	FT_h0	TRACED2, TIM3_ETR, TIM15_BKIN, UART5_RX, LCD_B7, SDMMC1_CMD, DCMI_D11/PSSI_D11, LCD_B2, EVENTOUT	-
85	A8	115	A4	D9	A9	146	D10	-	C7	84	117	D11	145	C11	PD3	I/O	FT_h2	DFSDM1_CKOUT, SPI2_SCK/I2S2_CK, USART2_CTS/ USART2_NSS, FMC_CLK, DCMI_D5/ PSSI_D5, LCD_G7, EVENTOUT	-
86	B7	116	B4	C9	C9	147	A11	-	D7	85	118	D10	146	D11	PD4	I/O	FT_h1	USART2_RTS, OCTOSPIM_P1_IO4, FMC_NOE, EVENTOUT	-
87	D7	117	C5	A9	B9	148	C10	-	B6	86	119	C11	147	C10	PD5	I/O	FT_h1	USART2_TX, OCTOSPIM_P1_IO5, FMC_NWE, EVENTOUT	-
-	-	118	-	-	K2	-	-	-	-	-	120	G9	148	F8	VSS	S	-	-	-
-	-	119	-	-	-	-	-	-	-	-	121	-	149	-	VDDMMC	S	-	-	-
88	-	-	-	-	-	-	-	-	-	-	-	-	-	-	VDD	S	-	-	-

Pin/ball name(1) (2)															Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
LQFP100 with SMPS	TFBGA100 with SMPS	LQFP144 with SMPS	WLCSP132 with SMPS	UFBGA169 with SMPS	UFBGA176+25 with SMPS	LQFP176 with SMPS	TFBGA225 with SMPS	LQFP64	TFBGA100	LQFP100	LQFP144	UFBGA176+25	LQFP176	TFBGA216					
-	A7	120	F6	B9	D9	149	B10	-	C6	87	122	B11	150	B11	PD6	I/O	FT_sh3	SAI1_D1, DFSDM1_CKIN4, DFSDM1_DATIN1, SPI3_MOSI/I2S3_SDO, SAI1_SD_A, USART2_RX, OCTOSPIM_P1_IO6, SDMMC2_CK, FMC_NWAIT, DCMI_D10/PSSI_D10, LCD_B2, EVENTOUT	-
-	C6	121	E6	D8	B8	150	A10	-	D6	88	123	A11	151	A11	PD7	I/O	FT_sh3	DFSDM1_DATIN4, SPI1_MOSI/I2S1_SDO, DFSDM1_CKIN1, USART2_CK, SPDIFRX1_IN0, OCTOSPIM_P1_IO7, SDMMC2_CMD, FMC_NE1, EVENTOUT	-
-	-	-	-	-	-	-	E9	-	-	-	-	-	-	B10	PJ12	I/O	FT	TRGOUT, LCD_G3, LCD_B0, EVENTOUT	-
-	-	-	-	-	-	-	D9	-	-	-	-	-	-	B9	PJ13	I/O	FT	LCD_B4, LCD_B1, EVENTOUT	-
-	-	-	-	-	-	-	C9	-	-	-	-	-	-	C9	PJ14	I/O	FT	LCD_B2, EVENTOUT	-
-	-	-	-	-	-	-	B9	-	-	-	-	-	-	D10	PJ15	I/O	FT	LCD_B3, EVENTOUT	-
-	-	-	A5	-	K6	151	-	-	-	-	-	H7	-	-	VSS	S	-	-	-
-	-	-	B5	A6	D5	152	E8	-	-	-	-	C8	-	E9	VDDMMC	S	-	-	-
-	-	122	D6	C8	A8	153	A9	-	-	-	124	C10	152	D9	PG9	I/O	FT_sh3	SPI1_MISO/I2S1_SDI, USART6_RX, SPDIFRX1_IN3, OCTOSPIM_P1_IO6, SAI2_FS_B, SDMMC2_D0, FMC_NE2/FMC_NCE, DCMI_VSYNC/ PSSI_RDY, EVENTOUT	-
-	-	123	A6	A8	C8	154	A8	-	-	-	125	B10	153	C8	PG10	I/O	FT_sh3	OCTOSPIM_P2_IO6, SPI1_SS/I2S1_WS, LCD_G3, SAI2_SD_B, SDMMC2_D1, FMC_NE3, DCMI_D2/ PSSI_D2, LCD_B2, EVENTOUT	-
-	-	124	B6	B8	A7	155	B8	-	-	-	126	B9	154	B8	PG11	I/O	FT_sh3	LPTIM1_IN2, SPI1_SCK/I2S1_CK, SPDIFRX1_IN0, OCTOSPIM_P2_IO7, SDMMC2_D2, USART10_RX, DCMI_D3/PSSI_D3, LCD_B3, EVENTOUT	-
-	-	125	C6	E8	D8	156	C8	-	-	-	127	B8	155	C7	PG12	I/O	FT_sh3	LPTIM1_IN1, OCTOSPIM_P2_NCS, SPI6_MISO/I2S6_SDI, USART6_RTS, SPDIFRX1_IN1, LCD_B4, SDMMC2_D3, USART10_TX, FMC_NE4, LCD_B1, EVENTOUT	-

Pin/ball name(1) (2)															Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
LQFP100 with SMPS	TFBGA100 with SMPS	LQFP144 with SMPS	WLCSP132 with SMPS	UFBGA169 with SMPS	UFBGA176+25 with SMPS	LQFP176 with SMPS	TFBGA225 with SMPS	LQFP64	TFBGA100	LQFP100	LQFP144	UFBGA176+25	LQFP176	TFBGA216					
-	-	126	D7	D7	B7	157	D8	-	-	-	128	A8	156	B3	PG13	I/O	FT_sh3	TRACED0, LPTIM1_OUT, SPI6_SCK/I2S6_CK, USART6_CTS/ USART6_NSS, SDMMC2_D6, USART10_CTS/ USART10_NSS, FMC_A24, LCD_R0, EVENTOUT	-
-	-	127	C7	C7	C7	158	A7	-	-	-	129	A7	157	A4	PG14	I/O	FT_sh3	TRACED1, LPTIM1_ETR, SPI6_MOSI/I2S6_SDO, USART6_TX, OCTOSPIM_P1_IO7, SDMMC2_D7, USART10_RTS, FMC_A25, LCD_B0, EVENTOUT	-
-	-	-	-	-	K7	159	-	-	-	-	130	H6	158	F7	VSS	S	-	-	-
-	-	-	A7	-	-	160	-	-	-	-	131	C7	159	E8	VDD	S	-	-	-
-	-	-	-	-	-	-	B7	-	-	-	-	-	-	D8	PK3	I/O	FT_h1	OCTOSPIM_P2_IO6, LCD_B4, EVENTOUT	-
-	-	-	-	-	-	-	C7	-	-	-	-	-	-	D7	PK4	I/O	FT_h1	OCTOSPIM_P2_IO7, LCD_B5, EVENTOUT	-
-	-	-	-	-	-	-	A6	-	-	-	-	-	-	C6	PK5	I/O	FT_h1	OCTOSPIM_P2_NCS, LCD_B6, EVENTOUT	-
-	-	-	-	-	-	-	B6	-	-	-	-	-	-	C5	PK6	I/O	FT_h1	OCTOSPIM_P2_DQS, LCD_B7, EVENTOUT	-
-	-	-	-	-	-	-	D7	-	-	-	-	-	-	C4	PK7	I/O	FT	LCD_DE, EVENTOUT	-
-	-	128	B7	-	K8	-	G8	-	-	-	-	-	-	-	VSS	S	-	-	-
-	-	129	-	-	-	-	-	-	-	-	-	-	-	G5	VDD	S	-	-	-
-	-	-	B8	-	-	-	-	-	-	-	-	-	-	-	VDDMMC		-	-	-
-	-	-	-	E7	D7	161	A5	-	-	-	132	B7	160	B7	PG15	I/O	FT_h1	USART6_CTS/ USART6_NSS, OCTOSPIM_P2_DQS, USART10_CK, FMC_SDNCAS, DCMI_D13/PSSI_D13, EVENTOUT	-
89	B6	130	A8	F7	A6	162	C6	55	A7	89	133	A10	161	A10	PB3(JTDO/ TRACESWO)	I/O	FT_h0	JTDO/TRACESWO, TIM2_CH2, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, SPI6_SCK/I2S6_CK, SDMMC2_D2, CRS_SYNC, UART7_RX, EVENTOUT	-
90	C5	131	E7	B6	B6	163	B5	56	A6	90	134	A9	162	A9	PB4(NJTRST)	I/O	FT_h0	NJTRST, TIM16_BKIN, TIM3_CH1, SPI1_MISO/I2S1_SDI, SPI3_MISO/I2S3_SDI, SPI2_SS/I2S2_WS, SPI6_MISO/I2S6_SDI, SDMMC2_D3, UART7_TX, EVENTOUT	-

Pin/ball name(1) (2)															Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
LQFP100 with SMPS	TFBGA100 with SMPS	LQFP144 with SMPS	WLCSP132 with SMPS	UFBGA169 with SMPS	UFBGA176+25 with SMPS	LQFP176 with SMPS	TFBGA225 with SMPS	LQFP64	TFBGA100	LQFP100	LQFP144	UFBGA176+25	LQFP176	TFBGA216					
91	A6	132	F7	C6	C6	164	E7	57	C5	91	135	A6	163	A8	PB5	I/O	FT_h0	TIM17_BKIN, TIM3_CH2, I2C1_SMBA, SPI1_MOSI/I2S1_SDO, I2C4_SMBA, SPI3_MOSI/I2S3_SDO, SPI6_MOSI/I2S6_SDO, FDCAN2_RX, OTG_HS_ULPI_D7, LCD_B5, FMC_SDCKE1, DCMI_D10/PSSI_D10, UART5_RX, EVENTOUT	-
92	D4	133	C8	A5	A5	165	A4	58	B5	92	136	B6	164	B6	PB6	I/O	FT_f	TIM16_CH1N, TIM4_CH1, I2C1_SCL, HDMI_CEC, I2C4_SCL, USART1_TX, LPUART1_TX, FDCAN2_TX, OCTOSPIM_P1_NCS, DFSDM1_DATIN5, FMC_SDNE1, DCMI_D5/PSSI_D5, UART5_TX, EVENTOUT	-
93	B5	134	D8	D6	B5	166	D6	59	A5	93	137	B5	165	B5	PB7	I/O	FT_fa	TIM17_CH1N, TIM4_CH2, I2C1_SDA, I2C4_SDA, USART1_RX, LPUART1_RX, DFSDM1_CKIN5, FMC_NL, DCMI_VSYNC/ PSSI_RDY, EVENTOUT	PVD_IN
94	A5	135	A9	E6	C5	167	C5	60	D5	94	138	D6	166	E6	BOOT0	I	B	-	VPP
95	A4	136	B9	B5	A2	168	B4	61	B4	95	139	A5	167	A7	PB8	I/O	FT_fsh3	TIM16_CH1, TIM4_CH3, DFSDM1_CKIN7, I2C1_SCL, I2C4_SCL, SDMMC1_CKIN, UART4_RX, FDCAN1_RX, SDMMC2_D4, SDMMC1_D4, DCMI_D6/PSSI_D6, LCD_B6, EVENTOUT	-
96	E3	137	E8	C5	B3	169	A3	62	A4	96	140	B4	168	B4	PB9	I/O	FT_fsh3	TIM17_CH1, TIM4_CH4, DFSDM1_DATIN7, I2C1_SDA, SPI2_SS/ I2S2_WS, I2C4_SDA, SDMMC1_CDIR, UART4_TX, FDCAN1_TX, SDMMC2_D5, I2C4_SMBA, SDMMC1_D5, DCMI_D7/PSSI_D7, LCD_B7, EVENTOUT	-

Pin/ball name[(1)] [(2)]															Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
LQFP100 with SMPS	TFBGA100 with SMPS	LQFP144 with SMPS	WLCSP132 with SMPS	UFBGA169 with SMPS	UFBGA176+25 with SMPS	LQFP176 with SMPS	TFBGA225 with SMPS	LQFP64	TFBGA100	LQFP100	LQFP144	UFBGA176+25	LQFP176	TFBGA216					
97	B4	138	F8	D5	B4	170	B3	-	D4	97	141	A4	169	A6	PE0	I/O	FT_h2	LPTIM1_ETR, TIM4_ETR, LPTIM2_ETR, UART8_RX, SAI2_MCK_A, FMC_NBL0, DCMI_D2/ PSSI_D2, LCD_R0, EVENTOUT	-
-	C4	139	C9	D4	C4	171	C4	-	C4	98	142	A3	170	A5	PE1	I/O	FT_h2	LPTIM1_IN2, UART8_TX, FMC_NBL1, DCMI_D3/ PSSI_D3, LCD_R6, EVENTOUT	-
-	-	140	A10	A4	A4	172	E6	-	-	-	-	-	-	-	VCAP	S	-	-	-
98	-	141	B10	-	K10	173	-	63	E4	99	-	-	-	F6	VSS	S	-	-	-
-	D3	142	D9	C4	D4	174	D5	-	F7	-	143	C6	171	E5	PDR_ON	S	-	-	-
99	-	143	A11	B4	A3	175	F5	-	-	-	-	-	-	-	VDDLDO	S	-	-	-
100	-	-	-	-	-	-	-	64	-	100	144	-	172	E7	VDD	S	-	-	-
-	-	-	-	-	-	-	A2	-	-	-	-	D4	173	C3	PI4	I/O	FT_h2	TIM8_BKIN, SAI2_MCK_A, TIM8_BKIN_COMP12, FMC_NBL2, DCMI_D5/ PSSI_D5, LCD_B4, EVENTOUT	-
-	-	-	-	-	-	-	B2	-	-	-	-	C4	174	D3	PI5	I/O	FT_h2	TIM8_CH1, SAI2_SCK_A, FMC_NBL3, DCMI_VSYNC/ PSSI_RDY, LCD_B5, EVENTOUT	-
-	-	-	-	-	-	-	C3	-	-	-	-	C3	175	D6	PI6	I/O	FT_h2	TIM8_CH2, SAI2_SD_A, FMC_D28, DCMI_D6/ PSSI_D6, LCD_B6, EVENTOUT	-
-	-	-	-	-	-	-	D4	-	-	-	-	C2	176	D4	PI7	I/O	FT_h2	TIM8_CH3, SAI2_FS_A, FMC_D29, DCMI_D7/PSSI_D7, LCD_B7, EVENTOUT	-
-	-	-	-	-	K12	-	-	-	-	-	-	J6	-	-	VSS	S	-	-	-
-	-	144	A12	-	-	176	-	-	-	-	-	-	-	-	VDD	S	-	-	-
-	-	-	-	-	G8	-	-	-	-	-	-	D7	-	-	VSS	S	-	-	-
-	-	-	-	-	G9	-	-	-	-	-	-	D8	-	-	VSS	S	-	-	-
-	-	-	-	-	H7	-	-	-	-	-	-	F8	-	-	VSS	S	-	-	-
-	-	-	-	-	H8	-	-	-	-	-	-	G12	-	-	VSS	S	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	F9	-	-	VSS	S	-	-	-
-	-	-	-	-	H9	-	-	-	-	-	-	H9	-	-	VSS	S	-	-	-
-	-	-	-	-	J8	-	-	-	-	-	-	H10	-	-	VSS	S	-	-	-
-	-	-	-	-	K9	-	-	-	-	-	-	J7	-	-	VSS	S	-	-	-
-	-	-	-	-	R15	-	-	-	-	-	-	J8	-	-	VSS	S	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	G6	-	-	VSS	S	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	K6	-	-	VSS	S	-	-	-

Pin/ball name(1) (2)															Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
LQFP100 with SMPS	TFBGA100 with SMPS	LQFP144 with SMPS	WLCSP132 with SMPS	UFBGA169 with SMPS	UFBGA176+25 with SMPS	LQFP176 with SMPS	TFBGA225 with SMPS	LQFP64	TFBGA100	LQFP100	LQFP144	UFBGA176+25	LQFP176	TFBGA216					
-	-	-	-	-	-	-	-	-	-	-	-	K7	-	-	VSS	S	-	-	-

1. The devices with SMPS correspond to commercial codes STM32H7A3xIxxQ and STM32H7A3xGxxQ.
2. A non-connected I/O in a given package is configured as an output tied to V_{SS}. Any analog peripheral connected to such a pad (such as OPAMP, VREF+) must be disabled.
3. Pxy_C and Pxy pins/balls are two separate pads (analog switch open). The analog switch is configured through a SYSCFG register. Refer to the product reference manual for a detailed description of the switch configuration bits.
4. There is a direct path between Pxy_C and Pxy pins/balls, through an analog switch. Pxy alternate functions are available on Pxy_C when the analog switch is closed. The analog switch is configured through a SYSCFG register. Refer to the product reference manual for a detailed description of the switch configuration bits.

Table 8. Port A alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	LPTIM1/TIM1/2/16/17	PDM_SAI1/TIM3/4/5/12/15	DFSDM1/LPTIM2/3/LPUART1/OCTOSPIM_P1/2/TIM8	CEC/DCMI/PSSI/DFSDM1/2/I2C1/2/3/4/LPTIM2/TIM15/USART1	CEC/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/SPI6/I2S6	DFSDM1/2/I2C4/OCTOSPIM_P1/SAI1/SPI3/I2S3/UART4	SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/I2S6/UART7/USART1/2/3/6	LPUART1/SAI2/SDMMC1/SPDIFRX1/SPI6/I2S6/UART4/5/8	FDCAN1/2/FMC/LCD/OCTOSPIM_P1/2/SDMMC2/SPDIFRX1/TIM13/14	CRS/FMC/LCD/OCTOSPIM_P1/OTG1_FS/OTG1_HS/SAI2/SDMMC2/TIM8	DFSDM1/2/I2C4/LCD/MDIOS/OCTOSPIM_P1/SDMMC2/SWPMI1/TIM1/8/UART7/9/USART10	FMC/LCD/MDIOS/SDMMC1/TIM1/8	COMP/DCMI/PSSI/LCD/TIM1	LCD/UART5	SYS
Port A	PA0	-	TIM2_CH1/TIM2_ETR	TIM5_CH1	TIM8_ETR	TIM15_BKIN	SPI6_SS/I2S6_WS	-	USART2_CTS/USART2_NSS	UART4_TX	SDMMC2_CMD	SAI2_SD_B	-	-	-	-	EVENTOUT
	PA1	-	TIM2_CH2	TIM5_CH2	LPTIM3_OUT	TIM15_CH1N	-	-	USART2_RTS	UART4_RX	OCTOSPIM_P1_IO3	SAI2_MCK_B	OCTOSPIM_P1_DQS	-	-	LCD_R2	EVENTOUT
	PA2	-	TIM2_CH3	TIM5_CH3	-	TIM15_CH1	-	DFSDM2_CKIN1	USART2_TX	SAI2_SCK_B	-	-	-	MDIOS_MDIO	-	LCD_R1	EVENTOUT
	PA3	-	TIM2_CH4	TIM5_CH4	OCTOSPIM_P1_CLK	TIM15_CH2	I2S6_MCK	-	USART2_RX	-	LCD_B2	OTG_HS_ULPI_D0	-	-	-	LCD_B5	EVENTOUT
	PA4	-	-	TIM5_ETR	-	-	SPI1_SS/I2S1_WS	SPI3_SS/I2S3_WS	USART2_CK	SPI6_SS/I2S6_WS	-	-	-	-	DCMI_HSYNC/PSSI_DE	LCD_VSYNC	EVENTOUT
	PA5	PWR_NDSTOP2	TIM2_CH1/TIM2_ETR	-	TIM8_CH1N	-	SPI1_SCK/I2S1_CK	-	-	SPI6_SCK/I2S6_CK	-	OTG_HS_ULPI_CK	-	-	PSSI_D14	LCD_R4	EVENTOUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO/I2S1_SDI	OCTOSPIM_P1_IO3	-	SPI6_MISO/I2S6_SDI	TIM13_CH1	TIM8_BKIN_COMP12	MDIOS_MDC	TIM1_BKIN_COMP12	DCMI_PIXCLK/PSSI_PDCK	LCD_G2	EVENTOUT
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	DFSDM2_DATIN1	SPI1_MOSI/I2S1_SDO	-	-	SPI6_MOSI/I2S6_SDO	TIM14_CH1	OCTOSPIM_P1_IO2	-	FMC_SDNWE	-	LCD_VSYNC	EVENTOUT
	PA8	MCO1	TIM1_CH1	-	TIM8_BKIN2	I2C3_SCL	-	-	USART1_CK	-	-	OTG_HS_SOF	UART7_RX	TIM8_BKIN2_COMP12	LCD_B3	LCD_R6	EVENTOUT
	PA9	-	TIM1_CH2	-	LPUART1_TX	I2C3_SMBA	SPI2_SCK/I2S2_CK	-	USART1_TX	-	-	-	-	-	DCMI_D0/PSSI_D0	LCD_R5	EVENTOUT
	PA10	-	TIM1_CH3	-	LPUART1_RX	-	-	-	USART1_RX	-	-	OTG_HS_ID	MDIOS_MDIO	LCD_B4	DCMI_D1/PSSI_D1	LCD_B1	EVENTOUT
	PA11	-	TIM1_CH4	-	LPUART1_CTS	-	SPI2_SS/I2S2_WS	UART4_RX	USART1_CTS/USART1_NSS	-	FDCAN1_RX	-	-	-	-	LCD_R4	EVENTOUT
	PA12	-	TIM1_ETR	-	LPUART1_RTS	-	SPI2_SCK/I2S2_CK	UART4_TX	USART1_RTS	SAI2_FS_B	FDCAN1_TX	-	-	-	-	LCD_R5	EVENTOUT
	PA13	JTMS/SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA14	JTCK/SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	TIM2_CH1/TIM2_ETR	-	-	HDMI_CEC	SPI1_SS/I2S1_WS	SPI3_SS/I2S3_WS	SPI6_SS/I2S6_WS	UART4_RTS	LCD_R3	-	UART7_TX	-	-	LCD_B6	EVENTOUT

Table 9. Port B alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	LPTIM1/TIM1/2/16/17	PDM_SAI1/TIM3/4/5/12/15	DFSDM1/LPTIM2/3/LPUART1/OCTOSPIM_P1/2/TIM8	CEC/DCMI/PSSI/DFSDM1/2/I2C1/2/3/4/LPTIM2/TIM15/USART1	CEC/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/SPI6/I2S6	DFSDM1/2/I2C4/OCTOSPIM_P1/SAI1/SPI3/I2S3/UART4	SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/I2S6/UART7/USART1/2/3/6	LPUART1/SAI2/SDMMC1/SPDIFRX1/SPI6/I2S6/UART4/5/8	FDCAN1/2/FMC/LCD/OCTOSPIM_P1/2/SDMMC2/SPDIFRX1/TIM13/14	CRS/FMC/LCD/OCTOSPIM_P1/OTG1_FS/OTG1_HS/SAI2/SDMMC2/TIM8	DFSDM1/2/I2C4/LCD/MDIOS/OCTOSPIM_P1/SDMMC2/SWPMI1/TIM1/8/UART7/9/USART10	FMC/LCD/MDIOS/SDMMC1/TIM1/8	COMP/DCMI/PSSI/LCD/TIM1	LCD/UART5	SYS
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	DFSDM2_CKOUT	-	DFSDM1_CKOUT	-	UART4_CTS	LCD_R3	OTG_HS_ULPI_D1	OCTOSPIM_P1_IO1	-	-	LCD_G1	EVENTOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	DFSDM1_DATIN1	-	-	LCD_R6	OTG_HS_ULPI_D2	OCTOSPIM_P1_IO0	-	-	LCD_G0	EVENTOUT
	PB2	RTC_OUT2	-	SAI1_D1	-	DFSDM1_CKIN1	-	SAI1_SD_A	SPI3_MOSI/I2S3_SDO	-	OCTOSPIM_P1_CLK	OCTOSPIM_P1_DQS	-	-	-	-	EVENTOUT
	PB3	JTDO/TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK/I2S1_CK	SPI3_SCK/I2S3_CK	-	SPI6_SCK/I2S6_CK	SDMMC2_D2	CRS_SYNC	UART7_RX	-	-	-	EVENTOUT
	PB4	NJTRST	TIM16_BKIN	TIM3_CH1	-	-	SPI1_MISO/I2S1_SDI	SPI3_MISO/I2S3_SDI	SPI2_SS/I2S2_WS	SPI6_MISO/I2S6_SDI	SDMMC2_D3	-	UART7_TX	-	-	-	EVENTOUT
	PB5	-	TIM17_BKIN	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI/I2S1_SDO	I2C4_SMBA	SPI3_MOSI/I2S3_SDO	SPI6_MOSI/I2S6_SDO	FDCAN2_RX	OTG_HS_ULPI_D7	LCD_B5	FMC_SDCKE1	DCMI_D10/PSSI_D10	UART5_RX	EVENTOUT
	PB6	-	TIM16_CH1N	TIM4_CH1	-	I2C1_SCL	HDMI_CEC	I2C4_SCL	USART1_TX	LPUART1_TX	FDCAN2_TX	OCTOSPIM_P1_NCS	DFSDM1_DATIN5	FMC_SDNE1	DCMI_D5/PSSI_D5	UART5_TX	EVENTOUT
	PB7	-	TIM17_CH1N	TIM4_CH2	-	I2C1_SDA	-	I2C4_SDA	USART1_RX	LPUART1_RX	-	-	DFSDM1_CKIN5	FMC_NL	DCMI_VSYNC/PSSI_RDY	-	EVENTOUT
	PB8	-	TIM16_CH1	TIM4_CH3	DFSDM1_CKIN7	I2C1_SCL	-	I2C4_SCL	SDMMC1_CKIN	UART4_RX	FDCAN1_RX	SDMMC2_D4	-	SDMMC1_D4	DCMI_D6/PSSI_D6	LCD_B6	EVENTOUT
	PB9	-	TIM17_CH1	TIM4_CH4	DFSDM1_DATIN7	I2C1_SDA	SPI2_SS/I2S2_WS	I2C4_SDA	SDMMC1_CDIR	UART4_TX	FDCAN1_TX	SDMMC2_D5	I2C4_SMBA	SDMMC1_D5	DCMI_D7/PSSI_D7	LCD_B7	EVENTOUT
	PB10	-	TIM2_CH3	-	LPTIM2_IN1	I2C2_SCL	SPI2_SCK/I2S2_CK	DFSDM1_DATIN7	USART3_TX	-	OCTOSPIM_P1_NCS	OTG_HS_ULPI_D3	-	-	-	LCD_G4	EVENTOUT
	PB11	-	TIM2_CH4	-	LPTIM2_ETR	I2C2_SDA	-	DFSDM1_CKIN7	USART3_RX	-	-	OTG_HS_ULPI_D4	-	-	-	LCD_G5	EVENTOUT
	PB12	-	TIM1_BKIN	-	OCTOSPIM_P1_NCLK	I2C2_SMBA	SPI2_SS/I2S2_WS	DFSDM1_DATIN1	USART3_CK	-	FDCAN2_RX	OTG_HS_ULPI_D5	DFSDM2_DATIN1	-	TIM1_BKIN_COMP12	UART5_RX	EVENTOUT
	PB13	-	TIM1_CH1N	-	LPTIM2_OUT	DFSDM2_CKIN1	SPI2_SCK/I2S2_CK	DFSDM1_CKIN1	USART3_CTS/USART3_NSS	-	FDCAN2_TX	OTG_HS_ULPI_D6	-	SDMMC1_D0	DCMI_D2/PSSI_D2	UART5_TX	EVENTOUT
	PB14	-	TIM1_CH2N	TIM12_CH1	TIM8_CH2N	USART1_TX	SPI2_MISO/I2S2_SDI	DFSDM1_DATIN2	USART3_RTS	UART4_RTS	SDMMC2_D0	-	-	-	-	LCD_CLK	EVENTOUT
	PB15	RTC_REFIN	TIM1_CH3N	TIM12_CH2	TIM8_CH3N	USART1_RX	SPI2_MOSI/I2S2_SDO	DFSDM1_CKIN2	-	UART4_CTS	SDMMC2_D1	-	-	-	-	LCD_G7	EVENTOUT

Table 10. Port C alternate functions

	Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
Port		SYS	LPTIM1/TIM1/2/16/17	PDM_SAI1/TIM3/4/5/12/15	DFSDM1/LPTIM2/3/LPUART1/OCTOSPIM_P1/2/TIM8	CEC/DCMI/PSSI/DFSDM1/2/I2C1/2/3/4/LPTIM2/TIM15/USART1	CEC/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/SPI6/I2S6	DFSDM1/2/I2C4/OCTOSPIM_P1/SAI1/SPI3/I2S3/UART4	SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/I2S6/UART7/USART1/2/3/6	LPUART1/SAI2/SDMMC1/SPDIFRX1/SPI6/I2S6/UART4/5/8	FDCAN1/2/FMC/LCD/OCTOSPIM_P1/2/SDMMC2/SPDIFRX1/TIM13/14	CRS/FMC/LCD/OCTOSPIM_P1/OTG1_FS/OTG1_HS/SAI2/SDMMC2/TIM8	DFSDM1/2/I2C4/LCD/MDIOS/OCTOSPIM_P1/SDMMC2/SWPMI1/TIM1/8/UART7/9/USART10	FMC/LCD/MDIOS/SDMMC1/TIM1/8	COMP/DCMI/PSSI/LCD/TIM1	LCD/UART5	SYS
Port C	PC0	-	-	-	DFSDM1_CKIN0	-	-	DFSDM1_DATIN4	-	SAI2_FS_B	FMC_A25	OTG_HS_ULPI_STP	LCD_G2	FMC_SDNWE	-	LCD_R5	EVENTOUT
	PC1	TRACED0	-	SAI1_D1	DFSDM1_DATIN0	DFSDM1_CKIN4	SPI2_MOSI/I2S2_SDO	SAI1_SD_A	-	-	SDMMC2_CK	OCTOSPIM_P1_IO4	-	MDIOS_MDC	-	LCD_G5	EVENTOUT
	PC2	PWR_CSTOP	-	-	DFSDM1_CKIN1	-	SPI2_MISO/I2S2_SDI	DFSDM1_CKOUT	-	-	OCTOSPIM_P1_IO2	OTG_HS_ULPI_DIR	OCTOSPIM_P1_IO5	FMC_SDNE0	-	-	EVENTOUT
	PC3	PWR_CSLEEP	-	-	DFSDM1_DATIN1	-	SPI2_MOSI/I2S2_SDO	-	-	-	OCTOSPIM_P1_IO0	OTG_HS_ULPI_NXT	OCTOSPIM_P1_IO6	FMC_SDCKE0	-	-	EVENTOUT
	PC4	-	-	-	DFSDM1_CKIN2	-	I2S1_MCK	-	-	-	SPDIFRX1_IN2	-	-	FMC_SDNE0	-	LCD_R7	EVENTOUT
	PC5	-	-	SAI1_D3	DFSDM1_DATIN2	PSSI_D15	-	-	-	-	SPDIFRX1_IN3	OCTOSPIM_P1_DQS	-	FMC_SDCKE0	COMP1_OUT	LCD_DE	EVENTOUT
	PC6	-	-	TIM3_CH1	TIM8_CH1	DFSDM1_CKIN3	I2S2_MCK	-	USART6_TX	SDMMC1_D0DIR	FMC_NWAIT	SDMMC2_D6	-	SDMMC1_D6	DCMI_D0/PSSI_D0	LCD_HSYNC	EVENTOUT
	PC7	TRGIO	-	TIM3_CH2	TIM8_CH2	DFSDM1_DATIN3	-	I2S3_MCK	USART6_RX	SDMMC1_D123DIR	FMC_NE1	SDMMC2_D7	SWPMI_TX	SDMMC1_D7	DCMI_D1/PSSI_D1	LCD_G6	EVENTOUT
	PC8	TRACED1	-	TIM3_CH3	TIM8_CH3	-	-	-	USART6_CK	UART5_RTS	FMC_NE2/FMC_NCE	FMC_INT	SWPMI_RX	SDMMC1_D0	DCMI_D2/PSSI_D2	-	EVENTOUT
	PC9	MCO2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S_CKIN	-	-	UART5_CTS	OCTOSPIM_P1_IO0	LCD_G3	SWPMI_SUSPEND	SDMMC1_D1	DCMI_D3/PSSI_D3	LCD_B2	EVENTOUT
	PC10	-	-	-	DFSDM1_CKIN5	DFSDM2_CKIN0	-	SPI3_SCK/I2S3_CK	USART3_TX	UART4_TX	OCTOSPIM_P1_IO1	LCD_B1	SWPMI_RX	SDMMC1_D2	DCMI_D8/PSSI_D8	LCD_R2	EVENTOUT
	PC11	-	-	-	DFSDM1_DATIN5	DFSDM2_DATIN0	-	SPI3_MISO/I2S3_SDI	USART3_RX	UART4_RX	OCTOSPIM_P1_NCS	-	-	SDMMC1_D3	DCMI_D4/PSSI_D4	LCD_B4	EVENTOUT
	PC12	TRACED3	-	TIM15_CH1	-	DFSDM2_CKOUT	SPI6_SCK/I2S6_CK	SPI3_MOSI/I2S3_SDO	USART3_CK	UART5_TX	-	-	-	SDMMC1_CK	DCMI_D9/PSSI_D9	LCD_R6	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Table 11. Port D alternate functions

	Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	LPTIM1/ TIM1/2/16/17	PDM_SAI1/ TIM3/4/5/12/15	DFSDM1/ LPTIM2/3/ LPUART1/ OCTOSPIM_P1/2/ TIM8	CEC/DCMI/PSSI/ DFSDM1/2/ I2C1/2/3/4/ LPTIM2/TIM15/ USART1	CEC/SPI1/ I2S1/SPI2/ I2S2/SPI3/ I2S3/ SPI4/5/ SPI6/I2S6	DFSDM1/2/I2C4/ OCTOSPIM_P1/ SAI1/SPI3/I2S3/ UART4	SDMMC1/ SPI2/I2S2/ SPI3/I2S3/ SPI6/I2S6/ UART7/ USART1/2/3/6	LPUART1/ SAI2/ SDMMC1/ SPDIFRX1/ SPI6/I2S6/ UART4/5/8	FDCAN1/2/FMC/LC D/OCTOSPIM_P1/2/ SDMMC2/ SPDIFRX1/ TIM13/14	CRS/FMC/LCD/ OCTOSPIM_P1/ OTG1_FS/ OTG1_HS/SAI2/ SDMMC2/TIM8	DFSDM1/2/ I2C4/LCD/ MDIOS/ OCTOSPIM_P1/ SDMMC2/ SWPMI1/ TIM1/8/ UART7/9/ USART10	FMC/LCD/ MDIOS/ SDMMC1/ TIM1/8	COMP/ DCMI/ PSSI/LCD/ TIM1	LCDUART5	SYS
Port D	PD0	-	-	-	DFSDM1_CKIN6	-	-	-	-	UART4_RX	FDCAN1_RX	-	UART9_CTS	FMC_D2/ FMC_DA2	-	LCD_B1	EVENTOUT
	PD1	-	-	-	DFSDM1_DATIN6	-	-	-	-	UART4_TX	FDCAN1_TX	-	-	FMC_D3/ FMC_DA3	-	-	EVENTOUT
	PD2	TRACED2	-	TIM3_ETR	-	TIM15_BKIN	-	-	-	UART5_RX	LCD_B7	-	-	SDMMC1_CMD	DCMI_D11/ PSSI_D11	LCD_B2	EVENTOUT
	PD3	-	-	-	DFSDM1_CKOUT	-	SPI2_SCK/ I2S2_CK	-	USART2_CTS/ USART2_NSS	-	-	-	-	FMC_CLK	DCMI_D5/ PSSI_D5	LCD_G7	EVENTOUT
	PD4	-	-	-	-	-	-	-	USART2_RTS	-	-	OCTOSPIM_P1_IO4	-	FMC_NOE	-	-	EVENTOUT
	PD5	-	-	-	-	-	-	-	USART2_TX	-	-	OCTOSPIM_P1_IO5	-	FMC_NWE	-	-	EVENTOUT
	PD6	-	-	SAI1_D1	DFSDM1_CKIN4	DFSDM1_DATIN1	SPI3_MOSI/ I2S3_SDO	SAI1_SD_A	USART2_RX	-	-	OCTOSPIM_P1_IO6	SDMMC2_CK	FMC_NWAIT	DCMI_D10/ PSSI_D10	LCD_B2	EVENTOUT
	PD7	-	-	-	DFSDM1_DATIN4	-	SPI1_MOSI/ I2S1_SDO	DFSDM1_CKIN1	USART2_CK	-	SPDIFRX1_IN0	OCTOSPIM_P1_IO7	SDMMC2_CMD	FMC_NE1	-	-	EVENTOUT
	PD8	-	-	-	DFSDM1_CKIN3	-	-	-	USART3_TX	-	SPDIFRX1_IN1	-	-	FMC_D13/ FMC_DA13	-	-	EVENTOUT
	PD9	-	-	-	DFSDM1_DATIN3	-	-	-	USART3_RX	-	-	-	-	FMC_D14/ FMC_DA14	-	-	EVENTOUT
	PD10	-	-	-	DFSDM1_CKOUT	DFSDM2_CKOUT	-	-	USART3_CK	-	-	-	-	FMC_D15/ FMC_DA15	-	LCD_B3	EVENTOUT
	PD11	-	-	-	LPTIM2_IN2	I2C4_SMBA	-	-	USART3_CTS/ USART3_NSS	-	OCTOSPIM_P1_IO0	SAI2_SD_A	-	FMC_A16/ FMC_CLE	-	-	EVENTOUT
	PD12	-	LPTIM1_IN1	TIM4_CH1	LPTIM2_IN1	I2C4_SCL	-	-	USART3_RTS	-	OCTOSPIM_P1_IO1	SAI2_FS_A	-	FMC_A17/ FMC_ALE	DCMI_D12/ PSSI_D12	-	EVENTOUT
	PD13	-	LPTIM1_OUT	TIM4_CH2	-	I2C4_SDA	-	-	-	-	OCTOSPIM_P1_IO3	SAI2_SCK_A	UART9_RTS	FMC_A18	DCMI_D13/ PSSI_D13	-	EVENTOUT
	PD14	-	-	TIM4_CH3	-	-	-	-	-	UART8_CTS	-	-	UART9_RX	FMC_D0/ FMC_DA0	-	-	EVENTOUT
	PD15	-	-	TIM4_CH4	-	-	-	-	-	UART8_RTS	-	-	UART9_TX	FMC_D1/ FMC_DA1	-	-	EVENTOUT

Table 12. Port E alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	LPTIM1/TIM1/2/16/17	PDM_SAI1/TIM3/4/5/12/15	DFSDM1/LPTIM2/3/LPUART1/OCTOSPIM_P1/2/TIM8	CEC/DCMI/PSSI/DFSDM1/2/I2C1/2/3/4/LPTIM2/TIM15/USART1	CEC/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/SPI6/I2S6	DFSDM1/2/I2C4/OCTOSPIM_P1/SAI1/SPI3/I2S3/UART4	SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/I2S6/UART7/USART1/2/3/6	LPUART1/SAI2/SDMMC1/SPDIFRX1/SPI6/I2S6/UART4/5/8	FDCAN1/2/FMC/LCD/OCTOSPIM_P1/2/SDMMC2/SPDIFRX1/TIM13/14	CRS/FMC/LCD/OCTOSPIM_P1/OTG1_FS/OTG1_HS/SAI2/SDMMC2/TIM8	DFSDM1/2/I2C4/LCD/MDIOS/OCTOSPIM_P1/SDMMC2/SWPMI1/TIM1/8/UART7/9/USART10	FMC/LCD/MDIOS/SDMMC1/TIM1/8	COMP/DCMI/PSSI/LCD/TIM1	LCD/UART5	SYS
Port E	PE0	-	LPTIM1_ETR	TIM4_ETR	-	LPTIM2_ETR	-	-	-	UART8_Rx	-	SAI2_MCK_A	-	FMC_NBL0	DCMI_D2/PSSI_D2	LCD_R0	EVENTOUT
	PE1	-	LPTIM1_IN2	-	-	-	-	-	-	UART8_Tx	-	-	-	FMC_NBL1	DCMI_D3/PSSI_D3	LCD_R6	EVENTOUT
	PE2	TRACECLK	-	SAI1_CK1	-	-	SPI4_SCK	SAI1_MCLK_A	-	-	OCTOSPIM_P1_IO2	-	USART10_RX	FMC_A23	-	-	EVENTOUT
	PE3	TRACED0	-	-	-	TIM15_BKIN	-	SAI1_SD_B	-	-	-	-	USART10_TX	FMC_A19	-	-	EVENTOUT
	PE4	TRACED1	-	SAI1_D2	DFSDM1_DATIN3	TIM15_CH1N	SPI4_SS	SAI1_FS_A	-	-	-	-	-	FMC_A20	DCMI_D4/PSSI_D4	LCD_B0	EVENTOUT
	PE5	TRACED2	-	SAI1_CK2	DFSDM1_CKIN3	TIM15_CH1	SPI4_MISO	SAI1_SCK_A	-	-	-	-	-	FMC_A21	DCMI_D6/PSSI_D6	LCD_G0	EVENTOUT
	PE6	TRACED3	TIM1_BKIN2	SAI1_D1	-	TIM15_CH2	SPI4_MOSI	SAI1_SD_A	-	-	-	SAI2_MCK_B	TIM1_BKIN2_COMP12	FMC_A22	DCMI_D7/PSSI_D7	LCD_G1	EVENTOUT
	PE7	-	TIM1_ETR	-	DFSDM1_DATIN2	-	-	-	UART7_RX	-	-	OCTOSPIM_P1_IO4	-	FMC_D4/FMC_DA4	-	-	EVENTOUT
	PE8	-	TIM1_CH1N	-	DFSDM1_CKIN2	-	-	-	UART7_TX	-	-	OCTOSPIM_P1_IO5	-	FMC_D5/FMC_DA5	COMP2_OUT	-	EVENTOUT
	PE9	-	TIM1_CH1	-	DFSDM1_CKOUT	-	-	-	UART7_RTS	-	-	OCTOSPIM_P1_IO6	-	FMC_D6/FMC_DA6	-	-	EVENTOUT
	PE10	-	TIM1_CH2N	-	DFSDM1_DATIN4	-	-	-	UART7_CTS	-	-	OCTOSPIM_P1_IO7	-	FMC_D7/FMC_DA7	-	-	EVENTOUT
	PE11	-	TIM1_CH2	-	DFSDM1_CKIN4	-	SPI4_SS	-	-	-	-	SAI2_SD_B	OCTOSPIM_P1_NCS	FMC_D8/FMC_DA8	-	LCD_G3	EVENTOUT
	PE12	-	TIM1_CH3N	-	DFSDM1_DATIN5	-	SPI4_SCK	-	-	-	-	SAI2_SCK_B	-	FMC_D9/FMC_DA9	COMP1_OUT	LCD_B4	EVENTOUT
	PE13	-	TIM1_CH3	-	DFSDM1_CKIN5	-	SPI4_MISO	-	-	-	-	SAI2_FS_B	-	FMC_D10/FMC_DA10	COMP2_OUT	LCD_DE	EVENTOUT
	PE14	-	TIM1_CH4	-		-	SPI4_MOSI	-	-	-	-	SAI2_MCK_B	-	FMC_D11/FMC_DA11	-	LCD_CLK	EVENTOUT
	PE15	-	TIM1_BKIN	-		-	-	-	-	-	-	-	USART10_CK	FMC_D12/FMC_DA12	TIM1_BKIN_COMP12	LCD_R7	EVENTOUT

Table 13. Port F alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	LPTIM1/ TIM1/2/16/17	PDM_SAI1/ TIM3/4/5/12/15	DFSDM1/ LPTIM2/3/ LPUART1/ OCTOSPIM_P1/2/ TIM8	CEC/DCMI/ PSSI/ DFSDM1/2/ I2C1/2/3/4/ LPTIM2/ TIM15/ USART1	CEC/SPI1/ I2S1/SPI2/ I2S2/SPI3/ I2S3/SPI4/5/ SPI6/I2S6	DFSDM1/2/I2C4/ OCTOSPIM_P1/ SAI1/SPI3/I2S3/ UART4	SDMMC1/SPI2/ I2S2/SPI3/ I2S3/SPI6/ I2S6/UART7/ USART1/2/3/6	LPUART1/ SAI2/ SDMMC1/ SPDIFRX1/ SPI6/I2S6/ UART4/5/8	FDCAN1/2/FMC/LCD/ OCTOSPIM_P1/2/ SDMMC2/SPDIFRX1/ TIM13/14	CRS/FMC/LCD/ OCTOSPIM_P1/ OTG1_FS/OTG1_HS/ SAI2/SDMMC2/TIM8	DFSDM1/2/ I2C4/LCD/ MDIOS/ OCTOSPIM_P1/ SDMMC2/ SWPMI1/TIM1/8/ UART7/9/ USART10	FMC/LCD/ MDIOS/ SDMMC1/ TIM1/8	COMP/ DCMI/ PSSI/LCD/ TIM1	LCD/ UART5	SYS
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	OCTOSPIM_P2_IO0	-	-	FMC_A0	-	-	EVENTOUT
	PF1	-	-	-	-	I2C2_SCL	-	-	-	-	OCTOSPIM_P2_IO1	-	-	FMC_A1	-	-	EVENTOUT
	PF2	-	-	-	-	I2C2_SMBA	-	-	-	-	OCTOSPIM_P2_IO2	-	-	FMC_A2	-	-	EVENTOUT
	PF3	-	-	-	-	-	-	-	-	-	OCTOSPIM_P2_IO3	-	-	FMC_A3	-	-	EVENTOUT
	PF4	-	-	-	-	-	-	-	-	-	OCTOSPIM_P2_CLK	-	-	FMC_A4	-	-	EVENTOUT
	PF5	-	-	-	-	-	-	-	-	-	OCTOSPIM_ P2_NCLK	-	-	FMC_A5	-	-	EVENTOUT
	PF6	-	TIM16_CH1	-	-	-	SPI5_SS	SAI1_SD_B	UART7_Rx	-	-	OCTOSPIM_P1_IO3	-	-	-	-	EVENTOUT
	PF7	-	TIM17_CH1	-	-	-	SPI5_SCK	SAI1_MCLK_B	UART7_Tx	-	-	OCTOSPIM_P1_IO2	-	-	-	-	EVENTOUT
	PF8	-	TIM16_CH1N	-	-	-	SPI5_MISO	SAI1_SCK_B	UART7_RTS	-	TIM13_CH1	OCTOSPIM_P1_IO0	-	-	-	-	EVENTOUT
	PF9	-	TIM17_CH1N	-	-	-	SPI5_MOSI	SAI1_FS_B	UART7_CTS	-	TIM14_CH1	OCTOSPIM_P1_IO1	-	-	-	-	EVENTOUT
	PF10	-	TIM16_BKIN	SAI1_D3	-	PSSI_D15	-	-	-	-	OCTOSPIM_P1_CLK	-	-	-	DCMI_D11/ PSSI_D11	LCD_DE	EVENTOUT
	PF11	-	-	-	-	-	SPI5_MOSI	-	-	-	OCTOSPIM_ P1_NCLK	SAI2_SD_B	-	FMC_SDNRAS	DCMI_D12/ PSSI_D12	-	EVENTOUT
	PF12	-	-	-	-	-	-	-	-	-	OCTOSPIM_ P2_DQS	-	-	FMC_A6	-	-	EVENTOUT
	PF13	-	-	-	DFSDM1_DATIN6	I2C4_SMBA	-	-	-	-	-	-	-	FMC_A7	-	-	EVENTOUT
	PF14	-	-	-	DFSDM1_CKIN6	I2C4_SCL	-	-	-	-	-	-	-	FMC_A8	-	-	EVENTOUT
	PF15	-	-	-	-	I2C4_SDA	-	-	-	-	-	-	-	FMC_A9	-	-	EVENTOUT

Table 14. Port G alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	LPTIM1/ TIM1/2/16/17	PDM_SAI1/ TIM3/4/5/12/15	DFSDM1/LPTIM2/3/ LPUART1/ OCTOSPIM_P1/2/ TIM8	CEC/DCMI/ PSSI/ DFSDM1/2/ I2C1/2/3/4/ LPTIM2/ TIM15/ USART1	CEC/SPI1/ I2S1/SPI2/ I2S2/SPI3/ I2S3/ SPI4/5/ SPI6/I2S6	DFSDM1/2/ I2C4/ OCTOSPIM_P1/ SAI1/SPI3/I2S3/ UART4	SDMMC1/ SPI2/I2S2/ SPI3/I2S3/ SPI6/I2S6/ UART7/ USART1/2/3/6	LPUART1/ SAI2/ SDMMC1/ SPDIFRX1/ SPI6/I2S6/ UART4/5/8	FDCAN1/2/FMC/LCD /OCTOSPIM_P1/2/ SDMMC2/SPDIFRX1/ TIM13/14	CRS/FMC/LCD/ OCTOSPIM_P1/ OTG1_FS/ OTG1_HS/SAI2/ SDMMC2/TIM8	DFSDM1/2/ I2C4/LCD/ MDIOS/ OCTOSPIM_P1/ SDMMC2/ SWPMI1/ TIM1/8/ UART7/9/ USART10	FMC/LCD/ MDIOS/ SDMMC1/ TIM1/8	COMP/DCMI/ PSSI/LCD/ TIM1	LCD/ UART5	SYS
Port G	PG0	-	-	-	-	-	-	-	-	-	OCTOSPIM_P2_IO4	-	UART9_RX	FMC_A10	-	-	EVENTOUT
	PG1	-	-	-	-	-	-	-	-	-	OCTOSPIM_P2_IO5	-	UART9_TX	FMC_A11	-	-	EVENTOUT
	PG2	-	-	-	TIM8_BKIN	-	-	-	-	-	-	-	TIM8_BKIN_ COMP12	FMC_A12	-	-	EVENTOUT
	PG3	-	-	-	TIM8_BKIN2	-	-	-	-	-	-	-	TIM8_BKIN2_ COMP12	FMC_A13	-	-	EVENTOUT
	PG4	-	TIM1_BKIN2	-	-	-	-	-	-	-	-	-	TIM1_BKIN2_ COMP12	FMC_A14/ FMC_BA0	-	-	EVENTOUT
	PG5	-	TIM1_ETR	-	-	-	-	-	-	-	-	-	-	FMC_A15/ FMC_BA1	-	-	EVENTOUT
	PG6	-	TIM17_BKIN	-	-	-	-	-	-	-	-	OCTOSPIM_P1_NCS	-	FMC_NE3	DCMI_D12/ PSSI_D12	LCD_R7	EVENTOUT
	PG7	-	-	-	-	-	-	SAI1_MCLK_A	USART6_CK	-	OCTOSPIM_P2_DQS	-	-	FMC_INT	DCMI_D13/ PSSI_D13	LCD_CLK	EVENTOUT
	PG8	-	-	-	TIM8_ETR	-	SPI6_SS/ I2S6_WS	-	USART6_RTS	SPDIFRX1_IN2	-	-	-	FMC_SDCLK	-	LCD_G7	EVENTOUT
	PG9	-	-	-	-	-	SPI1_MISO/ I2S1_SDI	-	USART6_RX	SPDIFRX1_IN3	OCTOSPIM_P1_IO6	SAI2_FS_B	SDMMC2_D0	FMC_NE2/ FMC_NCE	DCMI_VSYNC/ PSSI_RDY	-	EVENTOUT
	PG10	-	-	-	OCTOSPIM_P2_IO6	-	SPI1_SS/ I2S1_WS	-	-	-	LCD_G3	SAI2_SD_B	SDMMC2_D1	FMC_NE3	DCMI_D2/ PSSI_D2	LCD_B2	EVENTOUT
	PG11	-	LPTIM1_IN2	-	-	-	SPI1_SCK/ I2S1_CK	-	-	SPDIFRX1_IN0	OCTOSPIM_P2_IO7	SDMMC2_D2	USART10_RX	-	DCMI_D3/ PSSI_D3	LCD_B3	EVENTOUT
	PG12	-	LPTIM1_IN1	-	OCTOSPIM_P2_NCS	-	SPI6_MISO/ I2S6_SDI	-	USART6_RTS	SPDIFRX1_IN1	LCD_B4	SDMMC2_D3	USART10_TX	-	-	LCD_B1	EVENTOUT
	PG13	TRACED0	LPTIM1_OUT	-	-	-	SPI6_SCK/ I2S6_CK	-	USART6_CTS/ USART6_NSS	-	-	SDMMC2_D6	USART10_CTS/ USART10_NSS	-	-	LCD_R0	EVENTOUT
	PG14	TRACED1	LPTIM1_ETR	-	-	-	SPI6_MOSI/ I2S6_SDO	-	USART6_TX	-	OCTOSPIM_P1_IO7	SDMMC2_D7	USART10_RTS	-	-	LCD_B0	EVENTOUT
	PG15	-	-	-	-	-	-	-	USART6_CTS/ USART6_NSS	-	OCTOSPIM_P2_DQS	-	-	-	DCMI_D13/ PSSI_D13	-	EVENTOUT

Table 15. Port H alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	LPTIM1/TIM1/2/16/17	PDM_SAI1/TIM3/4/5/12/15	DFSDM1/LPTIM2/3/LPUART1/OCTOSPIM_P1/2/TIM8	CEC/DCMI/PSSI/DFSDM1/2/I2C1/2/3/4/LPTIM2/TIM15/USART1	CEC/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/SPI6/I2S6	DFSDM1/2/I2C4/OCTOSPIM_P1/SAI1/SPI3/I2S3/UART4	SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/I2S6/UART7/USART1/2/3/6	LPUART1/SAI2/SDMMC1/SPDIFRX1/SPI6/I2S6/UART4/5/8	FDCAN1/2/FMC/LCD/OCTOSPIM_P1/2/SDMMC2/SPDIFRX1/TIM13/14	CRS/FMC/LCD/OCTOSPIM_P1/OTG1_FS/OTG1_HS/SAI2/SDMMC2/TIM8	DFSDM1/2/I2C4/LCD/MDIOS/OCTOSPIM_P1/SDMMC2/SWPMI1/TIM1/8/UART7/9/USART10	FMC/LCD/MDIOS/SDMMC1/TIM1/8	COMP/DCMI/PSSI/LCD/TIM1	LCD/UART5	SYS
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH2	-	LPTIM1_IN2	-	-	-	-	-	-	-	OCTOSPIM_P1_IO4	SAI2_SCK_B	-	FMC_SDCKE0	-	LCD_R0	EVENTOUT
	PH3	-	-	-	-	-	-	-	-	-	OCTOSPIM_P1_IO5	SAI2_MCK_B	-	FMC_SDNE0	-	LCD_R1	EVENTOUT
	PH4	-	-	-	-	I2C2_SCL	-	-	-	-	LCD_G5	OTG_HS_ULPI_NXT	-	-	PSSI_D14	LCD_G4	EVENTOUT
	PH5	-	-	-	-	I2C2_SDA	SPI5_SS	-	-	-	-	-	-	FMC_SDNWE	-	-	EVENTOUT
	PH6	-	-	TIM12_CH1	-	I2C2_SMBA	SPI5_SCK	-	-	-	-	-	-	FMC_SDNE1	DCMI_D8/PSSI_D8	-	EVENTOUT
	PH7	-	-	-	-	I2C3_SCL	SPI5_MISO	-	-	-	-	-	-	FMC_SDCKE1	DCMI_D9/PSSI_D9	-	EVENTOUT
	PH8	-	-	TIM5_ETR	-	I2C3_SDA	-	-	-	-	-	-	-	FMC_D16	DCMI_HSYNC/PSSI_DE	LCD_R2	EVENTOUT
	PH9	-	-	TIM12_CH2	-	I2C3_SMBA	-	-	-	-	-	-	-	FMC_D17	DCMI_D0/PSSI_D0	LCD_R3	EVENTOUT
	PH10	-	-	TIM5_CH1	-	I2C4_SMBA	-	-	-	-	-	-	-	FMC_D18	DCMI_D1/PSSI_D1	LCD_R4	EVENTOUT
	PH11	-	-	TIM5_CH2	-	I2C4_SCL	-	-	-	-	-	-	-	FMC_D19	DCMI_D2/PSSI_D2	LCD_R5	EVENTOUT
	PH12	-	-	TIM5_CH3	-	I2C4_SDA	-	-	-	-	-	-	-	FMC_D20	DCMI_D3/PSSI_D3	LCD_R6	EVENTOUT
	PH13	-	-	-	TIM8_CH1N	-	-	-	-	UART4_TX	FDCAN1_TX	-	-	FMC_D21	-	LCD_G2	EVENTOUT
	PH14	-	-	-	TIM8_CH2N	-	-	-	-	UART4_RX	FDCAN1_RX	-	-	FMC_D22	DCMI_D4/PSSI_D4	LCD_G3	EVENTOUT
	PH15	-	-	-	TIM8_CH3N	-	-	-	-	-	-	-	-	FMC_D23	DCMI_D11/PSSI_D11	LCD_G4	EVENTOUT

Table 16. Port I alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	LPTIM1/ TIM1/2/16/17	PDM_SAI1/ TIM3/4/5/12/15	DFSDM1/LPTIM2/3/ LPUART1/ OCTOSPIM_P1/2/TIM8	CEC/DCMI/ PSSI/ DFSDM1/2/ I2C1/2/3/4/ LPTIM2/ TIM15/ USART1	CEC/SPI1/ I2S1/SPI2/ I2S2/SPI3/ I2S3/SPI4/5/ SPI6/I2S6	DFSDM1/2/I2C4/ OCTOSPIM_P1/ SAI1/SPI3/I2S3/ UART4	SDMMC1/ SPI2/I2S2/ SPI3/I2S3/ SPI6/I2S6/ UART7/ USART1/2/3/6	LPUART1/ SAI2/ SDMMC1/ SPDIFRX1/ SPI6/I2S6/ UART4/5/8	FDCAN1/2/FMC/L CD/ OCTOSPIM_P1/2/ SDMMC2/ SPDIFRX1/ TIM13/14	CRS/FMC/LCD/ OCTOSPIM_P1/ OTG1_FS/ OTG1_HS/SAI2/ SDMMC2/TIM8	DFSDM1/2/ I2C4/LCD/MDIOS/ OCTOSPIM_P1/ SDMMC2/SWPMI1/ TIM1/8/UART7/9/ USART10	FMC/LCD/ MDIOS/ SDMMC1/ TIM1/8	COMP/DCMI/ PSSI/LCD/TIM1	LCD/UART5	SYS
Port I	PI0	-	-	TIM5_CH4	-	-	SPI2_SS/ I2S2_WS	-	-	-	-	-	-	FMC_D24	DCMI_D13/ PSSI_D13	LCD_G5	EVENTOUT
	PI1	-	-	-	TIM8_BKIN2	-	SPI2_SCK/ I2S2_CK	-	-	-	-	-	TIM8_BKIN2_COMP12	FMC_D25	DCMI_D8/ PSSI_D8	LCD_G6	EVENTOUT
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO/ I2S2_SDI	-	-	-	-	-	-	FMC_D26	DCMI_D9/ PSSI_D9	LCD_G7	EVENTOUT
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI/ I2S2_SDO	-	-	-	-	-	-	FMC_D27	DCMI_D10/ PSSI_D10	-	EVENTOUT
	PI4	-	-	-	TIM8_BKIN	-	-	-	-	-	-	SAI2_MCK_A	TIM8_BKIN_COMP12	FMC_NBL2	DCMI_D5/ PSSI_D5	LCD_B4	EVENTOUT
	PI5	-	-	-	TIM8_CH1	-	-	-	-	-	-	SAI2_SCK_A	-	FMC_NBL3	DCMI_VSYNC/ PSSI_ RDY	LCD_B5	EVENTOUT
	PI6	-	-	-	TIM8_CH2	-	-	-	-	-	-	SAI2_SD_A	-	FMC_D28	DCMI_D6/ PSSI_D6	LCD_B6	EVENTOUT
	PI7	-	-	-	TIM8_CH3	-	-	-	-	-	-	SAI2_FS_A	-	FMC_D29	DCMI_D7/ PSSI_D7	LCD_B7	EVENTOUT
	PI8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PI9	-	-	-	OCTOSPIM_P2_IO0	-	-	-	-	UART4_RX	FDCAN1_RX	-	-	FMC_D30	-	LCD_ VSYNC	EVENTOUT
	PI10	-	-	-	OCTOSPIM_P2_IO1	-	-	-	-	-	-	-	-	FMC_D31	PSSI_D14	LCD_ HSYNC	EVENTOUT
	PI11	-	-	-	OCTOSPIM_P2_IO2	-	-	-	-	-	LCD_G6	OTG_HS_ ULPI_DIR	-	-	PSSI_D15	-	EVENTOUT
	PI12	-	-	-	OCTOSPIM_P2_IO3	-	-	-	-	-	-	-	-	-	-	LCD_HSYNC	EVENTOUT
	PI13	-	-	-	OCTOSPIM_P2_CLK	-	-	-	-	-	-	-	-	-	-	LCD_VSYNC	EVENTOUT
	PI14	-	-	-	OCTOSPIM_P2_NCLK	-	-	-	-	-	-	-	-	-	-	LCD_CLK	EVENTOUT
	PI15	-	-	-	-	-	-	-	-	-	LCD_G2	-	-	-	-	LCD_R0	EVENTOUT

Table 17. Port J alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	LPTIM1/ TIM1/2/16/17	PDM_SAI1/ TIM3/4/5/12/15	DFSDM1/LPTIM2/3/ LPUART1/ OCTOSPIM_P1/2/ TIM8	CEC/DCMI/ PSSI/ DFSDM1/2/ I2C1/2/3/4/ LPTIM2/ TIM15/ USART1	CEC/SPI1/ I2S1/SPI2/ I2S2/SPI3/ I2S3/SPI4/5/ SPI6/I2S6	DFSDM1/2/I2C4/ OCTOSPIM_P1/ SAI1/SPI3/I2S3/ UART4	SDMMC1/SPI2/ I2S2/SPI3/I2S3/ SPI6/I2S6/ UART7/ USART1/2/3/6	LPUART1/ SAI2/ SDMMC1/ SPDIFRX1/ SPI6/I2S6/ UART4/5/8	FDCAN1/2/FMC/LCD/ OCTOSPIM_P1/2/ SDMMC2/ SPDIFRX1/ TIM13/14	CRS/FMC/LCD/ OCTOSPIM_P1/ OTG1_FS/ OTG1_HS/SAI2/ SDMMC2/TIM8	DFSDM1/2/ I2C4/LCD/MDIOS/ OCTOSPIM_P1/ SDMMC2/ SWPMI1/TIM1/8/ UART7/9/ USART10	FMC/LCD/ MDIOS/ SDMMC1/ TIM1/8	COMP/ DCMI/ PSSI/LC D/TIM1	LCD/ UART5	SYS
Port J	PJ0	-	-	-	-	-	-	-	-	-	LCD_R7	-	-	-	-	LCD_R1	EVENTOUT
Port J	PJ1	-	-	-	OCTOSPIM_P2_IO4	-	-	-	-	-	-	-	-	-	-	LCD_R2	EVENTOUT
Port J	PJ2	-	-	-	OCTOSPIM_P2_IO5	-	-	-	-	-	-	-	-	-	-	LCD_R3	EVENTOUT
Port J	PJ3	-	-	-	-	-	-	-	-	-	-	-	UART9_RTS	-	-	LCD_R4	EVENTOUT
Port J	PJ4	-	-	-	-	-	-	-	-	-	-	-	UART9_CTS	-	-	LCD_R5	EVENTOUT
Port J	PJ5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R6	EVENTOUT
Port J	PJ6	-	-	-	TIM8_CH2	-	-	-	-	-	-	-	-	-	-	LCD_R7	EVENTOUT
Port J	PJ7	TRGIN	-	-	TIM8_CH2N	-	-	-	-	-	-	-	-	-	-	LCD_G0	EVENTOUT
Port J	PJ8	-	TIM1_CH3N	-	TIM8_CH1	-	-	-	-	UART8_TX	-	-	-	-	-	LCD_G1	EVENTOUT
Port J	PJ9	-	TIM1_CH3	-	TIM8_CH1N	-	-	-	-	UART8_RX	-	-	-	-	-	LCD_G2	EVENTOUT
Port J	PJ10	-	TIM1_CH2N	-	TIM8_CH2	-	SPI5_MOSI	-	-	-	-	-	-	-	-	LCD_G3	EVENTOUT
Port J	PJ11	-	TIM1_CH2	-	TIM8_CH2N	-	SPI5_MISO	-	-	-	-	-	-	-	-	LCD_G4	EVENTOUT
Port J	PJ12	TRGOUT	-	-	-	-	-	-	-	-	LCD_G3	-	-	-	-	LCD_B0	EVENTOUT
Port J	PJ13	-	-	-	-	-	-	-	-	-	LCD_B4	-	-	-	-	LCD_B1	EVENTOUT
Port J	PJ14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B2	EVENTOUT
Port J	PJ15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B3	EVENTOUT

Table 18. Port K alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	LPTIM1/ TIM1/2/16/17	PDM_SAI1/ TIM3/4/5/12/15	DFSDM1/LPTIM2/3/ LPUART1/ OCTOSPIM_P1/2/ TIM8	CEC/DCMI/ PSSI/ DFSDM1/2/ I2C1/2/3/4/ LPTIM2/ TIM15/ USART1	CEC/SPI1/ I2S1/SPI2/ I2S2/SPI3/ I2S3/SPI4/5/ SPI6/I2S6	DFSDM1/2/I2C4/ OCTOSPIM_P1/ SAI1/SPI3/I2S3/ UART4	SDMMC1/SPI2/ I2S2/SPI3/I2S3/ SPI6/I2S6/ UART7/ USART1/2/3/6	LPUART1/ SAI2/ SDMMC1/ SPDIFRX1/ SPI6/I2S6/ UART4/5/8	FDCAN1/2/FMC/LCD/ OCTOSPIM_P1/2/ SDMMC2/ SPDIFRX1/ TIM13/14	CRS/FMC/LCD/ OCTOSPIM_P1/ OTG1_FS/OTG1_HS/ SAI2/SDMMC2/TIM8	DFSDM1/2/ I2C4/LCD/MDIOS/ OCTOSPIM_P1/ SDMMC2/SWPMI1/ TIM1/8/UART7/9/ USART10	FMC/LCD/ MDIOS/ SDMMC1/ TIM1/8	COMP/ DCMI/ PSSI/LC D/TIM1	LCD/ UART5	SYS
Port K	PK0	-	TIM1_CH1N	-	TIM8_CH3	-	SPI5_SCK	-	-	-	-	-	-	-	-	LCD_G5	EVENTOUT
Port K	PK1	-	TIM1_CH1	-	TIM8_CH3N	-	SPI5_SS	-	-	-	-	-	-	-	-	LCD_G6	EVENTOUT
Port K	PK2	-	TIM1_BKIN	-	TIM8_BKIN	-	-	-	-	-	-	TIM8_BKIN_COMP12	TIM1_BKIN_COMP12	-	-	LCD_G7	EVENTOUT
Port K	PK3	-	-	-	OCTOSPIM_P2_IO6	-	-	-	-	-	-	-	-	-	-	LCD_B4	EVENTOUT
Port K	PK4	-	-	-	OCTOSPIM_P2_IO7	-	-	-	-	-	-	-	-	-	-	LCD_B5	EVENTOUT
Port K	PK5	-	-	-	OCTOSPIM_P2_NCS	-	-	-	-	-	-	-	-	-	-	LCD_B6	EVENTOUT
Port K	PK6	-	-	-	OCTOSPIM_P2_DQS	-	-	-	-	-	-	-	-	-	-	LCD_B7	EVENTOUT
Port K	PK7	-	-	-		-	-	-	-	-	-	-	-	-	-	LCD_DE	EVENTOUT

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of junction temperature, supply voltage and frequencies by tests in production on 100% of the devices with an junction temperature at T_J = 25 °C and $T_J = T_{Jmax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_J = 25 °C, V_{DD} = 3.3 V (for the 1.62 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure 19. Pin loading conditions.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in Figure 20. Pin input voltage.

Figure 19. **Pin loading conditions**

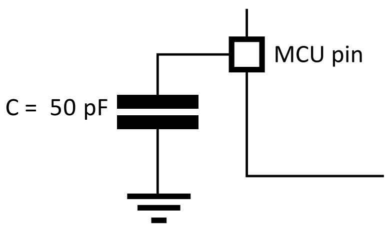
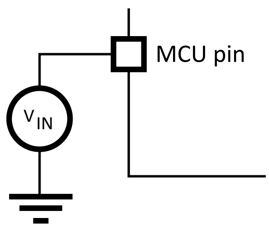
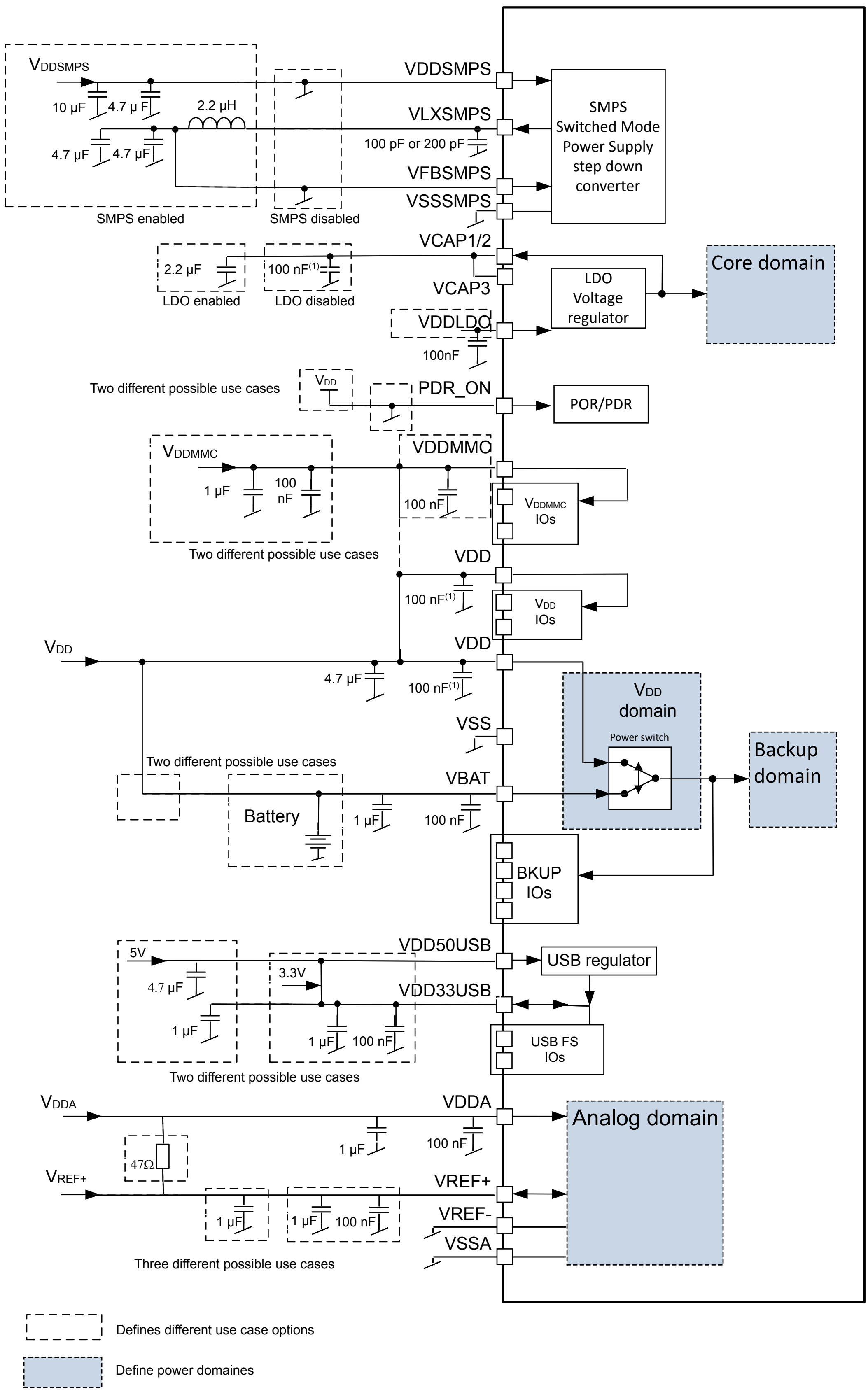


Figure 20. **Pin input voltage**



6.1.6 Power supply scheme

Figure 21. Power supply scheme



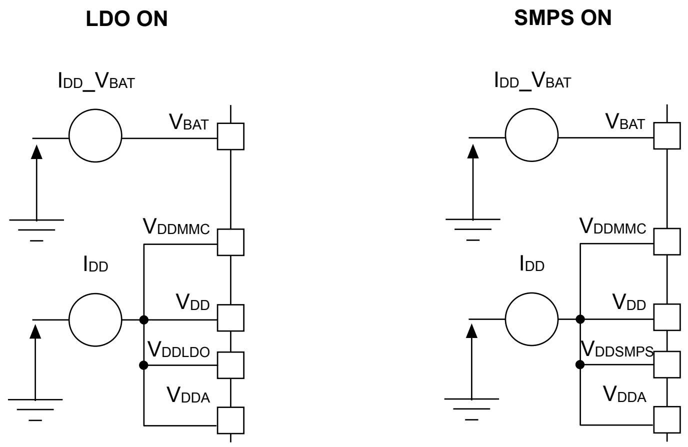
1. 100 nF filtering capacitor on each package pin.
2. A tolerance of +/- 20% is acceptable on decoupling capacitors.

Note: Refer to Getting started with STM32H7A3/7B3 and STM32H7B0 hardware development(AN5307) for more details.

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

6.1.7 Current consumption measurement

Figure 22. **Current consumption measurement scheme**



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 19. Voltage characteristics, Table 20. Current characteristics, and Table 21. Thermal characteristics may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 19. **Voltage characteristics**

All main power (V_{DD}, V_{DDA}, $V_{DD33USB}$, V_{DDMMC}, V_{DDSMPS}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

Symbols	Ratings	Min	Max	Unit
$V_{DDX} - V_{SS}$	External main supply voltage (including V_{DD}, V_{DDLDO}, V_{DDSMPS}, V_{DDA}, $V_{DD33USB}$, V_{DDMMC}, V_{BAT}, V_{REF+})	−0.3	4.0	V
V_{IN} (1)	Input voltage on FT_xxx pins	V_{SS}−0.3	Min(V_{DD}, V_{DDA}, $V_{DD33USB}$, V_{DDMMC}, V_{BAT}) +4.0 (2)(3)	V
	Input voltage on TT_xx pins	V_{SS}−0.3	4.0	V
	Input voltage on BOOT0 pin	V_{SS}	9.0	V
	Input voltage on any other pins	V_{SS}−0.3	4.0	V
$\|\Delta V_{DDX}\|$	Variations between different V_{DDX} power pins of the same domain	-	50	mV

Symbols	Ratings	Min	Max	Unit
$\|V_{SSx}-V_{SS}\|$	Variations between all the different ground pins	-	50	mV

1. *V_{IN} maximum value must always be respected. Refer to Table 64. I/O current injection susceptibility for the maximum allowed injected current values.*
2. *To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.*
3. *This formula has to be applied on power supplies related to the I/O structure described by the pin definition table.*

Table 20. Current characteristics

Symbols	Ratings	Max	Unit
ΣIV_{DD}	Total current into sum of all V_{DD} power lines (source)(1)	620	mA
ΣIV_{SS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	620	
IV_{DD}	Maximum current into each V_{DD} power pin (source)(1)	100	
IV_{SS}	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
I_{IO}	Output current sunk or sourced by any I/O and control pin	20	
	Output current sunk or sourced by Pxy_C pin	1	
$\Sigma I_{(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	140	
	Total output current sourced by sum of all I/Os and control pins(2)	140	
$I_{INJ(PIN)}$(3)(4)	Injected current on FT_xxx, TT_xx, RST and B pins except PA4, PA5	−5/+0	
	Injected current on PA4, PA5	−0/0	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/Os and control pins)(5)	±25	

1. *All main power (V_{DD}, V_{DDA}, V_{DDSMPS}, V_{DDLDO}, $V_{DD33USB}$, V_{DDMMC}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.*
2. *This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.*
3. *A positive injection is induced by V_{IN}>V_{DD} while a negative injection is induced by V_{IN}<V_{SS}. $I_{INJ(PIN)}$ must never be exceeded. Refer also to Table 19. Voltage characteristics for the maximum allowed input voltage values.*
4. *Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.*
5. *When several inputs are submitted to a current injection, the maximum $\sum I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).*

Table 21. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	−65 to +150	°C
T_{Jmax}	Maximum junction temperature	130(1)	

1. *The junction temperature is limited to 105 °C in the VOS0 voltage range.*

6.3 Operating conditions

6.3.1 General operating conditions

Table 22. General operating conditions

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
V_{DD}	Standard operating voltage	-	1.62(1)	-	3.6	V
V_{DDLDO}	Supply voltage for the internal regulator	VDDLDO ≤ VDD	1.62(1)	-	3.6	
			1.2(2)	-	3.6	
V_{DDSMPS}	Supply voltage for the internal SMPS Step-down converter	VDDSMPS = VDD	1.62(1)	-	3.6	
V_{DDMMC}	Standard operating voltage for independent MMC I/Os	Indenpent MMC I/Os used	1.62(1)	-	3.6	
		Independent MMC I/Os not used V_{DDMMC} = V_{DD}	1.62(1)	-	3.6	
$V_{DD33USB}$	Standard operating voltage, USB domain	USB used	3.0	-	3.6	
		USB not used	0	-	3.6	
V_{DDA}	Analog operating voltage	ADC or COMP used	1.62	-	3.6	
		DAC used	1.8	-		
		OPAMP used	2.0	-		
		VREFBUF used	1.8	-		
		ADC, DAC, OPAMP, COMP, VREFBUF not used	0	-		
V_{BAT}	Backup operating voltage	-	1.2	-	3.6	
V_{IN}	I/O Input voltage	TT_xx I/O	−0.3	-	V_{DD}+0.3	
		BOOT0	0	-	9	
		All I/O except BOOT0 and TT_xx	−0.3	-	Min(V_{DD}, V_{DDA}, $V_{DD33USB}$, V_{DDMMC}) +3.6 V < 5.5 V(3)	
V_{CORE}	Internal regulator ON (LDO or SMPS)(4)	VOS3 (max frequency 88 MHz)	0.95	1.0	1.05	
		VOS2 (max frequency 160 MHz)	1.05	1.10	1.15	
		VOS1 (max frequency 225 MHz)	1.15	1.20	1.25	
		VOS0 (max frequency 280 MHz)	1.25	1.30	1.35	
	Regulator OFF: external V_{CORE} voltage must be supplied from external regulator on VCAP pins	VOS3 (max frquency 88 MHz)	0.97	1.0	1.05	
		VOS2 (max frequency 160 MHz)	1.07	1.10	1.15	
		VOS1 (max frequency 225 MHz)	1.17	1.20	1.25	

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
V_{CORE}	Regulator OFF: external V_{CORE} voltage must be supplied from external regulator on VCAP pins	VOS0 (max frequency 280 MHz)	1.27	1.30	1.33	V
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation	–40	-	85	°C
		Low-power dissipation(5)	–40	-	105	
T_J	Junction temperature range	VOS0	–40	-	105	°C
		VOS3, VOS2, VOS1	–40	-	130	

1. *When a reset occurs, the functionality is guaranteed down to V_{PDRmax} or to the specified V_{DDmin} when the PDR is OFF. The PDR can only be switched OFF though the PDR_ON pin that is not available in all packages (refer to Table 7. STM32H7A3xI/G pin/ball definition)*
2. *Only for power-up sequence when the SMPS step-down converter is configured to supply the LDO.*
3. *This formula has to be applied on power supplies related to the I/O structures described by the pin definition table.*
4. *At startup, the external V_{CORE} voltage must remain higher or equal to 1.10 V before disabling the internal regulator (LDO).*
5. *In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see Section 7.11 Thermal characteristics).*

Table 23. Maximum allowed clock frequencies

Symbol (1)(2)	Parameter	VOS0	VOS1	VOS2	VOS3	Unit
f_{CPU}	CPU	280	225	160	88	MHz
f_{ACLK}	AXI	280	225	160	88	
f_{HCLK}	AHB	280	225	160	88	
f_{PCLK}	APB	140	112.5	80	44	
$f_{ltdc\_ker\_ck}$	LTDC	140	112.5	80	44	
$f_{fmc\_ker\_ck}$	FMC	280	225	160	88	
$f_{octospi\_ker\_clk}$	OCTOSPI1/2	280	225	160	88	
$f_{sdmmc\_ker\_ck}$	SDMMC1/2	280	225	160	88	
f_{DFSDM1_Aclk}	DFSDM1	140	112.5	80	44	
f_{DFSDM1_Clk}		140	112.5	80	44	
f_{DFSDM2_Aclk}	DFSDM2	140	112.5	80	44	
f_{DFSDM2_Clk}		140	112.5	80	44	
$f_{fdcan\_ker\_ck}$	FDCAN	140	112.5	80	44	
$f_{cec\_ker\_ck}$	HDMI_CEC	66	66	66	44	
$f_{I2C\_ker\_ck}$	I2C[1:4]	140	112.5	80	44	
$f_{lptim\_ker\_ck}$	LPTIM[1:3]	140	112.5	80	44	
$f_{rcc\_tim\_ker\_ck}$	TIM[2:7],TIM[12:14]	280	225	160	88	
$f_{rcc\_tim\_ker\_ck}$	PWM1,PWM8,TIM[15:17]	280	225	160	88	
f_{rng_clk}	RNG	140	112.5	80	44	
$f_{sai\_a\_ker\_ck}$	SAI1	150	150	80	80	
$f_{sai\_b\_ker\_ck}$						
$f_{sai\_a\_ker\_ck}$	SAI2	150	150	80	80	
$f_{sai\_b\_ker\_ck}$						

Symbol (1)(2)	Parameter	VOS0	VOS1	VOS2	VOS3	Unit
$f_{spdifrx\_ker\_ck}$	SPDIFRX1	280	225	160	88	MHz
$f_{spi\_ker\_ck}$	SPI[1:6]	280	225	160	88	
$f_{lpuart\_ker\_ck}$	LPUART1	140	112.5	80	44	
$f_{usart\_ker\_ck}$	USART1/2/3/6/10	280	225	160	88	
$f_{uart\_ker\_ck}$	UART4/5/7/8/9	280	225	160	88	
f_{adp_clk}	USBOTG	48	48	48	48	
f_{ulpi_ck}	USB1ULPI	66	66	66	66	
$f_{adc\_ker\_ck}$	ADC1/2	50	50	50	50	
f_{dac_pclk}	DAC1/2	140	112.5	80	44	
$f_{rtc\_ker\_ck}$	RTC	1	1	1	1	

1. *Guaranteed by design.*
2. *The maximum kernel clock frequencies can be limited by the maximum peripheral clock frequency (refer each peripheral electrical characteristics).*

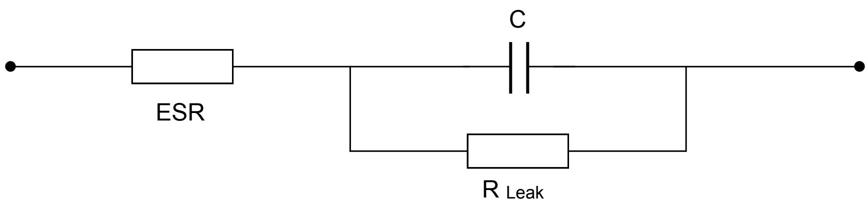
Table 24. Supply voltage and maximum frequency configuration

Power scale	V_{CORE} source	Max T_J (°C)	Max frequency (MHz)	Min V_{DD} (V)
VOS0	LDO/SMPS	105	280	1.71
VOS1	LDO/SMPS	130	225	1.62
VOS2	LDO/SMPS	130	160	1.62
VOS3	LDO/SMPS	130	88	1.62
SVOS4	LDO/SMPS	130	N/A	1.62
SVOS5	LDO/SMPS	130	N/A	1.62

6.3.2 VCAP external capacitor

Stabilization for the embedded LDO regulator is achieved by connecting an external capacitor C_{EXT} to the VCAPx pin. C_{EXT} is specified in Table 25. VCAP operating conditions. Two external capacitors must be connected to VCAP pins (refer to *Getting started with STM32H7A3/7B3 and STM32H7B0 hardware development* (AN5307).

Figure 23. **External capacitor C_{EXT}**



1. Legend: ESR is the equivalent series resistance.

Table 25. **VCAP operating conditions**

When the internal LDO voltage regulator is switched OFF, the two 2.2 µF VCAP capacitors are not required. However all VCAPx package pins must be connected together and it is recommended to add a ceramic filtering capacitor of 100 nF as close as possible to each VCAPx pin.

Symbol	Parameter	Conditions
CEXT	External capacitor for LDO enabled	2.2 µF(1)(2)
ESR	ESR of external capacitor	< 100 mΩ

1. *This value corresponds to CEXT typical value. A variation of ±20% is tolerated.*
2. *If the VCAP3 pin is available (depending on the package), it must be connected to the other VCAP pins. No additional capacitor is required.*

6.3.3 SMPS step-down converter

The devices embed a high power efficiency SMPS step-down converter requiring external components. Refer to *Getting started with STM32H7A3/7B3 and STM32H7B0 hardware development* (AN5307) for the required components and tradeoffs.

Table 26. **Characteristics of SMPS step-down converter external components**

Symbol	Parameter	Conditions
C_{IN}	Capacitance of external capacitor on VDDSMPS	4.7 µF
	ESR of external capacitor	100 mΩ
C_{filt}	Capacitance of external capacitor on VLXSMPS pin	220 pF
C_{OUT}	Capacitance of external capacitor on VFBSMPS pin	10 µF
	ESR of external capacitor	20 mΩ
L	Inductance of external Inductor on VLXSMPS pin	2.2 µH
-	Serial DC resistor	150 mΩ
I_{SAT}	DC current at which the inductance drops 30% from its value without current.	1.7 A
I_{RMS}	Average current for a 40 °C rise: rated current for which the temperature of the inductor is raised 40°C by DC current	1.4 A

Table 27. SMPS step-down converter characteristics for external usage

Symbol	Conditions	Min	Typ	Max	Unit
V_{DDSMPS}[(1)]	V_{OUT} = 1.8 V	2.3	-	3.6	V
	V_{OUT} = 2.5 V	3	-	3.6	
V_{OUT}[(2)]	I_{OUT}=600 mA	2.25	2.5	2.75	V
		1.62	1.8	1.98	
I_{OUT}	internal and external usage	-	-	600	mA
	External usage only[(3)]	-	-	600	
RDS_{ON}	-	-	100	120	mΩ
IDD_{SMPS_Q}	Quiescent current	-	220	-	µA
T_{SMPS_START}	V_{OUT} = 1.8 V	-	270	405	µs
	V_{OUT} = 2.5 V	-	360	540	

1. *The switching frequency is 2.4 MHz±10%*
2. *Including line transient and load transient.*
3. *These characteristics are given for SMPSEXTHP bit is set in the PWR_CR3 register.*

The SMPS current consumption can be determined using the following formula based on the maximum LDO current consumption provided in Section 6.3.7 Supply current characteristics:

$$I_{DDSMPS} = I_{DDLDO} \times (V_{CORE} \div (V_{DD} \times efficency))$$

where

I_{DDLDO} is the current in LDO configuration given in the following tables

V_{CORE} is the digital core supply (V_{CAP})

Efficiency is defined in the following curves.

Figure 24. SMPS efficicency vs load current in Run, Sleep and Stop mode with SVOS3 MR mode, T_J = 30 °C

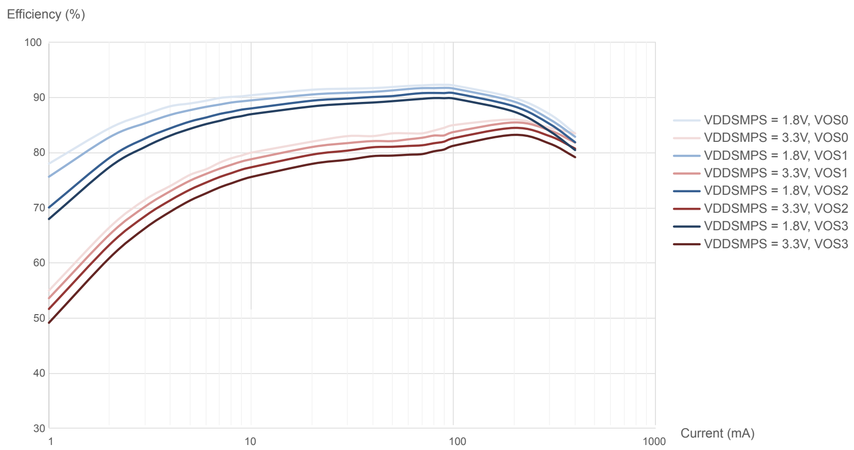


Figure 25. SMPS efficiency vs load current in Run, Sleep and Stop mode with SVOS3 MR mode, T_J = 130 °C

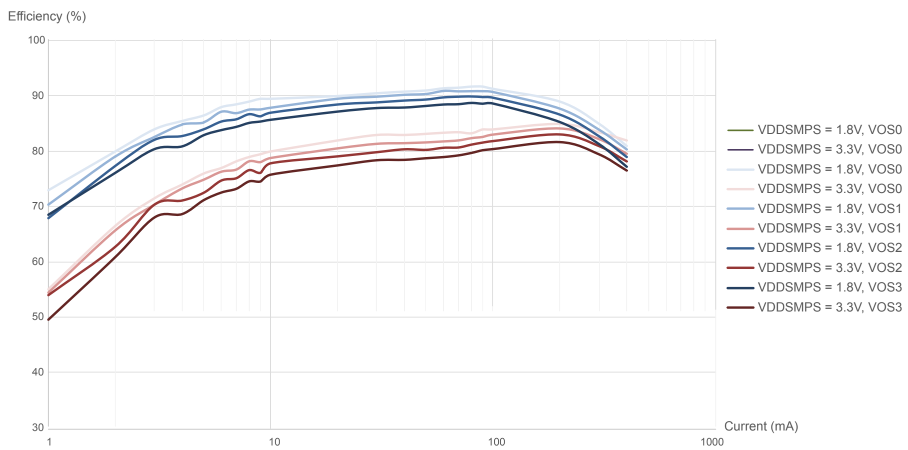


Figure 26. SMPS efficiency vs load current in Stop and DStop modes (SVOS3 LP mode, SVOS4, SVOS5), T_J = 30 °C

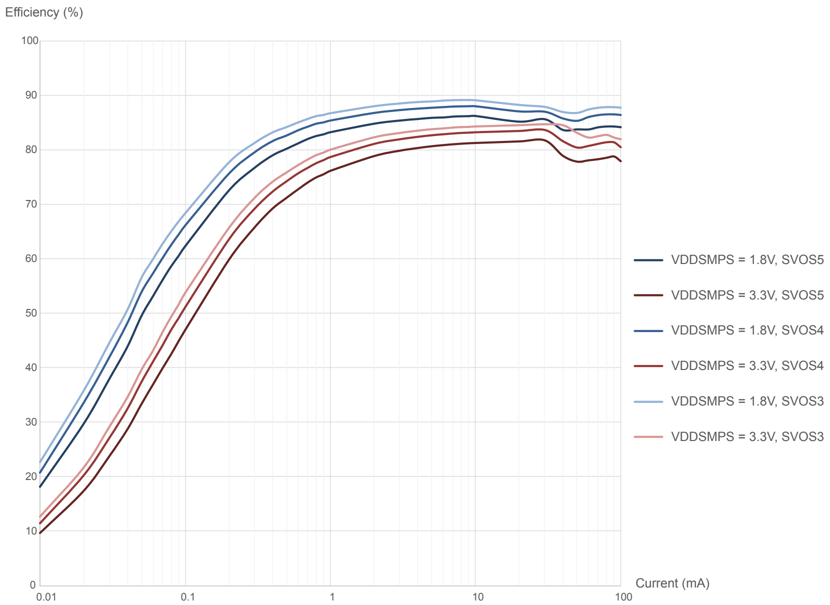


Figure 27. SMPS efficiency vs load current in Stop and DStop modes (SVOS3 LP mode, SVOS4, SVOS5), T_J = 130 °C

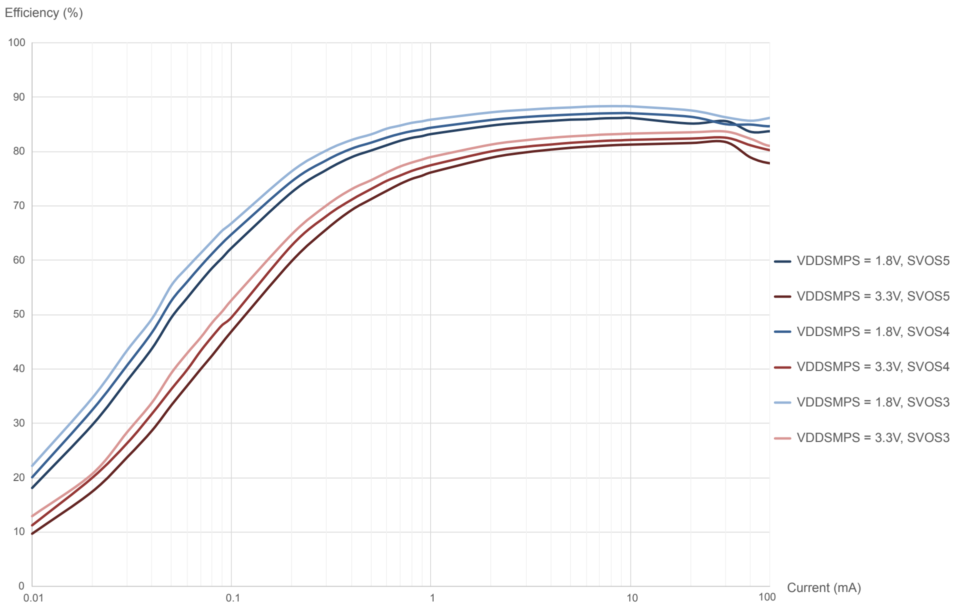


Figure 28. SMPS efficiency vs load current in Stop and DStop2 modes (SVOS3 LP mode, SVOS4, SVOS5), T_J = 30 °C

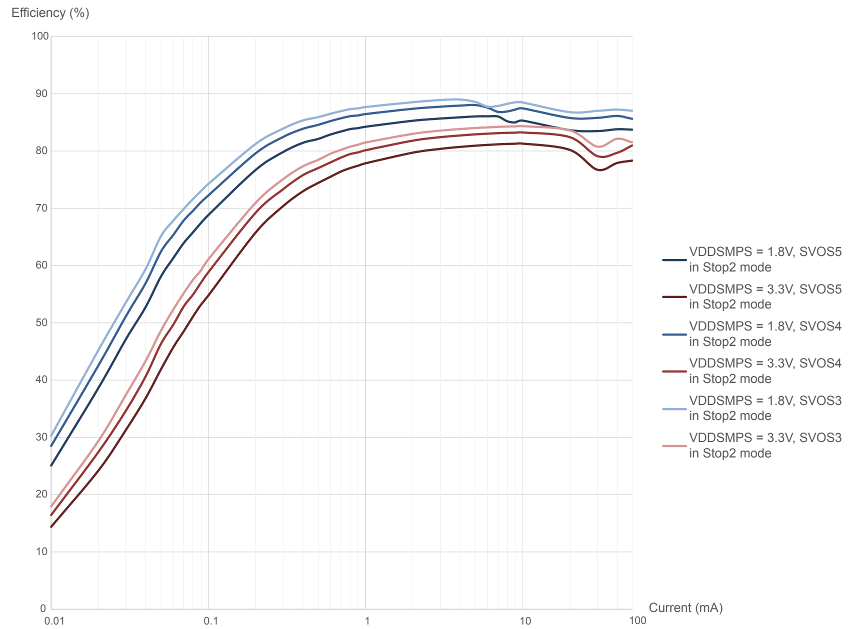
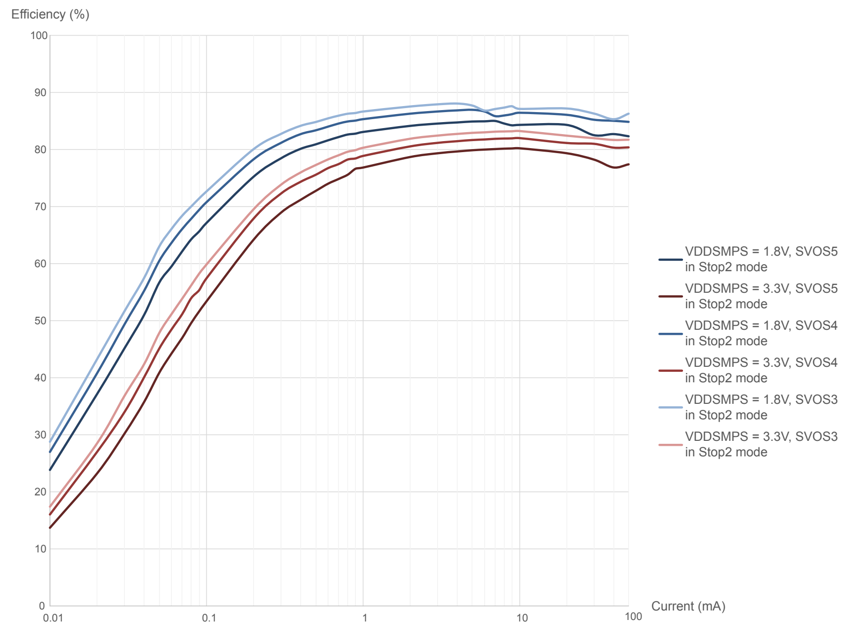


Figure 29. SMPS efficiency vs load current in Stop and DStop2 modes (SVOS3 LP mode, SVOS4, SVOS5), T_J = 130 °C



6.3.4 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Operating conditions at power-up / power-down (regulator ON)

Table 28. Operating conditions at power-up / power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	0	∞	µs/V
	V_{DD} fall time rate	10	∞	
t_{VDDA}	V_{DDA} rise time rate	0	∞	
	V_{DDA} fall time rate	10	∞	
t_{VDDUSB}	V_{DDUSB} rise time rate	0	∞	
	V_{DDUSB} fall time rate	10	∞	
VDDMMC	V_{DDMMC} rise time rate	0	∞	
	V_{DDMMC} fall time rate	10	∞	

6.3.5 Embedded reset and power control block characteristics

The parameters given in Table 29. Reset and power control block characteristics are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 22. General operating conditions.

Table 29. Reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$[(1)]	Reset temporization after POR released	-	-	377	550	µs
$V_{POR/PDR}$	Power-on/power-down reset threshold	Rising edge[(1)]	1.62	1.67	1.71	V
		Falling edge	1.58	1.62	1.68	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.04	2.10	2.15	
		Falling edge	1.95	2.00	2.06	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.34	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.63	2.70	2.78	
		Falling edge	2.54	2.61	2.68	
V_{PVD0}	Programmable Voltage Detector threshold 0	Rising edge	1.90	1.96	2.01	
		Falling edge	1.81	1.86	1.91	
V_{PVD1}	Programmable Voltage Detector threshold 1	Rising edge	2.05	2.10	2.16	
		Falling edge	1.96	2.01	2.06	
V_{PVD2}	Programmable Voltage Detector threshold 2	Rising edge	2.19	2.26	2.32	
		Falling edge	2.10	2.15	2.21	
V_{PVD3}	Programmable Voltage Detector threshold 3	Rising edge	2.35	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{PVD4}	Programmable Voltage Detector threshold 4	Rising edge	2.49	2.56	2.62	
		Falling edge	2.39	2.45	2.51	
V_{PVD5}	Programmable Voltage Detector threshold 5	Rising edge	2.64	2.71	2.78	
		Falling edge	2.55	2.61	2.68	
V_{PVD6}	Programmable Voltage Detector threshold 6	Rising edge	2.78	2.86	2.94	
		Falling edge in Run mode	2.69	2.76	2.83	
$V_{POR/PDR}$	Hysteresis for power-on/power-down reset	Hysteresis in Run mode	-	43	-	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{hyst\_BOR\_PVD}$	Hysteresis voltage of BOR	Hysteresis in Run mode	-	100	-	mV
$I_{DD\_BOR\_PVD}$(1)	BOR and PVD consumption from V_{DD}	-	-	-	0.630	µA
$I_{DD\_POR\_PDR}$	POR and PDR consumption from V_{DD}	-	0.8	-	1.2	
V_{AVM_0}	Analog voltage detector for VDDA threshold 0	Rising edge	1.66	1.71	1.76	V
		Falling edge	1.56	1.61	1.66	
V_{AVM_1}	Analog voltage detector for VDDA threshold 1	Rising edge	2.06	2.12	2.19	
		Falling edge	1.96	2.02	2.08	
V_{AVM_2}	Analog voltage detector for VDDA threshold 2	Rising edge	2.42	2.50	2.58	
		Falling edge	2.35	2.42	2.49	
V_{AVM_3}	Analog voltage detector for VDDA threshold 3	Rising edge	2.74	2.83	2.91	
		Falling edge	2.64	2.72	2.80	
V_{hyst_VDDA}	Hysteresis of VDDA voltage detector	-	-	100	-	mV
I_{DD_PVM}	PVM consumption from VDD(1)	-	-	-	0.25	µA
I_{DD_VDDA}	Voltage detector consumption on VDDA(1)	Resistor bridge	-	-	2.5	µA

1. *Guaranteed by design.*

6.3.6 Embedded reference voltage

The parameters given in Table 30 are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 22. General operating conditions.

Table 30. Embedded reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}(1)	Internal reference voltages	-40 °C < T_J < 130 °C	1.180	1.216	1.255	V
$t_{S\_vrefint}$(2)(3)	ADC sampling time when reading the internal reference voltage	-	4.3	-	-	µs
t_{S_vbat}(3)	V_{BAT} sampling time when reading the internal V_{BAT} reference voltage	-	9	-	-	
$t_{start\_vrefint}$(3)	Start time of reference voltage buffer when ADC is enable	-	-	-	4.4	µs
Irefbuf(3)	Reference Buffer consumption for ADC	V_{DD} = 3.3 V	9	13.5	23	µA
ΔVREFINT(3)	Internal reference voltage spread over the temperature range	-40 °C < T_J < 130 °C	-	5	15	mV
T_{coeff}	Average temperature coefficient	Average temperature coefficient	-	20	70	ppm/°C
$V_{DDcoeff}$	Average Voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	10	1370	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	-	25	-	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage	-	-	50	-	
V_{REFINT_DIV3}	3/4 reference voltage	-	-	75	-	

1. *Guaranteed by design and tested in production at 3.3 V*
2. *The shortest sampling time for the application can be determined by multiple iterations.*
3. *Guaranteed by design.*

Table 31. **Internal reference voltage calibration values**

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 °C, $_{VDDA}$ = 3.3 V	08FFF810 - 08FFF812

Table 32. **USB regulator characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD50USB}$	Supply voltage	-	4	5	5,5	V
$I_{DD50USB}$	Current consumption	-	-	13.5	-	µA
$V_{REGOUTV33V}$	Regulated output voltage	-	3	-	3.6	V
I_{OUT}	Output current load sinked by USB block	-	-	-	20	mA
T_{WKUP}	Wakeup time	-	-	120	170	µs

6.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in Figure 22. Current consumption measurement scheme.

All the run-mode current consumption measurements given in this section are performed with a CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode.
- All peripherals are disabled except when explicitly mentioned.
- The flash memory access time is adjusted with the minimum wait states number, depending on the f_{ACLK} frequency (refer to the table "Number of wait states according to CPU clock ($f_{rcc\_cpu\_ck}$) frequency and V_{CORE} range" available in the reference manual).
- When the peripherals are enabled, the AHB clock frequency is the CPU frequency divided by 2 and the APB clock frequency is AHB clock frequency divided by 2.

The parameters given in the below tables are derived from tests performed under the supply voltage conditions summarized in Table 22. General operating conditions and unless otherwise specified at ambient temperature.

The maximum current consumptions provided in the following tables are given for LDO regulator ON. To obtain the maximum SMPS current consumption, the efficiency curves can be used with the maximum LDO current consumption as entry value (refer to Section 6.3.3 SMPS step-down converter).

Table 33. Inrush current and inrush electric charge characteristics for LDO and SMPS

1. The typical values are given for V_{DDLDO} = V_{DDSMPS} = 3.3 V and for typical decoupling capacitor values of C_{EXT} and C_{OUT}.
2. The product consumption on V_{DDCORE} is not taken into account in the inrush current and inrush electric charge.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{RUSH}	Inrush current on voltage regulator power-on (POR or wakeup from Standby)	on V_{DDLDO}[1]		-	55	96 [2]	mA
		on V_{DDSMPS}[3]	SMPS supplies the V_{DDCORE}	-	25	92[4]	
	Inrush current on voltage regulator power-on (POR)	on V_{DDSMPS}[3]	SMPS supplies internal LDO V_{OUT} = 1.8 V[5]	-	45	135[4]	
			SMPS supplies internal LDO V_{OUT} = 2.5 V[5]	-		100[4]	
			SMPS supplies external circuit V_{OUT} = 1.8 V[5]	-	25	70[4]	
			SMPS supplies external circuit V_{OUT} = 2.5 V[5]	-		50[4]	
	Inrush current on voltage regulator power-on (wakeup from Standby)	on V_{DDSMPS}[3]	SMPS supplies internal LDO V_{OUT} = 1.8 V	-	70	200[4]	
			SMPS supplies internal LDO V_{OUT} = 2.5 V	-	95	210[4]	
Q_{RUSH}	Inrush current on voltage regulator power-on (POR or wakeup from Standby)	on V_{DDLDO}[1]		-	4.4	5.3[2]	µC
		on V_{DDSMPS}[3]	SMPS supplies the V_{DDCORE}	-	2.9	7[2]	
	Inrush current on voltage regulator power-on (POR)	on V_{DDSMPS}[3]	SMPS supplies internal LDO V_{OUT} = 1.8 V[5]	-	4.0	7.5[2]	
			SMPS supplies internal LDO V_{OUT} = 2.5 V[5]	-		5.7[2]	
			SMPS supplies external circuit VOUT = 1.8 V[5]	-	2.9	5.2[2]	
			SMPS supplies external circuit V_{OUT} = 2.5 V[5]	-		4[2]	
	Inrush current on voltage regulator power-on (wakeup from Standby)	on V_{DDSMPS}[3]	SMPS supplies internal LDO V_{OUT} = 1.8 V	-	8.0	15[2]	
			SMPS supplies internal LDO V_{OUT} = 2.5 V	-	14.5	20.5[2]	

1. *The inrush current and inrush electric charge on V_{DDLDO} are not present in Bypass mode or when the SMPS supplies V_{DDCORE}.*
2. *The maximum value is given for the maximum decoupling capacitor C_{EXT}.*
3. *The inrush current and inrush electric charge on V_{DDSMPS} is not present if the external component (L or C_{OUT}) is not present, that is if the SMPS is not used.*
4. *The maximum value is given for the maximum decoupling capacitor C_{OUT} and the minimum V_{DDSMPS} voltage.*
5. *The inrush current and inrush electric charge due to the transition from 1.2 V to the final V_{OUT} value (1.8 V or 2.5 V) is not taken into account.*

Table 34. Typical and maximum current consumption in Run mode, code with data processing running from ITCM, regulator ON

Data are in DTCM for best computation performance. In this case, the cache has no influence on consumption.

Symbol	Parameter	Conditions		$f_{rcc\_cpu\_ck}$ (MHz)	Typ LDO	Typ SMPS	Max(1)(2) T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 130 °C	unit
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS0	280	69.5	34.0	77	106	128	173	mA
				225	56.5	27.5	64	92	114	159	
			VOS1	225	52.0	24.0	58	80	98	136	
				200	46.5	21.0	52	75	93	130	
				180	42	19.0	47	70	88	125	
				168	39	18.0	45	67	85	122	
				160	37.5	17.0	43	65	83	120	
			VOS2	160	34.0	14.5	38	56	70	101	
				144	30.5	13.0	35	52	67	97	
				88	19.0	8.5	23	41	55	85	
			VOS3	88	18.0	7.5	21	35	46	71	
				60	12.5	5.5	16	29	41	66	
				25	6.0	3.0	9	23	34	59	
		All peripherals enabled	VOS0	280	133.5	63.5	142	173	196	242	
				225	108.0	51.5	115	146	168	214	
			VOS1	225	99.0	45.0	105	129	147	185	
				160	71.5	32.5	77	100	118	156	
			VOS2	160	65.0	27.5	69	87	102	132	
				88	41.5	17.5	45	63	77	108	
			VOS3	88	38.0	15.0	41	55	66	91	

1. *Guaranteed by characterization results, unless otherwise specified.*
2. *The maximum values are given for LDO regulator ON. Refer to Section 6.3.3 SMPS step-down converter for the SMPS maximum current consumption.*

Table 35. **Typical and maximum current consumption in Run mode, code with data processing running from flash memory, cache ON**

Symbol	Parameter	Conditions		$f_{rcc\_cpu\_ck}$ (MHz)	Typ LDO[1]	Typ SMPS[1]	Max[1][2]				unit
							T_J = 25 °C	T_J= 85 °C	T_J = 105 °C	T_J = 130 °C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS0	280	69.0	33.5	77	106	128	173	mA
				225	56.0	27.0	64	92	114	158	
			VOS1	225	51.5	23.5	58	80	98	136	
				200	46.5	21.5	52	75	92	129	
				180	42.0	19.0	47	70	88	125	
				168	39.0	18.0	45	67	85	122	
				160	37.5	17.0	43	65	83	120	
			VOS2	160	34.0	14.5	38	56	70	101	
				144	30.5	13.0	35	53	67	97	
				88	19.0	8.5	23	41	55	85	
			VOS3	88	17.5	7.5	21	35	46	71	
				60	12.5	5.0	16	29	41	66	
				25	6.0	2.5	9	23	34	59	
		All peripherals enabled	VOS0	280	132.5	63.5	142	173	195	241	
				225	107.5	51.0	115	145	168	213	
			VOS1	225	99.0	44.5	105	129	147	185	
				160	71.5	32.5	77	100	118	155	
			VOS2	160	65.0	27.5	69	87	102	132	
				88	41.5	17.5	45	63	77	108	
			VOS3	88	38.0	15.0	41	55	66	91	

1. *Guaranteed by characterization results, unless otherwise specified.*
2. *The maximum values are given for LDO regulator ON. Refer to Section 6.3.3 SMPS step-down converter for the SMPS maximum current consumption.*

Table 36. **Typical and maximum current consumption in Run mode, code with data processing running from flash memory, cache OFF**

Symbol	Parameter	Conditions		$f_{rcc\_cpu\_ck}$ (MHz)	Typ LDO[1]	Typ SMPS[1]	Max[1][2]				Unit
							T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 130 °C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS0	280	56.0	28.0	63	91	113	157	mA
				225	47.0	23.5	54	82	103	148	
			VOS1	225	43.0	21.0	49	71	89	126	
				160	34.0	16.5	39	62	79	116	
			VOS2	160	29.5	13.5	34.	51	65	96	
				88	18.5	9.0	23	40	54	84	
			VOS3	88	16.5	7.5	19	33	44	69	
		All peripherals enabled	VOS0	280	119.5	58.0	127	157	180	225	
				225	98.5	48.0	105	135	157	203	
			VOS1	225	90.5	42.0	96	120	138	176	

Symbol	Parameter	Conditions		$f_{rcc\_cpu\_ck}$ (MHz)	Typ LDO[1]	Typ SMPS[1]	Max[1][2]				Unit
							T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 130 °C	
I_{DD}	Supply current in Run mode	All peripherals enabled	VOS1	160	68.0	32.0	73	96	114	152	mA
			VOS2	160	60.5	26.5	64	82	97	127	
				88	41.0	18.0	45	62	77	107	
			VOS3	88	36.5	15.0	39	53	64	89	

1. *Guaranteed by characterization results, unless otherwise specified.*
2. *The maximum values are given for LDO regulator ON. Refer to Section 6.3.3 SMPS step-down converter for the SMPS maximum current consumption.*

Table 37. Typical consumption in Run mode and corresponding performance versus code position

Symbol	Parameter	Conditions		$f_{rcc\_cpu\_ck}$ (MHz)	Coremark	Typ LDO	Typ SMPS	Unit	LDO I_{DD}/ Coremark	SMPS I_{DD}/ Coremark	Unit
		Peripheral	Code								
I_{DD}	Supply current in Run mode	All peripherals disabled, cache ON	ITCM	280	1414	69.5	33.8	mA	49.2	23.9	µA/ Coremark
			FLASH	280	1414	69.0	33.4		48.8	23.6	
			AXI SRAM	280	1414	69.5	33.6		49.2	23.8	
			AHB SRAM	280	1414	70.0	33.7		49.5	23.8	
			SRD SRAM	280	1414	70.0	33.7		49.5	23.8	
		All peripherals disabled cache OFF	ITCM	280	1414	69.5	33.8		49.2	23.9	
			FLASH	280	668	56.0	28.0		83.8	41.9	
			AXI SRAM	280	668	62.5	30.2		93.6	45.2	
			AHB SRAM	280	295	59.5	28.8		201.7	97.6	
			SRD SRAM	280	295	59.0	28.5		200.0	96.6	

Table 38. Typical current consumption in Autonomous mode

Symbol	Parameter	Conditions[1]		f_{rcc_hclk4} (AHB4) (MHz)	Typ	Unit
I_{DD}	Supply current in Autonomous mode	Run, DStop mode	VOS3	64	2.98	mA
		Run, DStop2 mode	VOS3	64	2.64	

1. *System in Run mode, CPU domain is DStop or DStop2 mode with memories of the CPU domain shut-off enable or disable.*

Table 39. **Typical current consumption in Sleep mode, regulator ON**

Symbol	Parameter	Conditions		$f_{rcc\_cpu\_ck}$ (MHz)	Typ LDO	Typ SMPS	Max(1)(2)				Unit
							T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J= 130 °C	
$I_{DD(Sleep)}$	Supply current in Sleep mode	All peripherals disabled	VOS0	280	18.1	13.0	23	51	72	115	mA
				225	15.0	10.6	20	47	68	112	
			VOS1	225	13.7	9.3	18	40	57	93	
				160	10.3	6.8	14	36	53	90	
			VOS2	160	9.3	5.8	12	30	44	74	
				88	5.8	3.6	9	26	40	70	
			VOS3	88	5.2	3.0	8	21	32	57	

1. *Guaranteed by characterization results.*
2. *The maximum values are given for LDO regulator ON. Refer to Section 6.3.3 SMPS step-down converterfor the SMPS maximum current consumption.*

Table 40. **Typical current consumption in System Stop mode**

Symbol	Parameter	Conditions		Typ LDO	Typ SMPS	Max(1)(2)				Unit
						T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J= 130 °C	
$I_{DD(Stop)}$	Stop, DStop	Flash memory in low- power mode, memory shut-off disable	SVOS3 Main(3)	0.540	0.487	2.33	14.36	24.52	46.29	mA
			SVOS3 LP	0.495	0.193	2.27	14.21	24.28	45.94	
			SVOS4	0.370	0.137	1.59	10.58	18.52	35.90	
			SVOS5	0.245	0.090	0.98	7.18	13.10	26.61	
		Flash memory in normal mode, memory shut-off disable	SVOS3 Main(3)	0.560	0.504	2.39	14.62	24.93	47.01	
			SVOS3 LP	0.515	0.209	2.33	14.47	24.69	46.65	
			SVOS4	0.390	0.153	1.65	10.84	18.93	36.62	
			SVOS5	0.245	0.090	1.04	7.43	13.51	27.32	
		Flash memory in low- power mode, memory shut-off enable	SVOS3 Main(3)	0.530	0.481	2.31	14.23	24.27	45.71	
			SVOS3 LP	0.480	0.186	2.25	14.09	24.04	45.36	
			SVOS4	0.360	0.134	1.57	10.49	18.32	35.41	
			SVOS5	0.230	0.085	0.96	6.95	12.59	25.26	
		Flash memory in normal mode, memory shut-off enable	SVOS3 Main(3)	0.550	0.498	2.37	14.50	24.68	46.43	
			SVOS3 LP	0.500	0.204	2.31	14.35	24.45	46.07	
			SVOS4	0.380	0.151	1.63	10.75	18.73	36.13	
			SVOS5	0.230	0.085	1.02	7.21	13.00	25.97	
	Stop, DStop2	Flash memory in low- power mode, memory shut-off disable	SVOS3 Main(3)	0.161	0.343	0.32	1.67	2.86	5.58	
			SVOS3 LP	0.115	0.046	0.28	1.62	2.80	5.50	
			SVOS4	0.095	0.037	0.20	1.23	2.19	4.43	
			SVOS5	0.090	0.032	0.14	0.93	1.75	3.80	

Symbol	Parameter	Conditions		Typ LDO	Typ SMPS	Max[1][2]				Unit
						T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J= 130 °C	
$I_{DD(Stop)}$	Stop, DStop2	Flash memory in low -power mode, memory shut-off enable	SVOS3 Main[3]	0.146	0.337	0.30	1.55	2.63	5.04	mA
			SVOS3 LP	0.100	0.040	0.26	1.51	2.58	4.96	
			SVOS4	0.085	0.033	0.19	1.15	2.01	3.98	
			SVOS5	0.075	0.028	0.12	0.80	1.46	3.02	

1. *Guaranteed by characterization results.*
2. *The maximum values are given for LDO regulator ON. Refer to Section 6.3.3 SMPS step-down converterfor the SMPS maximum current consumption.*
3. *The SMPS is unnecessarily ON in System Stop mode, leading to an additional consumption. It is recommended to use SVOS3 LP mode to optimize power consumption.*

Table 41. Typical current consumption RAM shutoff in Stop mode

Symbol	Parameter	Conditions	Typ LDO			Unit
			SVOS3 LP	SVOS4	SVOS5	
Δ_{IDD}(Stop)	Stop, Dstop or Dstop2	AXISRAM1 shutoff power consumption (power consumption reduction when AXISRAM1 shutoff is enabled)	3.00	1.80	3.00	µA
		AXISRAM2 shutoff power consumption (power consumption reduction when AXISRAM2 shutoff is enabled)	4.40	2.70	4.40	
		AXISRAM13 shutoff power consumption (power consumption reduction when AXISRAM3 shutoff is enabled)	4.40	2.70	4.40	
		AHBSRAM1 shutoff power consumption (power consumption reduction when AHBSRAM1 shutoff is enabled)	0.90	0.50	0.70	
		AHBSRAM2 shutoff power consumption (power consumption reduction when AHBSRAM2 shutoff is enabled)	0.90	0.50	0.70	
		ITCM and ETM shutoff power consumption (power consumption reduction when ITCM and ETM shutoff is enabled)	1.00	0.60	0.90	
		GFXMMU and JPEG shutoff power consumption (power consumption reduction when GFXMMU and JPEG shutoff is enabled)	0.20	0.10	0.10	
		High-speed interface USB and FDCAN shutoff power consumption (power consumption reduction when High-speed interface USB and FDCAN shutoff is enabled)	0.20	0.10	0.10	
		SRDSRAM shutoff power consumption (power consumption reduction when SRDSRAM shutoff is enabled)	0.30	0.30	0.40	

Table 42. Typical and maximum current consumption in Standby mode

Symbol	Parameter	Conditions		Typ				Max (3.6V)[1]				Unit
		Backup SRAM	RTC & LSE[2]	1.62 V	2.4 V[3]	3 V[3]	3.3 V[3]	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 130 °C	
I_{DD} (Standby)	Supply current in Standby mode, **IWDG OFF**	OFF	OFF	1.97	2.76	3.02	3.30	4.0	11.0	22.0	57.0	µA
		ON	OFF	2.78	3.69	4.02	4.40	5.4	13.0	25.0	64.0	
		OFF	ON	2.46	3.37	3.73	4.07	5.0	12.2	23.3	59.0	
		ON	ON	3.27	4.30	4.73	5.17	6.4	14.2	26.3	66.0	

1. *Guaranteed by characterization results.*
2. *The LSE clock is in low-drive mode.*

3. *These values are given for PDR ON. When the PDR is OFF (internal reset OFF), the typical current consumption is reduced (refer to Section 6.3.5 Embedded reset and power control block characteristics).*

Table 43. Typical and maximum current consumption in V_{BAT} mode

Symbol	Parameter	Conditions		Typ				Max (3.6V)[1]				Unit
		Backup SRAM	RTC & LSE[2]	1.2 V	2 V	3 V	3.3 V	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J= 130 °C	
I_{DD} (VBAT)	Supply current in V_{BAT} mode	OFF	OFF	0.01	0.02	0.03	0.07	0.2	1.9	4.6	14	µA
		ON	OFF	0.85	0.93	1.05	1.14	1.5	3.6	7.5	20.0	
		OFF	ON	0.50	0.63	0.74	0.84	1.2	3.1	5.9	16	
		ON	ON	1.34	1.54	1.76	1.91	2.5	4.8	8.8	22.0	

1. *Guaranteed by characterization results.*
2. *The LSE clock is in low-drive mode.*

I/O system current consumption

I/O static current consumption

All the I/Os used as inputs with pull-up generate a current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in Table 65. I/O static characteristics.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

An additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid a current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see Table 44. Peripheral current consumption in Run mode), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW}=V_{DDx} \times f_{sw} \times C_L$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDx} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C_L is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The I/O compensation cell is enabled.
- $f_{rcc\_cpu\_ck}$ is the CPU clock. $f_{PCLK} = f_{rcc\_cpu\_ck}/4$, and $f_{HCLK} = f_{rcc\_cpu\_ck}/2$.

The given value is calculated by measuring the difference of current consumption

- with all peripherals clocked off
- with only one peripheral clocked on
- $f_{rcc\_cpu\_ck}$ = 280 MHz (Scale 0), $f_{rcc\_cpu\_ck}$ = 225 MHz (Scale 1), $f_{rcc\_cpu\_ck}$ = 160 MHz (Scale 2), $f_{rcc\_cpu\_ck}$ = 88 MHz (Scale 3)
- The ambient operating temperature is 25 °C and V_{DD}=3.3 V.

Table 44. Peripheral current consumption in Run mode

Peripheral		I_{DD}(Typ)				Unit
		VOS0	VOS1	VOS2	VOS3	
AHB3	MDMA	7.10	6.40	5.90	5.40	µA/MHz
	DMA2D	3.00	2.80	2.50	2.30	
	JPGDEC	4.70	4.40	4.00	3.60	
	FLITF	20.00	19.00	17.00	15.00	
	FMC registers	1.30	1.30	1.20	1.10	
	FMC kernel	10.00	9.30	8.40	7.70	
	OSPI1 registers	0.50	0.60	0.50	0.50	
	OSPI1 kernel	2.30	2.20	2.00	1.80	
	SDMMC1 registers	8.90	8.30	7.60	6.90	
	SDMMC1 kernel	2.20	2.00	1.80	1.60	
	OSPI2 registers	0.70	0.70	0.70	0.60	
	OSPI2 kernel	2.00	1.80	1.60	1.50	
	IOMNGR	0.30	0.30	0.30	0.30	
	GFXMMU	2.80	2.70	2.40	2.30	
	AXISRAM2	5.30	5.00	4.60	4.20	
	AXISRAM3	5.40	5.10	4.60	4.30	
	DTCM1	1.10	1.10	1.00	1.00	
	DTCM2	0.70	0.80	0.70	0.70	
	ITCM	1.10	1.10	1.00	1.00	
	AXISRAM1	5.30	5.00	4.60	4.20	
	Bridge	0.10	0.10	0.10	0.10	
AHB1	DMA1	0.90	0.90	0.80	0.70	
	DMA2	0.90	0.80	0.80	0.70	
	CRC	0.60	0.60	0.50	0.50	
	ADC12 registers	5.40	4.90	4.50	4.10	
	ADC12 kernel	1.10	1.00	0.90	0.80	
	USB1OTG registers	24.00	22.00	20.00	18.00	
	USB1OTG kernel	9.50	9.30	9.10	8.80	
	USB1ULPI	0.10	0.10	0.10	0.10	
	Bridge	0.10	0.10	0.10	0.10	
AHB2	DCMI	5.00	4.60	4.20	3.90	
	HSEM	0.10	0.10	0.10	0.10	
	RNG registers	1.50	1.40	1.20	1.10	
	RNG kernel	10.00	9.70	9.50	9.20	

Peripheral		I_{DD}(Typ)				Unit
		VOS0	VOS1	VOS2	VOS3	
AHB2	SDMMC2 registers	6.80	6.30	5.70	5.20	µA/MHz
	SDMMC2 kernel	2.30	2.10	1.90	1.70	
	BDMA1	1.70	1.60	1.50	1.30	
	AHBSRAM1	0.70	0.70	0.60	0.60	
	AHBSRAM2	0.70	0.60	0.60	0.50	
	Bridge	9.10	8.40	7.70	7.00	
AHB4	GPIOA	2.00	1.80	1.70	1.50	
	GPIOB	1.80	1.70	1.50	1.40	
	GPIOC	2.00	1.80	1.70	1.50	
	GPIOD	2.00	1.80	1.70	1.50	
	GPIOE	1.90	1.80	1.60	1.50	
	GPIOF	1.90	1.80	1.60	1.50	
	GPIOG	2.00	1.80	1.70	1.50	
	GPIOH	1.90	1.80	1.60	1.50	
	GPIOI	1.90	1.80	1.60	1.50	
	GPIOJ	1.90	1.80	1.60	1.50	
	GPIOK	2.00	1.80	1.70	1.50	
	BDMA2	4.20	3.90	3.50	3.20	
	SRDSRAM	0.60	0.50	0.50	0.50	
	BKPRAM	0.80	0.70	0.70	0.60	
	IWDG	0.07	0.07	0.07	0.07	
	Bridge	0.10	0.10	0.10	0.10	
APB3	LTDC	12.00	11.00	9.80	8.90	
	WWDG1	1.10	1.00	0.90	0.90	
	Bridge	0.10	0.10	0.10	0.10	
APB1	TIM2	7.50	6.90	6.30	6.20	
	TIM3	6.30	5.90	5.40	4.90	
	TIM4	5.80	5.40	4.90	4.50	
	TIM5	7.20	6.70	6.10	5.60	
	TIM6	1.60	1.50	1.30	1.20	
	TIM7	1.60	1.40	1.30	1.20	
	TIM12	3.60	3.30	3.00	2.80	
	TIM13	2.80	2.60	2.40	2.10	
	TIM14	2.50	2.30	2.10	1.90	
	LPTIM1 registers	0.80	0.80	0.70	0.60	
	LPTIM1 kernel	2.20	2.00	1.80	1.70	
	SPI2 registers	2.20	2.00	1.80	1.70	
	SPI2 kernel	0.90	0.80	0.80	0.70	
	SPI3 registers	2.70	2.40	2.30	2.00	
	SPI3 kernel	0.90	0.80	0.70	0.70	

Peripheral		I_{DD}(Typ)				Unit
		VOS0	VOS1	VOS2	VOS3	
APB1	SPDIFRX1 registers	0.60	0.50	0.50	0.40	µA/MHz
	SPDIFRX1 kernel	2.90	2.70	2.50	2.20	
	USART2 registers	2.00	1.80	1.70	1.50	
	USART2 kernel	4.60	4.30	3.90	3.60	
	USART3 registers	2.00	1.80	1.70	1.50	
	USART3 kernel	4.50	4.20	3.80	3.40	
	UART4 registers	1.70	1.60	1.50	1.30	
	UART4 kernel	3.70	3.40	3.10	2.80	
	UART5 registers	1.80	1.70	1.50	1.40	
	UART5 kernel	3.80	3.50	3.20	2.90	
	I2C1 registers	0.90	0.80	0.80	0.70	
	I2C1 kernel	2.10	2.00	1.80	1.70	
	I2C2 registers	0.90	0.80	0.70	0.70	
	I2C2 kernel	2.10	1.90	1.80	1.60	
	I2C3 registers	0.90	0.80	0.70	0.70	
	I2C3 kernel	2.20	2.00	1.80	1.70	
	HDMICEC registers	0.50	0.50	0.40	0.40	
	HDMICEC kernel	0.10	0.10	0.10	0.10	
	DAC1	1.40	1.30	1.20	1.10	
	UART7 registers	1.80	1.70	1.50	1.40	
	UART7 kernel	3.80	3.50	3.20	2.90	
	UART8 registers	2.10	2.00	1.80	1.70	
	UART8 kernel	3.80	3.50	3.20	2.90	
	Bridge	0.30	0.30	0.20	0.10	
	CRS	0.50	0.40	0.40	0.40	
	SWP registers	2.30	2.10	2.00	1.80	
	SWP kernel	0.10	0.10	0.10	0.10	
	OPAMP	4.20	3.80	3.50	3.20	
	MDIO	3.10	2.90	2.60	2.40	
	FDCAN registers	17.00	16.00	15.00	14.00	
	FDCAN kernel	5.60	4.80	3.50	1.10	
	Bridge	0.10	0.10	0.10	0.10	
APB2	TIM1	9.80	9.10	8.30	7.60	
	TIM8	9.50	8.80	8.00	7.30	
	USART1 registers	0.10	0.10	0.10	0.10	
	USART1 kernel	0.10	0.10	0.10	0.10	
	USART6 registers	3.80	4.00	4.50	6.30	
	USART6 kernel	0.10	0.10	0.10	0.10	
	USART10 registers	4.00	4.10	4.60	6.40	
	USART10 kernel	0.10	0.10	0.10	0.10	

Peripheral		I_{DD}(Typ)				Unit
		VOS0	VOS1	VOS2	VOS3	
APB2	UART9 registers	3.50	3.60	4.00	5.50	µA/MHz
	UART9 kernel	0.10	0.10	0.10	0.10	
	SPI1 registers	2.10	1.90	1.80	1.60	
	SPI1 kernel	0.90	0.80	0.70	0.70	
	SPI4 registers	2.10	1.90	1.70	1.50	
	SPI4 kernel	0.50	0.50	0.40	0.40	
	TIM15	5.30	4.90	4.40	4.00	
	TIM16	4.20	3.90	3.50	3.20	
	TIM17	4.30	4.00	3.60	3.30	
	SPI5 registers	2.00	1.90	1.70	1.50	
	SPI5 kernel	0.50	0.50	0.40	0.40	
	SAI1 registers	1.80	1.60	1.50	1.30	
	SAI1 kernel	1.40	1.30	1.20	1.00	
	SAI2 registers	2.30	2.10	1.90	1.70	
	SAI2 kernel	1.20	1.10	1.00	0.90	
	DFSDM1 registers	10.00	9.60	8.80	8.00	
	DFSDM1 kernel	0.10	0.10	0.10	0.10	
	Bridge	0.50	0.40	0.40	0.30	
APB4	SYSCFG	0.40	0.30	0.30	0.30	
	LPUART1 registers	1.10	1.00	0.90	0.80	
	LPUART1 kernel	2.30	2.10	1.90	1.70	
	SPI6 registers	1.70	1.50	1.40	1.30	
	SPI6 kernel	0.60	0.50	0.50	0.40	
	I2C4 registers	0.80	0.70	0.60	0.60	
	I2C4 kernel	1.90	1.70	1.60	1.40	
	LPTIM2 registers	0.60	0.60	0.50	0.50	
	LPTIM2 kernel	1.90	1.70	1.60	1.40	
	LPTIM3 registers	0.60	0.50	0.50	0.40	
	LPTIM3 kernel	1.50	1.40	1.30	1.20	
	DAC2	0.80	0.70	0.60	0.50	
	COMP12	0.40	0.30	0.30	0.30	
	VREF	0.30	0.30	0.20	0.20	
	RTCAPB	1.90	1.70	1.60	1.40	
	TMPSENS	2.30	2.10	2.00	1.80	
	DFSDM2 registers	1.70	1.50	1.40	1.30	
	DFSDM2 kernel	0.10	0.10	0.10	0.10	
	Bridge	0.10	0.10	0.10	0.10	

Table 45. Peripheral current consumption in Stop, Standby and V_{BAT} mode

Symbol	Parameter	Conditions	Typ	Max (3.6 V)				Unit
			3.3 V	T_J = 25 °C	T_J= 85 °C	T_J = 105 °C	T_J = 130 °C	
I_{DD}	RTC+LSE low drive	-	0.77	1.0	1.2	1.3	2.0	µA
	RTC+LSE medium- low drive	-	0.87	1.1	1.3	1.4	2.1	
	RTC+LSE medium- high drive	-	1.03	1.3	1.5	1.6	2.3	
	RTC+LSE High drive	-	1.38	1.6	1.8	1.9	2.6	
	Backup SRAM	-	1.10	1.4	2.0	3.2	7.0	

6.3.8 Wakeup time from low-power modes

The wakeup times given in Table 46. Low-power mode wakeup timings are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PC1) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD}=3.3 V.

Table 46. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ(1)	Max(1)(2)	Unit
$t_{WUSLEEP}$(3)	Wakeup from Sleep	-	5.00	5.00	CPU clock cycles
$t_{WUDSTOP}$(3)	Wakeup from DStop	SVOS3 Main, HSI, flash memory in normal mode	4.2	6	µs
		SVOS3 Main, HSI, flash memory in low-power mode	8.3	11	
		SVOS3 LP, HSI, flash memory in normal mode	5.0	7	
		SVOS3 LP, HSI, flash memory in low-power mode	9.0	12	
		SVOS4, HSI, flash memory in normal mode	15.7	19	
		SVOS4, HSI, flash memory in low-power mode	19.7	25	
		SVOS5, HSI, flash memory in normal mode	35.0	43	
		SVOS5, HSI, flash memory in low-power mode	35.0	43	
		SVOS3 Main, CSI, flash memory in normal mode	42.5	52	
		SVOS3 Main, CSI, flash memory in low power mode	48.0	58	
		SVOS3 LP, CSI, flash memory in normal mode	43.3	53	
		SVOS3 LP, CSI, flash memory in low power mode	48.8	59	
		SVOS4, CSI, flash memory in normal mode	54.0	65	
		SVOS4, CSI, flash memory in low-power mode	59.5	72	
		SVOS5, CSI, flash memory in normal mode	74.8	90	
		SVOS5, CSI, flash memory in low-power mode	74.8	90	
$t_{WUDSTOP2}$(3)	Wakeup from DStop2, clock kept running	SVOS3 LP, HSI, flash memory in low-power mode	9.7	13	
		SVOS4, HSI, flash memory in low-power mode	20.4	26	
		SVOS5, HSI, flash memory in low-power mode	35.7	44	
		SVOS3 LP, CSI, flash memory in low-power mode	51.3	62	
		SVOS4, CSI, flash memory in low-power mode	62.0	75	
		SVOS5, CSI, flash memory in low-power mode	77.3	93	
$t_{WUSTDBY}$(3)	Wakeup from Standby mode	-	257	330	

1. *Guaranteed by characterization results.*
2. *Measures done at −40 °C in the worst conditions.*
3. *The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.*

6.3.9 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode, the HSE oscillator is switched off and the input pin is a standard I/O.

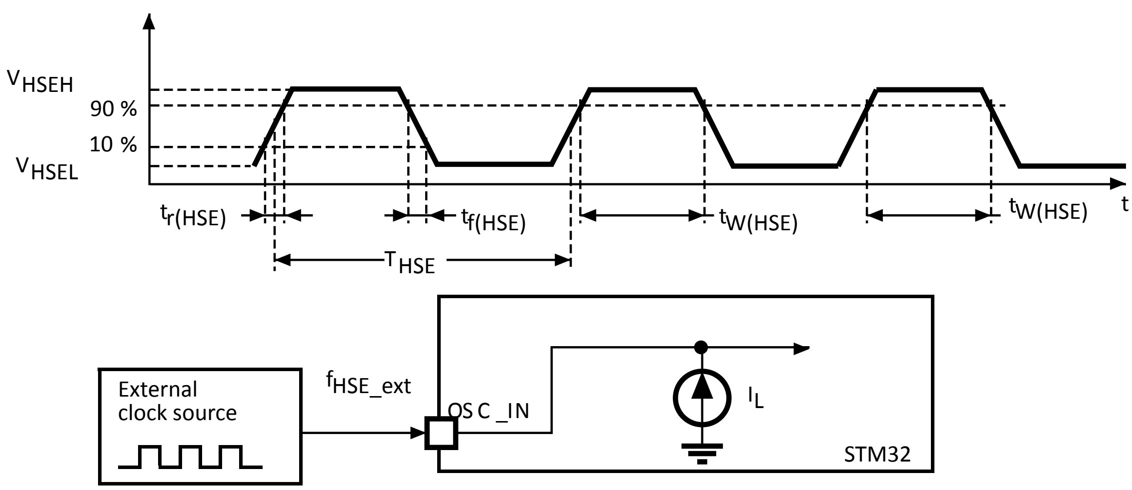
The external clock signal has to respect Table 47. High-speed external user clock characteristics in addition to Table 65. I/O static characteristics. The external clock can be low-swing (analog) or digital. In case of a low-swing analog input clock, the clock squarer must be activated (refer to RM0455).

Table 47. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
f_{HSE_ext}	User external clock source frequency	External digital/analog clock	4	25	50	MHz
V_{HSEH}	Digital OSC_IN input high-level voltage	External digital clock	0.7 V_{DD}	-	V_{DD}	V
V_{HSEL}	Digital OSC_IN input low-level voltage		V_{SS}	-	0.3 V_{DD}	
$t_{W(HSEH)}/t_{W(HSEL)}$(2)	Digital OSC_IN input high or low time	External digital clock	7	-	-	ns
V_{lswHSE} ($V_{HSEH}-V_{HSEL}$)(3)	Analog low-swing OSC_IN peak-to-peak amplitude	External analog low-swing clock	0.2	-	2/3 V_{DD}	V
$DuCy_{HSE}$	Analog low-swing OSC_IN duty cycle		45	50	55	%
$t_{r(HSE)}/t_{f(HSE)}$	Analog low-swing OSC_IN rise and fall times	External analog low-swing clock, 10% to 90%	0.05 / f_{HSE_ext}	-	0.3 / f_{HSE_ext}	ns

1. *Guaranteed by design.*
2. *The rise and fall times for a digital input signal are not specified. However the V_{HSEH} and V_{HSEL} conditions must be fulfilled.*
3. *The DC component of the signal must ensure that the signal peaks are located between V_{DD} and V_{SS}.*

Figure 30. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode, the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect Table 48. Low-speed external user clock characteristics in addition to Table 65. I/O static characteristics. The external clock can be low-swing (analog) or digital. In case of a low-swing analog input clock, the clock squarer must be activated (refer to RM0455).

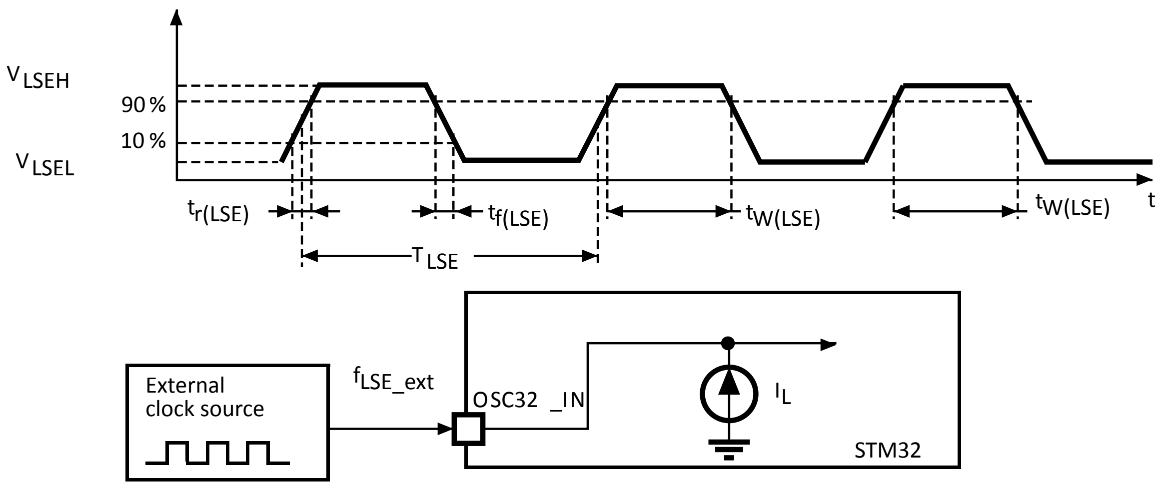
Table 48. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min[(1)]	Typ[(1)]	Max[(1)]	Unit
f_{LSE_ext}	User external clock source frequency	External digital/analog clock	-	32.768	1000	kHz
V_{LSEH}	Digital OSC32_IN input high-level voltage	External digital clock	0.7 V_{DD}	-	V_{DD}	V
V_{LSEL}	OSC32_IN input low-level voltage	External digital clock	V_{SS}	-	0.3 V_{DD}	V
$t_{w(LSEH)}$/ $t_{w(LSEL)}$	OSC32_IN high or low time	External digital clock	250	-	-	ns
V_{lsw_H}	Analog low-swing OSC_IN high-level voltage	External analog low-swing clock	0.6	-	1.225	V
V_{lsw_L}	Analog low-swing OSC_IN low-level voltage	External analog low-swing clock	0.35	-	0.8	V
V_{lswLSE} (V_{LSEH}−V_{LSEL})	Analog low-swing OSC_IN peak-to-peak amplitude	External analog low-swing clock	0.2	-	0.875	V
$DuCy_{LSE}$	Analog low-swing OSC_IN duty cycle	External analog low-swing clock	45	50	55	%
$t_{r(LSE)}$/$t_{f(LSE)}$	Analog low-swing OSC_IN rise and fall times	External analog low-swing clock, 10% to 90%	-	100	200	ns

1. Guaranteed by design.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 31. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 50 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in Table 49. 4-50 MHz HSE oscillator characteristics. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 49. 4-50 MHz HSE oscillator characteristics

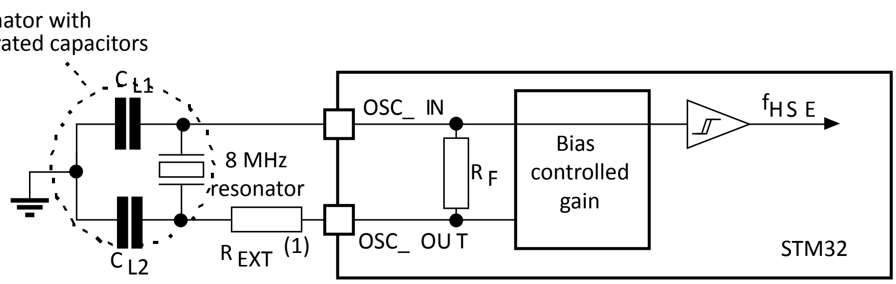
Symbol	Parameter	Operating conditions(1)	Min(2)	Typ(2)	Max(2)	Unit
F	Oscillator frequency	-	4	-	50	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	4	mA
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 4 MHz	-	0.35	-	
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 8 MHz	-	0.40	-	
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 16 MHz	-	0.45	-	
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 32 MHz	-	0.65	-	
		V_{DD}=3 V, Rm=30 Ω C_L=10 pF at 48 MHz	-	0.95	-	
$Gm_{critmax}$	Maximum critical crystal gm	Startup	-	-	1.5	mA/V
t_{SU}(4)	Start-up time	V_{DD} is stabilized	-	2	-	ms

1. *Resonator characteristics given by the crystal/ceramic resonator manufacturer.*
2. *Guaranteed by design.*
3. *This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.*
4. *$t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.*

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typical), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see Figure 32. Typical application with an 8 MHz crystal). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. The PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 32. **Typical application with an 8 MHz crystal**



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in Table 50. Low-speed external user clock characteristics. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

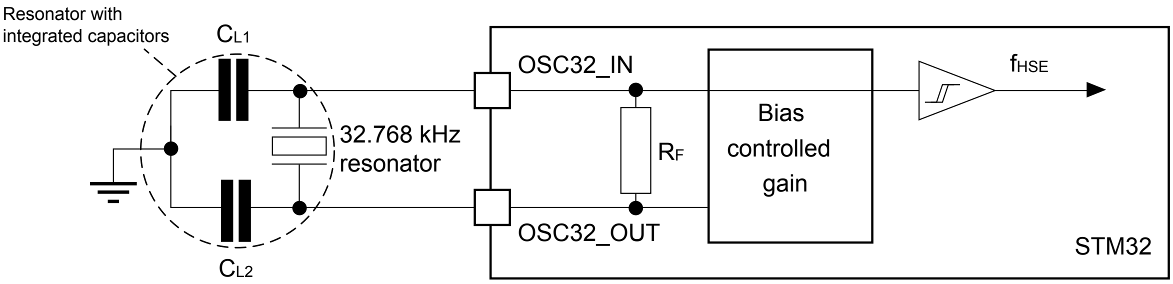
Table 50. **Low-speed external user clock characteristics**

Symbol	Parameter	Operating conditions(1)	Min(2)	Typ(2)	Max(2)	Unit
F	Oscillator frequency	-	-	32.768	-	kHz
I_{DD}	LSE current consumption	LSEDRV[1:0] = 00, Low drive capability	-	290	-	nA
		LSEDRV[1:0] = 01, Medium Low drive capability	-	390	-	
		LSEDRV[1:0] = 10, Medium high drive capability	-	550	-	
		LSEDRV[1:0] = 11, High drive capability	-	900	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00, Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01, Medium Low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10, Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11, High drive capability	-	-	2.7	
t_{SU}(3)	Startup time	VDD is stabilized	-	2	-	s

1. *Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers.*
2. *Guaranteed by design.*
3. *t_{SU} is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768k Hz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.*

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 33. **Typical application with a 32.768 kHz crystal**



1. An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.10 Internal clock source characteristics

The parameters given in Table 51. HSI48 oscillator characteristics to Table 54. LSI oscillator characteristics are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 22. General operating conditions.

48 MHz high-speed internal RC oscillator (HSI48)

Table 51. **HSI48 oscillator characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 frequency	V_{DD} = 3.3 V, T_J = 30 °C	47.5(1)	48	48.5(1)	MHz
TRIM(2)	User trimming step	-	-	0.175	0.250	%
USER TRIM COVERAGE(3)	User trimming coverage	± 32 steps	±4,70	±5.6	-	%
DuCy(HSI48)(2)	Duty cycle	-	45	-	55	%
ACCHSI48_REL(3)	Accuracy of the HSI48 oscillator over temperature (reference is 30 °C)	T_J = −40 to 130 °C	−4.5	-	4	%
ΔV_{DD}(HSI48)(2)	HSI48 oscillator frequency drift with V_{DD} (reference is 3.3 V)	V_{DD} = 3 to 3.6 V	-	0.025	0.05	%
		V_{DD} = 1.62 to 3.6 V	-	0.05	0.1	
t_{su}(HSI48)(2)	HSI48 oscillator startup time	-	-	2.1	4.0	µs
I_{DD}(HSI48)(2)	HSI48 oscillator power consumption	-	-	350	400	µA
N_T jitter(2)	Next transition jitter accumulated jitter on 28 cycles	-	-	± 0.15	-	ns
P_T jitter(2)	Paired transition jitter Accumulated jitter on 56 cycles(6)	-	-	± 0.25	-	ns

1. *Calibrated during manufacturing tests.*
2. *Guaranteed by design.*
3. *Guaranteed by characterization results.*
4. *Δf_{HSI} = ACCHSI48_REL + ΔV_{DD}*
5. *These values are obtained by using the formula: (Freq(3.6 V) − Freq(3.0 V)) / Freq(3.0 V) or (Freq(3.6 V) − Freq(1.62 V)) / Freq(1.62 V).*
6. *Jitter measurements are performed without clock sources activated in parallel.*

64 MHz high-speed internal RC oscillator (HSI)

Table 52. **HSI oscillator characteristics**

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
f_{HSI}	HSI frequency	V_{DD}=3.3 V, T_J=30 °C	63.7(2)	64	64.3(2)	MHz
TRIM	HSI user trimming step	Trimming is not a multiple of 32(3)	-	0.24	0.32	%
		Trimming is 128, 256 and 384(3)	−5.2	−1.8	-	
		Trimming is 64, 192, 320 and 448(3)	−1.4	−0.8	-	
		Other trimming are a multiple of 32 (not including multiple of 64 and 128)(3)	−0.6	−0.25	-	
DuCy(HSI)	Duty Cycle	-	45	-	55	%
$\Delta_{VDD\ (HSI)}$	HSI oscillator frequency drift over V_{DD} (reference is 3.3 V)	V_{DD}=1.62 to 3.6 V	−0.12	-	0.03	%
$\Delta_{TEMP\ (HSI)}$	HSI oscillator frequency drift over temperature (reference is 64 MHz)	T_J=-20 to 105 °C	−1(4)	-	1(4)	%
		T_J=−40 to $T_J$max °C	−2(4)	-	1(4)	
t_{su}(HSI)	HSI oscillator start-up time	-	-	1.4	2	µs
t_{stab}(HSI)	HSI oscillator stabilization time	at 1 % of target frequency	-	4	8	µs
		at 5 % of target frequency	-	-	4	
I_{DD}(HSI)	HSI oscillator power consumption	-	-	300	400	µA

1. *Guaranteed by design, unless otherwise specified.*
2. *Calibrated during manufacturing tests.*
3. *Trimming value of HSICAL[8:0] (refer to RM0455).*
4. *Guaranteed by characterization results.*

4 MHz low-power internal RC oscillator (CSI)

Table 53. **CSI oscillator characteristics**

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
f_{CSI}	CSI frequency	V_{DD} = 3.3 V, T_J = 30 °C	3.96(2)	4	4.04(2)	MHz
TRIM	CSI user trimming step	Trimming is not a multiple of 16	-	0.40	0.75	-
		Trimming is a multiple of 32	−4,75	−2,75	0.75	-
		Other trimming are a multiple of 16 (not including multiple of 32)	−0,43	0.00	0.75	%
DuCy(CSI)	Duty Cycle	-	45	-	55	%
Δ_{TEMP} (CSI)	CSI oscillator frequency drift over temperature	T_J = 0 to 85 °C	−3.7(3)	-	4,5(3)	%
		T_J = −40 to 130 °C	−11(3)	-	7,5(3)	
ΔV_{DD}(CSI)	CSI oscillator frequency drift over V_{DD}	V_{DD} = 1.62 to 3.6 V	−0.06	-	0.06	%
t_{su}(CSI)	CSI oscillator startup time	-	-	1	2	µs
t_{stab}(CSI)	CSI oscillator stabilization time (to reach ± 3 % of f_{CSI})	-	-	-	4	cycle
I_{DD}(CSI)	CSI oscillator power consumption	-	-	23	30	µA

1. *Guaranteed by design, unless otherwise specified.*
2. *Calibrated during manufacturing tests.*
3. *Guaranteed by characterization results.*

Low-speed internal (LSI) RC oscillator

Table 54. **LSI oscillator characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	V_{DD} = 3.3 V, T_J = 25 °C	31,4[1]	32	32,6[1]	kHz
		T_J = –40 to 110 °C, V_{DD} = 1.62 to 3.6 V	29,76[2]	-	33,6[2]	
		T_J = –40 to 130 °C, V_{DD} = 1.62 to 3.6 V	29,4[2]	-	33,6[2]	
$t_{su}(LSI)$[3]	LSI oscillator startup time	-	-	80	130	µs
$t_{stab}(LSI)$[3]	LSI oscillator stabilization time (5% of final value)	-	-	120	170	
$I_{DD}(LSI)$[3]	LSI oscillator power consumption	-	-	130	280	nA

1. *Calibrated during manufacturing tests.*
2. *Guaranteed by characterization results.*
3. *Guaranteed by design.*

6.3.11 PLL characteristics

The parameters given in Table 55. PLL characteristics (wide VCO frequency range) are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in Table 22. General operating conditions.

Table 55. **PLL characteristics (wide VCO frequency range)**

Symbol	Parameter	Conditions		Min[1]	Typ[1]	Max[1]	Unit
f_{PLL_IN}	PLL input clock	-		2	-	16	MHz
	PLL input clock duty cycle	-		10	-	90	%
$f_{PLL\_P\_OUT}$	PLL multiplier output clock P, Q, R	VOS0		1	-	280[2]	MHz
		VOS1		1	-	225[2]	
		VOS2		1	-	160[2]	
		VOS3		1	-	88[2]	
f_{VCO_OUT}	PLL VCO output	-		128	-	560[3]	
t_{LOCK}	PLL lock time	Normal mode		-	45	100[3]	µs
		Sigma-delta mode (f_{PLL_IN} ≥ 8 MHz)		-	60	120[3]	
Jitter	Cycle-to-cycle jitter	f_{VCO_OUT} = 128 MHz		-	60	-	±ps
		f_{VCO_OUT} = 200 MHz		-	50	-	
		f_{VCO_OUT} = 400 MHz		-	20	-	
		f_{VCO_OUT} = 560 MHz		-	15	-	
	Long term jitter	Normal mode (f_{PLL_IN} = 2 MHz), f_{VCO_OUT} = 560 MHz		-	±0.2	-	%
		Normal mode (f_{PLL_IN} = 16 MHz), f_{VCO_OUT} = 560 MHz		-	±0.8	-	
		Sigma-delta mode (f_{PLL_IN} = 2 MHz), f_{VCO_OUT} = 560 MHz		-	±0.2	-	
		Sigma-delta mode (f_{PLL_IN} = 16 MHz), f_{VCO_OUT} = 560 MHz		-	±0.8	-	
$I_{DD(PLL)}$	PLL power consumption	f_{VCO_OUT} = 560 MHz	V_{DD}	-	330	420	µA
			V_{CORE}	-	630	-	
		f_{VCO_OUT} = 128 MHz	V_{DD}	-	155	230	

Symbol	Parameter	Conditions		Min(1)	Typ(1)	Max(1)	Unit
$I_{DD(PLL)}$	PLL power consumption	f_{VCO_OUT} = 128 MHz	V_{CORE}	-	170	-	μA

1. *Guaranteed by design, unless otherwise specified.*
2. *This value must be limited to the maximum frequency due to the product limitation.*
3. *Guaranteed by characterization results.*

Table 56. PLL characteristics (medium VCO frequency range)

Symbol	Parameter	Conditions		Min(1)	Typ(1)	Max(1)	Unit
f_{PLL_IN}	PLL input clock	-		1	-	2	MHz
	PLL input clock duty cycle	-		10	-	90	%
f_{PLL_OUT}	PLL multiplier output clock P, Q, R	VOS0		1.17	-	210	MHz
		VOS1		1.17	-	210	
		VOS2		1.17	-	160(2)	
		VOS3		1.17	-	88(2)	
f_{VCO_OUT}	PLL VCO output	-		150	-	420	
t_{LOCK}	PLL lock time	Normal mode		-	45	80(3)	μs
		Sigma-delta mode			forbidden		
Jitter	Cycle-to-cycle jitter	f_{VCO_OUT} = 150 MHz	-	-	60	-	±ps
		f_{VCO_OUT} = 200 MHz	-	-	40	-	
		f_{VCO_OUT} = 400 MHz	-	-	18	-	
		f_{VCO_OUT} = 420 MHz	-	-	15	-	
	Period jitter	f_{VCO_OUT} = 150 MHz	f_{PLL_OUT} = 50 MHz	-	75	-	±-ps
		f_{VCO_OUT} = 400 MHz		-	25	-	
	Long term jitter	Normal mode, f_{VCO_OUT} = 400 MHz		-	±0.2	-	%
$I_{DD(PLL)}$	PLL power consumption on V_{DD}	f_{VCO_OUT} = 420 MHz	V_{DD}	-	275	360	μA
			V_{CORE}	-	450	-	
		f_{VCO_OUT} = 150 MHz	V_{DD}	-	160	240	
			V_{CORE}	-	165	-	

1. *Guaranteed by design, unless otherwise specified.*
2. *This value must be limited to the maximum frequency due to the product limitation.*
3. *Guaranteed by characterization results.*

6.3.12 Memory characteristics

Flash memory

The characteristics are given at T_J = –40 to 130 °C unless otherwise specified.

The devices are shipped to customers with the flash memory erased.

Table 57. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Word program	-	2.5	4	mA
		Sector erase	-	1.8	3	
		Mass erase	-	2.0	3	

Table 58. Flash memory programming

Symbol	Parameter	Conditions	Min[1]	Typ	Max[1]	Unit
t_{prog}	Word program time	128 bits (user area)	-	-	20	µs
		16 bits (OTP area)	-	-	20	
$t_{ERASE8KB}$	Sector erase time (8 Kbytes)	-	-	-	2.2	ms
t_{ME}	Single-bank mass erase time		-	-	10	
	Dual-bank mass erase time		-	-	10	
V_{prog}	Programming voltage		1.62	-	3.6	V

1. *Guaranteed by characterization results.*

Table 59. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min[1]	
N_{END}	Endurance	T_J = –40 to +130 °C	10	kcycles
t_{RET}	Data retention	1 kcycle at T_A = 85 °C	30	Years
	-	10 kcycles at T_A = 55 °C	20	

1. *Guaranteed by characterization results.*

6.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in Table 60. EMS characteristics. They are based on the EMS levels and classes defined in application note AN1709.

Table 60. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, LQFP144, $f_{rcc\_cpu\_ck}$ = 216 MHz, conforms to IEC 61000-4-2	3B
V_{FTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance		5A

As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 61. EMI characteristics for f_{HSE} = 8 MHz and f_{HCLK} = 64 MHz

Symbol	Parameter	Conditions	Monitored frequency band	Value	Unit
S_{EMI}	Peak[1]	V_{DD} = 3.6 V, T_A = 25 °C, LQFP64 package, compliant with IEC 61967-2	0.1 to 30 MHz	7	dBµV
			30 to 130 MHz	–1	
			130 MHz to 1 GHz	8	
			1 GHz to 2 GHz	7	
	Level[2]		0.1 GHz to 2 GHz	2.5	-

1. *Refer to the EMI radiated test chapter of application note AN1709 "EMC design guide for STM8, STM32 and Legacy MCUs" available from the ST website www.st.com..*
2. *Refer to the EMI level classification chapter of application note AN1709 "EMC design guide for STM8, STM32 and Legacy MCUs" available from the ST website www.st.com.*

6.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse) are applied to the pins of each sample according to each pin combination. This test conforms to the ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 standards.

Table 62. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Packages	Class	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to ANSI/ESDA/ JEDEC JS-001	Packages with SMPS	1C	1000[2]	V
			Packages without SMPS	2	2000	
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESDA/ JEDEC JS-002	All LQFP packages and WLCSP	C1	250	
			All BGA packages	C2a	500	

1. *Guaranteed by characterization results.*
2. *The electrostatic discharge is 2000 V for all pins, except V_{FBSMPS}, for which the test fails at 2000 V and passes at 1600 V.*

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with JESD78 IC latchup standard.

Table 63. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latchup class	T_J= +130 °C, conforming to JESD78	II level A

6.3.15 I/O current injection characteristics

As a general rule, a current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3.3 V-capable I/O pins) should be avoided during the normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when an abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during the device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

The following tables are the compilation of the SIC1/SIC2 and functional ESD results.

Negative induced A negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

Table 64. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	PF2, PI12	0	NA	mA
	PG1, PE9, PB0, PA7, PC4, PC5, PE7, PE8, PA4, PA5, PA6, PF2, PI12, PC2_C, PC3_C, PA0_C, PA1_C, BOOT0	0	0	
	All other I/Os	5	NA	

6.3.16 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 65. I/O static characteristics are derived from tests performed under the conditions summarized in Table 22. General operating conditions. All I/Os are CMOS and TTL compliant (except for BOOT0).

Note: For information on GPIO configuration, refer to the application note AN4899 “STM32 GPIO configuration for hardware settings and low-power consumption” available from the ST website www.st.com.

Table 65. I/O static characteristics

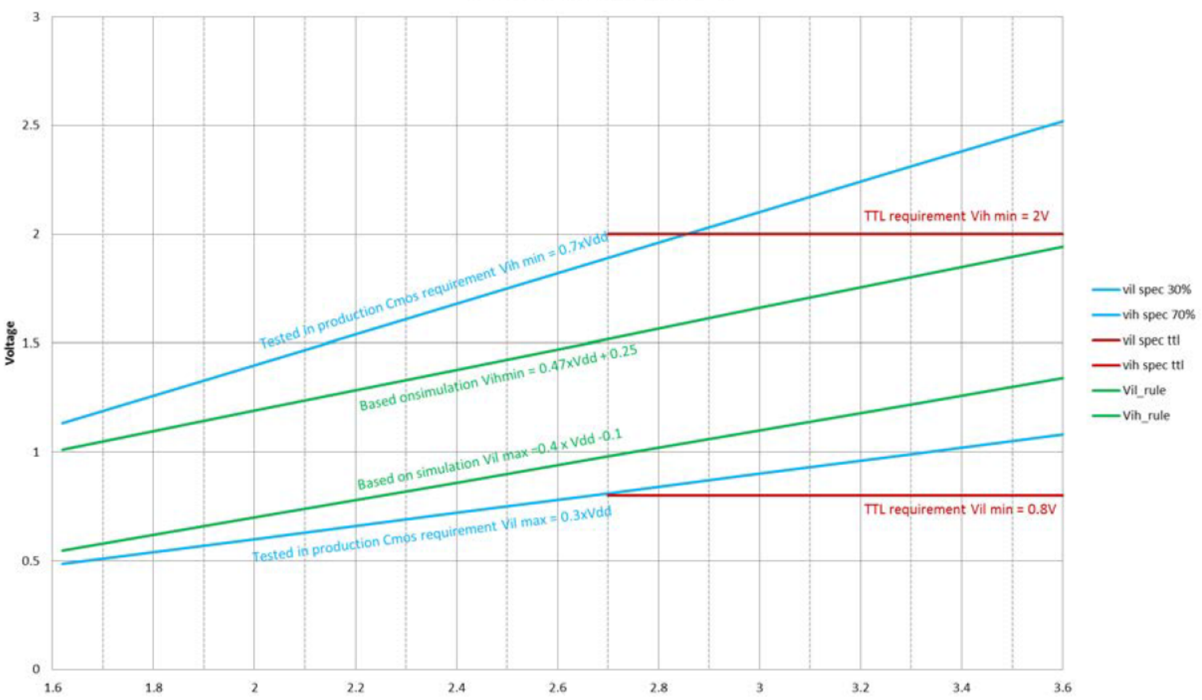
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	I/O input low-level voltage except BOOT0	$1.62\ V < V_{DDIOx} < 3.6\ V$	-	-	$0.3V_{DD}$ (1)	V
	I/O input low-level voltage except BOOT0		-	-	$0.4V_{DD}-0.1$(2)	
	BOOT0 I/O input low level voltage		-	-	$0.19V_{DD}+0.1$(2)	
V_{IH}	I/O input high level voltage except BOOT0	$1.62\ V < V_{DDIOx} < 3.6\ V$	$0.7V_{DD}$ (1)	-	-	V
	I/O input high level voltage except BOOT0		$0.47V_{DD}+0.25$(2)	-	-	
	BOOT0 I/O input high level voltage		$0.17V_{DD}+0.6$(2)	-	-	
V_{HYS}(2)	TT_xx, FT_xxx and NRST I/O input hysteresis	$1.62\ V < V_{DDIOx} < 3.6\ V$	-	250	-	mV
	BOOT0 I/O input hysteresis		-	200	-	
I_{lkg}	FT_xx input leakage current(2)	$0 < V_{IN} \leq Max(V_{DDxxx})$(5)	-	-	±250	nA
		$Max(V_{DDxxx}) < V_{IN} \leq 5.5\ V$ (3)(4)(5)	-	-	1500	
	FT_u I/O	$0 < V_{IN} \leq Max(V_{DDxxx})$(5)	-	-	±350	

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{lkg}	FT_u I/O	$Max(V_{DDxxx}) < V_{IN} \leq 5.5$ V (3)(4)(8)(5)	-	-	5000(6)	nA
	TT_xx input leakage current	$0 < V_{IN} \leq Max(V_{DDxxx})$(5)	-	-	±250	
	VPP (BOOT0 alternate function)	$0 < V_{IN} \leq V_{DDIOx}$	-	-	15	uA
		$V_{DDIOx} < V_{IN} \leq 9$ V	-	-	35	
RPU	Weak pull-up equivalent resistor(7)	$V_{IN} = V_{SS}$	30	40	50	kΩ
RPD	Weak pull-down equivalent resistor(7)	$V_{IN} = V_{DD}$(5)	30	40	50	
CIO	I/O pin capacitance	-	-	5	-	pF

1. *Compliant with CMOS requirements.*
2. *Guaranteed by design.*
3. *All FT_xx IO except FT_lu and FT_u.*
4. *V_{IN} must be less than $Max(V_{DDxxx}) + 3.6$ V.*
5. *$Max(V_{DDxxx})$ is the maximum value of all the I/O supplies.*
6. *To sustain a voltage higher than $MIN(V_{DD}, V_{DDA}, V_{DD33USB})$ +0.3 V, the internal pull-up and pull-down resistors must be disabled.*
7. *The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10%).*

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in Figure 34. V_{IL}/V_{IH} for all I/Os except BOOT0.

Figure 34. V_{IL}/V_{IH} for all I/Os except BOOT0



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in Section 6.2 Absolute maximum ratings. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see Table 20. Current characteristics).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see Table 20. Current characteristics).

Output voltage levels

Unless otherwise specified, the parameters given in Table 66. Output voltage characteristics for all I/Os except PC13, PC14, PC15 and PI8 and Table 67. Output voltage characteristics for PC13, PC14, PC15 and PI8 are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 22. General operating conditions. All I/Os are CMOS and TTL compliant.

Table 66. Output voltage characteristics for all I/Os except PC13, PC14, PC15 and PI8

The IIO current sourced or sunk by the device must always respect the absolute maximum rating specified in Table 19. Voltage characteristics, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣIIO.

Symbol	Parameter	Conditions(1)	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port(2) I_{IO}=8 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port(2) I_{IO}= −8 mA 2.7 V≤ V_{DD} ≤3.6 V	V_{DD}−0.4	-	
V_{OL}(3)	Output low level voltage	TTL port(2) I_{IO}=8 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage	TTL port(2) I_{IO}=-8 mA 2.7 V≤ V_{DD} ≤3.6 V	2.4	-	
V_{OL}(3)	Output low level voltage	I_{IO}=20 mA 2.7 V≤ V_{DD} ≤3.6 V	-	1.3	
V_{OH}(3)	Output high level voltage	I_{IO}=−20 mA 2.7 V≤ V_{DD} ≤3.6 V	V_{DD}−1.3	-	
V_{OL}(3)	Output low level voltage	I_{IO}= 4 mA 1.62 V≤ V_{DD} ≤3.6 V	-	0.4	
V_{OH} (3)	Output high level voltage	I_{IO}= −4 mA 1.62 V≤V_{DD}<3.6 V	V_{DD}−0.4	-	
V_{OLFM+}(3)	Output low level voltage for an FTf I/O pin in FM+ mode	I_{IO}= 20 mA 2.3 V≤ V_{DD}≤3.6 V	-	0.4	
		I_{IO}= 10 mA 1.62 V≤ V_{DD} ≤3.6 V	-	0.4	

1. *The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in Table 19. Voltage characteristics, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.*
2. *TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.*
3. *Guaranteed by design.*

Table 67. Output voltage characteristics for PC13, PC14, PC15 and PI8

Symbol	Parameter	Conditions(1)	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port(2) I_{IO}=3 mA, 2.7 V≤ VDD ≤ 3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port(2) I_{IO}= −3 mA, 2.7 V≤ V_{DD} ≤ 3.6 V	V_{DD}−0.4	-	

Symbol	Parameter	Conditions(1)	Min	Max	Unit
V_{OL} (3)	Output low level voltage	TTL port(2) I_{IO} = 3 mA, 2.7 V≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage	TTL port(2) I_{IO}=−3 mA, 2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL} (3)	Output low level voltage	I_{IO} = 1.5 mA, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH} (3)	Output high level voltage	I_{IO} = −1.5 mA, 1.62 V ≤ V_{DD} < 3.6 V	VDD−0.4	-	

1. *The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in Table 19. Voltage characteristics, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.*
2. *TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.*
3. *Guaranteed by design.*

Output buffer timing characteristics (HSLV option disabled)

The HSLV bit of SYSCFG_CCCSR register can be used to optimize the I/O speed when the product voltage is below 2.7 V.

Table 68. Output timing characteristics (HSLV OFF)

The frequency of the GPIOs that can be supplied in VBAT mode (PC13, PC14, PC15 and PI8) is limited to 2 MHz.

Speed	Symbol	Parameter	conditions	Min(1)	Max(1)	Unit
00	F_{max} (2)	Maximum frequency	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	12	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	3	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	12	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	3	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	16	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	4	
	t_r/t_f (3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	16.6	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	33.3	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	13.3	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	25	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	10	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	20	
01	F_{max} (2)	Maximum frequency	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	60	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	15	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	80	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	15	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	110	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	20	
	t_r/t_f (3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	5.2	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	4.2	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	7.5	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	2.8	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	5.2	

Speed	Symbol	Parameter	conditions	Min(1)	Max(1)	Unit
10	F_{max}(2)	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	85	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	35	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	110	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	40	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	166	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	100	
	t_r/t_f (3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	3.8	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	6.9	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	2.8	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	5.2	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	1.8	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	3.3	
11	F_{max}(2)	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	100	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	50	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	133	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	66	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	220	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	85	
	t_r/t_f (3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	3.3	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	6.6	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	2.4	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	4.5	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	1.5	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	2.7	

1. *Guaranteed by design.*
2. *The maximum frequency is defined with the following conditions: (t_r+t_f) ≤ 2/3 T, skew ≤ 1/20 T, 45%<Duty cycle<55%*
3. *The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.*
4. *Compensation system enabled.*

Output buffer timing characteristics (HSLV option enabled)

Table 69. Output timing characteristics (HSLV ON)

Speed	Symbol	Parameter	conditions	Min(1)	Max(1)	Unit
00	F_{max}(2)	Maximum frequency	C=50 pF, 1.62 V≤VDD≤2.7 V	-	10	MHz
			C=30 pF, 1.62 V≤VDD≤2.7 V	-	10	
			C=10 pF, 1.62 V≤VDD≤2.7 V	-	10	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤VDD≤2.7 V	-	11	ns
			C=30 pF, 1.62 V≤VDD≤2.7 V	-	9	
			C=10 pF, 1.62 V≤VDD≤2.7 V	-	6.6	

Speed	Symbol	Parameter	conditions	Min[1]	Max[1]	Unit
01	F_{max}[2]	Maximum frequency	C=50 pF, 1.62 V≤VDD≤2.7 V	-	50	MHz
			C=30 pF, 1.62 V≤VDD≤2.7 V	-	58	
			C=10 pF, 1.62 V≤VDD≤2.7 V	-	66	
	t_r/t_f[3]	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤VDD≤2.7 V	-	6.6	ns
			C=30 pF, 1.62 V≤VDD≤2.7 V	-	4.8	
			C=10 pF, 1.62 V≤VDD≤2.7 V	-	3	
10	F_{max}[2]	Maximum frequency	C=50 pF, 1.62 V≤VDD≤2.7 V[4]	-	55	MHz
			C=30 pF, 1.62 V≤VDD≤2.7 V[4]	-	80	
			C=10 pF, 1.62 V≤VDD≤2.7 V[4]	-	133	
	t_r/t_f[3]	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤VDD≤2.7 V[4]	-	5.8	ns
			C=30 pF, 1.62 V≤VDD≤2.7 V[4]	-	4	
			C=10 pF, 1.62 V≤VDD≤2.7 V[4]	-	2.4	
11	F_{max}[2]	Maximum frequency	C=50 pF, 1.62 V≤VDD≤2.7 V[4]	-	60	MHz
			C=30 pF, 1.62 V≤VDD≤2.7 V[4]	-	90	
			C=10 pF, 1.62 V≤VDD≤2.7 V[4]	-	175	
	t_r/t_f[3]	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤VDD≤2.7 V[4]	-	5.3	ns
			C=30 pF, 1.62 V≤VDD≤2.7 V[4]	-	3.6	
			C=10 pF, 1.62 V≤VDD≤2.7 V[4]	-	1.9	

1. *Guaranteed by design.*
2. *The maximum frequency is defined with the following conditions: $(t_r+t_f) \leq 2/3\ T$, skew ≤ 1/20 T, 45%<Duty cycle<55%*
3. *The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.*
4. *Compensation system enabled.*

Analog switch between ports Pxy_C and Pxy

PA0_C, PA1_C, PC2_C and PC3_C can be connected internally to PA0, PA1, PC2 and PC3, respectively (refer to SYSCFG_PMCR register in RM0468 reference manual). The switch is controlled by VDDSWITCH voltage level. It is defined through BOOSTVDDSEL bit of SYSCFG_PMCR. If the switch is closed the switch characteristics are given in the table below.

Table 70. Pxy_C and Pxy analog switch characteristics

Parameter	Conditions		Min	Typ	Max	Unit
Switch impedance	Switch control boosted		-	-	315	Ω
	Switch control not boosted	$V_{DDSWITCH}$ > 2.7 V	-	-	315	
		$V_{DDSWITCH}$ > 2.4 V	-	-	335	
		$V_{DDSWITCH}$ > 2.0 V	-	-	390	
		$V_{DDSWITCH}$ > 1.8 V	-	-	445	
		$V_{DDSWITCH}$ > 1.62 V	-	-	550	

6.3.17 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see Table 65. I/O static characteristics).

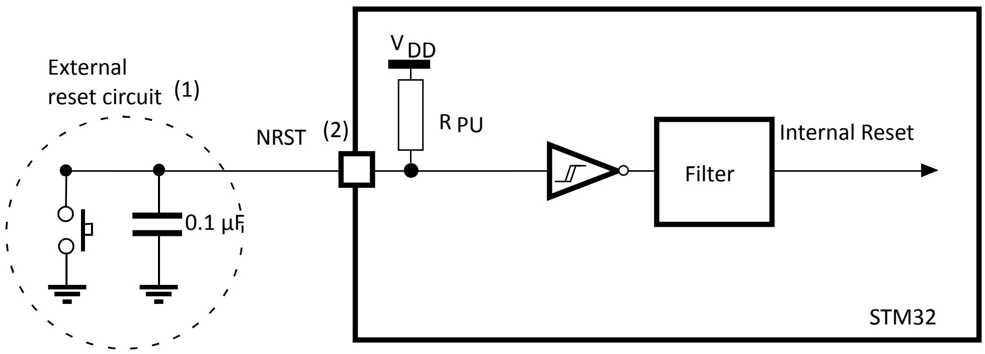
Unless otherwise specified, the parameters given in Table 71. NRST pin characteristics are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in Table 22. General operating conditions.

Table 71. **NRST pin characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}(1)	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	1.71 V < V_{DD} < 3.6 V	-	-	50	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	1.71 V < V_{DD} < 3.6 V	350	-	-	ns
		1.62 V < V_{DD} < 3.6 V	1000	-	-	

1. *Guaranteed by design.*
2. *The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10%).*

Figure 35. **Recommended NRST pin protection**



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in Table 65. I/O static characteristics. Otherwise the reset is not taken into account by the device.

6.3.18 FMC characteristics

Unless otherwise specified, the parameters given in the below tables for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in Table 22. General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS0.

Note: *At VOS1, the performance in some FMC modes can be degraded by up to 5 % compared to VOS0. This is indicated by a footnote when applicable.*

Refer to Section 6.3.16 I/O port characteristics for more details on the input/output alternate function characteristics.

Asynchronous waveforms and timings

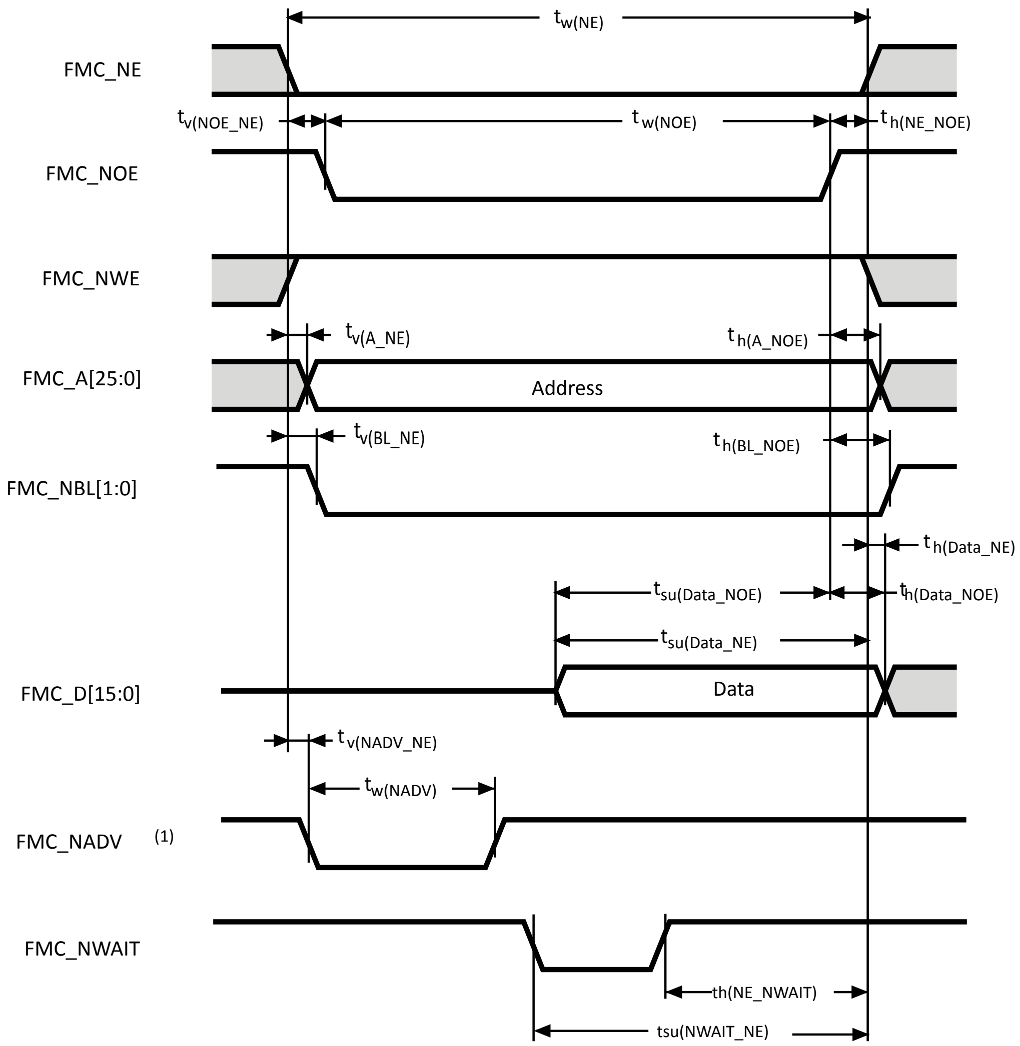
Figure 36 through Figure 38 represent asynchronous waveforms and Table 72 through Table 79 provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode , DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0

- Capacitive load C_L = 30 pF

In all timing tables, $T_{fmc\_ker\_ck}$ is the kernel clock period.

Figure 36. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 72. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings

Symbol	Parameter	Min(1)	Max(1)	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{fmc\_ker\_ck} - 1$	$3T_{fmc\_ker\_ck} + 1$	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	0	0.5	
$t_{w(NOE)}$	FMC_NOE low time	$2T_{fmc\_ker\_ck} - 1$	$2T_{fmc\_ker\_ck} + 1$	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	0	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	13	-	

Symbol	Parameter	Min(1)	Max(1)	Unit
$t_{su(Data\_NOE)}$	Data to FMC_NOEx high setup time	11	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc\_ker\_ck} + 1$	

1. *Guaranteed by characterization results.*

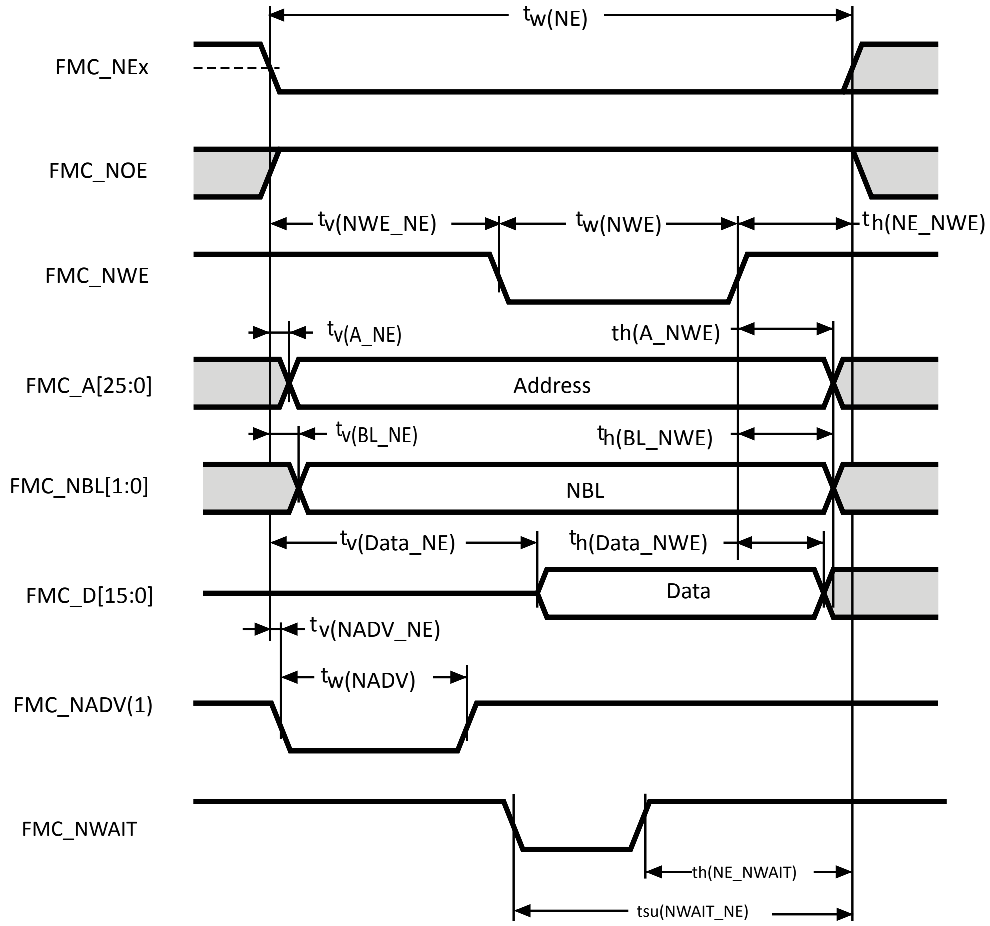
Table 73. Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings

NWAIT pulse width is equal to 1 AHB cycle.

Symbol	Parameter	Min(1)	Max(1)	Unit
$t_{w(NE)}$	FMC_NE low time	$7T_{fmc\_ker\_ck} + 1$	$7T_{fmc\_ker\_ck} + 1$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{fmc\_ker\_ck} - 1$	$5T_{fmc\_ker\_ck} + 1$	
$t_{w(NWAIT)}$	FMC_NWAIT low time	$T_{fmc\_ker\_ck} - 1 - 0.5$	-	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$4T_{fmc\_ker\_ck} + 9$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$3T_{fmc\_ker\_ck} + 12$	-	

1. *Guaranteed by characterization results.*

Figure 37. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 74. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings

Symbol	Parameter	Min[1]	Max[1]	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{fmc\_ker\_ck} - 1$	$3T_{fmc\_ker\_ck} + 1$	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc\_ker\_ck} - 1$	$T_{fmc\_ker\_ck}$	
$t_{w(NWE)}$	FMC_NWE low time	$T_{fmc\_ker\_ck} - 0.5$	$T_{fmc\_ker\_ck} + 0.5$	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc\_ker\_ck}$	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	2	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{fmc\_ker\_ck} - 0.5$	-	
$t_{v(Data\_NE)}$	Data to FMC_NEx low to Data valid	-	$T_{fmc\_ker\_ck} + 3$	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$T_{fmc\_ker\_ck+1}$	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc\_ker\_ck} + 1$	

1. *Guaranteed by characterization results.*

Table 75. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings

NWAIT pulse width is equal to 1 AHB cycle.

Symbol	Parameter	Min[1]	Max[1]	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{fmc\_ker\_ck} - 1$	$8T_{fmc\_ker\_ck} + 1$	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{fmc\_ker\_ck} - 1$	$6T_{fmc\_ker\_ck} + 1$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc\_ker\_ck} + 13$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc\_ker\_ck} + 12$	-	

1. *Guaranteed by characterization results.*

Figure 38. Asynchronous multiplexed PSRAM/NOR read waveforms

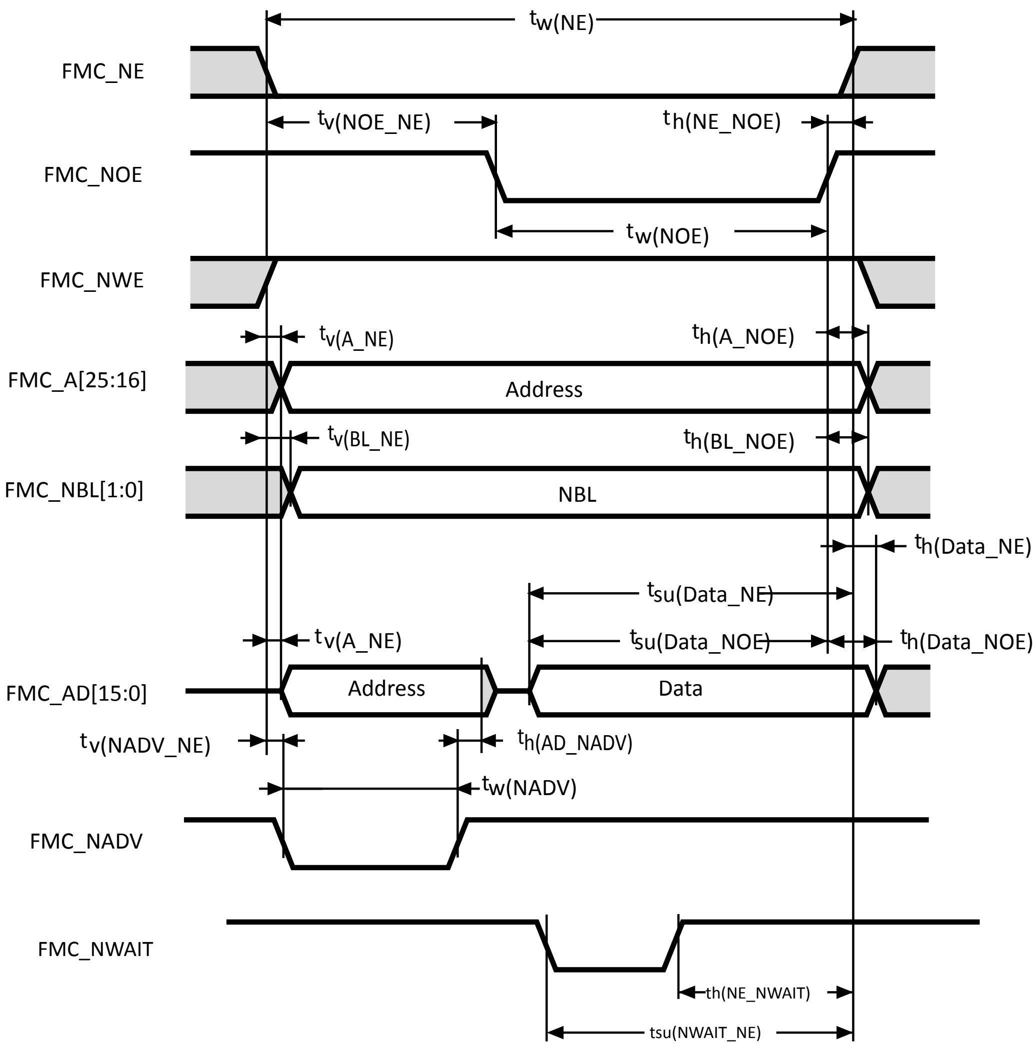


Table 76. Asynchronous multiplexed PSRAM/NOR read timings

Symbol	Parameter	Min[1]	Max[1]	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{fmc\_ker\_ck} - 1$	$4T_{fmc\_ker\_ck} + 1$	ns

Symbol	Parameter	Min(1)	Max(1)	Unit
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{fmc\_ker\_ck}$	$2T_{fmc\_ker\_ck} + 0.5$	ns
$t_{w(NOE)}$	FMC_NOE low time	$T_{fmc\_ker\_ck} - 1$	$T_{fmc\_ker\_ck} + 1$	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc\_ker\_ck} - 0.5$	$T_{fmc\_ker\_ck}+1$	
$t_{h(AD\_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	$T_{fmc\_ker\_ck} - 0.5$	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	13	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOE high setup time	11	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. *Guaranteed by characterization results.*

Table 77. Asynchronous multiplexed PSRAM/NOR read - NWAIT timings

Symbol	Parameter	Min(1)	Max(1)	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{fmc\_ker\_ck} - 1$	$8T_{fmc\_ker\_ck} + 1$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{fmc\_ker\_ck} - 1$	$5T_{fmc\_ker\_ck} + 1$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$4T_{fmc\_ker\_ck} + 9$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc\_ker\_ck} + 12$	-	

1. *Guaranteed by characterization results.*

Table 78. Asynchronous multiplexed PSRAM/NOR write timings

Symbol	Parameter	Min(1)	Max(1)	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{fmc\_ker\_ck} - 1$	$4T_{fmc\_ker\_ck}$	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	Tfmc_ker_c – 1	$T_{fmc\_ker\_ck} + 0.5$	
$t_{w(NWE)}$	FMC_NWE low time	$2T_{fmc\_ker\_ck}- 0.5$	$2T_{fmc\_ker\_ck} + 0.5$	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc\_ker\_ck} - 0.5$	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc\_ker\_ck}$	$T_{fmc\_ker\_ck}+ 1$	
$t_{h(AD\_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{fmc\_ker\_ck} - 0.5$	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{v(Data\_NADV)}$	FMC_NADV high to Data valid	-	$T_{fmc\_ker\_ck} + 2$	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$T_{fmc\_ker\_ck}+0.5$	-	

1. *Guaranteed by characterization results.*

Table 79. **Asynchronous multiplexed PSRAM/NOR write - NWAIT timings**

Symbol	Parameter	Min(1)	Max(1)	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{fmc\_ker\_ck} - 1$	$9T_{fmc\_ker\_ck}$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{fmc\_ker\_ck} - 0.5$	$7T_{fmc\_ker\_ck} + 0.5$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc\_ker\_ck} + 9$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc\_ker\_ck} + 12$	-	

1. *Guaranteed by characterization results.*

Synchronous waveforms and timings

Figure 39 through Figure 42 represent synchronous waveforms and Table 80 through Table 83 provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR flash; DataLatency = 0 for PSRAM

In all timing tables, $T_{fmc\_ker\_ck}$ is the kernel clock period, with the following FMC_CLK maximum values:

- For 2.7 V < V_{DD} < 3.6 V, FMC_CLK = 125 MHz at 20 pF
- For 1.8 V < V_{DD} < 1.9 V, FMC_CLK = 100 MHz at 20 pF
- For 1.62 V < V_{DD}<1.8 V, FMC_CLK = 100 MHz at 15 pF

Figure 39. Synchronous multiplexed NOR/PSRAM read timings

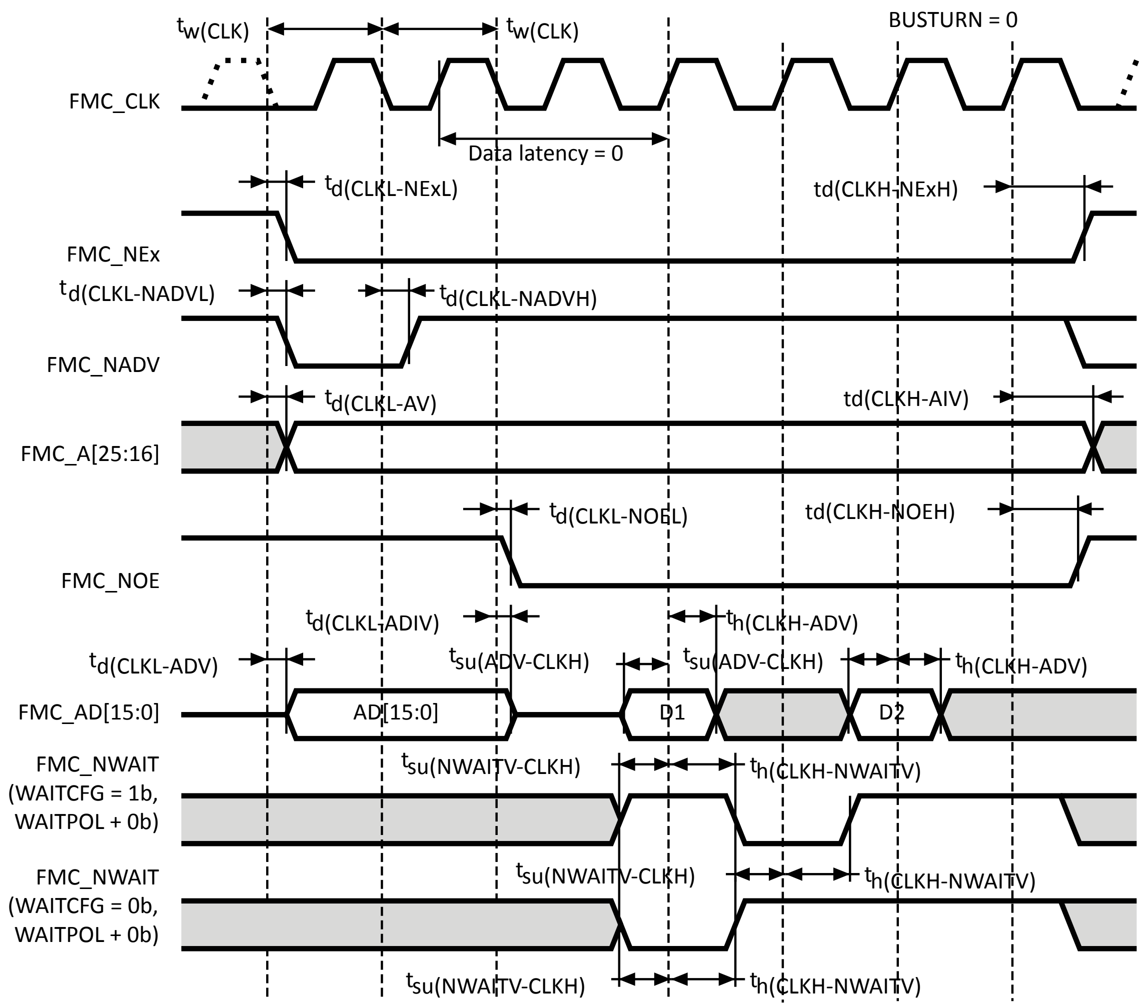


Table 80. Synchronous multiplexed NOR/PSRAM read timings

Symbol	Parameter	Min[1]	Max[1][2]	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{fmc\_ker\_ck} - 0.5$	-	ns
$t_{d(CLKL\text{-}NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH\_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{fmc\_ker\_ck}+1.5$	-	
$t_{d(CLKL\text{-}NADVL)}$	FMC_CLK low to FMC_NADV low	-	1	
$t_{d(CLKL\text{-}NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL\text{-}AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2.0	
$t_{d(CLKH\text{-}AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$T_{fmc\_ker\_ck}+1.5$	-	
$t_{d(CLKL\text{-}NOEL)}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(CLKH\text{-}NOEH)}$	FMC_CLK high to FMC_NOE high	$T_{fmc\_ker\_ck} +1.5$	-	
$t_{d(CLKL\text{-}ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(CLKL\text{-}ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(ADV\text{-}CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	3	-	

Symbol	Parameter	Min[1]	Max[1][2]	Unit
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	0.5	-	ns
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1	-	

1. *Guaranteed by characterization results.*
2. *At VOS1, these values are degraded by up to 5 %.*

Figure 40. Synchronous multiplexed PSRAM write timings

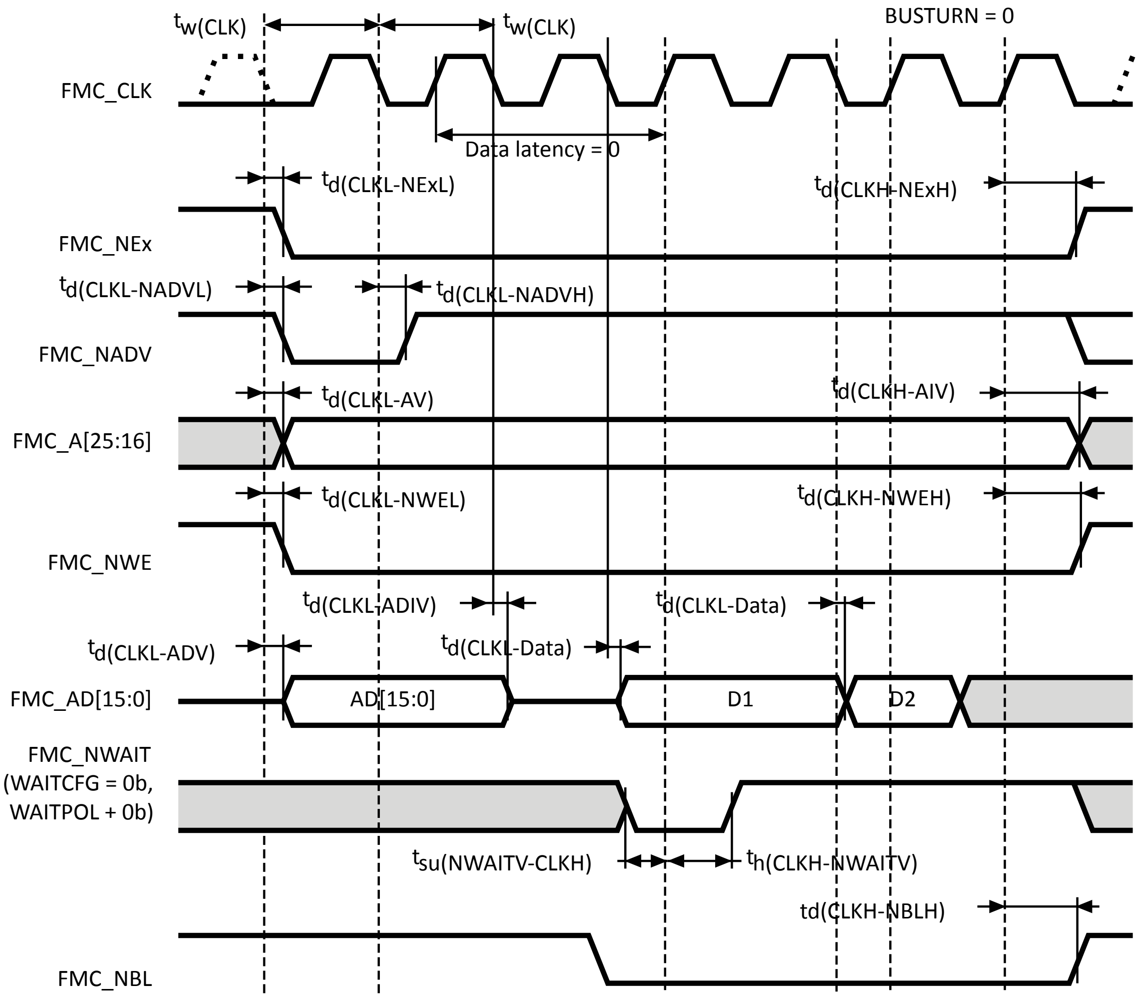


Table 81. Synchronous multiplexed PSRAM write timings

Symbol	Parameter	Min[1]	Max[1][2]	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{fmc\_ker\_ck} - 1$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x =0..2)	-	2	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x = 0…2)	$T_{fmc\_ker\_ck} + 1.5$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.5	

Symbol	Parameter	Min(1)	Max(1)(2)	Unit
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	ns
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x =16…25)	-	2	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x =16…25)	$T_{fmc\_ker\_ck}$ +1.5	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{fmc\_ker\_ck}$ +1	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to to FMC_AD[15:0] valid	-	2.5	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	3	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	2	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$T_{fmc\_ker\_ck}$ +0.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	2	-	

1. *Guaranteed by characterization results.*
2. *At VOS1, these values are degraded by up to 5 %.*

Figure 41. Synchronous non-multiplexed NOR/PSRAM read timings

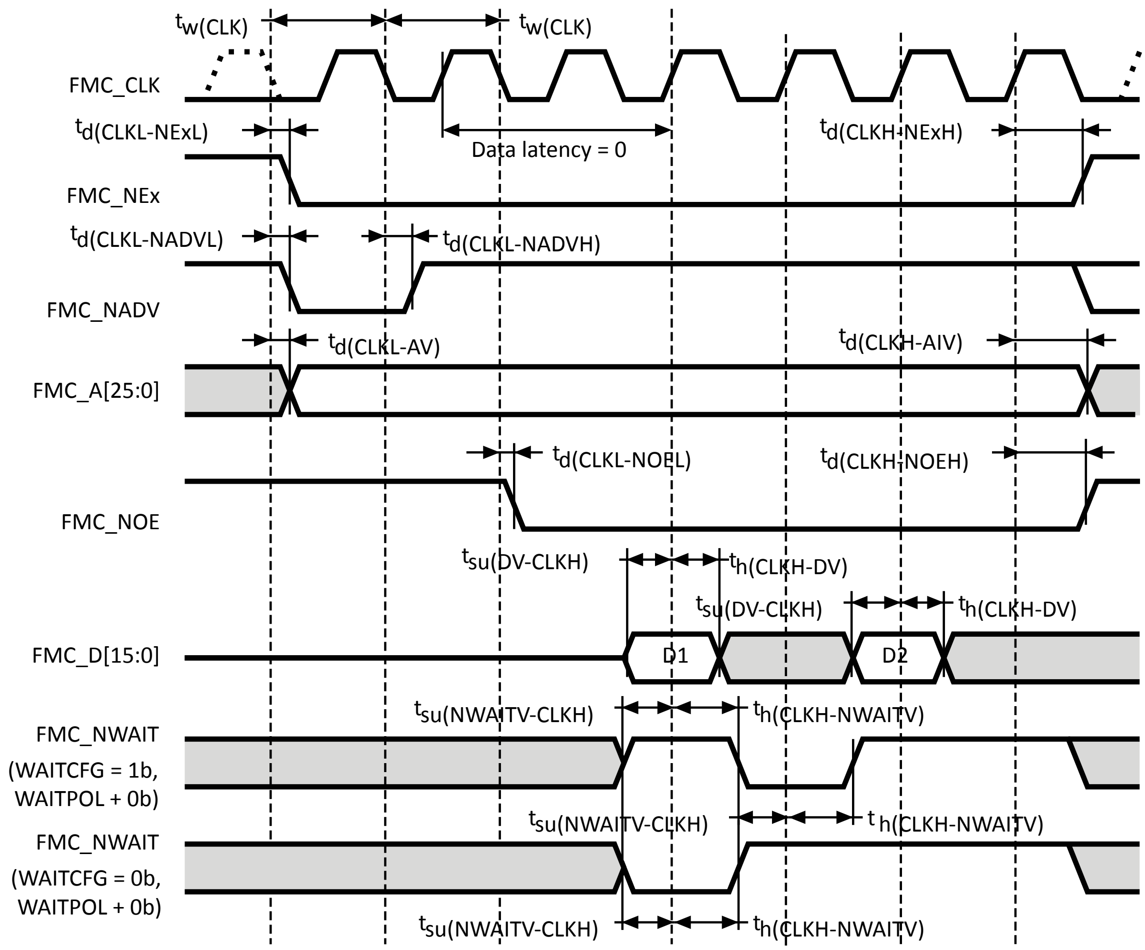


Table 82. Synchronous non-multiplexed NOR/PSRAM read timings

Symbol	Parameter	Min[1]	Max[1][2]	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{fmc\_ker\_ck}$ –0.5	-	ns
$t_{(CLKL\text{-}NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH\text{-}NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{fmc\_ker\_ck}$+1.5	-	
$t_{d(CLKL\text{-}NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL\text{-}NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL\text{-}AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH\text{-}AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$T_{fmc\_ker\_ck}$+1.5	-	
$t_{d(CLKL\text{-}NOEL)}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(CLKH\text{-}NOEH)}$	FMC_CLK high to FMC_NOE high	$T_{fmc\_ker\_ck}$+1	-	
$t_{su(DV\text{-}CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	3	-	
$t_{h(CLKH\text{-}DV)}$	FMC_D[15:0] valid data after FMC_CLK high	0.5	-	
$t_{(NWAIT\text{-}CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	

Symbol	Parameter	Min(1)	Max(1)(2)	Unit
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1	-	ns

1. *Guaranteed by characterization results.*
2. *At VOS1, these values are degraded by up to 5 %.*

Figure 42. Synchronous non-multiplexed PSRAM write timings

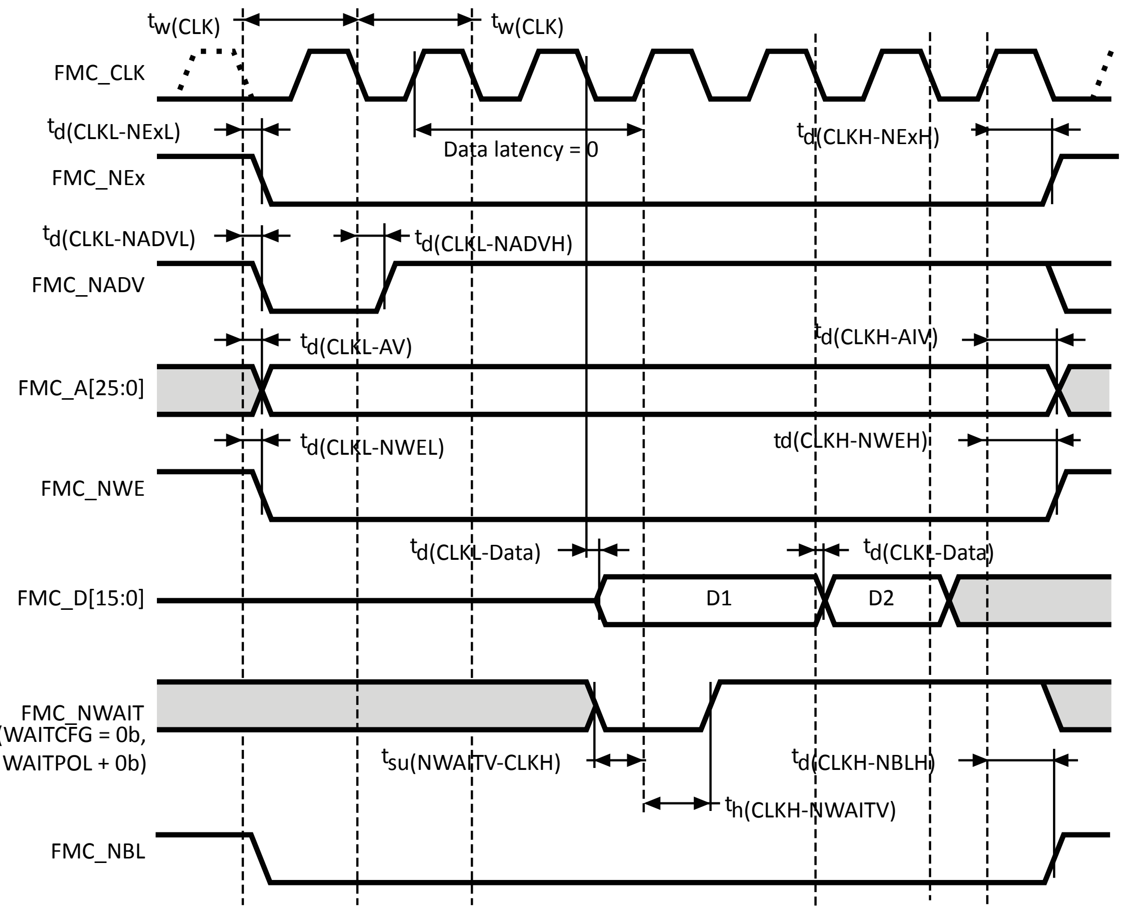


Table 83. Synchronous non-multiplexed PSRAM write timings

Symbol	Parameter	Min(1)	Max(1)(2)	Unit
$t_{(CLK)}$	FMC_CLK period	$2T_{fmc\_ker\_ck} - 0.5$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{fmc\_ker\_ck} + 1.5$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$T_{fmc\_ker\_ck} + 1.5$	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{fmc\_ker\_ck} + 1$	-	

Symbol	Parameter	Min(1)	Max(1)(2)	Unit
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	3	ns
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	2	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$T_{fmc\_ker\_ck}$ + 0.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	2	-	

1. *Guaranteed by characterization results.*
2. *At VOS1, these values are degraded by up to 5 %.*

NAND controller waveforms and timings

Figure 43 through Figure 46 represent synchronous waveforms, and Table 84 and Table 85 provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01
- COM.FMC_WaitSetupTime = 0x03
- COM.FMC_HoldSetupTime = 0x02
- COM.FMC_HiZSetupTime = 0x01
- ATT.FMC_SetupTime = 0x01
- ATT.FMC_WaitSetupTime = 0x03
- ATT.FMC_HoldSetupTime = 0x02
- ATT.FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0
- Capacitive load C_L = 30 pF

In all timing tables, $T_{fmc\_ker\_ck}$ is the kernel clock period.

Figure 43. NAND controller waveforms for read access

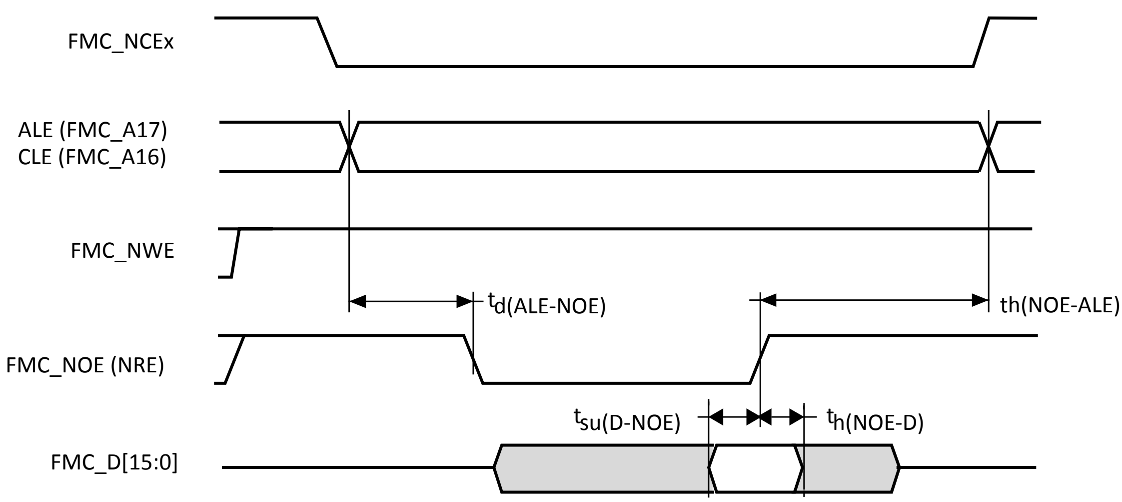


Figure 44. NAND controller waveforms for write access

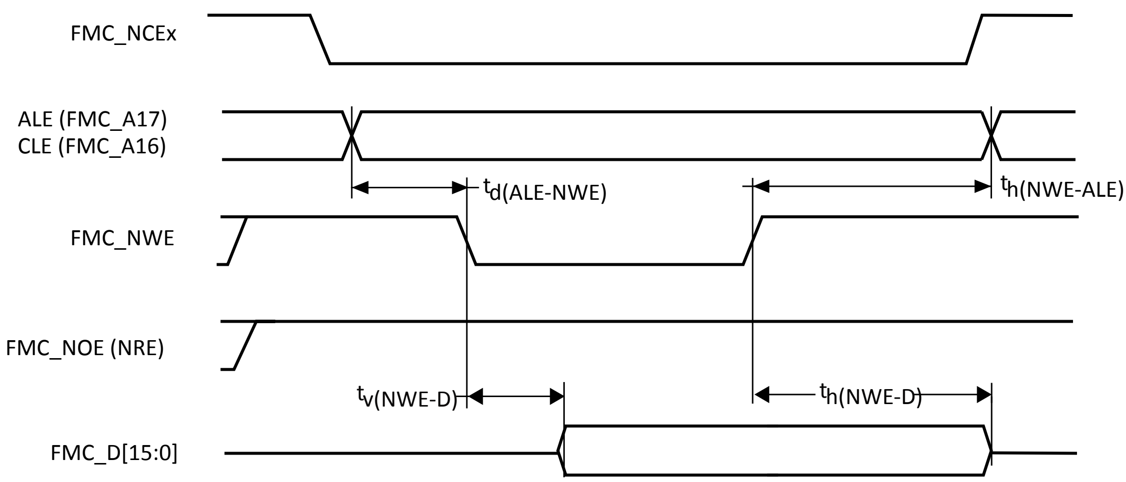


Figure 45. NAND controller waveforms for common memory read access

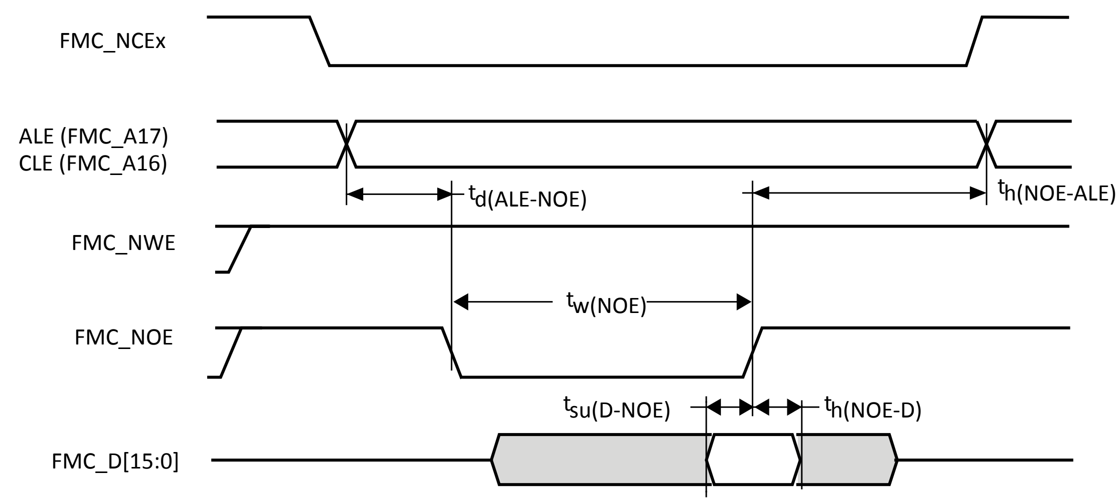


Figure 46. NAND controller waveforms for common memory write access

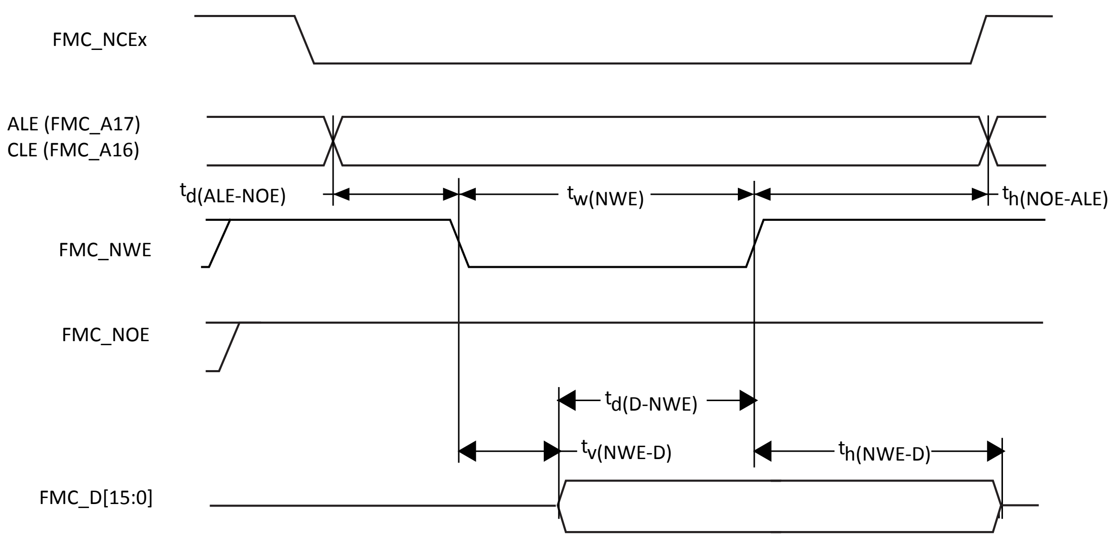


Table 84. Switching characteristics for NAND flash memory read cycles

Symbol	Parameter	Min[1]	Max[1]	Unit
$t_{w(N0E)}$	FMC_NOE low width	$4T_{fmc\_ker\_ck} - 0.5$	$4T_{fmc\_ker\_ck}+0.5$	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	8	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	$3T_{fmc\_ker\_ck} +0.5$	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$4T_{fmc\_ker\_ck} -1$	-	

1. *Guaranteed by characterization results.*

Table 85. Switching characteristics for NAND flash write cycles

Symbol	Parameter	Min[1]	Max[1]	Unit
$t_{w(NWE)}$	FMC_NWE low width	$4T_{fmc\_ker\_ck} - 0.5$	$4T_{fmc\_ker\_ck} +0.5$	ns
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	0	-	
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$2T_{fmc\_ker\_ck} + 1.5$	-	
$t_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$5T_{fmc\_ker\_ck} - 2$	-	
$t_{d(ALE-NWE)}$	FMC_ALE valid before FMC_NWE low	-	$3T_{fmc\_ker\_ck} +0.5$	
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$2T_{fmc\_ker\_ck} + 0.5$	-	

1. *Guaranteed by characterization results.*

SDRAM waveforms and timings

In all timing tables, $T_{fmc\_ker\_ck}$ is the kernel clock period, with the following FMC_SDCLK maximum values:

- For 2.7 V < V_{DD} <3.6 V: FMC_CLK =110 MHz at 20 pF
- For 1.8 V < V_{DD} <1.9 V: FMC_CLK =100 MHz at 20 pF
- For 1.62 V <$_{DD}$ <1.8 V, FMC_CLK =100 MHz at 15 pF

Figure 47. SDRAM read access waveforms (CL = 1)

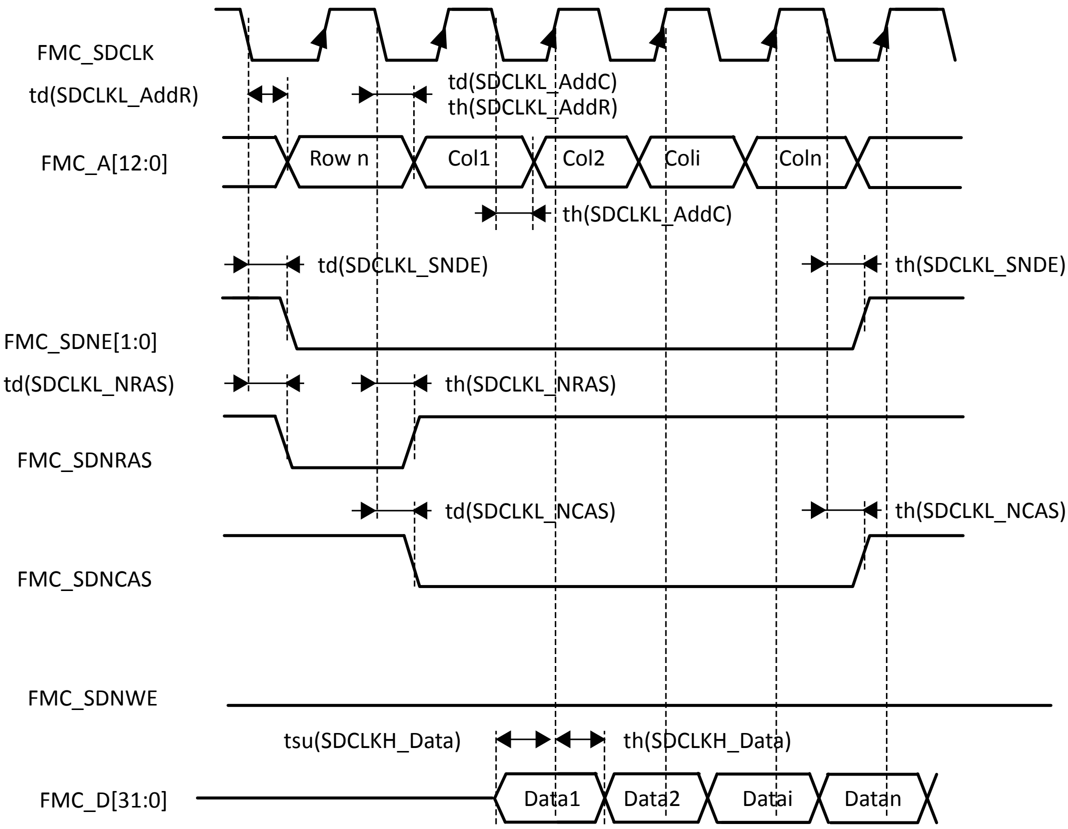


Table 86. SDRAM read timings

Symbol	Parameter	Min(1)	Max(1)(2)	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{fmc\_ker\_ck} - 1$	$2T_{fmc\_ker\_ck} + 0.5$	ns
$t_{su(SDCLKH\_Data)}$	Data input setup time	3	-	
$t_{h(SDCLKH\_Data)}$	Data input hold time	0	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL-SDNE)}$	Chip select valid time	-	2(3)	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	0.5	-	
$t_{d(SDCLKL\_SDNRAS)}$	SDNRAS valid time	-	2	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0.5	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	0.5	
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0	-	

1. *Guaranteed by characterization results.*
2. *At VOS1, these values are degraded by up to 5 %.*
3. *Using PC2_C I/O adds 4.5 ns to this timing.*

Table 87. **LPSDR SDRAM read timings**

Symbol	Parameter	Min[1]	Max[1][2]	Unit
$t_{W(SDCLK)}$	FMC_SDCLK period	$2T_{fmc\_ker\_ck} - 1$	$2T_{fmc\_ker\_ck}+0.5$	ns
$t_{su(SDCLKH\_Data)}$	Data input setup time	3	-	
$t_{h(SDCLKH\_Data)}$	Data input hold time	0.5	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	3.5	
$t_{d(SDCLKL\_SDNE)}$	Chip select valid time	-	2.5[3]	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL\_SDNRAS}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0	-	

1. *Guaranteed by characterization results.*
2. *At VOS1, these values are degraded by up to 5 %.*
3. *Using PC2_C I/O adds 16.5 ns to this timing.*

Figure 48. **SDRAM write access waveforms**

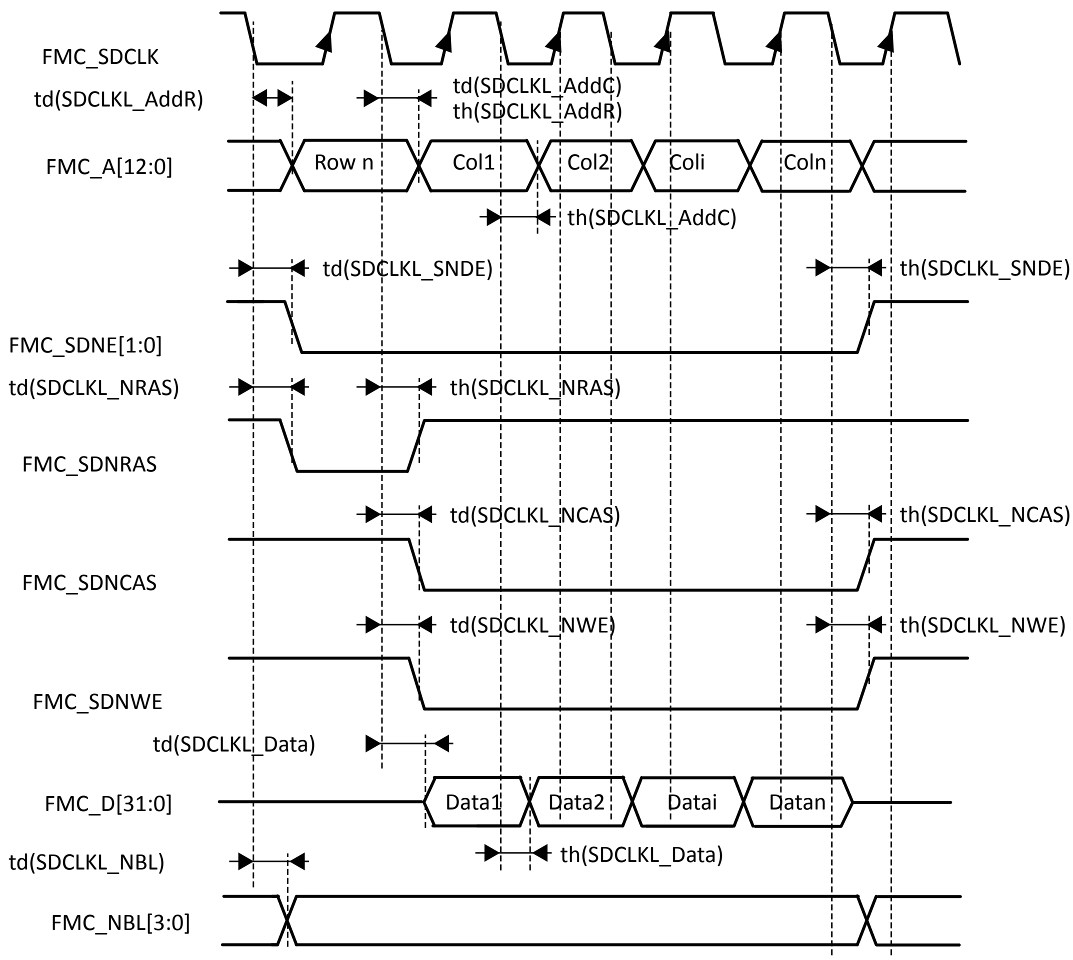


Table 88. **SDRAM write timings**

Symbol	Parameter	Min(1)	Max(1)(2)	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{fmc\_ker\_ck} - 1$	$2T_{fmc\_ker\_ck}+0.5$	ns
$t_{d(SDCLKL\ \_Data)}$	Data output valid time	-	2.5	
$t_{h(SDCLKL\ \_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	2	
$t_{d(SDCLKL\_SDNWE)}$	SDNWE valid time	-	2.5	
$t_{h(SDCLKL\_SDNWE)}$	SDNWE hold time	0.5	-	
$t_{d(SDCLKL\_\ SDNE)}$	Chip select valid time	-	2(3)	
$t_{h(SDCLKL-\_SDNE)}$	Chip select hold time	0.5	-	
$t_{d(SDCLKL\_SDNRAS)}$	SDNRAS valid time	-	1.5	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0.5	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0.5	-	

1. *Guaranteed by characterization results.*
2. *At VOS1, these values are degraded by up to 5 %.*
3. *Using PC2_C I/O adds 4.5 ns to this timing.*

Table 89. **LPSDR SDRAM write timings**

Symbol	Parameter	Min(1)	Max(1)(2)	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{fmc\_ker\_ck} - 1$	$2T_{fmc\_ker\_ck}+0.5$	ns
$t_{d(SDCLKL\ \_Data)}$	Data output valid time	-	2.5	
$t_{h(SDCLKL\ \_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	2.5	
$t_{d(SDCLKL-SDNWE)}$	SDNWE valid time	-	3	
$t_{h(SDCLKL-SDNWE)}$	SDNWE hold time	0	-	
$t_{d(SDCLKL-\ SDNE)}$	Chip select valid time	-	3(3)	
$t_{h(SDCLKL-\ SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL-SDNRAS)}$	SDNRAS valid time	-	2	
$t_{h(SDCLKL-SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS valid time	-	2	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS hold time	0	-	

1. *Guaranteed by characterization results.*
2. *At VOS1, these values are degraded by up to 5 %.*
3. *Using PC2_C I/O adds 16.5 ns to this timing.*

6.3.19 Octo-SPI interface characteristics

Unless otherwise specified, the parameters given in Table 90. OCTOSPI characteristics in SDR mode and Table 91. OCTOSPI characteristics in DTR mode (with DQS)/Octal and Hyperbus for the OCTOSPI interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in Table 22. General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- I/O compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS0

Note: At VOS1, the performance can be degraded by up to 5 % compared to VOS0. This is indicated by a footnote when applicable.

Refer to Section 6.3.16 I/O port characteristics for more details on the input/output alternate function characteristics.

Table 90. OCTOSPI characteristics in SDR mode

Delay block bypassed.

Symbol	Parameter	Conditions	Min(1)(2)	Typ(1)(2)	Max(1)(2)(3)	Unit
$F_{(CLK)}$	OCTOSPI clock frequency	1.62 V < V_{DD} < 3.6 V, VOS0, C_{LOAD} = 15 pF	-	-	90	MHz
		1.62 V < V_{DD} < 3.6 V, VOS0, C_{LOAD} = 20 pF	-	-	80	
		2.7 V < V_{DD} < 3.6 V, VOS0, C_{LOAD} = 20 pF	-	-	140	
$t_{w(CLKH)}$	OCTOSPI clock high and low time	PRESCALER[7:0] = n = 0,1,3,5	$t_{(CLK)}/2$	-	$t_{(CLK)}/2+1$	ns
$t_{w(CLKL)}$			$t_{(CLK)}/2-1$	-	$t_{(CLK)}/2$	
$t_{w(CLKH)}$	OCTOSPI clock high and low time	PRESCALER[7:0] = n = 2,4,6,8	$(n/2)*t_{(CLK)}/(n+1)$	-	$(n/2)*t_{(CLK)}/(n+1)+1$	
$t_{w(CLKL)}$			$(n/2+1)*t_{(CLK)}/(n+1)-1$	-	$(n/2+1)*t_{(CLK)}/(n+1)$	
$t_{s(IN)}$ (4)	Data input setup time	2.7 V < V_{DD} < 3.6 V	2	-	-	
		1.62 V < V_{DD} < 3.6 V	2	-	-	
$t_{h(IN)}$ (4)	Data input hold time	2.7 V < V_{DD} < 3.6 V	4.5	-	-	
		1.62 V < V_{DD} < 3.6 V	5	-	-	
$t_{v(OUT)}$	Data output valid time	-	-	1	1.5(4)	
$t_{h(OUT)}$	Data output hold time	-	0	-	-	

1. *All values apply to Octal and Quad-SPI mode.*
2. *Guaranteed by characterization results.*
3. *At VOS1, these values are degraded by up to 5 %.*
4. *Using PC2, PC3, PI11, PF0 or PF1 I/O in the data bus adds 3.5 ns to this timing value.*

Figure 49. OctoSPI timing diagram - SDR mode

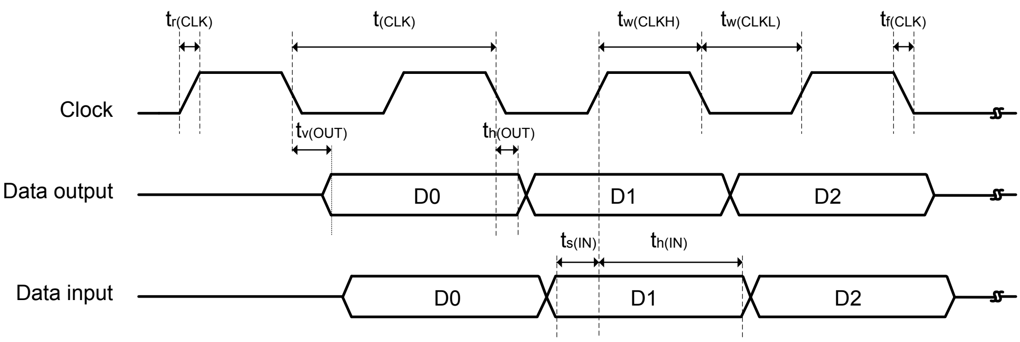


Table 91. OCTOSPI characteristics in DTR mode (with DQS)/Octal and Hyperbus

Symbol	Parameter	Conditions	Min[1]	Typ[1]	Max[1][2]	Unit
$F_{(CLK)}$[3][4]	OCTOSPI clock frequency	1.71 V < V_{DD} < 3.6 V, VOS0, C_{LOAD} = 15 pF	-	-	120[5]	MHz
		2.7 V < V_{DD} < 3.6 V, VOS0, C_{LOAD} = 20 pF	-	-	100	
		1.62 V < V_{DD} < 2.5 V, VOS0, C_{LOAD} = 20 pF	-	-	100/45[6]	
$t_{w(CLKH)}$	OCTOSPI clock high and low time	PRESCALER[7:0] = n = 0,1,3,5	$t_{(CLK)}/2$	-	$t_{(CLK)}/2+1$	ns
$t_{w(CLKL)}$			$t_{(CLK)}/2-1$	-	$t_{(CLK)}/2$	
$t_{w(CLKH)}$	OCTOSPI clock high and low time	PRESCALER[7:0] = n = 2,4,6,8	$(n/2)*t_{(CLK)}/(n+1)$	-	$(n/2)*t_{(CLK)}/(n+1)+1$	
$t_{w(CLKL)}$			$(n/2+1)*t_{(CLK)}/(n+1)-1$	-	$(n/2+1)*t_{(CLK)}/(n+1)$	
$t_{v(CLK)}$	Clock valid time	-	-	-	$t_{(CLK)}+1$	
$t_{h(CLK)}$	Clock hold time	-	$t_{(CLK)}/2-0.5$ $t_{(CLK)}/2$	-	-	
$t_{w(CS)}$	Chip select high time	-	3 x $t_{(CLK)}$	-	-	
$t_{v(DQ)}$	Data input vallid time	-	0	-	-	
$t_{v(DS)}$	Data strobe input valid time	-	0	-	-	
$t_{h(DS)}$	Data strobe input hold time	-	0	-	-	
$t_{v(RWDS)}$	Data strobe output valid time	-	-	-	3 x $t_{(CLK)}$	
$t_{sr(DQ)}$ $t_{sf(DQ)}$[7]	Data input setup time	-	−1	-	-	
$t_{hr(DQ)}$	Data input hold time	Rising edge	3	-	-	
$t_{hf(DQ)}$[7]		Falling edge	3.5	-	-	
$t_{vr(OUT)}$ $t_{vf(OUT)}$	Data output valid time	DHQC = 0	-	5.5	7[8]	
		DHQC = 1, PRESCALER[7:0]=1,2...	-	$t_{(CLK)}/4+1$	$t_{(CLK)}/4+2$[8]	
$t_{hr(OUT)}$ $t_{hf(OUT)}$	Data output hold time	DHQC = 0	4.5	-	-	

Symbol	Parameter	Conditions	Min[1]	Typ[1]	Max[1][2]	Unit
$t_{hr(OUT)}$ $t_{hf(OUT)}$	Data output hold time	DHQC = 1, PRESCALER[7:0]=1,2...	$t_{(CLK)}/4$	-	-	ns

1. *Guaranteed by characterization results, unless otherwise specified.*
2. *At VOS1, these values are degraded by up to 5 %.*
3. *The maximum frequency values are given for a maximum RWDS to DQ skew ≤ ±1.0 ns.*
4. *DHQC must be set to reach the mentioned frequency.*
5. *Guaranteed by design.*
6. *Using PC2, PC3, PI11, PF0 or PF1 I/Os limits the maximum clock frequency.*
7. *Delay block bypassed.*
8. *Using PC2, PC3, PI11, PF0 or PF1 I/O in the data bus adds 3.5 ns to this timing value.*

Figure 50. OctoSPI timing diagram - DTR mode

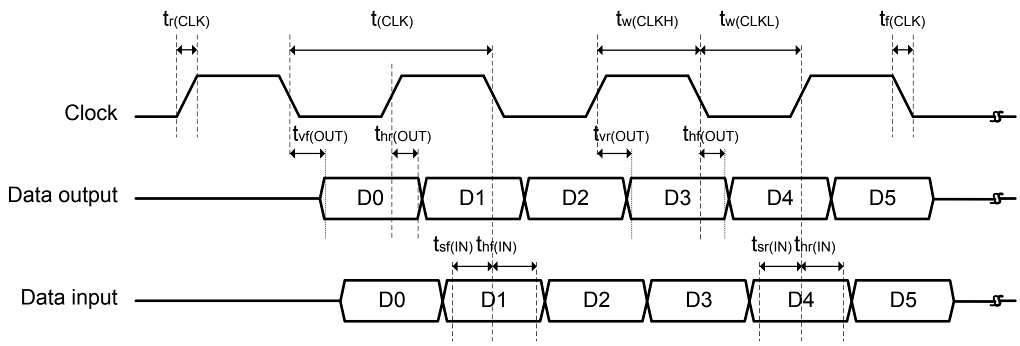


Figure 51. OctoSPI Hyperbus clock

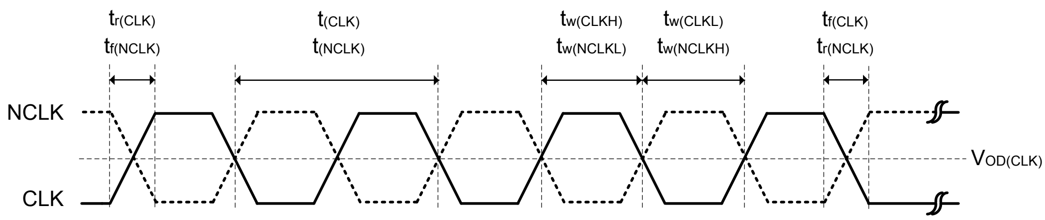


Figure 52. OctoSPI Hyperbus read

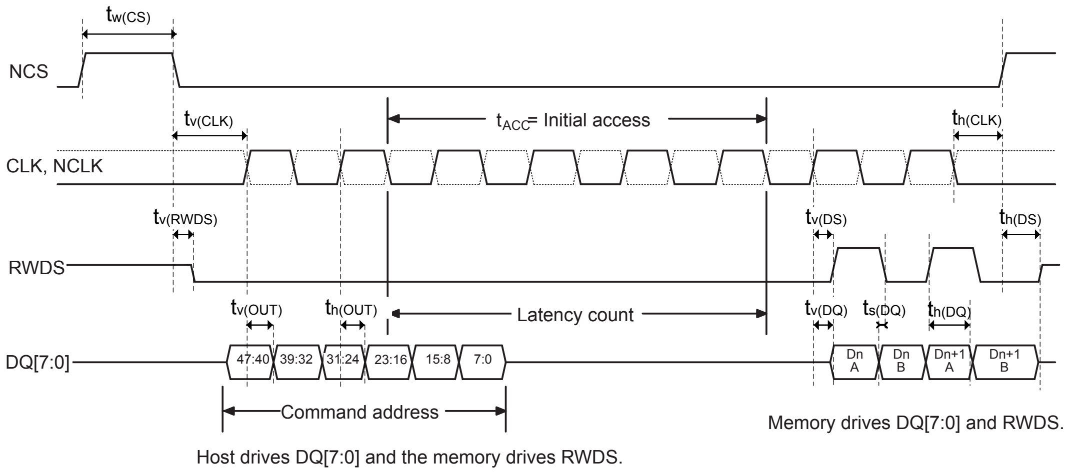
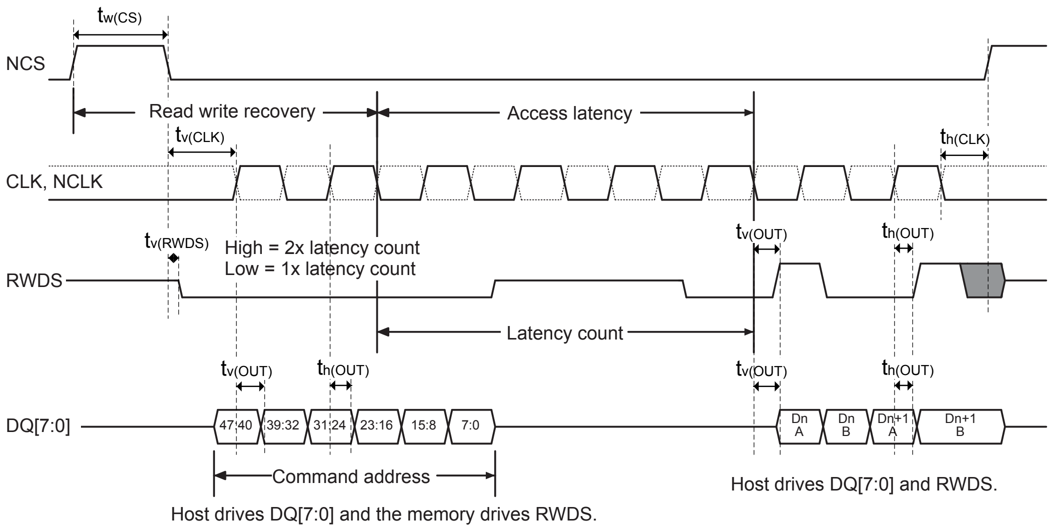


Figure 53. OctoSPI Hyperbus write



6.3.20 Delay block (DLYB) characteristics

Unless otherwise specified, the parameters given in Table 92. Delay Block characteristics for Delay Block are derived from tests performed under the ambient temperature, $f_{rcc\_cpu\_ck}$ frequency and VDD supply voltage summarized in Table 22. General operating conditions, with the following configuration:

Table 92. Delay Block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{init}	Initial delay	-	1400	1700	2700	ps
t_{Δ}	Unit Delay	-	40	47	59	

6.3.21 16-bit ADC characteristics

Unless otherwise specified, the parameters given in Table 93. ADC characteristics are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in Table 22. General operating conditions.

Table 93. ADC characteristics

Symbol	Parameter	Conditions		Min(1)	Typ(1)	Max(1)	Unit
V_{DDA}	Analog power supply for ADC ON	-		1.62	-	3.6	V
V_{REF+}(2)	Positive reference voltage	$V_{DDA} \geq 2$ V		1.62	-	V_{DDA}	
		$V_{DDA} < 2$ V		V_{DDA}			
V_{REF-}(2)	Negative reference voltage	-		V_{SSA}			
f_{ADC}	ADC clock frequency	1,62 V $\leq V_{DDA} \leq$ 3.6 V	BOOST = 11	0.12	-	50	MHz
			BOOST = 10	0.12	-	25	
			BOOST = 01	0.12	-	12.5	
			BOOST = 00	-	-	6.25	

Symbol	Parameter	Conditions				Min[1]	Typ[1]	Max[1]	Unit
f_S[3]	Sampling rate for Direct channels	Resolution = 16 bits, V_{DDA} > 2.5 V	T_J = 90 °C	f_{ADC} = 36 MHz	SMP = 1.5	-	-	3.60	MSPS
		Resolution = 16 bits		f_{ADC} = 37 MHz	SMP = 2.5	-	-	3.35	
		Resolution = 14 bits	T_J = 125 °C	f_{ADC} = 50 MHz	SMP = 2.5	-	-	5.00	
		Resolution = 12 bits		f_{ADC}=50 MHz	SMP = 2.5	-	-	5.50	
		Resolution = 10 bits		f_{ADC}=50 MHz	SMP=1.5	-	-	7.10	
		Resolution = 8 bits		f_{ADC}=50 MHz	SMP=1.5	-	-	8.30	
	Sampling rate for Fast channels	Resolution = 16 bits, V_{DDA}>2.5V	T_J = 90 °C	f_{ADC}=32 MHz	SMP=2.5	-	-	2.90	
		Resolution = 16 bits		f_{ADC}=31 MHz	SMP=2.5	-	-	2.80	
		Resolution = 14 bits	TJ = 125°C	f_{ADC}=33 MHz	SMP=2.5	-	-	3.30	
		Resolution = 12 bits		f_{ADC}=39 MHz	SMP=2.5	-	-	4.30	
		Resolution = 10 bits		f_{ADC}=48 MHz	SMP=2.5	-	-	6.00	
		Resolution = 8 bits		f_{ADC}=50 MHz	SMP=2.5	-	-	7.10	
	Sampling rate for Slow channels, BOOST = 00, f_{ADC} = 10 MHz	Resolution = 16 bits	T_J = 90 °C	f_{ADC}=10 MHz	SMP=1.5	-	-	1.00	
		Resolution = 14 bits	T_J = 125 °C			-	-		
		Resolution = 12 bits				-	-		
		Resolution = 10 bits				-	-		
		Resolution = 8 bits				-	-		
t_{TRIG}	External trigger period	Resolution = 16 bits				-	-	10	$1/f_{ADC}$
V_{AIN}[4]	Conversion voltage range	-				0	-	V_{REF+}	V
V_{CMIV}	Common mode input voltage	-				$V_{REF}/2$ − 10%	$V_{REF}/2$	$V_{REF}/2$ + 10%	V
R_{AIN}[5]	External input impedance	Resolution = 16 bits, T_J = 125 °C				-	-	170	Ω
		Resolution = 14 bits, T_J= 125 °C				-	-	435	
		Resolution = 12 bits, TJ$_J$ = 125 °C				-	-	1150	
		Resolution = 10 bits, T_J = 125 °C				-	-	5650	
		Resolution = 8 bits, T_J = 125 °C				-	-	26500	
C_{ADC}	Internal sample and hold capacitor	-				-	4	-	pF
$t_{ADCVREG\_STUP}$	ADC LDO startup time	-				-	5	10	µs

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
t_{STAB}	ADC power-up time	LDO already started	1	-	-	conversion cycle
t_{CAL}	Offset and linearity calibration time	-	165010			$1/f_{ADC}$
t_{OFF_CAL}	Offset calibration time	-	1280			
t_{LATR}	Trigger conversion latency for regular and injected channels without aborting the conversion	CKMODE = 00	1.5	2	2.5	
		CKMODE = 01	-	-	2.5	
		CKMODE = 10	-	-	2.5	
		CKMODE = 11	-	-	2.25	
$t_{LATRINJ}$	Trigger conversion latency for regular and injected channels when a regular conversion is aborted	CKMODE = 00	2.5	3	3.5	
		CKMODE = 01	-	-	3.5	
		CKMODE = 10	-	-	3.5	
		CKMODE = 11	-	-	3.25	
t_S	Sampling time	-	1.5	-	810.5	
t_{CONV}	Total conversion time (including sampling time)	N-bits resolution	tS + 0.5 + N/2	-	-	
$I_{DDA\_D(ADC)}$	ADC consumption on V_{DDA}, BOOST=11, Differential mode	Resolution = 16 bits, f_{ADC}=25 MHz	-	1440	-	µA
		Resolution = 14 bits, f_{ADC}=30 MHz	-	1350	-	
		Resolution = 12 bits, f_{ADC}=40 MHz	-	990	-	
	ADC consumption on V_{DDA}, BOOST=10, Differential mode f_{ADC}=25 MHz	Resolution = 16 bits	-	1080	-	
		Resolution = 14 bits	-	810	-	
		Resolution = 12 bits	-	585	-	
	ADC consumption on V_{DDA}, BOOST=01, Differential mode f_{ADC}=12.5 MHz	Resolution = 16 bits	-	630	-	
		Resolution = 14 bits	-	432	-	
		Resolution = 12 bits	-	315	-	
	ADC consumption on V_{DDA}, BOOST=00, Differential mode f_{ADC}=6.25 MHz	Resolution = 16 bits	-	360	-	
		Resolution = 14 bits	-	270	-	
		Resolution = 12 bits	-	225	-	
$I_{DDA\_SE(ADC)}$	ADC consumption on V_{DDA}, BOOST=11, Single-ended mode	Resolution = 16 bits, f_{ADC}=25 MHz	-	720	-	µA
		Resolution = 14 bits, f_{ADC}=30 MHz	-	675	-	
		Resolution = 12 bits, f_{ADC}=40 MHz	-	495	-	
	ADC consumption on V_{DDA}, BOOST=10, Single-ended mode f_{ADC}=25 MHz	Resolution = 16 bits	-	540	-	
		Resolution = 14 bits	-	405	-	
		Resolution = 12 bits	-	292.5	-	
	ADC consumption on V_{DDA}, BOOST=01, Single-ended mode f_{ADC}=12.5 MHz	Resolution = 16 bits	-	315	-	
		Resolution = 14 bits	-	216	-	
		Resolution = 12 bits	-	157.5	-	
	ADC consumption on V_{DDA}, BOOST=00, Single-ended mode f_{ADC}=6.25 MHz	Resolution = 16 bits	-	180	-	
		Resolution = 14 bits	-	135	-	
		Resolution = 12 bits	-	112.5	-	
$I_{DD(ADC)}$	ADC consumption on V_{DD}	f_{ADC}=50 MHz	-	400	-	

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
$I_{DD(ADC)}$	ADC consumption on V_{DD}	f_{ADC}=25 MHz	-	220	-	µA
		f_{ADC}=12.5 MHz	-	180	-	
		f_{ADC}=6.25 MHz	-	120	-	
		f_{ADC}=3.125 MHz	-	80	-	

1. *Guaranteed by design.*
2. *Depending on the package, V_{REF+} can be internally connected to V_{DDA} and V_{REF-} to V_{SSA}.*
3. *These values are valid UFBGA176+25 and one ADC. The values for other packages and multiple ADCs might be different*
4. *The voltage booster on ADC switches must be used for V_{DDA} < 2.4 V (embedded I/O switches).*
5. *The tolerance is 10 LSBs for 16-bit resolution, 4 LSBs for 14-bit resolution, and 2 LSBs for 12-bit, 10-bit and 8-bit resolutions.*

Table 94. Minimum sampling time vs R_{AIN}

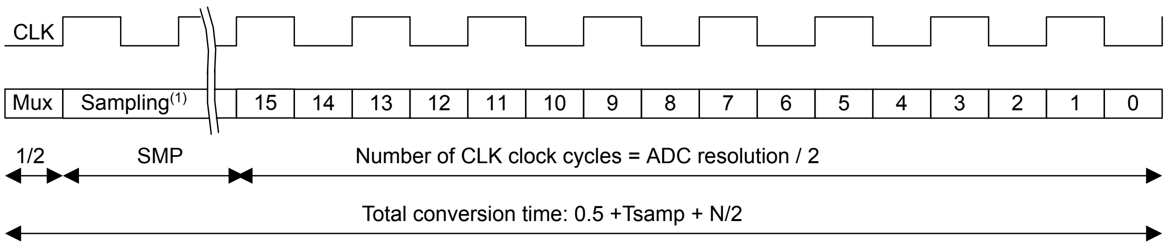
Data valid up to 130 °C, with a 47 pF PCB capacitor and V_{DDA}=1.6 V.

Resolution	RAIN (Ω)	Minimum sampling time (s)		
		Direct channels(1)(2)	Fast channels(1)(3)	Slow channels(1)(4)
16 bits	47	7.37E-08	1.14E-07	1.72E-07
14 bits	47	6.29E-08	9.74E-08	1.55E-07
	68	6.84E-08	1.02E-07	1.58E-07
	100	7.80E-08	1.12E-07	1.62E-07
	150	9.86E-08	1.32E-07	1.80E-07
	220	1.32E-07	1.61E-07	2.01E-07
12 bits	47	5.32E-08	8.00E-08	1.29E-07
	68	5.74E-08	8.50E-08	1.32E-07
	100	6.58E-08	9.31E-08	1.40E-07
	150	8.37E-08	1.10E-07	1.51E-07
	220	1.11E-07	1.34E-07	1.73E-07
	330	1.56E-07	1.78E-07	2.14E-07
	470	2.16E-07	2.39E-07	2.68E-07
	680	3.01E-07	3.29E-07	3.54E-07
10 bits	47	4.34E-08	6.51E-08	1.08E-07
	68	4.68E-08	6.89E-08	1.11E-07
	100	5.35E-08	7.55E-08	1.16E-07
	150	6.68E-08	8.77E-08	1.26E-07
	220	8.80E-08	1.08E-07	1.40E-07
	330	1.24E-07	1.43E-07	1.71E-07
	470	1.69E-07	1.89E-07	2.13E-07
	680	2.38E-07	2.60E-07	2.80E-07
	1000	3.45E-07	3.66E-07	3.84E-07
	1500	5.15E-07	5.35E-07	5.48E-07
	2200	7.42E-07	7.75E-07	7.78E-07
	3300	1.10E-06	1.14E-06	1.14E-06
8 bits	47	3.32E-08	5.10E-08	8.61E-08
	68	3.59E-08	5.35E-08	8.83E-08

Resolution	RAIN (Ω)	Minimum sampling time (s)		
		Direct channels(1)(2)	Fast channels(1)(3)	Slow channels(1)(4)
8 bits	100	4.10E-08	5.83E-08	9.22E-08
	150	5.06E-08	6.76E-08	9.95E-08
	220	6.61E-08	8.22E-08	1.11E-07
	330	9.17E-08	1.08E-07	1.32E-07
	470	1.24E-07	1.40E-07	1.63E-07
	680	1.74E-07	1.91E-07	2.12E-07
	1000	2.53E-07	2.70E-07	2.85E-07
	1500	3.73E-07	3.93E-07	4.05E-07
	2200	5.39E-07	5.67E-07	5.75E-07
	3300	8.02E-07	8.36E-07	8.38E-07
	4700	1.13E-06	1.18E-06	1.18E-06
	6800	1.62E-06	1.69E-06	1.68E-06
	10000	2.36E-06	2.47E-06	2.45E-06
	15000	3.50E-06	3.69E-06	3.65E-06

1. *Guaranteed by design.*
2. *Direct channels are connected to analog I/Os (PA0_C, PA1_C, PC2_C and PC3_C) to optimize ADC performance.*
3. *Fast channels correspond for ADCx_INPx to PA6, PB1, PC4, PF11, PF13 and for ADCx_INNx to PA7, PB0, PC5, PF12, PF14*
4. *Slow channels correspond to all ADC inputs except for the Direct and Fast channels.*

Figure 54. ADC conversion timing diagram



1. The sampling time defines the minimum sampling clock cycles (SMP) to be programmed in the ADC (refer to the product reference manual for details).

Table 95. ADC accuracy

Data guaranteed by characterization for BGA packages. The values for LQFP packages might differ. ADC DC accuracy values are measured after internal calibration.

Symbol	Parameter	Conditions(1)		Min	Typ	Max	Unit
ET	Total undadjusted error	Direct channel	Single ended	-	+10/–20	-	LSB
			Differential	-	±15	-	
		Fast channel	Single ended	-	+10/–20	-	
			Differential	-	±15	-	
		Slow channel	Single ended	-	±10	-	
			Differential	-	±10	-	

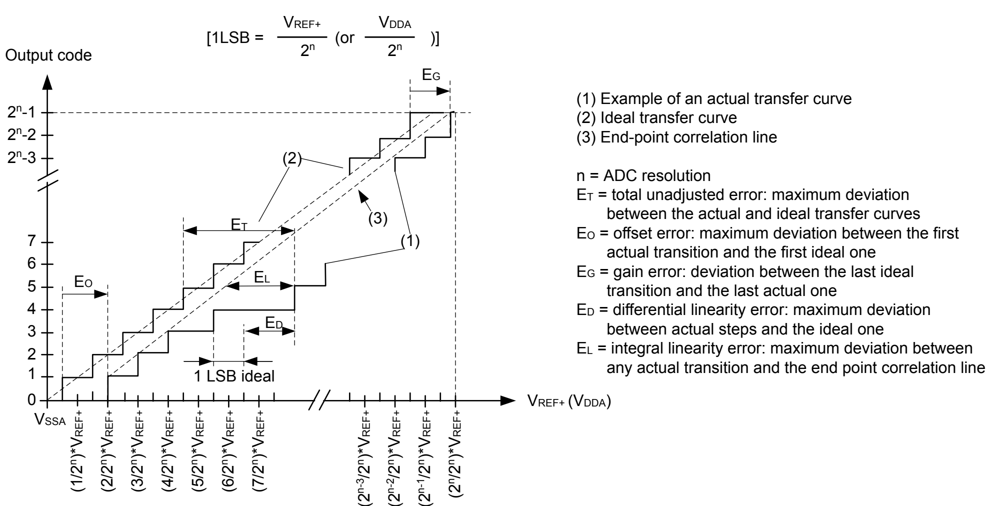
Symbol	Parameter	Conditions[(1)]		Min	Typ	Max	Unit
EO	Offset error	-		-	±10	-	LSB
EG	Gain error	-		-	±15	-	
ED	Differential linearity error	Single ended		-	+3/–1	-	
		Differential		-	+4.5/–1	-	
EL	Integral linearity error	Direct channel	Single ended	-	±11	-	
			Differential	-	±7	-	
		Fast channel	Single ended	-	±13	-	
			Differential	-	±7	-	
		Slow channel	Single ended	-	±10	-	
			Differential	-	±6	-	
ENOB	Effective number of bits	Single ended		-	12.2	-	Bits
		Differential		-	13.2	-	
SINAD	Signal-to-noise and distortion ratio	Single ended		-	75.2	-	dB
		Differential		-	81.2	-	
SNR	Signal-to-noise ratio	Single ended		-	77.0	-	
		Differential		-	81.0	-	
THD	Total harmonic distortion	Single ended		-	87	-	
		Differential		-	90	-	

1. *ADC clock frequency = 25 MHz, ADC resolution = 16 bits, V_{DDA}=V_{REF+}=3.3 V and BOOST=11.*

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in Section 6.3.15 I/O current injection characteristics does not affect the ADC accuracy.

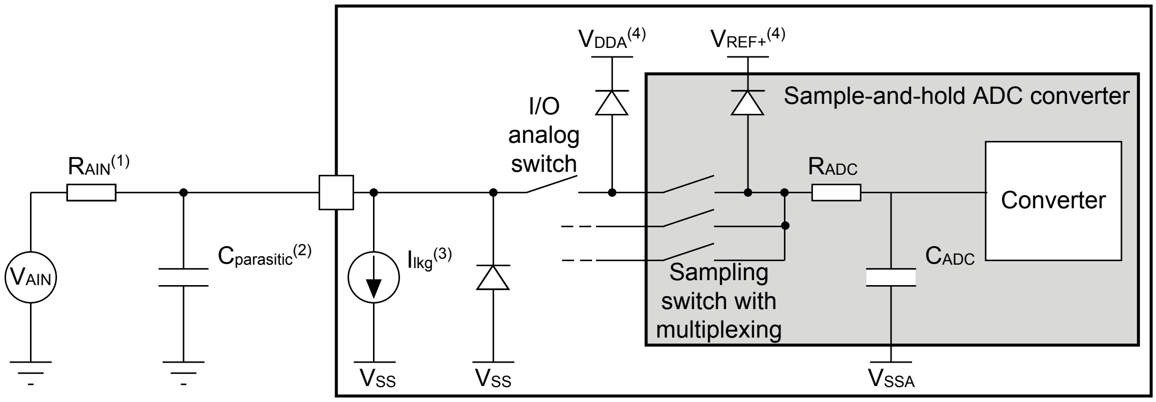
Figure 55. ADC accuracy characteristics



1. Example of an actual transfer curve.

2. Ideal transfer curve.
3. End point correlation line.
4. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
5. EO = Offset Error: deviation between the first actual transition and the first ideal one.
6. EG = Gain Error: deviation between the last ideal transition and the last actual one.
7. ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
8. EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 56. Typical connection diagram using the ADC with FT/TT pins featuring analog switch function



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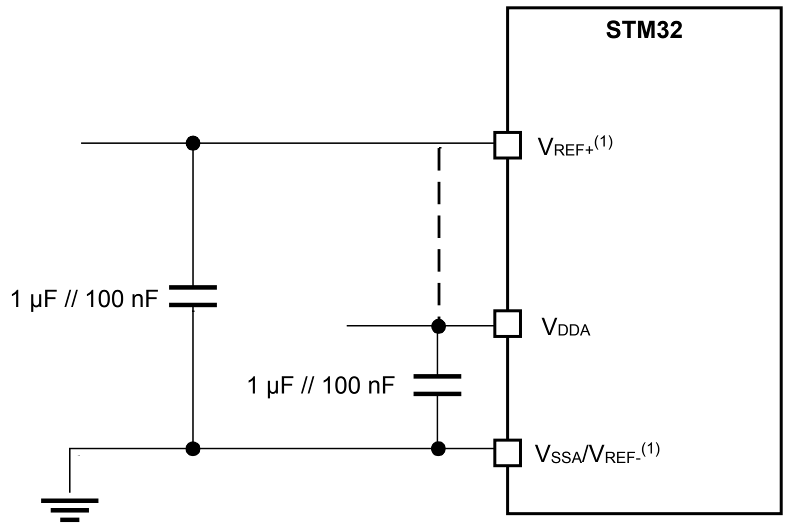
1. Refer to Table 93. ADC characteristics for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to Table 65. I/O static characteristics). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to Table 65. I/O static characteristics for the value of I_{lkg}.
4. Refer to .Figure 21. Power supply scheme.

General PCB design guidelines

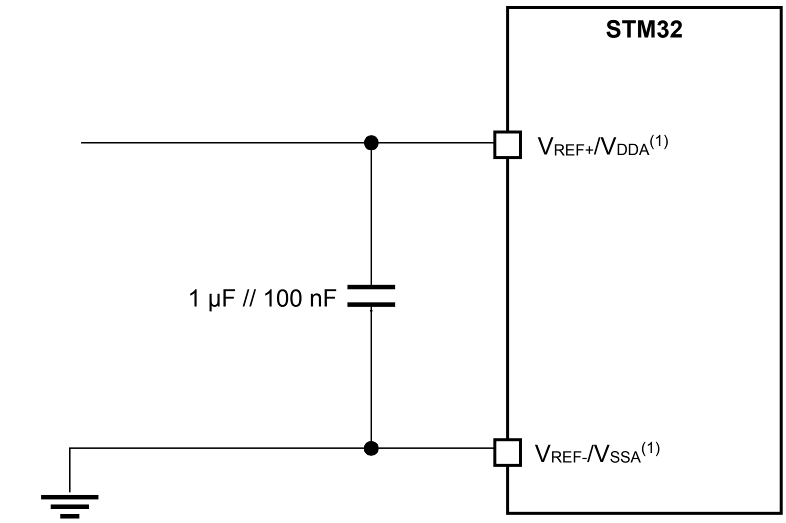
Power supply decoupling should be performed as shown in Figure 57. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA}) or Figure 58. Power supply and reference decoupling (V_{REF+} connected to V_{DDA}), depending on whether V_{REF+} is connected to V_{DDA} or not. The 100 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 57. **Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})**



1. V_{REF+} input is not available on all package (refer to Table 1. STM32H7A3xI/G features and peripheral counts) whereas V_{REF-} is available only on UFBGA176+25, TFBGA225 with SMPS and TFBGA216. When V_{REF-} is not available, it is internally connected to V_{SSA}.

Figure 58. **Power supply and reference decoupling (V_{REF+} connected to V_{DDA})**



1. V_{REF+} input is not available on all package (refer to Table 1. STM32H7A3xI/G features and peripheral counts) whereas V_{REF-} is available only on UFBGA176+25, TFBGA225 with SMPS and TFBGA216. When V_{REF-} is not available, it is internally connected to V_{SSA}.

6.3.22 DAC characteristics

Table 96. DAC characteristics

Symbol	Parameter	Conditions		Min[1]	Typ[1]	Max[1]	Unit
V_{DDA}	Analog supply voltage	-		1.8	3.3	3.6	V
V_{REF+}	Positive reference voltage	-		1.80	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-		-	V_{SSA}	-	
R_L	Resistive Load	DAC output buffer ON	connected to V_{SSA}	5	-	-	kΩ
			connected to V_{DDA}	25	-	-	
R_O	Output Impedance	DAC output buffer OFF		10.3	13	16	
R_{BON}	Output impedance sample and hold mode, output buffer ON	DAC output buffer ON	V_{DD} = 2.7 V	-	-	1.6	kΩ
			V_{DD} = 2.0 V	-	-	2.6	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	DAC output buffer OFF	V_{DD} = 2.7 V	-	-	17.8	kΩ
			V_{DD} = 2.0 V	-	-	18.7	
C_L	Capacitive Load	DAC output buffer OFF		-	-	50	pF
C_{SH}		Sample and Hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{DDA} −0.2	V
		DAC output buffer OFF		0	-	V_{REF+}	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value of ±0.5LSB, ±1LSB, ±2LSB, ±4LSB, ±8LSB)	Normal mode, DAC output buffer ON, C_L ≤ 50 pF, R_L ≥ 5 kΩ	±0.5 LSB	-	2.05	-	µs
			±1 LSB	-	1.97	-	
			±2 LSB	-	1.67	-	
			±4 LSB	-	1.66	-	
			±8 LSB	-	1.65	-	
		Normal mode, DAC output buffer OFF, ±1LSB C_L=10 pF		-	1.7	2	
t_{WAKEUP}[2]	Wakeup time from off state (setting the ENx bit in the DAC Control register) until the final value of ±1LSB is reached	Normal mode, DAC output buffer ON, C_L ≤ 50 pF, R_L = 5 kΩ		-	5	7.5	µs
		Normal mode, DAC output buffer OFF, C_L ≤ 10 pF		-	2	5	
PSRR	DC V_{DDA} supply rejection ratio	Normal mode, DAC output buffer ON, C_L ≤ 50 pF, R_L = 5 kΩ		-	−80	−28	dB
t_{SAMP}	Sampling time in Sample and Hold mode C_L=100 nF (code transition between the lowest input code and the highest input code when DAC_OUT reaches the ±1LSB final value)	MODE<2:0>_V12=100/101 (BUFFER ON)		-	0.7	2.6	ms
		MODE<2:0>_V12=110 (BUFFER OFF)		-	11.5	18.7	
		MODE<2:0>_V12=111[3] (INTERNAL BUFFER OFF)		-	0.3	0.6	µs
I_{leak}	Output leakage current	-		-	-	[4]	nA
C_{Iint}	Internal sample and hold capacitor	-		1.8	2.2	2.6	pF
t_{TRIM}	Middle code offset trim time	Minimum time to verify the each code		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	850	-	µV
		V_{REF+} = 1.8 V		-	425	-	

Symbol	Parameter	Conditions		Min(1)	Typ(1)	Max(1)	Unit
$I_{DDA(DAC)}$	DAC quiescent consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	360	-	µA
			No load, worst code (0xF1C)	-	490	-	
		DAC output buffer OFF	No load, middle/worst code (0x800)	-	20	-	
		Sample and Hold mode, C_{SH}=100 nF		-	$360*T_{ON}/(T_{ON}+T_{OFF})$(5)	-	
$I_{DDV(DAC)}$	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	170	-	
			No load, worst code (0xF1C)	-	170	-	
		DAC output buffer OFF	No load, middle/worst code (0x800)	-	160	-	
		Sample and Hold mode, Buffer ON, C_{SH}=100 nF (worst code)		-	$170*T_{ON}/(T_{ON}+T_{OFF})$(5)	-	
		Sample and Hold mode, Buffer OFF, C_{SH}=100 nF (worst code)		-	$160*T_{ON}/(T_{ON}+T_{OFF})$(5)	-	

1. *Guaranteed by design, unless otherwise specified.*
2. *In buffered mode, the output can overshoot above the final value for low input code (starting from the minimum value).*
3. *DACx_OUT pin is not connected externally (internal connection only).*
4. *Refer to Table 65. I/O static characteristics.*
5. *T_{ON} is the refresh phase duration, while T_{OFF} is the hold phase duration. Refer to the product reference manual for more details.*

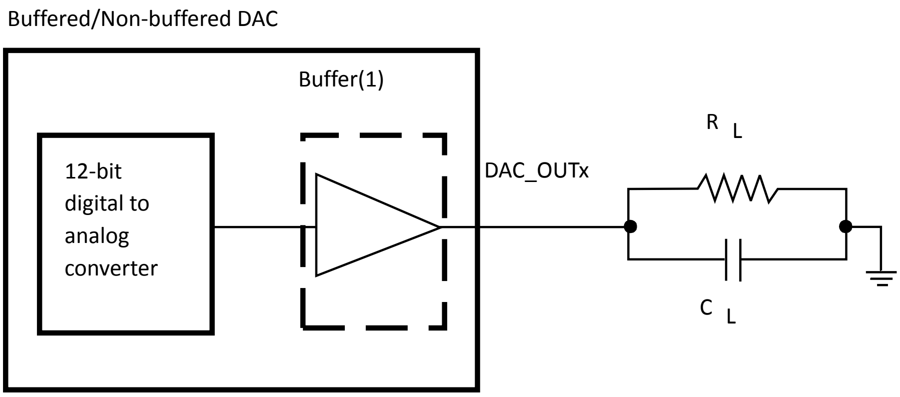
Table 97. DAC accuracy

Symbol	Parameter	Conditions		Min(1)	Typ(1)	Max(1)	Unit
DNL	Differential non linearity(2)	DAC output buffer ON		−2	-	2	LSB
		DAC output buffer OFF		−2	-	2	
INL	Integral non linearity(3)	DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ		−4	-	4	LSB
		DAC output buffer OFF, $C_L \leq 50$ pF, no R_L		−4	-	4	
Offset	Offset error at code 0x800(3)	DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ	V_{REF+} = 3.6 V	-	-	±12	LSB
			V_{REF+} = 1.8 V	-	-	±25	
		DAC output buffer OFF, $C_L \leq 50$ pF, no R_L	-	-	-	±8	
Offset1	Offset error at code 0x001(4)	DAC output buffer OFF, $C_L \leq 50$ pF, no R_L		-	-	±5	LSB
OffsetCal	Offset error at code 0x800 after factory calibration	DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ	V_{REF+} = 3.6 V	-	-	±5	LSB
			V_{REF+} = 1.8 V	-	-	±7	
Gain	Gain error(5)	DAC output buffer ON,$C_L \leq 50$ pF, $R_L \geq 5$ kΩ		-	-	±1	%
		DAC output buffer OFF, $C_L \leq 50$ pF, no R_L		-	-	±1	
TUE	Total undajusted error	DAC output buffer ON,$C_L \leq 50$ pF, $R_L \geq 5$ kΩ		-	-	±30	LSB
		DAC output buffer OFF, $C_L \leq 50$ pF, no R_L		-	-	±12	
TUECal	Total undajusted error after calibration	DAC output buffer ON $C_L \leq 50$pF, $R_L \geq 5$kΩ		-	-	±23	LSB
SNR	Signal-to-noise ratio(6)	DAC output buffer ON $C_L \leq 50$pF, $R_L \geq 5$kΩ 1 kHz, BW 500KHz		-	67.8	-	dB
		DAC output buffer OFF $C_L \leq 50$pF, no R_L 1kHz, BW 500KHz		-	67.8	-	

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
THD	Total harmonic distorsion(6)	DAC output buffer ON $C_L \leq 50pF$, $R_L \geq 5k\Omega$, 1 kHz	-	−78,6	-	dB
		DAC output buffer OFF $C_L \leq 50pF$, no R_L, 1 kHz	-	−78,6	-	
SINAD	Signal-to-noise and distorsion ratio(6)	DAC output buffer ON $C_L \leq 50pF$, $R_L \geq 5k\Omega$, 1 kHz	-	67.5	-	dB
		DAC output buffer OFF $C_L \leq 50pF$, no R_L, 1 kHz	-	67.5	-	
ENOB	Effective number of bits	DAC output buffer ON $C_L \leq 50pF$, $R_L \geq 5k\Omega$, 1 kHz	-	10.9	-	dB
		DAC output buffer OFF $C_L \leq 50pF$, no R_L, 1 kHz	-	10.9	-	

1. *Guaranteed by design, unless otherwise specified.*
2. *Difference between two consecutive codes minus 1 LSB.*
3. *Difference between the value measured at Code i and the value measured at Code i on a line drawn between Code 0 and last Code 4095.*
4. *Difference between the value measured at Code (0x001) and the ideal value.*
5. *Difference between the ideal slope of the transfer function and the measured slope computed from code 0x000 and 0xFFF when the buffer is OFF, and from code giving 0.2 V and (V_{REF+} − 0.2 V) when the buffer is ON.*
6. *Signal is −0.5dBFS with Fsampling = 1 MHz.*

Figure 59. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.23 Voltage reference buffer characteristics

Table 98. VREFBUF characteristics

Symbol	Parameter	Conditions		Min(1)	Typ(1)	Max(1)	Unit
V_{DDA}	Analog supply voltage	Normal mode	VSCALE = 000	2.8	3.3	3.6	V
			VSCALE = 001	2.4	-	3.6	
			VSCALE = 010	2.1	-	3.6	
			VSCALE = 011	1.8	-	3.6	
		Degraded mode(2)	VSCALE = 000	1.62	-	2.80	
			VSCALE = 001	1.62	-	2.40	
			VSCALE = 010	1.62	-	2.10	
			VSCALE = 011	1.62	-	1.80	

Symbol	Parameter	Conditions		Min(1)	Typ(1)	Max(1)	Unit
V_{REFBUF_OUT}	Voltage Reference Buffer Output	Normal mode at 30°C, I_{LOAD}=100 µA	VSCALE = 000	2.496(3)	2.5000	2.504(3)	V
			VSCALE = 001	2,0460	2.0490	2,0520	
			VSCALE = 010	1,8010	1.8040	1,8060	
			VSCALE = 011	1,4995	1.5015	1,5040	
		Degraded mode(2)	VSCALE = 000	VDDA− 150 mV	-	VDDA	
			VSCALE = 001	VDDA− 150 mV	-	VDDA	
			VSCALE = 010	VDDA− 150 mV	-	VDDA	
			VSCALE = 011	VDDA− 150 mV	-	VDDA	
TRIM	Trim step resolution	-	-	-	±0.05	±0.1	%
C_L	Load capacitor	-	-	0.5	1	1.50	uF
esr	Equivalent Serial Resistor of C_L	-	-	-	-	2	Ω
I_{LOAD}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{LOAD} = 500 µA	-	200	-	ppm/V
			I_{LOAD} = 4 mA	-	100	-	
I_{LOAD_reg}	Load regulation	500 µA ≤ I_{LOAD} ≤ 4 mA	Normal Mode	-	50	-	ppm/ mA
T_{coeff}	Temperature coefficient	−40 °C < T_J < +130 °C	-	-	-	Tcoeff VREFINT + 100	ppm/ °C
PSRR	Power supply rejection	DC	-	-	60	-	dB
		100KHz	-	-	40	-	
t_{START}	Startup time	C_L=0.5 µF	-	-	300	-	µs
		C_L=1 µF	-	-	500	-	
		C_L=1.5 µF	-	-	650	-	
I_{INRUSH}	Control of maximum DC current drive on V_{REFBUF_OUT} during startup phase(4)	-		-	8	-	mA
$I_{DDA(VREFBUF)}$	V_{REFBUF} consumption from V_{DDA}	I_{LOAD} = 0 µA	-	-	15	25	µA
		I_{LOAD} = 500 µA	-	-	16	30	
		I_{LOAD} = 4 mA	-	-	32	50	

1. *Guaranteed by design, unless otherwise specified.*
2. *In degraded mode, the voltage reference buffer cannot accurately maintain the output voltage (V_{DDA}−drop voltage).*
3. *Guaranteed by tests in production.*
4. *To properly control VREFBUF I_{INRUSH} current during the startup phase and the change of scaling, VDDA voltage should be in the range of 1.8 V-3.6 V, 2.1 V-3.6 V, 2.4 V-3.6 V and 2.8 V-3.6 V for VSCALE = 011, 010, 001 and 000, respectively.*

6.3.24 Analog temperature sensor characteristics

Table 99. Analog temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L (1)	V_{SENSE} linearity with temperature (from V_{SENSOR} voltage)	-	-	3	°C
	V_{SENSE} linearity with temperature (from ADC counter)	-	-	3	
Avg_Slope(2)	Average slope (from V_{SENSOR} voltage)	-	2	-	mV/°C
	Average slope (from ADC counter)	-	2	-	
V_{30} (3)	Voltage at 30°C ± 5 °C	-	0.62	-	V
t_{start_run} (1)	Startup time in Run mode (buffer startup)	-	-	25.2	µs
t_{S_temp} (1)	ADC sampling time when reading the temperature	9	-	-	
I_{sens} (1)	Sensor consumption	-	0.18	0.31	µA
$I_{sensbuf}$ (1)	Sensor buffer consumption	-	3.8	6.5	

1. *Guaranteed by design.*
2. *Guaranteed by characterization results.*
3. *Measured at V_{DDA} = 3.3 V ± 10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte.*

Table 100. Analog temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	Temperature sensor raw data acquired value at 30 °C, V_{DDA}=3.3 V	0x08FF F814 - 0x08FF F816
TS_CAL2	Temperature sensor raw data acquired value at 130 °C, V_{DDA}=3.3 V	0x08FF F818 - 0x08FF F81A

6.3.25 Digital temperature sensor characteristics

Table 101. Digital temperature sensor characteristics

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
f_{DTS} (2)	Output Clock frequency	-	500	750	1150	kHz
T_{LC} (2)	Temperature linearity coefficient	VOS2	1660	2100	2750	Hz/°C
T_{TOTAL_ERROR} (2)	Temperature offset measurement, all VOS	T_J =−40 °C to 30 °C	−13	-	4	°C
		T_J =30 °C to 130 °C	−7	-	2	
T_{VDD_CORE}	Additional error due to supply variation	VOS2	0	-	0	°C
		VOS0, VOS1, VOS3	−1	-	1	
t_{TRIM}	Calibration time	-	-	-	2	ms
t_{WAKE_UP}	Wake-up time from off state until DTS ready bit is set	-	-	67	116.00	µs
I_{DDCORE_DTS}	DTS consumption on V_{CORE}	-	8.5	30	70.0	µA

1. *Guaranteed by design, unless otherwise specified.*
2. *Guaranteed by characterization results.*

6.3.26 Temperature and V_{BAT} monitoring

Table 102. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	26	-	KΩ
Q	Ratio on V_{BAT} measurement	-	4	-	-
Er(1)	Error on Q	–10	-	+10	%
t_{S_vbat}(1)	ADC sampling time when reading V_{BAT} input	9	-	-	µs
$V_{BAThigh}$	High supply monitoring	-	3.55	-	V
V_{BATlow}	Low supply monitoring	-	1.36	-	

1. *Guaranteed by design.*

Table 103. V_{BAT} charging characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS in PWR_CR3= 0	-	5	-	KΩ
		VBRS in PWR_CR3= 1	-	1.5	-	

Table 104. Temperature monitoring characteristics

Symbol	Parameter	Min(1)	Typ(1)	Max(1)	Unit
$TEMP_{high}$	High temperature monitoring	-	117	-	°C
$TEMP_{low}$	Low temperature monitoring	-	–25	-	

1. *Guaranteed by design.*

6.3.27 Voltage booster for analog switch

Table 105. Voltage booster for analog switch characteristics

Symbol	Parameter	Condition	Min(1)	Typ(1)	Max(1)	Unit
V_{DD}	Supply voltage	-	1.62	2.6	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	-	50	µs
$I_{DD(BOOST)}$	Booster consumption	1.62 V ≤ V_{DD} ≤ 2.7 V	-	-	125	µA
		2.7 V < V_{DD} < 3.6 V	-	-	250	

1. *Guaranteed by characterization results.*

6.3.28 Comparator characteristics

Table 106. COMP characteristics

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.62	3.3	3.6	V
V_{IN}	Comparator input voltage range	-	0	-	V_{DDA}	
V_{BG}(2)	Scaler input voltage	-	-			
V_{SC}	Scaler offset voltage	-	-	±5	±10	mV

Symbol	Parameter	Conditions		Min(1)	Typ(1)	Max(1)	Unit
$I_{DDA(SCALER)}$	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	0.2	0.3	µA
		BRG_EN=1 (bridge enable)		-	0.8	1	
t_{START_SCALER}	Scaler startup time	-		-	140	250	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode		-	2	5	µs
		Medium mode		-	5	20	
		Ultra-low-power mode		-	15	80	
t_D(3)	Propagation delay for 200 mV step with 100 mV overdrive	High-speed mode		-	50	80	ns
		Medium mode		-	0.5	0.9	µs
		Ultra-low-power mode		-	2.5	7	
	Propagation delay for step > 200 mV with 100 mV overdrive only on positive inputs	High-speed mode		-	50	120	ns
		Medium mode		-	0.5	1.2	µs
		Ultra-low-power mode		-	2.5	7	
V_{offset}	Comparator offset error	Full common mode range		-	±5	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		4	10	22	
		Medium hysteresis		8	20	37	
		High hysteresis		16	30	52	
I_{DDA}(COMP)	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	-	400	600	nA
			With 50 kHz ±100 mV overdrive square signal	-	800	-	
		Medium mode	Static	-	5	7	µA
			With 50 kHz ±100 mV overdrive square signal	-	6	-	
		High-speed mode	Static	-	70	100	
			With 50 kHz ±100 mV overdrive square signal	-	75	-	

1. *Guaranteed by design, unless otherwise specified.*
2. *Refer to Section 6.3.6 Embedded reference voltage.*
3. *Guaranteed by characterization results.*

6.3.29 Operational amplifier characteristics

Table 107. Operational amplifier characteristics

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
V_{DDA}	Analog supply voltage Range	-	2	3.3	3.6	V
CMIR	Common Mode Input Range	-	0	-	V_{DDA}	
VI_{OFFSET}	Input offset voltage	25°C, no load on output	-	-	±1.5	mV
		All voltages and temperature, no load	-	-	±2.5	
ΔVI_{OFFSET}	Input offset voltage drift	-	-	±3.0	-	µV/°C
TRIMOFFSETP, TRIMLPOFFSETP	Offset trim step at low common input voltage (0.1*V_{DDA})	-	-	1.1	1.5	mV

Symbol	Parameter	Conditions		Min[1]	Typ[1]	Max[1]	Unit
TRIMOFFSETN, TRIMLPOFFSETN	Offset trim step at high common input voltage (0.9*V_{DDA})	-		-	1.1	1.5	mV
I_{LOAD}	Drive current	-		-	-	500	µA
I_{LOAD_PGA}	Drive current in PGA mode	-		-	-	270	
C_{LOAD}	Capacitive load	-		-	-	50	pF
CMRR	Common mode rejection ratio	-		-	80	-	dB
PSRR	Power supply rejection ratio	C_{LOAD} ≤ 50pf / R_{LOAD} ≥ 4 kΩ[2] at 1 kHz, V_{com}=V_{DDA}/2		50	66	-	dB
GBW	Gain bandwidth for high supply range	200 mV ≤ Output dynamic range ≤ V_{DDA} - 200 mV		4	7.3	12.3	MHz
SR	Slew rate (from 10% and 90% of output voltage)	Normal mode		-	3	-	V/µs
		High-speed mode		-	24	-	
AO	Open loop gain	200 mV ≤ Output dynamic range ≤ V_{DDA} - 200 mV		59	90	129	dB
φm	Phase margin	-		-	55	-	°
GM	Gain margin	-		-	12	-	dB
V_{OHSAT}	High saturation voltage	I_{load}=max or R_{LOAD}=min, Input at V_{DDA}		V_{DDA} −100 mV	-	-	mV
V_{OLSAT}	Low saturation voltage	I_{load}=max or R_{LOAD}=min, Input at 0 V		-	-	100	
t_{WAKEUP}	Wake up time from OFF state	Normal mode	C_{LOAD} ≤ 50pf, R_{LOAD} ≥ 4 kΩ, follower configuration	-	0.8	3.2	µs
		High speed mode	C_{LOAD} ≤ 50pf, R_{LOAD} ≥ 4 kΩ, follower configuration	-	0.9	2.8	
PGA gain	Non inverting gain error value	PGA gain = 2		−1	-	1	%
		PGA gain = 4		−2	-	2	
		PGA gain = 8		−2.5	-	2.5	
		PGA gain = 16		−3	-	3	
	Inverting gain error value	PGA gain = 2		−1	-	1	
		PGA gain = 4		−1	-	1	
		PGA gain = 8		−2	-	2	
		PGA gain = 16		−3	-	3	
	External non-inverting gain error value	PGA gain = 2		−1	-	1	
		PGA gain = 4		−3	-	3	
		PGA gain = 8		−3.5	-	3.5	
		PGA gain = 16		−4	-	4	
$R_{network}$	R2/R1 internal resistance values in non-inverting PGA mode[3]	PGA Gain=2		-	10/10	-	kΩ/ kΩ
		PGA Gain=4		-	30/10	-	
		PGA Gain=8		-	70/10	-	
		PGA Gain=16		-	150/10	-	
	R2/R1 internal resistance values in inverting PGA mode[3]	PGA Gain = -1		-	10/10	-	
		PGA Gain = -3		-	30/10	-	

Symbol	Parameter	Conditions		Min(1)	Typ(1)	Max(1)	Unit
$R_{network}$	R2/R1 internal resistance values in inverting PGA mode(3)	PGA Gain = -7		-	70/10	-	kΩ/ kΩ
		PGA Gain = -15		-	150/10	-	
Delta R	Resistance variation (R1 or R2)	-		−15	-	15	%
PGA BW	PGA bandwidth for different non inverting gain	Gain=2		-	GBW/2	-	MHz
		Gain=4		-	GBW/4	-	
		Gain=8		-	GBW/8	-	
		Gain=16		-	GBW/16	-	
	PGA bandwidth for different inverting gain	Gain = -1		-	5.00	-	MHz
		Gain = -3		-	3.00	-	
		Gain = -7		-	1.50	-	
		Gain = -15		-	0.80	-	
en	Voltage noise density	at 1 KHz	output loaded with 4 kΩ	-	140	-	nV/√Hz
		at 10 KHz		-	55	-	
$I_{DDA(OPAMP)}$	OPAMP consumption from V_{DDA}	Normal mode	no Load, quiescent mode, follower	-	570	1000	µA
		High-speed mode		-	610	1200	

1. *Guaranteed by design, unless otherwise specified.*
2. *R_{LOAD} is the resistive load connected to VSSA or to VDDA.*
3. *R2 is the internal resistance between the OPAMP output and th OPAMP inverting input. R1 is the internal resistance between the OPAMP inverting input and ground. PGA gain = 1 + R2/R1.*

6.3.30 Digital filter for Sigma-Delta Modulators (DFSDM) characteristics

Unless otherwise specified, the parameters given in Table 108. DFSDM measured timing 1.62-3.6 V for DFSDM are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in Table 22. General operating conditions and Section 6.3.1 .

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- VOS level set to VOS0

Refer to Section 6.3.16 I/O port characteristics for more details on the input/output alternate function characteristics (DìFSDM_CKINx, DFSDM_DATINx, DFSDM_CKOUT for DFSDM).

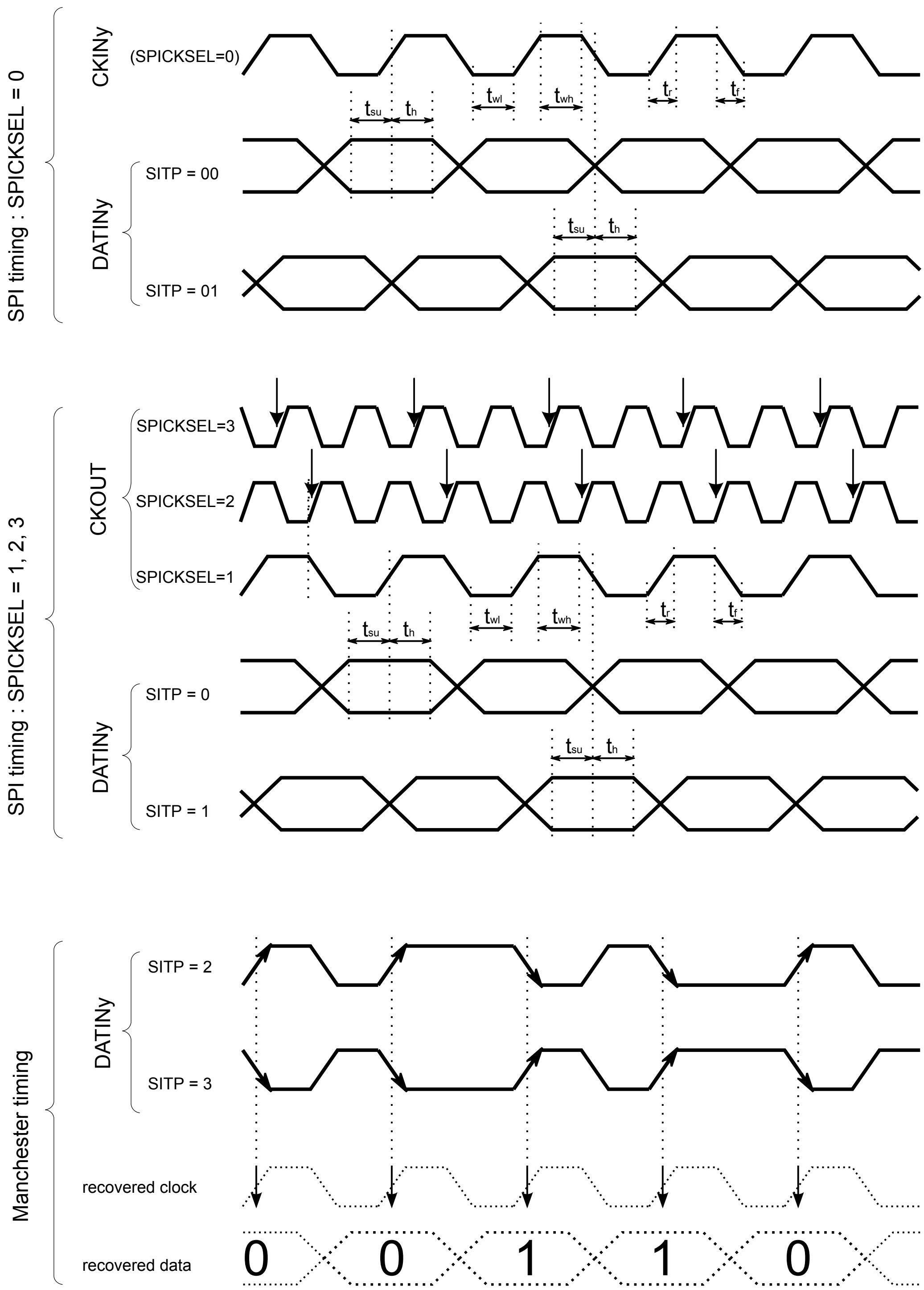
Table 108. DFSDM measured timing 1.62-3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	1.62 V < V_{DD} < 3.6 V		-	-	(1)	MHz
f_{CKIN} (1/ T_{CKIN})	Input clock frequency	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0),		-	-	20(2)	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]≠0)		-	-	20(2)	
f_{CKOUT}	Output clock frequency	1.62 < V_{DD} < 3.6 V		-	-	20	
DuCyCKOUT	Output clock frequency duty cycle	1.62 < V_{DD} < 3.6 V	Even division,CKOUTDIV[7:0] = n, 1, 3, 5, ...	45	50	55	%

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DuCyCKOUT	Output clock frequency duty cycle	$1.62 < V_{DD} < 3.6$ V	Odd division,CKOUTDIV[7:0] = n, 2, 4, 6, ...	(((n/ 2+1)/(n−1))*100)−5	(((n/2+1)/ (n−1))*100)	(((n/ 2+1)/(n−1))*100)+5	%
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), $1.62 < V_{DD} < 3.6$ V	-	$T_{CKIN}/2$ - 0.5	$T_{CKIN}/2$	-	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), $1.62 < V_{DD} < 3.6$ V	-	4	-	-	
t_h	Data input hold time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), $1.62 < V_{DD} < 3.6$ V	-	0.5	-	-	
$T_{Manchester}$	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0]=2,3), Internal clock mode (SPICKSEL[1:0]≠0), $1.62 < V_{DD} < 3.6$ V	-	(CKOUTDIV[7:0]+1) x $T_{DFSDMCLK}$	-	(2*CKOUTDIV[7:0]) x $T_{DFSDMCLK}$ (3)	

1. *The maximum DFSDM kernel clock is specified in Section 6.3.1 .*
2. *The internal DFSDMCLK clock must be at least 4 times faster than the external CKIN clock.*
3. *The internal DFSDMCLK must be at least 6 times faster than the Manchester data frequency.*

Figure 60. Channel transceiver timing diagrams



6.3.31 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in Table 109. DCMI characteristics for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and VDD supply voltage summarized in Table 22. General operating conditions and Section 6.3.1 , with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high

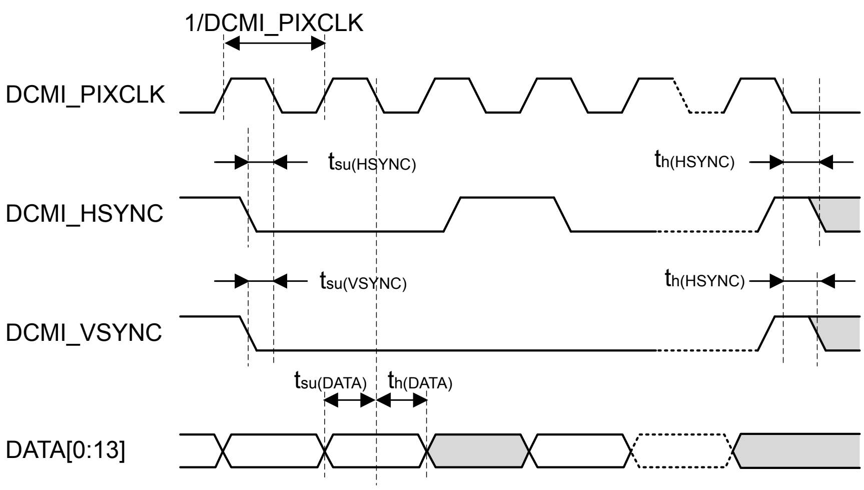
- Data formats: 14 bits
- Capacitive load C_L=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- Output speed is set to OSPEEDRy[1:0] = 11
- VOS level set to VOS0

Table 109. DCMI characteristics

Symbol	Parameter	Min[(1)]	Max[(1)]	Unit
-	Frequency ratio DCMI_PIXCLK/f_{HCLK}	-	0.4	-
DCMI_PIXCLK	Pixel Clock input	-	80	MHz
D_{pixel}	Pixel Clock input duty cycle	30	70	%
t_{su}(DATA)	Data input setup time	2.5	-	-
t_h(DATA)	Data hold time	1	-	
tsu(HSYNC), tsu(VSYNC)	DCMI_HSYNC/ DCMI_VSYNC input setup time	3	-	ns
th(HSYNC), th(VSYNC)	DCMI_HSYNC/ DCMI_VSYNC input hold time	1	-	-

1. *Guaranteed by design.*

Figure 61. DCMI timing diagram



6.3.32 PSSI interface characteristics

Unless otherwise specified, the parameters given in Table 110 and 111for PSSI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in Table 22. General operating conditions and Section 6.3.1 , with the following configuration:

- PSSI_PDCK polarity: falling
- PSSI_RDY and PSSI_DE polarity: low
- Bus width : 16 lines
- DATA width : 32 bits
- Capacitive load C=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- Output speed is set to OSPEEDRy[1:0] = 11

Note: At VOS1, the performance in Transmit mode can be degraded by up to 5 % compared to VOS0. This is indicated by a footnote when applicable.

Table 110. PSSI transmit characteristics

Guaranteed by characterization results.

Symbol	Parameter	Min	Max(1)	Unit
-	Frequency ratio PSSI_PDCK/f_{HCLK}	-	0.4	-
PSSI_PDCK	PSSI clock input	-	50	MHz
D_{pixel}	PSSI clock input duty cycle	30	70	%
$t_{dv(DATA)}$	Data output valid time	-	10	ns
$t_{dh(DATA)}$	Data output hold time	5	-	
$t_{dv((DE)}$	DE output valid time	-	14	
$t_{dh(DE)}$	DE output hold time	6	-	
$t_{su(RDY)}$	RDY input setup time	3	-	
$t_{h(RDY)}$	RDY input hold time	0	-	

1. *At VOS1, these values are degraded by up to 5 %.*

Table 111. PSSI receive characteristics

Guaranteed by characterization results.

Symbol	Parameter	Min	Max
-	Frequency ratio PSSI_PDCK/f_{HCLK}	-	0.4
PSSI_PDCK	PSSI clock input	-	100
D_{pixel}	PSSI clock input duty cycle	30	70
$t_{su(DATA)}$	Data input setup time	2	-
$t_{h(DATA)}$	Data input hold time	1	-
$t_{su((DE)}$	DE input setup time	3	-
$t_{h(DE)}$	DE input hold time	1	-
$t_{ov(RDY)}$	RDY output valid time	-	10
$t_{oh(RDY)}$	RDY output hold time	4.5	-

Figure 62. **PSSI timing diagram in Transmit mode**

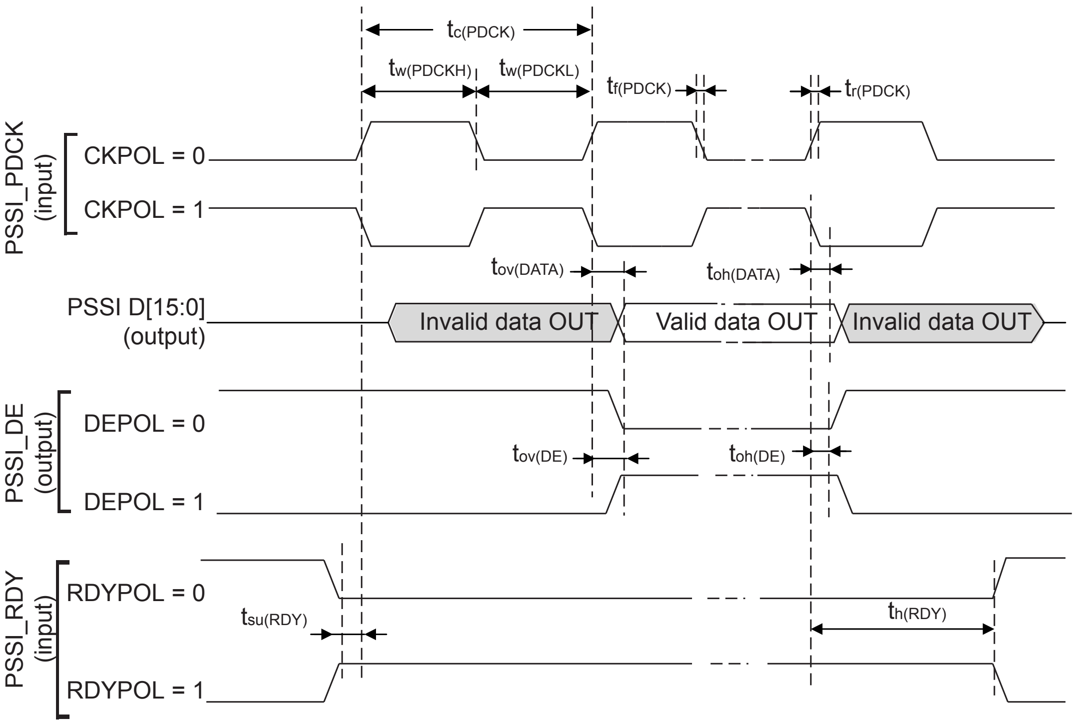
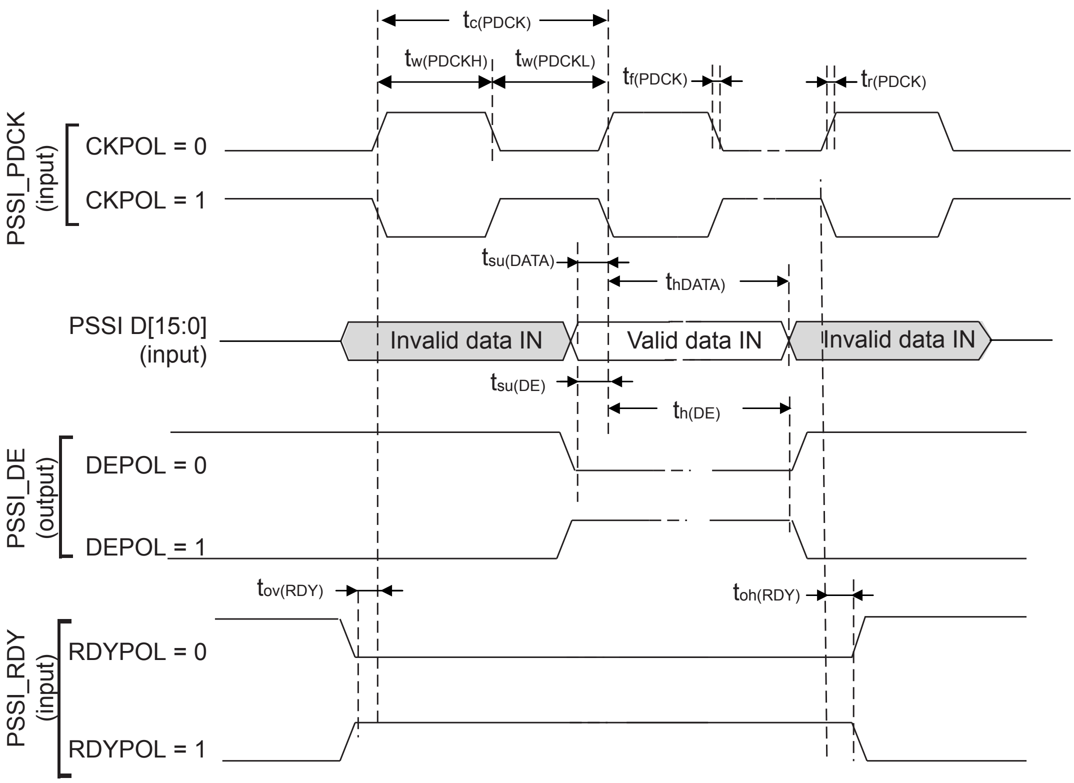


Figure 63. **PSSI timing diagram in Receive mode**



6.3.33 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in Table 112 for LCD-TFT are derived from tests performed under the ambient temperature, f_{HCLK} frequency and VDD supply voltage summarized in Table 22. General operating conditions and Section 6.3.1 , with the following configuration:

- LCD_CLK polarity: high
- LCD_DE polarity: low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L=30 pF
- Measurement points are done at CMOS levels: 0.5VDD
- IO Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS 0

Note: At VOS1, the performance can be degraded by up to 5 % compared to VOS0. This is indicated by a footnote when applicable.

Table 112. LTDC characteristics

Symbol	Parameter	Conditions	Min	Max[1]	Unit
f_{CLK}	LTDC clock output frequency	2.7 V < V_{DD} < 3.6 V, 20 pF	-	140	MHz
		2.7 V < V_{DD} < 3.6 V	-	133	
		1.62 V < V_{DD} < 3.6 V	-	66.5	
D_{CLK}	LTDC clock output duty cycle	-	45	55	%
$t_{w(CLKH)}$, $t_{w(CLKL)}$	Clock High time, low time	-	$t_{w(CLK)}$/2−0.5	$t_{w(CLK)}$/2+0.5	ns
$t_{v(DATA)}$	Data output valid time	2.7 V < V_{DD} < 3.6 V	-	3.0	
		1.62 V < V_{DD} < 3.6 V	-	7.5	
$t_{h(DATA)}$	Data output hold time	-	0	-	
$t_{v(HSYNC)}$, $t_{v(VSYNC)}$, $t_{v(DE)}$	HSYNC/VSYNC/DE output valid time	2.7 V < V_{DD} < 3.6 V	-	3.0	
		1.62 V < V_{DD} < 3.6 V	-	7.5	
$t_{h(HSYNC)}$, $t_{h(VSYNC)}$, $t_{h(DE)}$	HSYNC/VSYNC/DE output hold time	-	0	-	

1. *At VOS1, these values are degraded by up to 5 %.*

Figure 64. LCD-TFT horizontal timing diagram

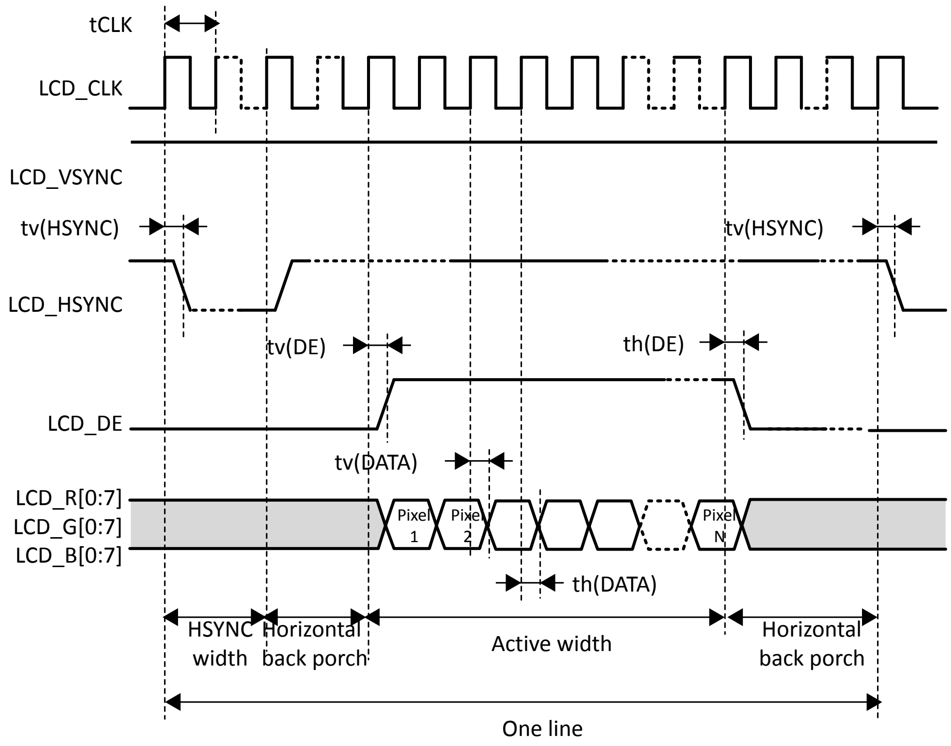
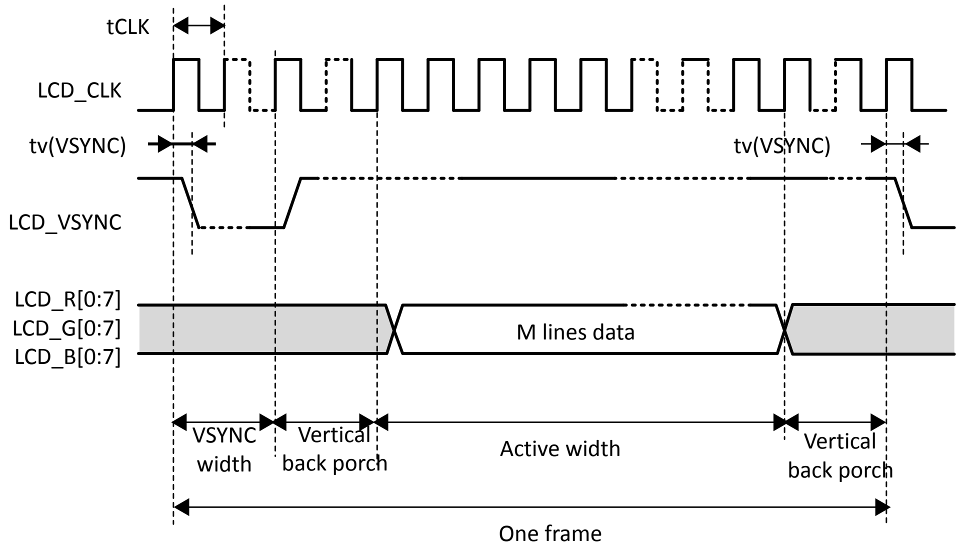


Figure 65. LCD-TFT vertical timing diagram



6.3.34 Timer characteristics

The parameters given in Table 113. TIMx characteristics are guaranteed by design.

Refer to Section 6.3.16 I/O port characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 113. TIMx characteristics

Symbol	Parameter	Conditions(1)	Min(2)	Max(2)	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK}$ = 280 MHz	1	-	$t_{TIMxCLK}$
		AHB/APBx prescaler>4, $f_{TIMxCLK}$ = 140 MHz	1	-	$t_{TIMxCLK}$
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 280 MHz	0	$f_{TIMxCLK}/2$	MHz
Res_{TIM}	Timer resolution		-	16/32	bit
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$

1. *The maximum timer frequency on APB1 or APB2 is up to 280 MHz, by setting the TIMPRE bit in the RCC_CFGR register. If APBx prescaler is 1 or 2 or 4, then TIMxCLK = rcc_hclk1, otherwise TIMxCLK = 4x $F_{rcc\_pclkx\_d2}$.*
2. *Guaranteed by design.*

6.3.35 Low-power timer characteristics

Table 114. LPTIMx characteristics

Symbol	Parameter	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	1	-	$t_{TIMxCLK}$
$f_{LPTIMxCLK}$	Timer kernel clock	0	100	MHz
f_{EXT}	Timer external clock frequency on Input1 and Input2	0	f_{LPTIM}xCLK/2	
Res_{TIM}	Timer resolution	-	16	bit
t_{MAX_COUNT}	Maximum possible count	-	65536	$t_{TIMxCLK}$

6.3.36 Communication interfaces

6.3.36.1 *I²C interface characteristics*

The I²C interface meets the timings requirements of the I2C-bus specification and user manual revision 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The parameters given in Table 115 and Table 116are obtained with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 00

Note: At VOS1, the performance can be degraded by up to 5 % compared to VOS0. This is indicated by a footnote when applicable.

The I²C timings requirements are guaranteed by design when the I²C peripheral is properly configured (refer to RM0455 reference manual) and when the i2c_ker_ck frequency is greater than the minimum shown in the table below:

Table 115. Minimum i2c_ker_ck frequency in all I²C modes

Symbol	Parameter	Condition		Min	Unit
f_{I2CCLK}	I2CCLK frequency	Standard-mode	-	2	MHz
		Fast-mode	Analog Filtre ON, DNF=0	9	
			Analog Filtre OFF, DNF=1	9	
		Fast-mode Plus	Analog Filtre ON, DNF=0	19	

Symbol	Parameter	Condition		Min	Unit
f_{I2CCLK}	I2CCLK frequency	Fast-mode Plus	Analog Filtre OFF, DNF=1	16	-

The SDA and SCL I/O requirements are met with the following restrictions:

- The SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but still present.
- The 20 mA output drive requirement in Fast-mode Plus is not supported. This limits the maximum load C_{Load} supported in Fm+, which is given by these formulas:

$t_{r(SDA/SCL)}$=0.8473xR_PxC_{Load}

$R_{P(min)}$= (V_{DD}-$V_{OL(max)}$)/$I_{OL(max)}$

Where R_P is the I2C lines pull-up. Refer to Section 6.3.16 I/O port characteristics for the I^2C I/Os characteristics.

All I^2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 116. I^2C analog filter characteristics

Symbol	Parameter	Min(1)	Max(1)	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by analog filter	50(2)	260(3)	ns

1. *Guaranteed by design.*
2. *Spikes whose width is lower than $t_{AF(min)}$ are filtered.*
3. *Spikes whose width is higer than $t_{AF(max)}$ are not filtered.*

6.3.36.2 *USART interface characteristics*

Unless otherwise specified, the parameters given in Table 117 for USART are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 22. General operating conditions and Section 6.3.1 , with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: 0.5V_{DD}
- IO Compensation cell activated.
- VOS level set to VOS0

Note: At VOS1, the performance can be degraded by up to 5 % compared to VOS0. This is indicated by a footnote when applicable.

Refer to Section 6.3.16 I/O port characteristics for more details on the input/output alternate function characteristics (NSS, CK, TX, RX for USART).

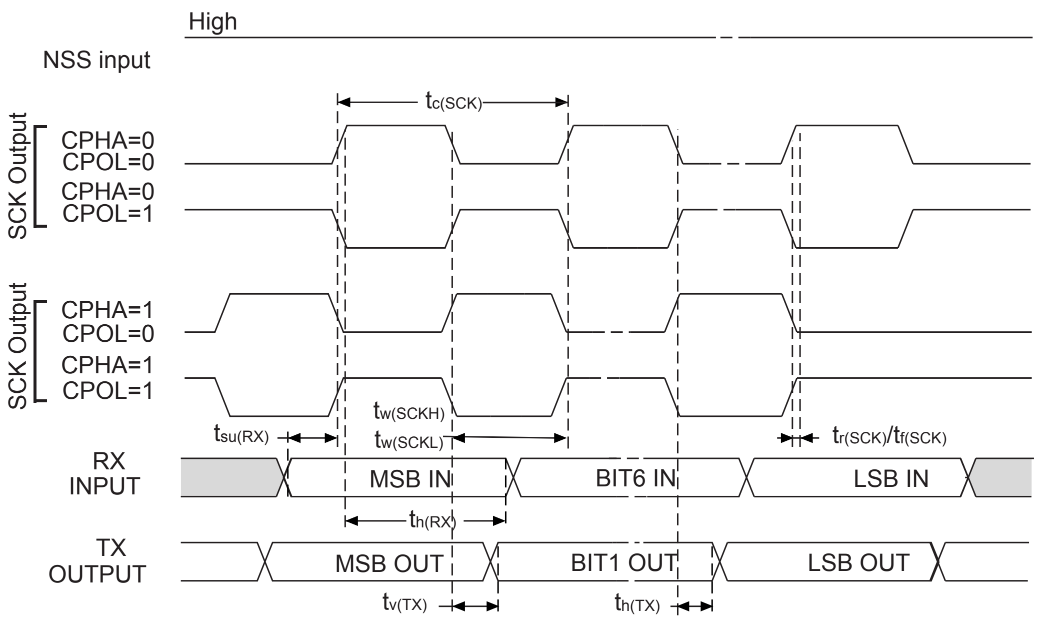
Table 117. USART characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
f_{CK}	USART clock frequency	Master mode	-	-	35	MHz
		Slave receiver mode			93.0	
		Slave mode transmitter mode, 2.7 V < V_{DD} < 3.6 V			29.0	
		Slave mode transmitter mode, 1.62 V < V_{DD} < 3.6 V			22.0	
$t_{su(NSS)}$	NSS setup time	Slave mode	t_{ker}+2	-	-	-
$t_{h(NSS)}$	NSS hold time	Slave mode	2	-	-	
$t_{w(SCKH)}$, $t_{w(SCKL)}$	CK high and low time	Master mode	$1/f_{ck}/2-2$	$1/f_{ck}/2$	$1/f_{ck}/2+2$	
$t_{su(RX)}$	Data input setup time	Master mode	17	-	-	ns
		Slave mode	1	-	-	

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
$t_{h(RX)}$	Data input hold time	Master mode	0	-	-	ns
		Slave mode	1.5	-	-	
$t_{v(TX)}$	Data output valid time	Slave mode transmitter mode, 1.62 V < V_{DD} < 3.6 V	-	15.5	22	
		Slave mode transmitter mode, 2.7 V < V_{DD} < 3.6 V	-	15.5	17	
		Master mode	-	1.5	2	
$t_{h(TX)}$	Data output hold time	Slave mode	12	-	-	
		Master mode	1	-	-	

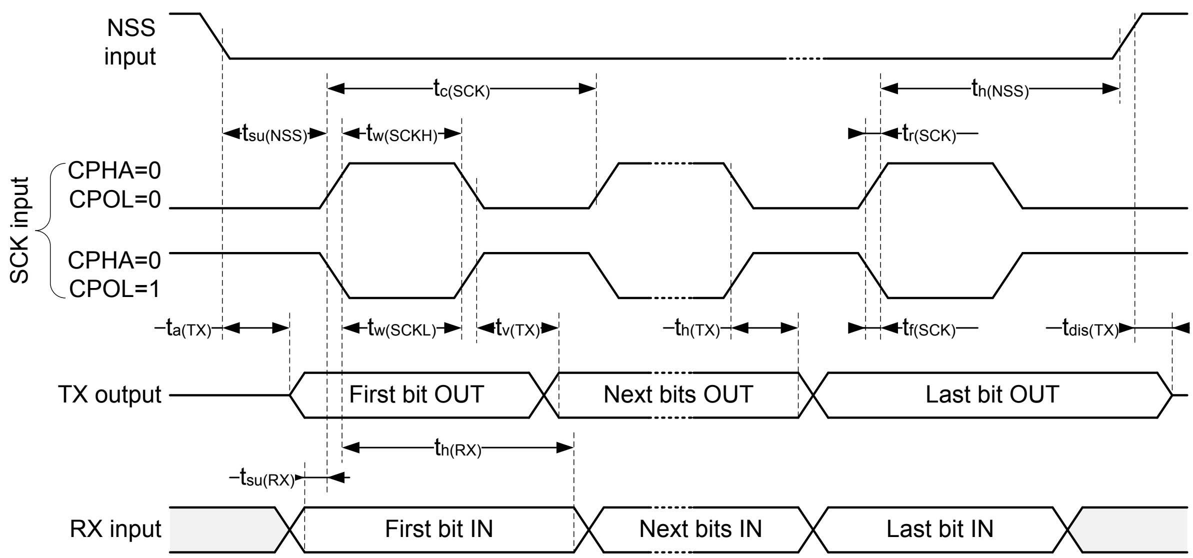
1. At VOS1, these values are degraded by up to 5 %.

Figure 66. USART timing diagram in Master mode



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Figure 67. USART timing diagram in Slave mode



6.3.36.3 *SPI interface characteristics*

Unless otherwise specified, the parameters given in Table 118 for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 22. General operating conditions and Section 6.3.1 , with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS0

Note: At VOS1, the performance can be degraded by up to 5 % compared to VOS0. This is indicated by a footnote when applicable.

Refer to Section 6.3.16 I/O port characteristics for more details on the input/output alternate function characteristics (SS, SCK, MOSI, MISO for SPI).

Table 118. SPI dynamic characteristics

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)(2)	Unit
f_{SCK}	SPI clock frequency	Master mode 2.7 < V_{DD}< 3.6 V, SPI1, 2, 3	-	-	125/100(3)	MHz
		Master mode, 2.7 < V_{DD}<3.6 V, SPI4, 5, 6			100	
		Master mode, 1.62 < V_{DD} < 3.6 V, SPI4, 5, 6			75/38(3)	
		Slave receiver mode, 1.62 < V_{DD} < 3.6 V			100	
		Slave mode transmitter/full duplex, 2.7 < V_{DD} < 3.6 V			45/31(3)	
		Slave mode transmitter/full duplex, 1.62 <V_{DD} < 3.6 V			29/18(3)	
$t_{su(SS)}$	SS setup time	Slave mode	2	-	-	ns
$t_{h(SS)}$	SS hold time	Slave mode	1	-	-	
$t_{su(MI)}$	Data input setup time	Master mode	3	-	-	ns

Symbol	Parameter	Conditions	Min[1]	Typ[1]	Max[1][2]	Unit
$t_{su(SI)}$	Data input setup time	Slave mode	2	-	-	ns
$t_{h(MI)}$	Data input hold time	Master mode	3	-	-	
$t_{h(SI)}$		Slave mode	1	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	13	27	
$t_{dis(SO)}$	Data output disable time	Slave mode	0	1	5	
$t_{v(SO)}$	Data output valid time	Slave mode, 2.7 < V_{DD} < 3.6 V	-	9/15[3]	11/16[3]	
		Slave mode, 1.62 < V_{DD} < 3.6 V	-	9/15[3]	17/27[3]	
$t_{v(MO)}$		Master mode, 2.7 < V_{DD} < 3.6 V	-	1/5[3]	1.5/7[3]	
		Master mode, 1.62 < V_{DD} < 3.6 V	-	1/5[3]	2/13[3]	
$t_{h(SO)}$	Data output hold time	Slave mode, 1.62 < V_{DD} < 3.6 V	7	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. *Guaranteed by characterization results.*
2. *At VOS1, these values are degraded by up to 5 %.*
3. *Using PC3_C / PC2_C (not available on all packages).*

Figure 68. SPI timing diagram - slave mode and CPHA = 0

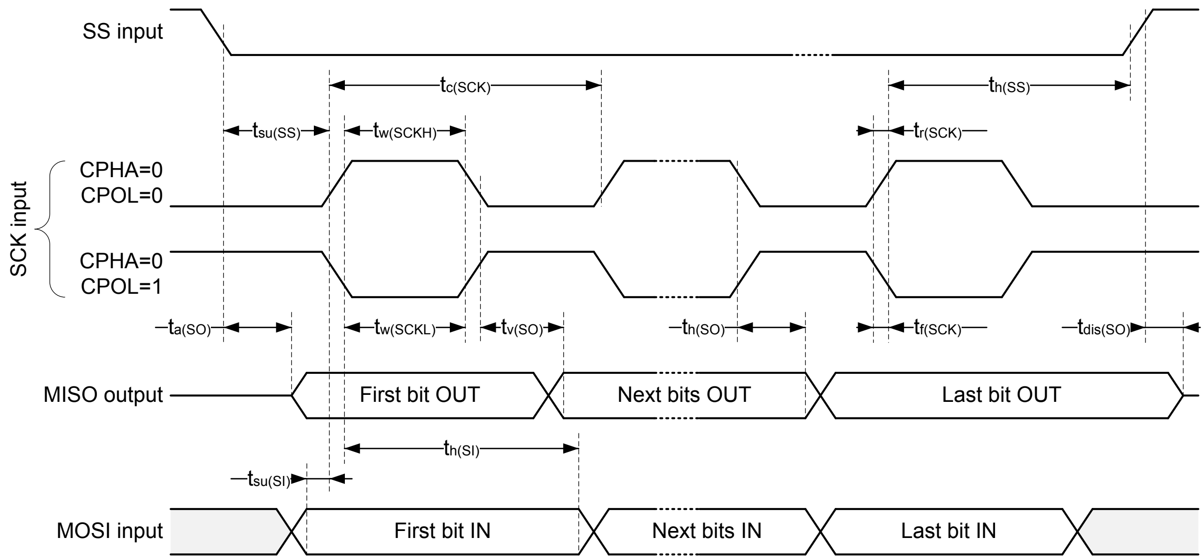
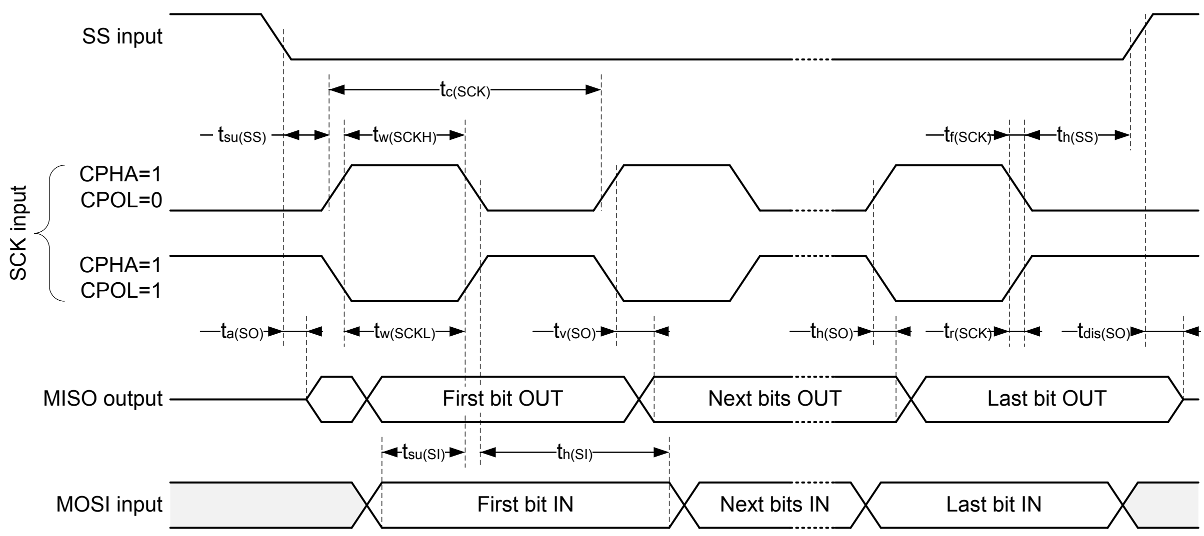
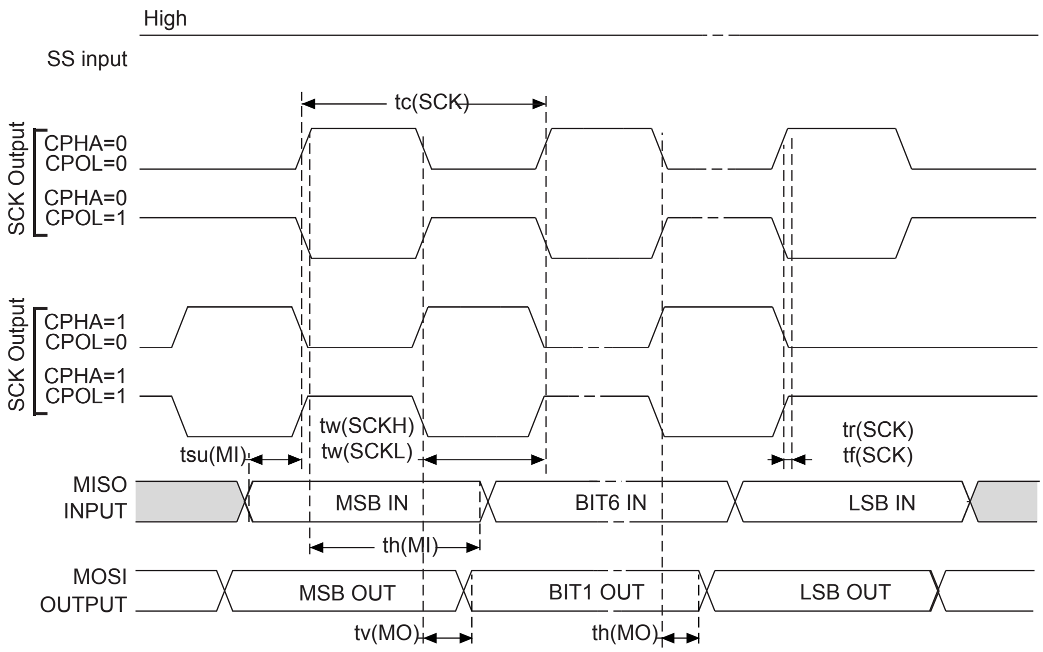


Figure 69. **SPI timing diagram - slave mode and CPHA = 1(1)**



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Figure 70. **SPI timing diagram - master mode(1)**



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

6.3.36.4 *I²S Interface characteristics*

Unless otherwise specified, the parameters given in Table 119 for I²S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 22. General operating conditions and Section 6.3.1 , with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10

- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when VDD ≤ 2.7 V
- VOS level set to VOS0

Note: *At VOS1, the performance can be degraded by up to 5 % compared to VOS0. This is indicated by a footnote when applicable.*

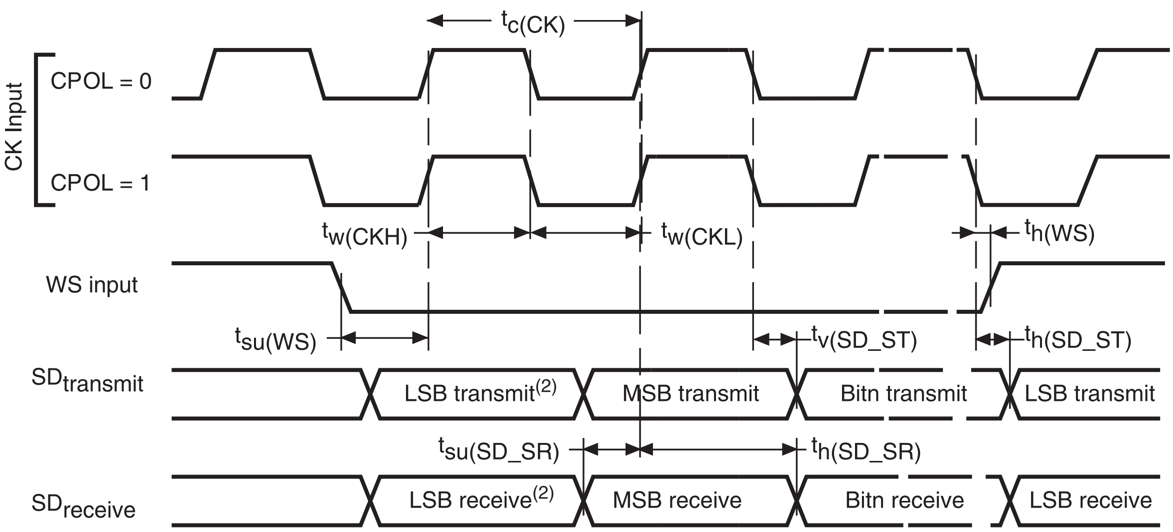
Refer to Section 6.3.16 I/O port characteristics for more details on the input/output alternate function characteristics (CK,SD,WS).

Table 119. I²S dynamic characteristics

Symbol	Parameter	Conditions	Min[1]	Max[1][2]	Unit
f_{MCK}	I²S main clock output	-	-	50	MHz
f_{CK}	I²S clock frequency	Master Tx	-	50/33[3]	MHz
		Master Rx	-	40	
		Slave Tx	-	31/18.5[3]	
		Slave Rx	-	50	
$t_{v(WS)}$	WS valid time	Master mode	-	5.5	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	2	-	
$t_{h(WS)}$	WS hold time	Slave mode	1	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	2	-	
$t_{su(SD\_SR)}$		Slave receiver	2	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	4.5	-	
$t_{h(SD\_SR)}$		Slave receiver	1	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	16/27[3]	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	4/15[3]	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	7	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	0	-	

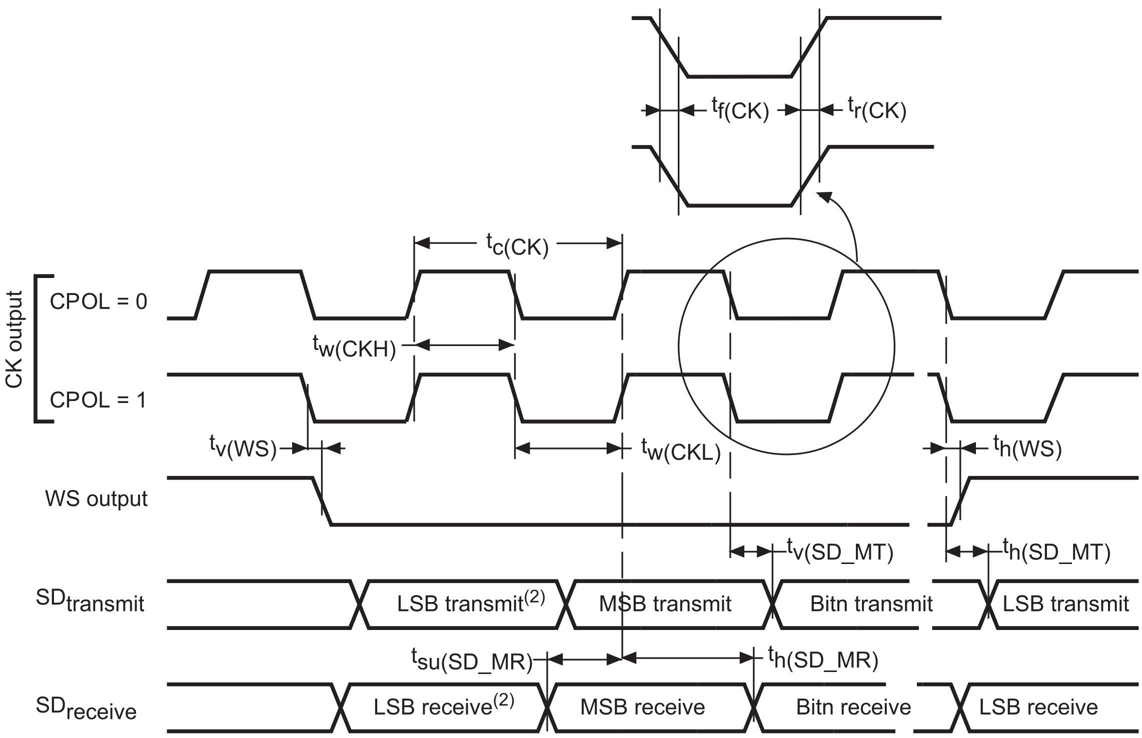
1. *Guaranteed by characterization results.*
2. *At VOS1, these values are degraded by up to 5 %.*
3. *Using PC3_C / PC2_C (not available on all packages).*

Figure 71. I²S slave timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 72. I²S master timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

6.3.36.5 SAI characteristics

Unless otherwise specified, the parameters given in Table 120 for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage conditions summarized in Table 22. General operating conditions and Section 6.3.1 , with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- IO Compensation cell activated.
- Measurement points are done at CMOS levels: 0.5VDD
- VOS level set to VOS0

Note: At VOS1, the performance can be degraded by up to 5 % compared to VOS0. This is indicated by a footnote when applicable.

Refer to Section 6.3.16 I/O port characteristics for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 120. SAI characteristics

Symbol	Parameter	Conditions	Min(1)	Max(1)(2)	Unit
f_{MCK}	SAI Main clock output	-	-	50	MHz
f_{CK}	SAI clock frequency	Master transmitter, 2.7 ≤ V_{DD} ≤ 3.6 V	-	34	
		Master transmitter, 1.62 ≤ V_{DD} ≤ 3.6 V	-	27	
		Master receiver, 1.6 ≤ V_{DD} ≤ 3.6 V	-	27	
		Slave transmitter, 2.7 ≤ VDD ≤ 3.6 V	-	37	
		Slave transmitter, 1.62 ≤ VDD ≤ 3.6 V	-	30	
		Slave receiver, 1.62 ≤ V_{DD}≤ 3.6 V	-	50	
$t_{v(FS)}$	F_S valid time	Master mode,2.7 ≤ V_{DD} ≤ 3.6 V	-	14.5	ns
		Master mode, 1.62 ≤ V_{DD} ≤ 3.6 V	-	18.5	
$t_{su(FS)}$	F_S setup time	Slave mode	8	-	
$t_{h(FS)}$	F_S hold time	Master mode	1	-	
	F_S hold time	Slave mode	2	-	
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	0.5	-	
$t_{su(SD\_B\_SR)}$		Slave receiver	1	-	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	5.5	-	
$t_{h(SD\_B\_SR)}$		Slave receiver	3	-	
$t_{v(SD\_B\_ST)}$	Data output valid time	Slave transmitter (after enable edge), 2.7 ≤ V_{DD} ≤ 3.6 V	-	13.5	
		Slave transmitter (after enable edge), 1.62 ≤ V_{DD} ≤ 3.6 V	-	16.5	
$t_{h(SD\_B\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	8	-	
$t_{v(SD\_A\_MT)}$	Data output valid time	Master transmitter (after enable edge), 2.7 ≤ V_{DD} ≤ 3.6 V	-	14	
		Master transmitter (after enable edge), 1.62 ≤ V_{DD} ≤ 3.6 V	-	18	
$t_{h(SD\_A\_MT)}$	Data output hold time	Master transmitter (after enable edge)	7.5	-	

1. *Guaranteed by characterization results.*
2. *At VOS1, these values are degraded by up to 5 %.*
3. *APB clock frequency must be at least twice SAI clock frequency.*

Figure 73. SAI master timing waveforms

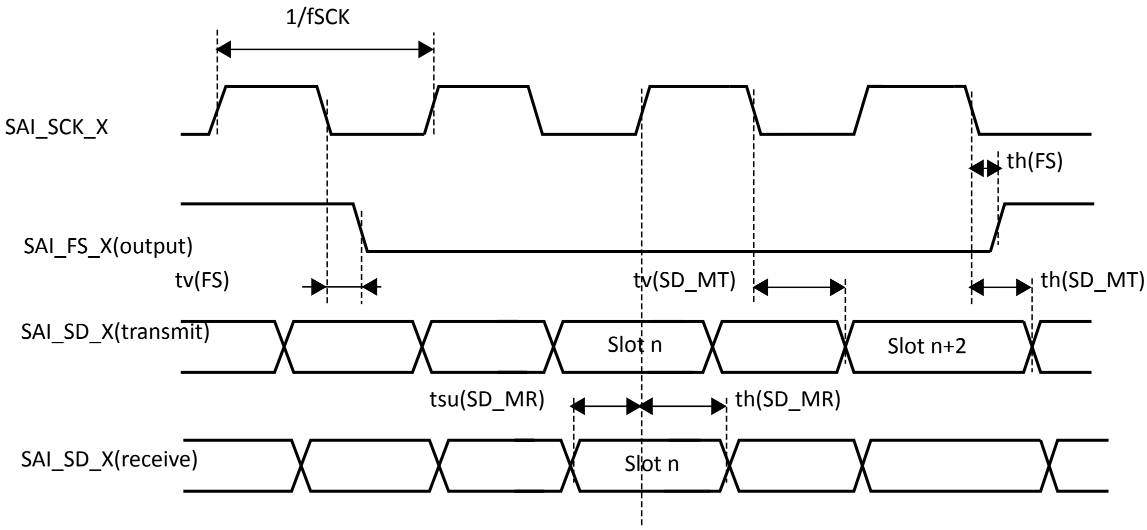
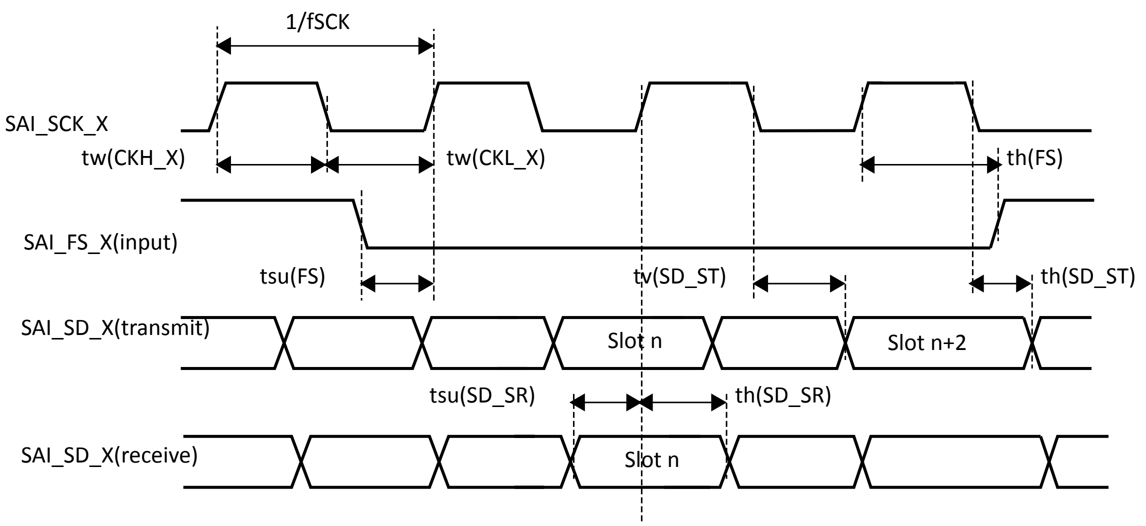


Figure 74. SAI slave timing waveforms



6.3.36.6 *MDIO characteristics*

Unless otherwise specified, the parameters given in Table 121 are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in Table 22. General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- I/O compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS0

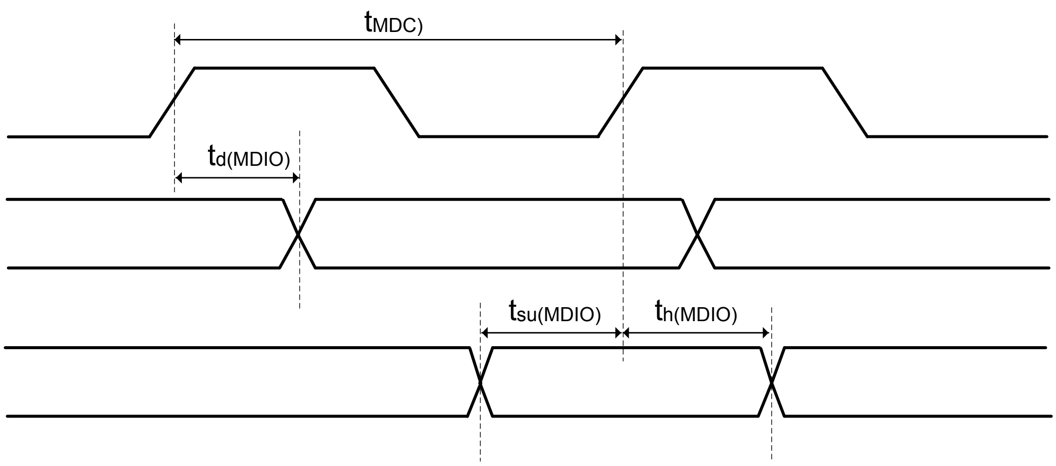
Note: At VOS1, the performance can be degraded by up to 5 % compared to VOS0. This is indicated by a footnote when applicable.

Table 121. **MDIO Slave timing parameters**

Symbol	Parameter	Min	Typ	Max(1)	Unit
F_{MDC}	Management Data Clock	-	-	30	MHz
$t_{d(MDIO)}$	Management Data Iput/output output valid time	9	11	21	ns
$t_{su(MDIO)}$	Management Data Iput/output setup time	2.5	-	-	
$t_{h(MDIO)}$	Management Data Iput/output hold time	1	-	-	

1. At VOS1, these values are degraded by up to 5 %.

Figure 75. **MDIO Slave timing diagram**



6.3.36.7 *SD/SDIO MMC card host interface (SDMMC) characteristics*

Unless otherwise specified, the parameters given in Table 122 and Table 123 for SDIO are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage summarized in Table 22. General operating conditions and Section 6.3.1 , with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS0

Note: At VOS1, the performance can be degraded by up to 5 % compared to VOS0. This is indicated by a footnote when applicable.

Refer to Section 6.3.16 I/O port characteristics for more details on the input/output characteristics.

Table 122. **Dynamics characteristics: SDMMC characteristics, V_{DD}=2.7 to 3.6 V**

Above 100 MHz, C_L = 20 pF.

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)(2)	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	133	MHz
-	SDIO_CK/f_{PCLK2} frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} =52 MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} =52 MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR/DDR mode						

Symbol	Parameter	Conditions	Min[1]	Typ[1]	Max[1][2]	Unit
t_{ISU}	Input setup time HS	-	2.5	-	-	ns
t_{IH}	Input hold time HS	-	0.5	-	-	
t_{IDW}[3]	Input valid window (variable window)	-	3.0	-	-	-
CMD, D outputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR/DDR mode						
t_{OV}	Output valid time HS	-	-	6	6.5	ns
t_{OH}	Output hold time HS	-	5	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	-	2.5	-	-	ns
t_{IHD}	Input hold time SD	-	0.5	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	-	-	1	1.5	ns
t_{OHD}	Output hold default time SD	-	0	-	-	

1. *Guaranteed by characterization results.*
2. *At VOS1, these values are degraded by up to 5 %.*
3. *The minimum window of time where the data needs to be stable for proper sampling in tuning mode.*

Table 123. Dynamics characteristics: eMMC characteristics VDD=1.71V to 1.9V

Above 100 MHz, C_L = 20 pF.

Symbol	Parameter	Conditions	Min[1]	Typ[1]	Ma[1][2]	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	85	MHz
$t_{W(CKL)}$	Clock low time	f_{PP} =52 MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} =52 MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	-	2.5	-	-	ns
t_{IH}	Input hold time HS	-	0.5	-	-	
t_{IDW}[3]	Input valid window (variable window)	-	3.5	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OVD}	Output valid time HS	-	-	6	6.5	ns
t_{OHD}	Output hold time HS	-	5.5	-	-	

1. *Guaranteed by characterization results.*
2. *At VOS1, these values are degraded by up to 5 %.*
3. *The minimum window of time where the data needs to be stable for proper sampling in tuning mode.*

Figure 76. SDIO high-speed mode

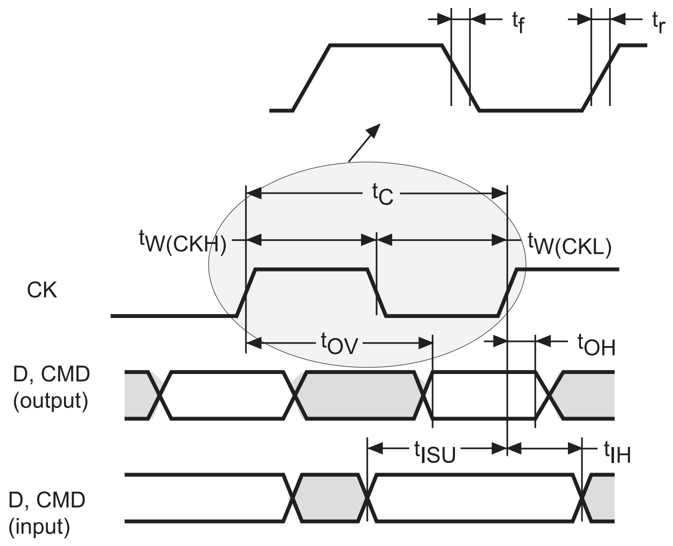


Figure 77. SD default mode

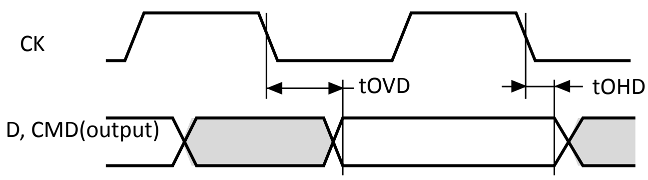
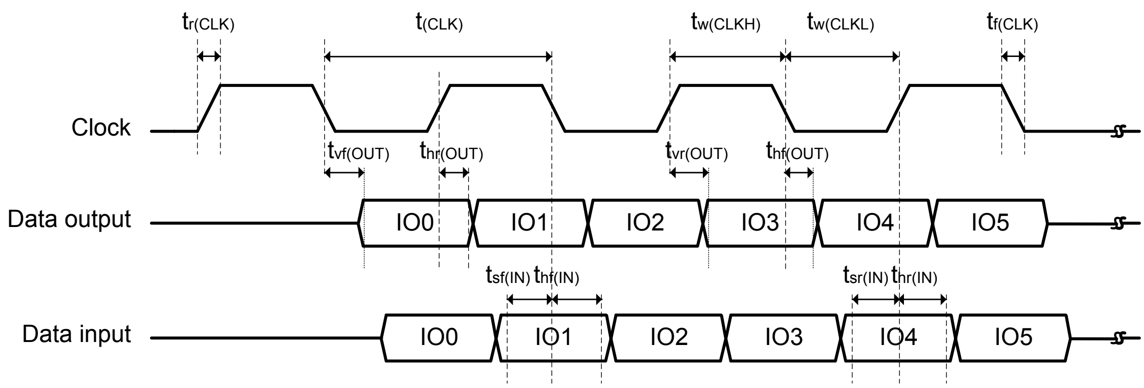


Figure 78. DDR mode



6.3.36.8 USB OTG_FS characteristics

Unless otherwise specified, the parameters given in Table 124. Dynamics characteristics: USB OTG_FS for ULPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage summarized in Table 22. General operating conditions and Section 6.3.1 , with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L=20 pF

- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- VOS level set to VOS0

Refer to Section 6.3.16 I/O port characteristics for more details on the input/output characteristics.

Table 124. Dynamics characteristics: USB OTG_FS

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{DD33USB}$	USB transceiver operating voltage	-	3.0[1]	-	3.6	V
R_{PUI}	Embedded USB_DP pull-up value during idle	-	900	1250	1600	Ω
R_{PUR}	Embedded USB_DP pull-up value during reception	-	1400	2300	3200	
Z_{DRV}	Output driver impedance[2]	Driver high and low	28	36	44	

1. *The USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics that are degraded in the 2.7 to 3.0 V voltage range.*
2. *No external termination series resistors are required on USB_DP (D+) and USB_DM (D-); the matching impedance is already included in the embedded driver.*

6.3.36.9 *USB OTG_HS characteristics*

Unless otherwise specified, the parameters given in Table 125 for ULPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage summarized in Table 22. General operating conditions and Section 6.3.1 , with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L=20 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- VOS level set to VOS0

Note: At VOS1, the performance can be degraded by up to 5 % compared to VOS0. This is indicated by a footnote when applicable.

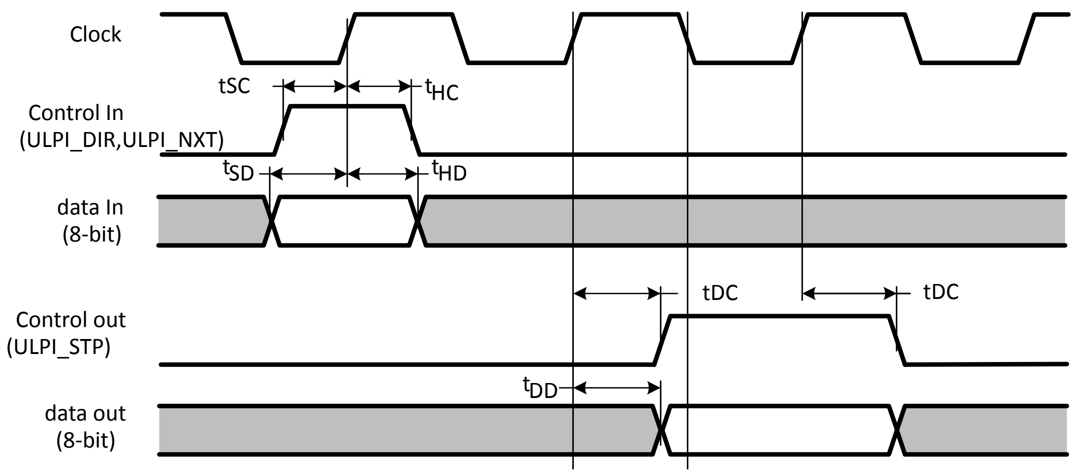
Refer to Section 6.3.16 I/O port characteristics for more details on the input/output characteristics.

Table 125. Dynamics characteristics: USB ULPI

Symbol	Parameter	Condition	Min[1]	Typ[1]	Max[1][2][3]	Unit
t_{SC}	Control in (ULPI_DIR , ULPI_NXT) setup time	-	3.5	-	-	ns
t_{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	-	2	-	-	
t_{SD}	Data in setup time	-	3	-	-	
t_{HD}	Data in hold time	-	0	-	-	
t_{DC}/t_{DD}	Control/Datal output delay	$2.7 < V_{DD} < 3.6$ V, C_L=20 pF	-	7	8.5	
		$1.71 < V_{DD} < 3.6$ V, C_L=15 pF	-	9	13	

1. *Guaranteed by characterization results.*
2. *At VOS1, these values are degraded by up to 5 %.*
3. *For external ULPI transceivers operating at 1.8 V, check carefully the timing values for compatibility.*

Figure 79. **ULPI timing diagram**



6.3.36.10 *JTAG/SWD interface characteristics*

Unless otherwise specified, the parameters given in Table 126 and Table 127 for JTAG/SWD are derived from tests performed under the ambient temperature, $f_{rcc\_cpu\_ck}$ frequency and V_{DD} supply voltage summarized in Table 22. General operating conditions and Section 6.3.1 , with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- VOS level set to VOS0

Note: *At VOS1, the performance can be degraded by up to 5 % compared to VOS0. This is indicated by a footnote when applicable.*

Refer to Section 6.3.16 I/O port characteristics for more details on the input/output characteristics:

Table 126. **Dynamics JTAG characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max[(1)]	Unit
F_{pp}	T_{CK} clock frequency	2.7 V <V_{DD}< 3.6 V	-	-	35	MHz
$1/t_{c(TCK)}$		1.62 V <V_{DD}< 3.6 V	-	-	27.5	ns
$t_{isu(TMS)}$	TMS input setup time	-	1	-	-	
$t_{ih(TMS)}$	TMS input hold time	-	1	-	-	
$t_{isu(TDI)}$	TDI input setup time	-	1.5	-	-	
$t_{ih(TDI)}$	TDI input hold time	-	1	-	-	
$t_{ov(TDO)}$	TDO output valid time	2.7 V <V_{DD}< 3.6 V	-	8	14	
		1.62 V <V_{DD}< 3.6 V	-	8	18	
$t_{oh(TDO)}$	TDO output hold time	-	7	-	-	

1. *At VOS1, these values are degraded by up to 5 %.*

Table 127. **Dynamics SWD characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max[(1)]	Unit
F_{pp}	SWCLK clock frequency	2.7V <V_{DD}< 3.6 V	-	-	76	MHz
$1/t_{c(SWCLK)}$		1.62 <V_{DD}< 3.6 V	-	-	55.5	

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
$t_{isu(SWDIO)}$	SWDIO input setup time	-	2	-	-	ns
$t_{ih(SWDIO)}$	SWDIO input hold time	-	1	-	-	
$t_{ov(SWDIO)}$	SWDIO output valid time	2.7V < V_{DD} < 3.6 V	-	8.5	13	
		1.62 < V_{DD} < 3.6 V	-	8.5	18	
$t_{oh(SWDIO)}$	SWDIO output hold	-	8	-	-	

1. *At VOS1, these values are degraded by up to 5 %.*

Figure 80. JTAG timing diagram

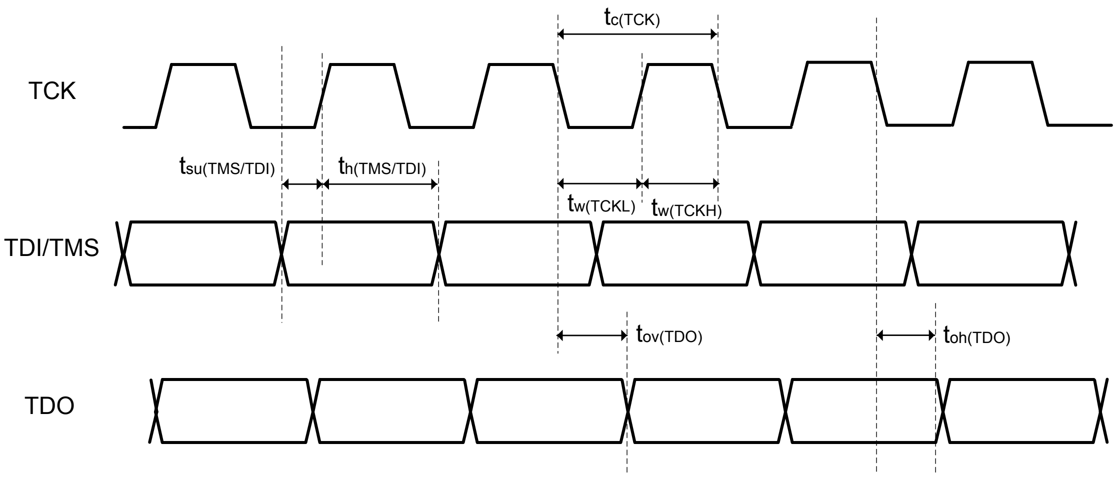
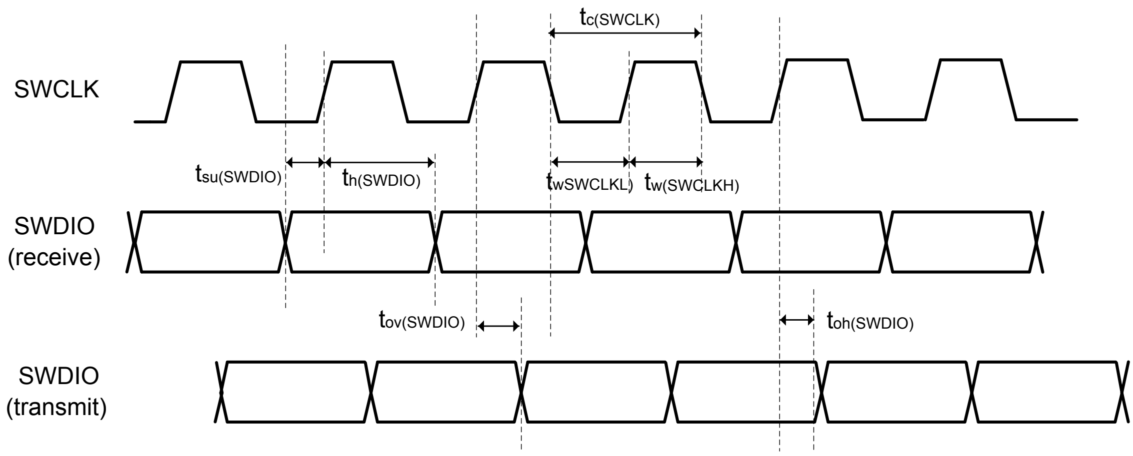


Figure 81. SWD timing diagram



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 LQFP64 package information

This is a 64-pins, 10 x 10 mm, low-profile quad flat package.

Note: *See list of notes in the notes section.*

Figure 82. LQFP64 - Outline(15.)

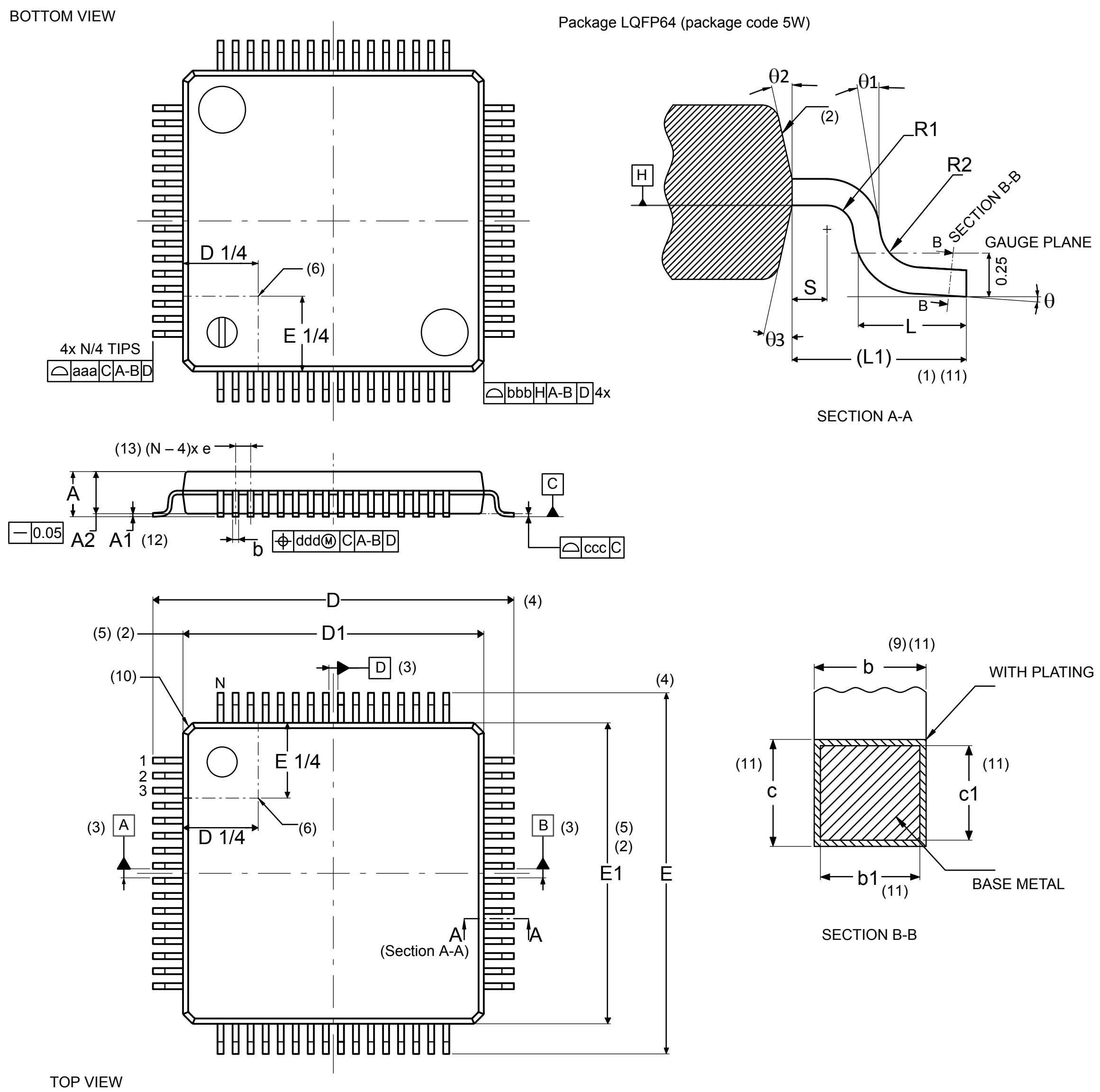


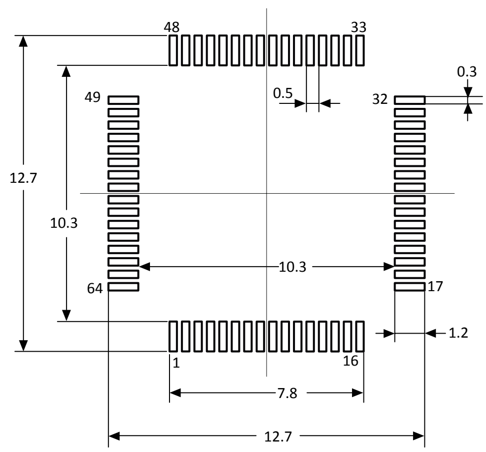
Table 128. **LQFP64 - Mechanical data**

Symbol	millimeters			inches[14.]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12.]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9.][11.]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11.]	0.17	0.20	0.23	00067	0.0079	0.0091
c[11.]	0.09	-	0.20	0.0035	-	0.0079
c1[11.]	0.09	-	0.16	0.0035	-	0.0063
D[4.]	12.00 BSC			0.4724 BSC		
D1[2.][5.]	10.00 BSC			0.3937 BSC		
E[4.]	12.00 BSC			0.4724 BSC		
E1[2.][5.]	10.00 BSC			0.3937 BSC		
e	0.500 BSC			0.0197 BSC		
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
N[13.]	64					
Θ	0°	3.5°	7°	0°	3.5°	7°
Θ1	0°	-	-	0°	-	-
Θ2	10°	12°	14°	10°	12°	14°
Θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1.]	0.20			0.0079		
bbb[1.]	0.20			0.0079		
ccc[1.]	0.08			0.0031		
ddd[1.]	0.08			0.0031		

Notes

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 83. LQFP64 - Recommended footprint



1. Dimensions are expressed in millimeters.

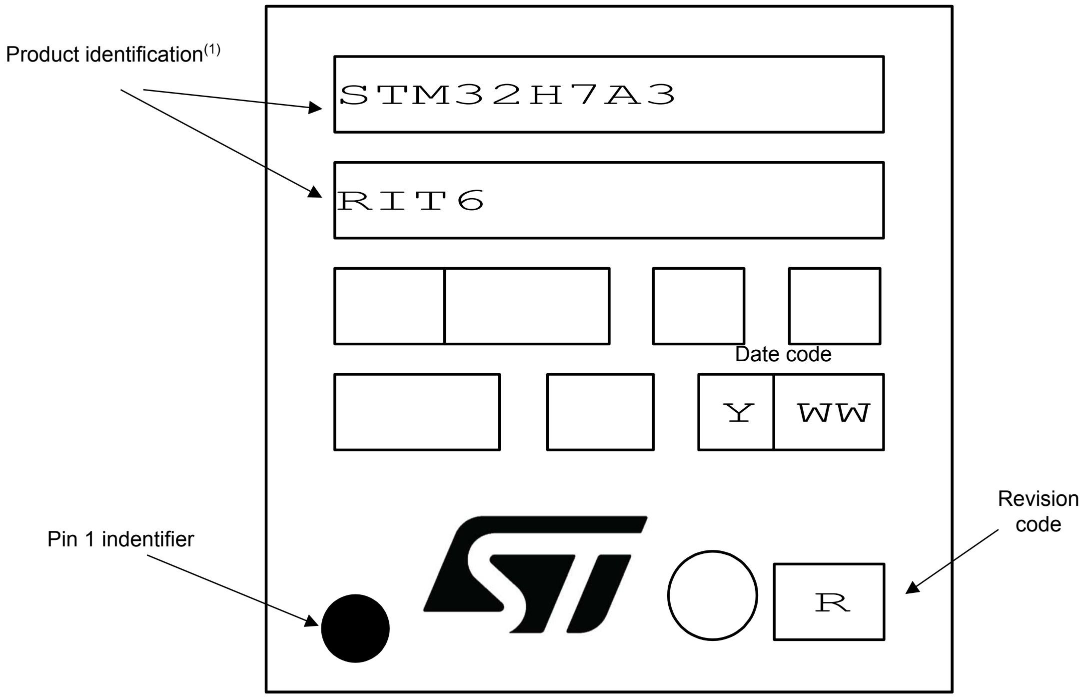
7.1.1 Device marking for LQFP64

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 84. LQFP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.2 LQFP100 package information

This LQFP is a 100 pins, 14 x 14 mm, low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 85. LQFP100 - Outline(15.)

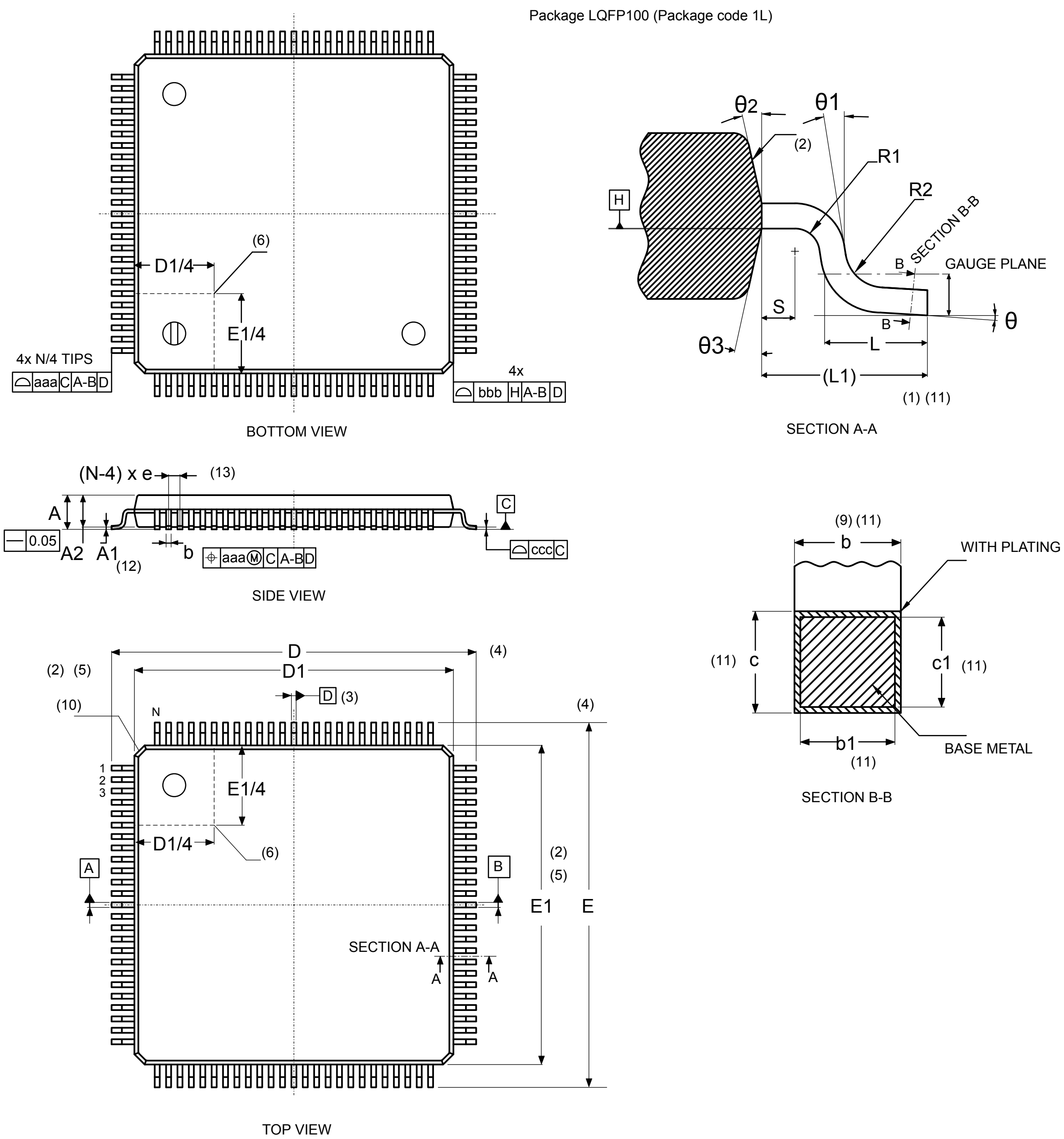


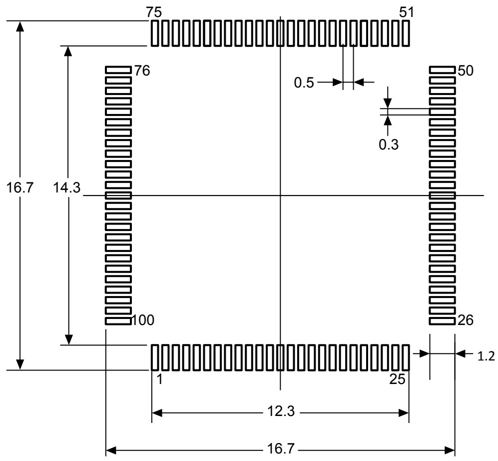
Table 129. LQFP100 - Mechanical data

Symbol	millimeters			inches[14.]		
	Min	Typ	Max	Min	Typ	Max
A	-	1.50	1.60	-	0.0590	0.0630
A1[12.]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9.][11.]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11.]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11.]	0.09	-	0.20	0.0035	-	0.0079
c1[11.]	0.09	-	0.16	0.0035	-	0.0063
D[4.]	16.00 BSC			0.6299 BSC		
D1[2.][5.]	14.00 BSC			0.5512 BSC		
E[4.]	16.00 BSC			0.6299 BSC		
E1[2.][5.]	14.00 BSC			0.5512 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1[1.][11.]	-	1.00	-	-	0.0394	-
N[13.]	100					
Θ	0°	3.5°	7°	0°	3.5°	7°
Θ1	0°	-	-	0°	-	-
Θ2	10°	12°	14°	10°	12°	14°
Θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1.]	0.20			0.0079		
bbb[1.]	0.20			0.0079		
ccc[1.]	0.08			0.0031		
ddd[1.]	0.08			0.0031		

Notes

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 86. LQFP100 - Recommended footprint



1. Dimensions are expressed in millimeters.

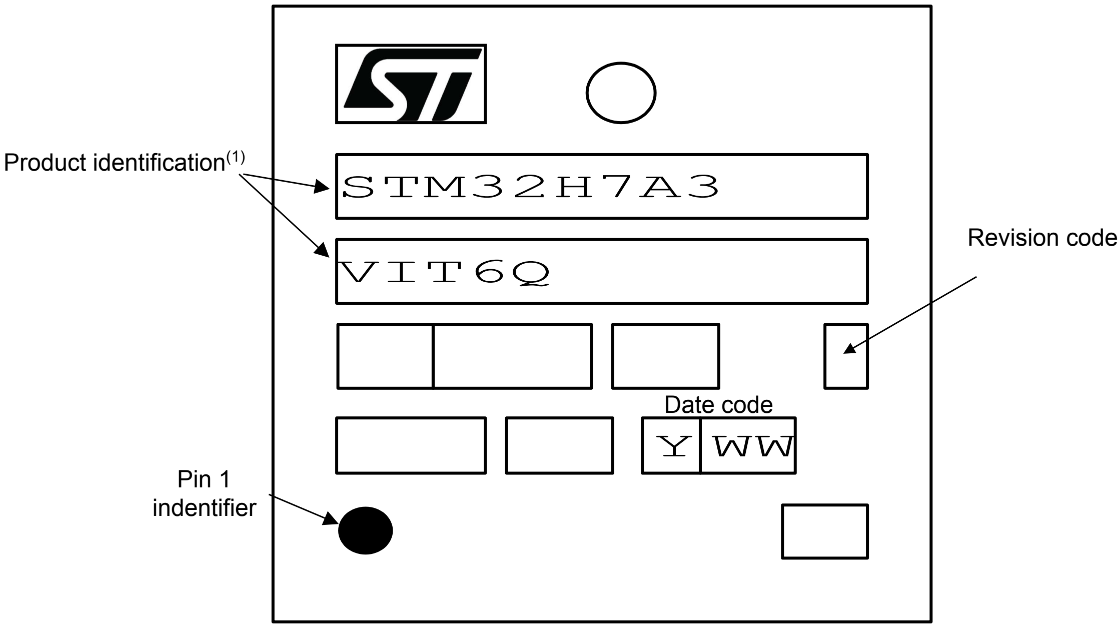
7.2.1 Device marking for LQFP100

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 87. **LQFP100 marking example (package top view)**

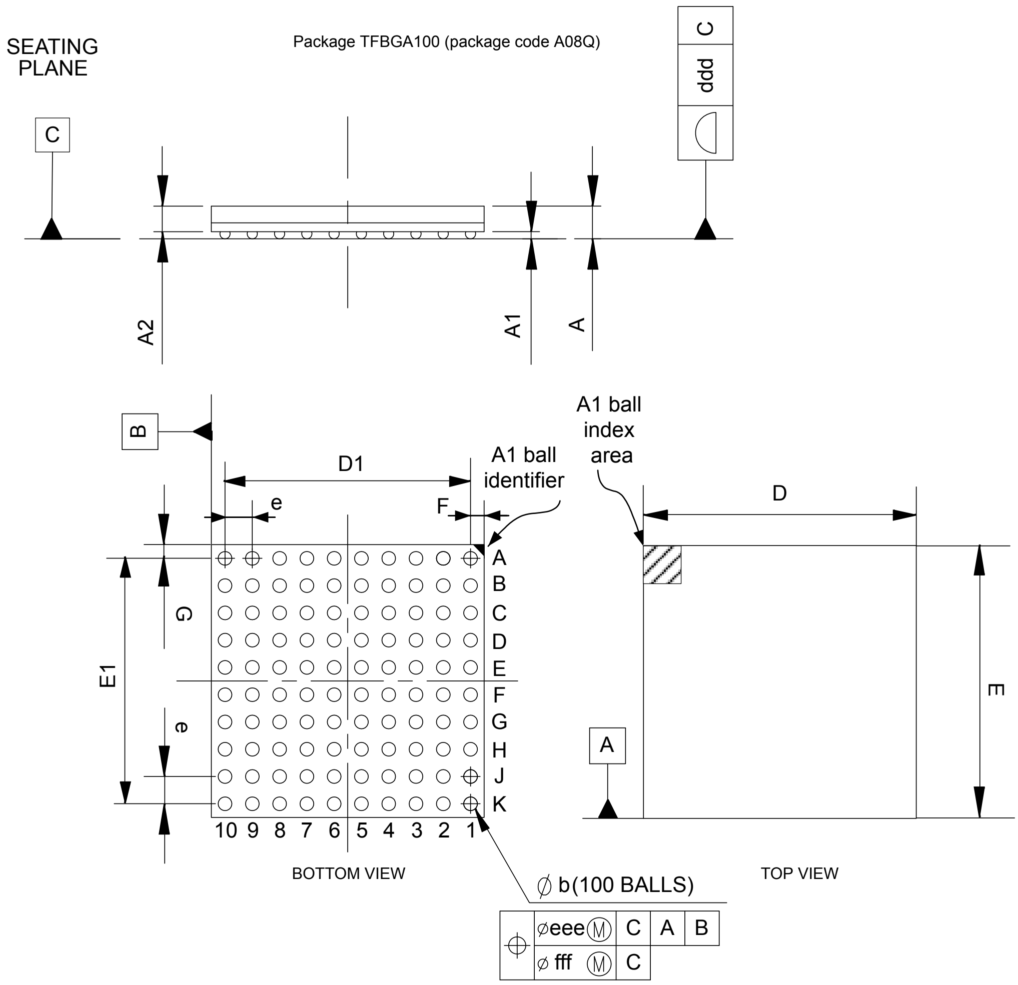


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.3 TFBGA100 package information

This TFBGA is a 100 ball, 8 x 8 mm, 0.8 mm pitch, thin profile fine pitch ball grid array package.

Figure 88. TFBGA100 - Outline



1. Drawing is not to scale

Table 130. **TFBGA100 - Mechanical data**

Symbol	millimeters			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
A[(2)]	-	-	1.100	-	-	0.0433
A1[(3)]	0.150	-	-	0.0059	-	-
A2	-	0.760	-	-	0.0299	-
b[(4)]	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	7.850	8.000	8.150	0.3091	0.3150	0.3209
D1	-	7.200	-	-	0.2835	-
E	7.850	8.000	8.150	0.3091	0.3150	0.3209
E1	-	7.200	-	-	0.2835	-
e	-	0.800	-	-	0.0315	-
F	-	0.400	-	-	0.0157	-
G	-	0.400	-	-	0.0157	-
ddd	-	-	0.100	-	-	0.0039
eee[(5)]	-	-	0.150	-	-	0.0059
fff[(6)]	-	-	0.080	-	-	0.0031

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*
2. *The total profile height (Dim A) is measured from the seating plane to the top of the component.*
3. - *The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metalized markings, or other feature of package body or integral heat slug.*
   - *A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.*
4. *Initial ball equal 0.350mm.*
5. *The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.*
6. *The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above The axis of each ball must lie simultaneously in both tolerance zones.*

Figure 89. **TFBGA100 - Recommended footprint**

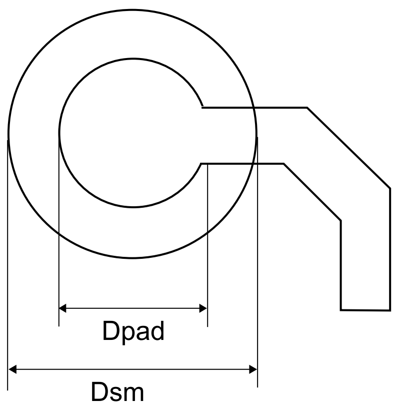


Table 131. **TFBGA100 - Recommended PCB design rules (0.8 mm pitch BGA)**

Dimension	Recommended values
Pitch	0.8
Dpad	0.400 mm
Dsm	0.470 mm typical (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

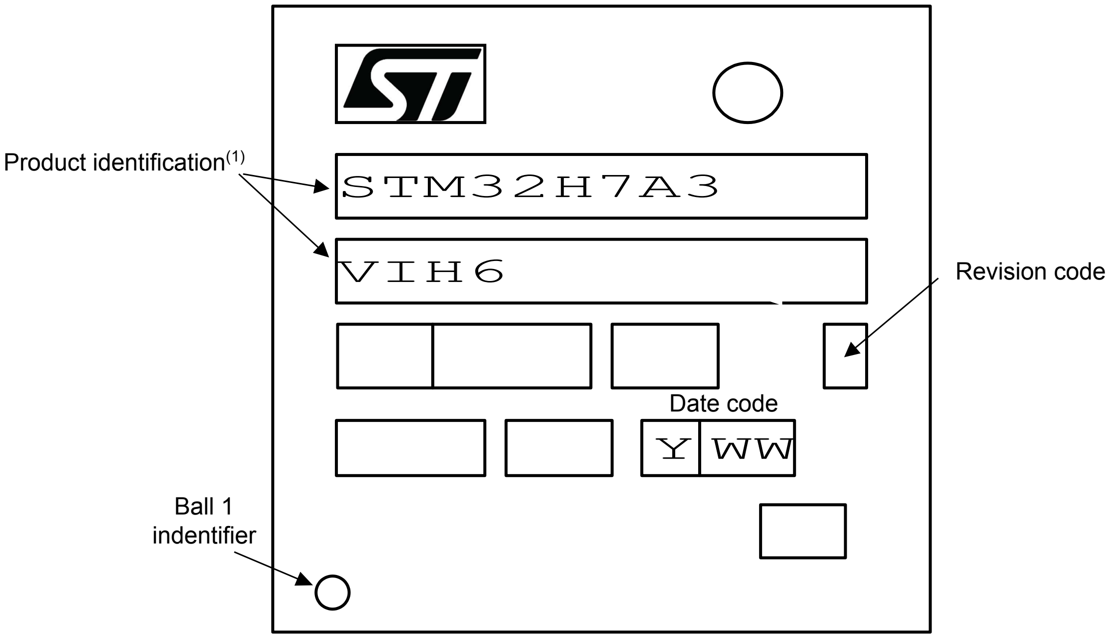
7.3.1 Device marking for TFBGA100

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 90. TFBGA100 marking example (package top view)

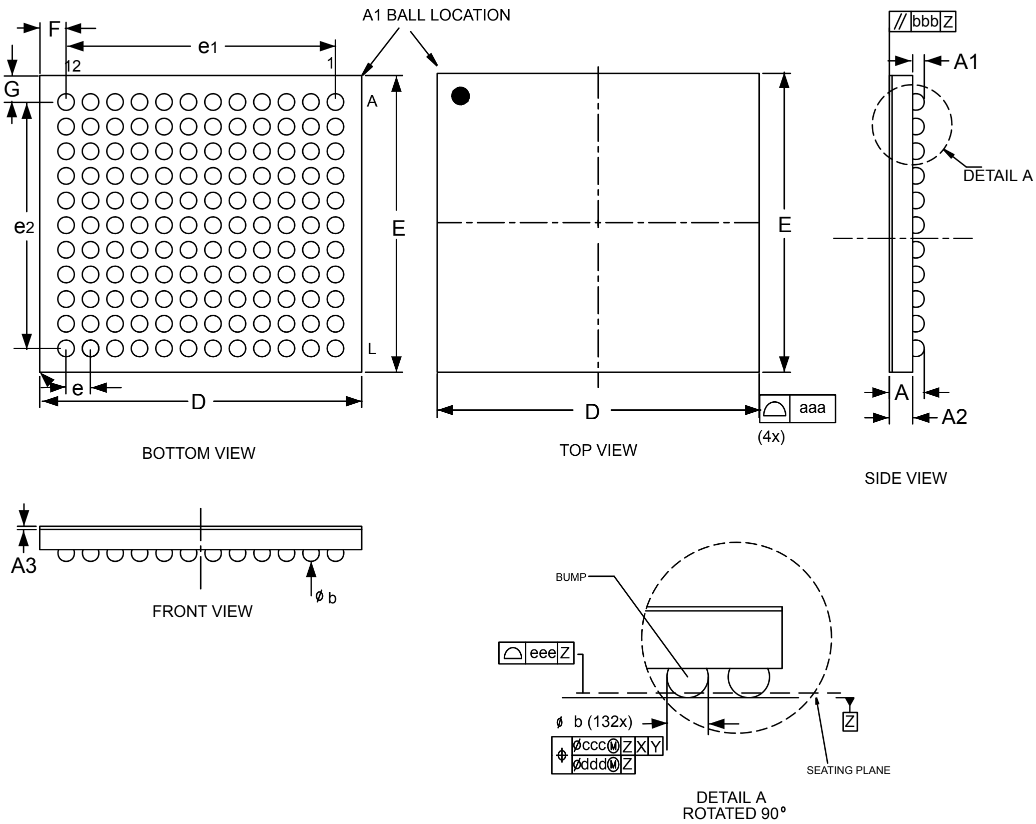


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.4 WLCSP132 package information

WLCSP132 is a 132 balls, 4.57 x 4.37 mm, 0.35 mm pitch, wafer level chip scale package.

Figure 91. WLCSP132 - Outline



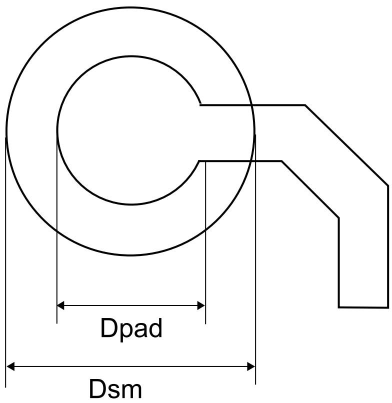
1. Drawing is not to scale.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.

Table 132. **WLCSP132 - Mechanical data**

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.58	-	-	0.023
A1	-	0.17	-	-	0.007	-
A2	-	0.38	-	-	0.015	-
A3	-	0.025	-	-	0.001	-
b	0.21	0.24	0.27	0.008	0.009	0.011
D	4.54	4.57	4.60	0.179	0.180	0.181
E	4.35	4.37	4.39	0.171	0.172	0.173
e	-	0.35	-	-	0.014	-
e1	-	3.85	-	-	0.152	-
e2	-	3.50	-	-	0.138	-
F[2]	-	0.360	-	-	0.014	-
G[2]	-	0.435	-	-	0.017	-
aaa	-	0.10	-	-	0.004	-
bbb	-	0.10	-	-	0.004	-
ccc	-	0.10	-	-	0.004	-
ddd	-	0.05	-	-	0.002	-
eee	-	0.05	-	-	0.002	-

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*
2. *Calculated dimensions are rounded to the 3rd decimal place*

Figure 92. **WLCSP132 - Recommended footprint**



1. Dimensions are expressed in millimeters.

Table 133. **WLCSP132 - Recommended PCB design rules**

Dimension	Recommended values
Pitch	0.35 mm
Dpad	0,200 mm
Dsm	0.200 mm typ. (depends on soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.080 mm

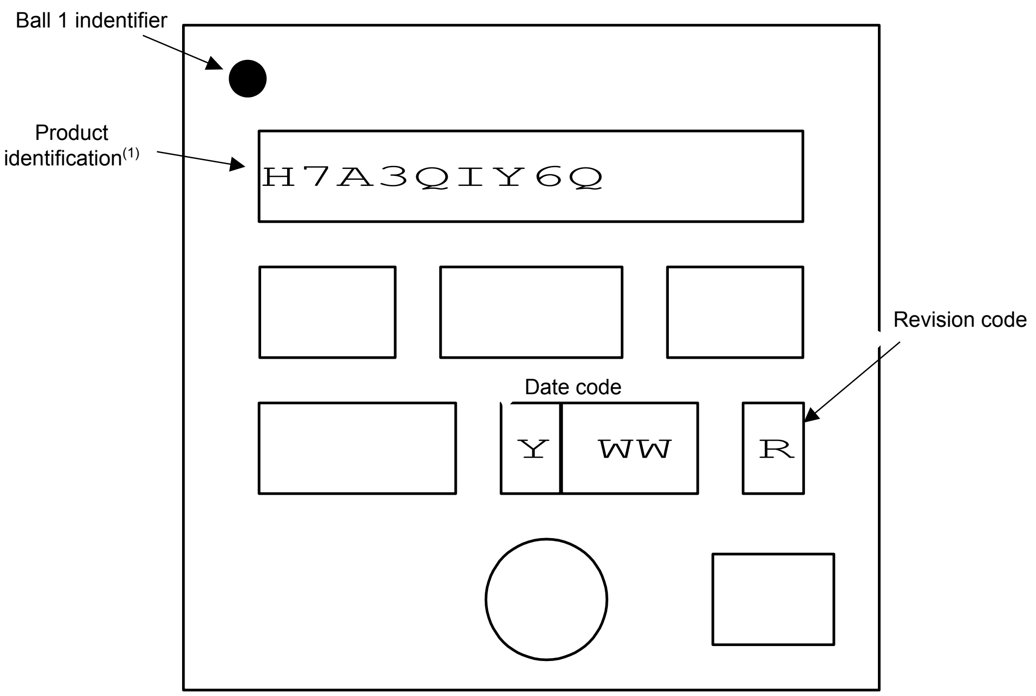
7.4.1 Device marking for WLCSP132

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 93. **WLCSP132 marking example (package top view)**



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.5 LQFP144 package information

LQFP144 is a 144-pin, 20 x 20 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 94. LQFP144 - Outline(15.)

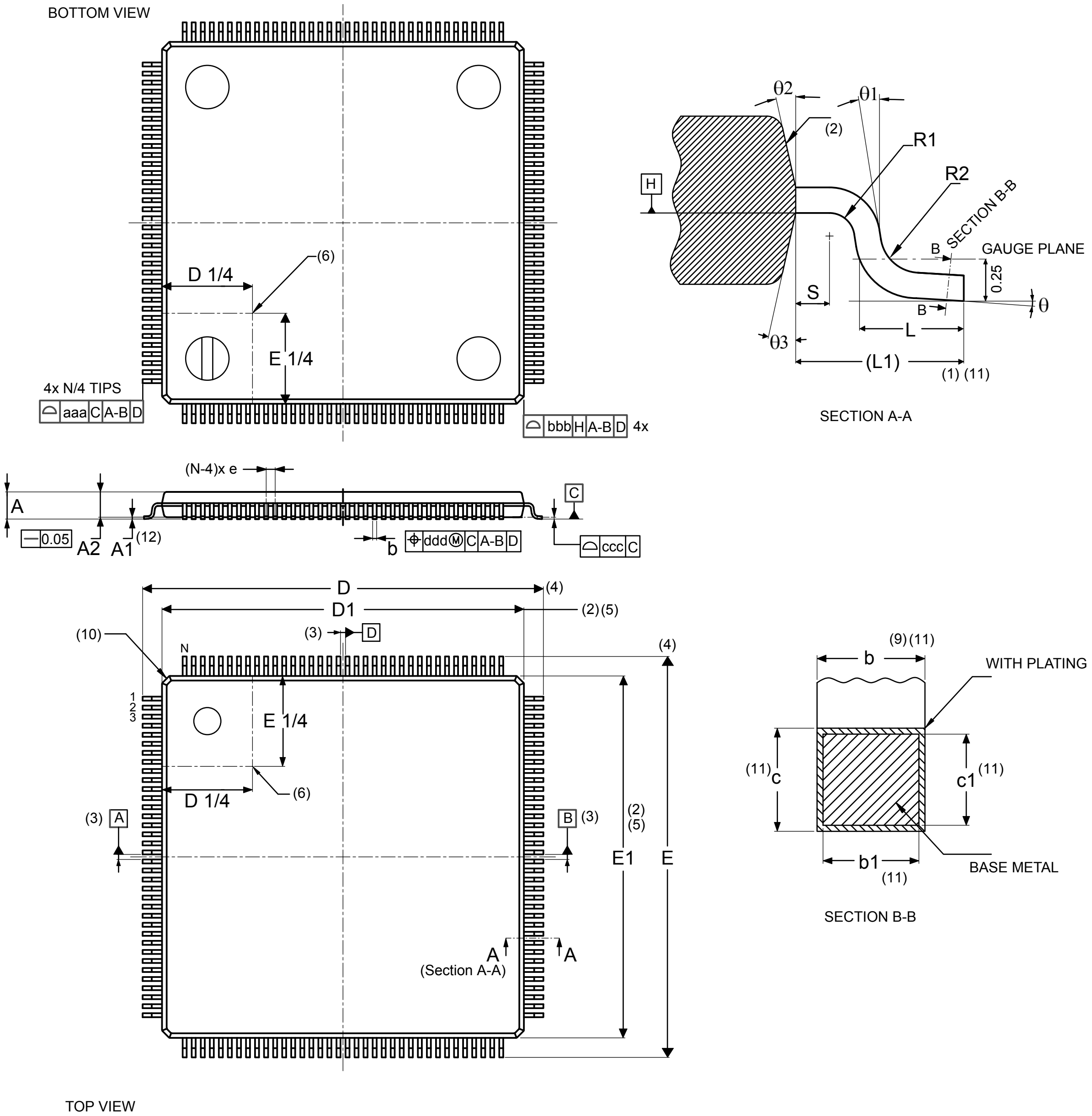


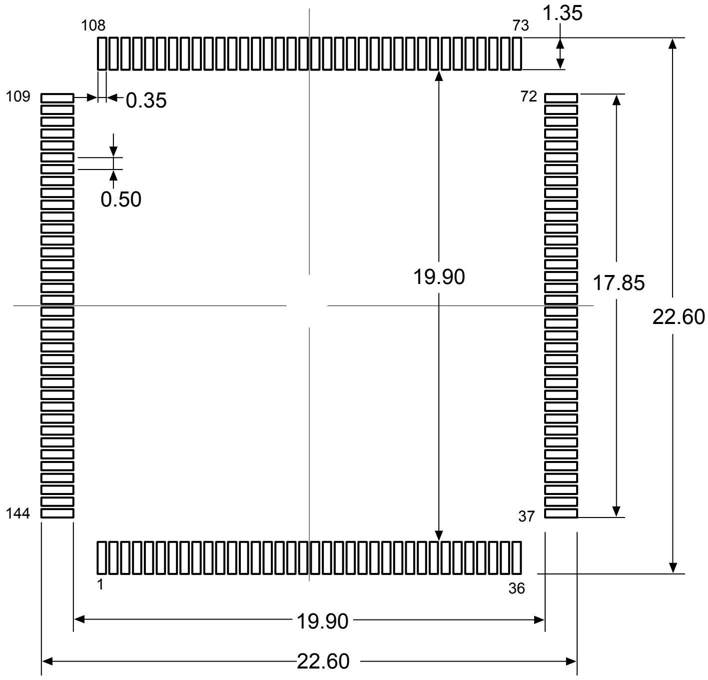
Table 134. **LQFP144 - Mechanical data**

Symbol	millimeters			inches[14.]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12.]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9.][11.]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11.]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11.]	0.09	-	0.20	0.0035	-	0.0079
c1[11.]	0.09	-	0.16	0.0035	-	0.0063
D[4.]	22.00 BSC			0.8661 BSC		
D1[2.][5.]	20.00 BSC			0.7874 BSC		
E[4.]	22.00 BSC			0.8661 BSC		
E1[2.][5.]	20.00 BSC			0.7874 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13.]	144					
Θ	0°	3.5°	7°	0°	3.5°	7°
Θ1	0°	-	-	0°	-	-
Θ2	10°	12°	14°	10°	12°	14°
Θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa	0.20			0.0079		
bbb	0.20			0.0079		
ccc	0.08			0.0031		
ddd	0.08			0.0031		

Notes:
1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.

10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 95. LQFP144 - Recommended footprint



1. Dimensions are expressed in millimeters.

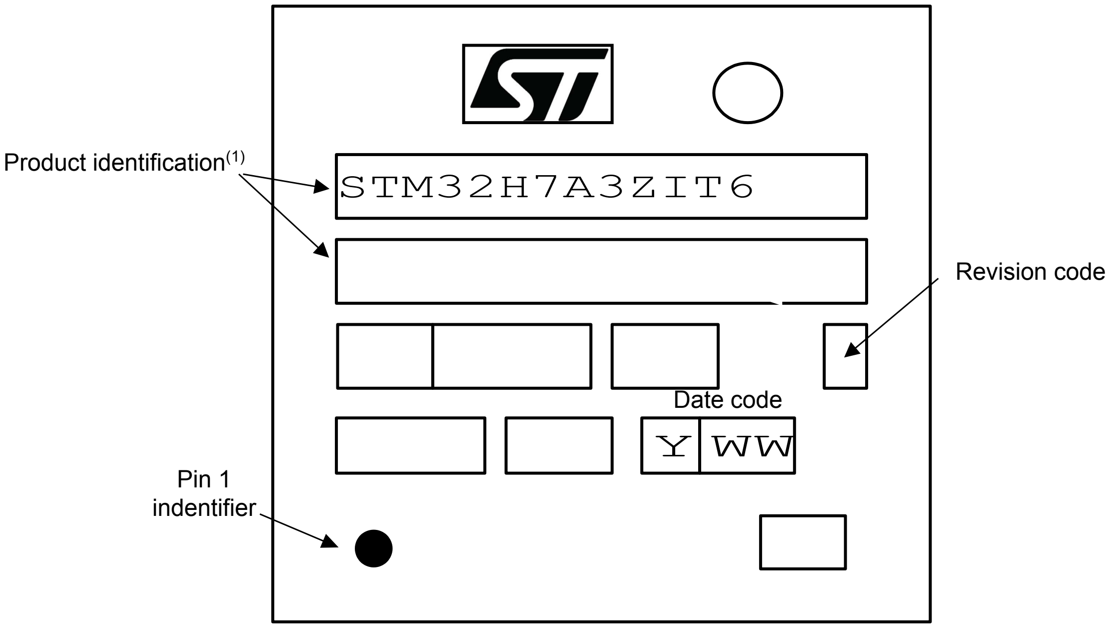
7.5.1 Device marking for LQFP144

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 96. LQFP144 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.6 LQFP176 package information

This LQFP is a 176-pin, 24 x 24 mm, 0.5 mm pitch, low profile quad flat package.

Note: See list of notes in the notes section.

Figure 97. LQFP176 - Outline(15.)

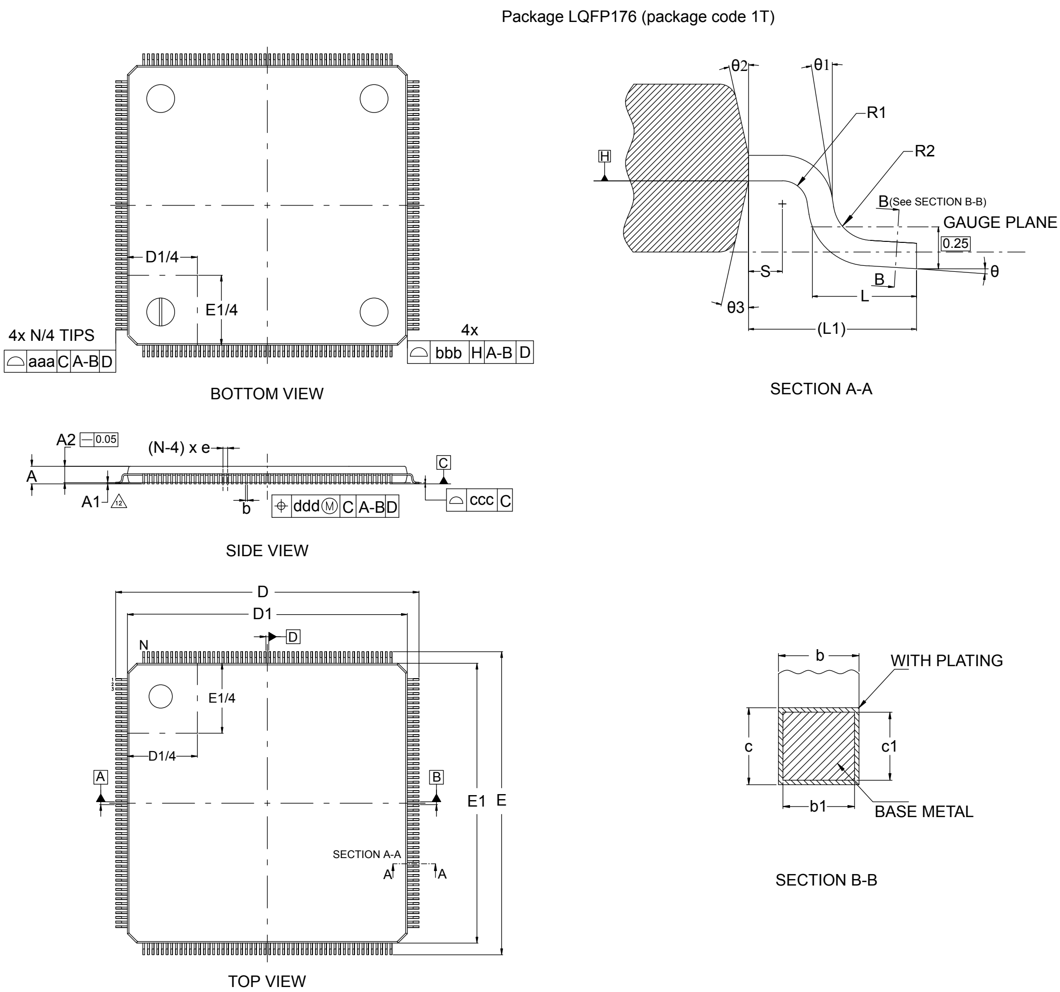


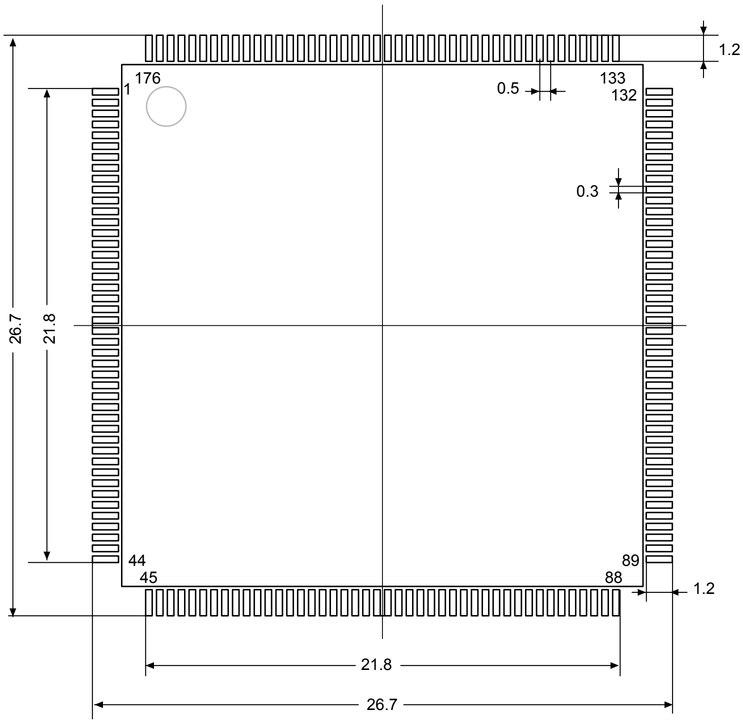
Table 135. LQFP176 - Mechanical data

Symbol	millimeters			inches[14.]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1[12.]	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b[9.][11.]	0.170	0.220	0.270	0.0067	0.0087	0.0106
b1[11.]	0.170	0.200	0.230	0.0067	0.0079	0.0091
c[11.]	0.090	-	0.200	0.0035	-	0.0079
c1[11.]	0.090	-	0.160	0.0035	-	0.063
D[4.]	26.000			1.0236		
D1[2.][5.]	24.000			0.9449		
E[4.]	26.000			0.0197		
E1[2.][5.]	24.000			0.9449		
e	0.500			0.1970		
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1[1.][11.]	1 REF			0.0394 REF		
N[13.]	176					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.080	-	-	0.0031	-	-
R2	0.080	-	0.200	0.0031	-	0.0079
S	0.200	-	-	0.0079	-	-
aaa[1.]	0.200			0.0079		
bbb[1.]	0.200			0.0079		
ccc[1.]	0.080			0.0031		
ddd[1.]	0.080			0.0031		

Notes

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 98. LQFP176 - Recommended footprint



Note: Dimensions are expressed in millimeters.

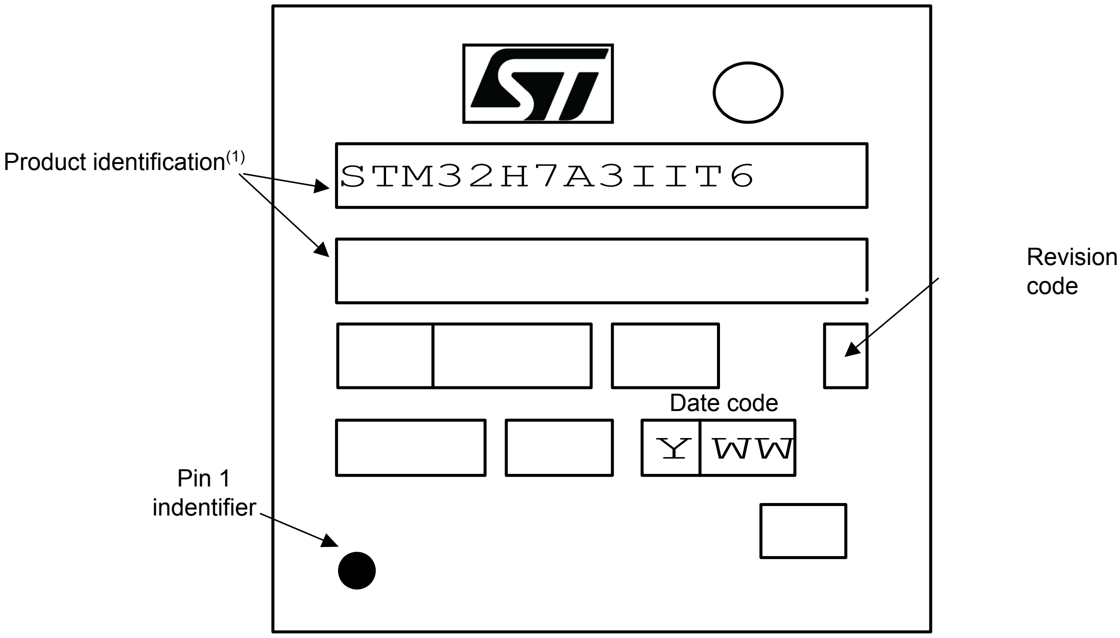
7.6.1 Device marking for LQFP176

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 99. **LQFP176 marking example (package top view)**

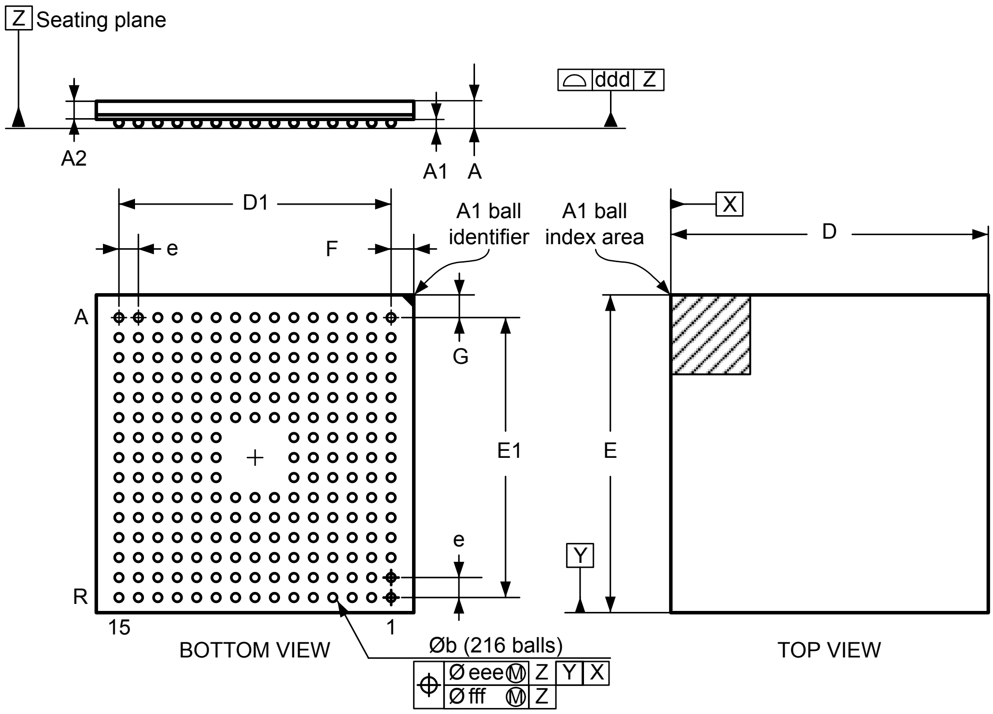


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.7 TFBGA216 package information

This TFBGA is a 216 ball, 13x13 mm, 0.8 mm pitch, fine pitch ball grid array package.

Figure 100. TFBGA216 - Outline



1. Drawing is not to scale.
2. – The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug.
   – A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

Table 136. **TFBGA216 - Mechanical data**

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1[2]	0.150	-	-	0.0059	-	-
A2	-	0.760	-	-	0.0299	-
b[3]	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	12.850	13.000	13.150	0.5059	0.5118	0.5177
D1	-	11.200	-	-	0.4409	-
E	12.850	13.000	13.150	0.5059	0.5118	0.5177
E1	-	11.200	-	-	0.4409	-
e	-	0.800	-	-	0.0315	-
F	-	0.900	-	-	0.0354	-
G	-	0.900	-	-	0.0354	-
ddd	-	-	0.100	-	-	0.0039
eee[4]	-	-	0.150	-	-	0.0059
fff[5]	-	-	0.080	-	-	0.0031

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. - *The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug.*
   - *A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.*
3. *Initial ball equal 0.350 mm.*
4. *The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.*
5. *The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above The axis of each ball must lie simultaneously in both tolerance zones.*

Figure 101. **TFBGA216 - Recommended footprint**

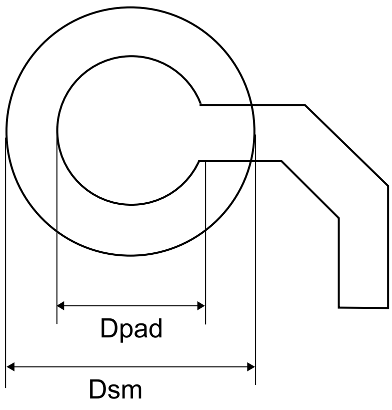


Table 137. TFBGA216 - Recommended PCB design rules (0.8 mm pitch)

Dimension	Recommended values
Pitch	0.8 mm
Dpad	0.400 mm
Dsm	0.470 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

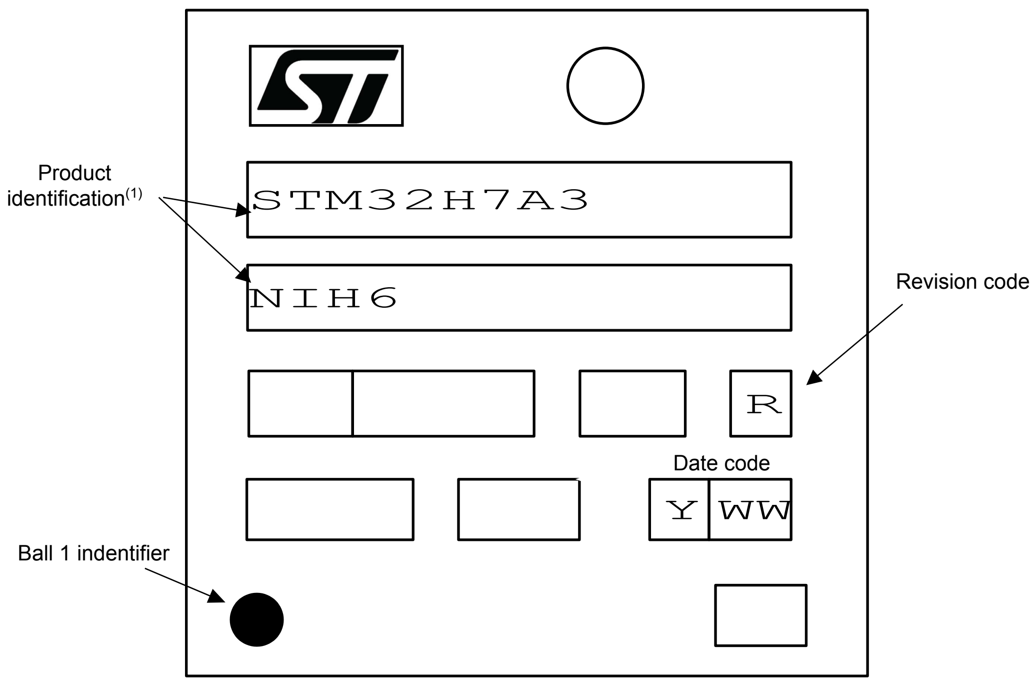
7.7.1 Device marking for TFBGA216

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 102. TFBGA216 marking example (package top view)

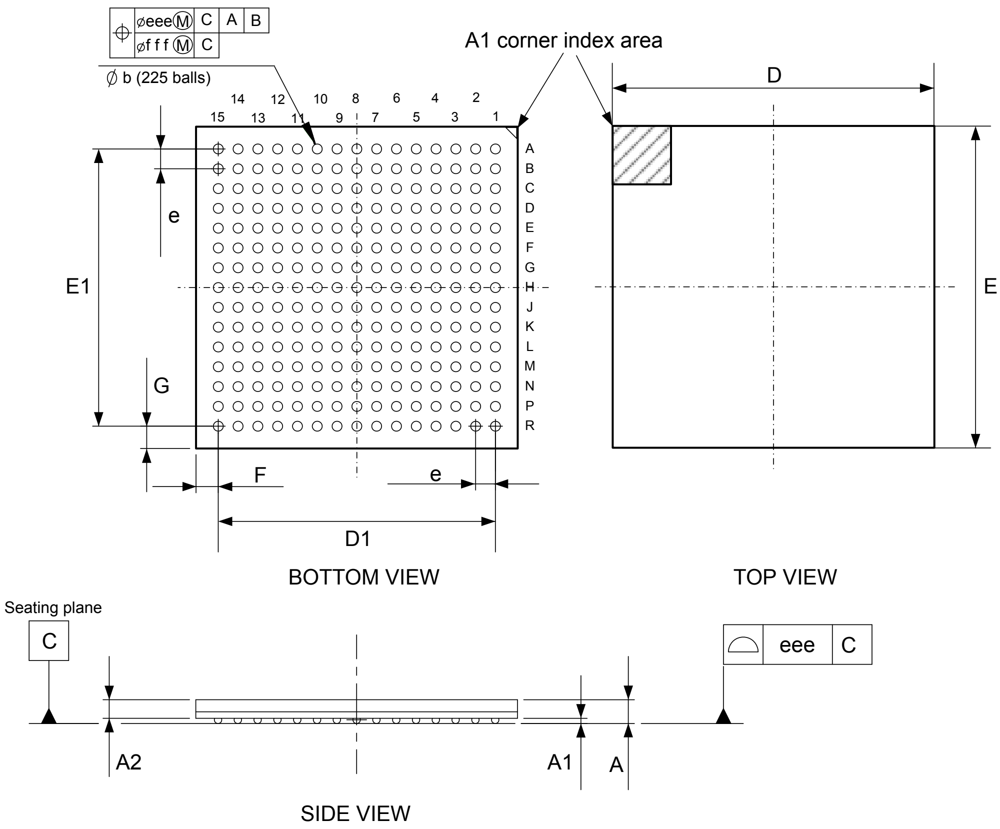


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.8 TFBGA225 package information

This TFBGA is a 225 ball, 13x13 mm, 0.8 mm pitch, fine pitch ball grid array package.

Figure 103. TFBGA225 - Outline



1. Drawing is not to scale.
2. – The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug.
   – A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

Table 138. **TFBGA225 - Mechanical data**

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A(2)	-	-	1.200	-	-	0.0472
A1(3)	0.150	-	-	0.0059	-	-
A2	-	0.760	-	-	0.0299	-
b(4)	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	12.850	13.000	13.150	0.5059	0.5118	0.5177
D1	-	11.200	-	-	0.4409	-
E	12.850	13.000	13.150	0.5059	0.5118	0.5177
E1	-	11.200	-	-	0.4409	-
e	-	0.800	-	-	0.0315	-
F	-	0.900	-	-	0.0354	-
G	-	0.900	-	-	0.0354	-
ddd	-	-	0.100	-	-	0.0039
eee(5)	-	-	0.150	-	-	0.0059
fff(6)	-	-	0.080	-	-	0.0031

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *The total profile height (Dim A) is measured from the seating plane to the top of the component.*
3. - *The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug.*
   - *A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.*
4. *Initial ball equal 0.350 mm.*
5. *The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.*
6. *The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above The axis of each ball must lie simultaneously in both tolerance zones.*

Figure 104. **TFBGA225 - Recommended footprint**

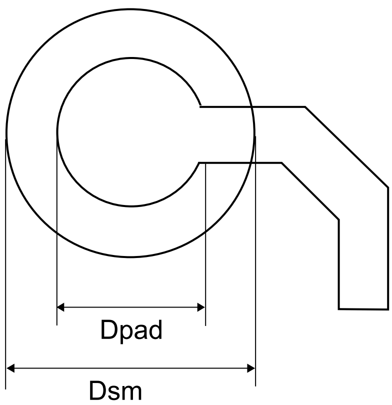


Table 139. TFBGA225 - Recommended PCB design rules (0.8 mm pitch)

Dimension	Recommended values
Pitch	0.8 mm
Dpad	0.400 mm
Dsm	0.470 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

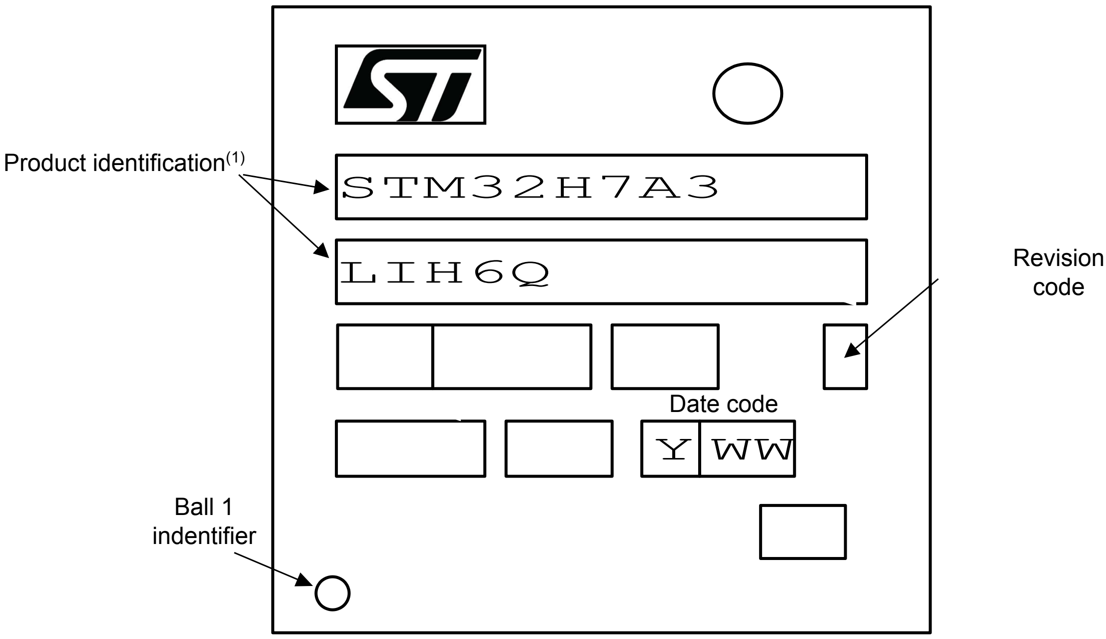
7.8.1 Device marking for TFBGA225

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 105. TFBGA225 marking example (package top view)

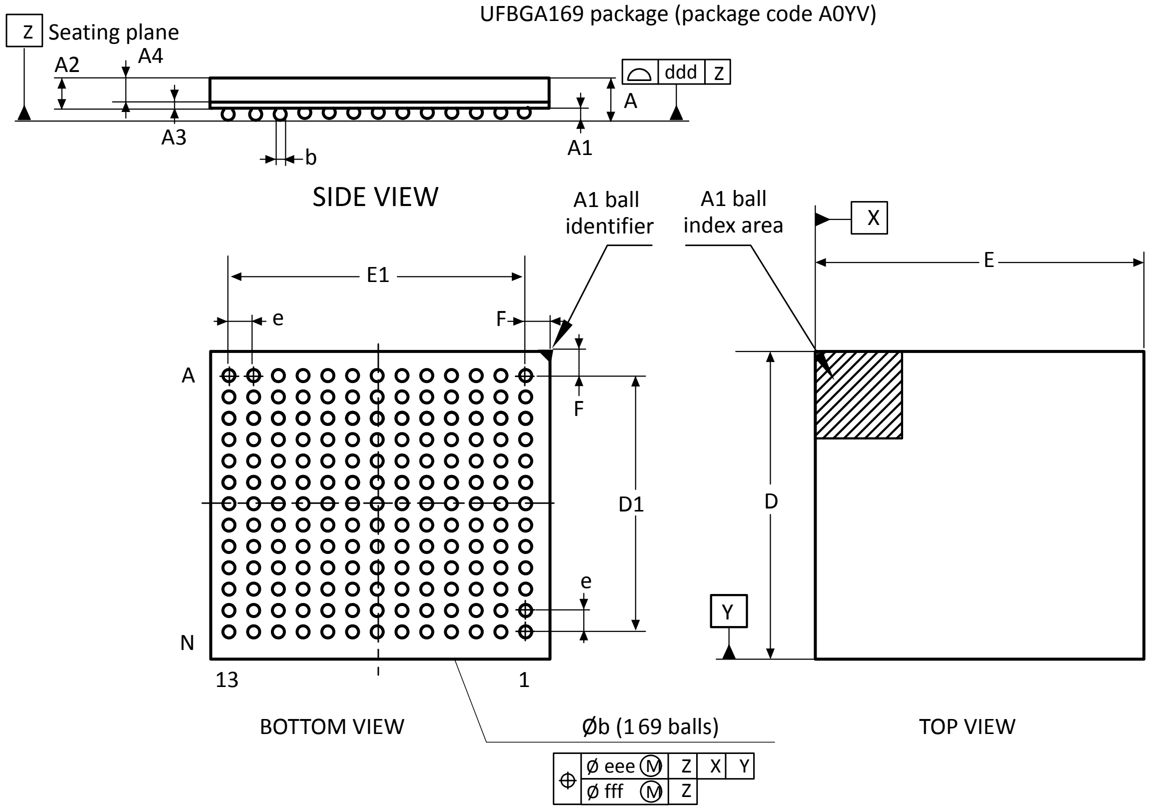


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.9 UFBGA169 package information

This UFBGA is a 169 balls, 7 x 7 mm, 0.50 mm pitch, ultra thin profile fine pitch ball grid array package

Figure 106. UFBGA169 - Outline



1. Drawing is not to scale.
2. – The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metalized markings, or other feature of package body or integral heat slug.
   – A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

Table 140. **UFBGA169 - Mechanical data**

Symbol	millimeters			inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A[2]	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.130	-	-	0.0051	-
A4	-	0.320	-	-	0.0126	-
b[3]	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	6.000	-	-	0.2362	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	6.000	-	-	0.2362	-
e	-	0.500	-	-	0.0197	-
F	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031
eee [4]	-	-	0.015	-	-	0.0059
fff[5]	-	-	0.050	-	-	0.0020

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. - *Ultra Thin profile: 0.50 < A ≤ 0.65 mm / Fine pitch: e < 1.00 mm pitch.*
   - *The total profile height (dim A) is measured from the seating plane to the top of the component*
   - *The maximum total package height is calculated by the following methodology:*
   - *A Max = A1 Typ + A2 Typ + A4 Typ +* $\sqrt{}$ *(* $A1^2+A2^2+A4^2$ *tolerance values)*
3. *The typical balls diameters before mounting is 0.20 mm.*
4. *The tolerance of position that controls the location of the pattern of balls with respect to datum A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datum A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.*
5. *The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above The axis of each ball must lie simultaneously in both tolerance zones.*

Figure 107. **UFBGA169 - Recommended footprint**

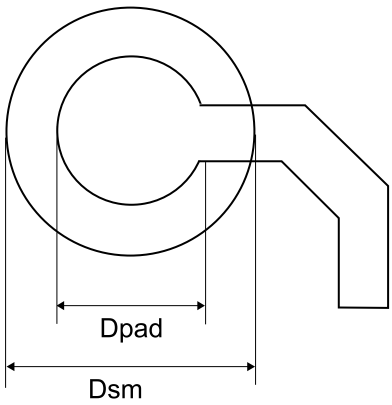


Table 141. UFBGA169 - recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5 mm
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter

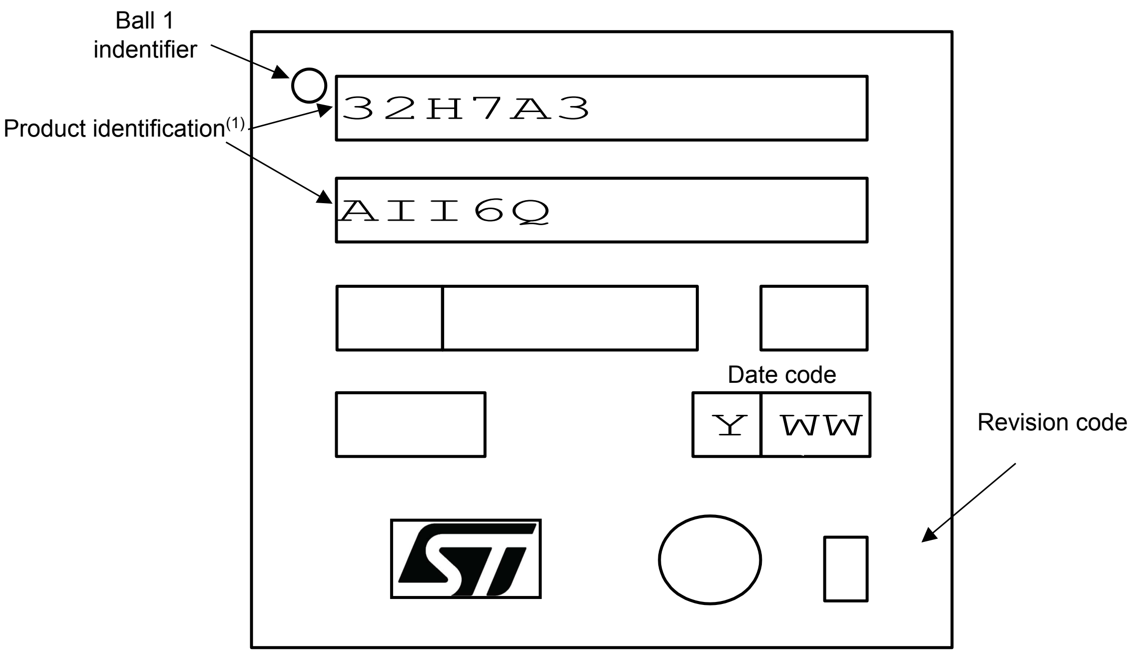
7.9.1 Device marking for UFBGA169

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 108. UFBGA169 marking example (package top view)

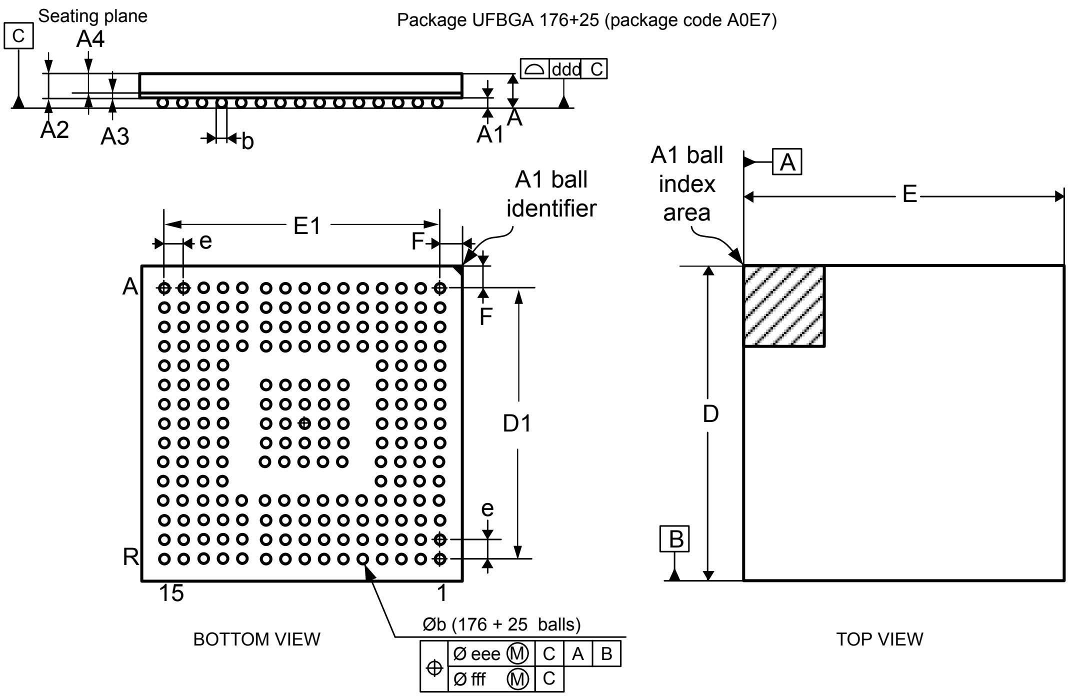


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.10 UFBGA(176+25) package information

This UFBGA is a 176+25 balls, 10 x 10 mm, 0.65 mm pitch, ultra thin profile fine pitch ball grid array package.

Figure 109. UFBGA(176+25) - Outline



1. Drawing is not to scale.
2. The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metalized markings, or other feature of package body or integral heat slug. A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

Table 142. **UFBGA(176+25) - Mechanical data**

Symbol	millimeters			inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A[2]	-	-	0.60	-	-	0.0236
A1	0.05	0.08	0.11	0.0020	0.0031	0.0043
A2	-	0.45	-	-	0.0177	-
A3	-	0.13	-	-	0.0051	-
A4	-	0.32	-	-	0.0126	-
b	0.24	0.29	0.34	0.0094	0.0114	0.0134
D	9.85	10.00	10.15	0.3878	0.03937	0.3996
D1	-	9.10	-	-	0.3583	-
E	9.85	10.00	10.15	0.3878	0.03937	0.3996
E1	-	9.10	-	-	0.3583	-
e	-	0.65	-	-	0.0256	-
F	-	0.45	-	-	0.0177	-
ddd	-	-	0.08	-	-	0.0031
eee [3]	-	-	0.15	-	-	0.0059
fff[4]	-	-	0.05	-	-	0.0020

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Ultra thin profile: 0.50 < A Max \u0001 0.65 mm / Fine pitch: e < 1.00 mm. The total profile height (Dim.A) is measured from the seating plane "C" to the top of the component.*
3. *The tolerance of position that controls the location of the pattern of balls with respect to datum A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datum A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.*
4. *The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above The axis of each ball must lie simultaneously in both tolerance zones.*

Figure 110. **UFBGA(176+25) - Recommended footprint**

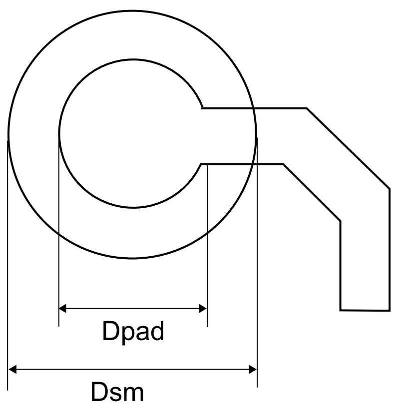


Table 143. **UFBGA(176+25) - Recommended PCB design rules (0.65 mm pitch BGA)**

Dimension	Recommended values
Pitch	0.65 mm
Dpad	0.300 mm
Dsm	0.400 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.300 mm aperture diameter
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

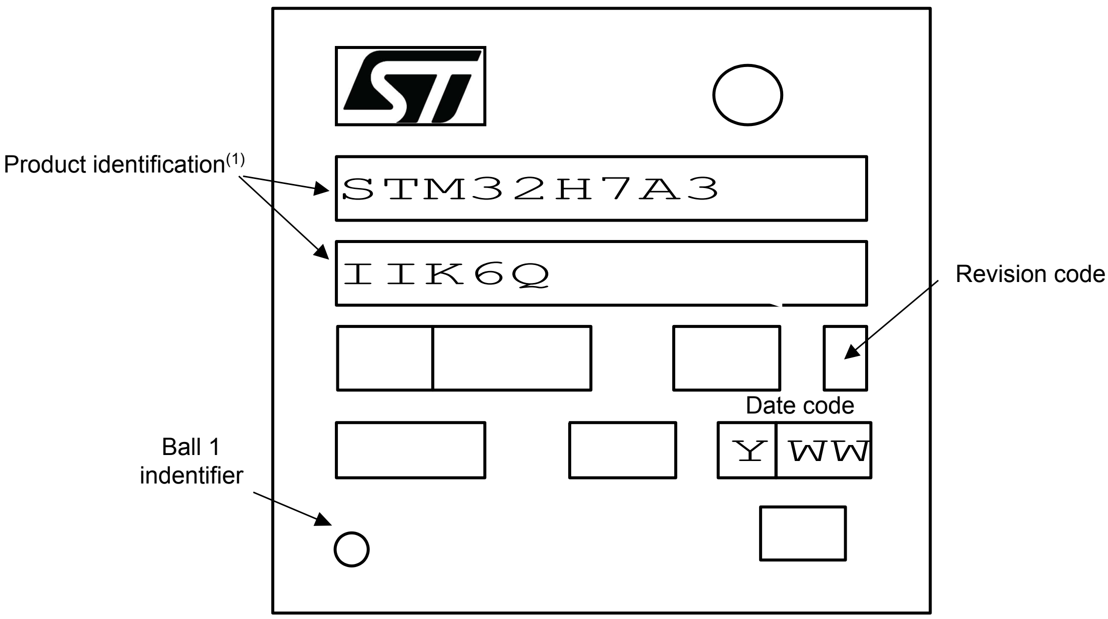
7.10.1 Device marking for UFBGA176+25

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 111. **UFBGA176+25 marking example (package top view)**



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.11 Thermal characteristics

The maximum chip-junction temperature, TJ max, in degrees Celsius, may be calculated using the following equation:

$T_J max = T_A max + (P_D max \times \Theta_{JA})$

Where:

- $T_A$max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D$max is the sum of P_{INT}max and $P_{I/O}$max ($P_D$max = P_{INT}max + $P_{I/O}$max),
- P_{INT}max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$max represents the maximum power dissipation on output pins where:

$P_{I/O}\text{max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH})$,

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 144. Thermal characteristics

Symbol	Definition	Parameter	value	unit
Θ_{JA}	Thermal resistance junction-ambiant	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm /0.5 mm pitch	48.8	°C/W
		Thermal resistance junction-ambient LQFP100 - 14 x 14 mm /0.5 mm pitch	47.4	
		Thermal resistance junction-ambient LQFP144 - 20 x 20 mm /0.5 mm pitch	46	
		Thermal resistance junction-ambient LQFP176 - 24 x 24 mm /0.5 mm pitch	43.6	
		Thermal resistance junction-ambient TFBGA100 - 8 x 8 mm /0.8 mm pitch	41.3	
		Thermal resistance junction-ambient TFBGA216 13 x 13 mm /0.8 mm pitch	39.4	
		Thermal resistance junction-ambient TFBGA225 13 x 13 mm /0.8 mm pitch	38.7	
		Thermal resistance junction-ambient UFBGA169 - 7 x 7 mm /0.5 mm pitch	41.4	
		Thermal resistance junction-ambient UFBGA176+25 - 10 x 10 mm / 0.65 mm pitch	44.4	
		Thermal resistance junction-ambient WLCSP132 - 4.57 x 4.37 mm / 0.35 mm pitch	34.6	
Θ_{JB}	Thermal resistance junction-board	Thermal resistance junction-board LQFP64 - 10 x 10 mm /0.5 mm pitch	37.2	°C/W
		Thermal resistance junction-board LQFP100 - 14 x 14 mm /0.5 mm pitch	39.2	
		Thermal resistance junction-board LQFP144 - 20 x 20 mm /0.5 mm pitch	41.3	
		Thermal resistance junction-board LQFP176 - 24 x 24 mm /0.5 mm pitch	40.2	
		Thermal resistance junction-board TFBGA100 - 8 x 8 mm /0.8 mm pitch	19	
		Thermal resistance junction-board UFBGA169 - 7 x 7 mm /0.5 mm pitch	15.3	
		Thermal resistance junction-board UFBGA176+25 - 10 x 10 mm /0.65 mm pitch	25	
		Thermal resistance junction-board TFBGA216 13 x 13 mm /0.8 mm pitch	21.9	
		Thermal resistance junction-board TFBGA225 13 x 13 mm /0.8 mm pitch	20.3	
		Thermal resistance junction-board WLCSP132 - 4.57 x 4.37 mm /0.35 mm pitch	NA	
Θ_{JC}	Thermal resistance junction-case	Thermal resistance junction-case LQFP64 - 10 x 10 mm /0.5 mm pitch	13	°C/W
		Thermal resistance junction-case LQFP100 - 14 x 14 mm /0.5 mm pitch	12.8	

Symbol	Definition	Parameter	value	unit
Θ_{JC}	Thermal resistance junction-case	Thermal resistance junction-case LQFP144 - 20 x 20 mm /0.5 mm pitch	12.6	°C/W
		Thermal resistance junction-case LQFP176 - 24 x 24 mm /0.5 mm pitch	11.5	
		Thermal resistance junction-case TFBGA100 - 8 x 8 mm /0.8 mm pitch	22.2	
		Thermal resistance junction-case UFBGA169 - 7 x 7 mm /0.5 mm pitch	19.9	
		Thermal resistance junction-case UFBGA176+25 - 10 x 10 mm /0.65 mm pitch	18.9	
		Thermal resistance junction-case TFBGA216 13 x 13 mm /0.8 mm pitch	22.2	
		Thermal resistance junction-case TFBGA225 13 x 13 mm /0.8 mm pitch	22.2	
		Thermal resistance junction-case WLCSP132 - 4.57 x 4.37 mm /0.35 mm pitch	NA	

7.11.1 Reference documents

- JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.
- For information on thermal management, refer to application note “Thermal management guidelines for STM32 32-bit Arm Cortex MCUs applications” (AN5036) available from *www.st.com*.

8 Ordering information

Example:	STM32	H	7A3	Z	I	T	6	Q	TR

Device family

STM32 = Arm-based 32-bit microcontroller

Product type

H = High performance

Device subfamily

7A3 = STM32H7A3 without cryptographic accelerator

Pin count

R = 64 pins

V = 100 pins/balls

Q = 132 balls

Z = 144 pins

A = 169 balls

I = 176 or 176 + 25 pins/balls

N = 216 balls

L = 225 balls

Flash memory size

I = 2 Mbytes

G = 1 Mbyte

Package

T = LQFP ECOPACK2

K = UFBGA 0.65 mm pitch ECOPACK2

I = UFBGA 0.5 mm pitch ECOPACK2

H = TFBGA ECOPACK2

Y = WLCSP ECOPACK2

Temperature range

6 = Industrial temperature range, –40 to 85 °C

Option

Q = with SMPS

Blank = without SMPS

Packing

TR = tape and reel

No character = tray or tube

For a list of available options (such as speed and package) or for further information on any aspect of this device, contact your nearest ST sales office.

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Revision history

Table 145. **Document revision history**

Date	Revision	Changes
22-Jan-2020	1	Initial release.
24-Apr-2020	2	Updated Octo-SPI interface in Table 1. STM32H7A3xI/G features and peripheral counts. Updated Figure 2. Power-up/power-down sequence in Section 6.1.6 Power supply scheme. Updated HSLV feature description in Section 3.8 General-purpose input/outputs (GPIOs). Section 5 Pin descriptions: updated Table 6. Legend/abbreviations used in the pinout table; changed SPDIFRX into SPDIFRX1 and updated all SPDIFRX1 pin names. Updated Table 19. Voltage characteristics to add V_{REF+} in the list of external main supply voltage. Removed clock frequencies from Table 22. General operating conditions and added new Section 6.3.1 . Changed condition for $t_{RSTTEMPO}$ in Table 29. Reset and power control block characteristics. Added $I_{DD50USB}$ in Table 32. USB regulator characteristics. Updated Table 40. Typical current consumption in System Stop mode, added Table 41. Typical current consumption RAM shutoff in Stop mode, added IWDG and changed SPDIFRX into SPDIFRX1 in Table 44. Peripheral current consumption in Run mode. Table 58. Flash memory programming: updated table title, updated t_{ME} description and unit. In the whole Section 6.3.18 FMC characteristics, replaced sentence "the T_{KERCK} is the fmc_ker_ck clock period" by "the $T_{fmc\_ker\_ck}$ is the kernel clock period". Section 6.3.19 Octo-SPI interface characteristics: added parameter measurement conditions, updated Table 90. OCTOSPI characteristics in SDR mode and Table 91. OCTOSPI characteristics in DTR mode (with DQS)/Octal and Hyperbus, updated Figure 51. OctoSPI Hyperbus clock, Figure 52. OctoSPI Hyperbus read and Figure 53. OctoSPI Hyperbus write. Updated Figure 57. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA}), note 1. and note 1.. Section 6.3.30 Digital filter for Sigma-Delta Modulators (DFSDM) characteristics, Section 6.3.31 Camera interface (DCMI) timing specificationsSection 6.3.33 LCD-TFT controller (LTDC) characteristics, Section 6.3.36.2 USART interface characteristics, Section 6.3.36.3 SPI interface characteristics, Section 6.3.36.4 I2S Interface characteristics, Section 6.3.36.5 SAI characteristics, Section 6.3.36.7 SD/SDIO MMC card host interface (SDMMC) characteristics, Section 6.3.36.8 USB OTG_FS characteristics, Section 6.3.36.9 USB OTG_HS characteristics, Section 6.3.36.10 JTAG/SWD interface characteristics: changed VOS level to VOS0 in the parameter measurement conditions.
08-Jul-2020	3	Updated note related to ULPI interface availability on packages that do not feature PC2 and PC3 I/Os in Table 1. STM32H7A3xI/G features and peripheral counts. Updated Table 20. Current characteristics, Table 21. Thermal characteristics and Figure 22. Current consumption measurement scheme.

Date	Revision	Changes
		Updated Figure 21. Power supply scheme. Added note to V_{REFINT} in Table 30. Embedded reference voltage.Added Table 33. Inrush current and inrush electric charge characteristics for LDO and SMPS. Updated Table 46. Low-power mode wakeup timings, Table 34. Typical and maximum current consumption in Run mode, code with data processing running from ITCM, regulator ON and Table 35. Typical and maximum current consumption in Run mode, code with data processing running from flash memory, cache ON. Updated Table 68. Output timing characteristics (HSLV OFF) and Table 69. Output timing characteristics (HSLV ON). Updated Table 62. ESD absolute maximum ratings and . Added notes related to performance degradation at VOS1 in Section 6.3.18 FMC characteristics, Section 6.3.19 Octo-SPI interface characteristics, Section 6.3.32 PSSI interface characteristics, Section 6.3.33 LCD-TFT controller (LTDC) characteristics, Section 6.3.36.2 USART interface characteristics, Section 6.3.36.3 SPI interface characteristics, Section 6.3.36.4 I2S Interface characteristics, Section 6.3.36.5 SAI characteristics, Section 6.3.36.6 MDIO characteristics, Section 6.3.36.7 SD/SDIO MMC card host interface (SDMMC) characteristics, Section 6.3.36.9 USB OTG_HS characteristics and Section 6.3.36.10 JTAG/SWD interface characteristics. Updated $F_{(CLK)}$ measurement conditions in Table 90. OCTOSPI characteristics in SDR mode and Table 91. OCTOSPI characteristics in DTR mode (with DQS)/Octal and Hyperbus. Added Figure 54. ADC conversion timing diagram. Added Section 6.3.32 PSSI interface characteristics. Updated Figure 66. USART timing diagram in Master mode and Figure 67. USART timing diagram in Slave mode. Added note related to ULPI transceivers operating at 1.8 V in Table 125. Dynamics characteristics: USB ULPI.
21-Aug-2020	4	In Section 3.31 True random number generator (RNG), changed "random number generator" in "true random number generator" and description updated. In Section 5 Pin descriptions, swapped PA1 and PA2 balls in *WLCSP132 ballout* schematic. Added reference to application note AN4899 in Section 6.3.16 I/O port characteristics. Updated DuCyCKOUT in Table 108. DFSDM measured timing 1.62-3.6 V Updated .
16-Sep-2020	5	Updated VDDMMC separate supply pad in Section 2 Description. Changed pin 88 connection to VDD in Figure *LQFP100 (STM32H7B3xI with SMPS) pinout* and Table 7. STM32H7A3xI/G pin/ball definition. Changed VDD_MMC_4 into VDDMMC in Table 7. STM32H7A3xI/G pin/ball definition. Updated Figure 21. Power supply scheme and Section 6.3.2 VCAP external capacitor. Added V_{BAT} in Section 6.3.1 General operating conditions. Updated High-speed external user clock generated from an external source and Low-speed external user clock generated from an external source. Updated .
28-Sep-2020	6	Updated V_{HSEL} maximum value in Table 47. High-speed external user clock characteristics.
04-May-2021	7	Added indication that patents apply to the devices in Section Features. Added reference to errata sheet in Section 1 Introduction. Updated WKUP signals in Figure 1. STM32H7A3xI/G block diagram and in Table 7. STM32H7A3xI/G pin/ball definition. Updated Section 3.38 Serial peripheral interfaces (SPI)/integrated interchip sound interfaces (I2S). Added note to TRIM parameter in Table 52. HSI oscillator characteristics.

Date	Revision	Changes
		Extended Figure 55. ADC accuracy characteristics to both ADC resolutions and updated Figure 56. Typical connection diagram using the ADC with FT/TT pins featuring analog switch function. Replace 110 °C by 130 °C in Table 100. Analog temperature sensor calibration values. Updated $t_{su(ADV\text{-}CLKH)}$, $t_{h(CLKH\text{-}ADV)}$, $t_{su(NWAIT\text{-}CLKH)}$ and $t_{h(CLKH\text{-}NWAIT)}$ minimum values in Table 9. Updated $t_{su(DV\text{-}CLKH)}$, $t_{h(CLKH\text{-}DV)}$, $t_{(NWAIT\text{-}CLKH)}$ and $t_{h(CLKH\text{-}NWAIT)}$ minimum values in Table 82. Synchronous non-multiplexed NOR/PSRAM read timings. Updated $t_{su(SDCLKH\ \_Data)}$ and $t_{h(SDCLKH\ \_Data)}$ minimum values in Table 86. SDRAM read timings. Updated $t_{su(SDCLKH\_Data)}$ and $t_{h(SDCLKH\_Data)}$ minimum values in Table 87. LPSDR SDRAM read timings. Section 6.3.19 Octo-SPI interface characteristics: • Updated $t_{S(IN)}/t_{H(IN)}$ conditions and minimum values in Table 90. OCTOSPI characteristics in SDR mode and updated Figure 49. OctoSPI timing diagram - SDR mode. • Updated Table 91. OCTOSPI characteristics in DTR mode (with DQS)/ Octal and Hyperbus and Figure 50. OctoSPI timing diagram - DTR mode. • Updated Figure 51. OctoSPI Hyperbus clock, Figure 52. OctoSPI Hyperbus read and Figure 53. OctoSPI Hyperbus write. Table 118. SPI dynamic characteristics: • Changed $t_{su(MI)}$ and $t_{h(MI)}$ minimum values in Master mode. • Removed $t_{w(SCKH)}$, $t_{w(SCKL)}$. Table 122. Dynamics characteristics: SDMMC characteristics, V_{DD}=2.7 to 3.6 V: • Modified t_{ISU} and t_{IH} minimum values for CMD/ D inputs in High-speed mode. • Modified t_{ISUD} and t_{IH} minimum values for CMD/ D inputs in Default mode. Table 123. Dynamics characteristics: eMMC characteristics VDD=1.71V to 1.9V: • Removed SDIO_CK/f_{PCLK2} frequency ratio. • Modified t_{ISU} and t_{IH} minimum values in CMD, D inputs (referenced to CK) in eMMC mode. Section 7.7 TFBGA216 package information: • Added note 2 below Figure 100. TFBGA216 - Outline. • Changed A maximum value from 1.100 to 1.200 and added note 2,3 4 and 5 in table 1.Table 136. TFBGA216 - Mechanical data. • Updated Figure 101. TFBGA216 - Recommended footprint and Table 137. TFBGA216 - Recommended PCB design rules (0.8 mm pitch) . Section 7.9 UFBGA169 package information: • Added note 2 below Figure 106. UFBGA169 - Outline. • Updated Table 140. UFBGA169 - Mechanical data. • Removed note related to non-solder mask below Figure 107. UFBGA169 - Recommended footprint. Section 7.10 UFBGA(176+25) package information: • Added note 2 below . • Updated .
19-May-2022	8	Renamed SPIx_NSS signal into SPIx_SS. Updated Table 20. Current characteristics. Removed $f_{TraceCK}$ / f_{JTCK} from Table 23. Maximum allowed clock frequencies. Updated note 3 in Table 40. Typical current consumption in System Stop mode. Updated Table 61. EMI characteristics for f_{HSE} = 8 MHz and f_{HCLK} = 64 MHz. Updated Table 66. Output voltage characteristics for all I/Os except PC13, PC14, PC15 and PI8 and Table 67. Output voltage characteristics for PC13, PC14, PC15 and PI8. Added Table 70. Pxy_C and Pxy analog switch characteristics

Date	Revision	Changes
		Added note to $t_{d(SDCLKL-\ SDNE)}$ maximum value in Table 86. SDRAM read timings, Table 87. LPSDR SDRAM read timings, Table 88. SDRAM write timings and Table 89. LPSDR SDRAM write timings. Updated Figure 56. Typical connection diagram using the ADC with FT/TT pins featuring analog switch function and notes below figures. Added note to t_{SAMP} in Table 96. DAC characteristics. Updated Table 108. DFSDM measured timing 1.62-3.6 V. In Table 117. USART characteristics, replaced $t_{su(SI)}$ and $t_{su(MI)}$ by $t_{su(RX)}$, $t_{h(SI)}$ and $t_{h(MI)}$ by $t_{h(RX)}$, $t_{v(SO)}$ and $t_{v(MO)}$ by $t_{v(TX)}$, and $t_{h(SO)}$ and $t_{h(MO)}$ by $t_{h(TX)}$. Updated Section 7.1.1 Device marking for LQFP64, Section 7.1 LQFP64 package information, Section 7.2 LQFP100 package information, Section 7.3 TFBGA100 package information, Section 7.6.1 Device marking for LQFP176, Section 7.7.1 Device marking for TFBGA216, Section 7.8 TFBGA225 package information, Section 7.9 UFBGA169 package information and Section 7.10 UFBGA(176+25) package information. Added Section Important security notice.

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