

OMAP-L137
Low-Power Applications Processor
Silicon Revision 1.0

Silicon Errata



Literature Number: SPRZ291
October 2008

OMAP-L137 Silicon Revision 1.0

1 Introduction

This document describes the known exceptions to the functional specifications for the *OMAP-L137 Low-Power Applications Processor*. For more detailed information, see the *OMAP-L137 Low-Power Applications Processor* data manual (literature number [SPRS563](#)).

1.1 Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all OMAP processors and support tools. Each commercial OMAP platform member has one of three prefixes: X, P, or null (no prefix). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices/tools (TMDS).

Device development evolutionary flow:

X	Experimental device that is not necessarily representative of the final device's electrical specifications
P	Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification
NULL	Fully-qualified production device

Support tool development evolutionary flow:

TMDX	Development-support product that has not yet completed Texas Instruments internal qualification testing
TMDS	Fully-qualified development-support product

X and P devices and TMDX development-support tools are shipped against the following disclaimer:
"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

1.2 Revision Identification

Figure 1 shows an example of the device markings.

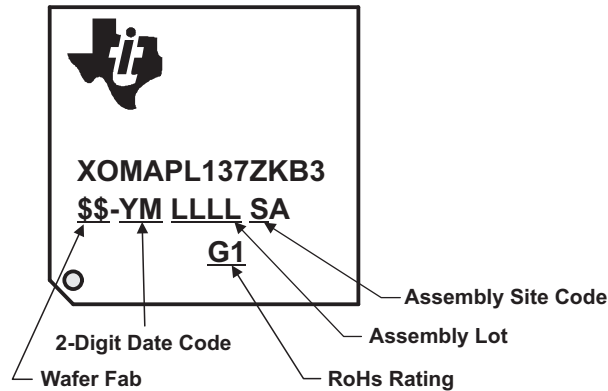


Figure 1. Example, Device Revision Codes for OMAP-L137 (ZKB Package)

NOTES:

A. Non-qualified devices are marked with the letters "X" or "P" at the beginning of the device name.

Each silicon revision uses a specific revision of the CPU and the C674x Megamodule. The CPU revision ID identifies the silicon revision of the CPU. [Table 1](#) lists the CPU and C674x Megamodule revision associated with each silicon revision. The CPU revision can be read from the REVISION_ID field of the CPU Control Status Register (CSR). The C674x Megamodule revision can be read from the REVISION field of the Megamodule Revision ID register (MM_REVID) located at address 0181 2000h.

The ROM code revision can be read from address location 0x1170 0008h. [Table 1](#) shows the ROM code revision for each revision of the device.

Table 1. Silicon Revision Variables

SILICON REVISION	CPU REVISION	C674x MEGAMODULE REVISION	ROM CODE REVISION
1.0	1.0 CPU ID + CPU REV ID (CSR.[31:16] = 1400h)	Revision 1 (MM_REVID.[15:0] = 0000h)	D800K001 (ASCII format)

2 Silicon Revision 1.0 Usage Notes and Known Design Exceptions to Functional Specifications

This section describes the usage notes and advisories that apply to silicon revision 1.0 of the *OMAP-L137* device.

2.1 Usage Notes for Silicon Revision 1.0

There are currently no known usage notes for silicon revision 1.0.

2.2 Silicon Revision 1.0 Known Design Exceptions to Functional Specifications

Table 2.3. Silicon Revision 1.0 Advisory List

Title	Page
Advisory 1.0.1 ARM Data Cache in Write-Back Mode is Not Functional: Must Use Write-Through or Non-Cached Mode	5

Advisory 1.0.1 **ARM Data Cache in Write-Back Mode is Not Functional: Must Use Write-Through or Non-Cached Mode**

Revision(s) Affected

1.0

Details

The ARM926 subsystem allows data memory regions to be write-back cacheable, write-through cacheable, or non-cached. On this device revision, the *Write-Back* mode is not functional; therefore, *Write-Through* or *Non-Cached* mode must always be used.

Workaround(s)

Only the *Write-Through* or *Non-Cached* mode can be used. *Write-Through* mode is preferred for better performance. The cache operation is controlled using the C and B bits in page or section descriptors. For operation in *Write-Through* mode, the C and B bits (bits 3:2 in the descriptor) must be set to a value of 10b.

The following is example code using a section descriptor to create a table entry for the first 1MB of external SDRAM on EMIFB as write-through cacheable:

```
LDR r1, SDRAM0_ADDR      ; table offset for SDRAM0 region
LDR r2, SDRAM0_DATA      ; descriptor pattern for SDRAM0 region
STR r2, [r0, r1, LSL#2]  ; store the table entry at TTB base + table
                           offset * 4
SDRAM0_ADDR               .word    0x00000C00
SDRAM0_DATA               .word    0xC0000CFA
```

For more information on ARM data cache modes and how to configure them, refer to the *ARM926EJ-S™ Technical Reference Manual* available at www.arm.com/documentation. Chapter 4 of the *ARM926EJ-S™ Technical Reference Manual* provides details about cache operations on the ARM926EJ-S processor.

Section descriptor: A section descriptor provides the base address of a 1MB block of memory. [Figure 2](#) shows the format of a section descriptor.

31	20	19	12	11	10	9	8	5	4	3	2	1	0
section base address		AP		SBZ		AP	Domain		1	C	B	1	0

Figure 2. Section Descriptor

[Table 2](#) shows the Section Descriptor bit assignments. [Table 3](#) shows the Page Table C and B bit settings for the DCache.

Table 2. Section Descriptor Bits

BITS	DESCRIPTION
31:20	Form the corresponding bits of the physical address for a section.
19:12	Always written as 0.
11:10	Specify the access permissions for this section.
9	Always written as 0.
8:5	Specify one of the 16 possible domains, held in the domain access control register, that contain the primary access controls.
4	Should be written as 1, for backwards compatibility.
3:2	Indicate if the area of memory mapped by this section is treated as write-back cacheable, write-through cacheable, noncached buffered, or noncached nonbuffered.
1:0	These bits must be 10 to indicate a section descriptor

Advisory 1.0.1 — *ARM Data Cache in Write-Back Mode is Not Functional: Must Use Write-Through or Non-Cached Mode*
www.ti.com

Table 3. Page Table C and B Bit Settings for the DCache

C BIT	B BIT	DESCRIPTION	ARM926EJ-S BEHAVIOR
0	0	Noncacheable, nonbufferable	DCache disabled. Read from external memory. Write as a nonbuffered store(s) to external memory. DCache is not updated.
0	1	Noncacheable, bufferable	DCache disabled. Read from external memory. Write as a buffered store(s) to external memory. DCache is not updated.
1	0	Write-through	DCache enabled: <ul style="list-style-type: none"> • Read hit - Read from DCache • Read miss - Linefill • Write hit - Write to the DCache, and buffered store to external memory • Write miss - Buffered store to external memory
1	1	Write-back	DCache enabled: <ul style="list-style-type: none"> • Read hit - Read from DCache • Read miss - Linefill • Write hit - Write to the DCache only • Write miss - Buffered store to external memory

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated