

This user guide addresses the features, setup and operation of the VersaKit development system for the evaluation and programming of Ramtron's high performance, fully-integrated, FRAM-Enhanced™, 8051-based VRS51L3xxx microcontrollers.

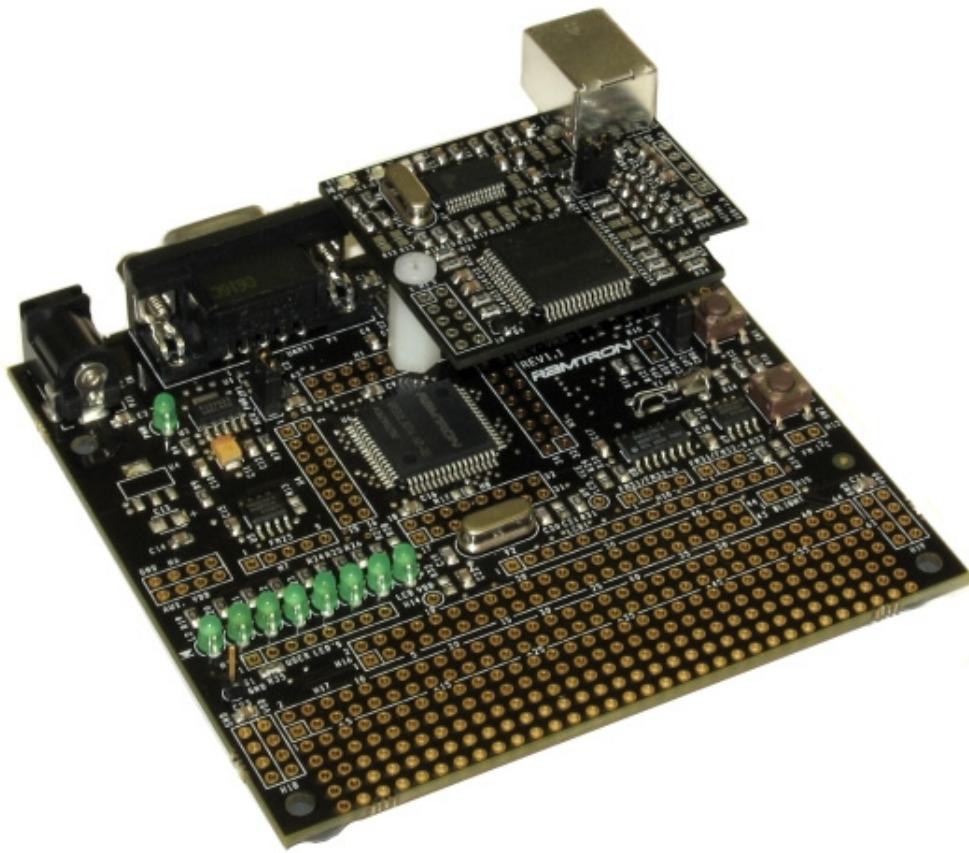


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1 VersaKit-30xx Development System Overview

The VersaKit-30xx development kit is a plug-and-play evaluation system for the VRS51L3xxx series of high performance, fully-integrated, FRAM-Enhanced™ 8051 microcontrollers. The VersaKit-30xx provides a complete and comprehensive programming and development platform, with ample prototyping space and easy access to chip peripherals and I/Os.

The VersaKit-30xx development system features:

- VRS51L3074 in QFP-64 package soldered onboard (contact Ramtron for details on the VRS51L3174 in QFP-44 package and the VRS51L2070)
- FM31xx MCU companion, FM25xx SPI FRAM and FM24xx I²C FRAM devices installed
- 5x2 header to connect VJTAG-USB programming/debugging interface
- 2 DB9 serial port female connectors and 1 onboard RS-232 transceiver with configuration jumper
- Tact switches for manual reset and external interrupt of the processor
- Four sets of 16 probing points around VRS51L3074 device
- 22x2 header alongside prototyping area to access QFP-44 device pins (header pin number corresponds to device pin number)
- 32x2 header alongside prototyping area to access QFP-64 device pins (header pin number corresponds to the device pin number)
- Prototyping space
- Character LCD interface header footprint
- External crystal footprint
- 8 uncommitted user LEDs
- Onboard 3.3V regulator with power-on LED
- Optional regulator footprint

1.1 The VersaKit-30xx content:

- Development board that supports the VRS51L3074 (or the VRS51L2070)
- VJTAG-USB programming/debugging interface
- USB Cable
- 6V Power supply

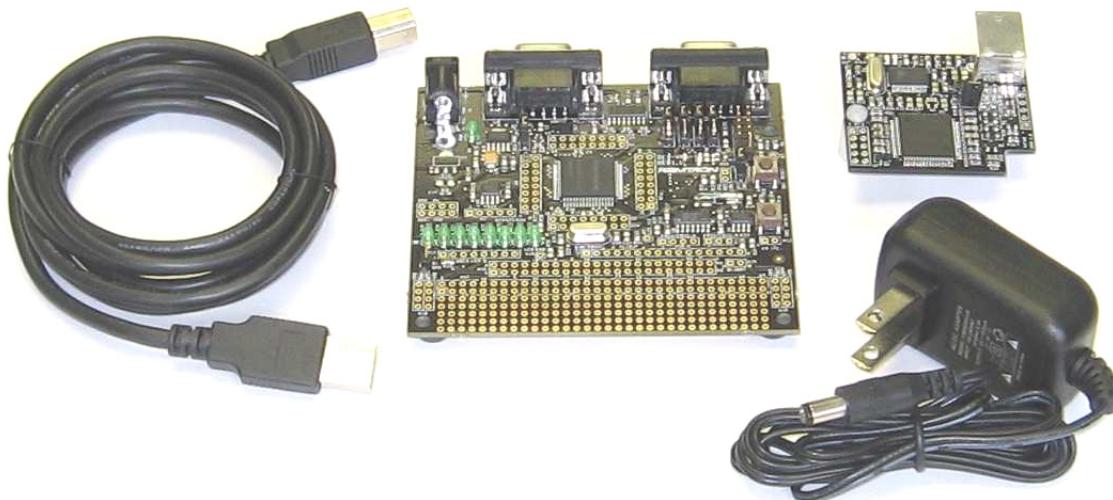


Figure 1: VersaKit-30xx

1.2 Supported Devices

The VersaKit-30xx ships with a VRS51L3074-40-Q soldered onto the development board.

VRS51L3174 Evaluation

Note that the VersaKit-30xx can also be used for evaluation of the VRS51L3174 (44-pin version of the VRS51L3074), since its peripherals are a subset of the VRS51L3074. A dedicated development board will be available for the 44-pin VRS51L3174 (part number VersaKit-31xx) in the future that is based on the VersaKit-30xx (there is a 44-pin QFP footprint under the installed VRS51L3074 on the VersaKit-30xx devboard for this purpose). Users should contact Ramtron for VersaKit-31xx availability. In the short term, code can be developed on the VRS51L3074 and easily ported to the VRS51L3174.

This user guide will address features associated with the VersaKit-31xx development board.

2 Overview of the VersaKit-30xx Development Board

The figure below offers a detailed look at the VersaKit-30xx development board and its principal features, which will be addressed in this document.

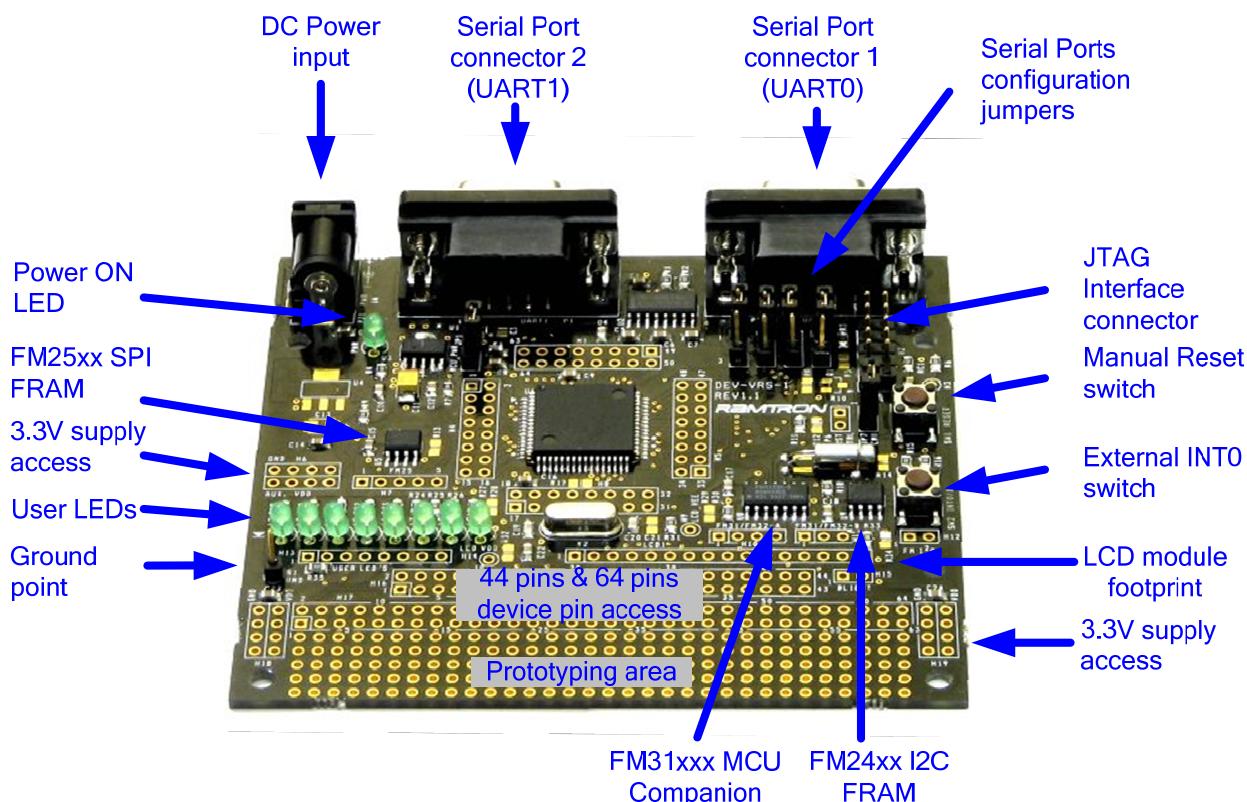


Figure 2: VersaKit-30xx development board

2.1 Power Supply Requirements

The VersaKit-30xx development board is powered via either the Versa JTAG USB (VJTAG-USB) board or an external power supply connected to PJ1. The VJTAG-USB provides up to about 110mA of power to the devboard or target board. The development board consumes from 30 to 40mA, leaving approximately 70mA for prototype development.

If your prototype's total power consumption is more than 70mA, we recommend using the external power supply shipped with the VersaKit-30xx. This should be connected to PJ1 on the devboard and can supply up to 300mA.

Note: If the external power supply is connected to PJ1, remove the JP1 jumper on the VJTAG-USB board.

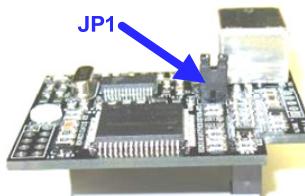


Figure 3: JP1 jumper of the VJTAG-USB board

If you need to use another power source, ensure that it respects the following parameters:

Table 1. Development board power supply specifications

Nominal input Voltage	6VDC
Maximum input voltage	11V DC
Current	200mA+
Plug Type	2.1mm Female Plug (Center positive)

Warning: Many commercially-available wall-mount DC power adapters exceed their output voltage rating when in low load condition. If you do not plan to use the power supply provided with the kit, verify that the specifications on the one you choose meets the requirements above before using it with the development board.

Ensure that the input voltage supplied to the devboard PWR-IN input is always below 11 volts.

2.2 VersaKit-30xx Devboard: Onboard Power Supply Configuration Regulators & JP1 Jumper

The VersaKit-30xx devboard includes a 3.3V low drop-out linear regulator to power the VRS51L3074 (through the JP1 jumper) and the RS-232 transceiver. This regulator provides up to 250mA of power and includes a thermal shutdown feature.

To facilitate use of the devboard as a prototyping platform, access to the 3.3V regulator output and ground access are available via two 4x2 header footprints located on each side of the prototyping area.

The development board also features an auxiliary LM2937 regulator footprint, which is powered by a DC power input and whose output is accessible on the H6 4x2 header footprint. The R9 resistor provides a path from the U4 output and H6 VDD to the Reg102-3.3 regulator output.

Heat from the regulators is dissipated through the devboard PCB. As such, the area on the PCB around the regulators may become hot when the regulators are operating.

Warning: It is mandatory to remove resistor R9 when installing a regulator in position U4.

Please refer to the development board schematics at the end of this document for more details about regulator configuration.

2.3

P1, P2 - RS-232 DB9 Connectors for Serial Ports

The development board includes a 2-channel RS-232 transceiver and two DB9 connectors to access the VRS51L3074's UARTs.

P1 – Provides access to VRS51L3074 UART 0

P2 – Provides access to VRS51L3074 UART 1

A set of four jumpers enables the P1 and P2 connectors to be assigned to the UARTs. A set of four headers (**JP2, JP3, JP4, JP5**) located directly below the P1 DB9 Connector configures the connection between the VRS51L3074, the RS-232 transceiver and DB9 connectors P1 and P2. Several configurations are possible with different header settings, but the two configurations below are the most typical:

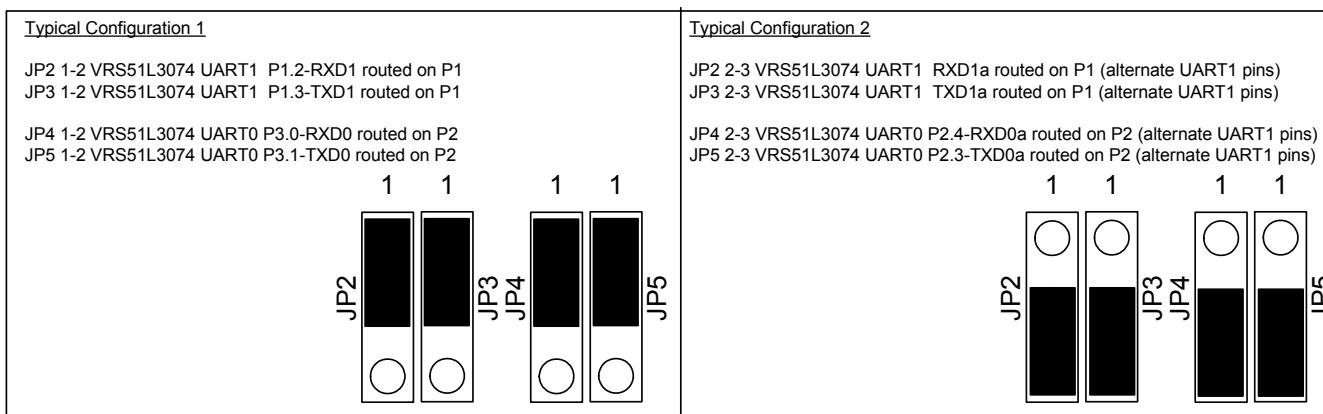


Figure 4: Typical configurations for headers and serial ports

VRS51L3074 Peripheral and I/O Access and Development Board Prototyping Area

The development board includes a set of probe points that surround the VRS51L3074. These probe points provide a direct connection to the device pins for signal probing.

64 probing points for
VRS51L3074 device

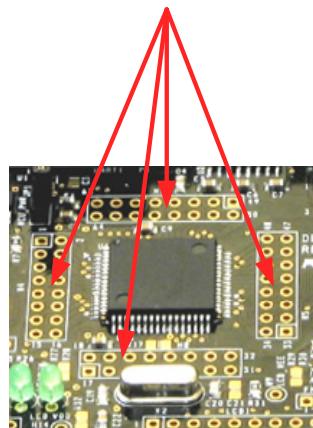


Figure 5: Probing points around the VRS51L3074-40-Q

Access to the device I/Os is also possible through two header footprints organized as follows:

The H17 header footprint provides access to the VRS51L3074 pins. Pin assignment on Header H17 directly corresponds to the VRS51L3074 pin-out.

If the VRS51L3174 is installed on the PCB, Header H16 provides a direct connection to the 44-pin device and the H16 Header pin assignment directly corresponds to the device pin-out.

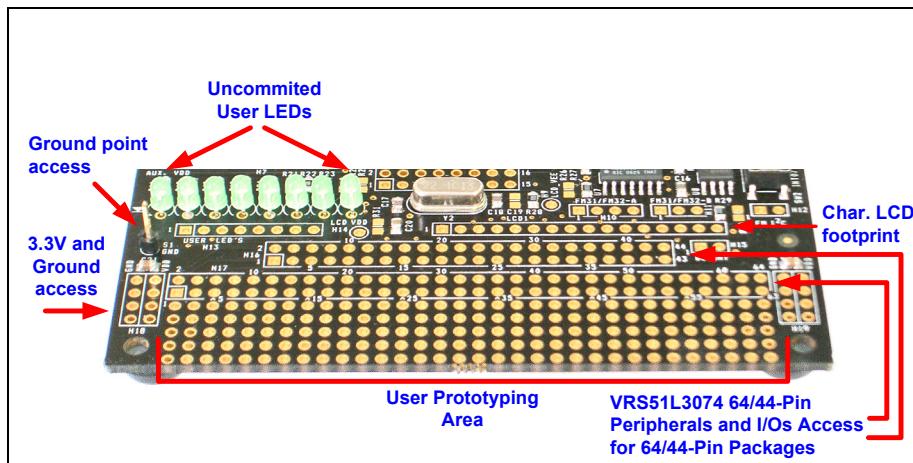


Figure 6: Prototyping area and access to VRS51L3074 I/O and peripherals pins

2.4.1 Probe headers for peripheral and I/O access around the VRS51L3074 QFP-64

The following figure shows the pin connections of the header footprints located around VRS51L3074-40-Q on the development board:

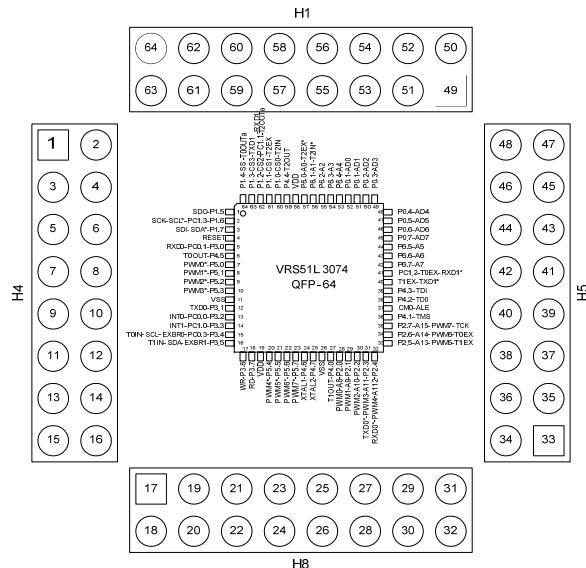


Figure 7: Probing vias around the VRS51L3074

2.4.2 Header footprints for VRS51L3074 QFP-64 peripherals and I/O access

To access the VRS51L3074 I/Os and peripherals, the devboard provides a 64-pin header footprint near the prototyping area. This header footprint provides access to all pins on the chip. The diagram below shows the header footprint pin-out.

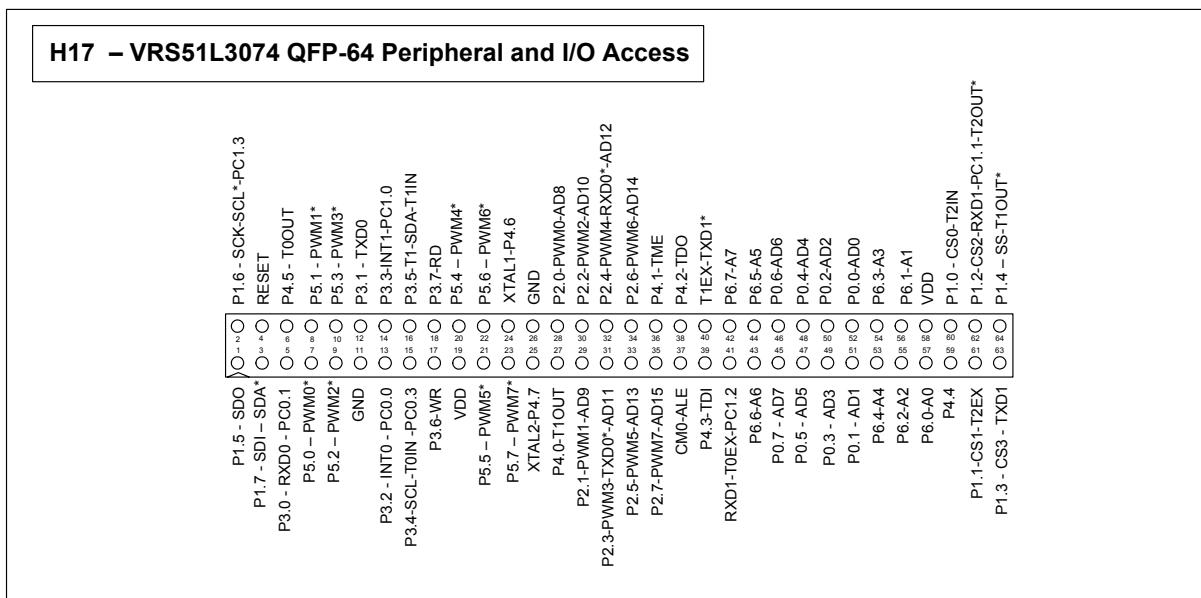


Figure 8: Pin description of H17 I/O and peripheral access

2.4.3 Probe headers for peripherals and I/O access around the VRS51L3174 QFP-44

The following figure shows the pin connections of the header footprints located around VRS51L3174 QFP-44 on the development board:

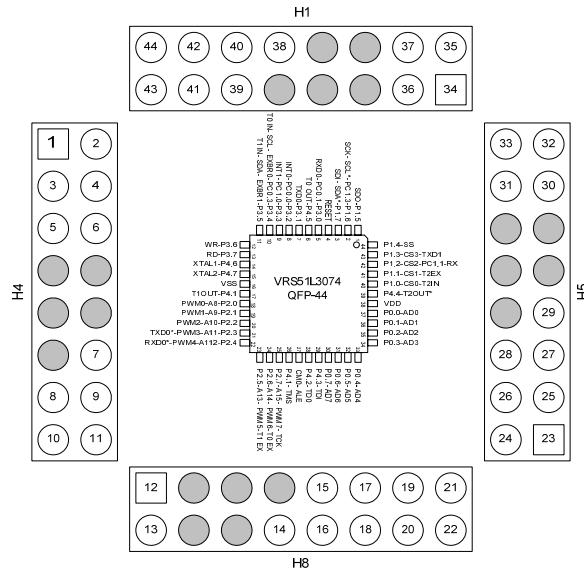
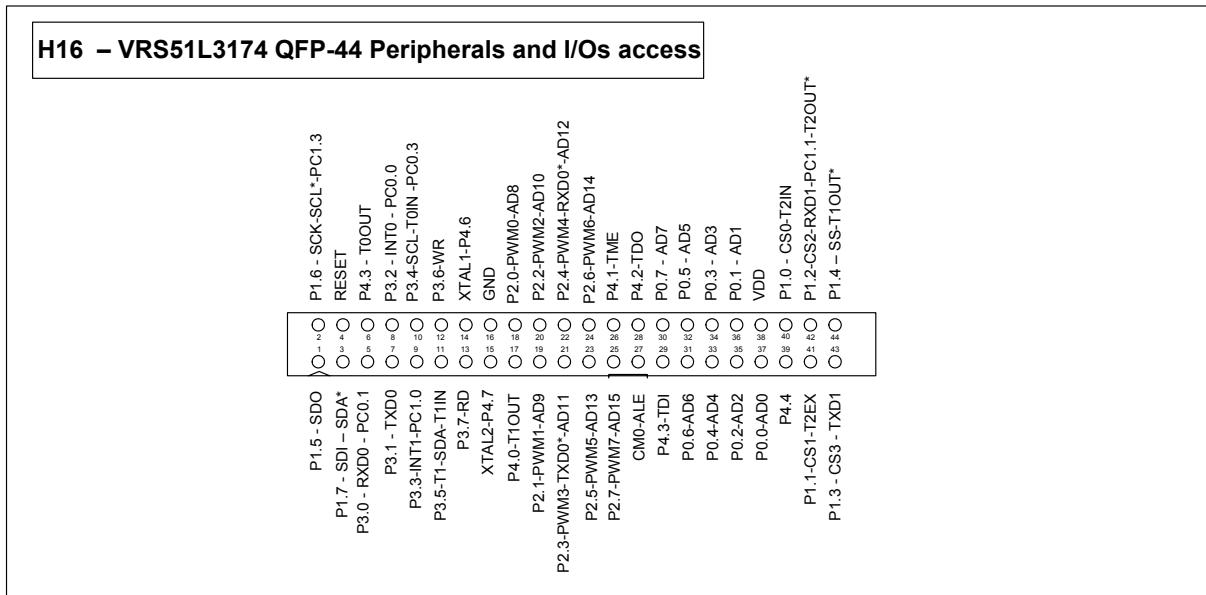


Figure 9: Probing vias around the VRS51L3174

2.4.4 Header footprints for VRS51L3174 QFP-44 peripheral and I/O access

To access the VRS51L3174 QFP-44 I/Os and peripherals, the development board provides a 44-pin header footprint near the prototyping area. This header footprint provides access to all the pins on the chip. The diagram below describes the header footprint pin-outs.



Ground Points on the Development Board

The VersaKit-30xx development board provides a ground access point (S1) located above the H18 Header on the right side of the PCB. This point can be used to connect measurement instruments to ground.

2.5 Tact Switches

The development board includes two tact switches:

- **SW1** – VRS51L3074 Reset Switch. This switch allows a manual reset of the VRS51L3074 device. The VRS51L3074 reset is active low.
Note: During programming or in-circuit debugging of the VRS51L3074, do not press SW1. Doing so could result in loss of synchronization between the Versa Ware JTAG software and VRS51L3074 debugger.
- **SW2** – VRS51L3074 Interrupt Switch. This switch allows users to manually send a low pulse to the device's INT0 pin. A connection can be established from the SW2 to the VRS51L3074 INT1 pin by installing a 0Ω resistor at position R28 and removing the 0Ω resistor from R27.

2.6 User LEDs

The development board includes a set of eight uncommitted, 3mm, green user LEDs. The anode of each LED is connected to the board's VCCMCU supply line through a 680R current limiting resistor, while the cathode of each LED is connected to the user LED's H13 header footprint.

2.7 Character LCD Module Header Footprint

The development board features a header footprint (LCD1) for easy installation of a character LCD module. When installed, the character LCD module header footprint and the VRS51L3074 are configured as follows:

Table 2: Character LCD header footprint pin-out

LCD	Connected to
LCD Data [7:4]	P0 [7:4]
LCD Data [3:0]	Not connected
LCD E	P0.2
LCD RW	P0.1
LCD RS	P0.0
LCD VEE	Accessible through H9

Most character LCD modules require a 5V supply. The LCD supply is accessed through H14. If the LCD module operates from 3.3V, a 0Ω resistor can be installed at position R31 to connect the LCD module supply and the devboard supply.

The LCD drive pin (VEE) is accessible through H9. The LCD driving voltage that must be applied on the VEE pin of the LCD module depends on the LCD type and varies among different manufacturers. Please consult the datasheet of your specific LCD module to establish the proper voltage. For your convenience, we have included an unpopulated 0805 resistor footprint between the H9 and the LCD VEE pin, as well as a 0805 capacitor footprint between the LCD VEE pin and the development board ground.

The LCD module backlight pins are accessible via the H15 2x1 header footprint

2.8 Onboard FM24C64 I²C FRAM, FM25CL64 SPI FRAM and FM31256 MCU Companion

A 5V, 64Kb I²C FRAM device (FM24CL64) is included with the development board at position U8. The SCL and SDA lines of FM24C64 are connected to the H12 2x1 header footprint.

The development board also features a FM31256 Processor Companion including FRAM at position U8, featuring 256Kb of FRAM memory, a real-time clock (RTC), a watchdog timer, an event counter and power fail monitoring circuitry. A 32 kHz crystal required for driving the FM31256's RTC is also included on the PCB.

Two 2K Ω pull-up resistors (R15 and R16) are connected between the 3.3V supply and the SDA and SCL lines, respectively. Two header footprints are provided for accessing the FM3164 I/Os. The FM3164's I²C communications interface is connected to H12.

Finally, an FM25CL64, a 3V 64Kb SPI FRAM, is also installed on the development board at position U5. The device communication interface I/Os are accessible through the H7 header footprint.

3 Overview of the VJTAG-USB interface

The VJTAG-USB board is a USB-based JTAG interface for in-circuit programming and debugging of Ramtron's VRS51L3074 and other JTAG-based microcontrollers. The VJTAG-USB connects directly to the VersaKit-30xx devboard and can be used on any prototype/production board featuring a Ramtron JTAG based MCU. The following figure depicts the VJTAG-USB interface and its principal features.

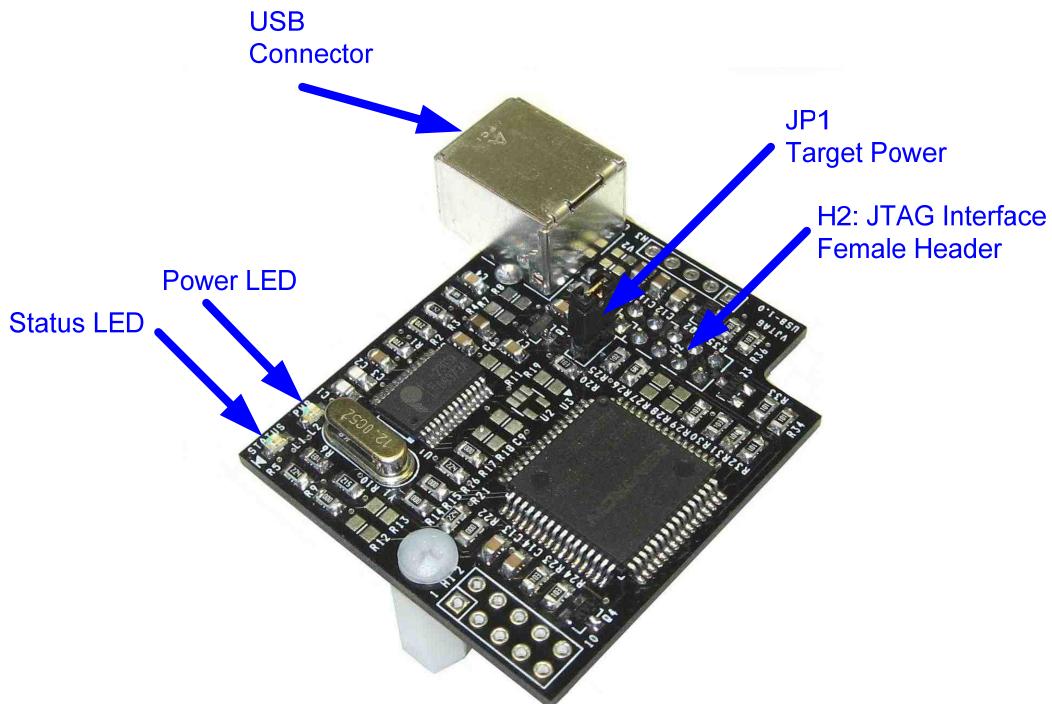


Figure 11: VJTAG-USB Interface

3.1 VJTAG-USB Power Supply Considerations and JP1 Header

The VJTAG-USB interface takes power via the USB serial bus; It can be used to provide a 3.3V supply to either the devboard or the connected target board, provided that the power current consumption does not exceed $\sim 100\text{mA}$ in total.

The JP1 Jumper provides a connection between the VJTAG-USB 3.3V power supply and the target board 3.3V power. If the target board gets its power supply from an external source, such as a DC adaptor, we recommended removing the JP1 Jumper.

3.2 Power and Status LEDs

The VJTAG-USB features two green surface mount LEDs indicating the state of the board.

The power LED is connected to the 3.3V supply of the VJTAG-USB. Depending on the state of the USB driver, when the USB cable is connected to the VJTAG-USB, the power LED may either turn ON or stay OFF. However, when the Versa Ware JTAG software is activated and the target device is recognized, the power LED will turn on and remain on.

If the USB cable is disconnected from the VJTAG-USB board while the Versa Ware JTAG is idling, when you reconnect the board, the power LED will remain off until the <Syncronize> button is clicked.

The status LED reports on communication between the Versa Ware JTAG software and the VJTAG-USB board.

Table 3: VJTAB-USB LED Functions

Status LED	Programmer Mode	Debug Mode
Off	Versa Ware JTAG Software is idling: The program in the target may or may not run.	Status LED should be ON or blinking
Sporadic blinking	Indicates that the Versa Ware JTAG Software and the VJTAG-USB board are communicating	Some operations such as <Restart>, will make both power and status LEDs blink
Blink	X	The target processor device is executing code
On	X	The target processor has halted

3.3 H2 JTAG Interface Connector

The VJTAG-USB features a 5x2 female socket (H2), located on the bottom side of the PCB. H2 is used to access the JTAG interface port of the VRS51L3074, which is installed on the devboard or target board.

On the devboard, the JTAG interface is accessed using a 5x2 male header. The header pin-out is shown below:

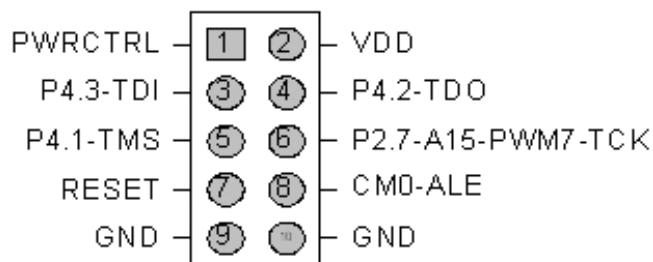


Figure 12: VJTAG-USB interface connector pin-out

The PWRCTRL line on the target board's JTAG header is optional. However, if the target board supply is from an external source and the onboard regulator does not have a power control feature, uncheck "Automatic power control" in the Versa Ware JTAG Software Device Options window.

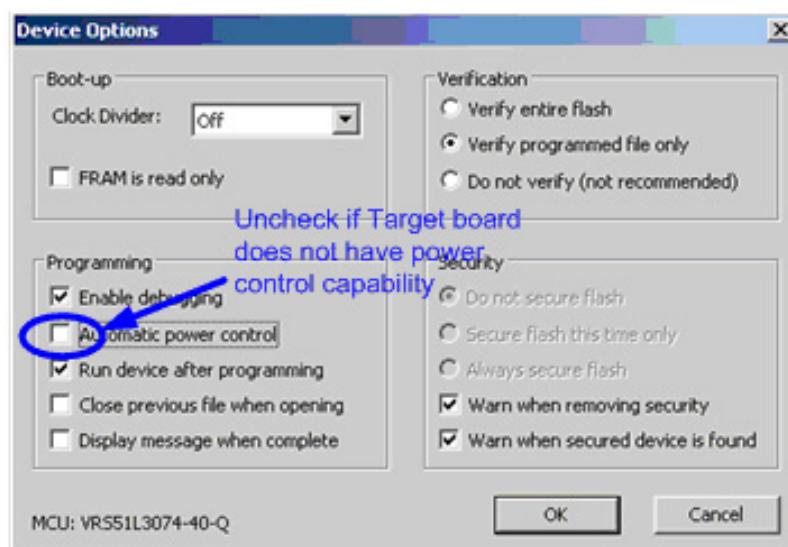


Figure 13: Versa Ware Automatic power control setting

4 Minimal Configuration of the Target Board

The following diagram demonstrates the target board configuration required for in-circuit programming and in-circuit debugging of the VRS51L2070/3074 using the JTAG-USB interface.

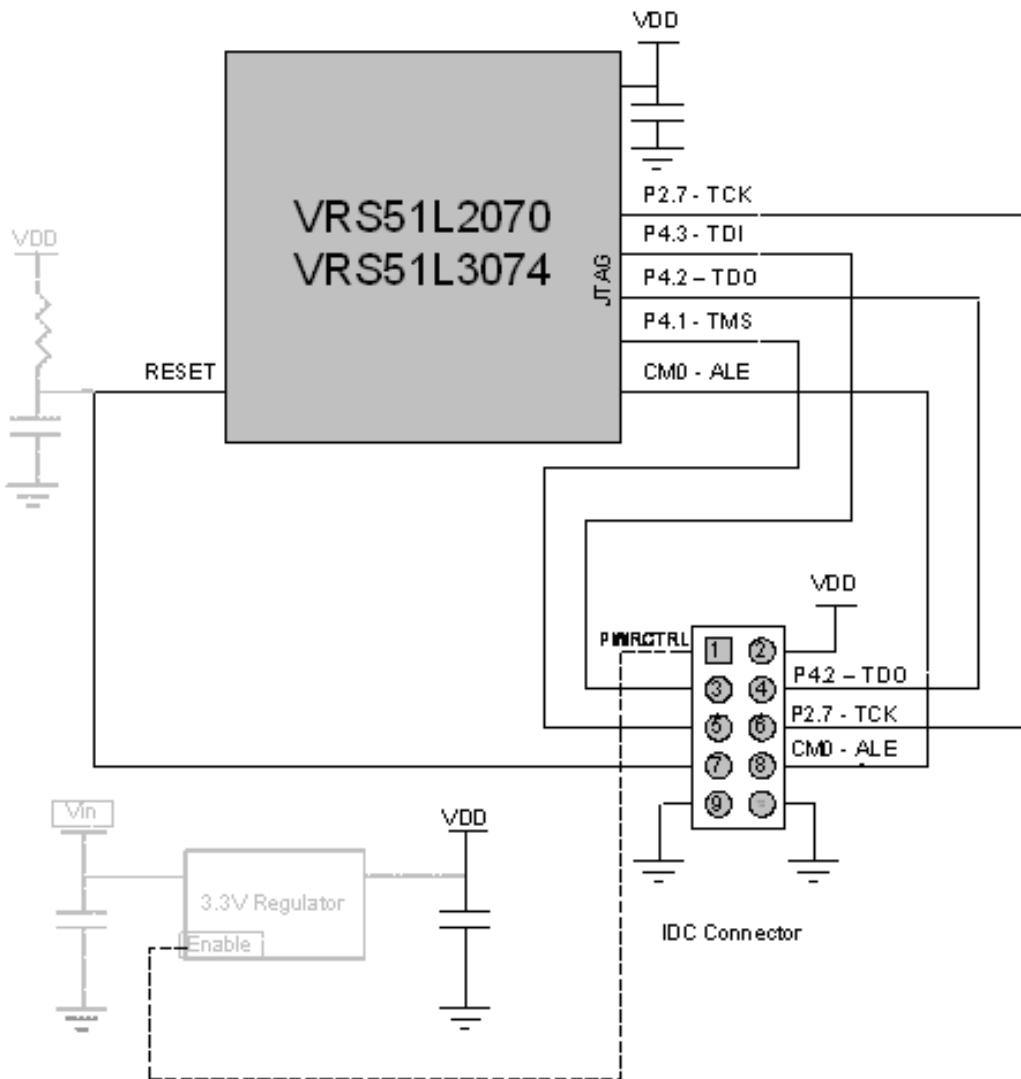


Figure 14: JTAG interface access on target board

5 Development Kit Setup for VRS51L3074 Evaluation

5.1 VersaKit-30xx Hardware Setup

The VRS51L3074 includes a Versa-JTAG programming/debugging interface port, accessed via the 5x2 header at position H2 (JTAG) on the development board. To evaluate the VRS51L3074, use the VersaKit-30xx VJTAG-USB to interface with Ramtron's Windows®-based Versa Ware JTAG programming/debugging software.



Figure 15: VJTAG-USB interface for programming and debugging the VRS51L3074

5.1.1 Basic VersaKit-30xx setup for VRS51L3074 evaluation

Setup of the VersaKit-30xx is quick and easy. Failure to perform the setup operations in the recommended order may result in software/OS instability.

First, insert the VJTAG-USB into the VersaKit-30xx devboard's Header H2 so that the CN1, USB connector sits directly above the rightmost DB9 connector. If the VJTAG-USB is going to provide the power supply for the devboard, then a jumper should be inserted at position JP1. If the board is going to receive power from an external source, remove the jumper from JP1.



Figure 16: Step 1: Install the VJTAG-USB on the development board

Next, connect the external power supply to the devboard (if required) and then connect the USB cable to the VJTAG-USB board.

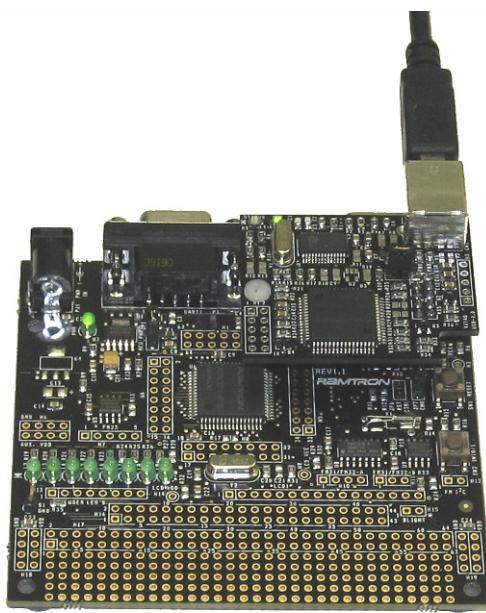


Figure 17: Connecting the USB Cable into the VJTAG-USB (no external power supply)

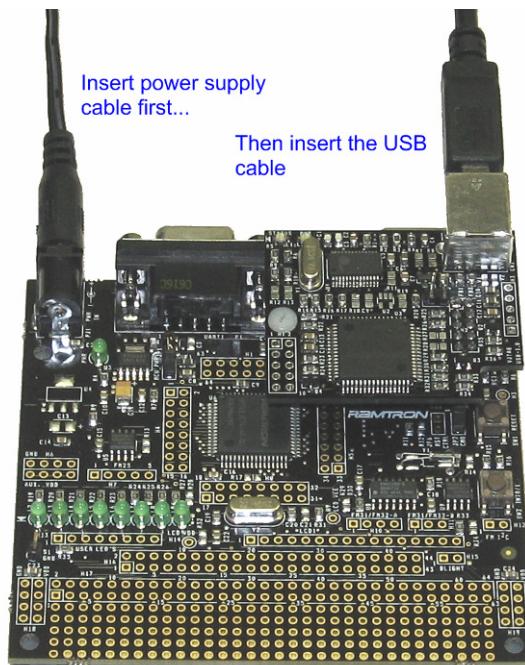


Figure 18: Connecting the power supply to the development board then the USB Cable to the VJTAG-USB

Warning: Do not remove the VJTAG-USB board from the development board without first disconnecting the USB cable. This may cause the Windows® OS to become unstable, requiring a computer reboot.

5.2 Overview of the Versa Ware JTAG Software

Versa Ware JTAG is a Windows®-based software tool that provides a user-friendly development platform for all Ramtron microcontrollers featuring a JTAG interface (the VRS51L2xxx, VRS51L3xxx and future derivatives).

The Versa Ware JTAG Software is composed of two parts:

- **Versa Ware JTAG Programmer**

The Versa Ware JTAG Programmer is used to perform operations such as erase, program, read, etc., on the target device's Flash memory.

- **Versa Ware JTAG Debugger**

The Versa Ware JTAG Debugger is a user interface that links the in-circuit debugger and the source code. All Ramtron MCUs with a JTAG interface include an integrated debugger that enables in-application debugging of the device via its JTAG interface.

The Versa Ware JTAG Debugger is compatible with the SDCC, Keil and Ride compilers.

The Versa Ware JTAG software was developed on Windows XP, but should operate properly on Windows Vista and Windows 2000 operating systems. It should also work on a Window 98 SE operating system on a computer with a UBS interface. Users without a USB interface, can use Ramtron's parallel port version of the JTAG interface. Please contact Ramtron to order one.

The following window shows the in-circuit debugger in action when the source code XRAM, SFR page 0, and watch list windows are open and the program is halted at a breakpoint.

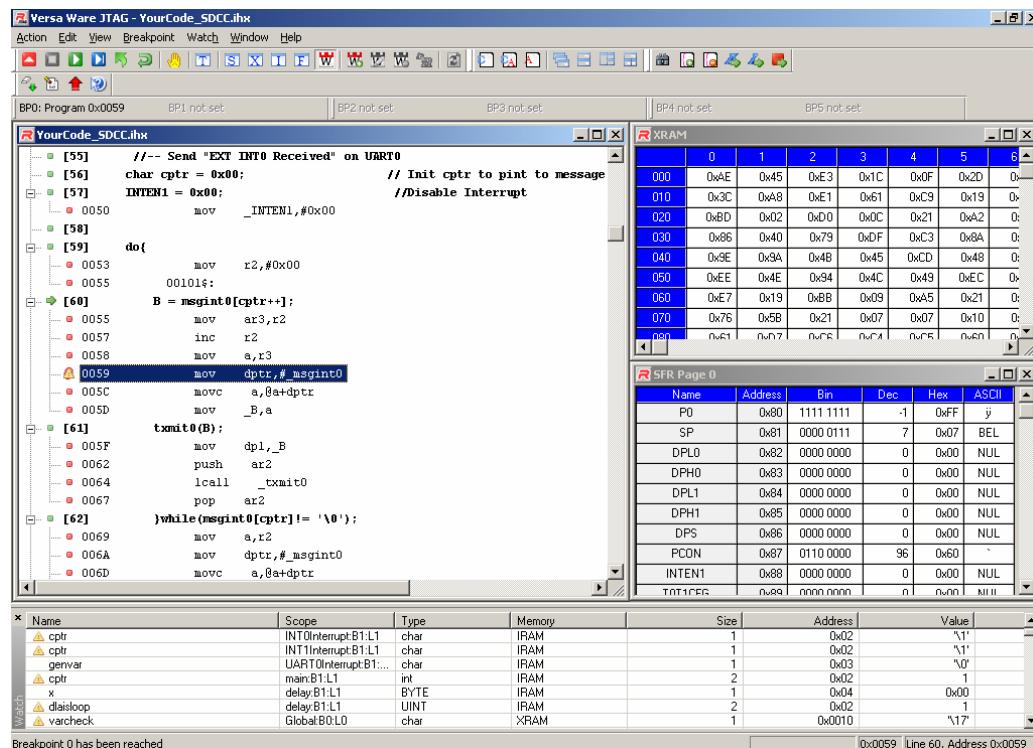


Figure 19: Versa Ware JTAG debugger window

The Versa Ware JTAG Debugger provides a comprehensive set of configuration options allowing users to tailor the user interface, watch variables and breakpoints settings.

5.3 Installing the Versa Ware JTAG Software

Installing the Versa Ware JTAG software is a two-step process that is handled automatically by the installation program.

- Versa Ware JTAG software installation
- Prolific PL2303X USB driver installation

As with most software/driver installations, we suggest creating a System Restore point before running the setup. To install Versa Ware JTAG, run the **Versa_Ware_JTAG_3x_SETUP.exe** file available for download on the Ramtron Web site and follow the instructions provided by the installation wizard.



Figure 20: Versa Ware JTAG Setup

5.4 Getting Started Using the Versa Ware JTAG Software

Once the software is installed, it can be run directly from the setup program, or by clicking on the Versa Ware JTAG shortcut created during the installation process.



5.4.1 Versa Ware JTAG programming interface

Upon startup, the software will attempt to connect to the VJTAG-USB interface.

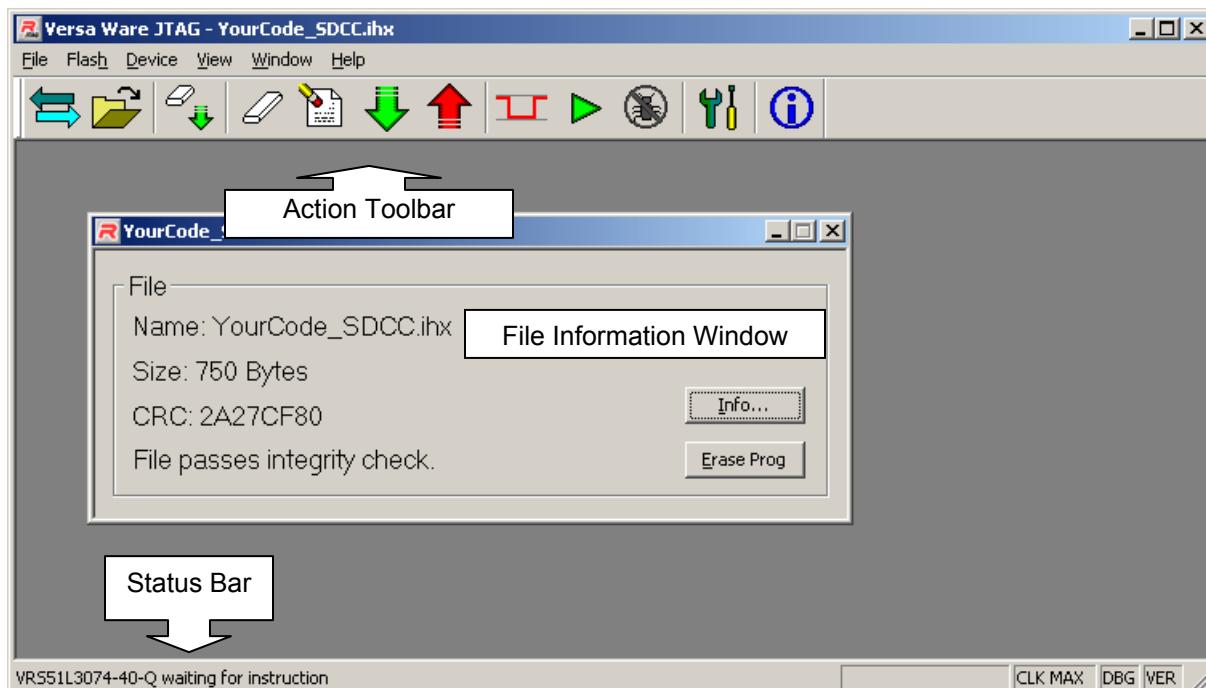


Figure 21: Versa Ware JTAG programming interface

Most of the functions provided by the Versa Ware JTAG software are executable via the action toolbar.

To download a HEX file into the VRS51L3074:

1. Ensure that the Versa-JTAG interface is properly connected to the H2 header of the development board.
2. Click on the synchronize  button. The status bar should show: "VRS51L3074-40-Q waiting for instruction".
3. Click open  to select the HEX file to be programmed into the VRS51L3074.
4. Click erase then program  to erase and program the Flash. By default, after this process is complete, the program will start.

The  synchronize button can be used to halt execution of the VRS51L3074 program and put the device into program mode. The  run button restarts program execution.

The options  button allows configuring the programming options, set the Flash security options, and activates the in-circuit debugger.



Figure 22: Versa Ware JTAG Device Options

Changes to any of the device options will become effective the next time an erase then program  operation is initiated.

5.4.2 Using the Versa Ware JTAG Debugger

Once the program is loaded into the VRS51L3074 Flash memory and the debugger is enabled, activate the debugger by clicking on the debugger  button. Upon startup, the debugger will halt the processor at address 0x0000 and wait.

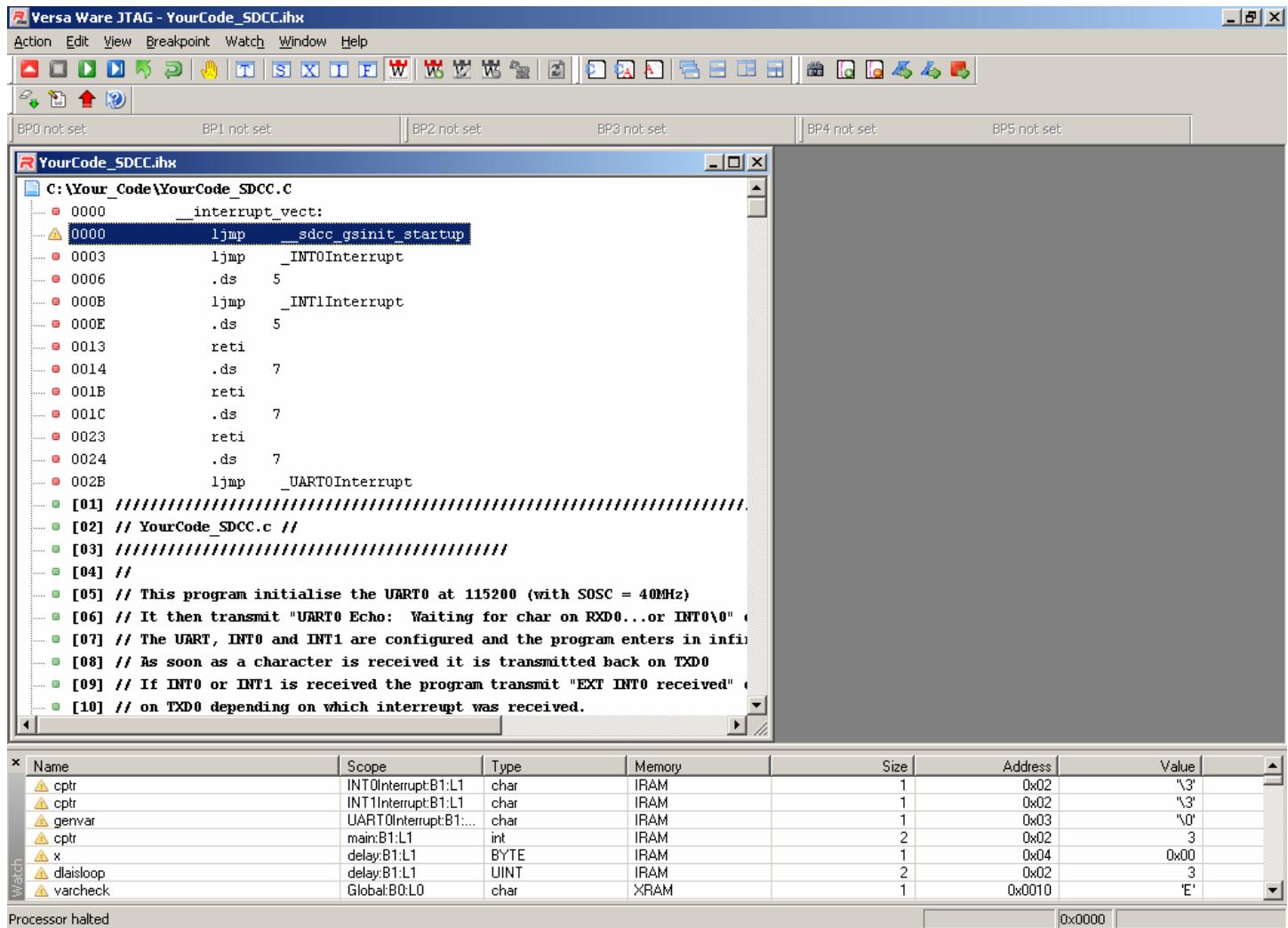


Figure 23: Versa Ware Debugger upon startup

Once the debugger starts, you can either run the program at full speed by clicking on run  or set a breakpoint anywhere in the code by either double clicking on a specific code line and then pressing run  or by setting the breakpoint manually. Alternatively, you can manually set breakpoints anywhere in the code by clicking the breakpoint setting button .

When a breakpoint is set in the code, the breakpoint reference number will be displayed in red right next to the code line. The breakpoint toolbar will then display the active breakpoint. Double clicking again on a given code line where a breakpoint has been set will disable that breakpoint.

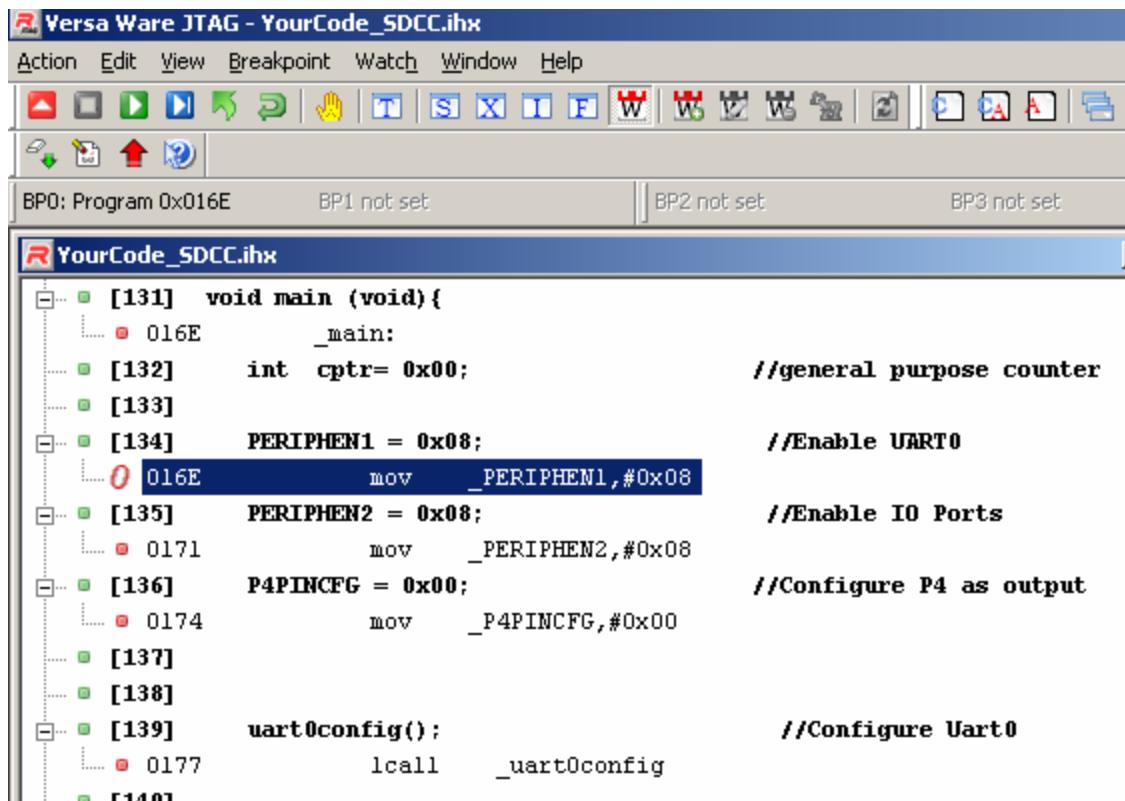


Figure 24: Setting Breakpoint by double clicking on a code line

Once a breakpoint is set, click on run . The processor will then start executing code at full speed until a breakpoint is reached or halted .

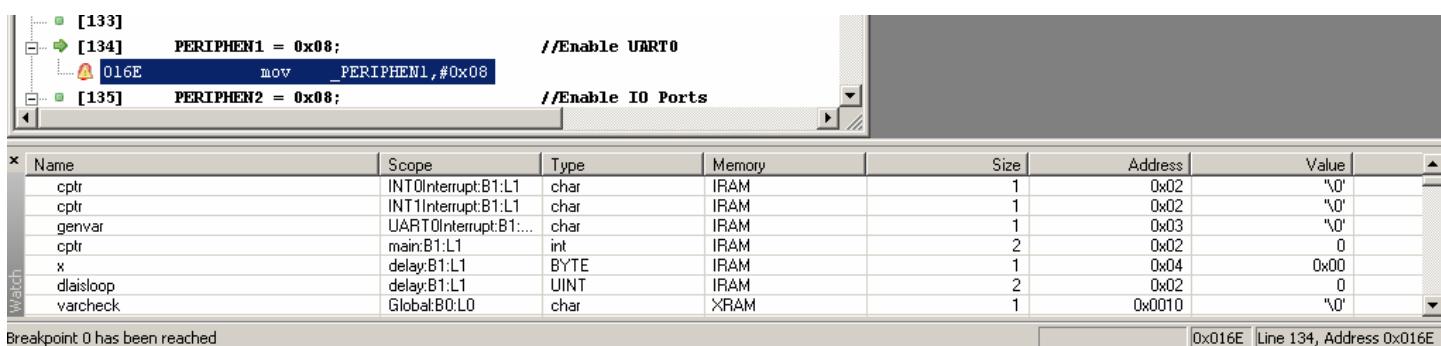


Figure 25: Breakpoint reached

Once a breakpoint is reached, you can either:

- Restart the program by clicking again on run .
- Single step through the code by clicking on step .
- View/Edit the SFR, IRAM, XRAM memory location by clicking SFR , IRAM  and XRAM  buttons.

When step  is clicked, the processor will execute the current instruction and step to the next instruction (and actually stop). The SFR, IRAM, XRAM or FRAM memory content can be viewed and edited at any time after a breakpoint is reached (this includes step  mode). The debugger provides table and list view options for the SFR, IRAM, XRAM and FRAM memory areas. It is also possible to open multiple windows for each of these memory areas.

Editing a given SFR, IRAM, XRAM and FRAM memory cell is simple:

- Double click on the memory location to be edited.
- Type in the new value to be written.
- Press <Enter> or double click another memory location.

Notes on the SFR edition:

In the case of the SFR memory location, it is important to note that some registers are partially or totally read or write only or can only be accessed when the related peripheral is activated. The SFR edition feature allows the user to partially control the peripheral.

5.5 Updating the Code without exiting the debugger

If during a debug session, you want to modify the code, recompile and reload the code into the Flash memory. The Versa Ware JTAG allows you to reload the code in Flash memory without exiting the Versa Ware JTAG debugging environment.

To do this, open the editor, modify the code and recompile it. Then return to the debugger and click on erase then program  button. Note that all the breakpoints you have set will be lost.

5.6 Exiting the Debugger

To exit the debugger, click on stop debugging . This will bring you back in the Versa Ware JTAG programming environment.

5.7 Summary of Versa Ware JTAG Debugger Commands

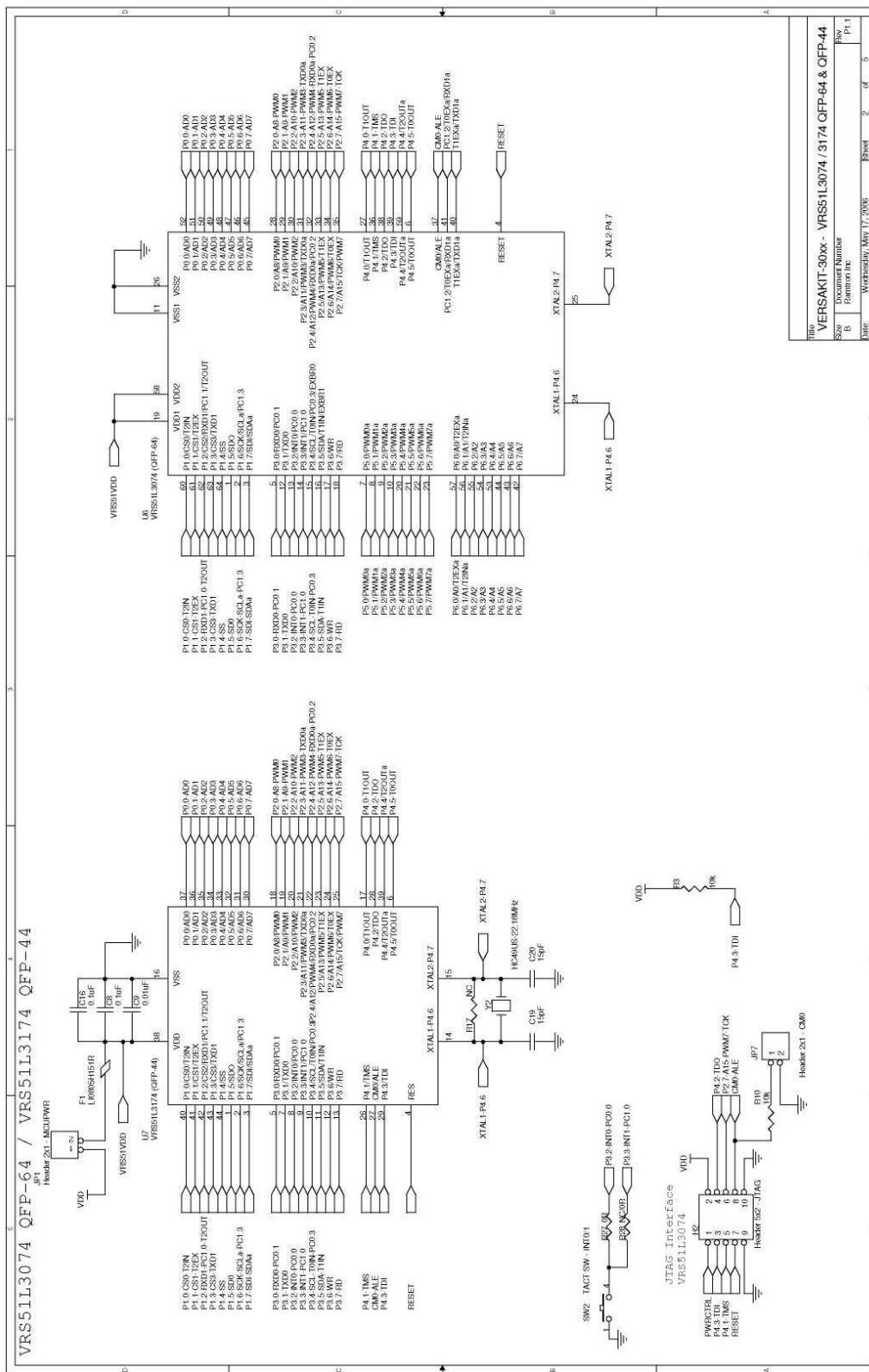
The following table summarizes the Versa Ware JTAG Debugger commands. Please consult the Versa Ware JTAG help for a detailed description of software features.

Table 4: Debugger command set

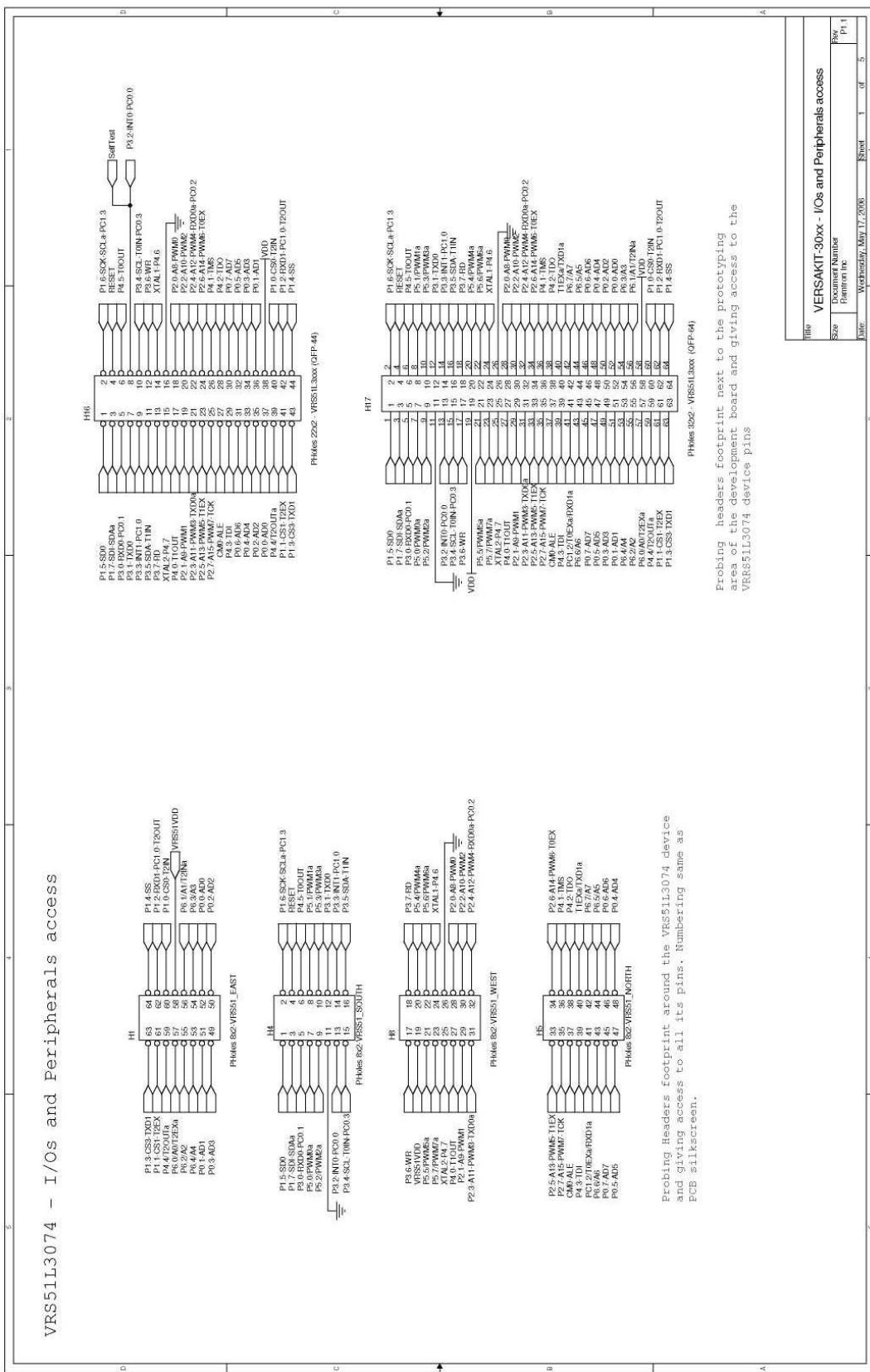
Command	Toolbar	Toolbar button	Menu	Keyboard Shortcut
Stop Debugging	Debugger		Action	
Halt	Debugger		Action	Ctrl + Backspace
Run	Debugger		Action	F7
Step	Debugger		Action	F6
Jump	Debugger		Action	
Restart	Debugger		Action	
Breakpoint Settings	Debugger		Breakpoint	Ctrl + Shift + B
Toggle Breakpoint 0			Breakpoint	Ctrl + B
Toggle Breakpoint 1 - 5			Breakpoint	Ctrl + F1 to Ctrl + F5
Run to Cursor			Breakpoint	F12
View Program Trace	Debugger		View	Ctrl + Shift + T
View SFR	Debugger		View	Ctrl + Shift/Alt + S
View XRAM	Debugger		View	Ctrl + Shift/Alt + X
View IRAM	Debugger		View	Ctrl + Shift/Alt + I
View FRAM (VRS51L307x)	Debugger		View	Ctrl + Shift + F
View Watch	Debugger		View	Ctrl + Shift + W
View Toolbars			View	
View Options			View	Ctrl + Shift + V
Add Watch	Debugger		Watch	
Edit Watch	Debugger		Watch	
Remove Watch	Debugger		Watch	
Force Watch	Debugger		Watch	
Refresh	Debugger		View	Ctrl + R
View C files	View			
View C + Asm	View			
View Assembler files	View			
Cascade	View		Window	
Tile	View		Window	
60:40 Horizontal	View		Window	
75:25 Vertical	View		Window	
Find			Edit	Ctrl + F
Find Next			Edit	F3
Copy			Edit	Ctrl + C
Next Function Block			Edit	Ctrl + PgDn
Previous Function Block			Edit	Ctrl + PgUp
Go to Address			Edit	Ctrl + Alt + G
Go to Line			Edit	Ctrl + Shift + G
Go to Stopped			Edit	Ctrl + G
Erase then Program	Program		Flash	F5
Erase Page	Program		Flash	
Read Flash	Program		Flash	
Help topics			Help	
About Versa Ware JTAG				

6 VersaKit-30xx Development Board Schematics

6.1 VRS51L3074



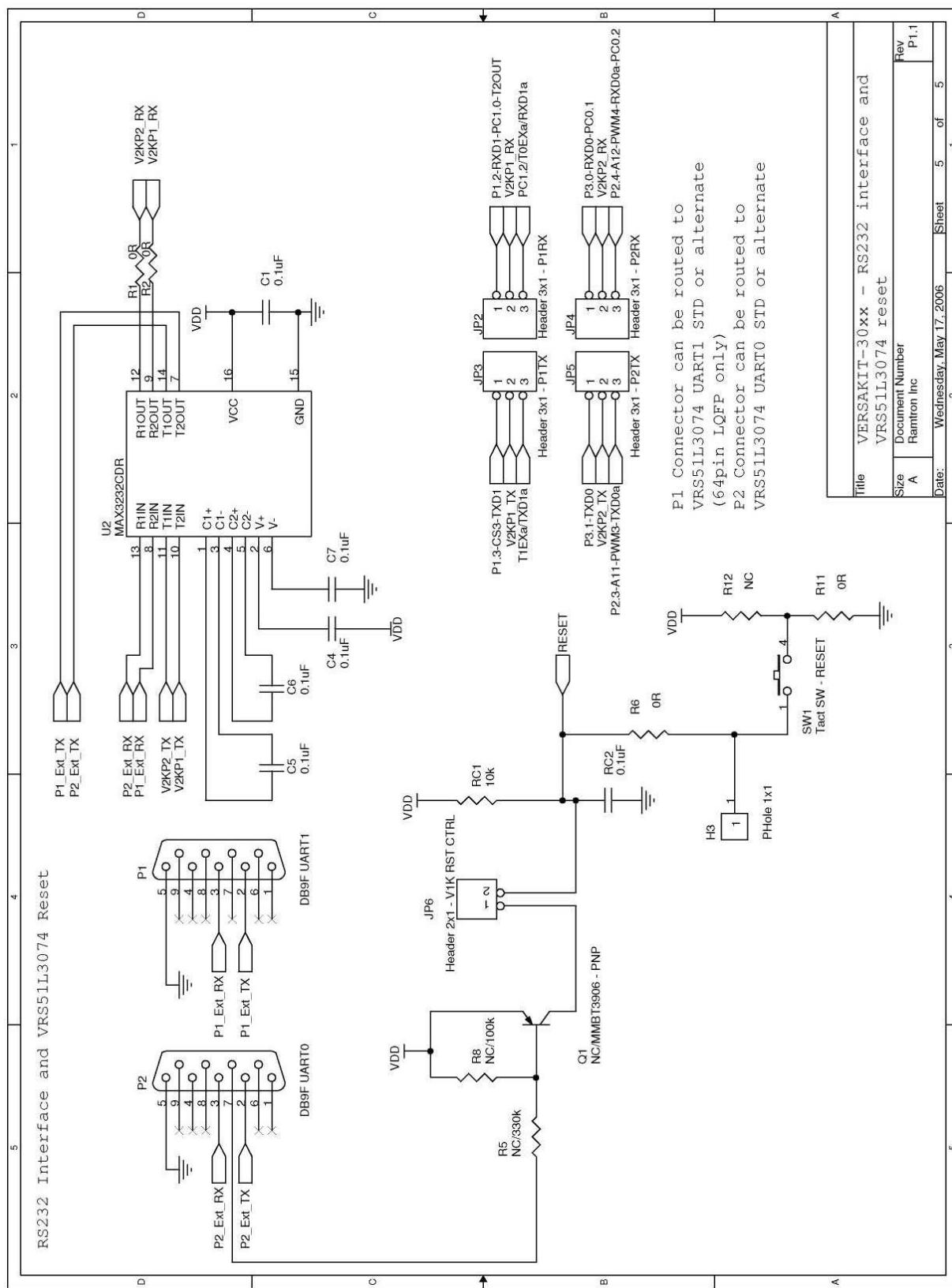
6.2 VRS51L3074 Peripheral Access



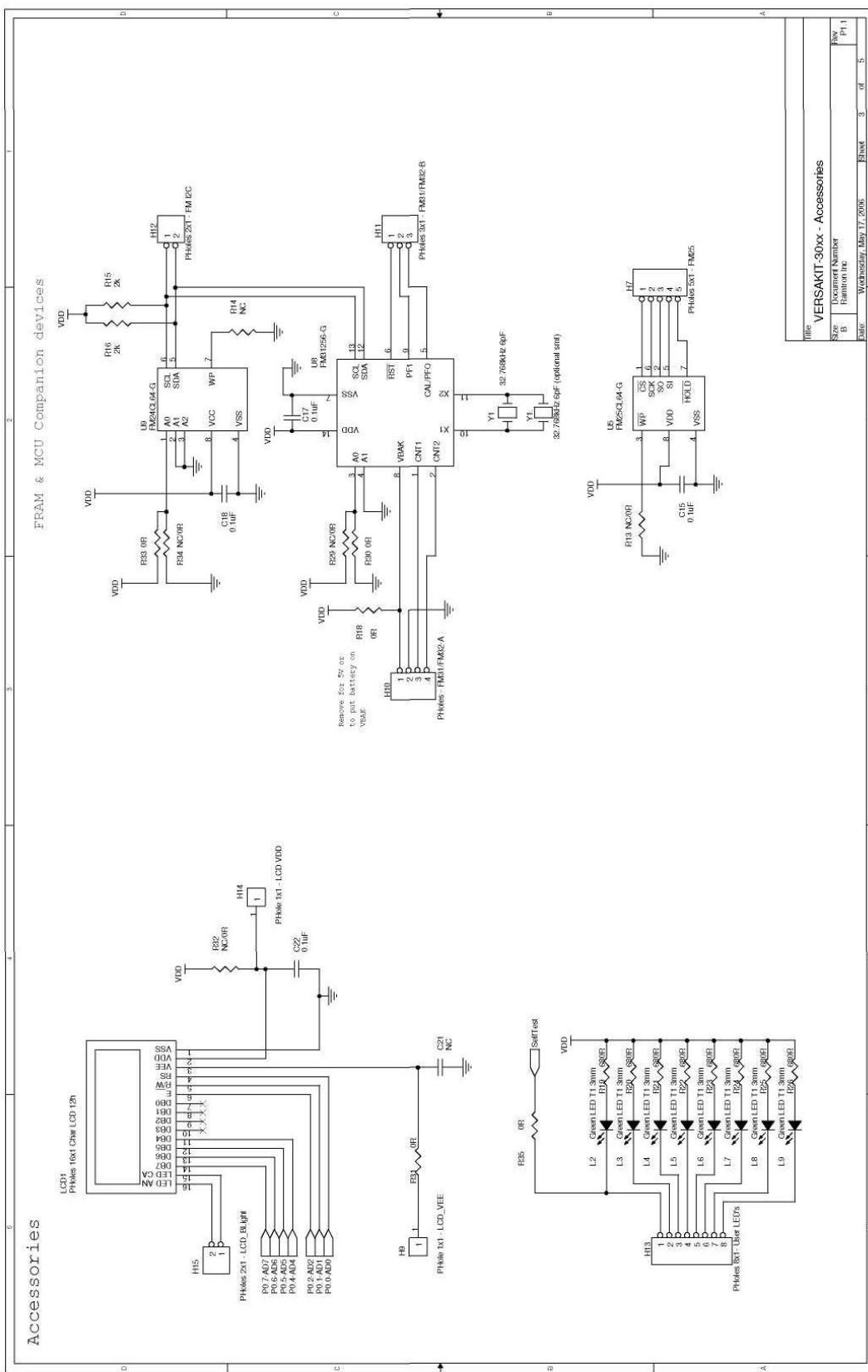
Probing Headers footprint around the VRS51L3074 device and giving access to all its pins. Numbering same as

Probing headers footprint next to the prototyping area of the development board and giving access to the VRR351L3074 device pins

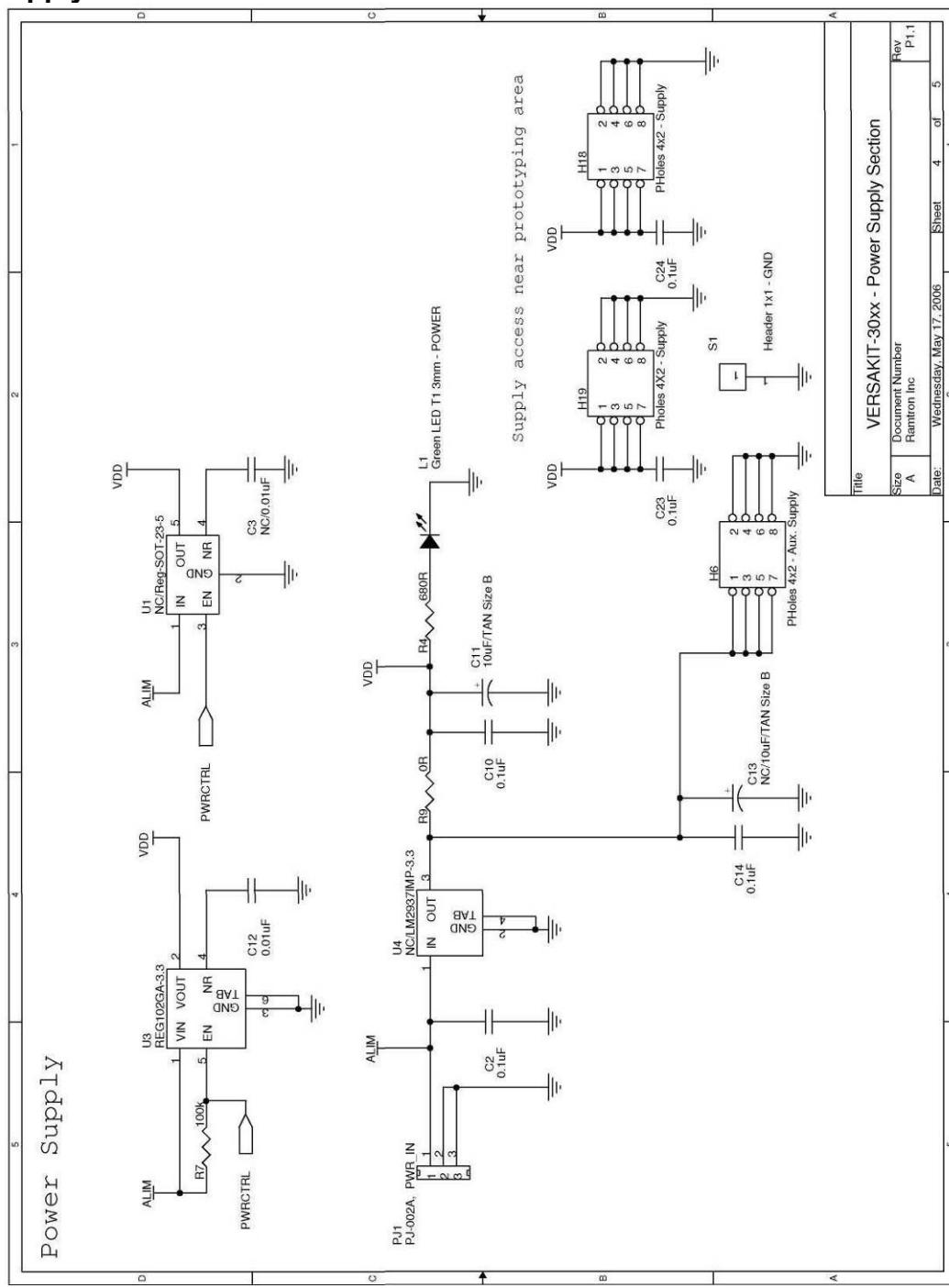
6.3 RS-232 Interface and Reset



6.4 Accessories



6.5 Power Supply



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