

PIC32MK 100-pin Motor Control Plug-In Module (PIM) Information Sheet

The PIC32MK 100-pin Motor Control Plug-in Module (PIM) (MA320024) is designed to demonstrate the capabilities of PIC32MK 100-pin Motor Control devices using external or internal on-chip op amps with the following hardware:

- dsPICDEM™ MCLV-2 Development Board (DM330021-2)
- dsPICDEM™ MCHV-2 Development Board (DM330023-2)
- dsPICDEM™ MCHV-3 Development Board (DM330023-3)

All three development boards support 100-pin PIM interfaces. For example, the PIC32MK1024MCF100 is a 32-bit Motor control microcontroller in a 100-pin TQFP package that can be used with all three boards.

Selecting the External On-board Op Amp Configuration

To operate the PIC32MK 100-pin Motor Control PIM using external on-board op amps, insert the External Op amp Configuration Board, which is included with the development board, into the appropriate header for the hardware in use:

- J14 (dsPICDEM MCLV-2 Development Board)
- J4 (dsPICDEM MCHV-2/MCHV-3 Development Board). In addition, for the MCHV-2/MCHV-3, ensure that jumpers are set at position 1-2 for J12, J13, J14, and position 5-6 for J11.

Figure 1 shows the connection location for the external on-board op amp on the dsPICDEM MCLV-2 Development Board.

FIGURE 1: EXTERNAL OP AMP CONFIGURATION BOARD



Selecting the Internal On-board Op Amp Configuration

To operate the PIC32MK 100-pin Motor Control PIM using internal on-chip Op Amps, insert the Internal Op Amp Configuration Board, which is included with the development board, into the appropriate header for the hardware in use:

- J14 (dsPICDEM MCLV-2 Development Board)
- J4 (dsPICDEM MCHV-2/MCHV-3 Development Board)

Figure 2 shows the connection location for the internal on-board op amp on the dsPICDEM MCLV-2 Development Board.

FIGURE 2: INTERNAL OP AMP CONFIGURATION BOARD



WARNING: Do not connect non-isolated oscilloscope probes to probe any traces while using the PIM with the dsPICDEM MCHV-2 or dsPICDEM MCHV-3 Development Boards. Instead, use a high-voltage differential probe, rate in excess of 600 VRMS (Common mode). Failure to heed this warning could result in hardware damage.

Table 1 provides the static mapping between the 100-pin PIM pins and the 100-pin device pins.

Figure 3 shows the 100-pin PIM header schematic.

Figure 4 shows the 100-pin PIM device schematic.

PIC32MK

TABLE 1: 100-PIN DEVICE TO 100-PIN PIM MAPPING

Device Pin Number	PIC32MK 100-pin Device Functional Description	PIM Pin Number	Device Pin Number	PIC32MK 100-pin Device Functional Description	PIM Pin Number
1	RG15	1	51	AN24	25
2	VDD	2	52	RPE0 (C1TX)	77, 88
3	RPA7 (U3TX)	51, 76	53	AN41/RPE1 (INDX2)	43
4	PWM1H	94	54	VBUS	—
5	PWM1L	93	55	VBUS3V3	62
6	PWM5L	4	56	D1-	—
7	PWM5H	71	57	D1+	—
8	PWM6L	6	58	VBUS2	53
9	PWM6H	7	59	D2-	54
10	RPG6 (HOME2)	61	60	D2+	55
11	AN18	29	61	RF5	60
12	AN17/RPG8 (QEB2)	42	62	VDD	62
13	MCLR	13	63	CLKI	—
14	AN16/RPG9 (QEA2)	41	64	RC15	64
15	VSS	15	65	VSS	65
16	VDD	16	66	RPA14 (INDX2)	48
17	AN22	8	67	RPA15 (U3RX)	52, 72
18	AN21	9	68	RD8	68
19	AN20	79	69	PGED2	27
20	AN10	35	70	PGEC2	26
21	AN9	24	71	DAC2	H
22	OA2OUT	D2	72	AN25	23
23	OA2IN+ (INDX2)	F2	73	RPC13	91
24	OA2IN-	E2	74	RPB8	92
25	OA1OUT	D1	75	VSS	75
26	OA1IN+ (QEB2)	F1	76	RPB9 (U2TX)	50
27	OA1IN-	E1	77	USBID2	56
28	VREF-	—	78	RC7	84
29	VREF+	28	79	RD12	69
30	AVDD	30	80	RD13	58
31	AVSS	31	81	RPC8 (U2RX)	49, 70
32	OA3OUT	D3	82	RD5	82
33	OA3IN-	E3	83	RD6	—
34	OA3IN+ (QEA2)	F3	84	RPC9	80
35	RC11	33	85	VSS	85
36	VSS	36	86	VDD	86
37	VDD	37	87	RPF0 (C1RX)	78, 87
38	RG11	34	88	RF1	89
39	AN36	38	89	RG1	83
40	AN37	69	90	RG0	90
41	AN12	40	91	RF6	59
42	FLT6	19	92	RF7	—
43	RPE14 (QEB2)	47	93	PWM3H	3
44	AN15	32	94	PWM3L	100
45	VSS	45	95	RG14	95
46	VDD	46	96	RG12	96
47	RD14	44	97	RG13	97
48	RD15	—	98	PWM2H	99
49	DAC3	85	99	PWM2L	98
50	FLT15	18	100	TDO	—

FIGURE 3: 100-PIN PIM HEADER SCHEMATIC

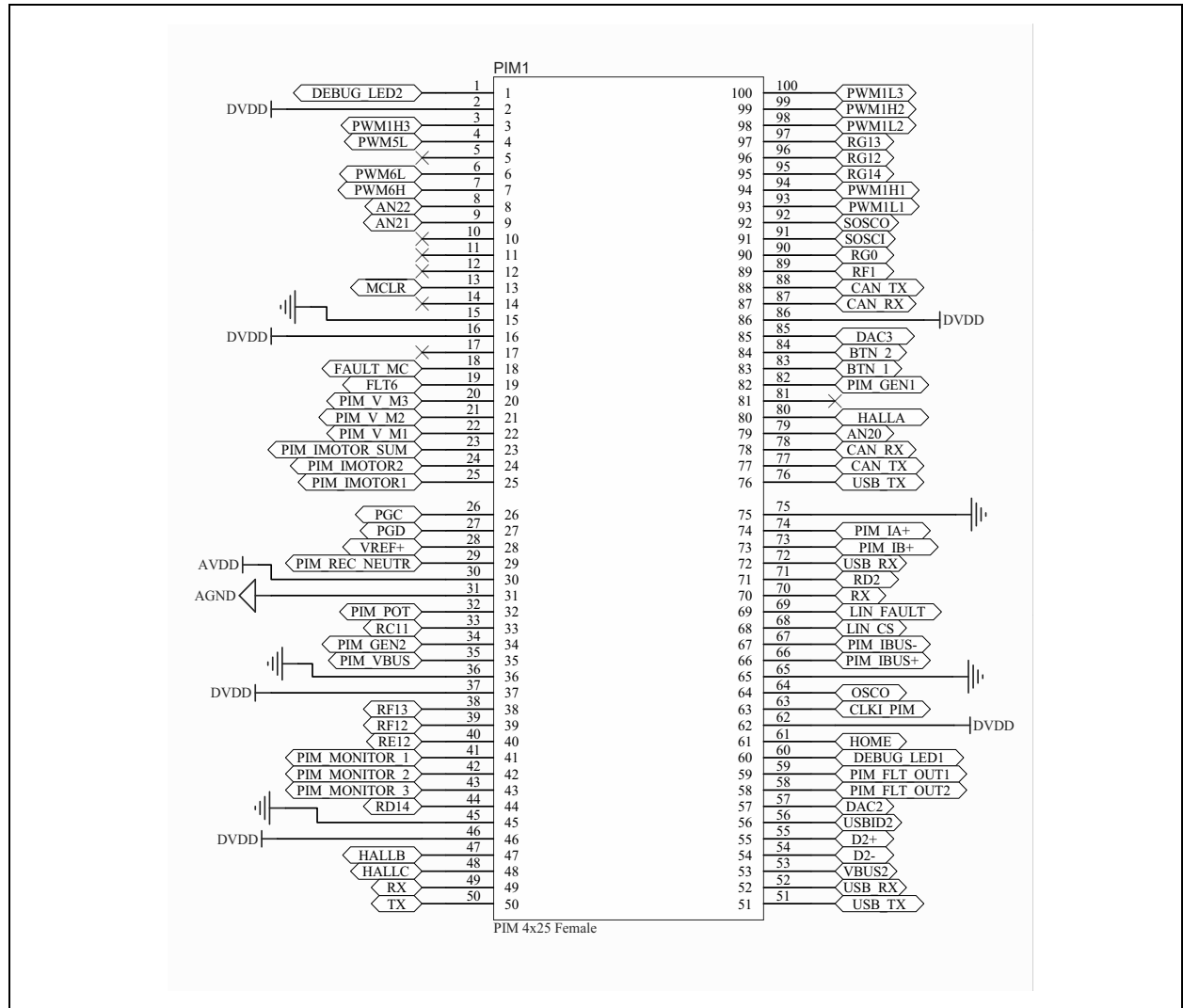
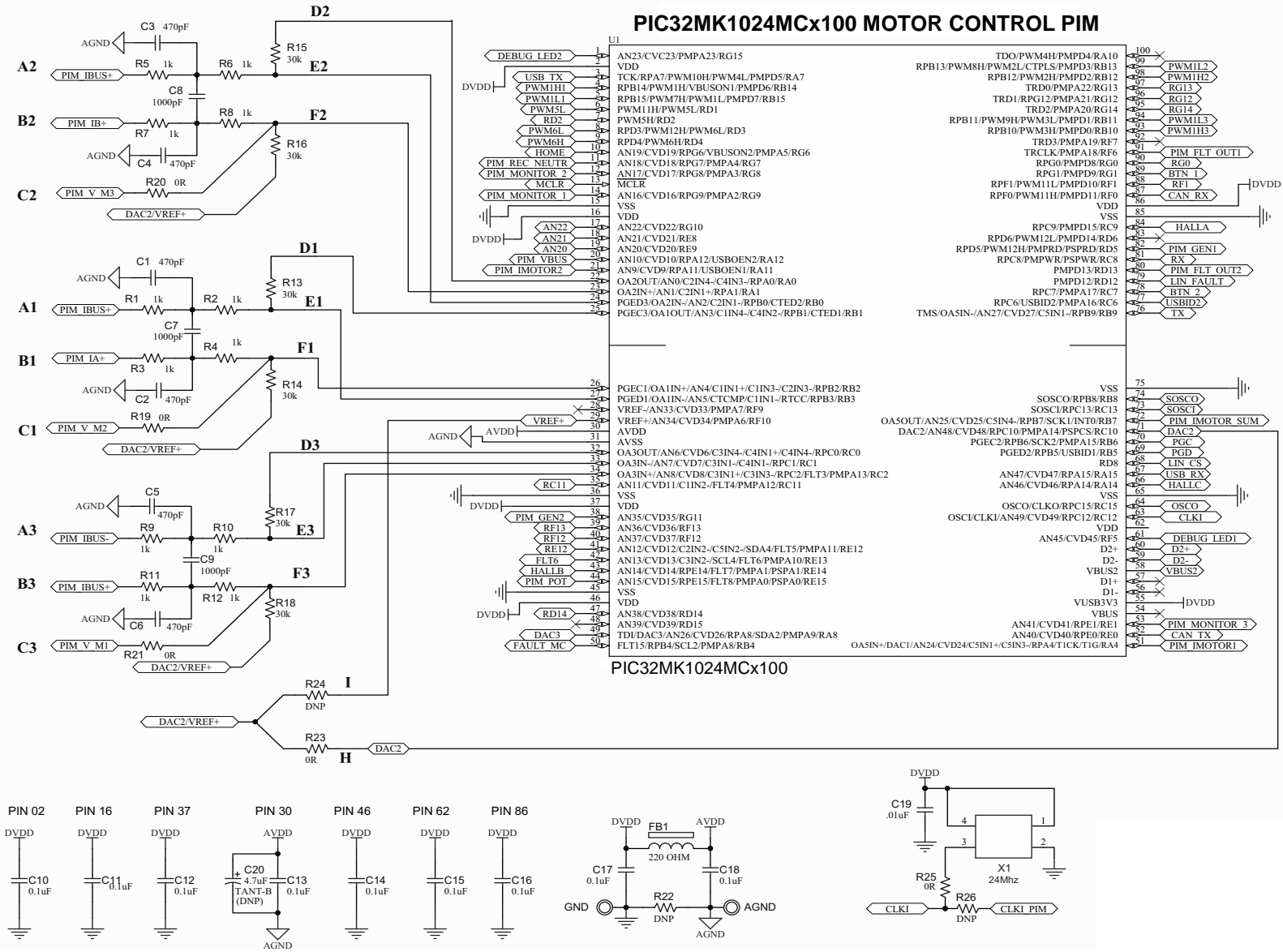


FIGURE 4: 100-PIN PIM DEVICE SCHEMATIC

The reference voltage (VREF) biases the op amps to VDD/2 so that bidirectional motor phase current can be sensed using unipolar op amps. The source of VREF can be selected either from the development board or from the internally generated reference voltage using DAC2 and resistors R23/R24, as shown in Figure 4. By default, the PIM is configured to source the reference voltage, internally generated using DAC2 by populating R23 and keeping R24 depopulated.

To source the reference voltage from Motor Control PIM, R23 needs to be depopulated and R24 must be populated with a zero ohm resistor.

The internal op amp configuration and passive resistor-capacitive network configures the filter bandwidth, op amp bias and op amp gain, as shown in Figure 4.

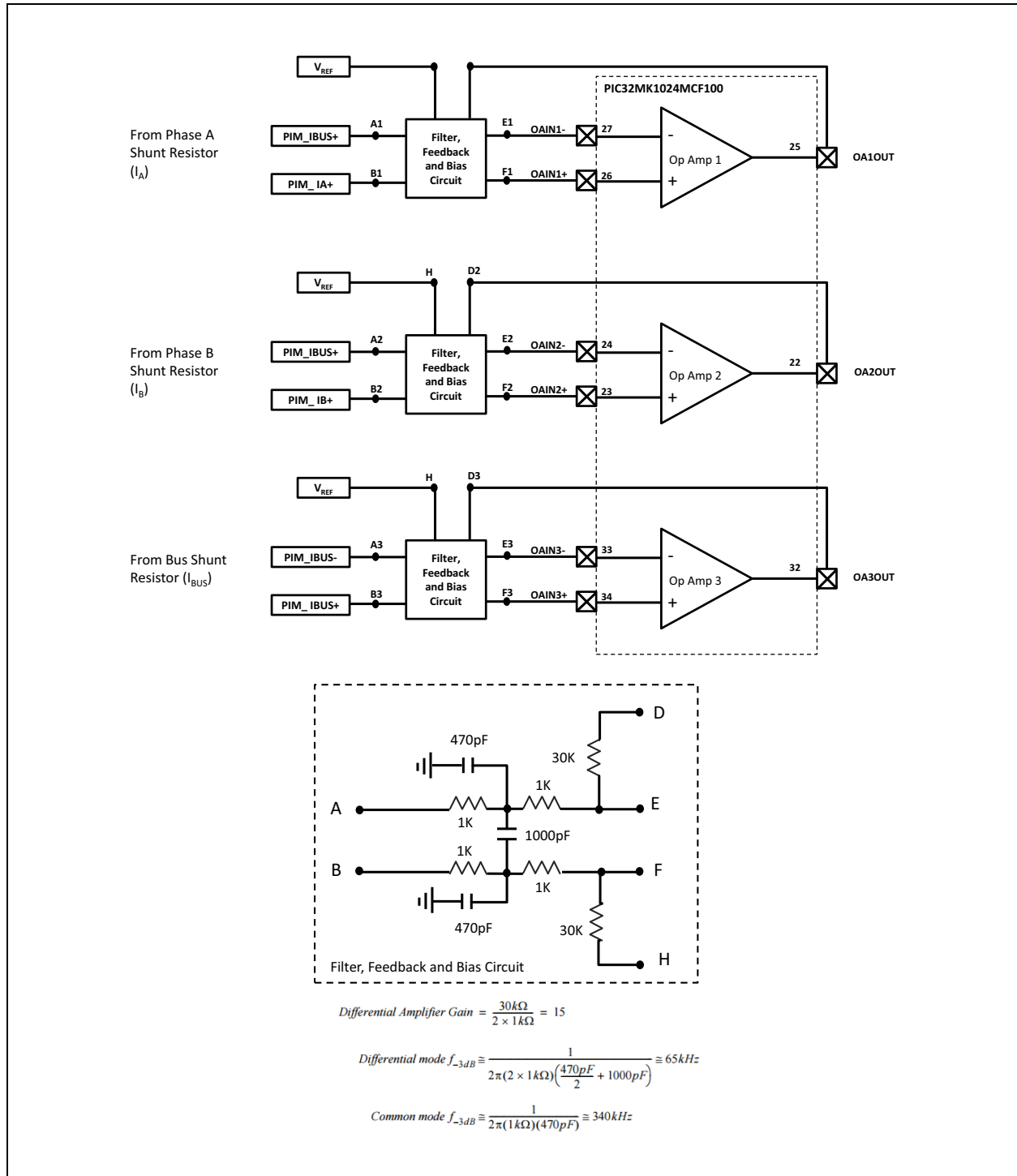
Table 2 classifies the passive components according to their functionality and also specifies the design equations for filter bandwidth and op amp gain.

TABLE 2: ANALOG FUNCTIONALITY LISTING

Op Amp Number	Analog Function	Passive Components	Design Equations
1	Low-Pass Filter	R1, R2, R3, R4, C1, C2, C7	$R1 \quad R2 \quad R3 \quad R4 \quad R$ $C1 \quad C2 \quad C$
	Differential Amplifier Input	R1, R2, R3, R4	
	Differential Amplifier Feedback	R13	$Common\ mode\ f_{-3dB} \cong \frac{1}{2\pi RC}$ $Differential\ mode\ f_{-3dB} \cong \frac{1}{2\pi(2R)\left(\frac{C}{2} \quad C_7\right)}$ $DifferentialAmplifierGain \quad \frac{R_{13}}{2R}$
2	Low-Pass Filter	R5, R6, R7, R8, C3, C4, C8	$R5 \quad R6 \quad R7 \quad R8 \quad R$ $C3 \quad C4 \quad C$
	Differential Amplifier Input	R5, R6, R7, R8	
	Differential Amplifier Feedback	R15	$Common\ mode\ f_{-3dB} \cong \frac{1}{2\pi RC}$ $Differential\ mode\ f_{-3dB} \cong \frac{1}{2\pi(2R)\left(\frac{C}{2} \quad C_8\right)}$ $DifferentialAmplifierGain \quad \frac{R_{15}}{2R}$
3	Low-Pass Filter	R9, R10, R11, R12, C5, C6, C9	$R9 \quad R10 \quad R11 \quad R12 \quad R$ $C5 \quad C6 \quad C$
	Differential Amplifier Input	R9, R10, R11, R12	
	Differential Amplifier Feedback	R17	$Common\ mode\ f_{-3dB} \cong \frac{1}{2\pi RC}$ $Differential\ mode\ f_{-3dB} \cong \frac{1}{2\pi(2R)\left(\frac{C}{2} \quad C_9\right)}$ $DifferentialAmplifierGain \quad \frac{R_{17}}{2R}$

Figure 5 illustrates a typical block diagram of the op amp circuit.

FIGURE 5: OP AMP CIRCUIT BLOCK DIAGRAM



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