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PCI Express Bandwidth to Be Doubled Again: PCIe 6.0 Announced, Spec to Land in 2021

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by Ryan Smith on June 18, 2019 5:00 PM EST

Posted in CPUs PCIe PCI-SIG PCIe 6.0

When the PCI Special Interest Group (PCI-SIG) first announced PCIe 4.0 a few years back, the group made it clear that they were not just going to make up for lost time after PCIe 3.0, but that they were going to accelerate their development schedule to beat their old cadence. Since then the group has launched the final versions of the 4.0 and 5.0 specifications, and now with 5.0 only weeks old, the group is announcing today that they are already hard at work on the next version of the PCIe specification, PCIe 6.0. True to PCIe development iteration, the forthcoming standard will once again double the bandwidth of a PCIe slot – a x16 slot will now be able to hit a staggering 128GB/sec – with the group expecting to finalize the standard in 2021.

As with the PCIe iterations before it, the impetus for PCIe 6.0 is simple: hardware vendors are always in need

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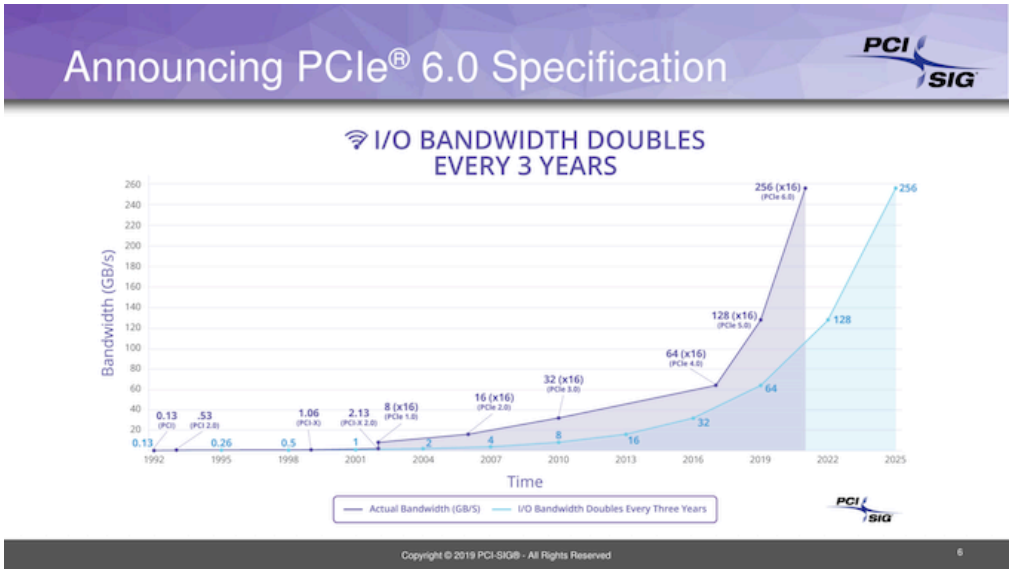
have all extended PCIe, and will in turn benefit from PCIe improvements. So PCIe speed boosts serve as the core of building ever-faster (and more interconnected) systems.



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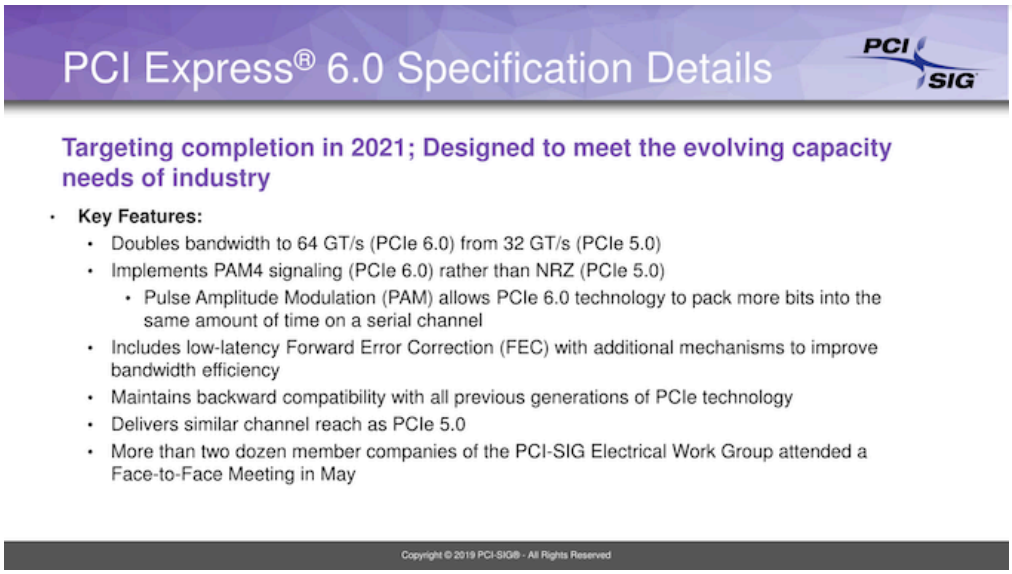
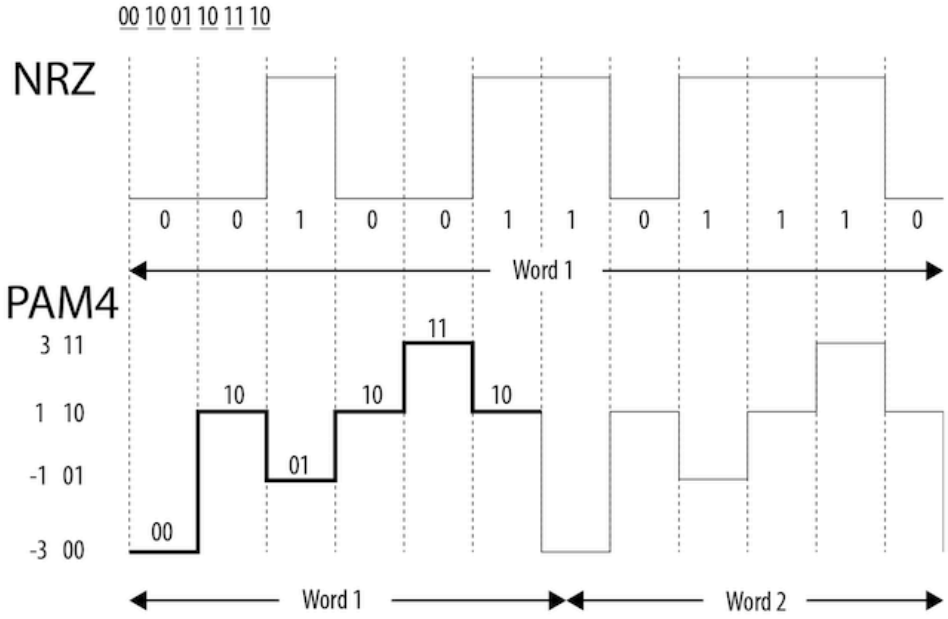
PCIe 6.0, in turn, is easily the most important/most disruptive update to the PCIe standard since PCIe 3.0 almost a decade ago. To be sure, PCIe 6.0 remains backwards compatible with the 5 versions that have preceded it, and PCIe slots aren't going anywhere. But with PCIe 4.0 & 5.0 already resulting in very tight signal requirements that have resulted in ever shorter trace length limits, simply doubling the transfer rate yet again isn't necessarily the best way to go. Instead, the PCI-SIG is going to upend the signaling technology entirely, moving from the Non-Return-to-Zero (NRZ) tech used since the beginning, and to Pulse-Amplitude Modulation 4 (PAM4).



At a *very* high level, what PAM4 does versus NRZ is to take a page from the MLC NAND playbook, and double the number of electrical states a single cell (or in this case, transmission) will hold. Rather than traditional 0/1 high/low signaling, PAM4 uses 4 signal levels, so that a signal can encode for four possible two-bit patterns: 00/01/10/11. This allows PAM4 to carry twice as much data as NRZ without having to double the transmission bandwidth, which for PCIe 6.0 would have resulted in a frequency around 30GHz(!).



NRZ vs. PAM4 (Base Diagram Courtesy Intel)

PAM4 itself is not a new technology, but up until now it's been the domain of ultra-high-end networking standards like 200G Ethernet, where the amount of space available for more physical channels is even more limited. As a result, the industry already has a few years of experience working with the signaling standard, and with their own bandwidth needs continuing to grow, the PCI-SIG has decided to bring it inside the chassis by basing the next generation of PCIe upon it.

The tradeoff for using PAM4 is of course cost. Even with its greater bandwidth per Hz, PAM4 currently costs more to implement at pretty much every level, from the PHY to the physical layer. Which is why it hasn't taken the world by storm, and why NRZ continues to be used elsewhere. The sheer mass deployment scale of PCIe will of course help a lot here – economies of scale still count for a lot – but it will be interesting to see where things stand in a few years once PCIe 6.0 is in the middle of ramping up.

Meanwhile, not unlike the MLC NAND in my earlier analogy, because of the additional signal states a PAM4 signal itself is more fragile than a NRZ signal. And this means that along with PAM4, for the first time in PCIe's

retransmission (such as DisplayPort 1.4 w/DSC). While FEC hasn't been necessary for PCIe until now, PAM4's fragility is going to change that. The inclusion of FEC shouldn't make a noticeable difference to end-users, but for the PCI-SIG it's another design requirement to contend with. In particular, the group needs to make sure that their FEC implementation is low-latency while still being appropriately robust, as PCIe users won't want a significant increase in PCIe's latency.

The upshot of the switch to PAM4 then is that by increasing the amount of data transmitted without increasing the frequency, the signal loss requirements won't go up. PCIe 6.0 will have the same 36dB loss as PCIe 5.0, meaning that while trace lengths aren't officially defined by the standard, a PCIe 6.0 link should be able to reach just as far as a PCIe 5.0 link. Which, coming from PCIe 5.0, is no doubt a relief to vendors and engineers alike.

Even with these changes, however, as previously mentioned PCIe 6.0 is fully backwards compatible with earlier standards, and this will go for both hosts and peripherals. This means that to a certain extent, hardware designers are essentially going to be implementing PCIe twice: once for NRZ, and again for PAM4. This will be handled at the PHY level, and while it's not a true doubling of logic (what is NRZ but PAM4 with half as many signal levels?), it does mean that backwards compatibility is a bit more work this time around. Though discussing the matter in today's press conference, it doesn't sound like the PCI-SIG is terribly concerned about the challenges there, as PHY designers have proven quite capable (e.g. Ethernet).

PCI Express Bandwidth
(Full Duplex)

Slot Width	PCIe 1.0 (2003)	PCIe 2.0 (2007)	PCIe 3.0 (2010)	PCIe 4.0 (2017)	PCIe 5.0 (2019)	PCIe 6.0 (2021)
x1	0.25GB/sec	0.5GB/sec	~1GB/sec	~2GB/sec	~4GB/sec	~8GB/sec
x2	0.5GB/sec	1GB/sec	~2GB/sec	~4GB/sec	~8GB/sec	~16GB/sec
x4	1GB/sec	2GB/sec	~4GB/sec	~8GB/sec	~16GB/sec	~32GB/sec
x8	2GB/sec	4GB/sec	~8GB/sec	~16GB/sec	~32GB/sec	~64GB/sec
x16	4GB/sec	8GB/sec	~16GB/sec	~32GB/sec	~64GB/sec	~128GB/sec

Putting all of this in practical terms then, PCIe 6.0 will be able to reach anywhere between ~8GB/sec for a x1 slot up to ~128GB/sec for a x16 slot (e.g. accelerator/video card). For comparison's sake, 8GB/sec is as much bandwidth as a PCIe 2.0 x16 slot, so over the last decade and a half, the number of lanes required to deliver that kind of bandwidth has been cut to 1/16th the original amount.

Overall, the PCI-SIG has set a rather aggressive schedule for this standard: the group has already been working on it, and would like to finalize the standard in 2021, two years from now. This would mean that the PCI-SIG will have improved PCIe's bandwidth by eight-fold in a five-year period, going from PCIe 3.0 and its 8 GT/sec rate in 2016 to 4.0 and 16 GT/sec in 2017, 5.0 and 32 GT/sec in 2019, and finally 6.0 and 64 GT/sec in 2021. Which would be roughly half the time it has taken to get a similar increase going from PCIe 1.0 to 4.0.

As for end users and general availability of PCIe 6.0 products, while the PCI-SIG officially defers to the hardware vendors here, the launch cycles of PCIe 4.0 and 5.0 have been very similar, so PCIe 6.0 will likely follow in those same footsteps. 4.0, which was finalized in 2017, is just now showing up in mass market hardware in 2019, and meanwhile Intel has already committed to PCIe 5.0-capable CPUs in 2021. So we may see PCIe 6.0 hardware as soon as 2023, assuming development stays on track and hardware vendors move just as quickly to implement it as they have on earlier standards. Though for client/consumer use, it bears pointing out that with the rapid development pace for PCIe – and the higher costs that PAM4 will incur – just because the PCI-SIG develops 6.0 it doesn't mean it will show up in client decides any time soon; economics and bandwidth needs will drive that decision.

Speaking of which, as part of today's press conference the group also gave a quick update on PCIe compliance testing and hardware rollouts. PCIe 4.0 compliance testing will finally kick off in August of this year, which should further accelerate 4.0 adoption and hardware support. Meanwhile PCIe 5.0 compliance testing is still under development, and like 4.0, once 5.0 compliance testing becomes available it should open the flood gates to much faster adoption there as well.

Source: PCI-SIG

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shabby - Tuesday, June 18, 2019 - link

I guess intel will skip 4 and 5 because their new desktop products will be out in 2021? Amiright hstewart?

HStewart - Tuesday, June 18, 2019 - link

You guess is a good as mine. But I believe the previous articles stated Intel is going 5 Only PCI 4 is skip

Arsenica - Wednesday, June 19, 2019 - link

Cascade lake in LGA4189 will feature PCIe 4.0

Santoval - Wednesday, June 19, 2019 - link

No it won't. Intel will debut PCIe 4.0 with Ice Lake Xeon CPUs, probably not with Ice Lake-S/H CPUs for desktop (which I don't think will ever be released; they will probably can that release and launch Tiger Lake CPUs for desktop directly) and probably the upcoming Ice Lake-U/Y CPUs for laptops and convertibles will not have PCIe 4.0 either.
Even Cooper Lake, the 14nm node based successor of Cascade Lake, will lack PCIe 4.0

halcyon - Wednesday, June 19, 2019 - link

Source for that?

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I confused Cascade Lake with Ice lake. Ice lake in LGA4189 will have PCIe 4.0

Korguz - Thursday, June 20, 2019 - link

Arsenica im confused with ALL the " Llake named " cpus... can never tell which is which, which it out, coming out, or future chips... is there no one at intel that has the power to change the names of the chips ? or is it a tactic to confuse people ??? geeze... as if the WAY TO MANY cpu sku's isnt bad enough.... one of the local stores here, desktop only.. has approx 22 cpu's listed !!!!!!!!

Targon - Thursday, June 20, 2019 - link

Intel loves to confuse consumers. Dual-core i7 laptops, which chips are dual core, quad core, hex core? Why charge extra for HyperThreading at this point, outside of the low end i3 vs. i5?

mode_13h - Thursday, June 20, 2019 - link

Intel is now a company lead by its marketing department. Product naming and differentiation is how those people "add value".

mode_13h - Thursday, June 20, 2019 - link

BTW, I would add to your list the whole bronze/silver/gold/platinum thing.

Anyway, at least there's (still) this: https://ark.intel.com/content/www/us/en/ark.html

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