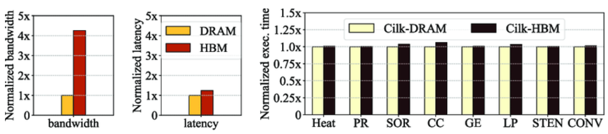
Fig 4 - uploaded by Yuxian Qiu



(a) Bandwidth (b) Latency (c) Performance

Bandwidth and latency of DRAM and HBM, and the impact of latency on application performance.

Source publication

+1

Bandwidth and Locality Aware Task-stealing for Manycore Architectures with Bandwidth-Asymmetric Memory

Article Full-text available

Dec 2018

Han Zhao · Quan Chen · Yuxian Qiu · [...] · Minyi Guo

Parallel computers now start to adopt Bandwidth-Asymmetric Memory architecture that consists of traditional DRAM memory and new High Bandwidth Memory (HBM) for high memory bandwidth. However, existing task schedulers suffer from low bandwidth usage and poor data locality problems in bandwidth-asymmetric memory architectures. To solve the two proble...

Contexts in source publication

Context 1

... 4(a) and 4(b) show the bandwidth and access latency of an HBM node normalized to the counterparts of a DRAM node measured with Intel MLC tool [1]. Observed from Figure 4, the bandwidth of an HBM node is 4.2× the bandwidth of a DRAM node, while the latency of an HBM node is 1.1× of the latency of a DRAM node. To show the impact of the slightly longer access latency of HBM nodes on application performance, we run all the benchmarks in Table 2 with one thread so that the required memory bandwidth is smaller than the bandwidth of a DRAM node. Figure 4(c) shows their performance in Cilk-DRAM and Cilk-HBM that store data in a DRAM node and an HBM node, respectively. ...

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Context 2

... show the impact of the slightly longer access latency of HBM nodes on application performance, we run all the benchmarks in Table 2 with one thread so that the required memory bandwidth is smaller than the bandwidth of a DRAM node. Figure 4(c) shows their performance in Cilk-DRAM and Cilk-HBM that store data in a DRAM node and an HBM node, respectively. Observed from Figure 4(c), except CC, the slightly longer latency of HBM nodes does not degrade application performance. ...

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Context 3

... show the impact of the slightly longer access latency of HBM nodes on application performance, we run all the benchmarks in Table 2 with one thread so that the required memory bandwidth is smaller than the bandwidth of a DRAM node. Figure 4(c) shows their performance in Cilk-DRAM and Cilk-HBM that store data in a DRAM node and an HBM node, respectively. Observed from Figure 4(c), except CC, the slightly longer latency of HBM nodes does not degrade application performance. This finding is consistent with the observation in prior work [35]. ...

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Context 4

... 4(a) and 4(b) show the bandwidth and access latency of an HBM node normalized to the counterparts of a DRAM node measured with Intel MLC tool [1]. Observed from Figure 4, the bandwidth of an HBM node is 4.2× the bandwidth of a DRAM node, while the latency of an HBM node is 1.1× of the latency of a DRAM node. To show the impact of the slightly longer access latency of HBM nodes on application performance, we run all the benchmarks in Table 2 with one thread so that the required memory bandwidth is smaller than the bandwidth of a DRAM node. Figure 4(c) shows their performance in Cilk-DRAM and Cilk-HBM that store data in a DRAM node and an HBM node, respectively. ...

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Context 5

... show the impact of the slightly longer access latency of HBM nodes on application performance, we run all the benchmarks in Table 2 with one thread so that the required memory bandwidth is smaller than the bandwidth of a DRAM node. Figure 4(c) shows their performance in Cilk-DRAM and Cilk-HBM that store data in a DRAM node and an HBM node, respectively. Observed from Figure 4(c), except CC, the slightly longer latency of HBM nodes does not degrade application performance. ...

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Context 6

... show the impact of the slightly longer access latency of HBM nodes on application performance, we run all the benchmarks in Table 2 with one thread so that the required memory bandwidth is smaller than the bandwidth of a DRAM node. Figure 4(c) shows their performance in Cilk-DRAM and Cilk-HBM that store data in a DRAM node and an HBM node, respectively. Observed from Figure 4(c), except CC, the slightly longer latency of HBM nodes does not degrade application performance. This finding is consis- tent with the observation in prior work [35]. ...

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... Barghi et al. [35] designed a locality-aware work stealing based on the actor model and NUMA architectures. Many other methods [36]- [44] also have tackled NUMA-aware work stealing by increasing local data access to mitigate NUMA effects on remote task stealing. Instead of creating tasks beforehand, cooperative stealing [45], [46] utilizes the message-passingbased approach where victims create tasks only when the worker sends a stealing request, in order to avoid overhead caused by concurrent deques. ...

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... Some approaches use the structure of iterative applications to improve data locality [10,11,19,21, 35] . ADWS is di erent from these approaches because the application of ADWS is not limited to iterative applications. ...

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