

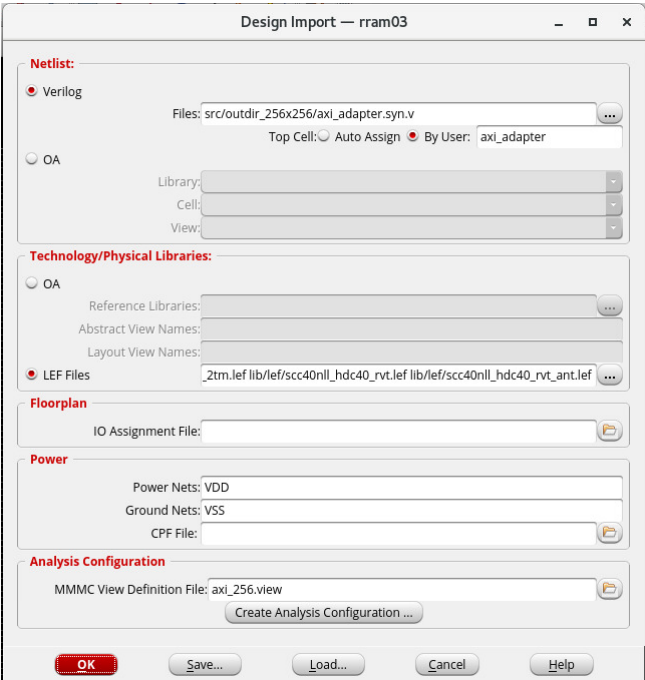
# 总结

单位: um²	AXI_32x32	AXI_128x128	AXI_256x256	AXI_512x512	rram_top
综合面积	1701.97	3792.10	6611.48	12349.64	97073.40
后端面积	2440.75	5422.14	9452.85	17651.29	138021.20
density	0.72726	0.72006	0.72268	0.73423	0.80775

报告地址: /data/SHARE/LJ/Area\_assessment

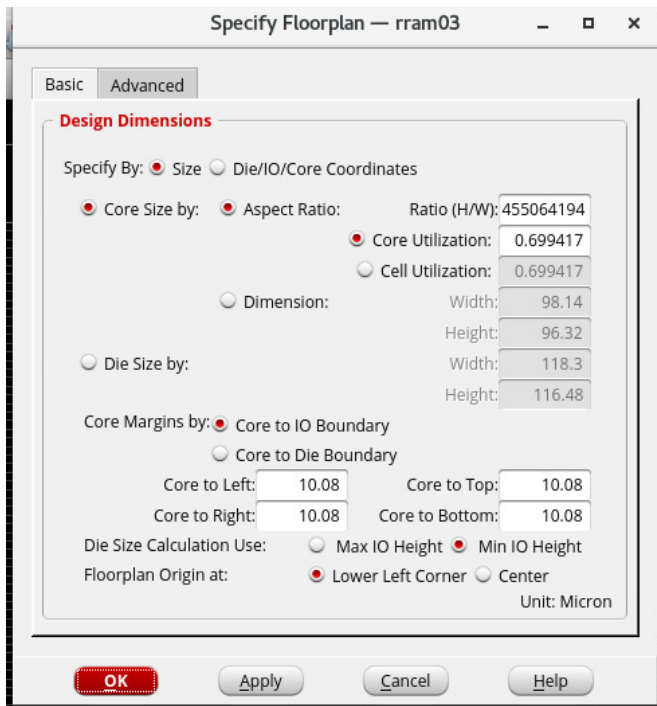
# 具体设置

## init\_design



## init\_floorplan

rram\_top 根据综合面积的 1.5 倍手动设置, AXI 使用自动生成的值  
ratio: 0.9 utilization: 0.7



The image shows a 'Specify Floorplan' dialog box for a component named 'rram03'. The dialog has two tabs: 'Basic' and 'Advanced'. The 'Basic' tab is selected. Under the 'Design Dimensions' section, the 'Specify By' options are 'Size' (selected) and 'Die/IO/Core Coordinates'. The 'Core Size by' options are 'Aspect Ratio' (selected) and 'Dimension'. The 'Aspect Ratio' is set to 455064194. The 'Core Utilization' is set to 0.699417. The 'Cell Utilization' is set to 0.699417. The 'Die Size by' options are 'Width' and 'Height', with values 98.14 and 96.32 respectively. The 'Die Size by' options are 'Width' and 'Height', with values 118.3 and 116.48 respectively. The 'Core Margins by' options are 'Core to IO Boundary' (selected) and 'Core to Die Boundary'. The 'Core to IO Boundary' options are 'Core to Left' (10.08), 'Core to Top' (10.08), 'Core to Right' (10.08), and 'Core to Bottom' (10.08). The 'Die Size Calculation Use' options are 'Max IO Height' and 'Min IO Height' (selected). The 'Floorplan Origin at' options are 'Lower Left Corner' (selected) and 'Center'. The 'Unit' is set to 'Micron'. The dialog has 'OK', 'Apply', 'Cancel', and 'Help' buttons at the bottom.

Specify Floorplan — rram03

Basic Advanced

**Design Dimensions**

Specify By: ☒ Size ☐ Die/IO/Core Coordinates

☒ Core Size by: ☒ Aspect Ratio: Ratio (H/W): 455064194

☒ Core Utilization: 0.699417

☐ Cell Utilization: 0.699417

☐ Dimension: Width: 98.14 Height: 96.32

☐ Die Size by: Width: 118.3 Height: 116.48

Core Margins by: ☒ Core to IO Boundary

☐ Core to Die Boundary

Core to Left: 10.08 Core to Top: 10.08

Core to Right: 10.08 Core to Bottom: 10.08

Die Size Calculation Use: ☐ Max IO Height ☒ Min IO Height

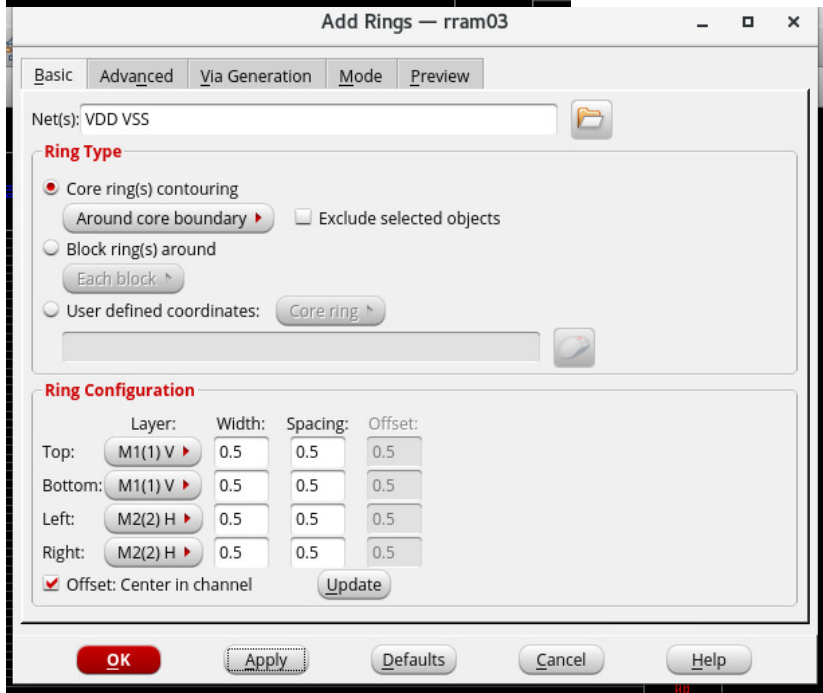
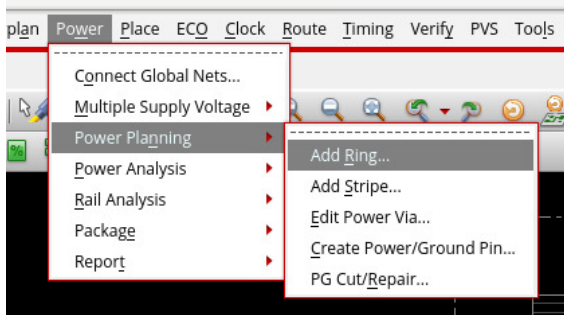
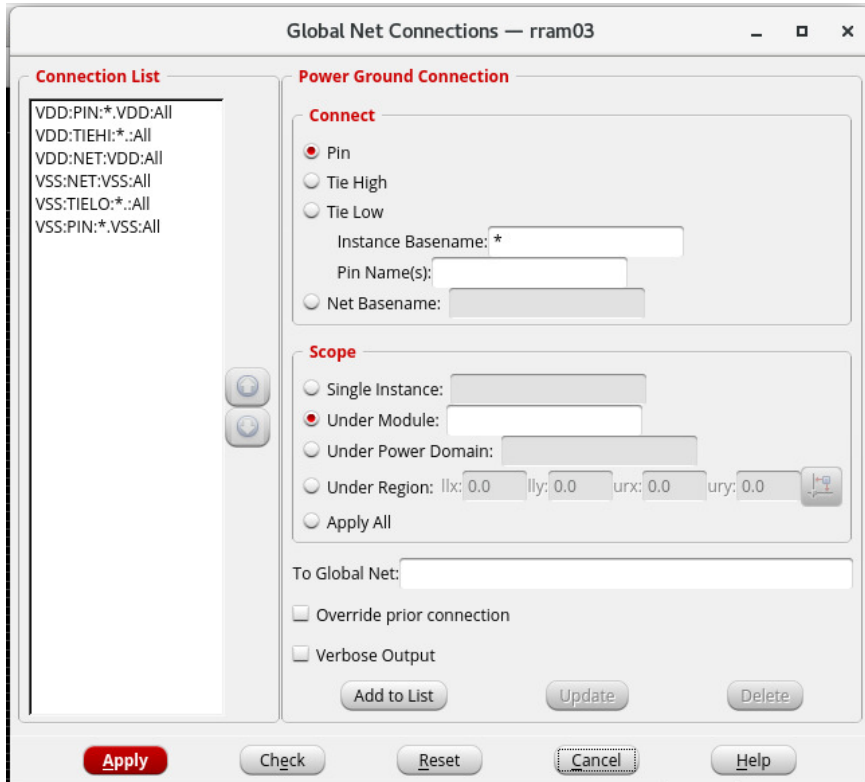
Floorplan Origin at: ☒ Lower Left Corner ☐ Center

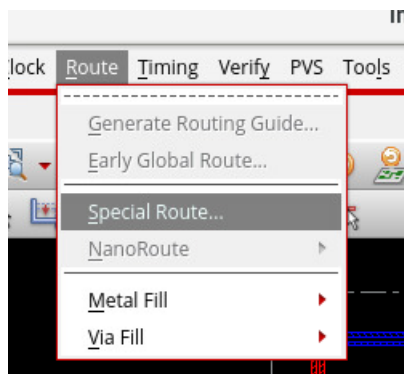
Unit: Micron

OK Apply Cancel Help

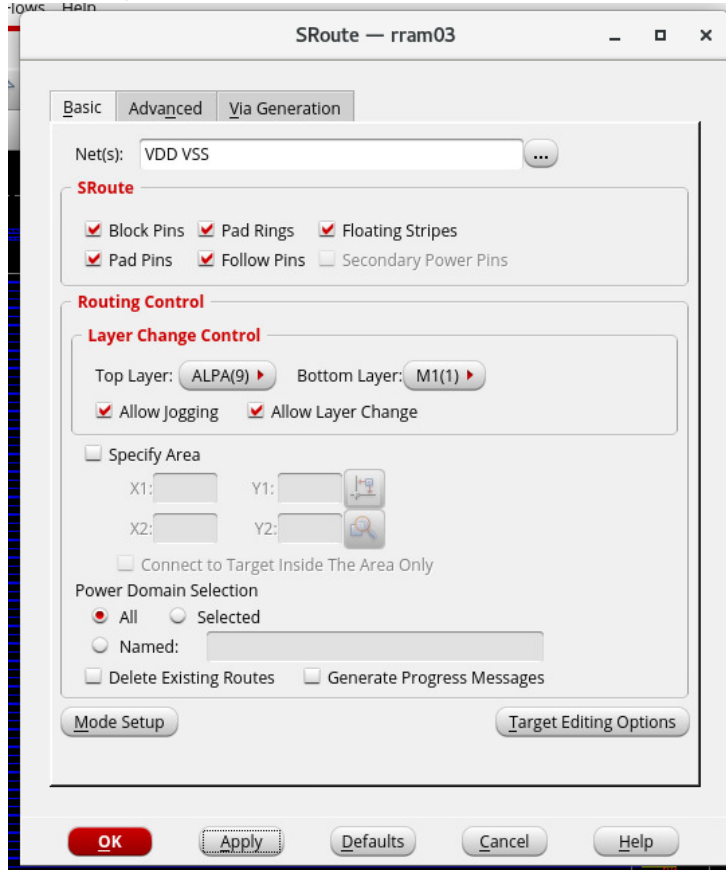
**power+route**

power -> connect global nets





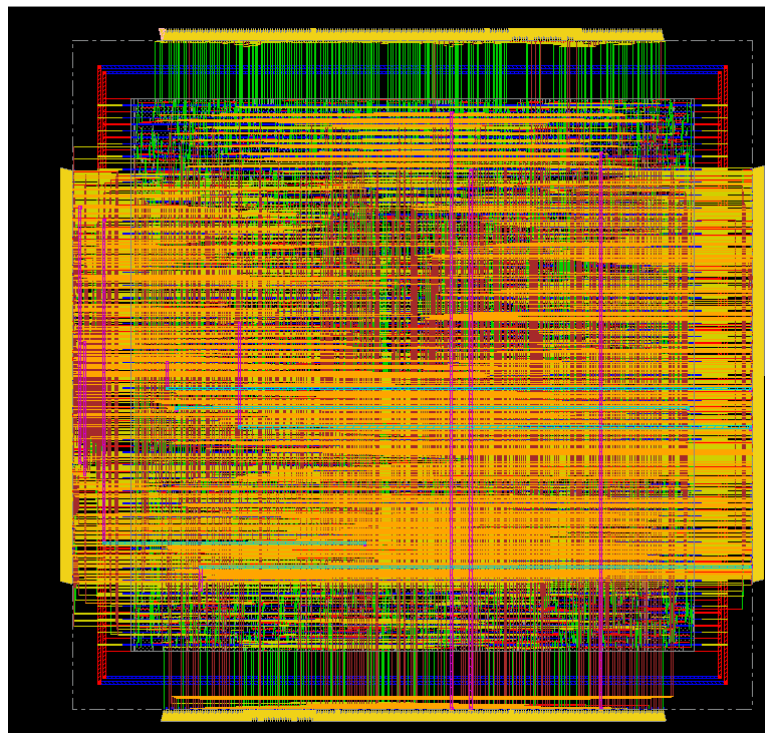
route -> special route



source init.tcl  
source power.Tcl  
(潘泽伦的 tcl)

## PIN

手动排 pin  
clk 改信号类型  
source placement.Tcl



## 报告生成

### summaryreport

```
innovus 4> summaryreport
Start to collect the design information.
Build netlist information for Cell axi_adapter.
Finished collecting the design information.
Generating standard cells used in the design report.
Analyze library ...
Analyze netlist ...
Generating HFO information report.
Generate no-driven nets information report.
Analyze timing ...
Analyze floorplan/placement ...
Analysis Routing ...
Report saved in file summaryReport/axi_adapter.main.htm.ascii
```