

总结

单位: um²	AXI_32x32	AXI_128x128	AXI_256x256	AXI_512x512	rram_top
综合面积	1701.97	3792.10	6611.48	12349.64	97073.40
后端面积	2440.75	5422.14	9452.85	17651.29	138021.20
density	0.72726	0.72006	0.72268	0.73423	0.80775

报告地址: /data/SHARE/LJ/Area_assessment

具体设置

init_design

Design Import — rram03

Netlist:

☒ Verilog

Files:

src/outdir_256x256/axi_adapter.syn.v

...

Top Cell:

☐ Auto Assign

☒ By User:

axi_adapter

☐ OA

Library:

Cell:

View:

Technology/Physical Libraries:

☐ OA

Reference Libraries:

Abstract View Names:

Layout View Names:

☒ LEF Files

_2tm.lef lib/lef/scc40nll_hdc40_rvt.lef lib/lef/scc40nll_hdc40_rvt_ant.lef

...

Floorplan

IO Assignment File:

Power

Power Nets:

VDD

Ground Nets:

VSS

CPF File:

Analysis Configuration

MMMC View Definition File:

axi_256.view

Create Analysis Configuration ...

OK

Save...

Load...

Cancel

Help

init_floorplan

rram_top 根据综合面积的 1.5 倍手动设置, AXI 使用自动生成的值
ratio: 0.9 utilization: 0.7

Specify Floorplan — rram03

Basic Advanced

Design Dimensions

Specify By: ☒ Size ☐ Die/IO/Core Coordinates

☒ Core Size by: ☒ Aspect Ratio: Ratio (H/W): 455064194

☒ Core Utilization: 0.699417

☐ Cell Utilization: 0.699417

☐ Dimension: Width: 98.14

Height: 96.32

☐ Die Size by: Width: 118.3

Height: 116.48

Core Margins by: ☒ Core to IO Boundary

☐ Core to Die Boundary

Core to Left: 10.08 Core to Top: 10.08

Core to Right: 10.08 Core to Bottom: 10.08

Die Size Calculation Use: ☐ Max IO Height ☒ Min IO Height

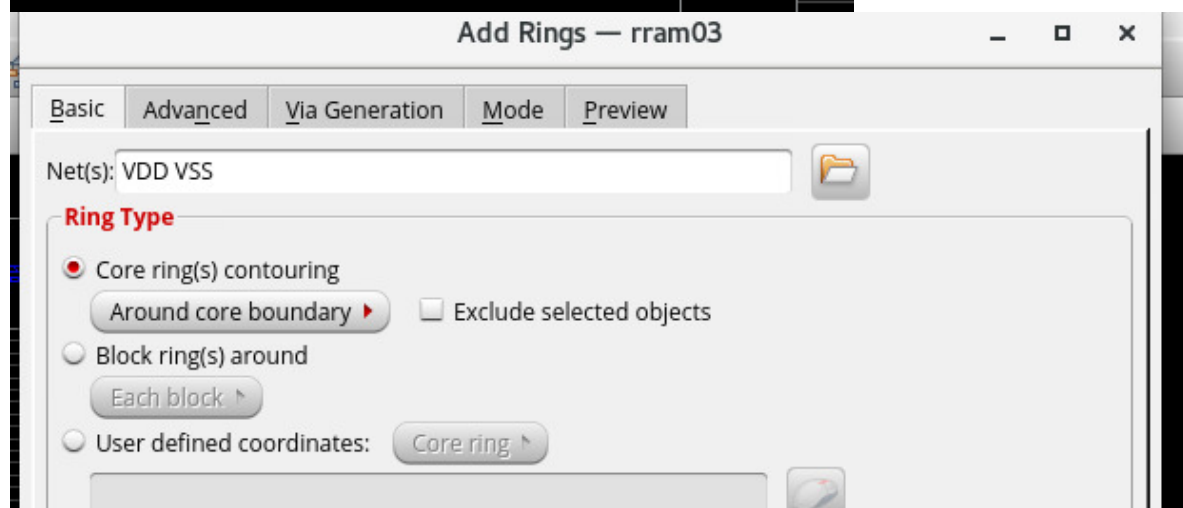
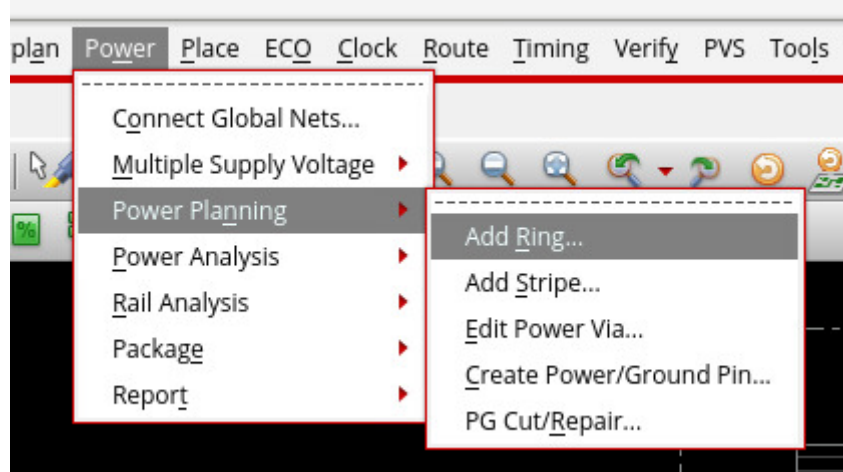
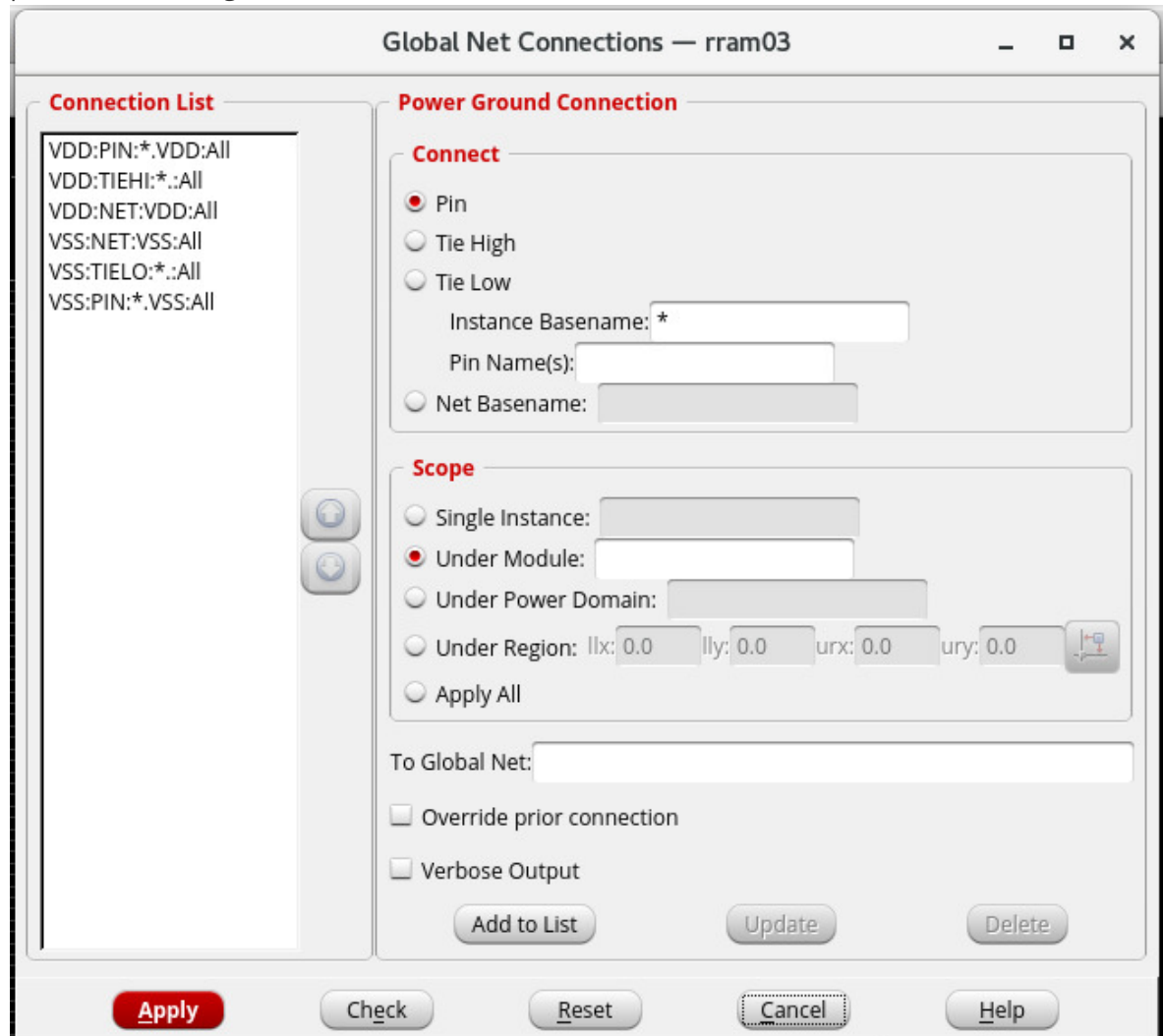
Floorplan Origin at: ☒ Lower Left Corner ☐ Center

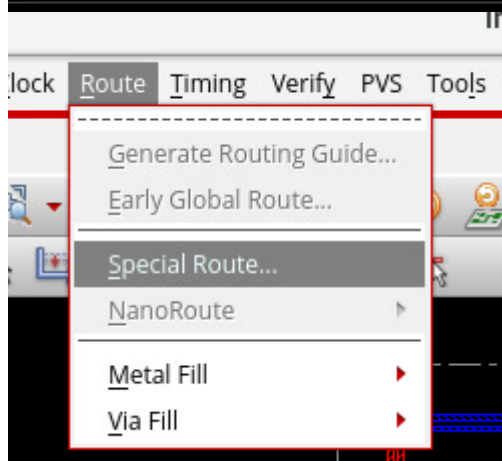
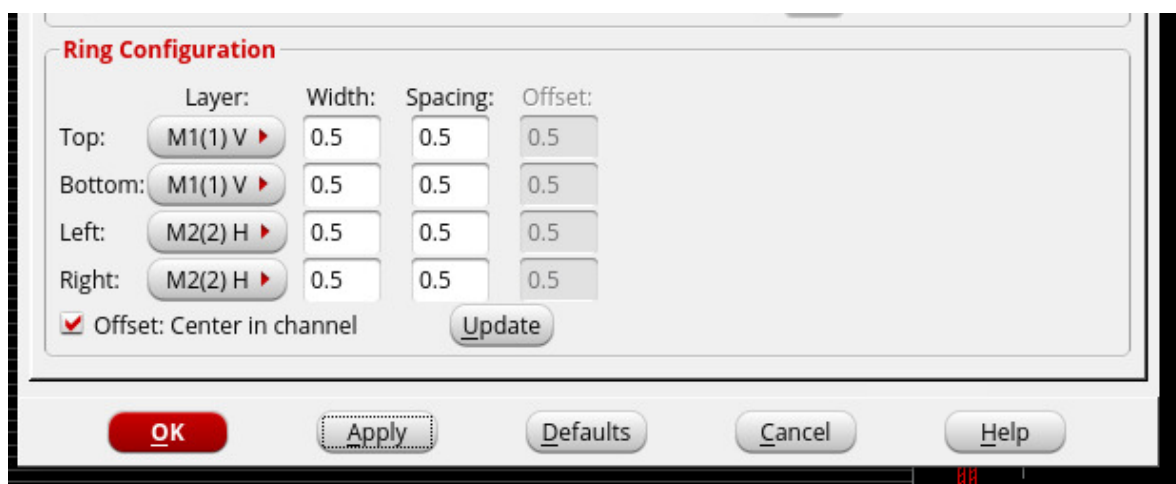
Unit: Micron

OK Apply Cancel Help

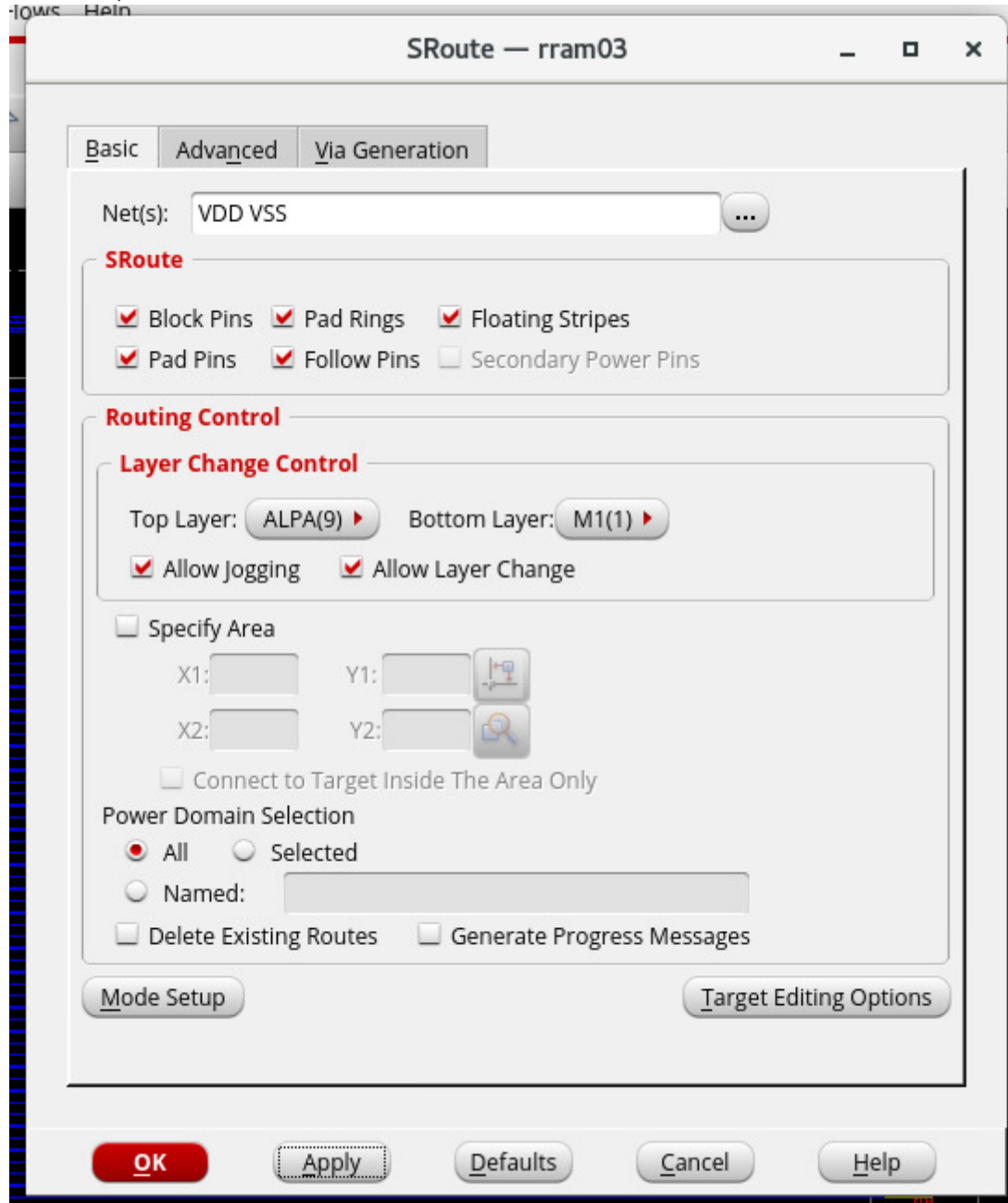
power+route

power -> connect global nets





route -> special route



source init.tcl

source power.Tcl

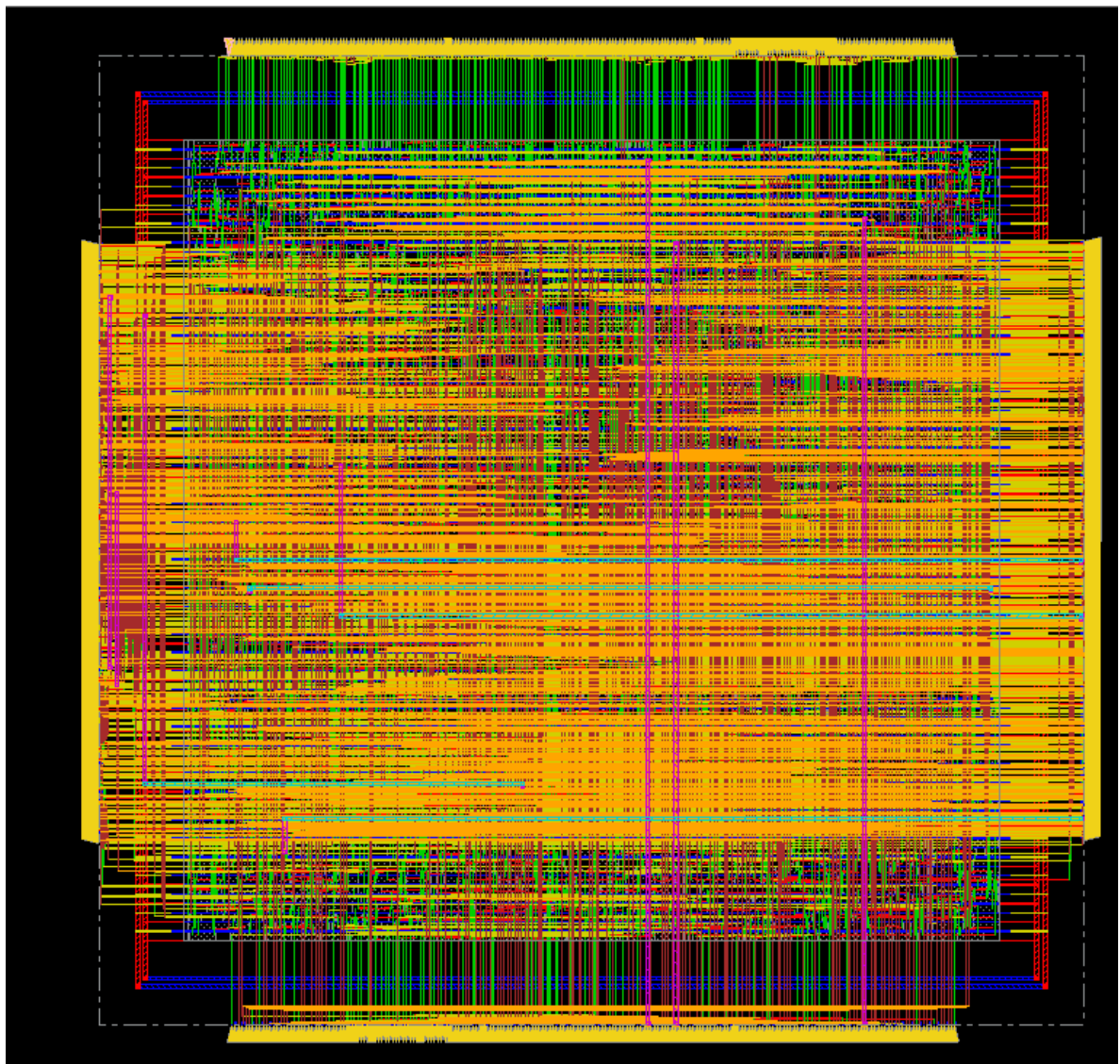
(潘泽伦的 tcl)

PIN

手动排 pin

clk 改信号类型

source placement.Tcl



报告生成

summaryreport

```
innovus 4> summaryreport
Start to collect the design information.
Build netlist information for Cell axi_adapter.
Finished collecting the design information.
Generating standard cells used in the design report.
Analyze library ...
Analyze netlist ...
Generating HFO information report.
Generate no-driven nets information report.
Analyze timing ...
Analyze floorplan/placement ...
Analysis Routing ...
Report saved in file summaryReport/axi_adapter.main.htm.ascii
```