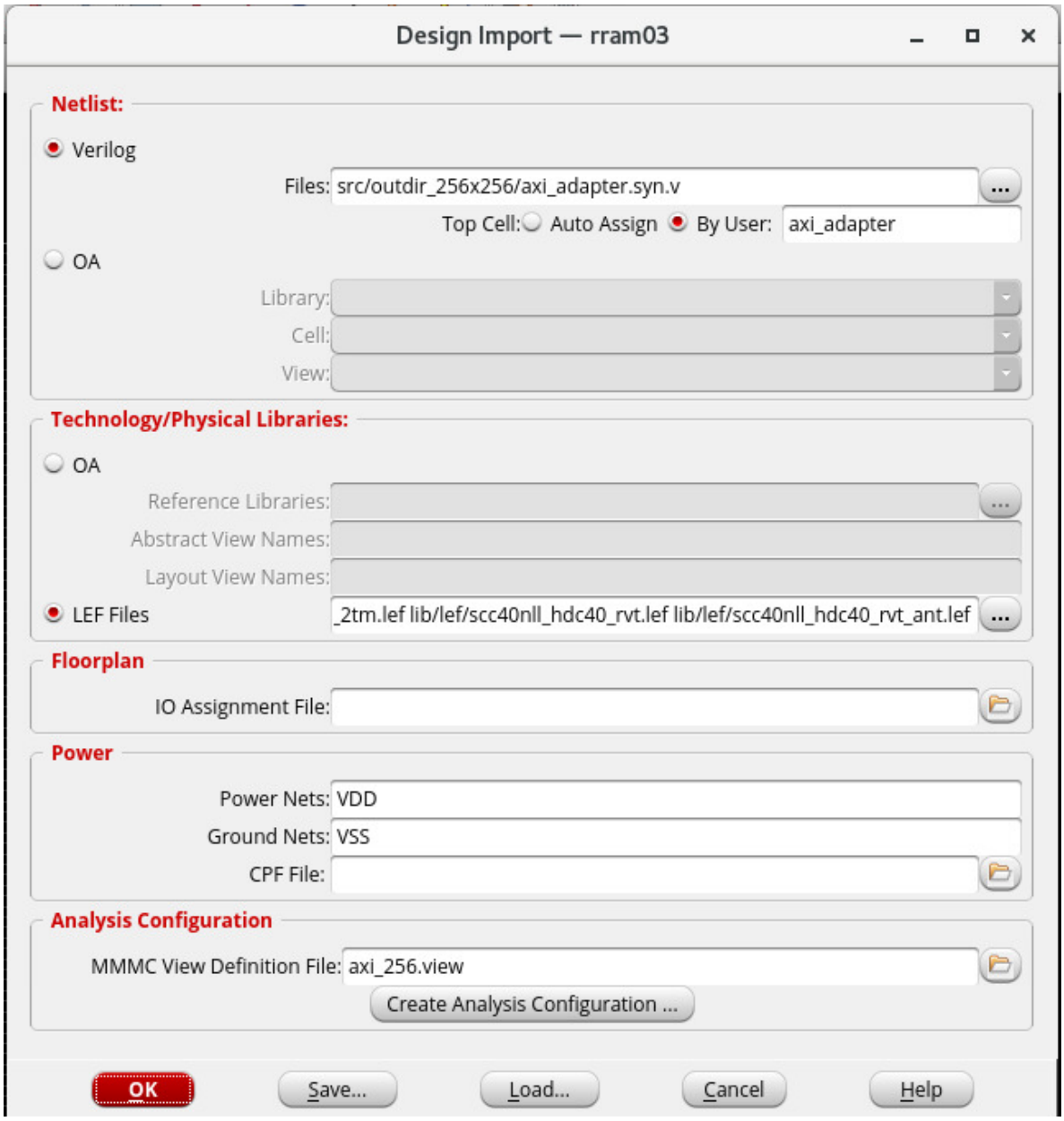
总结

单位：um²	AXI_32x32	AXI_128x128	AXI_256x256	AXI_512x512	rram_top
综合面积	1701.97	3792.10	6611.48	12349.64	97073.40
后端面积	2440.75	5422.14	9452.85	17651.29	138021.20
density	0.72726	0.72006	0.72268	0.73423	0.80775

报告地址：/data/SHARE/LJ/Area_assessment

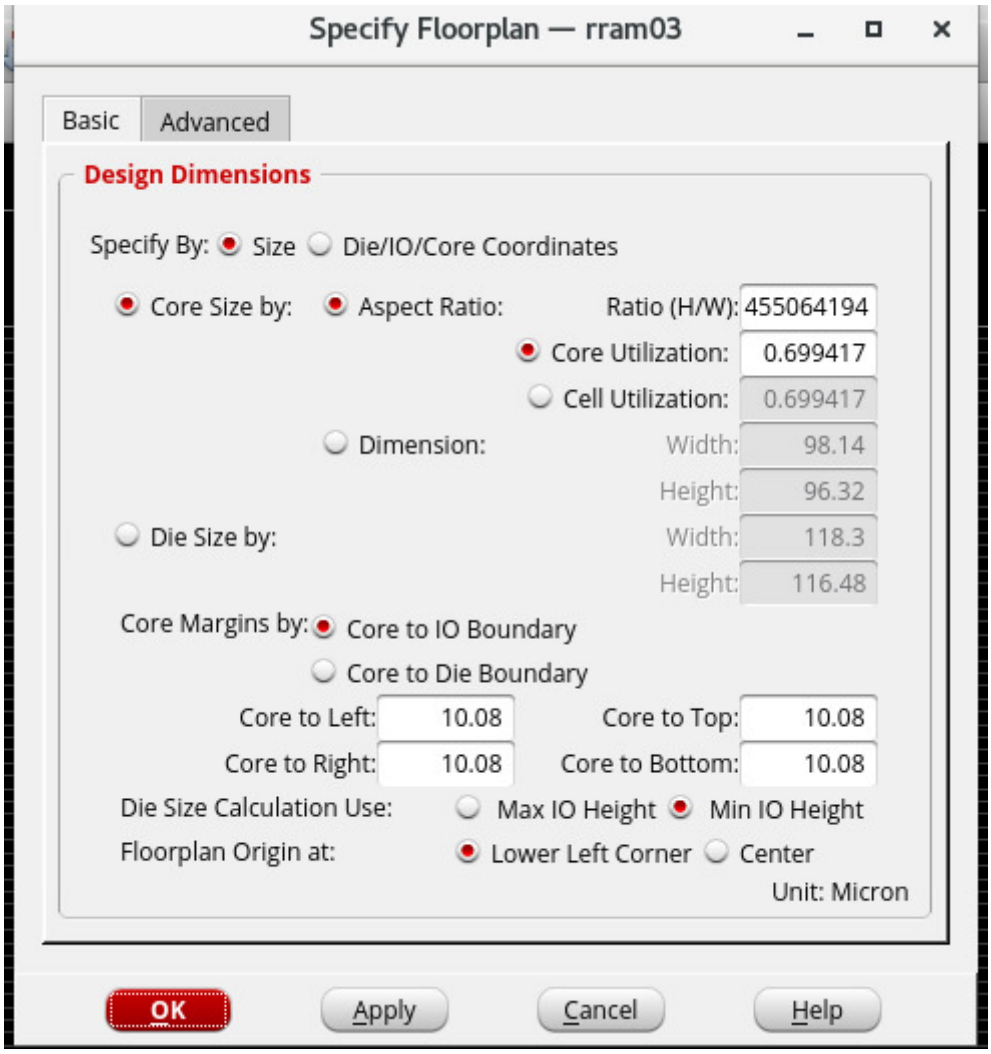
具体设置

init_design



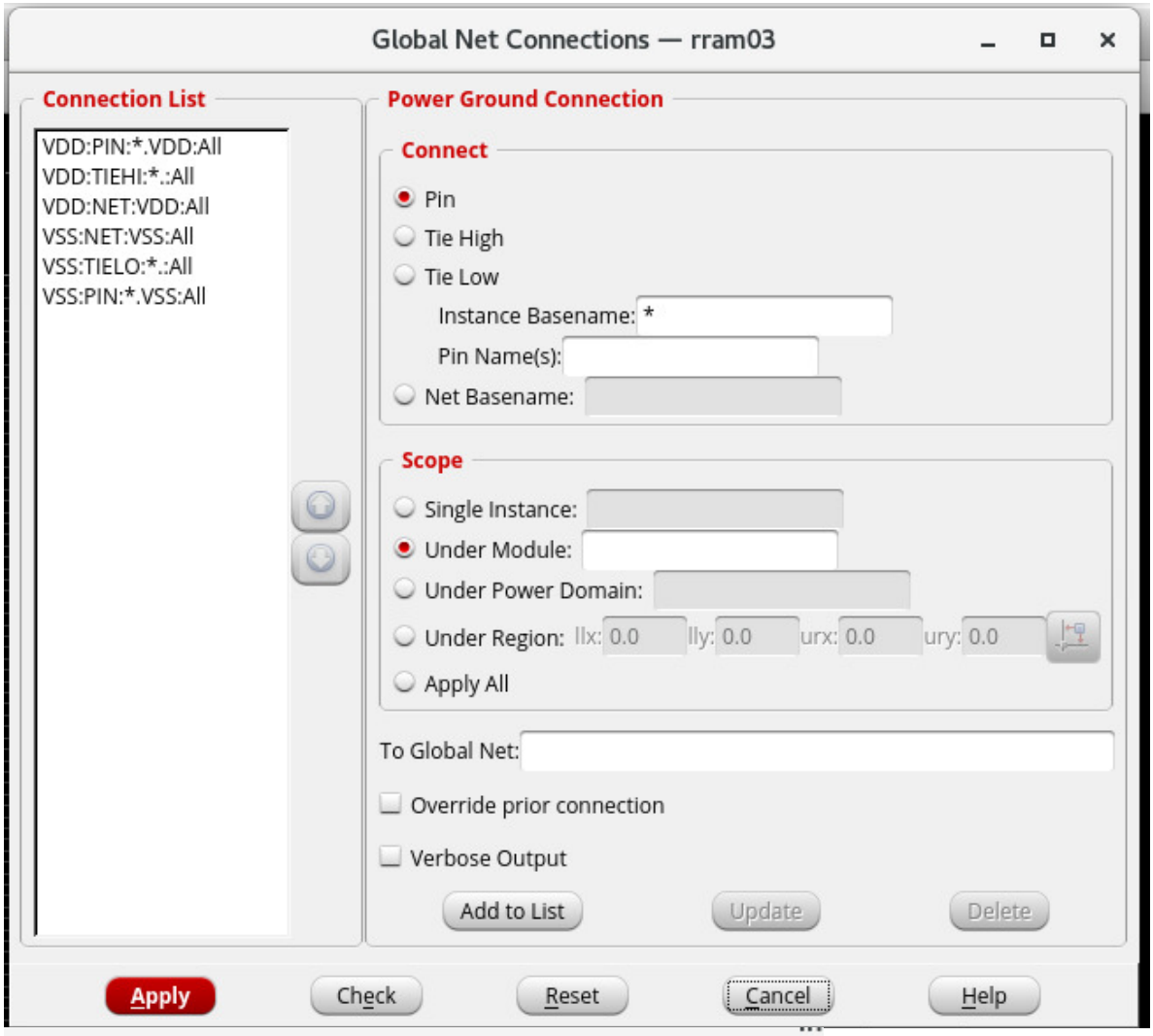
init_floorplan

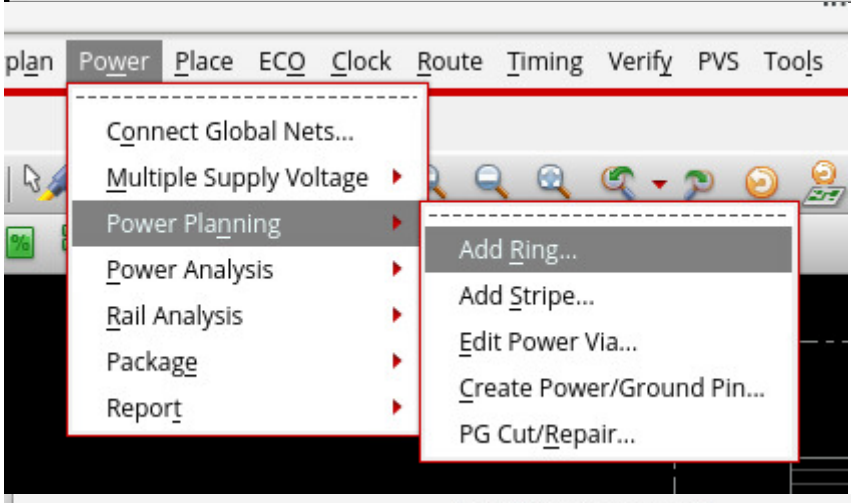
rram_top 根据综合面积的 1.5 倍手动设置，AXI 使用自动生成的值
ratio：0.9 utilization：0.7

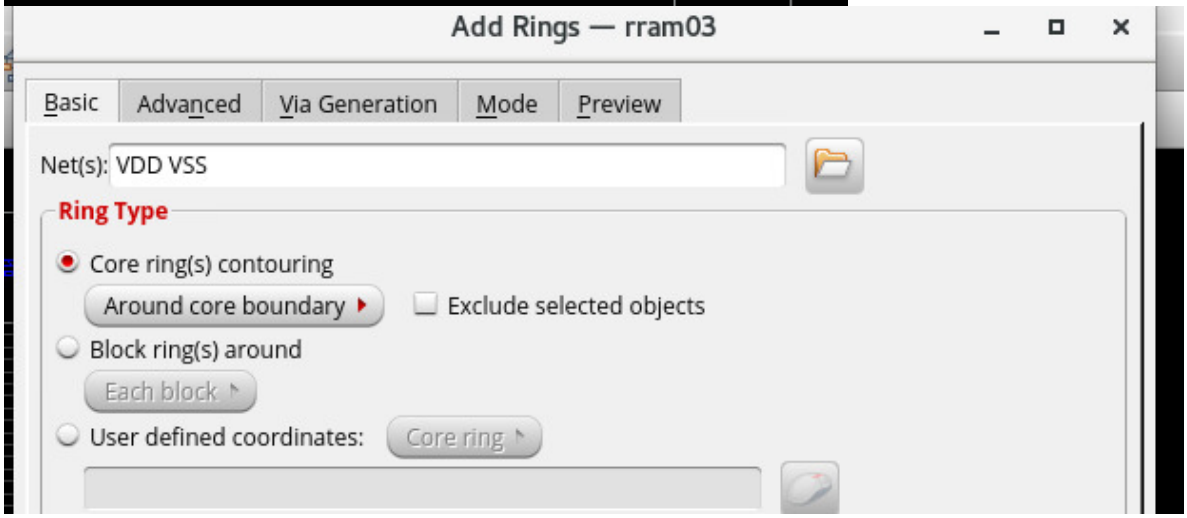


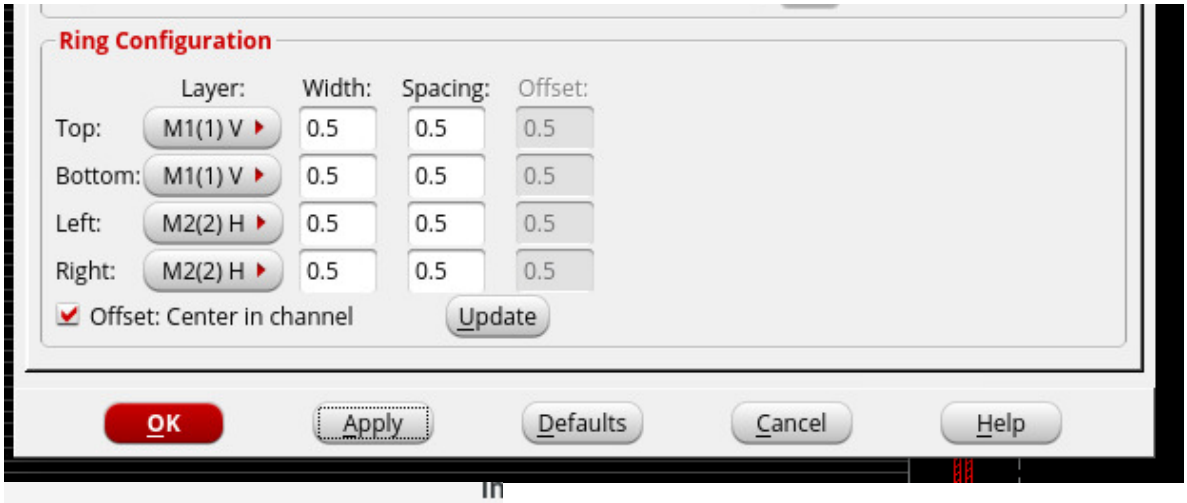
power+route

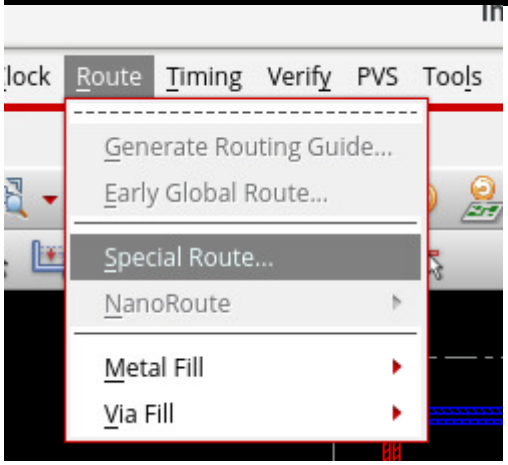
power -> connect global nets



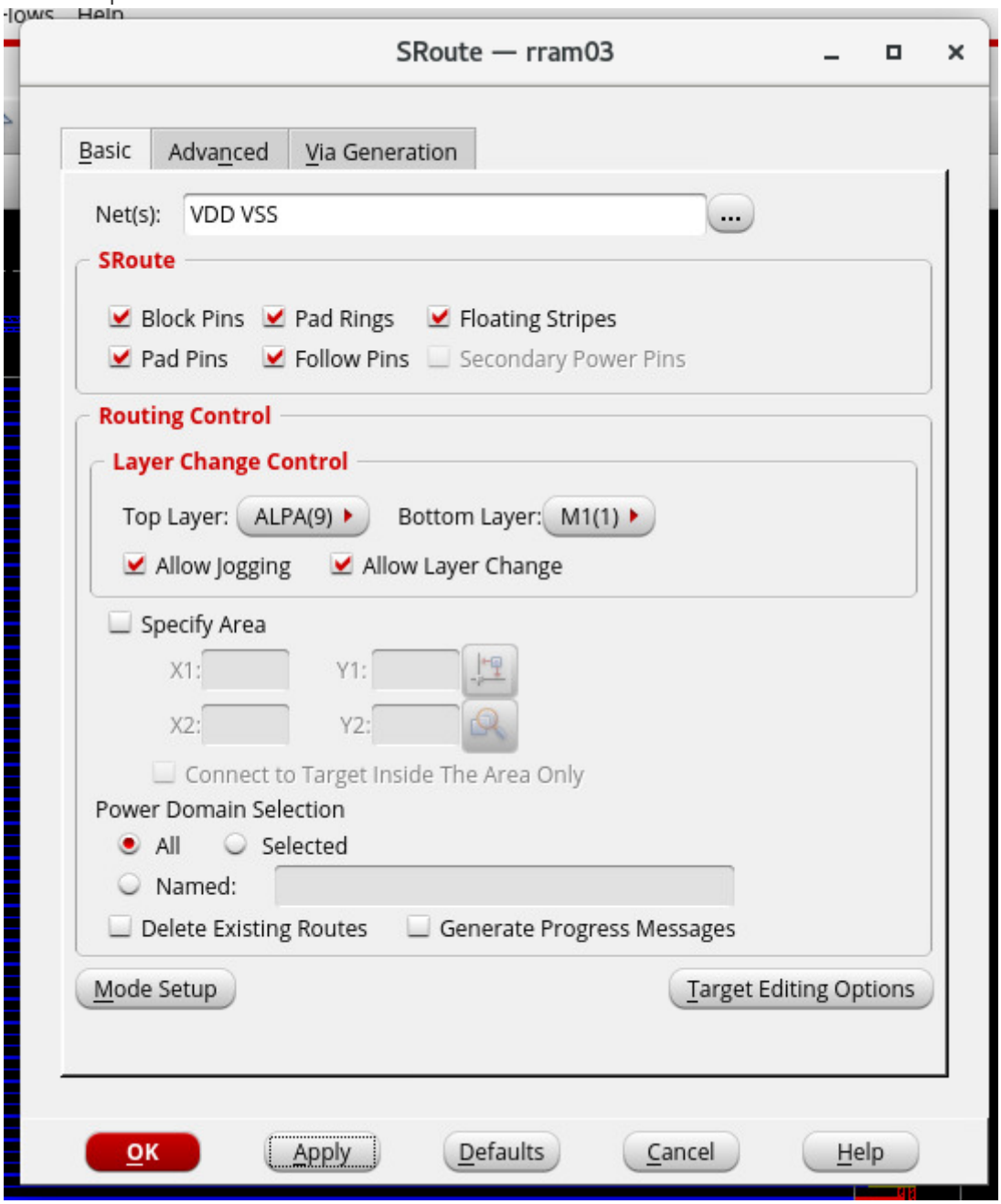





Ring Configuration
Layer:
Width:
Spacing:
Offset:
Top:
M1(1) V
0.5
0.5
0.5
Bottom:
M1(1) V
0.5
0.5
0.5
Left:
M2(2) H
0.5
0.5
0.5
Right:
M2(2) H
0.5
0.5
0.5
Offset: Center in channel
Update
OK
Apply
Defaults
Cancel
Help


lock
Route
Timing
Verify
PVS
Tools
Generate Routing Guide...
Early Global Route...
Special Route...
NanoRoute
Metal Fill
Via Fill

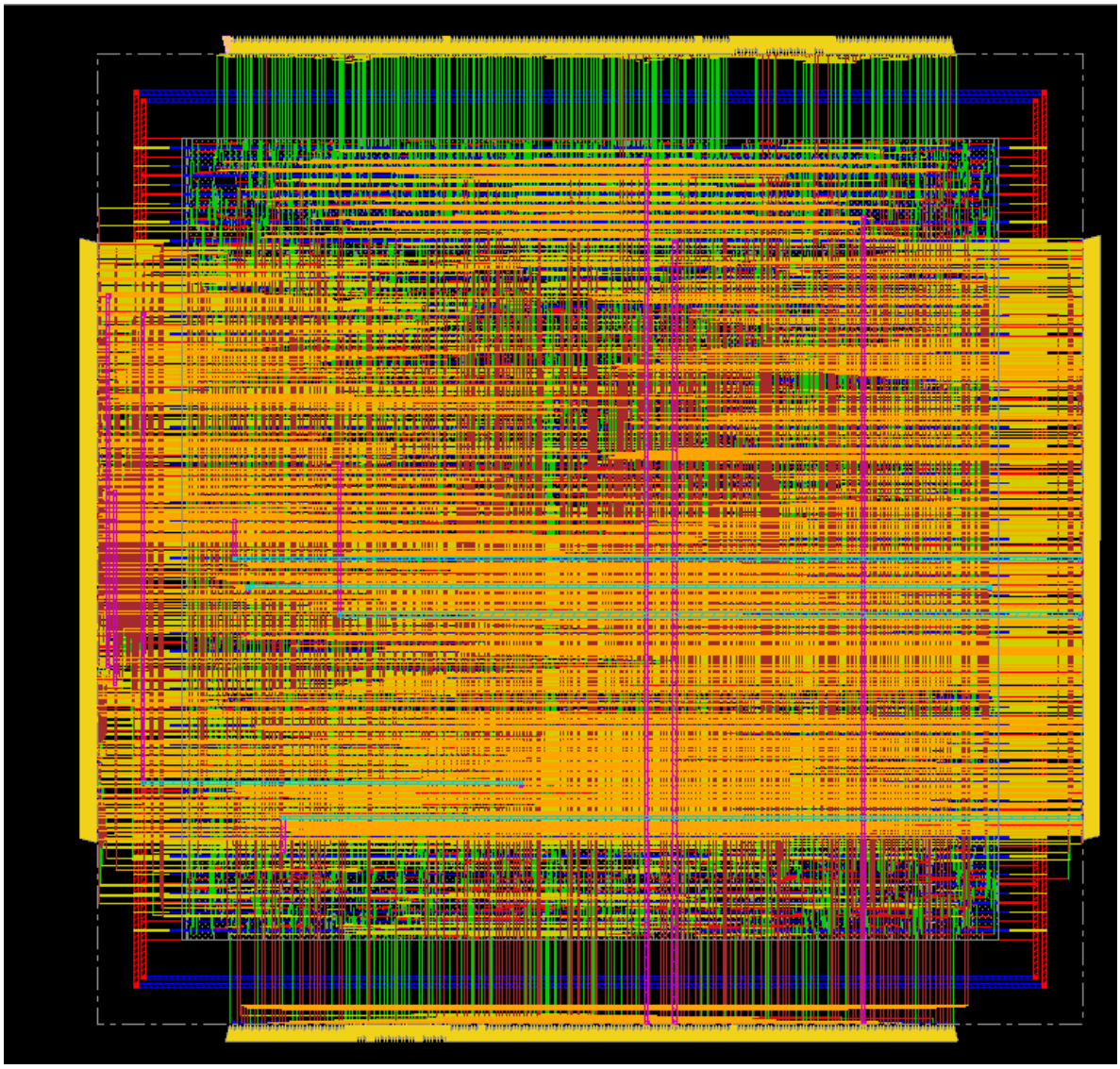
route -> special route



source init.tcl
source power.Tcl
（潘泽伦的 tcl）

PIN

手动排 pin
clk 改信号类型
source placement.Tcl



报告生成

summaryreport

```
innovus 4> summaryreport
Start to collect the design information.
Build netlist information for Cell axi_adapter.
Finished collecting the design information.
Generating standard cells used in the design report.
Analyze library ...
Analyze netlist ...
Generating HFO information report.
Generate no-driven nets information report.
Analyze timing ...
Analyze floorplan/placement ...
Analysis Routing ...
Report saved in file summaryReport/axi_adapter.main.htm.ascii
```