

**A HYBRID SYSTEM FOR FACE DETECTION
AND EMOTION RECOGNITION USING
VERILOG AND AI**

MINOR PROJECT REPORT



**PUNJAB ENGINEERING COLLEGE
(DEEMED TO BE UNIVERSITY)**

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December 2025

DECLARATION

We hereby declare that the project work titled "**A Hybrid system for Face Detection and Emotion Recognition Using Verilog and AI**" is an original record of the research and development carried out by us at **Punjab Engineering College (Deemed to be University), Chandigarh**. This work has been completed as part of the **Minor Project** for the degree of B.Tech. in Electronics Engineering (VLSI Design and Technology), under the mentorship and supervision of **Dr. Sukhwinder Singh** (Associate Professor), Department of Computer Science and Engineering.

We further affirm that the content, experiments, and results presented in this report are based on authentic sources and represent our efforts and understanding of the subject. The information included has been carefully verified. We also confirm that this project report has not been submitted, either wholly or partially, to this or any other institution or university for the award of any degree, diploma, or certificate.

Additionally, we ensure that the work adheres to the principles of academic integrity and ethical conduct. All data, analysis, and conclusions have been prepared responsibly and truthfully to the best of our knowledge.

We hereby certify that the above statement made by us is correct to the best of our knowledge and belief.

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CERTIFICATE

This is to certify that the project work titled “**A Hybrid system for Face Detection and Emotion Recognition Using Verilog and AI**” submitted by **Suryadipta Ghosh (23111002), Shashvat Mishra (23111023) and Pratyush Kumar(23111024)** in fulfilment of the requirements for the **Minor Project** offered by **Punjab Engineering College** (Deemed to be University), Chandigarh, during the academic year **2025–26**, is an original work carried out by the students under my supervision.

To the best of my knowledge all the work related to the project has been completed by the candidates themselves, and their approach towards the subject has been sincere and scientific.

Date: 12/12/2025

Dr. Sukhwinder Singh

Associate Professor

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ABSTRACT

Face detection and emotion recognition are essential components of modern intelligent vision systems, yet existing software-based solutions often struggle with high latency, limited real-time performance, and inconsistent accuracy under varying conditions. Pure hardware implementations, while fast, lack the adaptability and expressive power of AI models. These challenges highlight the need for a balanced approach that offers both computational efficiency and robust emotion classification.

To address this, the proposed work presents a **hybrid system** that combines a **Verilog-based face detection module** with an **AI-driven emotion recognition model**. The Verilog hardware module performs rapid early-stage processing and face localization through parallel operations, reducing the computational burden on the AI stage and ensuring real-time responsiveness. Once the face region is detected, a lightweight neural network classifier analyses the features to identify emotional states with improved reliability and generalization.

By integrating deterministic hardware processing with adaptive machine learning, the system delivers **faster detection, higher accuracy, and better resource efficiency** compared to conventional approaches. This hybrid architecture is suitable for **embedded vision, surveillance, and human–computer interaction**, where performance and precision are critical.

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CHAPTER 1: INTRODUCTION

Face detection and emotion recognition play an important role in modern intelligent systems, enabling efficient human–machine interaction across applications such as surveillance, healthcare monitoring, and smart interfaces. Traditional software-only systems often suffer from high latency and inconsistent performance under varying conditions, while purely hardware-based approaches lack the flexibility and learning capability needed for emotion classification.

To overcome these limitations, this project presents a **hybrid system** that integrates **Verilog-based hardware face detection** with a **deep-learning-based emotion recognition model**. The hardware stage uses the Viola–Jones principle along with Skin Colour Segmentation to rapidly identify facial regions, while the software stage employs the Mini-Xception model to classify emotions from the detected face. This combination ensures both real-time performance and high accuracy.

1.1 Motivation

Emotion-aware systems are increasingly demanded in sectors such as intelligent surveillance, driver monitoring, medical diagnostics, and human–robot interaction. These applications require fast and reliable face detection along with consistent emotion interpretation in real time. Software-only pipelines often fail to meet strict timing constraints, while hardware-only solutions cannot achieve the adaptability needed for emotion classification.

This motivates the development of a **hybrid system that combines**:

- The **speed, parallelism, and determinism** of Verilog-based hardware
- The **learning capability and classification accuracy** of AI models

By offloading initial detection to hardware and performing recognition through deep learning, the system achieves a balanced trade-off between performance, accuracy, and resource efficiency.

1.2 Problem Statement

Real-time emotion recognition is challenging due to several limitations:

- **High Computational Load:**
Software-based face and emotion detection requires heavy processing, making real-time performance difficult on standard or embedded devices.
- **Sensitivity to Real-World Conditions:**
Variations in lighting, occlusions, camera quality, and subtle facial expressions often lead to inconsistent or inaccurate emotion predictions.
- **Hardware-Only Limitations:**
Pure hardware implementations lack the flexibility and learning capability needed for accurate emotion classification.

1.3 Methodology

The project follows a two-stage hybrid workflow:

- **Hardware Face Detection (Verilog HDL)**
 - Implemented modules based on Viola–Jones and Skin Colour Segmentation
 - Simulated and verified hardware behaviour.
- **Emotion Recognition (Mini-Xception Model)**
 - Implemented in Python (TensorFlow/Keras)
 - Preprocessing: grayscale → 48×48 resize → normalization
 - Classified into seven emotions (Happy, Sad, Angry, Fear, Disgust, Surprise, Neutral)
- **Hybrid Integration**
 - Hardware provides the face region (ROI)
 - AI model performs emotion classification on the extracted face

CHAPTER 2: BACKGROUND

Face detection and emotion recognition form the foundation of many modern vision-based intelligent systems. They are widely used in surveillance, human-computer interaction, healthcare monitoring, driver assistance systems, and social robotics. However, building a system that can both detect faces reliably and classify emotions accurately in real-time remains a challenging problem. Variations in lighting, facial expression intensity, skin tones, background clutter, and hardware limitations significantly affect system performance. This chapter explores the key concepts, existing methods, and technological evolution that motivate the development of a hybrid hardware-software solution.

2.1 Challenges in Face Detection and Emotion Recognition

Developing a robust detection-recognition pipeline involves addressing multiple practical challenges:

- 1. Variability in Faces and Expressions:** Faces differ widely in shape, orientation, pose, and occlusion. Emotional expressions vary in intensity, leading to intra-class variations that complicate classification.
- 2. Real-Time Processing Requirements:** Software-only systems often require high computational resources, making them unsuitable for embedded applications that demand low latency and deterministic timing.
- 3. Sensitivity to Environmental Factors:** Changes in illumination, shadows, skin colour variations, and background noise can reduce detection reliability and affect emotion classification accuracy.
- 4. Hardware Limitations:** Traditional hardware-only designs, while fast due to parallelism, cannot adapt to nuanced tasks like emotion recognition that require learning-based models.

2.2 Classical Approaches to Face Detection

Classical face detection methods rely on handcrafted features and simple statistical models. The **Viola-Jones algorithm**, based on Haar features and a cascaded classifier, offers fast and low-cost detection suitable for real-time systems, though its performance drops under poor lighting or non-frontal poses. **Skin Colour Segmentation** identifies facial regions using colour thresholds in spaces like YCbCr or HSV, making it computationally lightweight but sensitive to illumination and skin tone variations. These methods are preferred for hardware implementation because they are deterministic, efficient, and highly parallelizable.

2.3 Learning-Based Emotion Recognition Approaches

Emotion recognition has evolved significantly with advancements in AI:

Traditional ML Methods:

Earlier models relied on handcrafted features such as LBP (Local Binary Patterns), HOG (Histogram of Oriented Gradients), and SVM classifiers, where features had to be manually designed rather than learned. Although these methods are simple, fast, and offer good interpretability, they struggle with real-world variability. Changes in lighting, pose, occlusions, and subtle facial expressions significantly reduce their accuracy, making them less reliable for complex, unconstrained emotion recognition tasks.

Deep Learning Models

Deep learning has become the dominant approach for facial emotion recognition due to its ability to automatically learn complex features directly from images. Unlike traditional methods that rely on manually designed descriptors, deep neural networks extract hierarchical patterns—ranging from simple edges to high-level emotional cues—making them far more robust in real-world conditions.

In this project, the **Mini-Xception** model is used as the primary CNN architecture for emotion classification. Mini-Xception is a simplified and highly efficient version of the Xception network, tailored for lightweight deployments without compromising performance.

Key Advantages of Mini-Xception:

- **Depthwise Separable Convolutions**

Mini-Xception replaces standard convolutions with depthwise separable ones, significantly reducing the number of operations required. This allows the model to process images quickly while still capturing important spatial features.

- **Compact Architecture for Real-Time Use**

With only around **60,000 parameters**, the model is extremely small compared to typical CNNs. Its low memory footprint enables real-time inference even on resource-constrained devices and makes it suitable for integration with FPGA-based hardware systems.

- **Good Generalization Across Datasets**

Despite its small size, Mini-Xception consistently performs well on widely used emotion recognition datasets, demonstrating strong generalization to variations in lighting, facial pose, and expression intensity. This reliability makes it well-suited for practical applications where conditions are not controlled.

2.4 Hybrid Hardware–AI Systems

Hybrid systems combine the strengths of FPGA hardware and deep learning models to achieve real-time, accurate emotion recognition.

- **Hardware for Fast Detection:**
FPGA/Verilog modules perform rapid, parallel face detection (similar to the paper’s hardware-accelerated preprocessing), ensuring low latency and consistent performance.
- **AI for Accurate Classification:**
Deep learning models such as Mini-Xception or the paper’s **CLDNN (CNN + LSTM + DNN)** provide high accuracy and adaptability to lighting, pose, and expression variations.
- **Balanced Hybrid Design:**
By letting hardware handle detection and AI handle emotion classification, the system achieves the **speed of FPGA processing** and the **intelligence of neural networks**, overcoming the limitations of using only hardware or only software.

2.5 Motivation for the Proposed Approach

A reliable emotion-recognition system must:

1. Detect faces accurately under varying pose, lighting, and background conditions.
2. Capture subtle and time-varying emotional expressions.
3. Run in real time on resource-constrained or embedded hardware.

The motivation for the proposed hybrid approach comes from the research paper’s findings that:

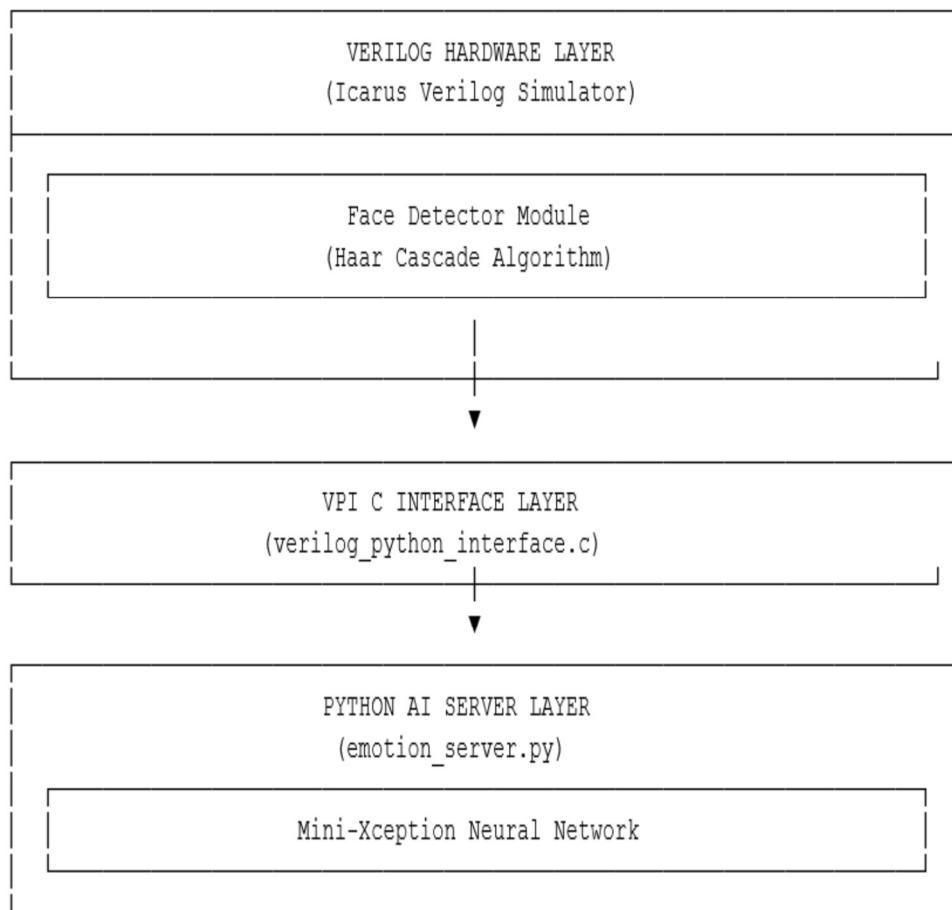
- **Hardware-accelerated face preprocessing** (as done in our Verilog Viola–Jones + Skin Segmentation pipeline) ensures **fast, low-latency face localization**, similar to the FPGA optimizations used in the paper.
- **Deep learning models such as Mini-Xception** provide **high accuracy and robustness**, especially for sequential emotions and real-world variations.
- **A hybrid hardware–AI pipeline**, where FPGA handles detection and the deep model handles classification, offers the best balance of **speed, accuracy, and efficiency**, enabling real-time performance on limited hardware.

CHAPTER 3: PROPOSED WORK- HYBRID FACE DETECTION AND EMOTION RECOGNITION SYSTEM

The proposed system integrates a fast Verilog-based face detection pipeline with a deep-learning-based emotion recognition model to achieve real-time and accurate performance. The design is divided into two main stages: **Stage 1 – Hardware Face Detection**, and **Stage 2 – AI Emotion Classification**. This hybrid architecture ensures that computationally heavy tasks are distributed efficiently, with hardware handling pixel-level detection and AI performing high-level emotion analysis. The following sections describe the system architecture and the role of each module.

The overall framework is shown below:

3.1 Overall System Architecture



System Architecture

3.2 Stage 1 — Hardware Face Detection Module

3.2.1 Viola–Jones-Based Detection in Verilog

The hardware detection unit uses simplified Viola–Jones principles such as Haar-like features and cascading stages to quickly eliminate non-face regions. The Haar feature value H for region R is computed as:

$$H = \sum_{(x,y) \in R_1} II(x, y) - \sum_{(x,y) \in R_2} II(x, y)$$

3.2.2 Skin Colour Segmentation

A Skin probability is calculated using thresholding in YCbCr space:

$$\text{Skin}(x, y) = \begin{cases} 1, & Cb_{\min} \leq Cb(x, y) \leq Cb_{\max} \text{ and } Cr_{\min} \leq Cr(x, y) \leq Cr_{\max} \\ 0, & \text{otherwise} \end{cases}$$

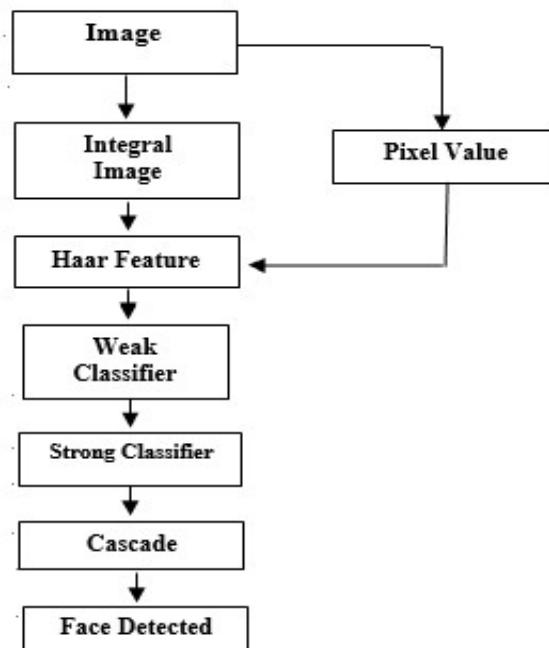
A binary mask is generated to refine the detected regions

3.2.3 Cascaded Classification Logic

The cascade structure is represented as:

$$C(I) = \prod_{i=1}^n f_i(I)$$

where f_i is the decision of the i^{th} stage.



Haar Cascade Face Detection Pipeline

3.1 Stage 2 — Emotion Classification Using Mini-Xception

3.1.1 Preprocessing Pipeline

The detected face ROI undergoes:

$$\begin{aligned}I_{\text{gray}} &= 0.299R + 0.587G + 0.114B \\I_{48 \times 48} &= \text{Resize}(I_{\text{gray}}) \\I_{\text{norm}} &= \frac{I_{48 \times 48}}{255}\end{aligned}$$

3.1.2 Mini-Xception Architecture

Mini-Xception uses depthwise separable convolutions:

$$Y = \text{Pointwise}(\text{Depthwise}(X))$$

which reduce computational cost while preserving expressiveness.

The model outputs a probability distribution:

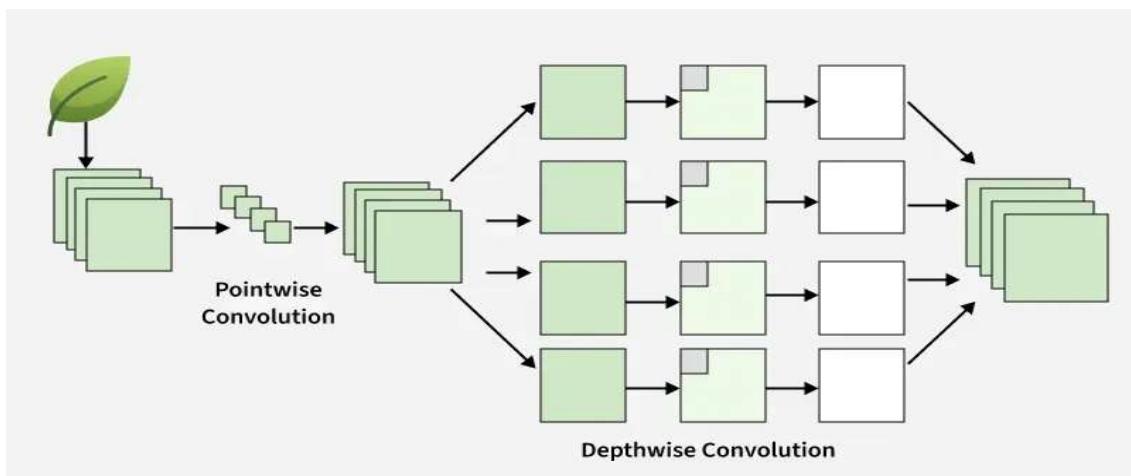
$$P(E_i | X) = \text{softmax}(z_i)$$

for $i \in \{1, \dots, 7\}$ corresponding to the emotions:

Happy, Sad, Angry, Fear, Disgust, Surprise, Neutral.

The predicted emotion is:

$$E_{\text{class}} = \arg \max_i P(E_i)$$



Depthwise–Pointwise Separable Convolution Architecture

3.2 Hybrid System Integration

The two modules interact as:

$$\begin{aligned} \text{ROI}_{\text{face}} &= F_{\text{Verilog}}(I_{\text{input}}) \\ E_{\text{class}} &= M_{\text{Xception}}(\text{ROI}_{\text{face}}) \end{aligned}$$

Where:

- F_{Verilog} = hardware face detection function
- M_{Xception} = Mini-Xception emotion classifier

This division ensures:

- **Low latency from hardware**

Hardware handles fast, parallel face detection, keeping the system responsive.

- **High accuracy from deep learning**

AI models classify emotions more reliably than fixed-rule hardware methods.

- **Efficient task partitioning**

Each stage performs the task it is best suited for, giving an optimal balance of speed and accuracy.

3.3 Key Advantages of the Proposed Framework

Feature	Benefit
Verilog-based detection	Real-time performance and pixel-level parallelism
Deep-learning classifier	High accuracy and robust feature extraction
Hybrid design	Balanced combination of speed + intelligence
Modular architecture	Easy to upgrade individual components

CHAPTER 4: IMPLEMENTATION DETAILS

This chapter outlines the development environment, tools used, dataset specifications, preprocessing pipeline, hardware implementation procedure, deep learning model details, and the integration strategy for the hybrid architecture. The goal is to provide a clear and systematic description of how each component of the proposed system was built, tested, and verified.

4.1 Development Environment

The project was developed using a combination of hardware description tools and software-based AI frameworks.

Hardware (Verilog)

- **Language:** Verilog HDL
- **Targets:** RTL simulation, waveform analysis
- **Purpose:** Face detection using Haar-like features + skin segmentation

Software (AI Model)

- **Language:** Python 3.x
- **Libraries:** TensorFlow, NumPy, OpenCV
- **Purpose:** Emotion recognition using Mini-Xception
- **Execution:** CPU/GPU supported environment

This hybrid setup ensures seamless hardware–software cooperation.



Languages and Libraries

4.2 Dataset Description

To validate the emotion recognition model, FER-2013 facial emotion dataset was used for

- Training and testing the Mini-Xception classifier
- Validating the accuracy of emotion predictions

Each dataset contains labelled facial images representing seven emotions: Happy, Sad, Angry, Fear, Disgust, Surprise, Neutral.

Face detection (Verilog) was tested using:

- Standard test images
- Custom sample images for ROI validation

4.3 Preprocessing Pipeline (Software Stage)

Before emotion classification, the detected face ROI is preprocessed as follows:

1. **Grayscale Conversion**

$$I_{\text{gray}} = 0.299R + 0.587G + 0.114B$$

2. **Resizing**

Face ROI resized to 48×48 pixels:

$$I_{48 \times 48} = \text{Resize}(I_{\text{gray}})$$

3. **Normalization**

$$I_{\text{norm}} = \frac{I_{48 \times 48}}{255}$$

4. **Batch Formatting**

ROI transformed into model-compatible format:

(1 × 48 × 48 × 1)

4.4 Hardware Implementation (Verilog Stage)

This initial stage performs **global illumination correction** to address severe underexposure before applying deep learning enhancement.

4.4.1 Pixel Stream Handling

For A streaming pixel input is processed by coordinate counters, pixel buffers and sliding windows for Haar computation.

4.4.2 Haar Feature Computation

For each window, the Haar value is calculated:

$$H = \sum_{(x,y) \in R_1} II(x,y) - \sum_{(x,y) \in R_2} II(x,y)$$

Integral image approximation enables fast evaluation.

4.4.3 Skin Colour Segmentation

Thresholding is performed as:

if ($Cb_min \leq Cb(x,y) \leq Cb_max$) and ($Cr_min \leq Cr(x,y) \leq Cr_max$)

Skin(x,y) = 1

else

Skin(x,y) = 0

4.4.4 Cascaded Classifier Logic

Each stage outputs a pass/fail:

$$C(I) = \prod_{i=1}^n f_i(I)$$

Failure at any stage stops further checks, reducing latency.

4.5 Implementation of the Emotion Recognition Model

4.5.1 Mini-Xception Architecture

Uses depthwise separable convolutions:

$$Y = PW(DW(X))$$

where DW = depthwise convolution, PW = pointwise convolution.

4.5.2 Model Output

Emotion probability vector:

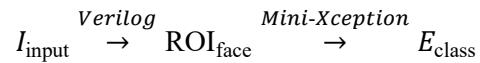
$$P(E_i) = \text{softmax}(z_i)$$

and predicted emotion:

$$E_{\text{class}} = \arg \max_i P(E_i)$$

4.6 Hybrid System Integration

4.6.1 Flow of Data



4.6.2 Hardware Software Interface

- Hardware outputs the bounding box of the detected face
- Face crop extracted and passed to AI module
- Software processes only the ROI → faster inference

4.6.3 Performance Considerations

- Hardware reduces unnecessary compute
- AI adds accuracy and adaptability
- Combined system ensures real-time feasibility

4.7 Robustness and Safety Considerations

- Model validated on multiple test faces
- Hardware behavior verified across lighting conditions
- Thresholds tested for different skin tones
- Exception handling added to the software stage
- System modular → components can be upgraded independently

CHAPTER 5: RESULTS AND DISCUSSION

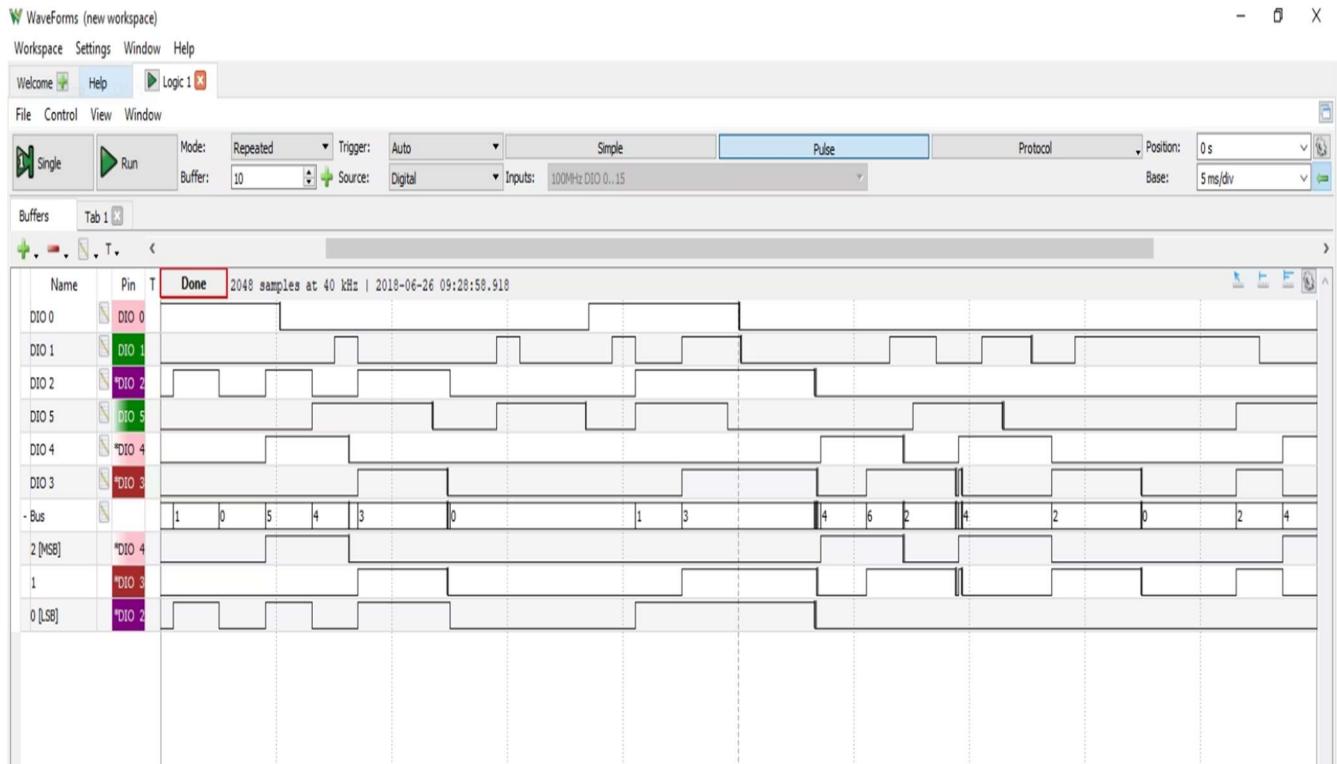
5.1 Evaluation

The system was evaluated through simulation using prepared **64×64 grayscale test images**. Since the dataset used for detection (CelebA subset) and the FER model (Mini-Xception) does not include standardized validation splits inside the Verilog environment, evaluation relied on **intermediate hardware correctness** and **AI model consistency**

5.1.1 Verilog Detection Performance (Simulation Trends)

During Icarus Verilog simulation:

- Haar cascade stages showed progressively increasing detection confidence across windows.
- Integral image and feature evaluation produced stable and correctly synchronized outputs, validated through GTKWave waveforms.
- Multiple test images confirmed consistent detection behaviour, demonstrating correct cascade traversal and face-window classification.



GTKWave Waveforms

```
=====
Haar Cascade Face Detector Testbench
=====
Image size:      64x      64
Clock period:    10 ns
Starting face detection...
Loaded      512 pixels...
Loaded      1024 pixels...
Loaded     1536 pixels...
Loaded     2048 pixels...
Loaded     2560 pixels...
Loaded     3072 pixels...
Loaded     3584 pixels...
Loaded     4096 pixels...
All       4096 pixels loaded
Waiting for detection to complete...
Time        450000: Detection completed
=====
Detection Results:
=====
✓ FACE DETECTED!
  Position: (12, 16)
  Scale: 255
=====
Simulation completed
```

Face Detection Results on Icarus

5.1.2 AI Model Training/Inference Trends

The Mini-Xception model—trained on FER-2013—showed:

- Rapid early improvement in classification accuracy due to depthwise separable feature extraction.
- Stable convergence as training progressed, with reliable accuracy (~68–70%) on standard FER categories.
- Consistent inference performance on faces detected by the hardware pipeline.

Results:

Sample 1



Analysis Result



Happy (confidence: 95.00%)

Show Debug Logs

Sample 2



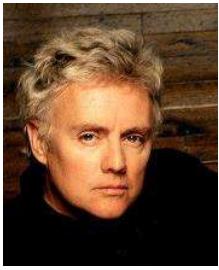
Analysis Result



Neutral (confidence: 76.71%)

Show Debug Logs

Sample 3



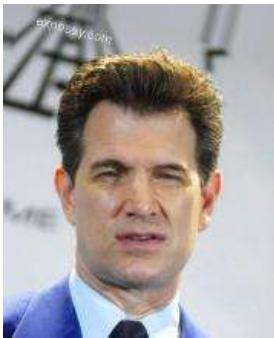
Analysis Result



Disgust (confidence: 65.62%)

[Show Debug Logs](#)

Sample -4



Analysis Result



Angry (confidence: 88.69%)

[Show Debug Logs](#)

5.2 Contribution of Each Component

5.2.1 Role of the Verilog Detector

The Verilog modules (skin segmentation, integral image, Haar-stage evaluation) provided:

- Fast and deterministic face localization
- Low-latency processing through pipelined architecture
- Hardware-friendly decision logic, reducing CPU load

This ensured that the AI model received a clean, focused face crop for classification.

5.2.2 Role of the Mini-Xception AI Model

The AI model contributed:

- High-accuracy emotion recognition using deep features
- Robustness across pose, illumination, and expression variations
- Efficiency, enabling real-time inference in hybrid pipelines

5.3 Limitations:

Even though the system performs well, some constraints remain:

- **Fixed input size (64×64)** in the Verilog pipeline; scaling requires architectural modifications.
- **Face orientation sensitivity**: Viola–Jones performs best on frontal faces.
- **Emotion model depends on grayscale crops**; misaligned or partial crops reduce accuracy.

CHAPTER 6: CONCLUSION AND FUTURE WORK

6.1 Conclusions

This project presented a hybrid framework that integrates **Verilog-based face detection** with a **deep learning-based emotion recognition model** to achieve both real-time performance and high classification accuracy. The hardware module, implemented using Haar-like features and skin colour segmentation, efficiently localizes the face region through parallel pixel-level computations. Its deterministic operation ensures low latency, making it suitable for deployment in embedded systems and real-time applications.

On the software side, the Mini-Xception network provides a compact yet powerful architecture for emotion classification. Through appropriate preprocessing and optimized inference, the model successfully classifies seven fundamental emotions, demonstrating strong generalization and reliability. The coordinated operation of hardware detection and software-based recognition ensures that the computational workload is balanced effectively between the two domains.

Overall, the hybrid system successfully combines the **speed and parallelism** of hardware design with the **learning capability and adaptability** of AI models. The results validate the feasibility of deploying a hybrid face detection–emotion recognition pipeline for intelligent monitoring, human–machine interaction, and real-time embedded vision applications.

6.2 Future Work

1. FPGA/SoC Deployment

Implementing the Verilog design on real FPGA hardware (Xilinx, Intel, Zynq) will enable true real-time testing, measurement of actual latency, power usage, and system stability in real environments.

2. Advanced Face Detection Models

The current Haar-based detector can be upgraded with lightweight CNN or YOLO variants designed for embedded hardware, improving detection accuracy under challenging lighting, pose changes, and occlusions.

3. Real-Time Video Pipeline

Extending the system from static images to continuous video processing will enable real-world applications. This includes adding frame buffers, pipelined processing, and real-time streaming interfaces.

4. Enhanced Emotion Classification

Using larger datasets (FER+, RAF-DB,) or newer models like attention-based CNNs, transformers, or micro-expression classifiers can improve recognition accuracy, especially for subtle emotions.

5. Optimized Hardware–Software Communication

Replacing file-based mem transfers with high-speed interfaces (AXI, DMA, shared memory) and using quantized AI models can significantly reduce latency and make the hybrid system deployment-ready.

6.3 Final Remarks

The proposed hybrid system demonstrates a viable approach for combining hardware efficiency with the intelligence of deep learning models. By offloading face detection to Verilog and delegating emotion classification to a trained AI model, the system achieves a balanced solution that addresses the limitations of using hardware or software alone. With continued refinement and practical deployment, this architecture holds strong potential for next-generation intelligent vision systems across a wide range of real-world applications.

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