

Decoupling capacitors and SWD header

[illegible]

The diagram shows two timing diagrams, J2 and J3, with signal transitions indicated by red arrows and levels by red numbers.

J2:

- T_SWDIO_TMS: 9
- T_SWDCLK_JCLK: 8
- T_SWO_TDO: 7
- T_GNDDetect: 6
- T_TDI: 5
- T_RESET: 4
- T_VCP_TX: 3
- T_VCP_RX: 2
- 1

J3:

- PROTECTED_SV: 2
- 1
- J4:
- T_VCC: 3
- GPI01: 2
- GPI02: 1

[illegible][illegible]

To see the DAC vs Output voltage,
see [math/find_resistors.m](#)

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