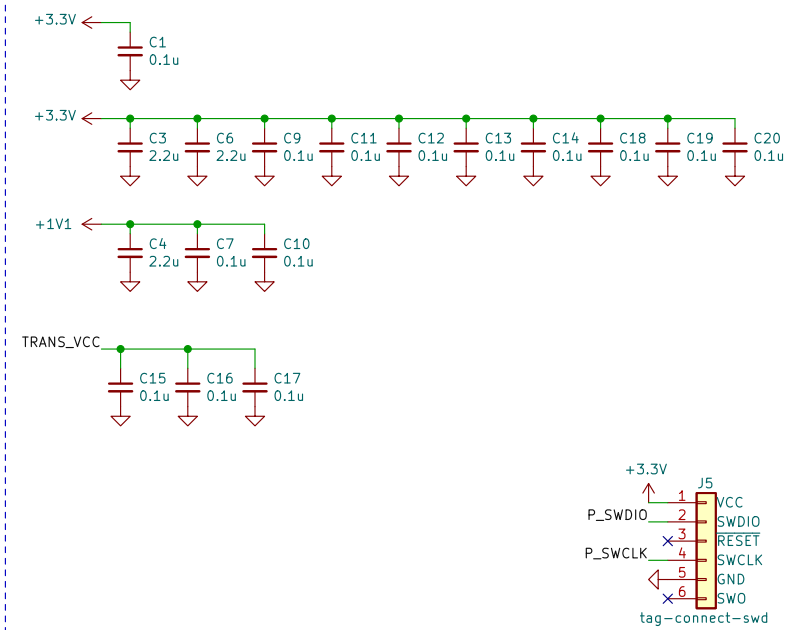
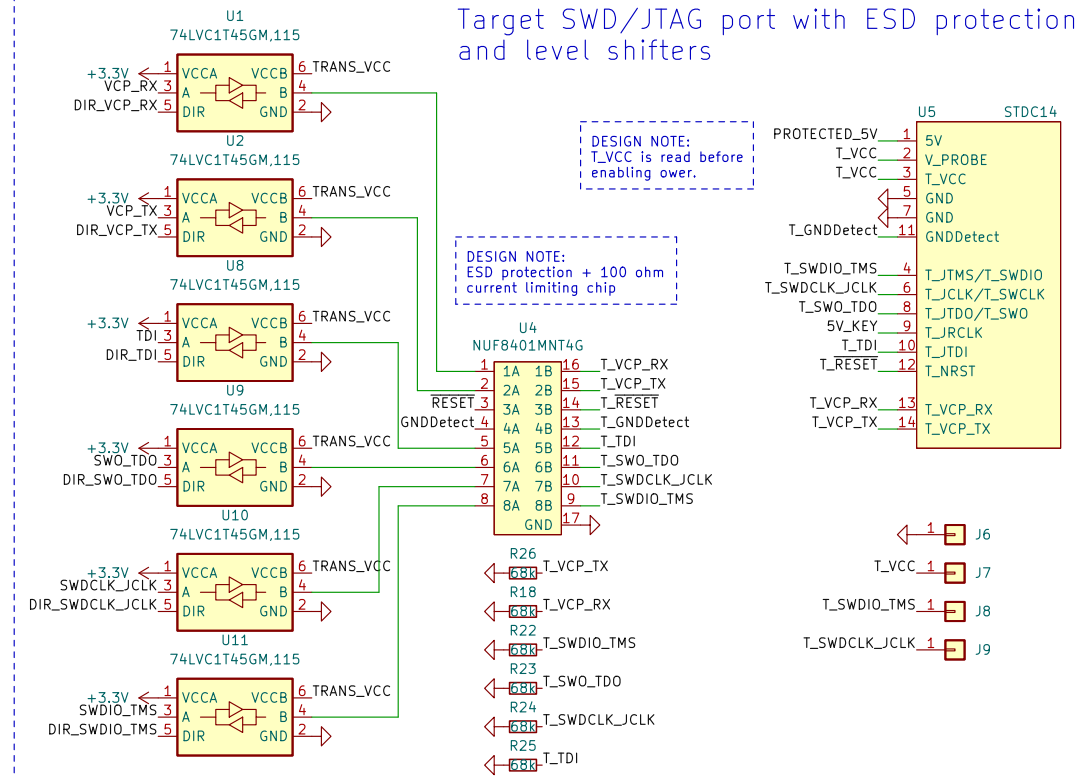


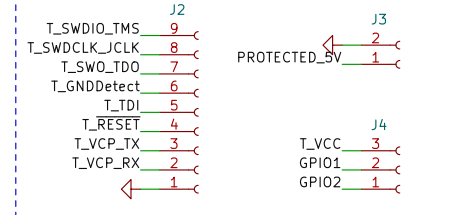
Decoupling capacitors and SWD header



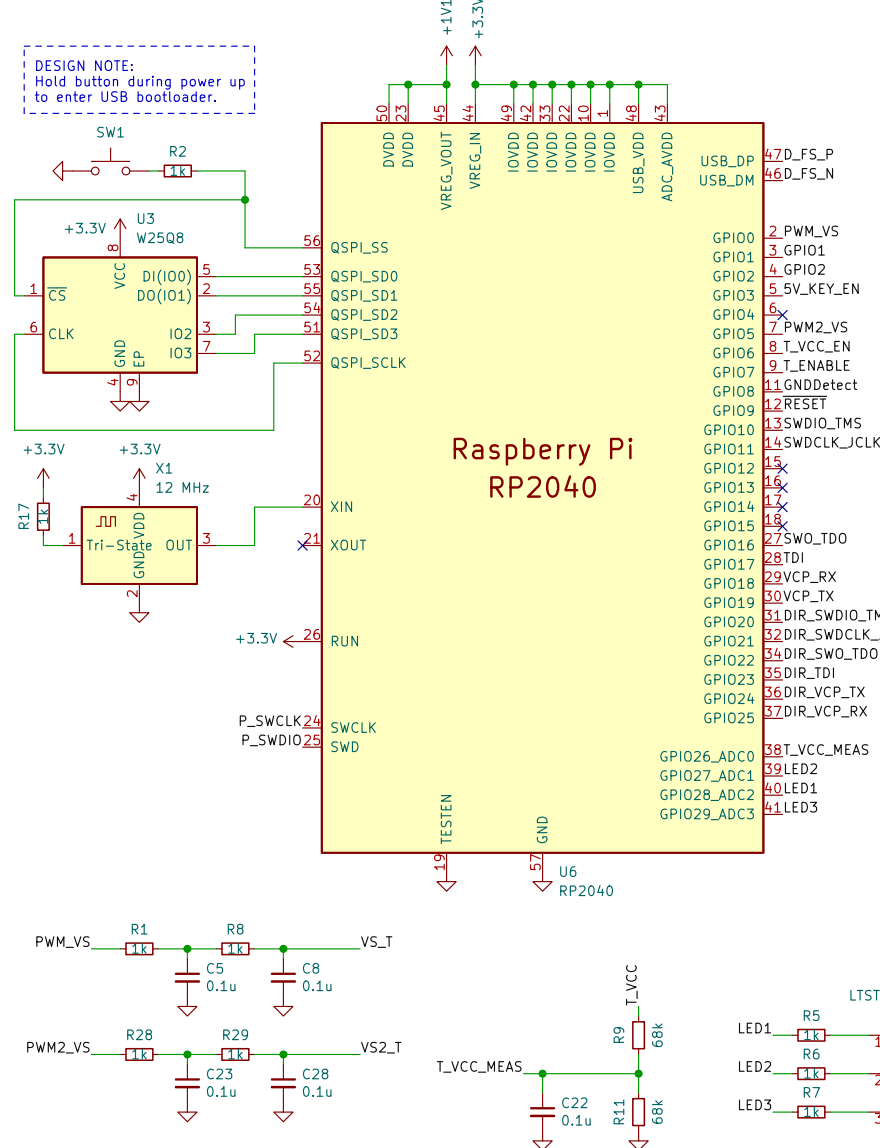
Target SWD/JTAG port with ESD protection and level shifters



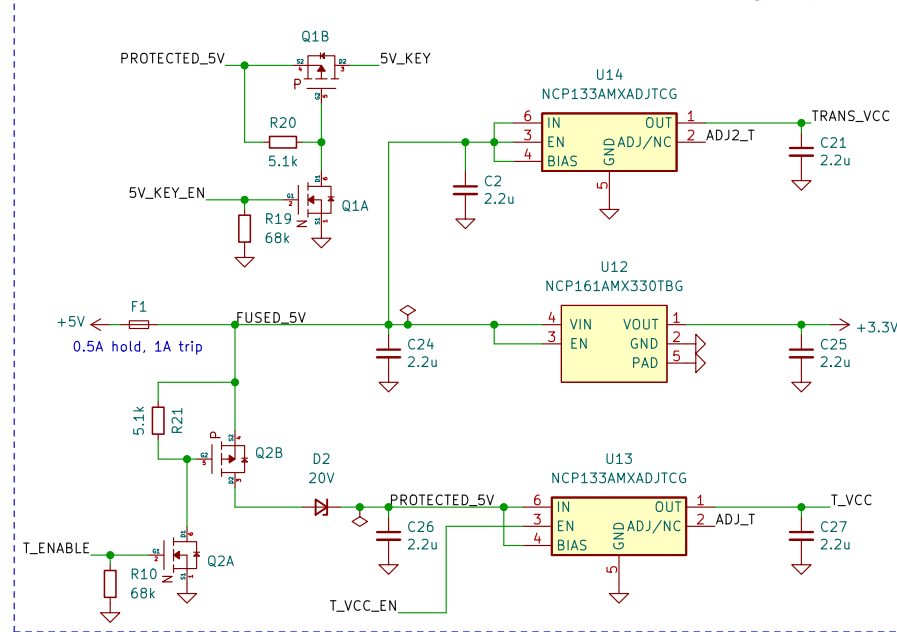
Board-edge castellated vias



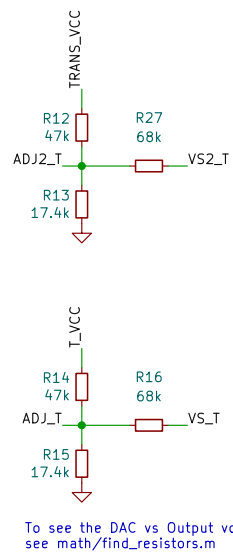
MCU



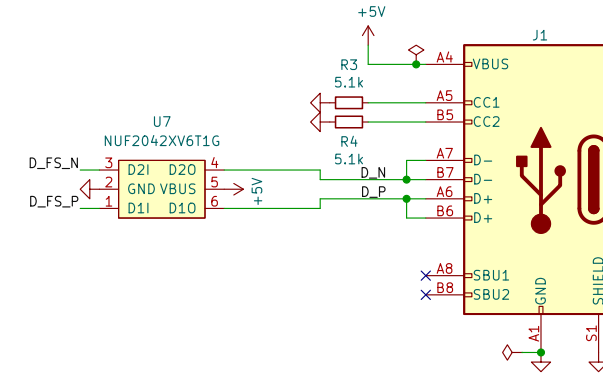
MCU, Translators, and Target power



Target voltage feedback with PWM DAC control



USB-C port with ESD protection



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Designed by: Emil Fresk
Twitter / Github: @korken89
Link: <https://github.com/probe-rs/rs-probe>

Sheet: /	File: rs-probe.kicad_sch	
Title: The Rusty Probe		
Size: A3	Date: 2022-03-09	Rev: D
KiCad E.D.A.	(6.0.2)	Id: 1/1