WE310G4-I/P Module

Hardware User Guide

1VV0301767 Rev 9
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Released
Confidential

Technical Documentation

Contents

1. Applicability Table

Table 1: Applicability Table

Products
WE310G4-I
WE310G4-P

2. Introduction

2.1. Scope

This document describes electrical specifications, mechanical information, interface application, and manufacturing information about the Telit WE310G4-I/P Wi-Fi/BLE module. With the help of this document and other application notes or user guides, users can understand the Telit WE310G4-I/P Wi-Fi/BLE module well and develop various products quickly.

2.2. Audience

This document is intended for Telit customers, especially system integrators, about to implement their applications using the Telit module.

2.3. Contact Information, Support

For technical support and general questions, e-mail:

- TS-EMEA@telit.com
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- TS-SRD@telit.com
- TS-ONEEDGE@telit.com

Alternatively, use: https://www.telit.com/contact-us/

Product information and technical documents are accessible 24/7 on our website: https://www.telit.com

2.4. Conventions

Note: Provide advice and suggestions that may be useful when integrating the module.

Danger: This information MUST be followed, or catastrophic equipment failure or personal injury may occur.

ESD Risk: Notifies the user to take proper grounding precautions before handling the product.

Warning: Alerts the user on important steps about the module integration.

All dates are in ISO 8601 format, that is YYYY-MM-DD.

2.5. Terms and conditions

Refer to https://www.telit.com/hardware-terms-conditions/.

2.6. Disclaimer

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3. General Product Description

3.1. Overview

The WE310G4-I/P is a combo module with a dual-band (2.4 GHz and 5 GHz) and Bluetooth Low Energy (BLE 5.0) combo module that provides an easy and cost-effective way for users to add wireless connectivity to their products. This module is available in two form factors – with an antenna and without an antenna. WE310G4-I is integrated with a ceramic antenna of 15mmx18mm dimension. The WE310G4-P is integrated with an RF pad of 13.1mmX14.3mm dimension. Both the form factors share the same Pinout and are pin-to-pin compatible. These modules are designed to be pin-to-pin compatible with the single-band WE310G4-I/P combo modules with the same functionalities and features.

3.2. Product Variants and Frequency Bands

The Telit WE310G4 module is available in two variants. To see the details on the differences between the two variants, refer to the figure Product Variants and Frequency Band.

- WE310G4-I
- WE310G4-P

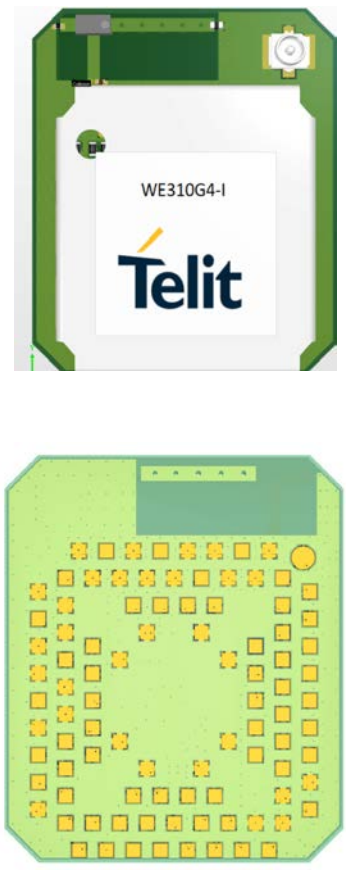
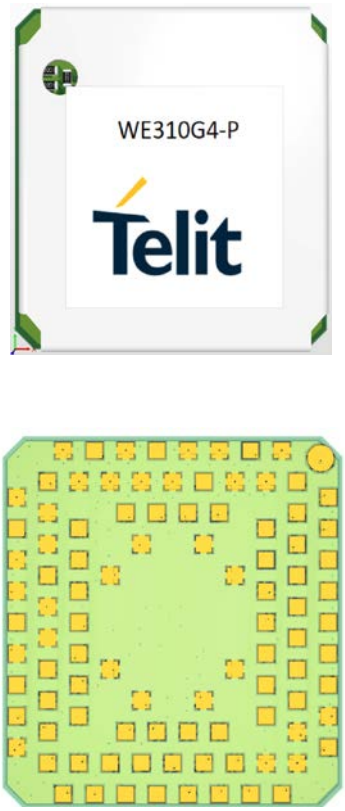
WE310G4-I	WE310G4-P
	

Figure 1: Product Variants and Frequency Band

Notes:

- (EN) The integration of the WE310G4-I/P module within the user application shall be done according to the design rules described in this manual.
- (IT) L'integrazione del modulo cellulare WE310G4-I/P all'interno dell'applicazione dell'utente dovrà rispettare le indicazioni progettuali descritte in questo manuale.
- (DE) Die Integration des WE310G4-I/P Mobilfunk-Moduls in ein Gerät muß gemäß der in diesem Dokument beschriebenen Kunstruktionsregeln erfolgen.
- (SL) Integracija WE310G4-I/P modula v uporabniški aplikaciji bo morala upoštevati projektna navodila, opisana v tem priročniku.
- (SP) La utilización del modulo WE310G4-I/P debe ser conforme a los usos para los cuales ha sido deseñado descritos en este manual del usuario.
- (FR) L'intégration du module cellulaire WE310G4-I/P dans l'application de l'utilisateur sera faite selon les règles de conception décrites dans ce manuel..
- [HE]
האינטגרטור מתבקש ליישם את ההנחיות המפורטות במסמך זה בתהליך האינטגרציה של המודם הסלולרי WE310G4-I/P עם המוצר.

3.3. Block Diagram

The following figure shows a high-level block diagram of the WE310G4-I/P module and its major functional blocks.

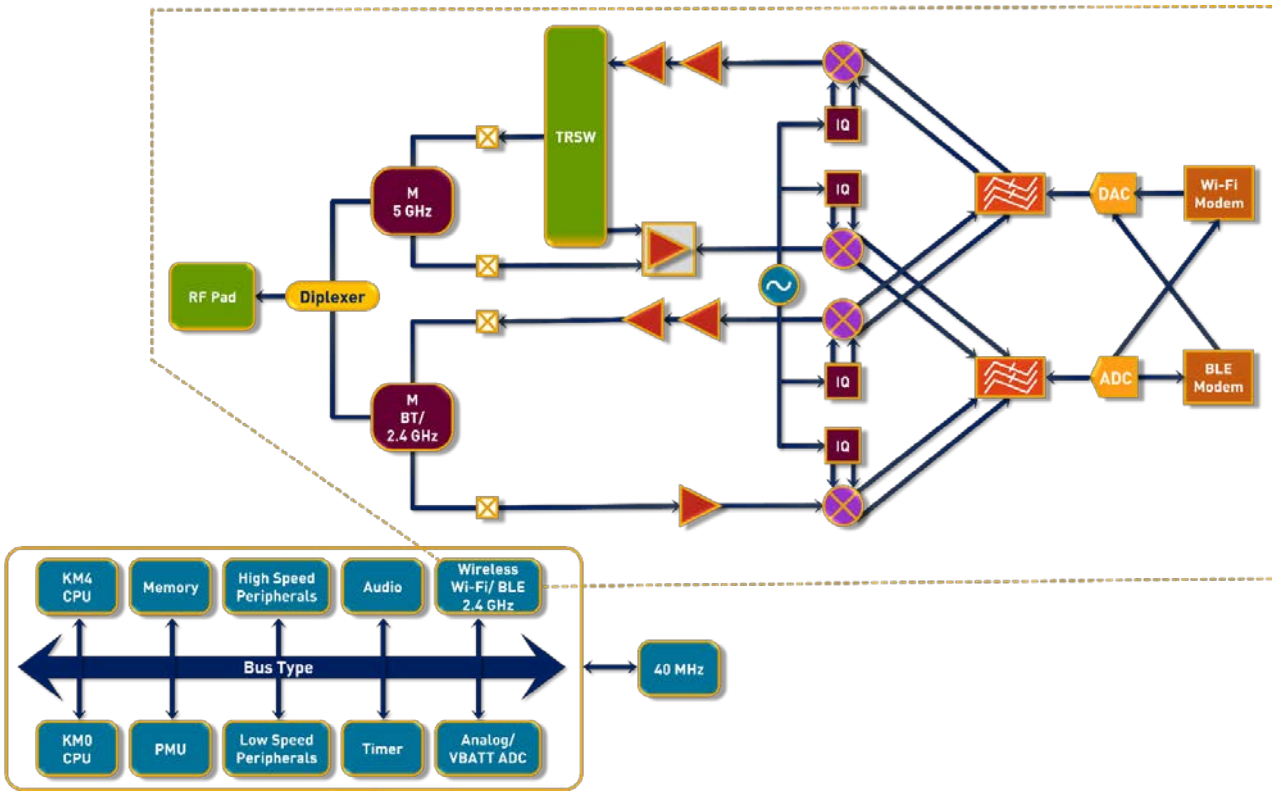


Figure 2: Telit WE310G4-I/P Module Block Diagram

4. Features

4.1. Main Features

1 Highly integrated single chip with low power dual-band (2.4GHz and 5Ghz) Wireless LAN (WLAN) and Bluetooth Low Energy (BLE5.0) communication controller.

2 High-performance ArmV8-M-Cortex-M33 (KM4) processor + low power Armv8-M-Cortex-M23 (KM0) processor, WLAN (802.11 a/b/g/n) MAC, a 1T1R capable WLAN baseband, RF, Bluetooth, and peripherals.

3 High-speed connectivity interfaces, SPI, SDIO, and USB

4 4 MB FLASH Memory (32Mbits)

5 512KB RAM

6 156KB Retention SRAM

Table 2: Main Features

Item	Description
Wi-Fi	802.11 a/b/g/n 2.4 GHz and 5 GHz 20MHz/40MHz up to MC7 Low power architecture Low Power beacon listen mode Low-power Rx mode Very low power suspend mode (DLPS) Built-in PA Internal PTA interface for arbitrating data transmission between Wi-Fi and Internal Bluetooth or external 2.4 GHz devices
BLE	BLE 5.0 Both central and peripheral modes High power mode (8dbm, share the same PA with Wi-Fi) Internal co-existence mechanism between Wi-Fi and BT to share the same antenna
Temperature Range	Operating: -40°C ~ 85°C Junction: -40°C ~ 105°C Storage: -55°C ~ 125°C

The WE310G4-I/P module supports the following peripherals interfaces.

Table 3: Supported Peripherals (The supported peripherals will be fixed after preliminary tests on MKT samples)

Item	Peripherals	Comment
UART	UART0	Supports Low Power Mode Wakeup
	AUX_UART	LOG UART/Low power mode wakeup (no Flow control)). Used for flashing, RF Tests, and logs.
SPI	SPI0	Master/Slave Clock up to 50 MHz
I2C	HS_I2C	Standard/fast/high-speed mode (up to 3.33Mbps)
SDIO	1-Bit SDIO mode	Maximum Clock 50 MHz
PWM	HS_PWM8/ LP_PWM2	

Item	Peripherals	Comment
DVI	I2S	Sampling rates: • 8kHz ~ 176.4kHz • Mono • Stereo • 5.1 channel. The sample size for Mono: • 16-bit • 32-bit The sample size for Stereo & 5.1 channel: • 16-bit • 24-bit • 32-bit PCM not supported
USB		USB 2.0 CDC class device
ADC	12-bit SAR ADC	Single-ended input Range: 0~3.3V
RTC		12- or 24-hour format (seconds, minutes, hours, days) Daylight saving compensation Register write protection

5. PIN Allocation

5.1. Pin-Out

All IOs are in LVTTL 3.3V logic.

Note: The table below highlights module pins that are connected to the same signal/pin in SoC. For example, pin V11 is also connected to pins AA7 and F2. Therefore, either V11 or AA7 / F2 shall be connected.

Table 4: Pin-Out Description

Multiplexed Pin list					
WE310G4 – Pin Group 1		WE310G4 – Pin Group 2		WE310G4 – Pin Group 3	
Pin	Signal	Pin	Signal	Pin	Signal
V11	I2C_SCL	AA7	SPI_CLK	F2	DXI_CLK
V13	I2C_SDA	Y6	SPI_CS	C1	DVI_WA0
D7	SD_D0	-	-	D2	DVI_RX
D9	IO4/SD_D1_INT	AA5	SPI_MOSI	-	-
D11	IO5	Y8	SPI_MISO	E1	DVI_TX
D13	SPI_INT/IO6	-	-	R16	DAC

Primary serial port					
Pin	Signal	I/O	Function	Comment	Pull-down Restriction
Y16	RXD0	I	Serial data Input (RXD)		>1K
AA15	TXD0	O	Serial data Output (TXD)		>1K
Y18	CTS0	I	Input for Clear to send a signal (CTS)		>1K
AA17	RTS0	O	Output for Request to send a signal RTS		>1K

USB					
Pin	Signal	I/O	Function	Comment	Pull-down Restriction
U19	USB_D+	I/O	USB differential Data (+)		>1K
V18	USB_D-	I/O	USB differential Data (-)		>1K

Auxiliary Serial Port					
Pin	Signal	I/O	Function	Comment	Pull-down Restriction
Y10	TX_AUX	O	Auxiliary (DEBUG) UART output	Program mode pin	>1K
AA9	RX_AUX	I	Auxiliary (DEBUG) UART input		>1K

DIGITAL IO					
Pin	Signal	I/O	Function	Comment	Pull-down Restriction
V11	IO1/I2C_SCL	I/O	Configurable GPIO	Floating, if not connected	
V13	IO2/I2C_SDA	I/O	Configurable GPIO	Floating, if not connected	
D7	IO3/SD_D0	I/O	Configurable GPIO	Floating, if not connected	

DIGITAL IO					
Pin	Signal	I/O	Function	Comment	Pull-down Restriction
D9	IO4/SD_D1_INT	I/O	Configurable GPIO	SDIO Interrupt	
D11	IO5	I/O	Configurable GPIO	Floating, if not connected	
D13	SPI_INT/IO6	I/O	SPI Interrupt/Configurable GPIO	Floating, if not connected	

SPI					
Pin	Signal	I/O	Function	Comment	Pull-down Restriction
AA5	SPI_MOSI	I/O	MOSI		
Y6	SPI_CS	I/O	Chip Select		>1K
AA7	SPI_CLK	I/O	Clock		>1K
Y8	SPI_MISO	I/O	MISO		>1K

ADC and DAC					
Pin	Signal	I/O	Function	Comment	Pull-down Restriction
B18	ADC	I	Analog to Digital Converter Input	0V ~ 3.3V	>1K
R16	DAC	O	PWM output	Floating, if not connected	

RF					
Pin	Signa1l	I/O	Function	Comment	Pull-down Restriction
A5	WIFI/BT ANTENNA	I/O	RF pad (50 ohm) on P variant		

Miscellaneous					
Pin	Signal	I/O	Function	Comment	Pull-down Restriction
N16	ON*	I	RESET pin	Active low	
L16	WAKEUP	I/O	Wakeup is not supported. It can only be used as a GPIO.		>1K

* - Denotes the pin is active low type.

Audio					
Pin	Signal	I/O	Function	Comment	Pull-down Restriction
C1	DVI_WA0	O	I2S Frame Sync	Floating, if not connected	
D2	DVI_RX	O	I2S RX	Floating, if not connected	
E1	DVI_TX	I	I2S TX	Floating, if not connected	
F2	DVI_CLK	I	I2S CLK	Floating, if not connected	

Power Supply					
Pin	Signal	I/O	Function	Comment	Pull-down Restriction
W1	VBATT_3V3	-	Main power supply 3.3V	Power	
AA3	VBATT_3V3	-	Main power supply 3.3V	Power	
A3	GND	-	RF Ground	Power	
A7	GND	-	RF Ground	Power	

Power Supply					
Pin	Signal	I/O	Function	Comment	Pull-down Restriction
A9	GND	-	RF Ground	Power	
A13	GND	-	RF Ground	Power	
A17	GND	-	RF Ground	Power	
B4	GND	-	RF Ground	Power	
B6	GND	-	RF Ground	Power	
B10	GND	-	RF Ground	Power	
B12	GND	-	RF Ground	Power	
B14	GND	-	RF Ground	Power	
B16	GND	-	RF Ground	Power	
C19	GND	-	RF Ground	Power	
D18	GND	-	RF Ground	Power	
F8	GND	-	Thermal Ground	Power	
F12	GND	-	Thermal Ground	Power	
F18	GND	-	Thermal Ground	Power	
G19	GND	-	Thermal Ground	Power	
H6	GND	-	Thermal Ground	Power	
H14	GND	-	Thermal Ground	Power	
J19	GND	-	Thermal Ground	Power	
K18	GND	-	Thermal Ground	Power	
M18	GND	-	Thermal Ground	Power	
N19	GND	-	Thermal Ground	Power	
P6	GND	-	Thermal Ground	Power	
P14	GND	-	Thermal Ground	Power	
T8	GND	-	Thermal Ground	Power	
T12	GND	-	Thermal Ground	Power	
U1	GND	-	Power Ground	Power	
V2	GND	-	Power Ground	Power	
W19	GND	-	Power Ground	Power	
Y2	GND	-	Power Ground	Power	
Y4	GND	-	Power Ground	Power	

Debug Port (SWD)				
Pin	Signal	I/O	Function	Comment
J4	SWD_CLK	SWD_CLK		
L4	SWD_DATA	SWD_DATA	Bootstrap pin. LOW for SWD	The Pull-down resistor is restricted

RESERVED					
Pin	Signal	I/O	Function	Comment	Pull-down Restriction
A11	RESERVED	-	RESERVED		
A15	RESERVED	-	RESERVED		
B2	RESERVED	-	RESERVED		
B8	RESERVED	-	RESERVED		

RESERVED					
Pin	Signal	I/O	Function	Comment	Pull-down Restriction
E19	RESERVED	-	RESERVED		
G1	RESERVED	-	RESERVED		
G4	RESERVED	-	RESERVED		
G16	RESERVED	-	RESERVED		
H2	RESERVED	-	RESERVED		
H18	RESERVED	-	RESERVED		
J1	RESERVED	-	RESERVED		
J16	RESERVED	-	RESERVED		
K2	RESERVED	-	RESERVED		
L1	RESERVED	-	RESERVED		
L19	RESERVED	-	RESERVED		
M2	RESERVED	-	RESERVED		
N1	RESERVED	-	RESERVED		
N4	RESERVED	-	RESERVED		
P2	RESERVED	-	RESERVED		
P18	RESERVED	-	RESERVED		
R1	RESERVED	-	RESERVED		
R4	RESERVED	-	RESERVED		
R19	RESERVED	-	RESERVED		
T2	RESERVED	-	RESERVED		
T18	RESERVED	-	RESERVED		
V7	RESERVED	-	RESERVED		
V9	RESERVED	-	RESERVED		
Y12	RESERVED	-	RESERVED		
Y14	RESERVED	-	RESERVED		
AA11	RESERVED	-	RESERVED		
AA13	RESERVED	-	RESERVED		
E4	RESERVED	-	RESERVED	P version only	
E16	RESERVED	-	RESERVED	P version only	
U4	RESERVED	-	RESERVED	P version only	
U16	RESERVED	-	RESERVED	P version only	

Note: Unused Pins can be left floating.

5.2. General Purpose I/O

Module by default has 1 dedicated GPIO (IO3). The remaining GPIOs are multiplexed with other interfaces.

Table 5: General Purpose I/O

Pin	Signal Name	GPIO Number
V11	IO1/I2C_SCL/SD_CMD	IO1
V13	IO2/I2C_SDA/SD_CLK	IO2
D7	IO3/ SD_D0	IO3
D9	IO4/SD_D1_INT	IO4

Pin	Signal Name	GPIO Number
D11	IO5	IO5
D13	SPI_INT/IO6	IO6
Y16	RXD0	IO7
AA15	TXD0	IO8
Y18	CTS0	IO9
AA17	RTS0	IO10
U19	USB_D+	IO11
V18	USB_D-	IO12
Y10	TX_AUX	IO13
AA9	RX_AUX	IO14
AA5	SPI_MOSI	IO8
Y6	SPI_CS	IO9
AA7	SPI_CLK	IO10
Y8	SPI_MISO	IO7
B18	ADC	IO19
R16	DAC	IO4
L16	WAKEUP	IO21
C1	DVI_WA0	IO2
D2	DVI_RX	IO3
E1	DVI_TX	IO5
F2	DVI_CLK	IO1
J4	SWD_CLK	IO26
L4	SWD_DATA	IO27

Table 6: General Purpose I/O Alternate Function

GPIO Number	Alternate Function 1- I2C	Alternate Function 2 SPI	Alternate Function 3 1bit mode SDIO	Alternate Function 4 I2S	Alternate Function 5 PWM
IO1	I2C_SCL (I2C Clock)	SPI_CLK	SD_CMD (SD Command)	DVI_CLK	PWM
IO2	I2C_SDA (I2C Data)	SPI_CS	SD_CLK (SD Clock)	DVI_WA0	
IO3			SD_D0 (SD Data 0)	DVI_RX	
IO4		SPI_MOSI	SD_D1 (SD Interrupt)	I2S_MCLK	
IO5		SPI_MISO		DVI_TX	
IO6		SPI_INT			PWM

5.3. SAR ADC Characteristics

Table 7: SAR ADC Characteristics

Parameter	Condition	Minimum	Typical	Maximum	Unit
Temperature		-40	25	125	C°
Resolution	Bypass mode		12		Bits
	Resistor driver mode		12		Bits
Clock Source	From digital			1000	kHz
DC Offset Error	Cover VBAT=1.62~3.63V		2		LSB

5.4. Pad Layout

The Pad layout for both (WE310G4-I and WE310G4-P) versions of the module is the same, the only difference is the dimension of the module as WE310G4-I has the onboard antenna.

The following figures show the pad layout:

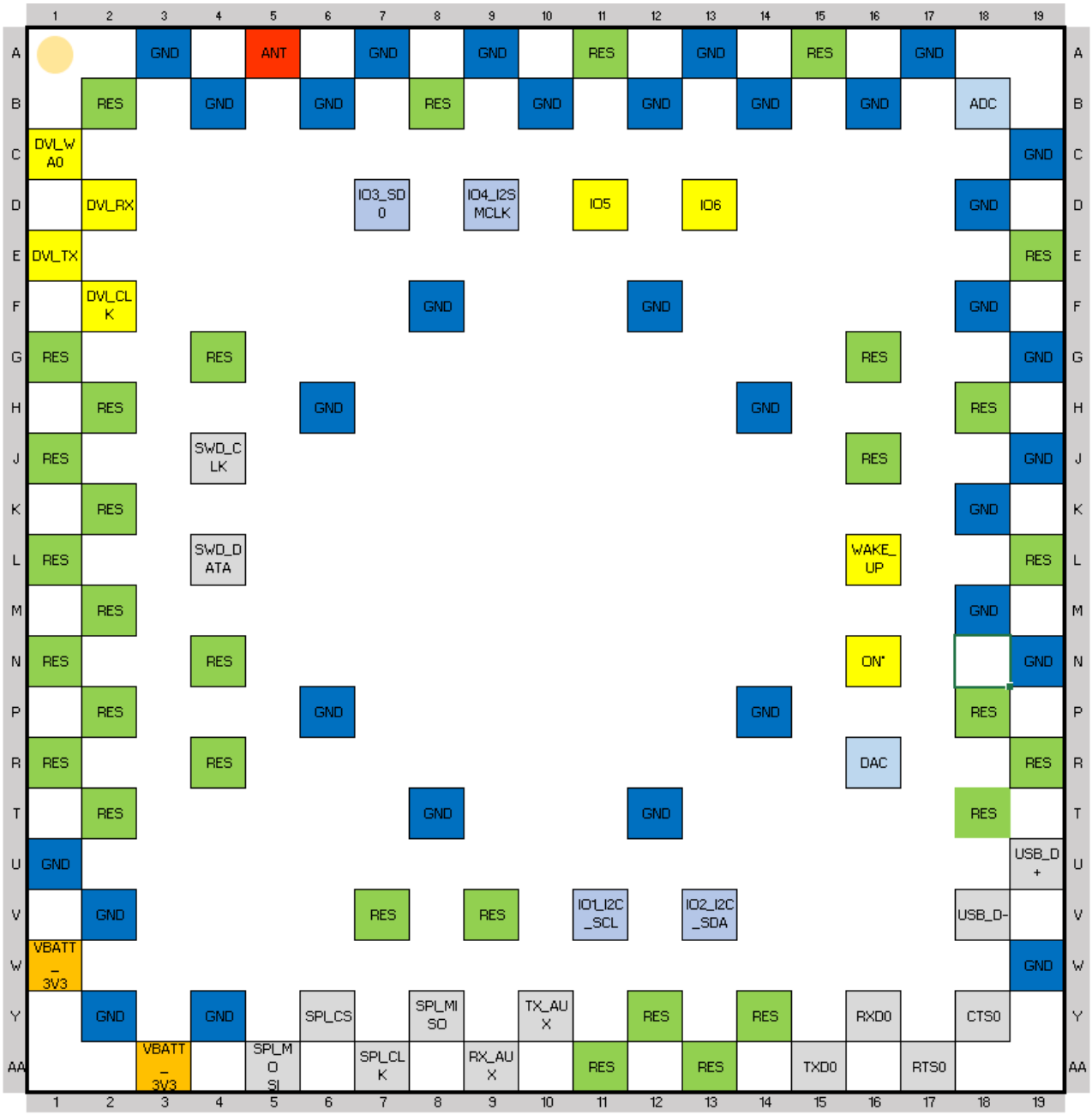


Figure 3: Telit WE310G4-I Pads Layout Top View

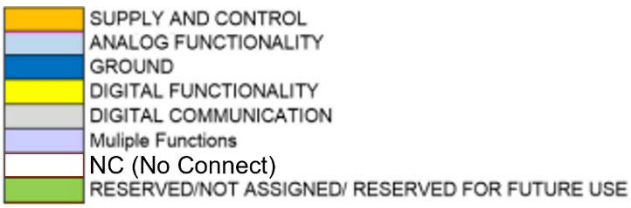


Figure 4: Telit WE310G4-I PIN Out Legend

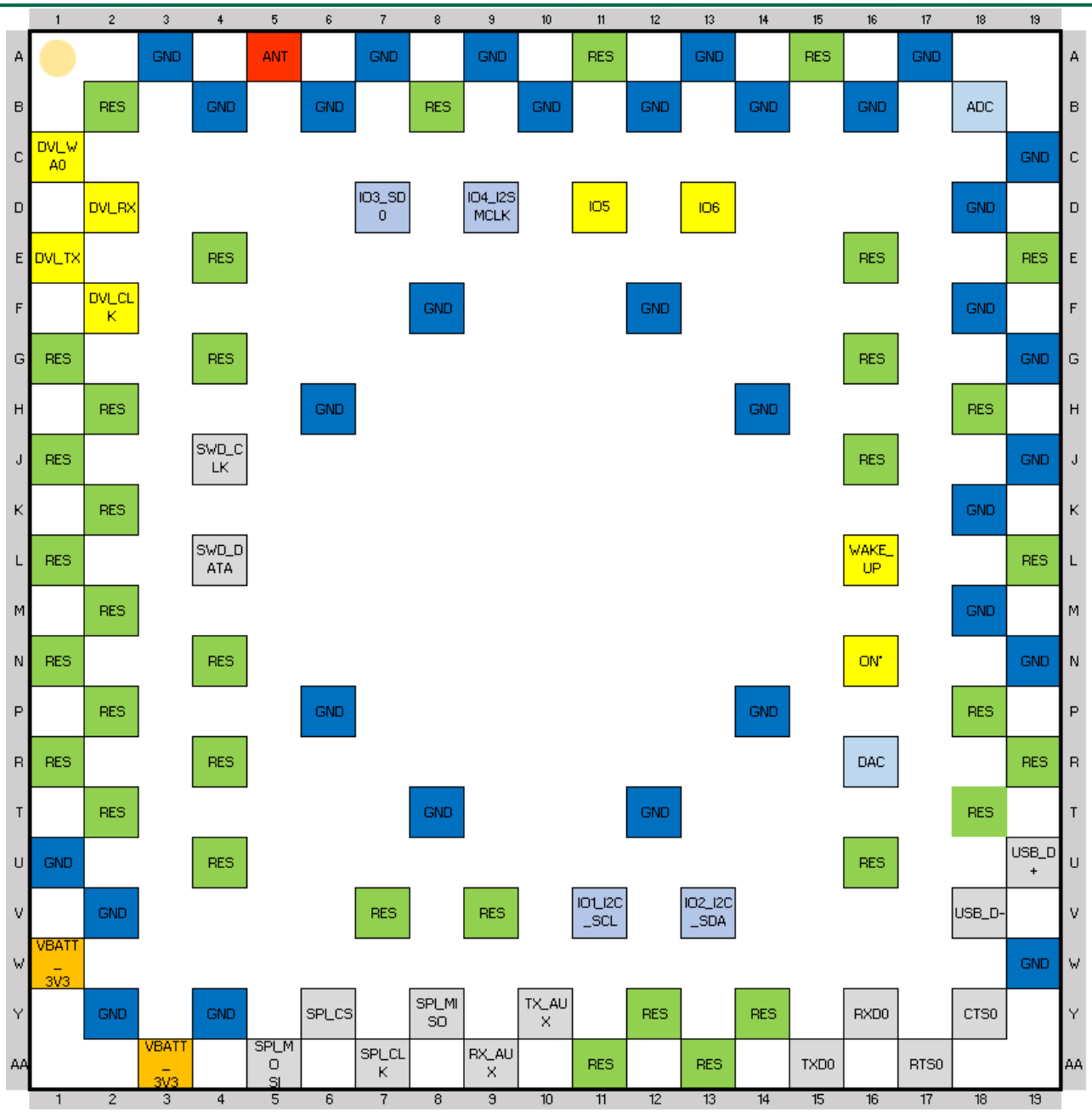


Figure 5: Telit WE310G4-P Pads Layout Top View

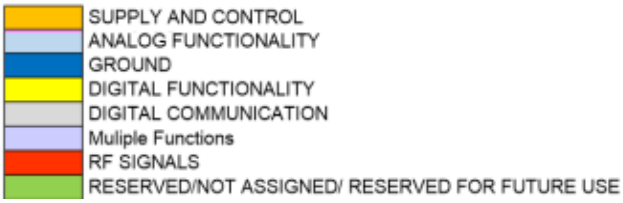


Figure 6: Telit WE310G4-P PIN Out Legend

6. Power Supply

6.1. Power Supply Requirements

The WE310G4-I/P can be directly supplied by a 3.3V power supply source capable of at least 500mA or higher. The voltage supply to all the required parts of the chipset is provided by an embedded switching regulator.

Table 8: Power Supply Requirements

Power Supply	Minimum	Typical	Maximum
Main Power ratings	3.0 V	3.3V	3.6 V

6.2. Logic Levels

Table 9: Logic Levels

Levels with VIO = 3.3V	Min
VIH Input high-level	2.0V
VIL Input low-level	-
VOH Output high-level	2.4V
VOL Output low-level	-
IT+ Schmitt-trigger High Level	1.78V
IT- Schmitt-trigger Low Level	1.36V
ILL input-Leakage Current	-10 µA

6.3. Power up, Power off, and Reset Sequences

Module power-up, power-off, and reset sequences are shown below:

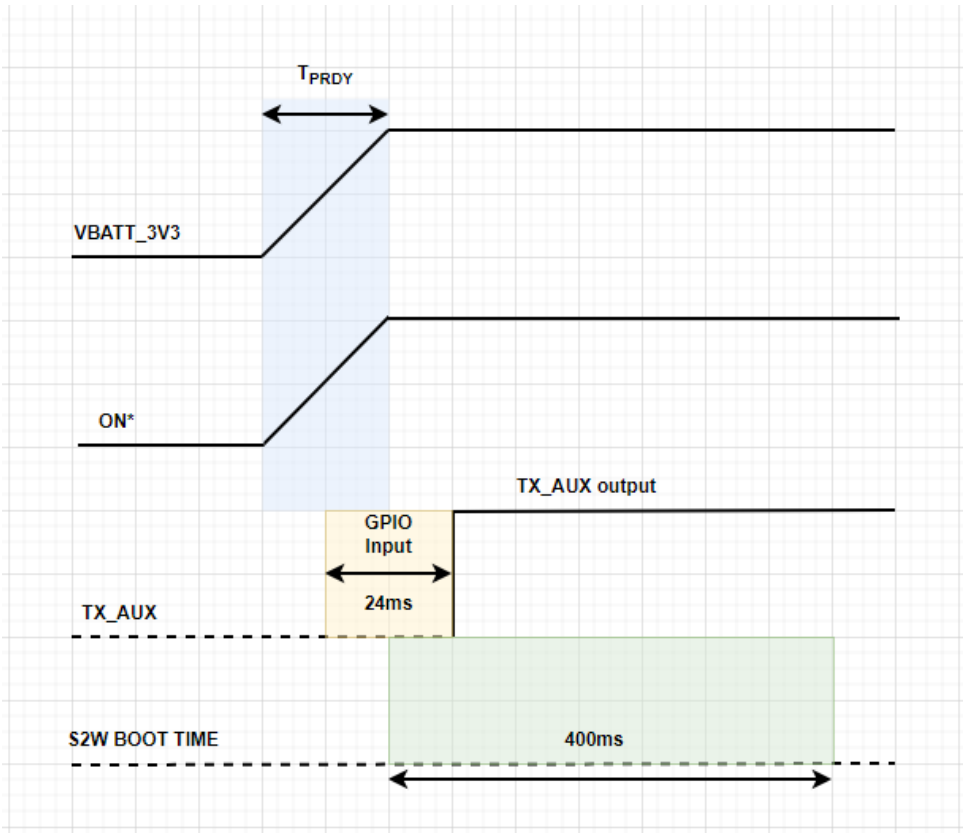


Figure 7: Power On Sequence

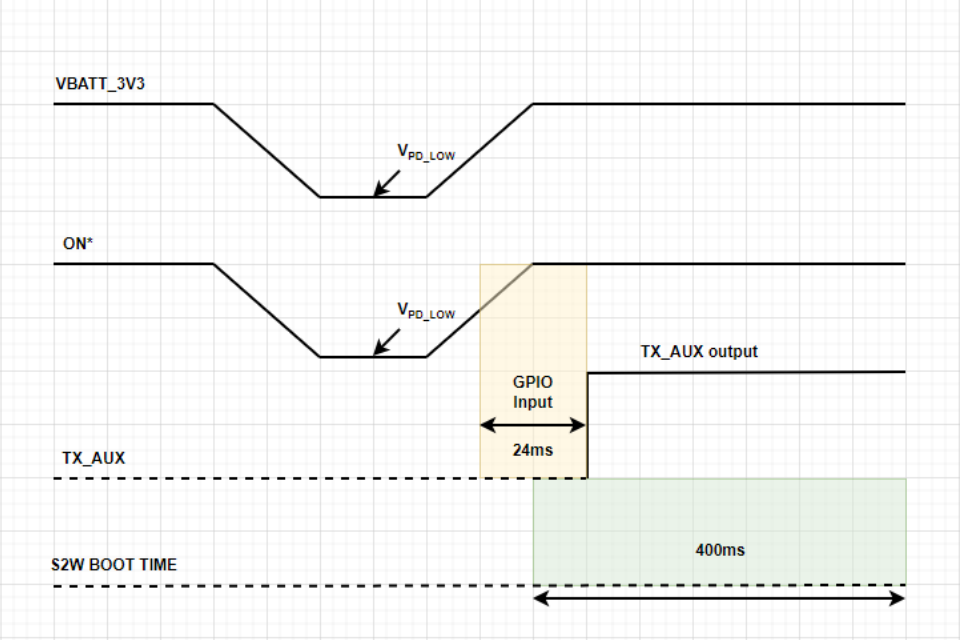


Figure 7: Power Off and Power On Sequence

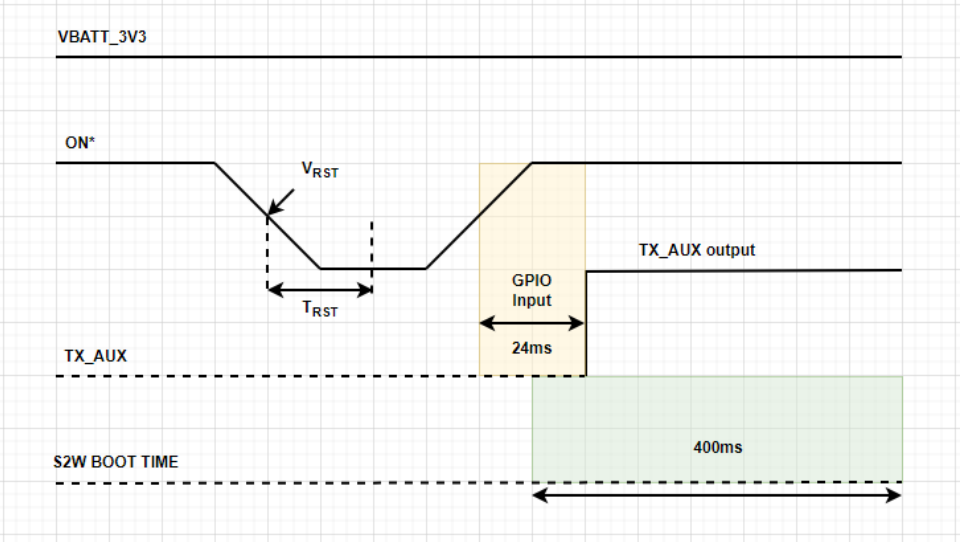


Figure 8: Reset Sequence

Table 10: Timing Specification of the Power up, Power off, and Reset sequence

Symbol	Parameter	Min	Typical	Max	Unit
T_{PRDY}	VDD_IO ready time	0.6	0.6	1	ms
V_{RST}	Shutdown occurs after ON* is lower than this voltage	0	0	0.2*VBATT_3V3	V
T_{RST}	The required time when ON* is lower than VRST	1	1	-	ms
V_{PD_LOW}	Power-down low voltage	0	0	0.3	V

6.4. Average power consumption

The table below shows the current consumption in different states. These measurements are obtained from a DC power analyzer.

Table 11: Module power consumption in different states

Power Consumption	Typical Average (mA)
Standby	0.003
Idle (Radio OFF, UART ON)	13.6

Power Consumption	Typical Average (mA)
Deep Sleep (Radio OFF) (no Wi-Fi Association)	0.05
Deep Sleep (Radio ON) (with Wi-Fi Association)	1.74
DTIM=3	0.545
DTIM=10	0.189
BLE RX (peak current, connected to BT NW)	54.5
BLE TX (peak current, connected to BT NW)	55.1
Wi-Fi RX (continuous)	53

6.5. WLAN Continuous Tx power consumption

The table below shows the current consumed by the module at different WLAN data rates in non-signaling mode. These measurements are obtained from a DC power analyzer.

Table 12: 2.4 GHz WLAN Continuous Tx Power Consumption

Wi-Fi 2.4GHz / CH 6 Standard 802.11x	Modulation	Data Rates	WE310G4-I RF Output (dBm)	Current mA@3.3V
b	BPSK	1 Mbps	17	243
	QPSK	2 Mbps	17	242
	CCK	5.5 Mbps	17	238
	CCK	11 Mbps	17	232
g	BPSK	6 Mbps	16	212
	BPSK	9 Mbps	16	207
	QPSK	12 Mbps	16	202
	QPSK	18 Mbps	16	197
	16 QAM	24 Mbps	16	192
	16 QAM	36 Mbps	16	177
	64 QAM	48 Mbps	16	170
	64 QAM	54 Mbps	16	165
n	BPSK	MCS0_20	15	202
	QPSK	MCS1_20	15	192
	QPSK	MCS2_20	15	187
	16 QAM	MCS3_20	15	178
	16 QAM	MCS4_20	15	168
	64 QAM	MCS5_20	15	160
	64 QAM	MCS6_20	15	157
	64 QAM	MCS7_20	15	152
	BPSK	MCS0_40	14	192
	QPSK	MCS1_40	14	182
	QPSK	MCS2_40	14	168
	16QAM	MCS3_40	14	162
	16QAM	MCS4_40	13	145
	64QAM	MCS5_40	13	137
	64QUAM	MCS6_40	13	133
	64QAM	MCS7_40	13	130

Table 13: 5 GHz WLAN Continuous Tx Power Consumption

Wi-Fi 5GHz CH100 Standard 802.11x	Modulation	Data Rates	WE310G4-I RF Output (dBm)	Current mA@3.3V
a	BPSK	6 Mbps	13	268
	BPSK	9 Mbps	13	262
	QPSK	12 Mbps	13	257
	QPSK	18 Mbps	13	247
	16 QAM	24 Mbps	13	237
	16 QAM	36 Mbps	13	225
	16 QAM	48 Mbps	13	212
	16 QAM	54 Mbps	13	207
n	BPSK	MCS0_20	13	265
	QPSK	MCS1_20	13	252
	QPSK	MCS2_20	13	242
	16 QAM	MCS3_20	13	232
	16 QAM	MCS4_20	10	207
	64 QAM	MCS5_20	10	197
	64 QAM	MCS6_20	10	193
	64 QAM	MCS7_20	10	188

6.6. SPI Characteristics

The external bus capacitance cannot exceed 15pF when working at the maximum clock of 50MHz.

Timing Diagrams

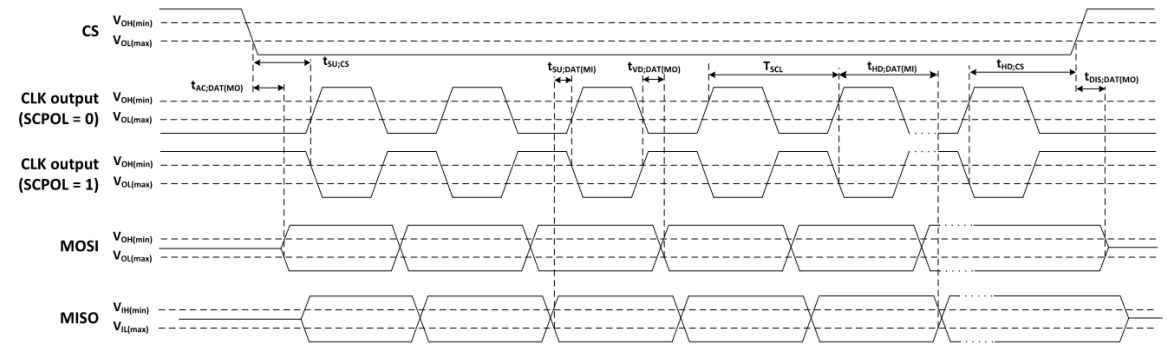


Figure 7: SPI Timing Diagram - Master (SCPH = 0)

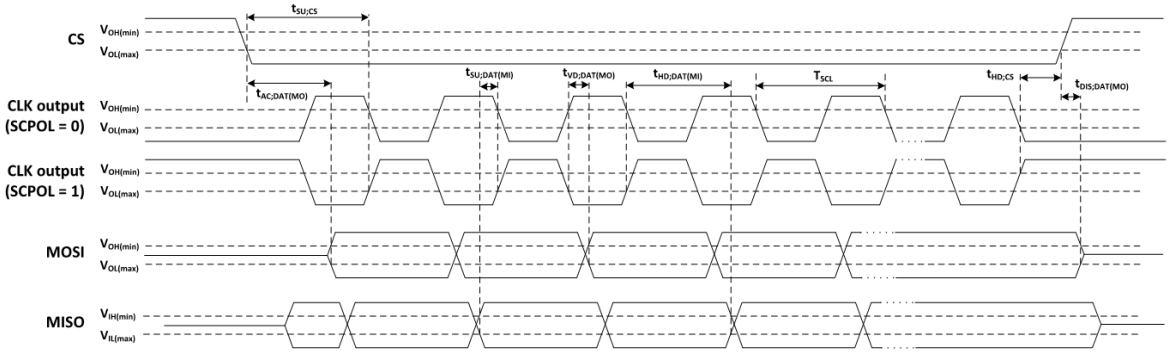


Figure 8: SPI Timing Diagram - Master (SCPH = 1)

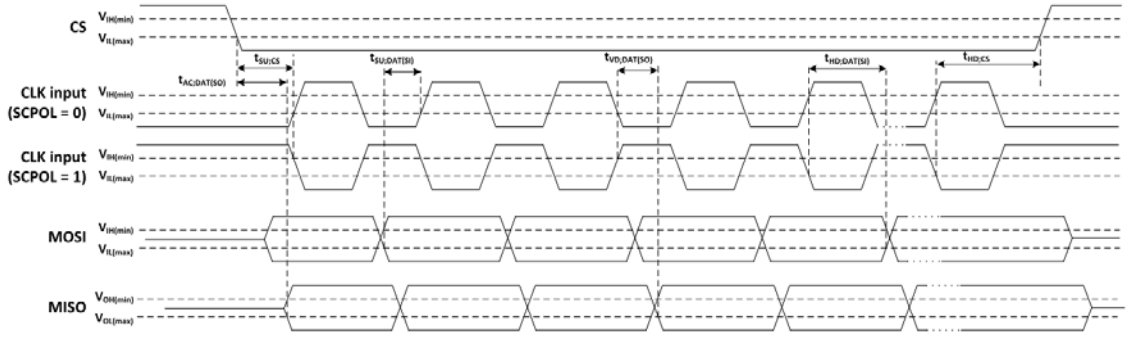


Figure 9: SPI Timing Diagram - Slave (SCPH = 0)

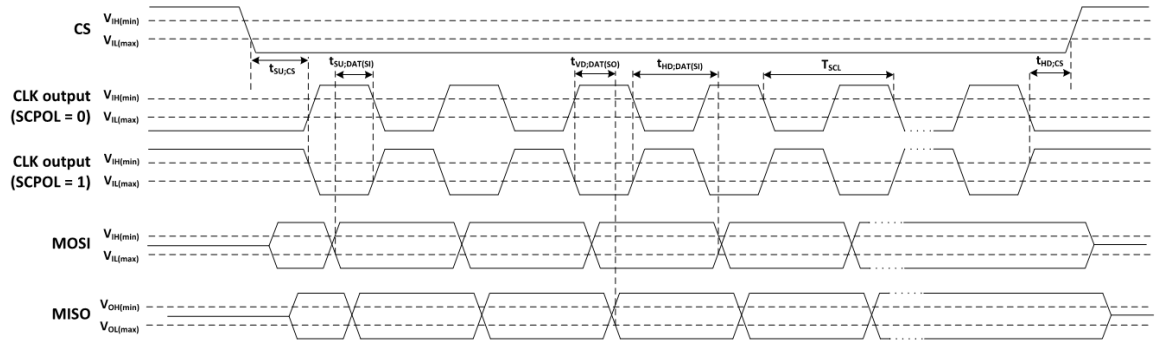


Figure 10: SPI Timing Diagram - Slave (SCPH = 1)

SPI Timing

SPI supports both master mode and slave mode. However, it operates as a slave in the S2W firmware.

Table 14: SPI Timing

Symbol	Parameter	Conditions	Pad(3.3V±10%)		Pad(1.8V±10%)		Unit
			Min	Max	Min	Max	
T_{SCL}	SPI clock period	Master	20	-	20	-	ns
Duty Cycle	SPI duty cycle	Master	45	55	45	55	%
		Slave	30	70	30	70	%
$t_{su;CS(M)}$	CS setup time	Master	30.00	31.10	30.01	31.07	ns
$t_{SU;CS(S)}$		Slave	15	-	15	-	ns
$t_{HD;CS(M)}$	CS hold time	Master	18.90	20.00	18.93	19.99	ns
$t_{HD;CS(S)}$		Slave	18	-	18	-	ns
$t_{AC;DAT(M0)}$/$t_{AC;DAT(SO)}$	Data output access time	Master	20.07	-	20.02	-	ns
		Slave	4.43	-	5.50	-	ns
$t_{VD;DAT(MO)}$/$t_{VD;DAT(SO)}$	Data output valid time	Master	-0.81	-0.23	-0.92	-0.23	ns
		Slave	-	14.57	-	19.54	ns
$t_{SU;DAT(MI)}$/$t_{SU;DAT(SI)}$	Data input setup time	Master	4	-	4	-	ns
		Slave	2	-	2	-	ns
$t_{HD;DAT(MI)}$/$t_{HD;DAT(SI)}$	Data input hold time	Master	2	-	2	-	ns
		Slave	1	-	1	-	ns

7. RF Specification

7.1. Wi-Fi Tx Power

The table below contains the Wi-Fi non-signaling conducted and radiated Tx power. These measurements are performed at room temperature 25 °C @3.3V.
The WE310G4-I column lists the Tx power with its antenna gain of 2.5 dBi for 2.4GHZ and 4.5 dBi for 5GHZ.

Table 15: Wi-Fi Tx Power 2.4 GHz

Wi-Fi 2.4 GHz / CH 1 Standard 802.11x	Modulation	Data Rates	WE310G4-P RF Output (dBm)	WE310G4-I RF Output (dBm)
b	BPSK	1 Mbps	17	19.5
	QPSK	2 Mbps	17	19.5
	CCK	5.5 Mbps	17	19.5
	CCK	11 Mbps	17	19.5
g	BPSK	6 Mbps	16	18.5
	BPSK	9 Mbps	16	18.5
	QPSK	12 Mbps	16	18.5
	QPSK	18 Mbps	16	18.5
	16 QAM	24 Mbps	16	18.5
	16 QAM	36 Mbps	16	18.5
	64 QAM	48 Mbps	16	18.5
	64 QAM	54 Mbps	16	18.5
n	BPSK	MCS0_20	15	17.5
	QPSK	MCS1_20	15	17.5
	QPSK	MCS2_20	15	17.5
	16 QAM	MCS3_20	15	17.5
	16 QAM	MCS4_20	15	17.5
	64 QAM	MCS5_20	15	17.5
	64 QAM	MCS6_20	15	17.5
	64 QAM	MCS7_20	15	17.5
	BPSK	MCS0_40	14	16.5

Table 16: Wi-Fi Tx Power 5GHz

Wi-Fi 5 GHz / CH 100 Standard 802.11x	Modulation	Data Rates	WE310G4-P RF Output (dBm)	WE310G4-I RF Output (dBm)
a	BPSK	6 Mbps	13	17.5
	BPSK	9 Mbps	13	17.5
	QPSK	12 Mbps	13	17.5
	QPSK	18 Mbps	13	17.5
	16 QAM	24 Mbps	13	17.5
	16 QAM	36 Mbps	13	17.5
	16 QAM	48 Mbps	13	17.5
	16 QAM	54 Mbps	13	17.5
n	BPSK	MCS0_20	13	17.5

Wi-Fi 5 GHz / CH 100 Standard 802.11x	Modulation	Data Rates	WE310G4-P RF Output (dBm)	WE310G4-I RF Output (dBm)
	QPSK	MCS1_20	13	17.5
	QPSK	MCS2_20	13	17.5
	16 QAM	MCS3_20	13	17.5
	16 QAM	MCS4_20	10	14.5
	64 QAM	MCS5_20	10	14.5
	64 QAM	MCS6_20	10	14.5
	64 QAM	MCS7_20	10	14.5

7.2. Wi-Fi Rx Sensitivity

Wi-Fi Rx sensitivity at RF pad @ 25 °C.

Table 17: Wi-Fi Rx Sensitivity 2.4 GHz

Wi-Fi 2.4 GHz / CH 6	Modulation	Data Rates	Sensitivity (dBm)
b	BPSK	1 Mbps	-95
	QPSK	2 Mbps	-92
	CCK	5.5 Mbps	-89
	CCK	11 Mbps	-89
g	BPSK	6 Mbps	-92
	BPSK	9 Mbps	-90
	QPSK	12 Mbps	-88
	QPSK	18 Mbps	-87
	16 QAM	24 Mbps	-84
	16 QAM	36 Mbps	-80
	64 QAM	48 Mbps	-76
	64 QAM	54 Mbps	-75
n	BPSK	MCS0_20	-90
	QPSK	MCS1_20	-89
	QPSK	MCS2_20	-87
	16 QAM	MCS3_20	-84
	16 QAM	MCS4_20	-81
	64 QAM	MCS5_20	-76
	64 QAM	MCS6_20	-75
	64 QAM	MCS7_20	-73

Table 18: Wi-Fi Rx Sensitivity 5 GHz

Wi-Fi 5 GHz / CH 36	Modulation	Data Rates	Sensitivity (dBm)
a	BPSK	6 Mbps	-93
	BPSK	9 Mbps	-92
	QPSK	12 Mbps	-91
	QPSK	18 Mbps	-88
	16 QAM	24 Mbps	-85
	16 QAM	36 Mbps	-82
	64 QAM	48 Mbps	-77
	64 QAM	54 Mbps	-75

Wi-Fi 5 GHz / CH 36	Modulation	Data Rates	Sensitivity (dBm)
n	BPSK	MCS0_20	-93
	QPSK	MCS1_20	-90
	QPSK	MCS2_20	-87
	16 QAM	MCS3_20	-84
	16 QAM	MCS4_20	-81
	64 QAM	MCS5_20	-76
	64 QAM	MCS6_20	-75
	64 QAM	MCS7_20	-73

7.3. BLE Tx Power

The following table lists the BLE conducted Tx power at the RF pad of the WE310G4-P module at 25°C @3.3V power supply. To calculate the radiated RF power, the user shall consider the antenna gain. For example, the WE310G4-I has an antenna gain of 2.5dBi, therefore the resultant BLE Tx power is 7.5dBm.

Table 19: BLE Tx Power

Packet Type CH 19	Output Power (dBm)
LE 1M	5
LE 2M	5

7.4. BLE Rx Sensitivity

BLE Rx sensitivity at RF pad @ 25 °C.

Table 20: BLE Rx Sensitivity

Packet Type CH 19	Rx Sensitivity (dBm)
LE 1M	-97
LE 2M	-94

8. Design Guidelines

8.1. General Digital Interface Recommendations

There are two UARTs in WE310G4, intended to be used as explained below.

1. UART0 is for AT commands and responses for application use. Baud rate supported 300 ~ 921600 (default baud 115200). HW flow control is supported.

   Note: Total baud rate error shall be less than 3% to communicate correctly.

2. AUX UART (also referred to as UART1) is for flashing, RF Tests, and debug logs (can't be turned off). Do not use this port for AT commands. Doesn't support HW flow control.
   - Program Mode: Fixed baud rate is 1.5 Mbps.
   - Run Mode: Fixed baud rate is 115200 bps.
3. WE310G4 module is shipped with the default firmware, developers often need to flash the module during development. We recommend having an option for flashing the module. This is a generic requirement during production and certification. TX_AUX pin (Y10) is the Program/Run mode pin. This pin state must be LOW to place WE310G4 in program mode.

A sample circuit is shown below:

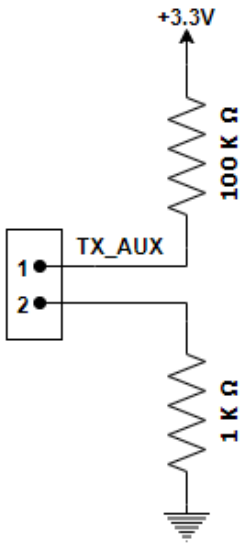


Figure 11: Sample Circuit for Program/Run mode

Telit recommends a voltage translator if the components/peripherals interfacing with WE310G4-I/P have different digital logic levels other than 3.3V.

Using voltage translator components in your design makes the system ready for operation at the full VIO voltage range, 3.3V to system I/O voltage. However, using a resistor divider and/or emitter follower circuits, as voltage translators does not protect the module against latch-up. Furthermore, you cannot guarantee a constant voltage on the divider net.

The use of open collector buffers or bi-directional voltage level translators with unidirectional signals is correct, but they suffer from some RF noise, and they are dependent on pull-ups/Downs on the two sides of the voltage translator.

Some translators operate with different power ranges on the two sides: pay attention to the direction in this case.

In general, we recommend unidirectional level shifters but if bi-directional buffers are preferred, please consider those that require external PU/PD instead of having embedded PU/PD circuitry. Some brands that we recommend:

1. Texas Instruments TXS series
2. NXS NVT200x series

If the system includes a cellular module, consider adding some bypass capacitors to the supply lines of the voltage level translators to protect RF signals.

For bypass use 33pF for the 0402 packages or 56pF, when you use 0201. For example, SN74AVC2T245, SN74AVC4T774, or SN74LVC2T45, for 5V signals.

Moreover, while using level shifters for better testability, it is recommended to use those having OE pins. Test pulling the "EN" lines of the level shifts with the addition of a 10K resistor to GND or VCC, depending on the level shifter used. This will create access points that would put shifts in tri-state and can be conveniently used for testing and firmware updates originating from external serial ports such as a PC.

It is recommended to connect the WE310G4-I/P ON* (N16 pin) to control the Enable pin of the level shifter, in this way a tri-state will be guaranteed during BOOT.

8.2. Power supply design guidelines

We recommend adding an external EMI filter to improve the quality of the power supply especially when the module will be embedded with other technologies, (such as Cellular).

The pi-greca filter composed of ferrite bead and 10pF capacitors (C2, C3) is used to provide a high impedance value for high-frequency signals, while the 100uF and 22uF capacitors (C1. C5, and C4) are used to bypass low frequencies from switching regulator circuit and to provide a supply tank for high current absorption

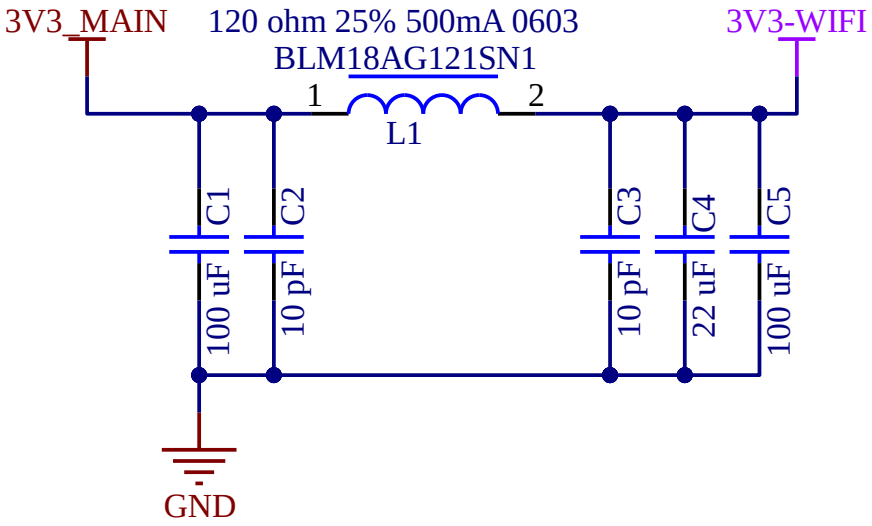


Figure 12:Telit WE310G4 EMI Filter Example Circuit

The figure above shows an example circuit with the minimum allowable capacitor values.

Table 21: Power Supply Requirements

Power Supply	Minimum	Typical	Maximum
Main Power ratings	3.0 V	3.3V	3.6 V

Note: The hardware shutdown voltage of the module is 3.0V. If the voltage drops below 3.0V, the module will be shut down. The Extreme Operating Voltage Range MUST never be exceeded.

If the power supply is not properly designed, it can cause a large voltage drop.

8.3. Bypass Capacitors

To improve the harmonic filtering, we recommend adding bypass capacitors, close to:

1. Power Sources and signals on input-output connectors
2. At power supply output PADs.
3. At the component's power supply input PADs (even if shielded).
4. Diodes in forwarding conduction, like LEDs, on the anode and/or cathodes if not directly tied to a power net.
5. Transistor bases, mainly for bipolar ones, phototransistors, and opto-isolator
6. Analog microphone pads.
7. Operational Amplifiers Inputs and Supplies.

The bypass capacitors should have a self-resonant frequency close to the frequency generated on your board or transmitted from the boards that will operate in the same environment in which your board operates.

For example, to effectively filter the Wi-Fi RF bands, these small signal capacitors must have a self-resonant (SRF) at about 2.4 GHz. For example, capacitor values, depending on manufacture and its mechanical dimensions should be around 10pF, in general by reducing the packaging size you will need to increase the capacitance value. Please carefully check the datasheet to find the proper component suitable for this purpose.

Another example is for GSM, in general, you can use 33pF 0402 or 56pF 0201

8.4. General Design Rules

The WE310G4-I has an embedded ceramic antenna. To preserve the bandwidth, keep attention to not place any copper or mechanical component in front or close to the ceramic antenna.

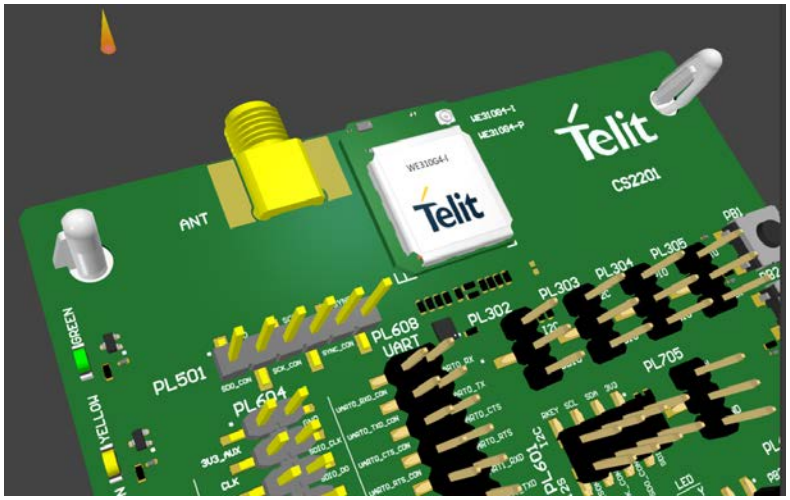


Figure 13: WE310G4-I Placement Example

- For the WE310G4-I version the antenna is placed directly on the board, so you will need to leave a copper keep-out area as shown below:

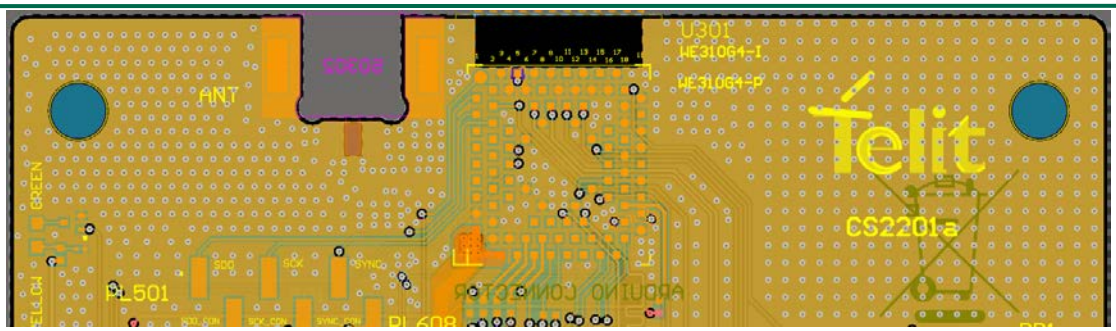


Figure 14: WE310G4-I Placement Example Showing No Copper in all Layer Of The Board

- To avoid Antenna detuning, remove the copper shielding in this area in all layers keeping only FR4.
- For WE310G4-P you will need to use an external antenna connected to the antenna pad of the module, such as an SMA connector as shown in the figure below.

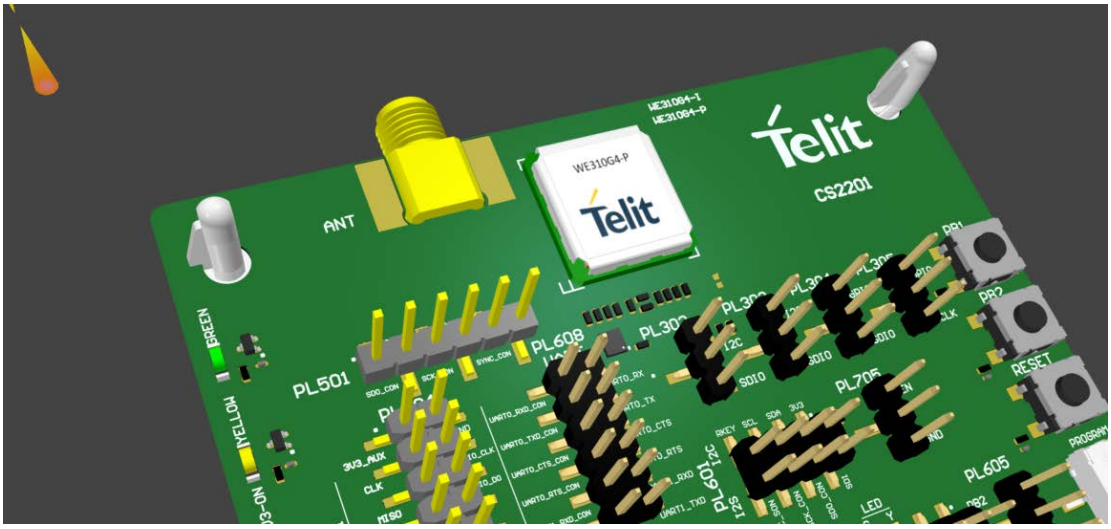


Figure 15: WE310G4-P Placement

In this case, considering the position of the external antenna concerning other boards is very important. The conductive planes close to the antenna can modify the impedance seen by the antenna or detune it.

- The WE310G4-P module provides a 50Ω antenna pad, which needs to be routed to the antenna connector (or the integrated antenna) with a transmission line
- Please keep as close as possible to 50Ω impedance in the RF track, including the RF Pad.
- To avoid step impedance, try to draw the RF trace as much as possible to the pad with the matching components.

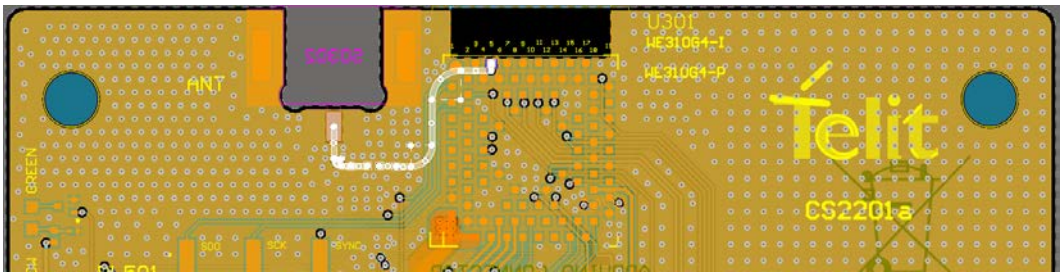


Figure 16: RF Track Example

- To have a good impedance control consider using a Grounded coplanar waveguide structure (G-CPW) line.

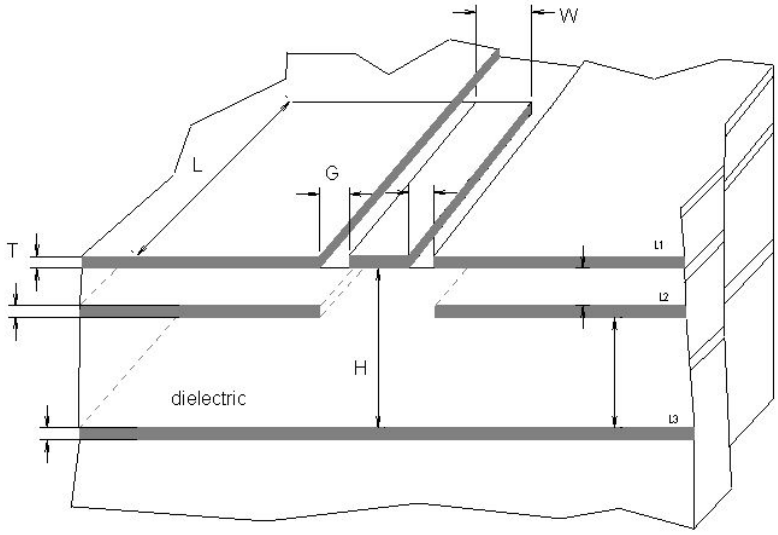


Figure 17: Coplanar Waveguide Dimensioning Example

The final dimensions depend on the use of stack-up. While the WE310G4-I is already tuned to the embedded antenna, the WE310G4-P version needs to be tuned in relationship to the stack-up used.

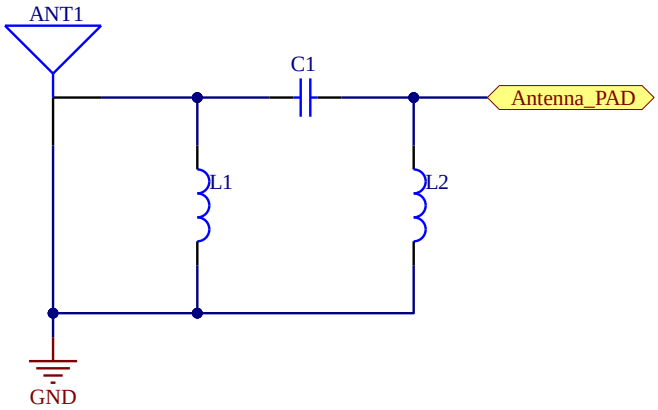


Figure 18: Minimal RF Matching Network Circuitry

A possible network topology is seen in the above figure, and it consists of three passive components.

To reuse Telit's FCC certification for our module, the antenna on the application board shall have a gain of 2.5dBi @2.4GHz band and 4.5dBi @5GHz band. The separation distance between the user and/or bystander and the device's radiating element must be greater than 20cm and no other radiating element must be present inside the application closer than 20cm to our antennas. However, a separate test for any other radiating element could be necessary.

For an external antenna, it is recommended to use a dipole antenna GW.11. A113 from Taoglass.

8.5. Audio

The digital audio data interface supports I2S. Since many external processors and applications have fast transient signals, it is recommended to add an RC filter on all DVI lines (R~22Ohm and C~10nF). If the DVI lines, I2S, are run on external layers RF may disturb the lines, to resolve this, add in parallel, to 10nF, another capacitor of about 10pF to 33pF.

8.6. Audio Considerations

Since, components and PCBs are getting smaller while the component's density increases, another problem that becomes important is heat dissipation.

For that reason, pay special attention to the PCB stack-up and component placement. The following PCB design rules will help RF immunity and improve heat dissipation.

1. Use at least six layers of PCB technology.
2. Layer 2 and Layer 4 should be mainly ground.
3. On top of Layer 1 and at the bottom of Layer 6, a place mainly ground plane interrupted just by component pads and RF antenna tracks.
4. Minimum tracks connecting Layer3 to Layer5. This is done to avoid ground interruption and heat dissipation.
5. Use Layer3 and Layer5 only for signals, where power lines are wider tracks and surrounded by ground to reduce the risk of crosstalk with other signals.
6. Use one layer for horizontal lines only, and another one for vertical lines. Fill the remaining space with the ground.
7. Use several vias to connect all ground planes and areas in all layers with possible through-hole drills.
8. Place warmer components on the PCB side facing up and do not place anything near them, leaving space for air.
9. If it is a closed application, consider opening holes on the top and bottom of the cover for ventilation.

It is recommended to use 4 layers only if the number of interconnections gives you the possibility to route them on layer 2 and layer 3 in a way that power lines and signal lines do not intersect, and the module is operating continuously so heat dissipation is not a must. All the rest suggestions described above must be fulfilled.

The audio, USB, and ADC lines must be routed avoiding intersections with any other signal.

The top and bottom layers should be mainly a ground plane interrupted just by the component's pads, vias, and RF tracks. Connect all ground areas avoiding isolated islands with several vias. In this way, the signal tracks are more protected from picking up RF due to the Faraday-Cage effect. Long exposed tracks can easily pick up RF power and especially in your case with many RF power sources you can generate high-frequency intermodulation harmonics that the same exposed tracks can then irradiate very efficiently.

The PCB outline should be surrounded by GND vias interconnected from TOP to Bottom.

We also recommend filling the free space in the inner layers with the ground.

Pay attention to interconnecting all the ground areas or planes to guarantee a strong equipotential node. Remove dead copper areas and net antenna tracks or vias.

It is recommended to bury in inner layers:

1. Analog or digital audio lines.
2. Memory address and data bus.

3 Fast digital signals like SPI or SDIO, clocks, and quartz.

4 USB and long serial.

The following figure shows an example of fast signal track routing. In this example, the tracks are routed in an inner layer and surrounded by GND and GND vias to be shielded. If possible, try to shield with GND areas above and below areas.

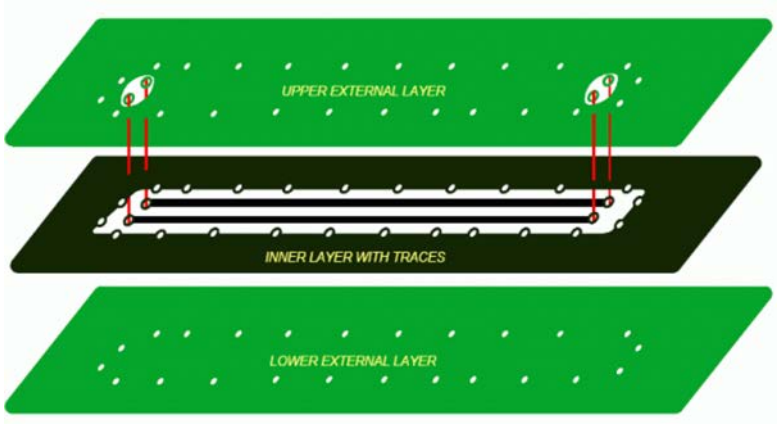


Figure 19: Layout Example for FAST Digital Lines

Lines to resolve this, add in parallel, to 10nF, another capacitor of about 10pF to 33pF.

8.7. ESD Characteristics

Refer to the table below for the ESD characteristics of the WE310G4-I/P modules.

Table 22: ESD Characteristics

ESD	Voltage
Human Body Model (HBM)	±2000
Charge Device Model	± 500

9. Mechanical Design

9.1. WE310G4-I

The following is the Top and bottom view of the Telit WE310G4-I module.

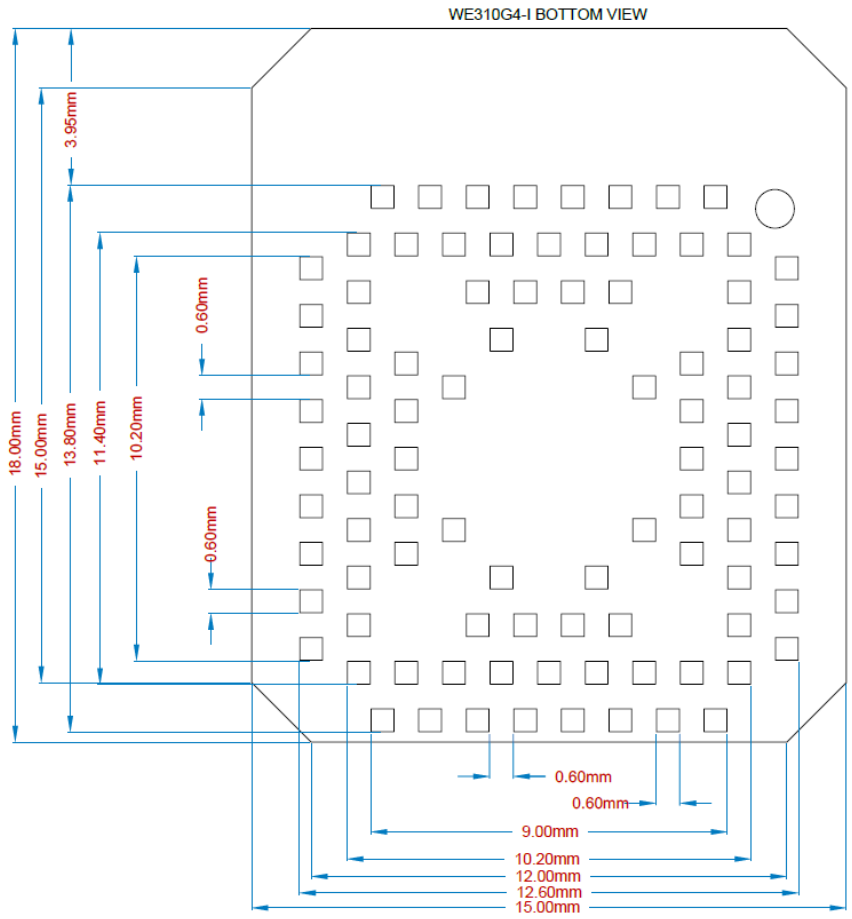


Figure 20: WE310G4-I Bottom View

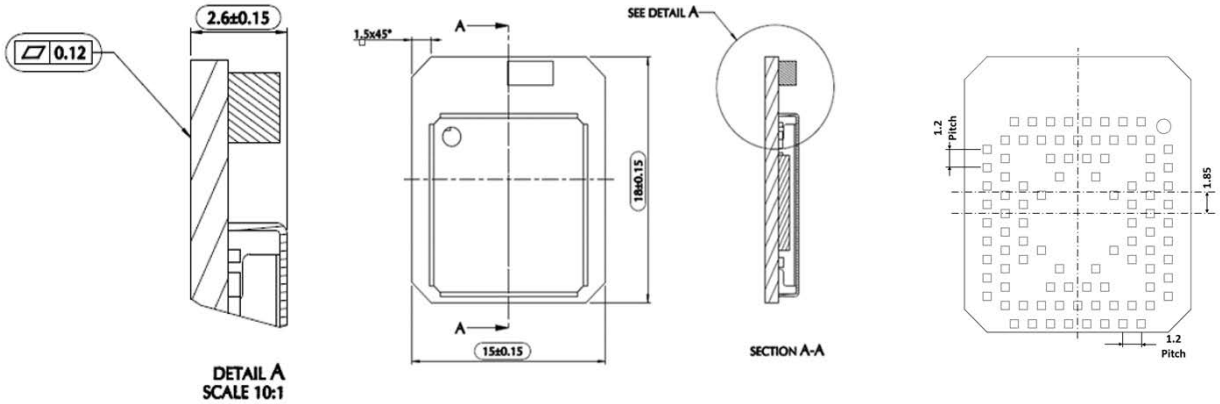


Figure 21: WE310G4-I Sides View and Mechanical Design

9.2. WE310G4-P

The following is the Top and bottom view of the Telit WE310G4-P module.

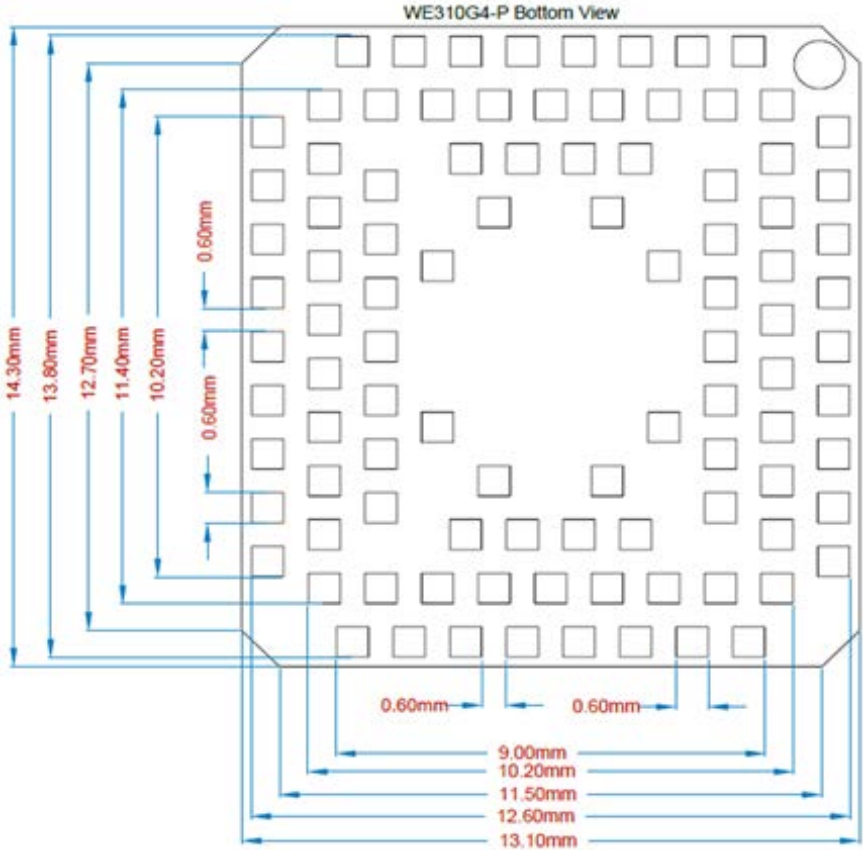


Figure 22: WE310FG4-P Bottom View

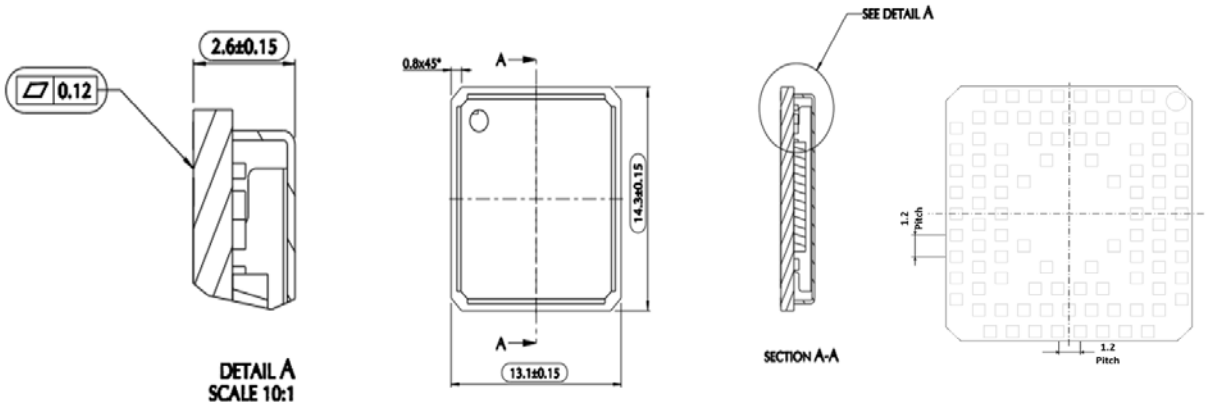


Figure 23: WE310G4-P Side View and Mechanical Design

9.3. PCB Pad Design

For the solder pads, it is recommended to use a Non-Solder Mask Defined pad (NSMD) on the PCB.

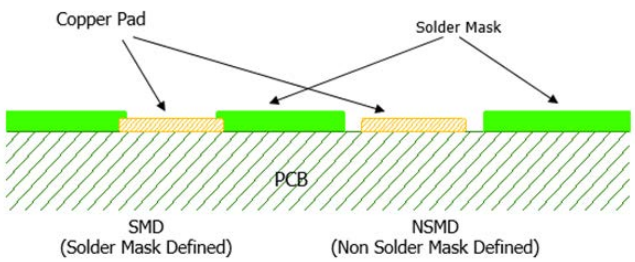


Figure 24: SMD and NSMD Pad

9.4. PCB Pad Dimensions

It is not recommended to place via or micro-via not covered by the solder resist in an area of 0.3 mm around the pads unless it carries the same signal as the pad itself as shown below.

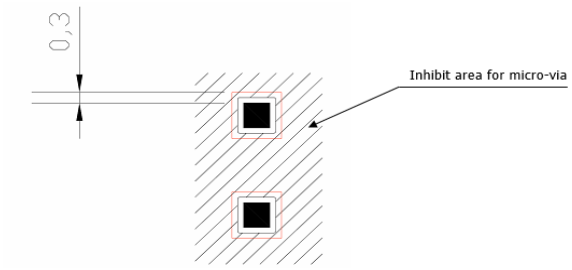


Figure 25: Inhibit Area for Not Solder Covered Vias

The holes in the pad are allowed only for blind holes and not for through holes. The following table shows the recommended PCB pad surfaces.

Table 23: PCB Finishing Recommendation

Finish	Layer thickness [µm]	Properties
Electroless Ni / Immersion Au	3 –7 / 0.03 – 0.15	Good solderability protection, high shear force values

The PCB must be able to resist the higher temperatures that can occur during the lead-free process. This issue should be discussed with the PCB supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.

It is not necessary to panel the application PCB. However, it is recommended to use milled contours and predrilled board breakouts; scoring or v-cut solutions are NOT recommended.

9.5. Stencil

The Stencil's aperture layout can be the same as the recommended footprint (1:1). It is recommended to use a stencil foil with a thickness ≥ 120 µm.

9.6. Solder Paste

Table 24: Recommended Solder Paste Type

Component	Lead-free
Solder paste	Sn/Ag/Cu

To avoid or minimize the cleaning efforts after assembly, it is recommended to use a "no-clean" solder paste.

9.7. PCB Pad Dimensions

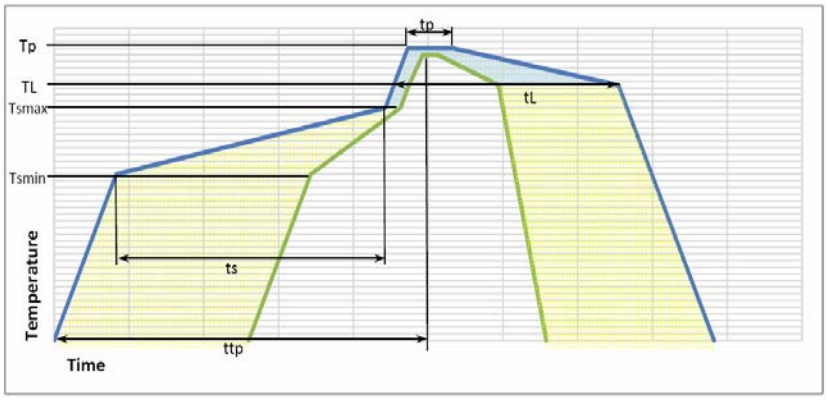


Figure 26: Solder Reflow Profile

Table 25: Solder Reflow Specification

Profile Feature	Pb-Free Assembly
Average ramp-up rate (TL to Tp)	3 °C/second max.
Preheat Temperature Min. (Tsmin) Temperature Max. (Tsmax) Time (min to max) (ts)	 150 °C 200 °C 60-180 seconds
Tsmax to TL Ramp-up rate	 3 °C/second max
Time maintained above Temperature (TL) Time (tL)	 217 °C 60-150 seconds
Peak temperature (Tp)	245 +0/-5 °C
Time within 5 °C of the actual peak temperature (tp)	10-30 seconds
Ramp-down rate	6 °C/second max.
Time 25 °C to peak temperature	8 minutes max.

Note: All temperatures refer to the topside of the package, measured on the package body surface t.

Danger: The WE310G4-I/P module withstands only one reflow process.

The above solder reflow profile represents the typical SAC reflow limits and does not guarantee adequate adherence of the module to the customer application throughout the temperature range. The customer must optimize the reflow profile depending on the overall system considering such factors as thermal mass and warpage.

10. Packaging

10.1. Tray

The WE310G4-I/P modules are packaged on trays of 50 pieces each when small quantities are required (that is, for test and evaluation purposes).

These trays are not designed for use in SMT processes for pick and place handling.

The following is the packaging process:

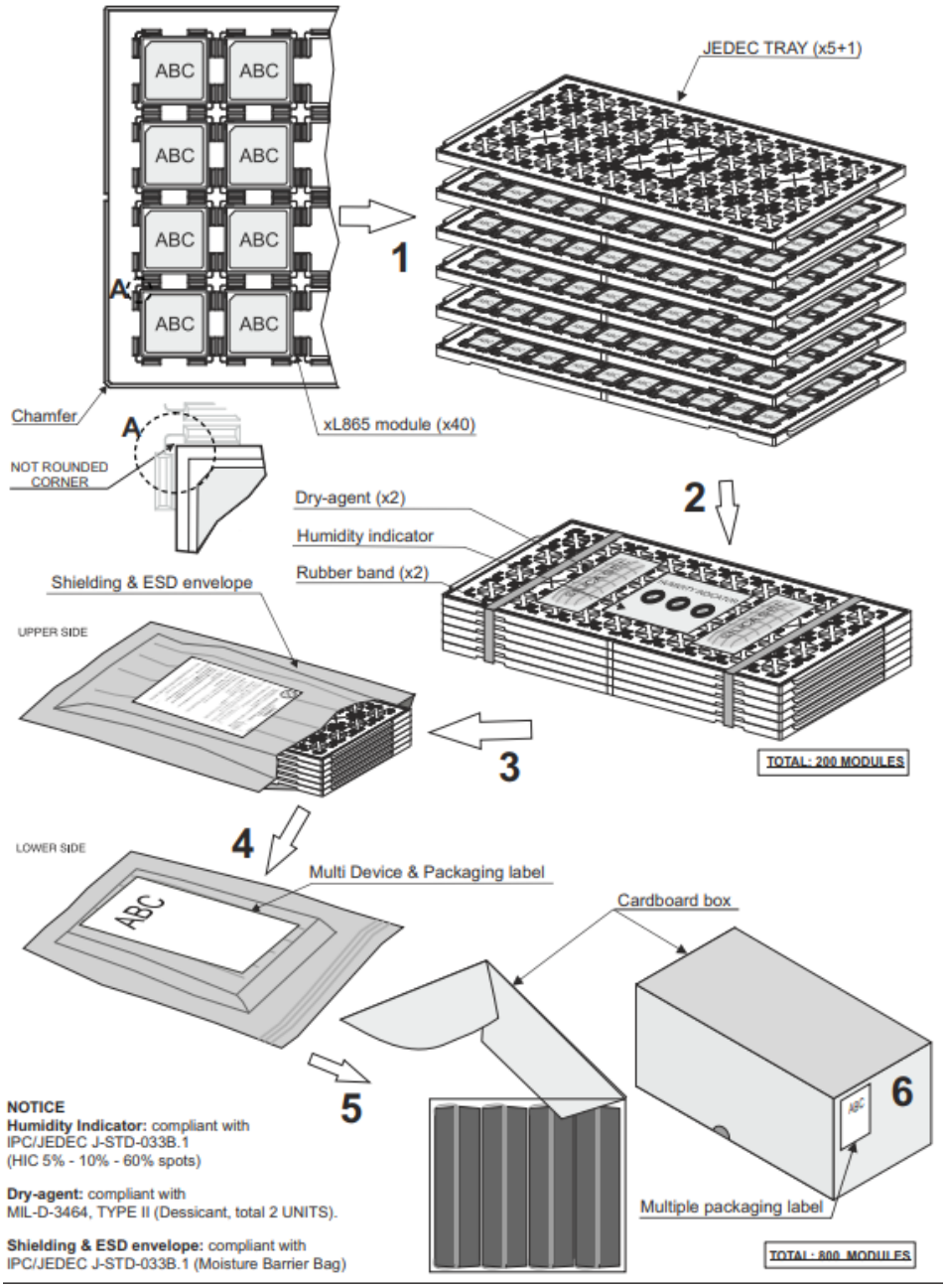


Figure 27: WE310G4-I/P Packaging example

Danger: The maximum temperature for these trays shall not exceed 65°C.

10.2. Moisture sensitivity

The WE310G4-I/P module is classified as a LEVEL 3 moisture-sensitive device following IPC/JEDEC J-STD-020.

Moreover, the customer must take care of the following conditions:

1. The shelf life of the product inside the dry bag is 12 months starting from the bag seal date when stored in a non-condensing atmospheric environment of < 40°C and < 90% relative humidity (RH).
2. An environmental condition during the production: <= 30°C / 60% RH according to IPC/JEDEC J-STD-033B.
3. The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition b) “IPC/JEDEC J-STD-033B paragraph §5.2” is respected.
4. Baking is required if conditions b) or c) are not respected
5. Baking is required if the humidity indicator inside the bag indicates 10% RH or more.

11. Conformity Assessment Issues

11.1. Approvals

Table 26: Approvals Summary

Module	Europe RED / UKCA	US FCC	CA ISED
WE310G4-I	Yes	Yes	Yes
WE310G4-P	Yes	Yes	Yes

11.2. Europe Approvals

RED Declaration of Conformity

Hereby, Telit Communications S.p.A declares that the WE310G4-I and WE310G4-P Modules comply with Directive 2014/53/EU.

The full text of the EU Declaration of Conformity is available at the following internet address: https://www.telit.com/red/

Text of 2014/53/EU Directive (RED) and UKCA requirements can be found here:

https://eur-lex.europa.eu/legal-content/EN/TXT/?uri=CELEX:32014L0053

UKCA Declaration of Conformity

Hereby, Telit Communications S.p.A declares that the WE310G4-I and WE310G4-P Modules comply with the d Radio Equipment Regulations 2017 for UKCA.

The full text of the UKCA declaration of conformity is available at the following internet address: https://www.telit.com/ukca

The UKCA requirements can be found here:

https://www.gov.uk/guidance/using-the-ukca-marking

RED / UKCA Antennas

This radio transmitter has been approved under RED / UKCA to operate with the antenna types listed below with the maximum permissible gain indicated. The usage of a different antenna in the final hosting device may need a new assessment of the host's conformity to RED / UKCA.

Table 27: RED / UKCA Antenna Type

Model	Antenna Type
WE310G4-I	Omnidirectional Dipole Antenna
WE310G4-P	

11.3. FCC/IC Regulatory Notices

Hereby, Telit Communications S.p.A declares that the WE310G4-I/P Module is following Directive 2014/53/EU.

The full text of the EU Declaration of Conformity is available at the following internet address: https://www.telit.com/red

11.4. FCC/IC Compliance

Modification Statement

Telit has not approved any changes or modifications to this device by the user. Any changes or modifications could void the user's authority to operate the equipment.

Telit n'approuve aucune modification apportée à l'appareil par l'utilisateur, quelle qu'en soit la nature. Tout changement ou modification peuvent annuler le droit d'utilisation de l'appareil par l'utilisateur.

Interference Statement

This device complies with Part 15 of the FCC Rules and Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions:

1. This device may not cause interference, and
2. This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

1. l'appareil ne doit pas produire de brouillage, et
2. l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Wireless Notice

This device complies with FCC/ISED radiation exposure limits set forth for an uncontrolled environment and meets the FCC radio frequency (RF) Exposure Guidelines and RSS-102 of the ISED radio frequency (RF) Exposure rules. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter. The antenna should be installed and operated with a minimum distance of 20 cm between the radiator and your body.

Le présent appareil est conforme à l'exposition aux radiations FCC / ISED définies pour un environnement non contrôlé et répond aux directives d'exposition de la fréquence de la FCC radiofréquence (RF) et RSS-102 de la fréquence radio (RF) ISED règles d'exposition. L'émetteur ne doit pas être colocalisé ni fonctionner conjointement avec à autre antenne ou autre émetteur. L'antenne doit être installée de façon à garder une distance minimale de 20 centimètres entre la source de rayonnements et votre corps.

FCC Class B Digital Device Notice

This equipment has been tested and found to comply with the limits for a Class B digital device, according to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used following the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or

television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment to an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

CAN ICES-3 (B) / NMB-3 (B)

This Class B digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de classe B est conforme à la norme canadienne ICES-003.

List of Applicable FCC rules

Parts 15C, 2.1091

Limited Module Procedures

N/A

Trace Antenna Designs

See 7.4 Antenna design

Antennas

This radio transmitter has been approved by FCC and ISED to operate with the antenna types listed below with the maximum permissible gain indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Type Max Gain

Omnidirectional 2.5dBi@2.4GHz band and 4.5dBi@5GHz band.

Le présent émetteur radio a été approuvé par ISDE pour fonctionner avec les types d'antenne énumérés ci-dessous et ayant un gain admissible maximal. Les types d'antenne non inclus dans cette liste, et dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

Type Gain Maximal

Omnidirectional 2.5dBi@2.4GHz band and 4.5dBi@5GHz band.

Label and Compliance Information

The product has FCC ID and ISED label on the device itself. Also, the OEM host product manufacturer will be informed to display a label referring to the enclosed module. The exterior label will read as follows:

Contains TX FCC ID: RI7WE310G4

Contains IC: 5131A-WE310G4

Information on Test Modes and Additional Testing Requirements

The module has been evaluated in mobile stand-alone conditions. For different operational conditions from a stand-alone modular transmitter in a host (multiple, simultaneously transmitting modules or other transmitters in a host), additional testing may be required (collocation, retesting...).

If this module is intended for use in a portable device, you are responsible for separate approval to satisfy the SAR requirements of FCC Part 2.1093 and IC RSS-102.

Additional Testing, Part 15 Subpart B Disclaimer

The modular transmitter is only FCC-authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and the host product manufacturer is responsible for compliance with any other FCC rules that apply to the host not covered by the modular transmitter grant of certification.

If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed. The end product with an embedded module may also need to pass the FCC Part 15 unintentional emission testing requirements and be properly authorized per FCC Part 15.

12. Acronyms and Abbreviations

Table 28: Acronyms and Abbreviations

Acronym	Definition
ADC	Analog – Digital Converter
BLE	Bluetooth low energy
CLK	Clock
DAC	Digital – Analog Converter
GPIO	General Purpose Input Output
HS	High Speed
I/O	Input Output
MISO	Master Input – Slave Output
MOSI	Master Output – Slave Input
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
RTC	Real-Time Clock
SDIO	Secure Digital Input Output
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
WLAN	Wireless LAN

13. Related Documents

Refer to https://dz.telit.com/ for current documentation and downloads.

Table 29: Related Documents

S.no	Book Code	Document Title
1	80704ST11102A	WE310G4-I/P AT Command Reference Guide
2	1VV0301775	WE310G4-IP Evaluation Board Quick Start Guide

14. Document History

Table 30: Document History

Revision	Date	Changes
9	2023-11-08	Added SPI Characteristics Updated Wi-Fi Tx Power WE310G4-I RF Output (dBm) Updated BLE Tx Power Power up, Power off, and Reset sequence Updated dBi and band frequency
8	2023-07-12	Updated IO4 function on Table 3, Table 4, and Table 5. Added Pin-Out Reserved Table values E4, E16, U4, and U16 R-Key location updated in figure Telit WE310G4-I Pads Layout Top View R-Key location updated in Telit WE310G4-P Pads Layout Top View Updated figure WE310G4-I Side View and Mechanical Design with R-Key location Updated figure WE310G4-P Side View and Mechanical Design with R-Key location
7	2023-02-08	BLE was replaced with Bluetooth® Low Energy and BT was replaced with Bluetooth® wireless technology
6	2023-01-02	Updated Logic Level and Timing Specification of -Power up/shutdown sequence table
5	2022-08-26	Overview content update Main features content update Sample circuit image update
4	2022-07-27	Image updates in the RF Track Example section.
3	2022-07-12	Image updates in the General Design Rules section.
2	2022-05-17	Image updates in the General Design Rules section.
1	2022-05-11	Average Power Consumption table update.
0	2022-03-31	Preliminary Release.

From Mod.0818 Rev.11

Technical Documentation