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ANALYSIS, DESIGN OF A 500 ZERO VOLTAGE SWITCHING PHASE-SHIFTED FULL-BRIDGE DC/DC CONVERTER BASED POWER SUPPLY

BY

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Introduction

1.1 Project Objectives

The project is aimed at coming up with specification design and analysis of a high efficient 500W DC/DC converter for 24V systems. My design uses a 700V accumulator as the input and outputs a regulated 24V that can be used to power high voltage DC equipments. A switched mode Phase shifted Zero Voltge or Soft Switching full bridge DC/DC converter was designed taking into considerations the appropriate trade offs in terms of cost, losses and reliability.

1.2 Switched mode power supply (SMPS)

DC voltage power supplies are utilized in most electrical/electronic equipment in order to meet the power requirement of the electronic circuits in the equipment. The power supply used to obtain regulated DC voltage from AC power line may be either a linear regulator or a Switch Mode Power Supply (SMPS).

Linear regulators may be convenient for the power supply applications where the unregulated input voltage is close to and more than the desired regulated output voltage since inefficiency is the main drawback of these type of regulators. The low noise level and simplicity are the two advantages of the linear regulators.

The SMPS technology offers several advantages over the linear regulator technology such as higher efficiency, higher bandwidth (better regulation), smaller size, an lower weight. The semiconductor switching device in an SMPS is operated either in cut-off mode (blocking high voltages) or saturation mode (carrying high currents). Since no current flows through the semiconductor switch in cut-off (off) state and the voltage across the device is low in saturation (on) state, the conduction power loss is low. Likewise, the very high speed switching nature of the power semiconductors leads to low switching losses. Thus, the low conduction and switching losses result in higher efficiency of SMPSs than linear regulators. An SMPS regulates the output voltage closely in spite of the changes in the input supply voltage and the load current, with almost no change in efficiency. Due to the high operating switching frequencies of the semiconductor switching devices; transformers, inductors, and capacitors utilized in an SMPS are getting smaller in size and lower in weight which results in smaller, lighter, and more economical power supplies.

Generally an SMPS system consists of the basic elements presented in the block diagram in Figure 1.1 . In an SMPS, when the unregulated input voltage is supplied from the AC grid, typically, the AC line voltage that is either single-phase or three-phase is rectified to DC voltage by a diode bridge rectifier. The diode bridge output voltage is filtered by a large electrolytic capacitor so that ripple voltage magnitude of the unregulated DC voltage is reduced. The heart of an SMPS system is formed by a switch mode DC/DC converter that outputs regulated DC voltage. The DC/DC converter block mainly utilizes power semiconductor devices (switches), passive filter components, and an isolation transformer when galvanic isolation is necessary. The power semiconductor devices may be either gate controlled switching devices including Bipolar Junction Transistors (BJTs), Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), Insulated Gate Bipolar Transistors (IGBTs) or uncontrolled (naturally commutated) devices which are power diodes. The passive components are utilized either for AC voltage and current conversion with isolation (transformers) or for energy storage (inductors and capacitors). The output sensor and controller block consists of measurement and control circuits. The measured DC/DC converter circuit variables such as load voltage, load current and input unregulated DC voltage are scaled and input to the controller for feedback purpose in order to regulate the output. The controller of the DC/DC converter can be implemented either by analog/digital hardware or by digital software. The control method is determined by utilizing the desired specifications of the system. An analog/digital hardware implementation has the main advantage of rapid response at the output to a change in the line or load due to the continuous sampling and processing. However, digital software implementations increase flexibility while eliminating the dependence on environmental effects and aging, and reducing the amount of external hardware

components. Complex control algorithms can also be implemented using digital software controllers in a simpler manner. The controller generates control signals for the Pulse Width Modulation (PWM) block which outputs the gate signals of the controllable semiconductor switch

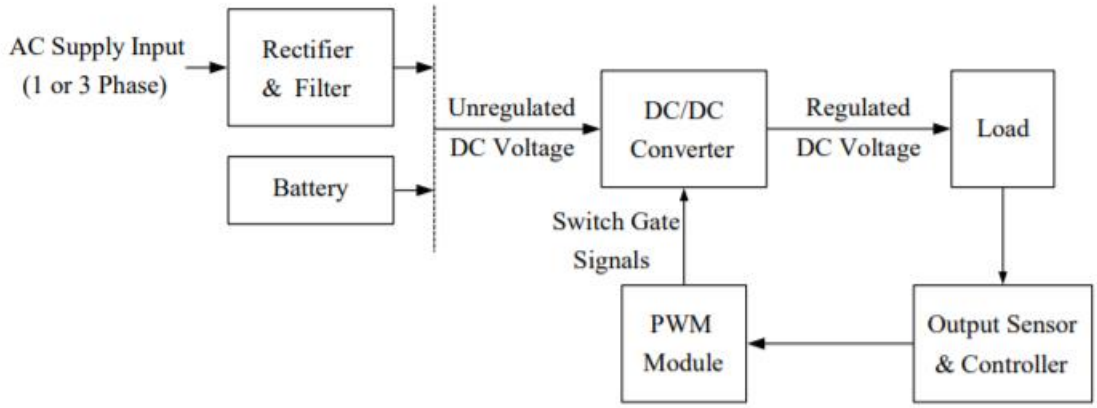

Figure 1.1 Generalized block diagram of an SMPS system.

The circuit topology of the switch mode DC/DC converter fully defines its functional attributes and performance . There are various types of DC/DC converter circuit topologies utilized in SMPSs based on the system requirements such as input to output voltage relationship, power rating, and the need for galvanic isolation. The simplest and most basic two DC/DC converter topologies are the step-down and step-up converters. All DC/DC converter topologies can be derived from these two. Derived from these, are the widely utilized single-switch flyback and forward converters that have electrical isolation between the input and output. Such converters are typically utilized at low power (much less than a kilowatt) and in low cost applications. At higher power, voltage, or current ratings more complex power converters become necessary. The half-bridge and full-bridge DC/DC converters which are derived from the step-down converter are the highest performance converters. When galvanic isolation and/or a significant voltage/current level change are required, these converters are accompanied with an isolation transformer also.

Switch mode DC/DC power supplies can be operated at high switching frequencies due to the advances in semiconductor technology providing fast switches with small rise and fall times yielding high frequency operation with low loss. Due to the high switching frequency operation of the DC/DC power supply, the size and weight of the welding machine can be reduced since the size of magnetic components in the power supply can be made smaller, which results in more light and portable welding machine. In such welding power supplies the size and weight are reduced while the performance is increased, which results in portable welding machines having improved welding quality. Another requirement of the welding power supplies is galvanic isolation between the input and output. Increasing switching frequency also increases the current control bandwidth, which is necessary for high quality weld. The workpiece where the welding action takes place, completes the electric circuit path at the output. For safety reasons, the input supply of the welding machine must be electrically isolated from output, where the arc load exists. Therefore, an isolation transformer must be utilized in the power supply of a welding machine. Since the arc load behaves as a nonlinear resistor, it is also required that the static and dynamic current regulation performance of these DC/DC power supplies must be high for better welding performance.

1.3 The Full-Bridge Phase-Shifted Zero Voltage or Soft Switching DC/DC Converter

The basic configuration of the full-bridge DC/DC converter, which is shown in Figure 1.2, employs a full-bridge inverter, an isolation transformer, and an output rectifier. The full-bridge inverter utilizes fully controllable semiconductor switches and outputs high frequency AC voltage waveform by utilizing the input DC voltage. Then, the inverter output voltage is isolated and scaled (if required) by the high frequency transformer. Following, the transformer output voltage is rectified by the diode bridge rectifier (half-bridge or full-bridge, depending on the application requirements) and finally filtered to provide smooth DC voltage or current. It should be kept in mind that the DC/DC converter system consists of mainly two stages, DC/AC and AC/DC stages. Thus, the name DC/DC converter here is attributed to the system, rather than the individual converter topologies.

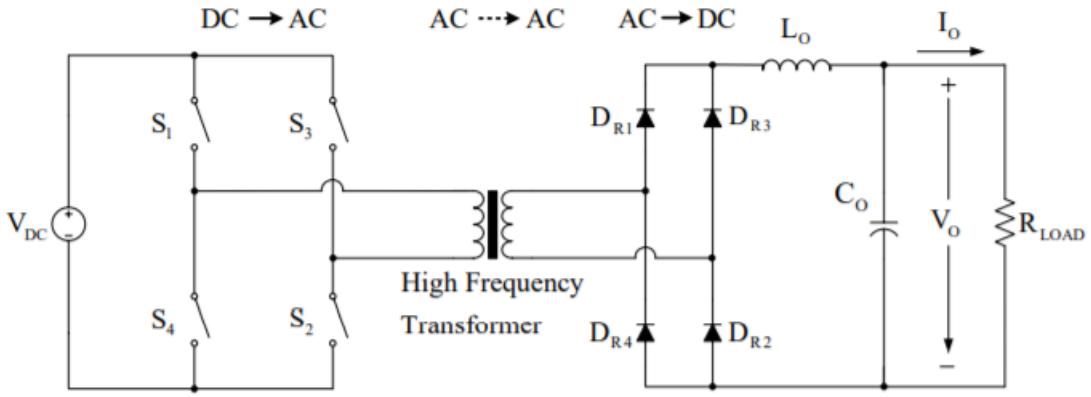

Figure 1.2 The full-bridge DC/DC converter basic circuit configuration.

With no auxiliary components in the converter circuit, the switches are considered to be under hard-switching operating condition, which corresponds to the switch voltage and current simultaneously being large during the switching intervals and implies considerable switching loss and stress on the switching devices. Generally in all hard-switching converters and most practically in high power converters the switching losses are a major limiting factor on the switching frequency. In order to maintain a high energy efficiency and acceptable cost in the converter, the switching frequency is confined to a practically acceptable range. The reduced switching frequency results in larger passive components (transformer, inductor, capacitor) and heavier DC/DC converters, which is a considerable drawback of the industrial equipment power supply.

Soft-switching techniques, when applicable to a power converter, aid in energy efficiency enhancement, switching frequency increase (passive component size and weight reduction), switching device electrical/thermal stress reduction, EMI reduction, and cost reduction. In a soft-switching circuit, the switches commutate at zero voltage or current. Thus, the switching power losses on the device are annihilated. Soft-switching is obtained by adding resonant components (inductors and capacitors) to or using the parasitic components of a power converter circuit.

Soft-switching process is provided in the DC/DC converter circuit with a resonant switch, which consists of a controllable semiconductor switch (S), a reverse parallel external diode (freewheeling diode), and a resonant inductor (LR) or a resonant capacitor (CR). Soft-switching of the controllable

switch can be provided using either Zero Current Switching (ZCS) or Zero Voltage Switching (ZVS) technique. Figure 1.5 illustrates the resonant switches utilized for the ZCS and ZVS conditions. Whether a circuit can operate with the soft-switching principle depends on the ability of the resonant part of the circuit to reset itself. If the circuit is capable of self resetting, then soft- switching is applicable. Otherwise, soft-switching is not possible. With additional external circuit components most circuits can be made to operate with soft-switching, however for most circuits the solution is cost prohibitive. Thus, the technique is mostly applied to circuits that have self resetting capability.
For the resonant switch providing ZCS operation, a resonant inductor (LR) is connected in series with the controllable switch, as shown in Figure 1.5.a. When the switch is in off-state, the inductor current is zero, an opportunity exists for soft turnon. Since the inductor current is continuous and can not change instantaneously, with sufficient LR the device fully turns-on (the voltage across the switch (VS) is reduced to the on-state value) before the inductor current reaches a significant value. Hence, there exists only a small amount of switching power loss at turn-on process. The turn-off process for ZCS operation is accomplished by the resonance operation between LR and an external capacitor which is not included in Figure 1.5.a. The capacitor may be connected either in series with or parallel to the resonant switch based on the converter circuit topology. Once the resonance transition begins, the current decreases to zero. Thus, the opportunity for zero current turn-off is created. As a result of this resonance, VS starts to increase after IS is reduced to zero, hence ZCS is satisfied during turn-off switching interval also.

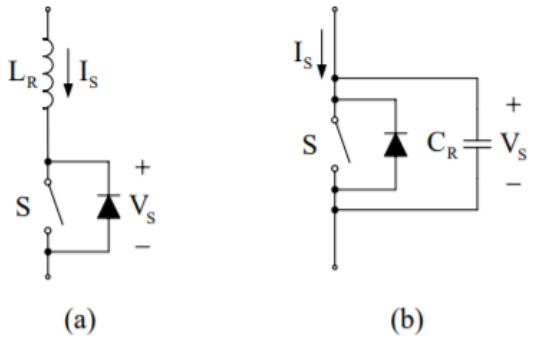

Figure 1.3 The elementary resonant switches for: (a) ZCS, and (b) ZVS operation

The resonant switch for the ZVS operation is provided by the connection of a resonant capacitor (CR) across the switch, as shown in Figure 1.5.b. This resonant capacitor may be the internal parasitic capacitance of the semiconductor switch or an externally added capacitor if required. The turn-off of the switch is completed with low switching power loss due to CR, which slows down the rise of VS, hence the switch is completely turned-off (IS is reduced to zero) before VS reaches a significant value. The turn-on of the switch for ZVS operation is carried out by the resonance of CR with an external inductor, which is connected to the resonant switch either in series or parallel. Due to resonance, IS starts to increase after VS is reduced to zero, resulting in a ZVS operation during turn-on switching interval.The full-bridge DC/DC converter is one conventional topology that favors softs witching with minor or no circuit topology modifications and specific operating modes. The circuit can be modified for operation under either ZCS or ZVS condition. The semiconductor switching device parasitic output capacitance can be utilized for ZVS operation. Thus, except for specific operating conditions (such as cases where switch dead-times become a limiting factor), there is no need for external circuit components. Otherwise, additional capacitors are connected in parallel to the switches to complete the circuit for ZVS operation. For ZVS operation of the full-bridge DC/DC converter, the operating method of the converter plays a critical role. Under phase-shifted switch pulse pattern operation (the switch logic signals of one leg are phase-shifted with respect to the other), the converter can operate with self resetting capability. Thus, this PWM method is favorable when combined with ZVS of the converter. Operating under ZVS condition permits to increase the switching frequency, which results in smaller size, lower weight, and higher bandwidth. When the full-bridge DC/DC converter is operated with the phase-shifted PWM method, the converter and its switch pulse pattern are identified with the name "Full-Bridge Phase-Shifted (FB-PS) DC/DC Converter." Further, when this converter is operated under ZVS condition, it is so called as "FB-PS-ZVS DC/DC Converter." In the circuit, the resonance that provides ZVS operation is between the switch output capacitance and the transformer leakage inductance. Figure 1.4 shows the DC/DC converter system with the resonant components emphasized.

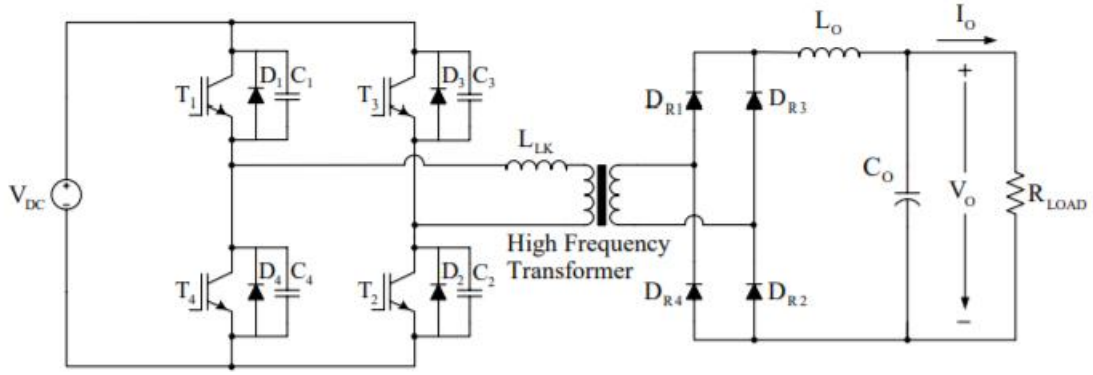

Figure 1.4 The FB-PS-ZVS DC/DC converter circuit diagram emphasizing the device parasitic capacitance or the externally added capacitors and the transformer parasitic leakage inductance.

SWITCH MODE DC/DC CONVERTERS

2.1 Introduction

The switch mode DC/DC converter is the main part of an SMPS. There are various types of DC/DC converter circuit topologies utilized in the SMPSs based on the system requirements such as output to input voltage relationship, power rating, and the need for galvanic isolation.

This part reviews the popular DC/DC converter circuit topologies and their basic operation principles. being the focus of the thesis, the full-bridge DC/DC converter, is discussed in detail. For the full-bridge DC/DC converter, the phase-shifted PWM method is discussed after the conventional PWM method

for the DC/DC converters is given. Thus, this chapter builds the basic background for the FB-PS-ZVS DC/DC converter study of the thesis.

2.2 Switch Mode DC/DC Converter Overview

Switch mode DC/DC converters can be investigated in two classes based on the demand for isolation. If electrical (galvanic) isolation is required due to the safety reasons, a transformer is utilized in the DC/DC converter. The most popular DC/DC converter topologies belonging to both nonisolated and isolated converter classes are listed in Figure 2.1. Topologically, the step-down and step-up converters are the basic topologies and the rest can be derived from these two converters.

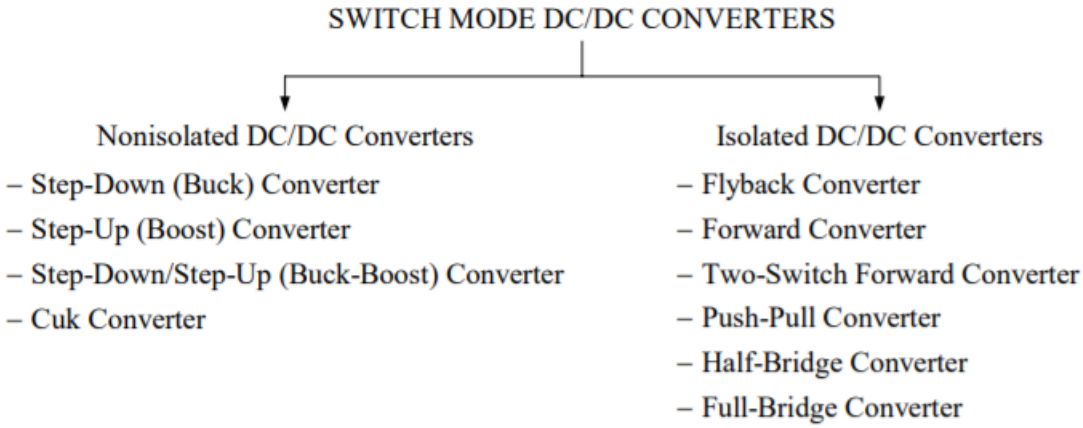

Figure 2.1 Topological classification of the popular switch mode DC/DC converters.

In this section, the listed DC/DC converter circuit topologies in Figure 2.1 are reviewed by utilizing their basic circuit configuration. The circuit topologies discussed are in their basic form and modified forms are not discussed in this review. Thus the switching (commutation) behavior of the switches is not altered from the form inherent to the circuit. Therefore, the switches are generally considered to be under hard-switching operating condition, which corresponds to the voltage and current simultaneously being large during switching and implies considerable switching loss and stress on the device. Hence, there will be high switching losses and stress during the turn-on and turn-off process that limits the switching frequency of the controllable switch.

2.2.2 Isolated DC/DC Converters

Isolated DC/DC converters utilize a high frequency transformer to provide electrical isolation between the load and the input line due to safety reasons mainly. The isolated DC/DC converter topologies listed in Figure 2.1 are derived from the basic nonisolated DC/DC converter topologies. These converters have a wide power range of application from a few watts to hundreds of kilowatts. In the following, an overview of the most popular isolated DC/DC converters is given.

The flyback DC/DC converter, shown in Figure 2.2, is derived from the buck-boost converter. The inductor in the buck-boost converter is substituted with the flyback transformer which behaves like an

inductor practically. By winding the secondary of the transformer in reverse polarity with respect to the primary, the polarity of the diode and capacitor is reversed with respect to the buck-boost converter. While the switch (S) is conducting, the magnetizing inductance of the transformer is charged by the DC voltage source (VDC) and the transformer secondary voltage reverse biases the diode (D) resulting in no power transfer from input to the output. When the switch is turned off, the stored energy in the magnetizing inductance supplies the load current through the diode. The DC conversion ratio for the flyback converter, which is given in (2.5), is derived by utilizing the inductor volt-second balance rule which is applied to the magnetizing inductance of the transformer. Since the applied voltage to the primary winding is always at the same polarity, the flux induced in the flyback transformer core is in one direction only, which means the core is utilized only in the first quadrant of the B-H curve. Due to the poor magnetic core utilization, the flyback DC/DC converters can be utilized up to a few hundred watts only.

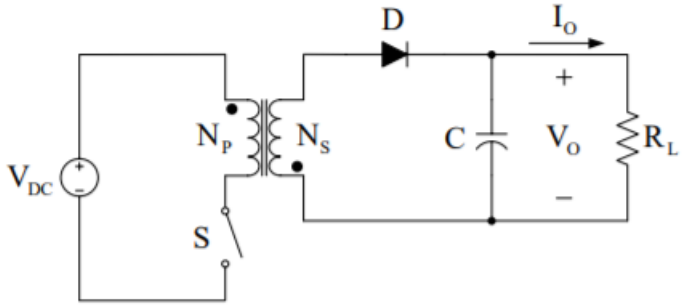

Figure 2.2 The flyback DC/DC converter circuit configuration.

$$\frac{V_O}{V_{DC}} = \frac{N_S}{N_P} \cdot \frac{d}{1-d} \qquad (2.5)$$

The full-bridge DC/DC converter, shown in Figure 2.3 , is derived from the stepdown converter and is obtained simply by replacing the capacitors C1 and C2 in the half-bridge DC/DC converter with the controllable switching devices. The basic operating scheme of this converter is providing the conduction of the switch pairs (S1 and S2, S3 and S4) alternately with the same duty cycle, which results in the voltage levels of -VDC or VDC applied to the transformer primary winding. The circuit operations carried out at the output stage are the same as in the push-pull DC/DC converter. The DC voltage conversion ratio of the full-bridge DC/DC converter is obtained from the filter inductor (L) volt-second balance rule. When one of the switch pairs (S1 and S2 or S3 and S4) is on for the duration of d·TS, the voltage across the filter inductor is the difference between the referred input voltage to the secondary side and the output voltage. When all of the switches are off for the time interval of (1-d)·TS, the voltage across the filter inductor is the reverse of the output voltage. This operation is completed in a half switching period interval. In the other interval the switches of the other switch pair are on for the duration of d·TS again. Thus, the total duration of the power transfer is 2·d·TS. The resulting equality derived from the filter inductor volt-second balance rule is given in (2.9), where d can be 0.5 at most. By utilizing (2.10), the DC voltage conversion ratio for the full-bridge DC/DC converter is obtained as in (2.10). Although the circuit topologies of the fullbridge DC/DC converter and the push-pull DC/DC converter differ from each other, their DC conversion ratio is the same. While the push-pull DC/DC converter is typically rated at less than a kilowatt, the full-bridge DC/DC converter has a wide power range, up to hundreds of kilowatts.

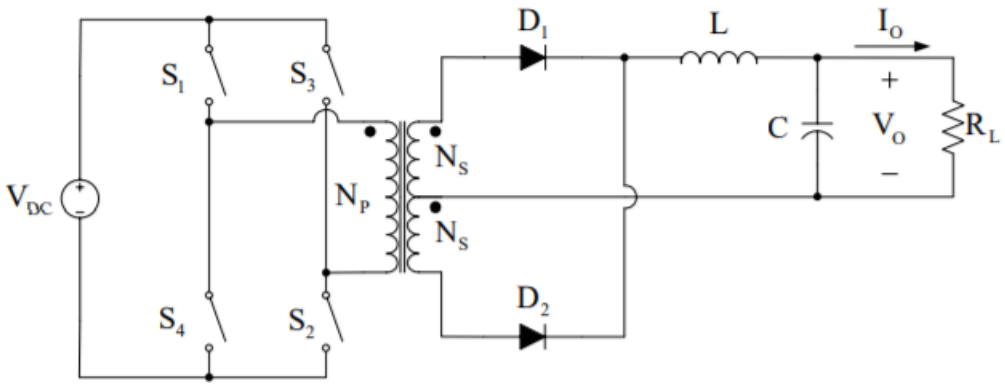

Figure 2.3 The full-bridge DC/DC converter circuit configuration.

$$\left(\frac{N_S}{N_P}V_{DC}-V_O\right)\cdot 2\cdot d\cdot T_S = V_O\cdot(1-2\cdot d)\cdot T_S \qquad (2.9)$$

$$\frac{V_O}{V_{DC}} = 2\cdot\frac{N_S}{N_P}\cdot d \qquad (2.10)$$

2.3 PWM Methods for The Switch Mode DC/DC Converters

The switch gate PWM signals of the switch mode DC/DC converters are generated by utilizing the reference voltage, which is calculated in the power supply control block using the measured and scaled feedback signals. In the analog implementation, the reference voltage is compared with a suitable sawtooth (or triangular) carrier voltage waveform to obtain the PWM signal for the controllable switch gate. In the conventional PWM method the sawtooth carrier waveform is fixed and the reference voltage magnitude is varied to regulate the output. However, in the phase-shifted PWM method the phase difference between the sawtooth carrier waveforms of the inverter legs is varied while the reference voltage is kept constant.

2.3.1 Conventional PWM Methods

The switch gate PWM signals of the single-switch DC/DC converters (for the stepdown, step-up, buck-boost, Cúk, flyback, and forward converter) are generated by comparing the calculated reference voltage in the control block, with a sawtooth carrier voltage waveform at the selected switching frequency. In the single loop voltage control mode, the reference voltage is obtained by the compensation of the error voltage, which is the difference between the measured output voltage of the

DC/DC converter and the desired reference output voltage. As illustrated in Figure 2.4, the switch is on in the intervals, where the reference voltage is higher than the sawtooth voltage, and the switch is off otherwise.

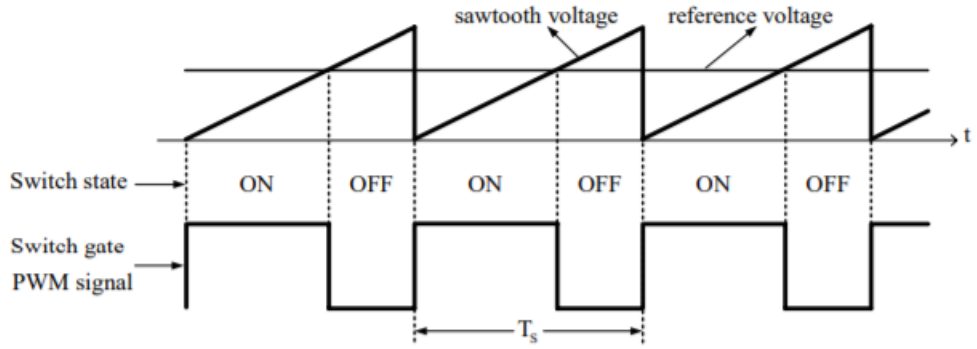

Figure 2.4 Conventional PWM signal generation scheme for the single-switch DC/DC converters.

For the push-pull, half-bridge and full-bridge DC/DC converters, a reference voltage that specifies the duty cycle of each switch is compared with a sawtooth carrier voltage waveform at twice the switching frequency. The alternating switch or switch pair is on during the interval that the reference voltage is higher than the sawtooth voltage and for the reverse case all of the switches are off. The sawtooth and reference voltage waveforms are shown and the resulting conducting switches in the corresponding time intervals are stated for these DC/DC converters in Figure 2.5. Also the applied transformer primary voltage waveform is shown in the same figure. As illustrated in Figure 2.5, the voltage levels at the transformer primary are -VDC/2 and VDC/2 for the half-bridge DC/DC converter, and -VDC, 0, and VDC for the pushpull and full-bridge DC/DC converters.

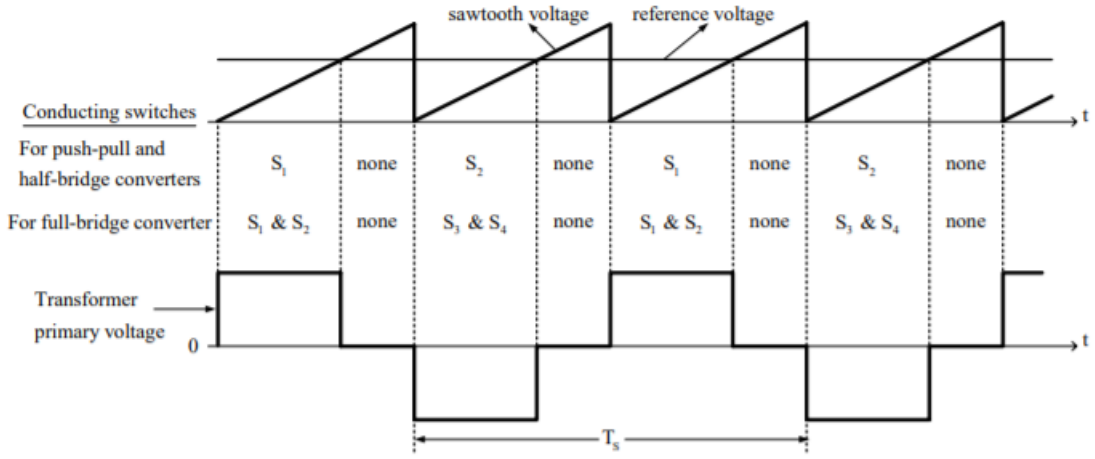

Figure 2.5 Conventional PWM signal generation scheme for the push-pull, half-bridge, and full-bridge DC/DC converters.

2.3.2 Phase-Shifted PWM Methods

The switch gate PWM signals of the full-bridge DC/DC converter can also be generated by utilizing the phase-shifted PWM method. While the generated switch PWM signals are the same, the generation

method of these signals is different from the conventional PWM method. In this PWM method while keeping the sawtooth carrier voltage waveform of one inverter leg constant, the output is regulated by phase shifting the carrier sawtooth voltage waveform of other leg as illustrated in Figure 2.6. To implement this method two sawtooth voltage waveforms, each for two switches of one inverter leg, are compared with the reference voltage (VR) which has a constant magnitude of half of the peak value of the sawtooth voltage waveform. Hence, all of the switches have the same duty cycle of 50%, ideally. The compensated error voltage is converted to the phase angle (φ) between the two carrier sawtooth voltage waveforms. Hence, in this PWM method, instead of the reference voltage, the phase angle is utilized as the control variable.

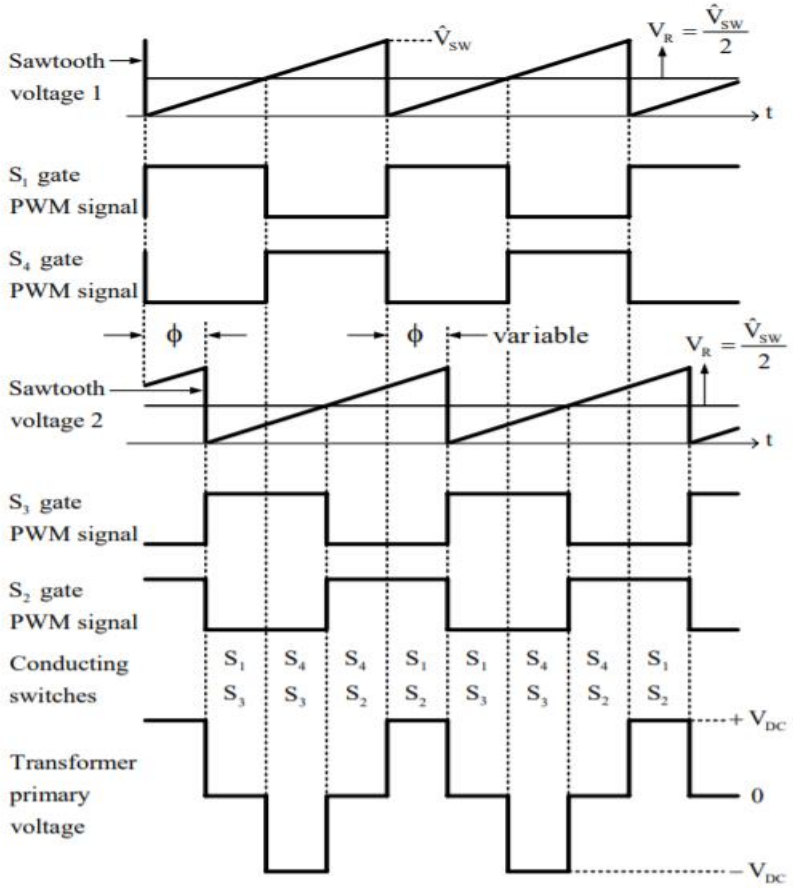

Figure 2.6 Phase-shifted PWM signal generation scheme for the full-bridge DC/DC converter.

ANALYSIS OF THE FULL-BRIDGE PHASE-SHIFTED ZERO VOLTAGE SWITCHING DC/DC CONVERTER

3.1 Introduction

The achievement of efficient high-frequency power conversion requires reduction of switching losses. Conventional resonant converters can provide zero-current switching (ZCS) or zero-voltage switching (ZVS). They generally require a wide range of frequency control, thus making the optimization of the filter components difficult. Quasi-resonant and multi-resonant converters have been proposed for reduced frequency range , but the high component stresses make them impractical for high-power and high-voltage applications. The recently-introduced constant frequency resonant converters can achieve ZCS or ZVS. However, it is at the expense of increased component stresses.When conventional PWM converters are operated at higher frequencies, the circuit parasitics are shown to have detrimental effects on the converter performance. Switching losses are especially pronounced in high-power, high-voltage applications. Snubbers are normally required, thus adding significant losses in high frequency opcration. A recently proposed new operating mode of the full-

bridge PWM converter permits all switching devices to operate under ZVS by using circuit parasitics to achieve resonant switching . To achieve ZVS, the two legs of the bridge are operated with a phase shift. This operation allows a resonant discharge of the output capacitance of the MOSFETs, and, subsequently, forces the conduction of cach MOSFET's antiparallel diode prior to the conduction of the MOSFET. Fig. 3.1 illustrates the waveforms in the circuit.

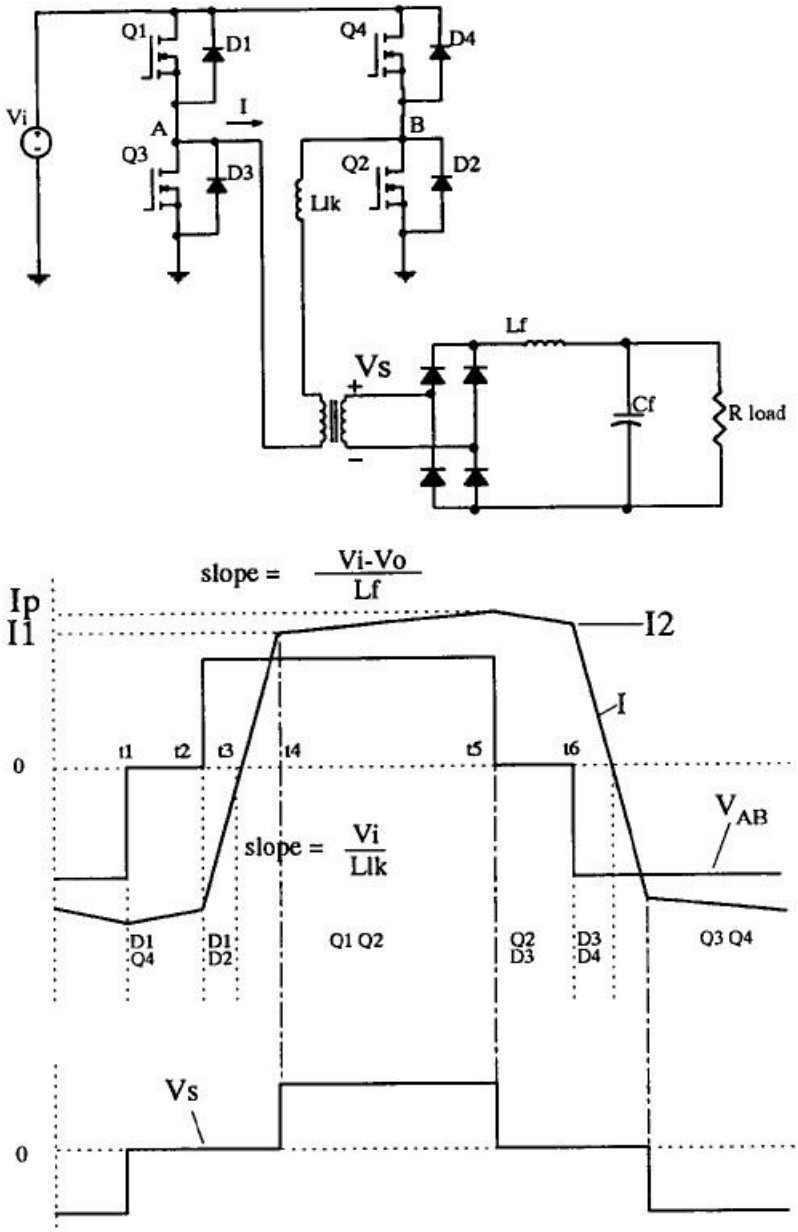

Figure 3.1 FB-ZVS-PWM converter and primary and secondary waveforms.

The zero-voltage switched PWM converter (ZVS-PWM) shown in Fig. 3.1 requires no additional active devices, and utilizer leakage inductance of the power transformer to achieve ZVS. It has a some-what higher rms current than the conventional full-bridge PWM converter, but has much lower rms currents than the resonant converters. The ZVS allows operation with much reduced switching losses and stresses, and eliminates the need for primary snubbers. It enables high switching frequency operation for improved power density and conversion efficiency. These advantages make this converter well suited for high-power, high-frequency applications.

The operation of this converter requires design considerations that differ from the conventional full-bridge PWM. The small-signal response of the ZVS converter also differs significantly from that of its

PWM counterpart. The paper presents the complete steady-state analysis of the ZVS-PWM converter. The paper also presents assessment of various losses in the circuit.

An analysis based design procedure is presented, and certain design considerations are discussed in the paper. 500w prototype is built to verify the proposed design procedure. The steady-state characteristics predicted from the analytical model are verified experimentally.

3.2 OPERATİON PRİCİPLE OF PS-FB ZVS DC-DC CONVERTER

The full-bridge PWM converter is operated in a mode that provides zero-voltage turn-on for the active switches. The current and voltage in the transformer primary are shown in Fig. 3.1. The gating signals are such that, instead of turning on the diagonally opposite switches in the bridge simultaneously, a phase shift is introduced between the switches in the left leg and those in the right leg. This phase shift determines the operating duty cycle of the converter.

The zero-voltage turn-on is achieved by using the energy stored in the leakage inductance of the transformer to discharge the output capacitance of the switches before turning them on.

Q4 and D1 are conducting, and at time t2, switch Q4 turns off and the current through the primary of the transformer charges the output capacitance of Q4 and discharges the output capacitance of Q2, turning on the diode D2. After D2 starts conducting, Q2 can be turned on with virtually no voltage applied across it. In order to achieve zero-voltage turn-on the energy stored in the leakage inductance has to be larger than the energy stored in the output capacitances. Therefore ZVS is lost for low load currents. The same is true for Q4 at t6:

At time t5, switch Q1 tums off and the current through the primary discharges the output capacitance of Q3 and charges the output capacitance of Q1, subsequently, diode ID3 is turned on. After D3 starts conducting, Q3 can be turned on with no voltage applied across it. In this case, when Q1 turns off, the current through the primary of the transformer is the output current reflected to the primary. The energy of the large filter inductor in the secondary is used to achieve ZVS.Therefore, ZVS is achieved easily for the switches Ql or Q3.

3.3 STEADY-STATE ANALYSIS OF PS-FB ZVS DC-DC CONVERTER

3.3.1 Required Dead Times

The mechanism by which ZVS is achieved is different for both legs of the bridge.

For transistors Q2 and Q4, the ZVS is provided by the resonance between the leakage inductance,Llk, and the output capacitance of the switch. Figure 2a shows the waveform of the current through D2-Q2.

Before Q2 is turned off, the current in the primary is circulating through diode D3 and transistor Q2, and the primary voltage is clamped to zero. When Q2 is turned off, the current through the primary forces the diode D4 to turn on, and the energy remaining in the primary leakage inductance is returned to the source. In order to turn on D4, the output capacitance of Q4 has to be discharged and the output capacitance of Q2 charged to the input voltage.The energy available for charging the output capacitance of Q4 and charging the output capacitance of Q2 is the energy stored in Llk, after t2 (or t6).Also, the transformer winding capacitance has to be charged in the process. Then the energy in Llk has to be:

$$E = \frac{1}{2} L_{lk} I_2^2 > \frac{4}{3} C_{MOS} V_{in}^2 + \frac{1}{2} C_{TR} V_{in}^2 \qquad 3.1$$

where I2 the current through the primary at time t2 (or t6), Vin is the input voltage, Llk is the

transformer leakage inductance, Cmos is the output capacitance of the switch at Vin and Ctr is the transformer winding capacitance. The term 4/3*Vin^2*Cmos, corresponds to two times the energy stored in the nonlinear drain-to-source capacitor, whose capacitance is inversely proportional to the square root of the voltage.

In order to ensure that Q4 will turn on with zero voltage, a dead time is needed between the turn-off of Q2 and turn-on of Q4 to ensure that D4 conducts prior to turn on of Q4. Knowing the elements that are involved in the process, the dead time required to ensure the maximum possible load range with ZVS can be determined. The resonance between Llk, Cmos and Ctr provides a sinusoidal voltage across the capacitances that reaches a maximum at one fourth of the resonant period,

$$\delta\tau_{max} = \frac{T}{4} = \frac{\pi}{2}\sqrt{L_{lk}C}$$

$$\text{where } C = C_{MOS} + C_{TR}. \qquad 3.2$$

The dead time between Q2 and Q4 is set at $\delta\tau_{max}$ to ensure that all the energy stored in Llk is available charge/discharge the capacitances.

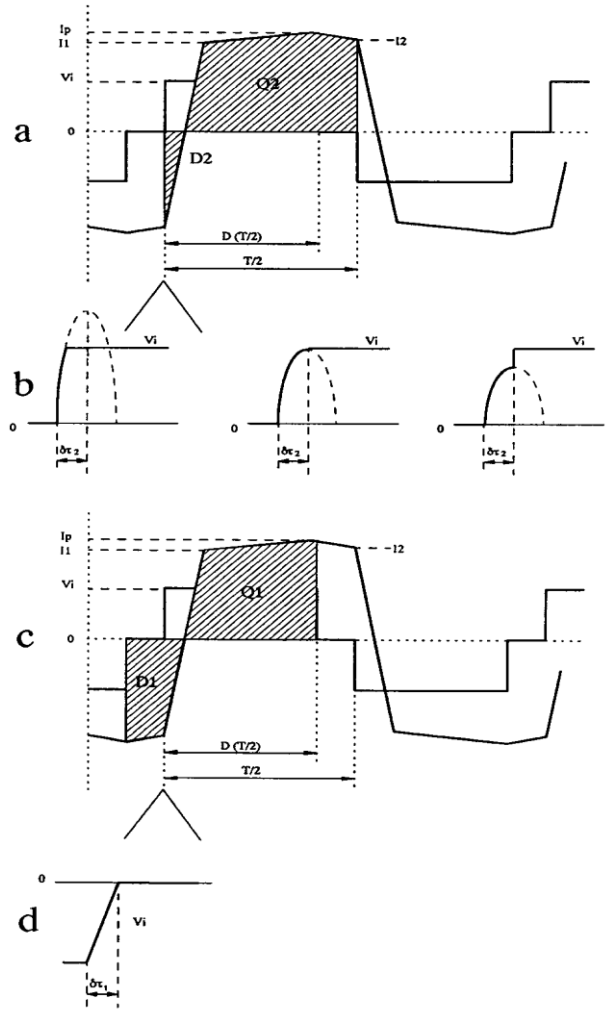

Figure 3.2 a)voltage and current in D2 and Q2. b)Detail of rising edge of the voltage c)Voltage and current D1 and Q1 d) Detail of rising edge of the voltage

Figure 3.2b presents detail of the voltage across Q4 at turn-off (time t2) for three different values of load current. The first voltage waveform corresponds to the case when the energy in Llk is larger than The energy required to charge/discharge the capacitors. The switch output capacitances are charged/discharged in less than $\delta\tau_{max}$, and the voltage is clamped to the input voltage. The second voltage waveform corresponds to the limit case when the energy in Llk is equal to the energy required to charge the capacitances. The last waveform corresponds to the case when the energy in Llk is not sufficient to charge/discharge the output capacitances, and ZVS is lost. After $\delta\tau_{max}$ Q4 (or Q2) is turned on and the voltage Vab increases sharply to Vin.

The ZVS for Q2 and Q4 is dependent on the load of the converter, and for light loads, the current through Llk at t2 (or t6) may not be sufficient to charge/discharge the output capacitance of the FETs and to turn on the antiparallel diode (D2 or D4).

For switches Ql and Q3, ZVS is provided by a different process. Before Ql is turned off, the current in the primary is reaching its peak value (Fig. 3.2c). The primary current is the reflected filter inductor current. When Q1 is turned off the energy available to charge the Q3 output capacitance of Ql and discharge the output capacitance of Q3 is the energy stored in Llk plus the energy in the output filter inductor. The latter is available because the filter inductor current does not yet freewheel through the rectifier until the voltage across the secondary has fallen to zero. Since the energy in the filter inductor is large compared to that required to charge/discharge the capacitances in the primary, the capacitances of the switches can be considered charged approximately at a linear rate with a constant current (Fig. 3.2d).

The value of the dead time, required between Ql and Q3 can be determined from the equation

$$4C_{MOS}V_{in} + C_{TR}V_{in} = I_p\,\delta\tau_1 \qquad 3.3$$

where the term 4CmosVin, corresponds to twice the charge stored in the nonlinear drain-to-source capacitance of the MOSFET.

The dead time can be calculated with the peak value of the primary current, Ip, that corresponds to the peak value of the current ripple in the output filter inductor reflected to the primary.

3.3.2 Zero voltage switching range

The ZVS for Ql and Q3 can be achieved even at light loads because D1 and D3 can always be turned on by the reflected current of the output filter inductance. However, Q2 and Q4 only achieve ZVS for a load current above a critical value. The critical current required in the primary to achieve ZVS can be calculated from (3.1)

$$I_{crit} = \sqrt{\frac{2}{L_{lk}}\left(\frac{4}{3}C_{MOS}\,V_{in}^2 + \frac{1}{2}C_{TR}\,V_{in}^2\right)} \qquad 3.4$$

The available current through Llk, at t2, can be calculated as,

$$I_2 = \frac{N_s}{N_p}\left(I_{load} + \frac{\Delta I}{2} - \frac{V_{out}}{L_f}(1-D)\frac{T}{2}\right) \qquad 3.5$$

where Lf is the filter inductance, Vout is the output voltage, D is the duty cycle in the primary, T is the switching period, Iload is the average output filter current, ▲I is the output filter inductor current ripple, and Np and Ns correspond to the number of turns in the primary and secondary of the transformer, respectively.

Finally, ZVS is achieved for values of load current such that

$$I_2 > Icrit$$

3.6

Or

$$I_{load} > \frac{N_p}{N_s} \; I_{crit} - \frac{\Delta I}{2} + \frac{V_{out}}{I_f}(1 - D)\frac{T}{2}$$

3.7

When the load current reflected to the primary is lower than the magnetizing current, the magnetizing becomes part of the ZVS process. For such light loads the energy available to charge/discharge the output capacitances of the switches Q2 and Q4 at times to respectively, is the energy stored in the leakage inductance, plus the energy stored in the magnetizing inductance of the transformer. This is because the magnetizing current can not circulate through the secondary of the transformer during intervals t1- t2 and t5- t6 due to the low output inductor filter currents freewheeling through the rectifier. The use of the magnetizing current has been fully described in reference [9] .

3.3.3 Choice of Switching Frequency, Leakage Inductance and Duty Cycle.

ZVS is achieved over a greater load range with larger values of Llk However, the finite slope in the rising and falling edges of the primary current reduces the duty cycle available in the secondary. For a desired dc-to-dc transformation, Llk has to be selected together with the frequency of operation and transformer turns ratio. The voltage gain of the ZVS-PWM converter can be expressed as:

$$\frac{V_{out}}{V_{in}} = \frac{N_s}{N_p} \; D_{eff}$$

3.8

where Deff is the duty cycle of the secondary voltage.

The primary duty cycle, that is set by the control of the circuit, can be expressed as:

$$D = D_{eff} + \Delta D$$

3.9

where ▲D is the loss of duty cycle due to the finite slope of the risin and falling edges of the primary current. Looking at Fig. 3.3 ▲D can be expressed as:

$$\Delta D = \frac{I_1 + I_2}{\frac{V_{in}}{L_{lk}} \; \frac{T}{2}}$$

3.10

$$\Delta D = \frac{\frac{N_s}{N_p}}{\frac{V_{in}}{L_{lk}} \; \frac{T}{2}} \left(2I_{load} - \frac{V_{out}}{L_f}(1 - D)\frac{T}{2} \right)$$

3.11

Putting Eq. (3.11) into (3.9) and using Eq. (3.8), the following expression is obtained:

$$D = \frac{1 + \frac{4L_{lk}f_s}{R'} - \frac{L_{lk}}{L'_f}}{\frac{1}{D_{eff}} - \frac{L_{lk}}{L'_f}} \qquad 3.12$$

Where R'=Rload*(Np/Ns)^2 and Lf' =Lf*(Np/Ns)^2 are the load resistance and filter inductor reflected to the primary.

When the term containing (1 - D) in Eq. (11) is small compared to 2*Iload, the Eq. (12) can be simplified to:

$$D = D_{eff}\left(1 + 4\frac{L_{lk}}{R'} f_s\right) \qquad 3.13$$

For a given power, input-output voltage ratio, and maximum duty cycle, the transformer turns ratio, switching frequency and leakage inductance have to be chosen to satisfy:

$$1 \geq D_{\max} \geq \frac{N_p}{N_s} \frac{V_{out}}{V_{in}} \left(1 + 4 \frac{L_{lk}}{R'} f_s\right) \qquad 3.14$$

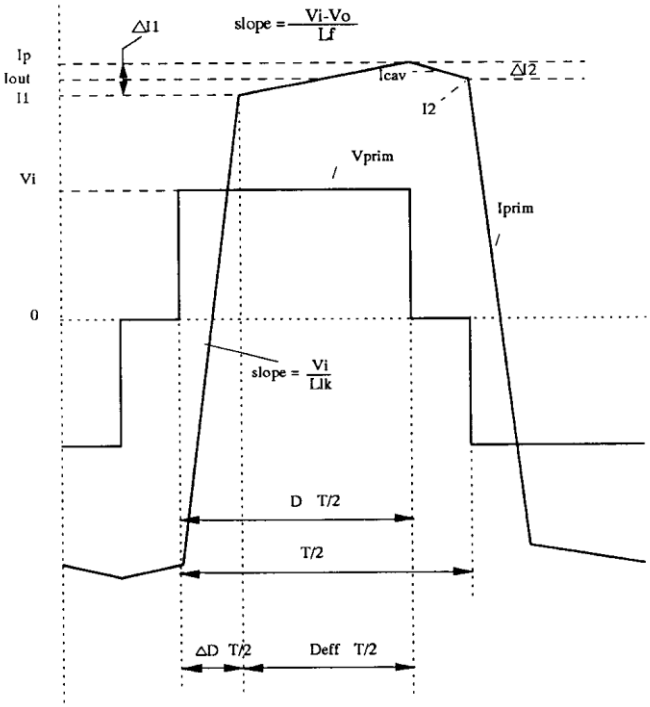

Figure 3.3 Definition of variables of the waveforms

3.3.4 Loss Analysis.

The ZVS-PWM converter provides ZVS for the devices, but it has larger rms currents in the primary than the conventional full bridge PWM converter. It is of primary interest to quantiff the conduction losses and compare them with those of the conventional PWM counterpart.

The conduction losses due to channel resistance of the switches can be calculated as:

$$P_Q = R_{on}\ I_{rms}^2 \qquad 3.15$$

where Ron is the channel resistance of the switch and Irms is the rms value of the current through the switch. The conduction losses for the switches are:

*Q2 or Q4

$$P_{Q_{2,4}} = R_{on} \cdot \left[\left(\frac{I_1}{\sqrt{3}} \right)^2 \frac{\Delta D}{2} + \left(I_{out}^2 + \frac{\Delta I_1^{\ 2}}{3} \right) D_{eff} + \left(I_{cav}^2 + \frac{\Delta I_2^{\ 2}}{3} \right) (1 - D) \right] \qquad 3.16$$

*Q1 or Q3

$$P_{Q_{1,3}} = R_{on} \cdot \left[\left(\frac{I_1}{\sqrt{3}} \right)^2 \frac{\Delta D}{2} + \left(I_{out}^2 + \frac{\Delta I_1^{\ 2}}{3} \right) D_{eff} \right] \qquad 3.17$$

where the first and second terms inside the brackets correspond to the rms currents during intervals t3 - t4 and t4 - t5 ,respectively. The third term for losses in Q2 and Q4 corresponds to the rms current during the time the primary voltage (V_{AB}) is clamped to zero, interval t1- t2- (t5 – t6). All the rest of the variables used are defined in Fig. 3.3.

Since the conventional PWM converter is always designed to minimize the leakage of the transformer, ▲D =~0 There is also no conduction during the interval t1 - t2 (t5 - t6).

The conduction losses on the primary bridge diodes are:

$$P_D = V_{diode}\ I_{av} \qquad 3.18$$

where Vdiode is the forward voltage drop on the diodes, and Iav is the average current through the diodes. The conduction loss of the diodes can be written as:

*D2 or D4

$$P_{D_{2,4}} = \left(\frac{I_2}{2} \right) V_{diode} \frac{\Delta D}{2} \qquad 3.19$$

*D1 or D3

$$P_{D_{1,3}} = V_{diode} \left[I_{out} (1 - D) + \frac{I_2}{2} \frac{\Delta D}{2} \right] \qquad 3.20$$

these losses are negligible in a conventional full-bridge PWM converter.

The conduction losses in the rectifier are the same for conventional PWM and ZVS-PWM.

*Rectifier

$$P_{rect} = 4\left(\frac{I_{out}}{2}\ V_f\right)$$

3.21

where Vf is the forward drop for the rectifier diodes, assuming that a full-bridge rectifier is used.

From the loss expressions, it can be deduced that the ZVS-PWM converter has larger conduction losses than the conventional PWM bridge, particularly when using small duty cycle and large Llk which imply large (1 - D) and large ▲D, respectively. The main advantage in terms of efficiency for the ZVS-PWM is provided by the reduced switching losses and the elimination of the need for snubber circuits across the bridge switches. This reduction of switching losses permits efficient operation at higher frequencies and reduces stress in the devices.

The use of snubber circuits across the output rectifier, common to both conventional PWM and ZVS-PWM, adds additional losses.The losses for the rectifier snubber are dependent on the available devices, and are discussed in detail in Section 4.

3.3.4 High frequency transformer.

High frequency transformers are designed to support integration with electronic switches in the form of high frequency signals. And they are designed to obtain the output voltage that is maintained between the lowest input voltage when the maximum load is connected. The duty cycle is an important parameter in controlling the operation of the system to transfer the energy of the transformer from the primary side to the secondary side. The offset time of each working period is half-worked alternately in order to reverse the primary side of the system and to allow the current to flow to the current circuit on the secondary side of the high frequency transformer. As a result, having to consider the loss of work cycles when calculating the rotation ratio. Otherwise, the converter may have a high loss value [16]. Especially during the control period under extreme load conditions, especially if it exists. For higher leakage induction values [17], the voltage is shown in the equation (3.22).

$$\frac{V_o}{V_{in}} = \frac{N_s}{N_p} \cdot ph - I_o \cdot \left(\frac{N_s}{N_p}\right) \cdot \frac{L_r}{V_{in}} \cdot f$$

3.22

For the energy loss from transformer ratio, without the cupper loss, can be can be calculated by this equation (3.22).

$$pheff = \frac{V_o}{V_{in}} \cdot \frac{N_p}{N_s}$$

3.23

The principle of choosing the size and shape of the transformer will mainly consider the efficiency and increasing temperature. Some transformer design experiences, along with a few repetitions, need to choose the most appropriate axis with a balanced core and loss of coil. For the loss of an acceptable

axis, determine the maximum magnetic flux limit at 0.1 Tesla. Therefore, the number of primary windings of the transformer can be calculated.

$$N_p = \frac{V_{in} \cdot ph_{eff}}{2 \cdot B_{\max} \cdot A_c \cdot f}$$

$$B_{\max} = \frac{V_{in} \cdot ph_{eff}}{2 \cdot N_p \cdot A_c \cdot f}$$

3.24 and 3.25

The ripple of inductor current can be calculated from the equation below

$$\Delta I_{L1} = \%Ripple \cdot \frac{I_o}{2}$$

3.26

The inductance of the L1 filter and the maximum current are determined according to the induced ripple current .

$$L_1 = \frac{1}{\Delta I_{L1}} \cdot V_o \left(1 - ph_{eff}\right) \cdot T$$

3.27

Output of the capacitor ripple current is a function other than the phase shift of the power conversion circuit. Current rectifier can completely reduce the current ripple in capacity in the case of Pheff= 0.48. Current ripple output capacitor, RMS current and ESR loss can be calculated by the following equation

$$\Delta I_{Co} = \frac{V_o}{L_1} \cdot T \cdot \left(1 - 2 \cdot ph_{eff}\right)$$

$$I_{Co.rms} = \sqrt{\frac{1}{12} \cdot \Delta I_{Co^2}}$$

$$P_{Co} = I_{Co.rms^2} \cdot ESR_{out}$$

3.27, 3.28 and 3.29

The ripple voltage of the capacitor value can be calculated from the equation

$$\Delta V_{Co} = \frac{V_o \cdot \left(1 - 2 \cdot ph_{eff}\right) \cdot T^2}{16 \cdot L_f \cdot C_o}$$

3.30

The capacitor value used to filter the output voltage can be calculated as

$$C_o = \frac{V_o \cdot \left(1 - 2 \cdot ph_{eff}\right) \cdot T^2}{16 \cdot L_m \cdot \Delta V_{Co}}$$

3.40

Design of Phase-Shifted Full-Bridge Power Converter

4.1 Specific Concidirations

The high voltage and power level of the converter require special attention to parasitics that can affect the operation. The primary leakage inductance and output capacitance of the devices are used to achieve ZVS, as has been described in Section 3.

The transformer design does not need to be optimized to reduce the leakage inductance as would be

the case for a conventional PWM converter. However, the parasitic capacitance of the windings has an adverse effect: it needs to be discharged at the same time as the output capacitances of the power FETs are charged/discharged. This increases the total energy required to be stored in the leakage inductance to ensure ZVS, as is presented in Eq.(3.4), resulting in a larger critical current required to achieve ZVS (Eq. 3.5). To reduce this effect, the transformer should be designed to minimize the winding parasitic capacitances.

The ringing across the rectifier is affected by the leakage inductance of the transformer, the winding capacitance and the rectifier diode characteristics. This ringing across the rectifier occurs when the voltage rises in the secondary of the transformer. In a full-bridge rectifier, when voltage is applied to the seccondary, two of the rectifier diodes are reverse biased, and the leakage of the transformer rings with the diode capacitance and winding capacitances. Even though fast recovery rectifiers are employed in this application, the diode reverse recovery can produce peak voltages higher than three times the voltage applied to the secondary.

The ringing has to be snubbed, but the use of an RC snubber in parallel with the rectifier would introduce large losses since the ringing frequency is less than 10 times the switching frequency, due to the large values of Llk. This frequency is,

$$f_{rng} = \frac{1}{2\pi\sqrt{\left(\frac{N_s}{N_p}\right)^2 L_{lk}\, C}} \qquad 4.23$$

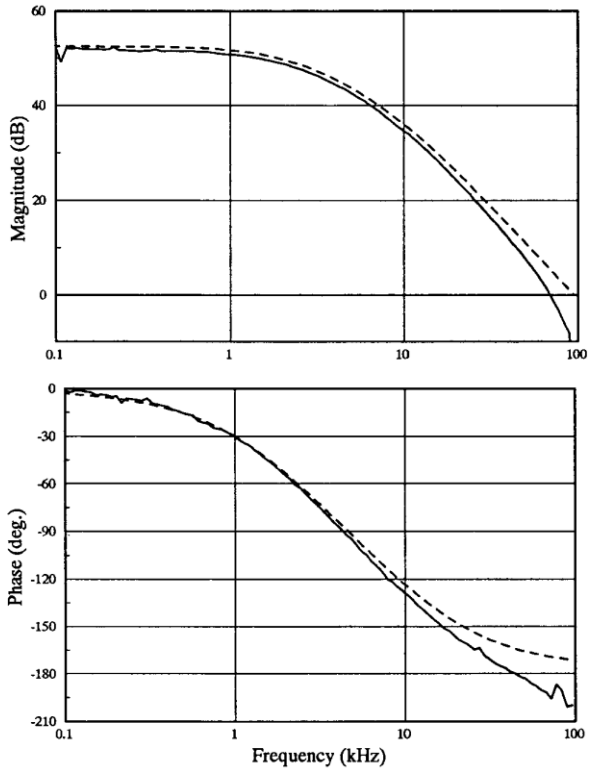

Figure 4.1: control the output transfer function , Measurements (solid lines) and prediction (dashed lines)

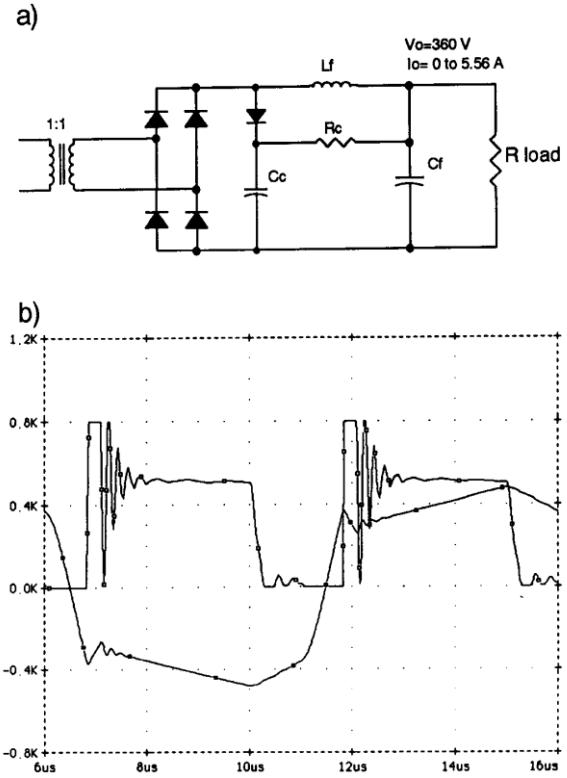

Figure 4.2:a) clamping circuit b)simulated rectifier circuit with the clamping circuit

where C is the equivalent capacitance of the rectifying diodes and the transformer windings.

A scheme has been proposed that clamps the maximum peak voltage of the ringing and returns part of the energy to the output. Figure 4.2a presents the clamping circuit used.

The design of the clamping circuit is based on balancing the charge that is transferred to the clamping capacitor, Cc with the charge returned to the load in order to keep the voltage across Cc constant .Figure 4.2b presents a simulation of the voltage across the rectifier and the primary current after adding the clamping circuit.

4.2 Design Guidelines

The equations presented in Section 3 are used to design the powerstage. This section outlines the design procedure for the ZVS-PWM.In the next section this procedure is used to design a prototype hardware.

1. Choose Dmax. Dmax should be chosen as large as possible. This allows to maximize Np/Ns and subsequently reduce the conduction losses in the primary (Eq. 3.20). Dmax is, however, limited by the time available for resetting the current-sensing transformer and by the duty cycle range allowed by the PWM controller.

2. Choose Vsec. Vsec should be chosen as low as possible to reduce the voltage stress of the rectifiers, and to maximize Np/Ns . However, reducing Vsec , i. e. increasing (Np, Ns) reduces the primary current and consequently increases the value of the Llk required for achieving a desired ZVS range. For this reason the initial choice of Vsec is somewhat arbitrary, and the final value is obtained after several iterations through steps 2 to 5.

Vsec has to satisfy:

$$V_{sec} \geq \frac{V_{out}}{D_{max}} \qquad 4.24$$

$$\frac{N_p}{N_s} = \frac{V_{in}}{V_{sec}} \qquad 4.25$$

The initial choice of Vsec should be somewhat higher than Vout/Dmax:.Once Vsec is chosen it is straightforward to calculate (Np/Ns), Deff(Eq. 3.8) and AD (Eq.3.9).

3. Chose the ZVS range. Calculate Icrit from Eq.(3.7). For this calculation it is necessary to choose the value of the output inductor current ripple, I_l, Since D is not known at partial loads, it is not possible to calculate Icrit exactly. In the first iteration of the design it is reasonable to make the average output inductor filter reflected to the primary equal to the value of Icrit.

After the first iteration is completed, the values required for the exact calculation can be determined and used as initial data for the next iteration.

4. Calculate Llk from Eq.(3.4). To perform this calculation it is necessary to choose the devices for the bridge and estimate the parasitic capacitance of the transformer.

5. Calculate the switching frequency from Eq. (3.11) or (3.12). After completing these steps the initial design is obtained. This design, however, may not be unsatisfactory from the point of view of circuit realization. The following cases may occur:

*Switching frequency too low (high): In this case it is possible to go to step 4 and reduce (increase) the ZVS range or to return to step 2 and increase (decrease) Vsec

* Llk too high (low): In this case it is possible to go to step 4 and reduce (increase) the ZVS range or to return to step 2 and increase (decrease) Vsec

4.3 POWER STAGE DESİGN

TABLE 4.3

Input voltage (V_{DC})	700V
Output voltage (V_O)	24V
Output current (IO)	20.8A
Switching frequency (f_S)	50khz
Output Power	500W
Dmax	0.48
Vsec	55V
Output voltage ripple ΔVo	0.25%Vo=60mv
Output inductor current ripple ΔI_l	10%Io=2.083A
Rload	1.152
Deff	0.445
Icrit	1.60
Np/Ns	13
Llk	76.5uH

The ZVS range is chosen to be from full load to 50% load, this implies a minimum load current for ZVS of 10.4 A. Using Eq. (3.7), the initial guess for Icrit =1.60 A

Choosing the devices with Cmos = 113 pF, and estimating the transformer capacitance to be Ctr = 100 pF, the Eq. (3.4) gives Llk 76.5 uH.

Lf =127.34uH calculated from Eq. 3.11

Design high frequency transformer

I use ferrit transformer for PS.FB.ZVS converter.Transformer model is Ferroxcube PQ40/40 3c90.

Np = 78 turn calculated form equation 3.24 .Np/ Ns =13 ,Ns = 6 turn.

ΔVc=0.25%Vout

ΔVc =0.06V

Co = 2000Uf

Table 3-38. Dimensional Data for PQ Ferrite Cores

PQ, Ferrite Cores (TDK)													
Part No.	A cm	B cm	C cm	D cm	E cm	G cm	Part No.	A cm	B cm	C cm	D cm	E cm	G cm
PQ20/16	2.050	1.800	1.620	1.400	0.880	1.030	PQ32/30	3.200	2.750	3.035	2.200	1.345	2.130
PQ20/20	2.050	1.800	2.020	1.400	0.880	1.430	PQ35/35	3.510	3.200	3.475	2.600	1.435	2.500
PQ26/20	2.650	2.250	2.015	1.900	1.200	1.150	PQ40/40	4.050	3.700	3.975	2.800	1.490	2.950
PQ26/25	2.650	2.250	2.475	1.900	1.200	1.610	PQ50/50	5.000	4.400	4.995	3.200	2.000	3.610
PQ32/20	3.200	2.750	2.055	2.200	1.345	1.150							

Table 3-39. Design Data for PQ Ferrite Cores

PQ, Ferrite Cores (TDK)											
Part No.	W_{tcu} grams	W_{tfe} grams	MLT cm	MPL cm	W_a/A_c	A_c cm^2	W_a cm^2	A_p cm^4	K_g cm^5	A_t cm^2	*AL mh/1K
PQ20/16	7.4	13.0	4.4	3.74	0.765	0.620	0.474	0.294	0.0166	16.9	1617
PQ20/20	10.4	15.0	4.4	4.54	1.061	0.620	0.658	0.408	0.0230	19.7	1313
PQ26/20	31.0	31.0	5.6	4.63	0.508	1.190	0.604	0.719	0.0611	28.4	2571
PQ26/25	17.0	36.0	5.7	5.55	0.716	1.180	0.845	0.997	0.0826	32.6	2187
PQ32/20	18.9	42.0	6.6	5.55	0.475	1.700	0.808	1.374	0.1415	36.3	3046
PQ32/30	35.5	55.0	6.7	7.46	0.929	1.610	1.496	2.409	0.2315	46.9	2142
PQ35/35	59.0	73.0	7.5	8.79	1.126	1.960	2.206	4.324	0.4520	60.7	2025
PQ40/40	97.2	95.0	8.4	10.20	1.622	2.010	3.260	6.553	0.6272	77.1	1792
PQ50/50	158.5	195.0	10.3	11.30	1.321	3.280	4.332	14.209	1.8099	113.9	2800

* This AL value has been normalized for a permeability of 1K. For a close approximation of AL for other values of permeability, multiply this AL value by the new permeability in kilo-perm. If the new permeability is 2500, then use 2.5.

Experimental result

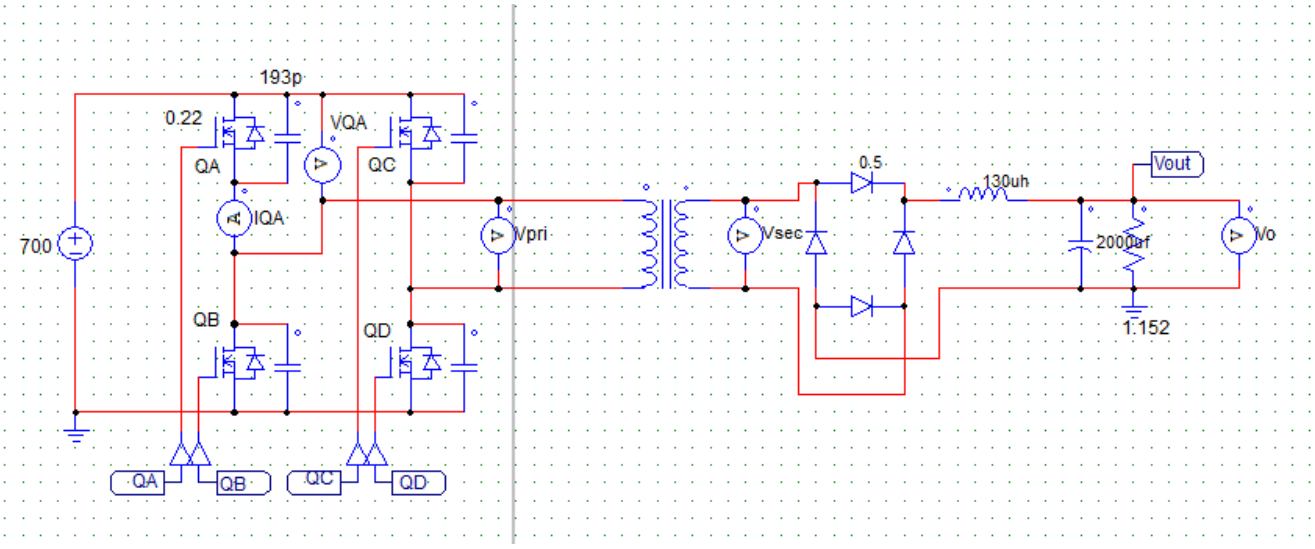

Figure 5.3 : PS.FB.ZVS DC TO DC CONVERTER

In the first part of the circuit will be full bridge phase-shift ZVS converter by PWM switching signals QA - QD with the phase shift method to allow the switch of the device to be in ZVS mode and also result in effective voltage control. In the second part, it is a high frequency rectifier circuit that

converts AC - DC voltage with a diode device D1 - D4 is presented in Figure 15.

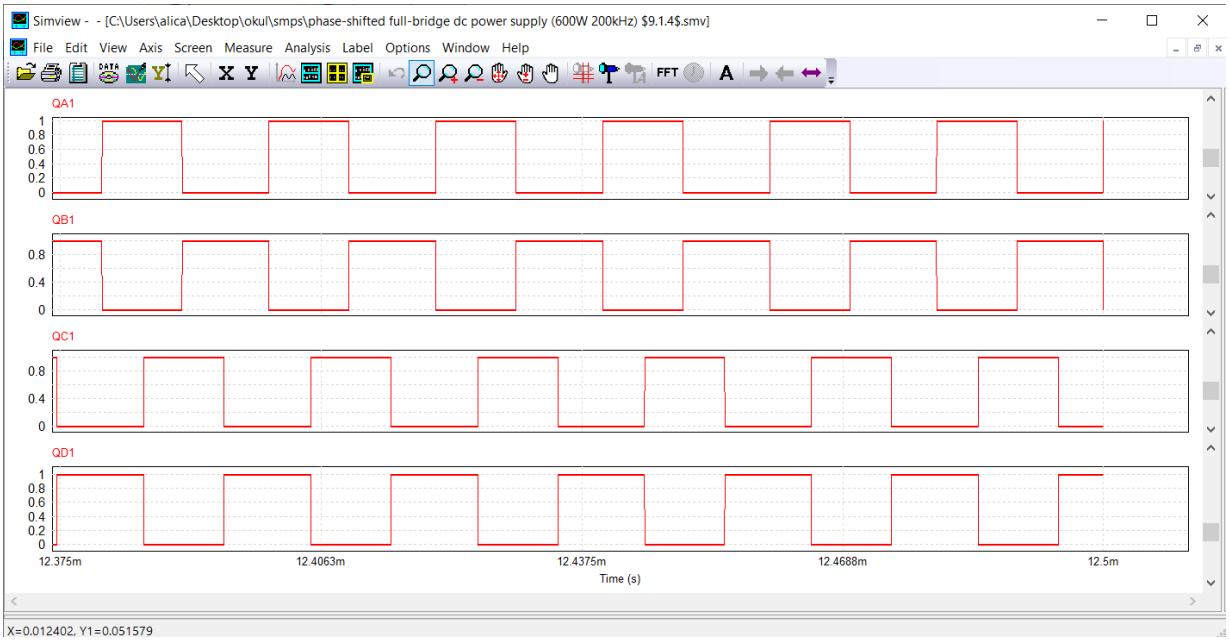

Figure 5.4: Gate pulses

PWM switching signals Q1-Q4 with the phase shift method show a simplified circuit of a phase shifted full bridge. The four switches work in a phase shift to control the range of circuits that are connected to the primary side of the high frequency transformer. The duty cycle of the switch signal is 48 %. The signal of the switch of Q1 and Q2 is divided into half the work time. Similarly,in Q3 and Q4 the performance of the phase shift signal is shown in the Fig. 4.4.

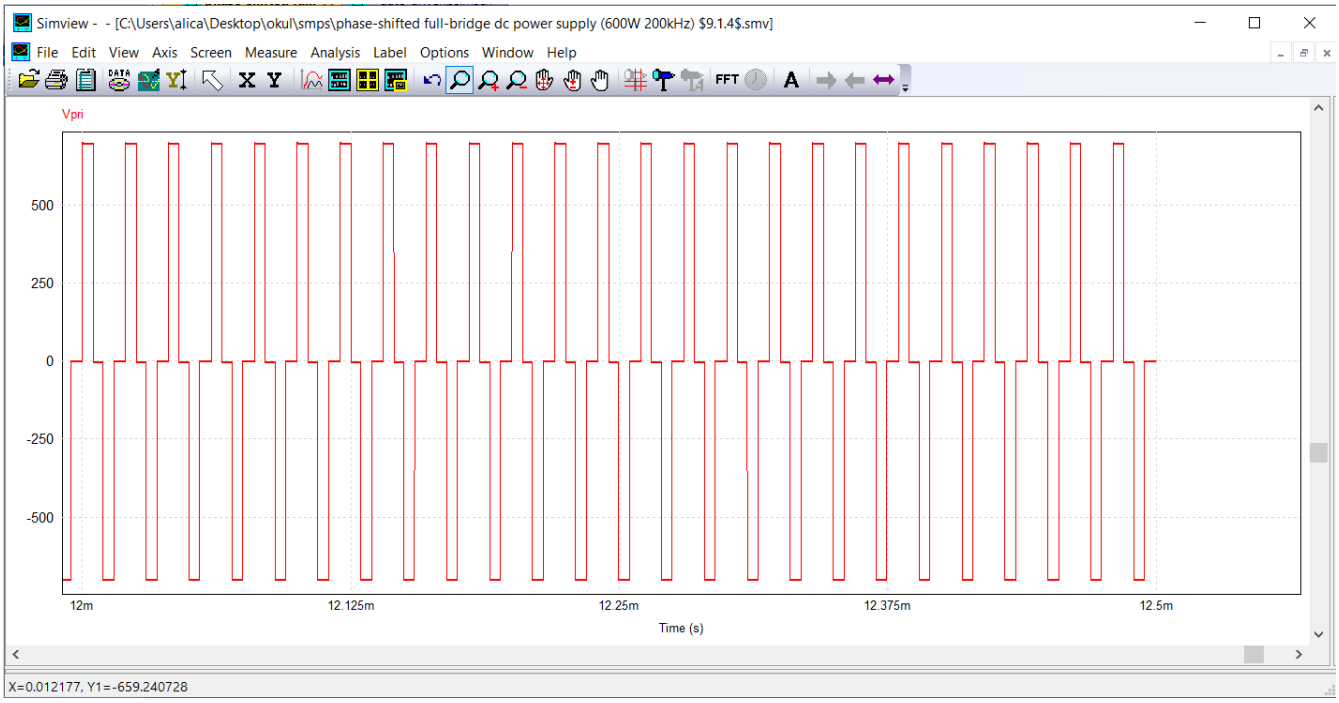

Figure 5.5 : primary voltage of the transformer

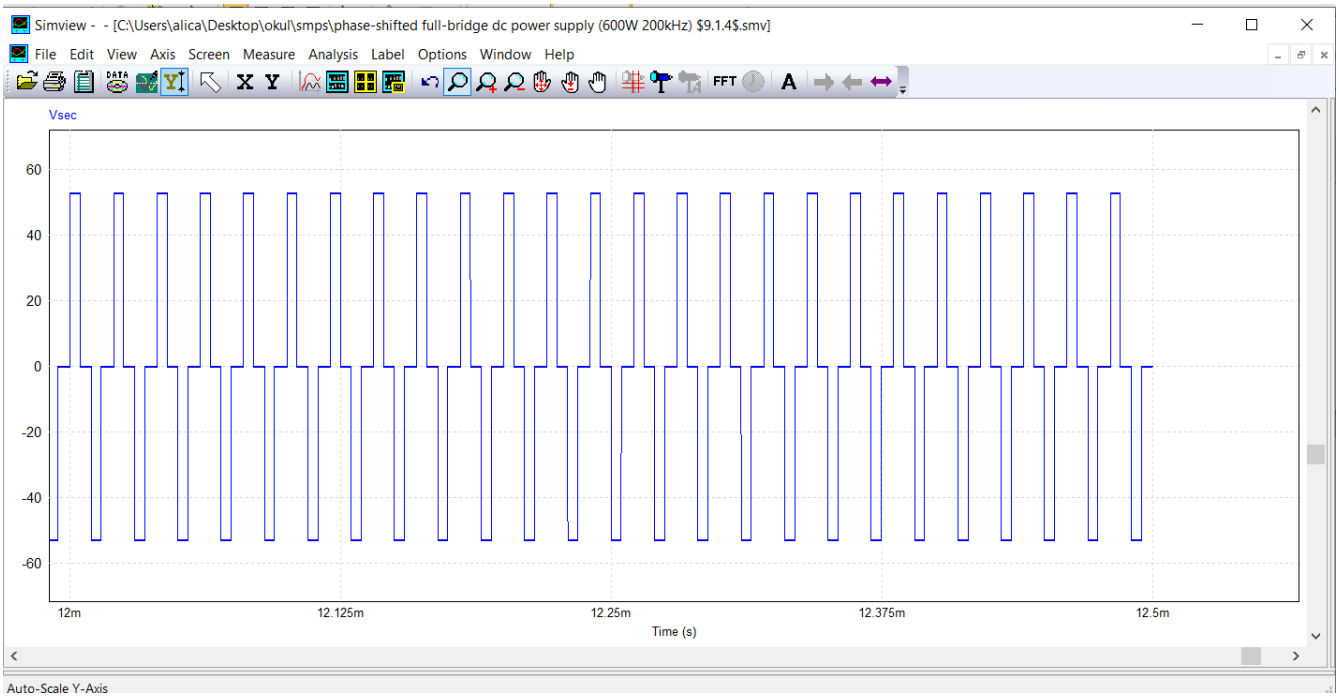

Figure 5.6 : secondary voltage of the transformer

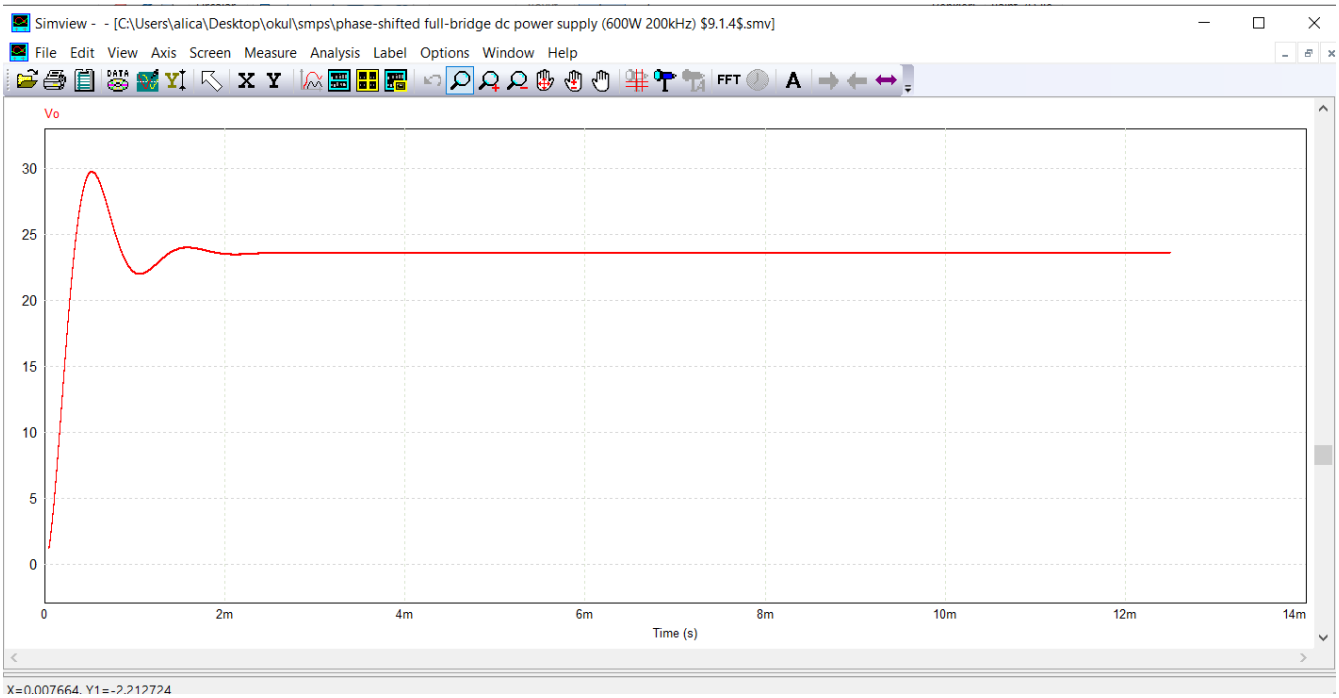

Figure 5.7 : Vout of the converter

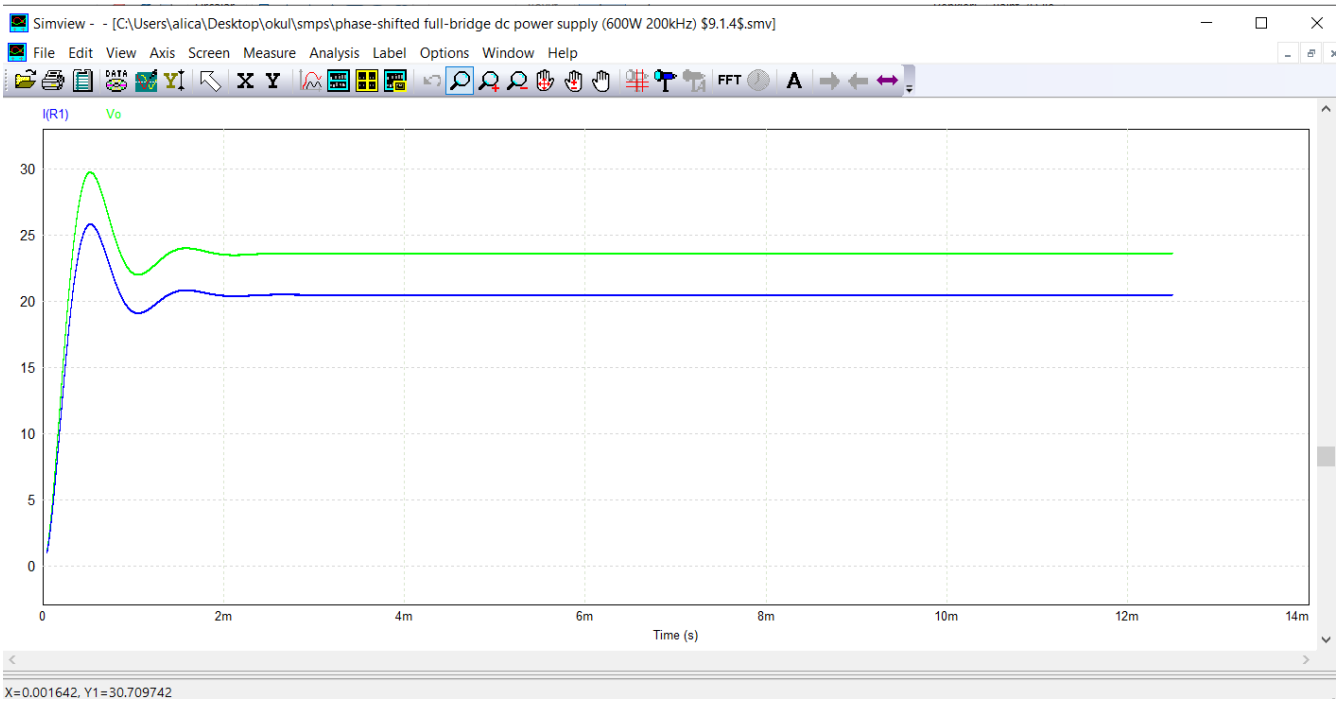

Figure 5.8:Iout and Vout of the conveter .

CONCLUSIONS

An iterative method for designing a PS-FB ZVS DC-DC converter has been presented in this paper and the steady-state analysis of the converter enumerated. A 500W rating phase-shifted full bridge zero voltage switch converter was designed and model in PSIM environment. The converter zero voltage switching was investigated over the design range and the operational waveforms including the inverter, transformer primary and secondary voltage-current, the load current, and the FET device switching waveforms performed satisfactorily. The system achieved 94% efficiency under full load condition

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