

Product Specification

Part Name: EPD Display Module

Customer Part ID:

Zhongjingyuan Part ID: ZJY200200-0154DAAMFGN

Ver: A

Customer:

Approved by

From: Zhengzhou Zhongjingyuan Electronic Technology Co., LTD.

Approved by

Zhengzhou Zhongjingyuan Electronic Technology Co., LTD.

302, Building 9, Yida Science and Technology New Town, No. 16, Jinzhan Street,
High-tech Industrial Development Zone, Zhengzhou, Henan, China

Notes:

1. Please contact Zhengzhou Zhongjingyuan Electronic Technology Co., LTD. before assigning your product based on this module specification
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by Zhengzhou Zhongjingyuan Electronic Technology Co., LTD. for any intellectual property claims or other problems that may result from application based on the module described herein.

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REVISION HISTORY

Rev	Date	Item	Page	Remark
1.0	JUN.04.2020	New Creation	ALL	
1.1	NOV.23.2020	Update DC Characteristics Add Packaging	P20 P31	

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1. Over View

ZJY200200-0154DAAMFGN is a TFT active matrix electrophoretic display, with interface and a reference system design. The 1.54" active area contains 200×200 pixels, and has 1-bit black/white full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

2. Features

- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- Landscape, portrait mode
- Antiglare hard-coated front-surface
- Low current sleep mode
- On chip display RAM
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and source driving voltage
- I²C Signal Master Interface to read external temperature sensor
- Available in COG package IC thickness 300um

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	1.54	Inch	
Display Resolution	200(H)×200(V)	Pixel	Dpi:184
Active Area	27.0(H)×27.0(V)	mm	
Pixel Pitch	0.14×0.14	mm	
Pixel Configuration	Square		
Outline Dimension	31.80(H)×37.32(V) × 0.98(D)	mm	
Weight	2.18±0.5	g	

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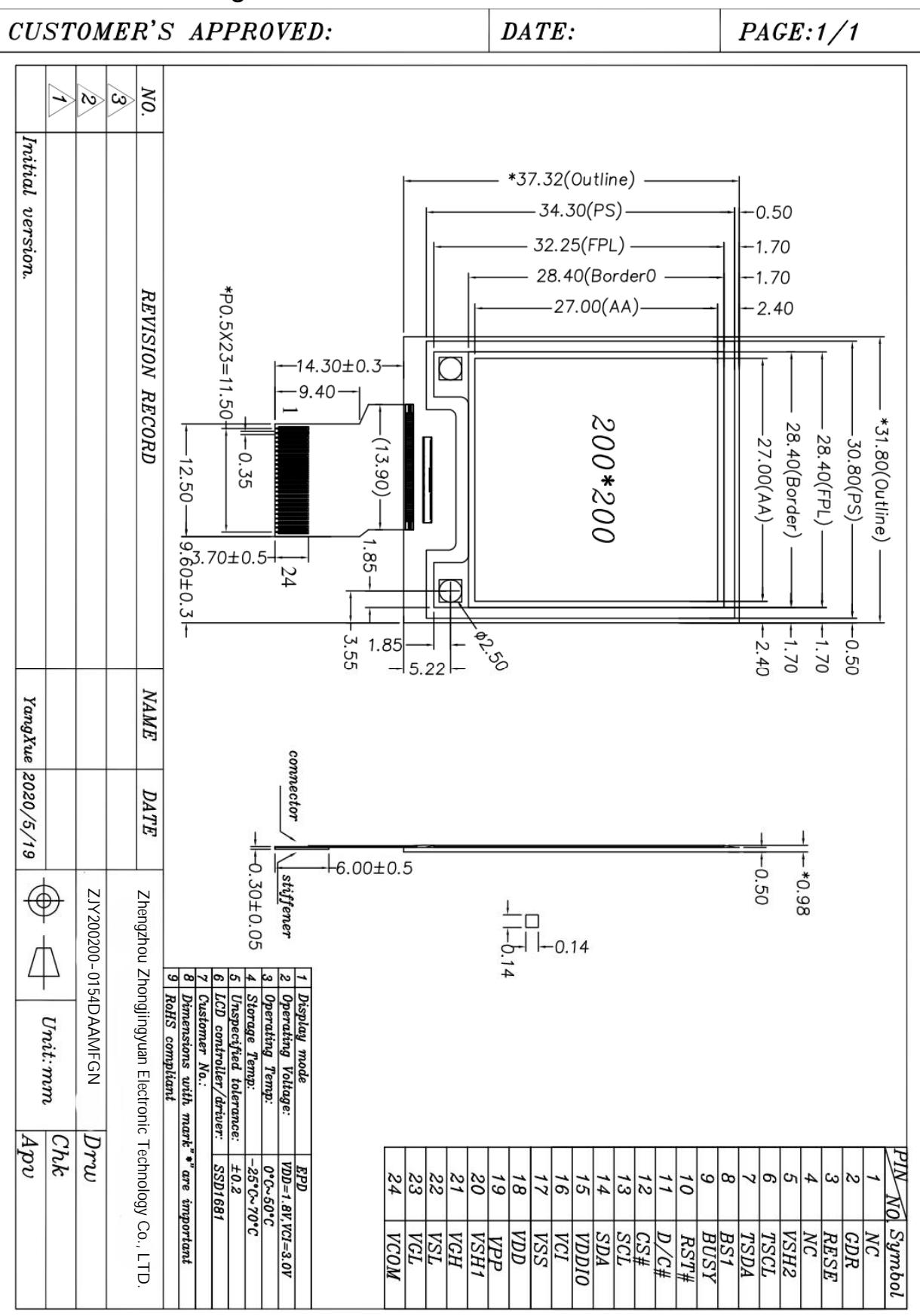


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4. Mechanical Drawing of EPD module



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5. Input /Output Pin Assignment

5-1) Pin out List

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	VSH2	C	Positive Source driving voltage(Red)	
6	TSCL	O	I ² C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I ² C Interface to digital temperature sensor Data pin	
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

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Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled Low.

Note 5-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled High, the data will be interpreted as data. When the pin is pulled Low, the data will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin (BUSY) is Busy state output pin. When Busy is Low, the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin

Low when the driver IC is working such as:

- Outputting display waveform; or
- Communicating with digital temperature sensor

Note 5-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

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6.Command Table

Command Table												Driver Output control	Description																																																									
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command																																																											
0	0	01	0	0	0	0	0	0	0	1			Gate setting A[8:0]= C7h [POR], 200 MUX MUX Gate lines setting as (A[8:0] + 1).																																																									
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	B[2:0] = 000 [POR]. Gate scanning sequence and direction																																																											
0	1		0	0	0	0	0	0	0	A ₈	B[2]: GD Selects the 1st output Gate GD=0 [POR], G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, ... GD=1, G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, ...																																																											
0	1		0	0	0	0	0	0	B ₂	B ₁	B ₀	B[1]: SM Change scanning order of gate driver. SM=0 [POR], G0, G1, G2, G3...199 (left and right gate interlaced) SM=1, G0, G2, G4 ...G198, G1, G3, ...G199																																																										
											B[0]: TB TB = 0 [POR], scan from G0 to G199 TB = 1, scan from G199 to G0.																																																											
0	0	03	0	0	0	0	0	0	1	1	Set Gate driving voltage A[4:0] = 00h [POR] VGH setting from 10V to 20V																																																											
0	1		0	0	0	A ₄	A ₃	A ₂	A ₁	A ₀	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>A[4:0]</th> <th>VGH</th> <th>A[4:0]</th> <th>VGH</th> </tr> </thead> <tbody> <tr><td>00h</td><td>20</td><td>0Dh</td><td>15</td></tr> <tr><td>03h</td><td>10</td><td>0Eh</td><td>15.5</td></tr> <tr><td>04h</td><td>10.5</td><td>0Fh</td><td>16</td></tr> <tr><td>05h</td><td>11</td><td>10h</td><td>16.5</td></tr> <tr><td>06h</td><td>11.5</td><td>11h</td><td>17</td></tr> <tr><td>07h</td><td>12</td><td>12h</td><td>17.5</td></tr> <tr><td>08h</td><td>12.5</td><td>13h</td><td>18</td></tr> <tr><td>07h</td><td>12</td><td>14h</td><td>18.5</td></tr> <tr><td>08h</td><td>12.5</td><td>15h</td><td>19</td></tr> <tr><td>09h</td><td>13</td><td>16h</td><td>19.5</td></tr> <tr><td>0Ah</td><td>13.5</td><td>17h</td><td>20</td></tr> <tr><td>0Bh</td><td>14</td><td>Other</td><td>NA</td></tr> <tr><td>0Ch</td><td>14.5</td><td></td><td></td></tr> </tbody> </table>				A[4:0]	VGH	A[4:0]	VGH	00h	20	0Dh	15	03h	10	0Eh	15.5	04h	10.5	0Fh	16	05h	11	10h	16.5	06h	11.5	11h	17	07h	12	12h	17.5	08h	12.5	13h	18	07h	12	14h	18.5	08h	12.5	15h	19	09h	13	16h	19.5	0Ah	13.5	17h	20	0Bh	14	Other	NA	0Ch	14.5		
A[4:0]	VGH	A[4:0]	VGH																																																																			
00h	20	0Dh	15																																																																			
03h	10	0Eh	15.5																																																																			
04h	10.5	0Fh	16																																																																			
05h	11	10h	16.5																																																																			
06h	11.5	11h	17																																																																			
07h	12	12h	17.5																																																																			
08h	12.5	13h	18																																																																			
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09h	13	16h	19.5																																																																			
0Ah	13.5	17h	20																																																																			
0Bh	14	Other	NA																																																																			
0Ch	14.5																																																																					



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Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source driving voltage A[7:0] = 41h [POR], VSH1 at 15V B[7:0] = A8h [POR], VSH2 at 5V. C[7:0] = 32h [POR], VSL at -15V Remark: VSH1>=VSH2
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		

A[7]/B[7] = 1,
VSH1/VSH2 voltage setting from 2.4V
to 8.8V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
8Eh	2.4	Afh	5.7
8Fh	2.5	B0h	5.8
90h	2.6	B1h	5.9
91h	2.7	B2h	6
92h	2.8	B3h	6.1
93h	2.9	B4h	6.2
94h	3	B5h	6.3
95h	3.1	B6h	6.4
96h	3.2	B7h	6.5
97h	3.3	B8h	6.6
98h	3.4	B9h	6.7
99h	3.5	BAh	6.8
9Ah	3.6	BBh	6.9
9Bh	3.7	BCh	7
9Ch	3.8	BDh	7.1
9Dh	3.9	BEh	7.2
9Eh	4	BFh	7.3
9Fh	4.1	C0h	7.4
A0h	4.2	C1h	7.5
A1h	4.3	C2h	7.6
A2h	4.4	C3h	7.7
A3h	4.5	C4h	7.8
A4h	4.6	C5h	7.9
A5h	4.7	C6h	8
A6h	4.8	C7h	8.1
A7h	4.9	C8h	8.2
A8h	5	C9h	8.3
A9h	5.1	CAh	8.4
AAh	5.2	CBh	8.5
ABh	5.3	CCh	8.6
ACh	5.4	CDh	8.7
ADh	5.5	CEh	8.8
AEh	5.6	Other	NA

A[7]/B[7] = 0,
VSH1/VSH2 voltage setting from 9V
to 17V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
23h	9	3Ch	14
24h	9.2	3Dh	14.2
25h	9.4	3Eh	14.4
26h	9.6	3Fh	14.6
27h	9.8	40h	14.8
28h	10	41h	15
29h	10.2	42h	15.2
2Ah	10.4	43h	15.4
2Bh	10.6	44h	15.6
2Ch	10.8	45h	15.8
2Dh	11	46h	16
2Eh	11.2	47h	16.2
2Fh	11.4	48h	16.4
30h	11.6	49h	16.6
31h	11.8	4Ah	16.8
32h	12	4Bh	17
33h	12.2	Other	NA
34h	12.4		
35h	12.6		
36h	12.8		
37h	13		
38h	13.2		
39h	13.4		
3Ah	13.6		
3Bh	13.8		

C[7:0]	VSL
0Ah	-5
0Ch	-5.5
0Eh	-6
10h	-6.5
12h	-7
14h	-7.5
16h	-8
18h	-8.5
1Ah	-9
1Ch	-9.5
1Eh	-10
20h	-10.5
22h	-11
24h	-11.5
26h	-12
28h	-12.5
2Ah	-13
2Ch	-13.5
2Eh	-14
30h	-14.5
32h	-15
34h	-15.5
36h	-16
38h	-16.5
3Ah	-17
Other	NA

0	0	08	0	0	0	0	0	1	0	0	0	Initial Code Setting OTP Program	Program Initial Code Setting
												The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.	

0	0	09	0	0	0	0	1	0	0	1	Write Register for Initial Code Setting	Write Register for Initial Code Setting Selection A[7:0] ~ D[7:0]: Reserved Details refer to Application Notes of Initial Code Setting
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		
0	1		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		

0	0	0A	0	0	0	0	1	0	1	0	Read Register for Initial Code Setting	Read Register for Initial Code Setting
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Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																																
0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start Control	Booster Enable with Phase 1, Phase 2 and Phase 3 for soft start current and duration setting.																																
0	1		1	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		A[7:0] -> Soft start setting for Phase1 = 8Bh [POR]																																
0	1		1	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		B[7:0] -> Soft start setting for Phase2 = 9Ch [POR]																																
0	1		1	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		C[7:0] -> Soft start setting for Phase3 = 96h [POR]																																
0	1		0	0	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D[7:0] -> Duration setting = 0Fh [POR]																																
Bit Description of each byte: A[6:0] / B[6:0] / C[6:0]:																																												
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Bit[6:4]</th> <th>Driving Strength Selection</th> </tr> </thead> <tbody> <tr><td>000</td><td>1(Weakest)</td></tr> <tr><td>001</td><td>2</td></tr> <tr><td>010</td><td>3</td></tr> <tr><td>011</td><td>4</td></tr> <tr><td>100</td><td>5</td></tr> <tr><td>101</td><td>6</td></tr> <tr><td>110</td><td>7</td></tr> <tr><td>111</td><td>8(Strongest)</td></tr> </tbody> </table>													Bit[6:4]	Driving Strength Selection	000	1(Weakest)	001	2	010	3	011	4	100	5	101	6	110	7	111	8(Strongest)														
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000	1(Weakest)																																											
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100	5																																											
101	6																																											
110	7																																											
111	8(Strongest)																																											
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Bit[3:0]</th> <th>Min Off Time Setting of GDR [Time unit]</th> </tr> </thead> <tbody> <tr><td>0000</td><td>NA</td></tr> <tr><td>~</td><td></td></tr> <tr><td>0011</td><td></td></tr> <tr><td>0100</td><td>2.6</td></tr> <tr><td>0101</td><td>3.2</td></tr> <tr><td>0110</td><td>3.9</td></tr> <tr><td>0111</td><td>4.6</td></tr> <tr><td>1000</td><td>5.4</td></tr> <tr><td>1001</td><td>6.3</td></tr> <tr><td>1010</td><td>7.3</td></tr> <tr><td>1011</td><td>8.4</td></tr> <tr><td>1100</td><td>9.8</td></tr> <tr><td>1101</td><td>11.5</td></tr> <tr><td>1110</td><td>13.8</td></tr> <tr><td>1111</td><td>16.5</td></tr> </tbody> </table>													Bit[3:0]	Min Off Time Setting of GDR [Time unit]	0000	NA	~		0011		0100	2.6	0101	3.2	0110	3.9	0111	4.6	1000	5.4	1001	6.3	1010	7.3	1011	8.4	1100	9.8	1101	11.5	1110	13.8	1111	16.5
Bit[3:0]	Min Off Time Setting of GDR [Time unit]																																											
0000	NA																																											
~																																												
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0100	2.6																																											
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1100	9.8																																											
1101	11.5																																											
1110	13.8																																											
1111	16.5																																											
D[5:0]: duration setting of phase D[5:4]: duration setting of phase 3 D[3:2]: duration setting of phase 2 D[1:0]: duration setting of phase 1																																												
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Bit[1:0]</th> <th>Duration of Phase [Approximation]</th> </tr> </thead> <tbody> <tr><td>00</td><td>10ms</td></tr> <tr><td>01</td><td>20ms</td></tr> <tr><td>10</td><td>30ms</td></tr> <tr><td>11</td><td>40ms</td></tr> </tbody> </table>													Bit[1:0]	Duration of Phase [Approximation]	00	10ms	01	20ms	10	30ms	11	40ms																						
Bit[1:0]	Duration of Phase [Approximation]																																											
00	10ms																																											
01	20ms																																											
10	30ms																																											
11	40ms																																											
0	0	10	0	0	0	0	1	0	0	0	Deep Sleep mode	Deep Sleep mode Control:																																
0	1		0	0	0	0	0	0	A ₁	A ₀		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>A[1:0] :</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>00</td><td>Normal Mode [POR]</td></tr> <tr><td>01</td><td>Enter Deep Sleep Mode 1</td></tr> <tr><td>11</td><td>Enter Deep Sleep Mode 2</td></tr> </tbody> </table>	A[1:0] :	Description	00	Normal Mode [POR]	01	Enter Deep Sleep Mode 1	11	Enter Deep Sleep Mode 2																								
A[1:0] :	Description																																											
00	Normal Mode [POR]																																											
01	Enter Deep Sleep Mode 1																																											
11	Enter Deep Sleep Mode 2																																											
After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high. Remark: To Exit Deep Sleep mode, User required to send HWRESET to the driver																																												

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Command Table																										
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description														
0	0	14	0	0	0	1	0	1	0	0	HV Ready Detection	HV ready detection A[7:0] = 00h [POR] The command required CLKEN=1 and ANALOGEN=1. Refer to Register 0x22 for detail. After this command initiated, HV Ready detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).														
0	1		0	A ₆	A ₅	A ₄	0	A ₂	A ₁	A ₀		A[6:4]=n for cool down duration: 10ms x (n+1) A[2:0]=m for number of Cool Down Loop to detect. The max HV ready duration is 10ms x (n+1) x (m) HV ready detection will be trigger after each cool down time. The detection will be completed when HV is ready. For 1 shot HV ready detection, A[7:0] can be set as 00h.														
0	0	15	0	0	0	1	0	1	0	1	VCI Detection	VCI Detection A[2:0] = 100 [POR] , Detect level at 2.3V A[2:0] : VCI level Detect														
0	1		0	0	0	0	0	A ₂	A ₁	A ₀		<table border="1" style="margin-left: auto; margin-right: auto;"> <tr><th>A[2:0]</th><th>VCI level</th></tr> <tr><td>011</td><td>2.2V</td></tr> <tr><td>100</td><td>2.3V</td></tr> <tr><td>101</td><td>2.4V</td></tr> <tr><td>110</td><td>2.5V</td></tr> <tr><td>111</td><td>2.6V</td></tr> <tr><td>Other</td><td>NA</td></tr> </table> <p>The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. After this command initiated, VCI detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).</p>	A[2:0]	VCI level	011	2.2V	100	2.3V	101	2.4V	110	2.5V	111	2.6V	Other	NA
A[2:0]	VCI level																									
011	2.2V																									
100	2.3V																									
101	2.4V																									
110	2.5V																									
111	2.6V																									
Other	NA																									
0	0	18	0	0	0	1	1	0	0	0	Temperature Sensor Control	Temperature Sensor Selection A[7:0] = 48h [POR], external temperature sensor A[7:0] = 80h Internal temperature sensor														
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[11:0] = 7FFh [POR]														
0	1		A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄																
0	1		A ₃	A ₂	A ₁	A ₀	0	0	0	0																
0	0	1B	0	0	0	1	1	0	1	1	Temperature Sensor Control (Read from temperature register)	Read from temperature register.														
1	1		A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄																
1	1		A ₃	A ₂	A ₁	A ₀	0	0	0	0																
0	0	12	0	0	0	1	0	0	0	1	SW RESET	<p>It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode</p> <p>During operation, BUSY pad will output high.</p> <p>Note: RAM are unaffected by this command.</p>														

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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	1C	0	0	0	1	1	1	0	0	Temperature Sensor Control (Write Command to External temperature sensor)	Write Command to External temperature sensor. A[7:0] = 00h [POR], B[7:0] = 00h [POR], C[7:0] = 00h [POR], A[7:6] A[7:6] Select no of byte to be sent 00 Address + pointer 01 Address + pointer + 1st parameter 10 Address + pointer + 1st parameter + 2nd pointer 11 Address A[5:0] – Pointer Setting B[7:0] – 1 st parameter C[7:0] – 2 nd parameter The command required CLKEN=1. Refer to Register 0x22 for detail. After this command initiated, Write Command to external temperature sensor starts. BUSY pad will output high during operation.
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h. BUSY pad will output high during operation. User should not interrupt this operation to avoid corruption of panel images.
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	RAM content option for Display Update A[7:0] = 00h [POR] B[7:0] = 00h [POR] A[7:4] Red RAM option 0000 Normal 0100 Bypass RAM content as 0 1000 Inverse RAM content A[3:0] BW RAM option 0000 Normal 0100 Bypass RAM content as 0 1000 Inverse RAM content
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A[2:0] = 011 [POR] A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	0	A ₂	A ₁	A ₀	
0	0	11	0	0	0	1	0	0	0	1		

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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	22	0	0	1	0	0	0	1	0	Display Update	Display Update Sequence Option:
0	1	A7	A6	A5	A4	A3	A2	A1	A0	Control 2	Enable the stage for Master Activation A[7:0]= FFh (POR)	
											Operating sequence	Parameter (in Hex)
											Enable clock signal	80
											Disable clock signal	01
											Enable clock signal → Enable Analog	C0
											Disable Analog → Disable clock signal	03
											Enable clock signal → Load LUT with DISPLAY Mode 1 → Disable clock signal	91
											Enable clock signal → Load LUT with DISPLAY Mode 2 → Disable clock signal	99
											Enable clock signal → Load temperature value → Load LUT with DISPLAY Mode 1 → Disable clock signal	B1
											Enable clock signal → Load temperature value → Load LUT with DISPLAY Mode 2 → Disable clock signal	B9
											Enable clock signal → Enable Analog → Display with DISPLAY Mode 1 → Disable Analog → Disable OSC	C7
											Enable clock signal → Enable Analog → Display with DISPLAY Mode 2 → Disable Analog → Disable OSC	CF
											Enable clock signal → Enable Analog → Load temperature value → DISPLAY with DISPLAY Mode 1 → Disable Analog → Disable OSC	F7
											Enable clock signal → Enable Analog → Load temperature value → DISPLAY with DISPLAY Mode 2 → Disable Analog → Disable OSC	FF
0	0	24	0	0	1	0	0	1	0	0	Write RAM (Black White) / RAM 0x24	After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly
											For Write pixel: Content of Write RAM(BW) = 1	
											For Black pixel: Content of Write RAM(BW) = 0	

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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED) / RAM 0x26	After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly. For Red pixel: Content of Write RAM(RED) = 1 For non-Red pixel [Black or White]: Content of Write RAM(RED) = 0
0	0	27	0	0	1	0	0	1	1	1	Read RAM	After this command, data read on the MCU bus will fetch data from RAM. According to parameter of Register 41h to select reading RAM0x24/ RAM0x26, until another command is written. Address pointers will advance accordingly. The 1 st byte of data read is dummy data.
0	0	28	0	0	1	0	1	0	0	0	VCOM Sense	Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value. The sensed VCOM voltage is stored in register The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	29	0	0	1	0	1	0	0	1	VCOM Sense Duration	Stabling time between entering VCOM sensing mode and reading acquired. A[3:0] = 9h, duration = 10s. VCOM sense duration = (A[3:0]+1) sec
0	0	2A	0	0	1	0	1	0	1	0	Program VCOM OTP	Program VCOM register into OTP The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	2B	0	0	1	0	1	0	1	1	Write Register for VCOM Control	This command is used to reduce glitch when ACVCOM toggle. Two data bytes D04h and D63h should be set for this command.
0	1		0	0	0	0	0	1	0	0		
0	1		0	1	1	0	0	0	1	1		

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0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register A[7:0] = 00h [POR]	Write VCOM register from MCU interface A[7:0] = 00h [POR]			
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		A[7:0]	VCOM	A[7:0]	VCOM
												08h	-0.2	44h	-1.7
												0Ch	-0.3	48h	-1.8
												10h	-0.4	4Ch	-1.9
												14h	-0.5	50h	-2
												18h	-0.6	54h	-2.1
												1Ch	-0.7	58h	-2.2
												20h	-0.8	5Ch	-2.3
												24h	-0.9	60h	-2.4
												28h	-1	64h	-2.5
												2Ch	-1.1	68h	-2.6
												30h	-1.2	6Ch	-2.7
												34h	-1.3	70h	-2.8
												38h	-1.4	74h	-2.9
												3Ch	-1.5	78h	-3
												40h	-1.6	Other	NA
0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read for Display Option A[7:0]: VCOM OTP Selection (Command 0x37, Byte A) B[7:0]: VCOM Register (Command 0x2C) C[7:0]~G[7:0]: Display Mode (Command 0x37, Byte B to Byte F) [5 bytes] H[7:0]~K[7:0]: Waveform Version (Command 0x37, Byte G to Byte J) [4 bytes]	Read Register for Display Option:			
1	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		A[7:0]: VCOM OTP Selection (Command 0x37, Byte A)			
1	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		B[7:0]: VCOM Register (Command 0x2C)			
1	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		C[7:0]~G[7:0]: Display Mode (Command 0x37, Byte B to Byte F) [5 bytes]			
1	1		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		H[7:0]~K[7:0]: Waveform Version (Command 0x37, Byte G to Byte J) [4 bytes]			
1	1		E ₇	E ₆	E ₅	E ₄	E ₃	E ₂	E ₁	E ₀					
1	1		F ₇	F ₆	F ₅	F ₄	F ₃	F ₂	F ₁	F ₀					
1	1		G ₇	G ₆	G ₅	G ₄	G ₃	G ₂	G ₁	G ₀					
1	1		H ₇	H ₆	H ₅	H ₄	H ₃	H ₂	H ₁	H ₀					
1	1		I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀					
1	1		J ₇	J ₆	J ₅	J ₄	J ₃	J ₂	J ₁	J ₀					
1	1		K ₇	K ₆	K ₅	K ₄	K ₃	K ₂	K ₁	K ₀					
0	0	2E	0	0	1	0	1	1	1	0	User ID Read	Read 10 Byte User ID stored in OTP: A[7:0]~J[7:0]: UserID (R38, Byte A and Byte J) [10 bytes]			
1	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀					
1	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀					
1	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀					
1	1		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀					
1	1		E ₇	E ₆	E ₅	E ₄	E ₃	E ₂	E ₁	E ₀					
1	1		F ₇	F ₆	F ₅	F ₄	F ₃	F ₂	F ₁	F ₀					
1	1		G ₇	G ₆	G ₅	G ₄	G ₃	G ₂	G ₁	G ₀					
1	1		H ₇	H ₆	H ₅	H ₄	H ₃	H ₂	H ₁	H ₀					
1	1		I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀					
1	1		J ₇	J ₆	J ₅	J ₄	J ₃	J ₂	J ₁	J ₀					

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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	2F	0	0	1	0	1	1	1	1	Status Bit Read	Read IC status Bit [POR 0x01] A[5]: HV Ready Detection flag [POR=0] 0: Ready 1: Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1: VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01]
1	1		0	0	A ₅	A ₄	0	0	A ₁	A ₀		Remark: A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively.
0	0	30	0	0	1	1	0	0	0	0	Program WS OTP	Program OTP of Waveform Setting The contents should be written into RAM before sending this command. The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	31	0	0	1	1	0	0	0	1	Load WS OTP	Load OTP of Waveform Setting The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [153 bytes], which contains the content of VS[nX-LUTm], TP[nX], RP[n], SR[nXY], and FR[n] Refer to Session 6.7 WAVEFORM SETTING
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	1		:	:	:	:	:	:	:	:		
0	1			
0	0	34	0	0	1	1	0	1	0	0	CRC calculation	CRC calculation command For details, please refer to SSD1681 application note. BUSY pad will output high during operation.
0	0	35	0	0	1	1	0	1	0	1	CRC Status Read	CRC Status Read A[15:0] is the CRC read out value
1	1		A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈		
1	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		

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0	0	36	0	0	1	1	0	1	1	0	Program OTP selection	Program OTP Selection according to the OTP Selection Control [R37h and R38h] The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	37	0	0	1	1	0	1	1	1	Write Register for Display Option	Write Register for Display Option A[7] Spare VCOM OTP selection 0: Default [POR] 1: Spare B[7:0] Display Mode for WS[7:0] C[7:0] Display Mode for WS[15:8] D[7:0] Display Mode for WS[23:16] E[7:0] Display Mode for WS[31:24] F[3:0] Display Mode for WS[35:32] 0: Display Mode 1 1: Display Mode 2 F[6]: PingPong for Display Mode 2 0: RAM Ping-Pong disable [POR] 1: RAM Ping-Pong enable G[7:0]~J[7:0] module ID /waveform version. Remarks: 1) A[7:0]~J[7:0] can be stored in OTP 2) RAM Ping-Pong function is not supported for Display Mode 1
0	0	38	0	0	1	1	1	0	0	0	Write Register for User ID	Write Register for User ID A[7:0]~J[7:0]: UserID [10 bytes] Remarks: A[7:0]~J[7:0] can be stored in OTP
0	0	39	0	0	1	1	1	0	0	1	OTP program mode	OTP program mode A[1:0] = 00: Normal Mode [POR] A[1:0] = 11: Internal generated OTP programming voltage Remark: User is required to EXACTLY follow the reference code sequences

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0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A[7:0] = C0h [POR], set VBD as HIZ. A[7:6] :Select VBD option
0	1		A ₇	A ₆	A ₅	A ₄	0	A ₂	A ₁	A ₀		A[7:6] Select VBD as 00 GS Transition, Defined in A[2] and A[1:0]
												01 Fix Level, Defined in A[5:4]
												10 VCOM
												11[POR] HIZ
												A [5:4] Fix Level Setting for VBD
												A[5:4] VBD level 00 VSS 01 VSH1 10 VSL 11 VSH2
												A[2] GS Transition control
												A[2] GS Transition control 0 Follow LUT (Output VCOM @ RED) 1 Follow LUT
												A [1:0] GS Transition setting for VBD
												A[1:0] VBD Transition 00 LUT0 01 LUT1 10 LUT2 11 LUT3
0	0	3F	0	0	1	1	1	1	1	1	End Option (EOPT)	Option for LUT end A[7:0]= 02h [POR]
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		22h Normal.
												07h Source output level keep previous output before power off
0	0	41	0	1	0	0	0	0	0	1	Read RAM Option	Read RAM Option A[0]= 0 [POR] 0 : Read RAM corresponding to RAM0x24 1 : Read RAM corresponding to RAM0x26
0	1		0	0	0	0	0	0	0	A ₀		
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit for RAM
0	1		0	0	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		A[5:0]: XSA[5:0], XStart, POR = 00h B[5:0]: XEA[5:0], XEnd, POR = 15h
0	1		0	0	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit for RAM
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		A[8:0]: YSA[8:0], YStart, POR = 000h B[8:0]: YEA[8:0], YEnd, POR = 127h
0	1		0	0	0	0	0	0	0	A ₈		
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	1		0	0	0	0	0	0	0	B ₈		

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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																				
0	0	46	0	1	0	0	0	1	1	0	Auto Write RED RAM for Regular Pattern	Auto Write RED RAM for Regular Pattern A[7:0] = 00h [POR]																				
0	1		A ₇	A ₆	A ₅	A ₄	0	A ₂	A ₁	A ₀		A[7]: The 1st step value, POR = 0 A[6:4]: Step Height, POR= 000 Step of alter RAM in Y-direction according to Gate <table border="1"><tr><th>A[6:4]</th><th>Height</th><th>A[6:4]</th><th>Height</th></tr><tr><td>000</td><td>8</td><td>100</td><td>128</td></tr><tr><td>001</td><td>16</td><td>101</td><td>200</td></tr><tr><td>010</td><td>32</td><td>110</td><td>200</td></tr><tr><td>011</td><td>64</td><td>111</td><td>200</td></tr></table>	A[6:4]	Height	A[6:4]	Height	000	8	100	128	001	16	101	200	010	32	110	200	011	64	111	200
A[6:4]	Height	A[6:4]	Height																													
000	8	100	128																													
001	16	101	200																													
010	32	110	200																													
011	64	111	200																													
												A[2:0]: Step Width, POR= 000 Step of alter RAM in X-direction according to Source <table border="1"><tr><th>A[2:0]</th><th>Width</th><th>A[2:0]</th><th>Width</th></tr><tr><td>000</td><td>8</td><td>100</td><td>128</td></tr><tr><td>001</td><td>16</td><td>101</td><td>200</td></tr><tr><td>010</td><td>32</td><td>110</td><td>200</td></tr><tr><td>011</td><td>64</td><td>111</td><td>200</td></tr></table>	A[2:0]	Width	A[2:0]	Width	000	8	100	128	001	16	101	200	010	32	110	200	011	64	111	200
A[2:0]	Width	A[2:0]	Width																													
000	8	100	128																													
001	16	101	200																													
010	32	110	200																													
011	64	111	200																													
												BUSY pad will output high during operation.																				
0	0	47	0	1	0	0	0	1	1	1	Auto Write B/W RAM for Regular Pattern	Auto Write B/W RAM for Regular Pattern A[7:0] = 00h [POR]																				
0	1		A ₇	A ₆	A ₅	A ₄	0	A ₂	A ₁	A ₀		A[7]: The 1st step value, POR = 0 A[6:4]: Step Height, POR= 000 Step of alter RAM in Y-direction according to Gate <table border="1"><tr><th>A[6:4]</th><th>Height</th><th>A[6:4]</th><th>Height</th></tr><tr><td>000</td><td>8</td><td>100</td><td>128</td></tr><tr><td>001</td><td>16</td><td>101</td><td>200</td></tr><tr><td>010</td><td>32</td><td>110</td><td>200</td></tr><tr><td>011</td><td>64</td><td>111</td><td>200</td></tr></table>	A[6:4]	Height	A[6:4]	Height	000	8	100	128	001	16	101	200	010	32	110	200	011	64	111	200
A[6:4]	Height	A[6:4]	Height																													
000	8	100	128																													
001	16	101	200																													
010	32	110	200																													
011	64	111	200																													
												A[2:0]: Step Width, POR= 000 Step of alter RAM in X-direction according to Source <table border="1"><tr><th>A[2:0]</th><th>Width</th><th>A[2:0]</th><th>Width</th></tr><tr><td>000</td><td>8</td><td>100</td><td>128</td></tr><tr><td>001</td><td>16</td><td>101</td><td>200</td></tr><tr><td>010</td><td>32</td><td>110</td><td>200</td></tr><tr><td>011</td><td>64</td><td>111</td><td>200</td></tr></table>	A[2:0]	Width	A[2:0]	Width	000	8	100	128	001	16	101	200	010	32	110	200	011	64	111	200
A[2:0]	Width	A[2:0]	Width																													
000	8	100	128																													
001	16	101	200																													
010	32	110	200																													
011	64	111	200																													
												During operation, BUSY pad will output high.																				
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[5:0]: 00h [POR].																				
0	1		0	0	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																						
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: 000h [POR].																				
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																						
0	1		0	0	0	0	0	0	0	A ₈																						
0	0	7F	0	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read Commands.																				

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7. Electrical Characteristics

7-1) Absolute maximum rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	V _{CI}	-0.5 to +4.0	V
Logic Input voltage	V _{IN}	-0.5 to V _{CI} +0.5	V
Logic Output voltage	V _{OUT}	-0.5 to V _{CI} +0.5	V
Operating Temp range	T _{OPR}	0 to +50	°C
Storage Temp range	T _{TSTG}	-25 to +70	°C
Optimal Storage Temp	T _{TSTGo}	23±2	°C
Optimal Storage Humidity	H _{TSTGo}	55±10	%RH

7-2) Panel DC Characteristics

The following specifications apply for: V_{SS}=0V, V_{CI}=3.0V, T_{OPR} =23°C

Parameter	Symbol	Conditions	Applicable pin	Min.	Typ.	Max	Units
Single ground	V _{SS}	-		-	0	-	V
Logic supply voltage	V _{CI}	-	V _{CI}	2.2	3.0	3.7	V
Core logic voltage	V _{DD}		V _{DD}	1.7	1.8	1.9	V
High level input voltage	V _{IH}	-	-	0.8 V _{CI}	-	-	V
Low level input voltage	V _{IL}	-	-	-	-	0.2 V _{CI}	V
High level output voltage	V _{OH}	I _{OH} = -100uA	-	0.9 V _{CI}	-	-	V
Low level output voltage	V _{OL}	I _{OL} = 100uA	-	-	-	0.1 V _{CI}	V
Typical power	P _{TYP}	V _{CI} =3.0V	-	-	4.5	-	mW
Deep sleep mode	P _{STPY}	V _{CI} =3.0V	-	-	0.003	-	mW
Typical operating current	I _{opr_V_{CI}}	V _{CI} =3.0V	-	-	1.5	-	mA
Image update time	-	25 °C	-	-	3	-	sec
Sleep mode current	I _{slp_V_{CI}}	DC/DC off No clock No input load Ram data retain	-	-	20		uA
Deep sleep mode current	I _{dslp_V_{CI}}	DC/DC off No clock No input load Ram data not retain	-	-	1	5	uA

- The Typical power consumption is measured with following pattern transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern.(Note 7-1)
- The standby power is the consumed power when the panel controller is in standby mode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by YES
- Vcom is recommended to be set in the range of assigned value ± 0.1V.

Note 7-1

The Typical power consumption

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7-3) Panel AC Characteristics

7-3-1) MCU Interface

7-3-1-1) MCU Interface selection

The module can support 3-wire/4-wire serial peripheral. MCU interface is pin selectable by BS1 shown in Table 7-1.

MCU Interface	Pin Name					
	BS1	RES#	CS#	D/C#	SCL	SDA
4-wire serial peripheral interface (SPI)	L	RES#	CS#	DC#	SCL	SDA
3-wire serial peripheral interface (SPI) - 9 bits SPI	H	RES#	CS#	L	SCL	SDA

Table 7-1 : Interface pins assignment under different MCU interface

Note

- (1) L is connected to V_{SS} and H is connected to V_{DDIO}

7-3-1-2) MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, D/C# and CS#. The control pins status in 4-wire SPI in writing command/data is shown in Table 6-2 and the write procedure 4-wire SPI is shown in Table 7-2

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

Table 7-2 : Control pins status of 4-wire SPI

Note:

- (1) L is connected to V_{SS} and H is connected to V_{DDIO}
- (2) ↑ stands for rising edge of signal
- (3) SDA (Write Mode) is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

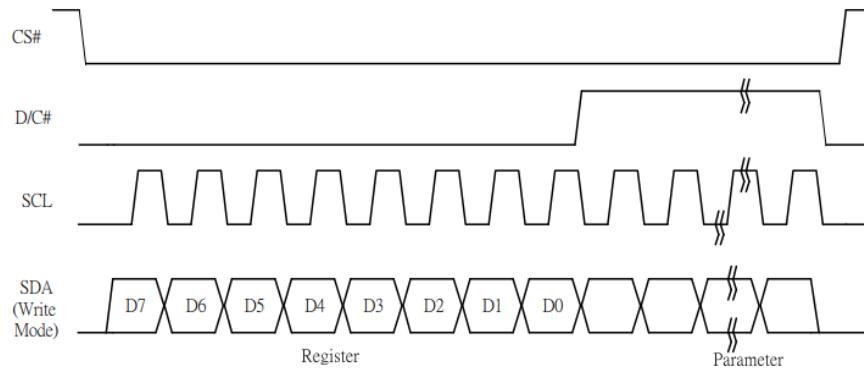


Figure 7-1 : Write procedure in 4-wire SPI mode

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In the read operation (Command 0x1B, 0x27, 0x2D, 0x2E, 0x2F, 0x35). After CS# is pulled low, the first byte sent is command byte, D/C# is pulled low. After command byte sent, the following byte(s) read are data byte(s), so D/C# bit is then pulled high. An 8-bit data will be shifted out on every clock falling edge. The serial data SDA bit shifting sequence is D7, D6, to D0 bit. Figure 6-2 shows the read procedure in 4-wire SPI.

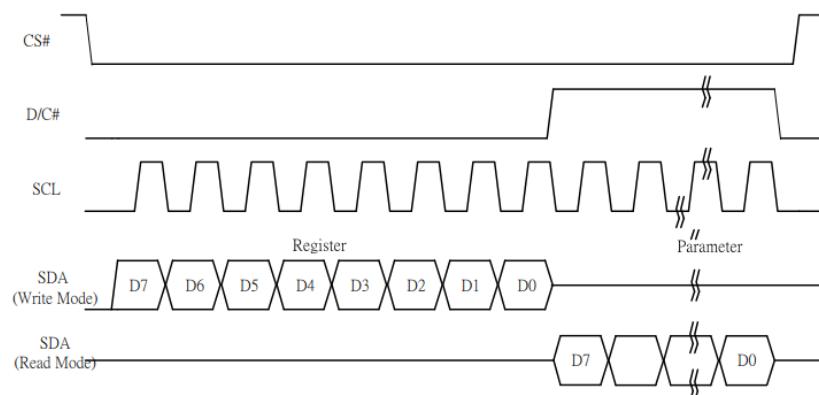


Figure 7-2 : Read procedure in 4-wire SPI mode

7-3-1-3) MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data SDA and CS#. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 7-3.

In the write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1, the following byte is data. Table 6-3 shows the write procedure in 3-wire SPI

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

Table 7-3 : Control pins status of 3-wire SPI

Note:

- (1) L is connected to VSS and H is connected to VDDIO
- (2) ↑ stands for rising edge of signal

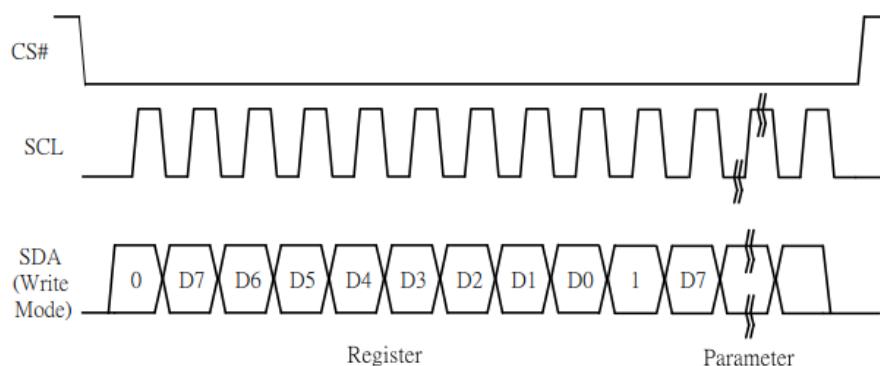


Figure 7-3 : Write procedure in 3-wire SPI

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In the read operation (Register 0x1B, 0x27, 0x2D, 0x2E, 0x2F, 0x35). SDA data are transferred in the unit of 9 bits. After CS# pull low, the first byte is command byte, the D/C# bit is as 0 and following with the register byte. After command byte send, the following byte(s) are data byte(s), with D/C# bit is 1. After D/C# bit sending from MCU, an 8-bit data will be shifted out on every clock falling edge. The serial data SDA bit shifting sequence is D7, D6, to D0 bit. Figure 7-4 shows the read procedure in 3-wire SPI.

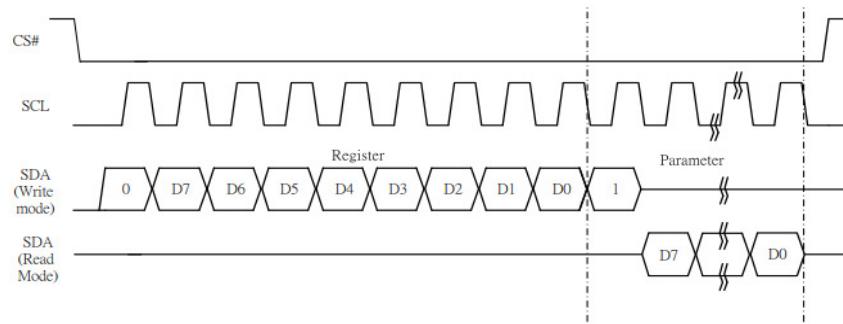


Figure 7-4 : Read procedure in 3-wire SPI mode

7-3-2)Serial Peripheral Interface

Write mode

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL frequency (Write Mode)	-	-	20	MHz
t _{CSSU}	Time CS# has to be low before the first rising edge of SCLK	60	-	-	ns
t _{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	65	-	-	ns
t _{CSHIGH}	Time CS# has to remain high between two transfers	100	-	-	ns
t _{SCLHIGH}	Part of the clock period where SCL has to remain high	25	-	-	ns
t _{SCLLOW}	Part of the clock period where SCL has to remain low	25	-	-	ns
t _{SISSU}	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10	-	-	ns
t _{SIHLD}	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40	-	-	ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL frequency (Read Mode)	-	-	2.5	MHz
t _{CSSU}	Time CS# has to be low before the first rising edge of SCLK	100	-	-	ns
t _{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	50	-	-	ns
t _{CSHIGH}	Time CS# has to remain high between two transfers	250	-	-	ns
t _{SCLHIGH}	Part of the clock period where SCL has to remain high	180	-	-	ns
t _{SCLLOW}	Part of the clock period where SCL has to remain low	180	-	-	ns
t _{SOSSU}	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL	-	50	-	ns
t _{SOHLD}	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL	-	0	-	ns

Note: All timings are based on 20% to 80% of VDDIO-VSS

Table 7-4: Serial Peripheral Interface Timing Characteristics

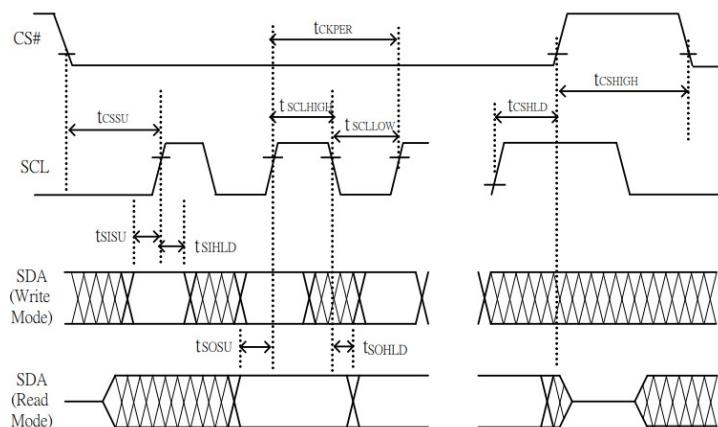
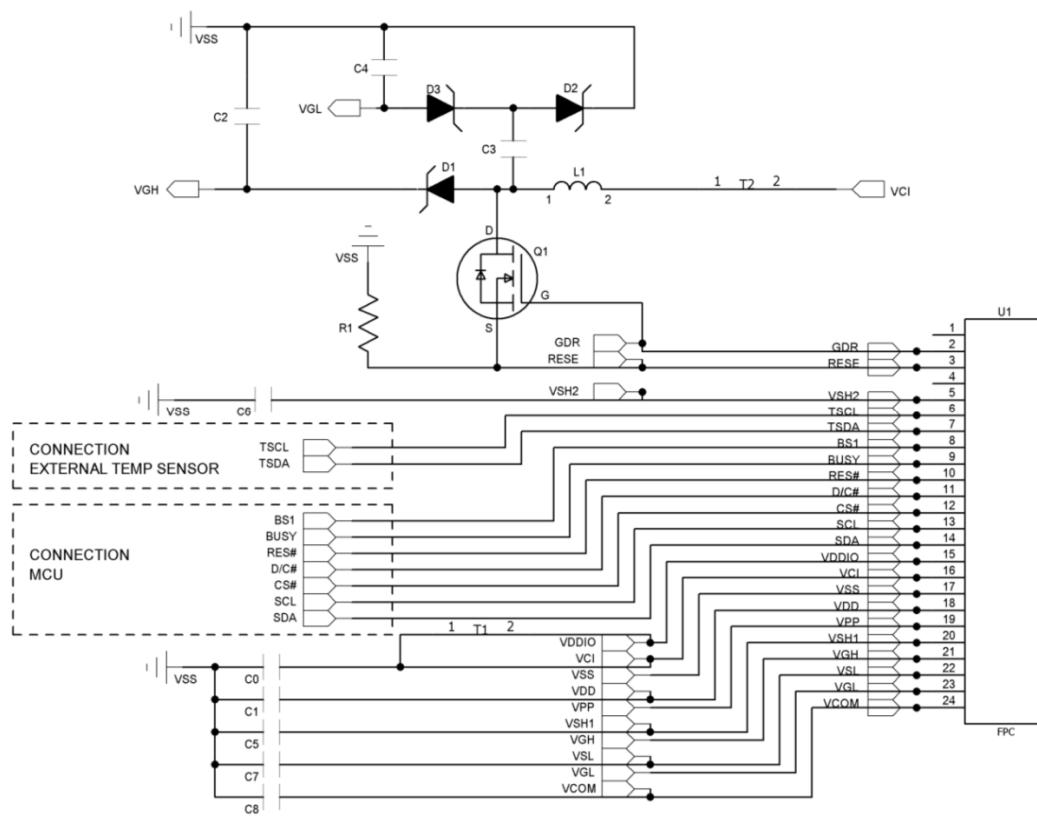


Figure 7-5: SPI timing diagram

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7-4) Reference Circuit



Part Name	Value	Requirements/Reference Part
C0-C1	1uF	X5R/X7R; Voltage Rating : 6V or 25V
C2-C7	1uF	0402/0603/0805; X5R/X7R; Voltage Rating : 25V
C8	1uF	0402/0603/0805; X5R/X7R; Voltage Rating : 25V
R1	2.2 ohm	0402/0603/0805; 1% variation, $\geq 0.05W$
D1-D3	Diode	MBR0530 1) Reverse DC voltage $\geq 30V$ 2) $I_o \geq 500mA$ 3) Forward voltage $\leq 430mV$
Q1	NMOS	Si1304BDL/NX3008NBK 1) Drain-Source breakdown voltage $\geq 30V$ 2) $V_{gs(th)} = 0.9V$ (Typ), $1.3V$ (Max) 3) $R_{ds(on)} \leq 2.1\Omega$ @ $V_{gs} = 2.5V$
L1	47uH	CDRH2D18 / LDNP-470NC $I_o = 500mA$ (Max)
U1	0.5mm ZIF socket	24pins, 0.5mm pitch

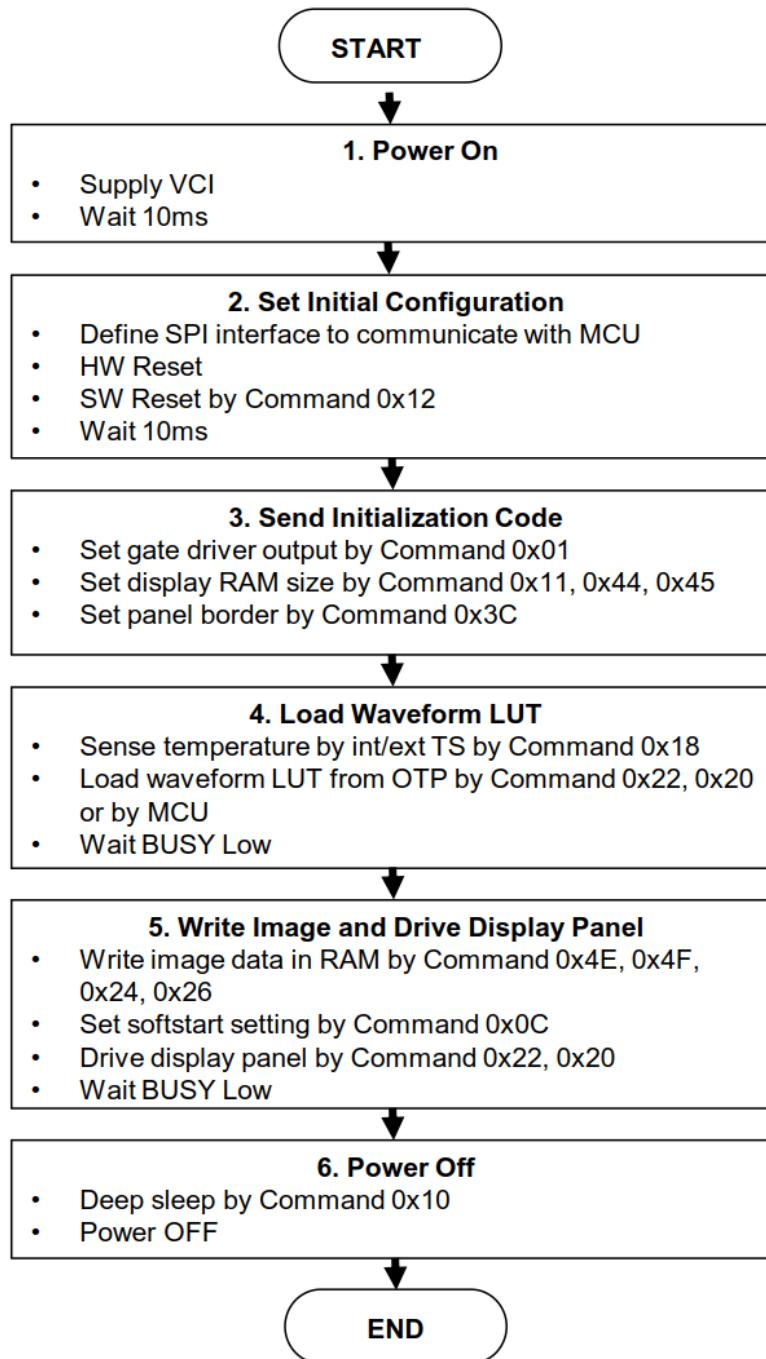
Remarks:

- 1) The recommended component value and reference part in Table is subject to change depending on panel loading.
- 2) Customer is required to review if the selected component value and part is suitable for their application.

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8. Operation Flow and Code Sequence

8-1) General operation flow to drive display panel



9. Optical Specifications

9-1) Specifications

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	9-1
CR	Contrast Ratio	Indoor	8:1		-		9-2
GN	2Grey Level	-		DS+(WS-DS)*n(m-1)			9-3
T update	Image update time	at 25 °C		3	-	sec	
Life		Topr		1000000times or 5years			

Notes: 9-1. Luminance meter: Eye-One Pro Spectrophotometer.

9-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

9-3 WS: White state, DS: Dark state

10. Handling, Safety and Environment Requirements

WARNING

The display glass may break when it is dropped or bumped on a hard surface. Handle with care.

Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.

Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status

Product specification	The data sheet contains final product specifications.
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Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134).

Stress above one or more of the limiting values may cause permanent damage to the device.

These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

Product Environmental certification

RoHS

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11.Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = 50°C, RH=35% for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the high temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard# IEC 60 068-2-2Bp.	When experiment finished, the EPD must meet electrical performance standards.
2	Low-Temperature Operation	T = 0°C for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the low temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard# IEC 60 068-2-2Ab.	When experiment finished, the EPD must meet electrical performance standards.
3	High-Temperature Storage	T = +70°C, RH=35% for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the high temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard# IEC 60 068-2-2Bp.	When experiment finished, the EPD must meet electrical performance standards.
4	Low-Temperature Storage	T = -25°C for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the low temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard# IEC 60 068-2-2Ab	When experiment finished, the EPD must meet electrical performance standards.
5	High Temperature, High-Humidity Operation	T=+40°C, RH=80% for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard# IEC 60 068-2-3CA.	When experiment finished, the EPD must meet electrical performance standards.
6	High Temperature, High-Humidity Storage	T=+50°C, RH=80% for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard# IEC 60 068-2-3CA.	When experiment finished, the EPD must meet electrical performance standards.

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7	Temperatur e Cycle	<p style="text-align: center;">[-25°C 30mins] →[Temperature rise 30mins] [+70°C,RH=35% 30mins] →[Temperature drop 30mins], 1cycle=2hrs, 50 cycles Test in white pattern</p>	<ol style="list-style-type: none"> 1. Samples are put in the Temp & Humid. Environmental Chamber. Temperature cycle starts with -25°C, storage period 30 minutes. After 30 minutes, it needs 30min to let temperature rise to 60 °C . After 30min, temperature will be adjusted to 60°C,RH=35% and storage period is 30 minutes. After 30 minutes, it needs 30min to let temperature rise to -25 °C. One temperature cycle (2hrs) is complete. 2. Temperature cycle repeats 50 times. 3. When 50 cycles finished, the samples will be taken out from experiment chamber and set aside a few minutes. As EPDs return to room temperature, tests will observe the appearance, and test electrical and optical performance based on standard# IEC 60 068-2-14NB. 	When experiment finished, the EPD must meet electrical performance standards.
8	UV exposure Resistance	765 W/m ² for 168 hrs,40°C	Standard# IEC 60 068-2-5 Sa	
9	Electrostatic discharge	Machine Model: +/-250V, 0Ω, 200PF	Standard# IEC61000-4-2	
10	Package Vibration	1.04G, Frequency : 10~500Hz Direction : X, Y, Z Duration:1hours in each direction	Full packed for shipment	
11	Package Drop Impact	Drop from height of 122 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment	

Actual EMC level to be measured on customer application.

Note: (1) The protective film must be removed before temperature test.

(2) There's temperature vs display quality limitation in our display module, we guarantee 1 pixel display quality from 5°C ~ 30°C, and 2 pixel display quality for 0°C~ 5°C & 30°C ~ 40°C.

(3) In order to make sure the display module can provide the best display quality, the update should be made after putting the display module in stable temperature environment for 4 hours at 25°C.

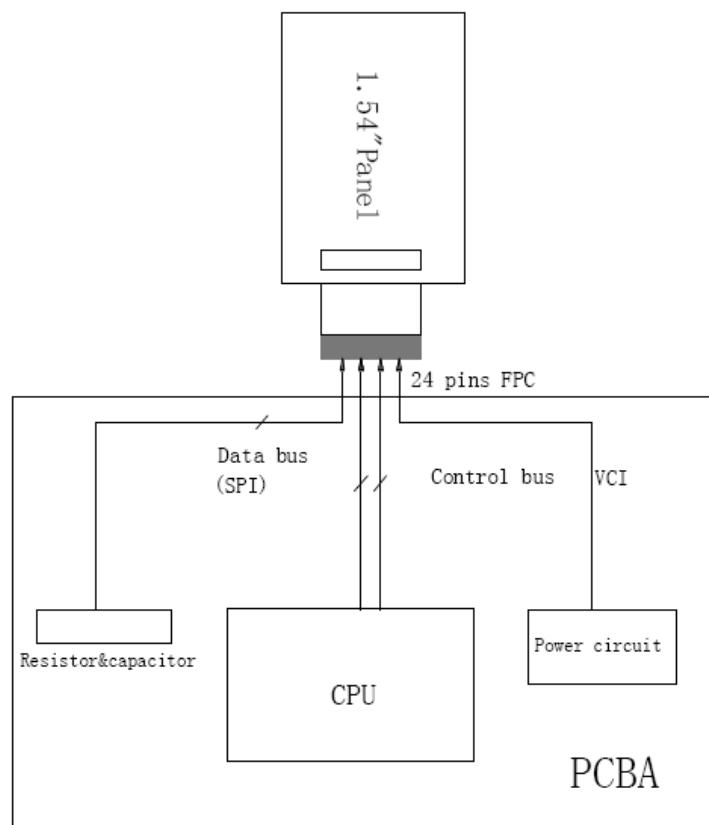
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12. Block Diagram





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13. Point and line standard

Shipment Inseption Standard

Part-A: Active area

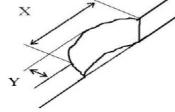
Part-B: Border area

Equipment: Electrical test fixture, Point gauge

Outline dimension:

31.8(H) × 37.32(V) × 0.98(D)

Unit: mm

Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle	
	23±2°C	55±5%RH	1200~1500Lux	300 mm	35 Sec		
Name	Causes	Spot size			Part-A	Part-B	
Spot	B/W spot in glass or protection sheet, foreign mat. Pin hole	D ≤ 0.15mm			Ignore	Ignore	
		0.15mm < D ≤ 0.25mm			2		
		0.25mm < D			0		
Scratch or line defect	Scratch on glass or Scratch on FPL or Particle is Protection sheet.	Length	Width	Part-A	Ignore		
		L ≤ 1.0mm	W≤0.1 mm	Ignore			
		1.0 mm < L≤ 2.5mm	0.1 mm<W≤ 0.2mm	2			
		2.5 mm < L	0.2mm < W	0			
Air bubble	Air bubble	D1, D2 ≤ 0.15 mm			Ignore	Ignore	
		0.15 mm < D1,D2 ≤ 0.2mm			2		
		0.2mm < D1, D2			0		
Side Fragment		 $X \leq 3\text{mm}$, $Y \leq 0.5\text{mm}$ & display is ok, Ignore					

Remarks: Spot define: That only can be seen under WS or DS defects.

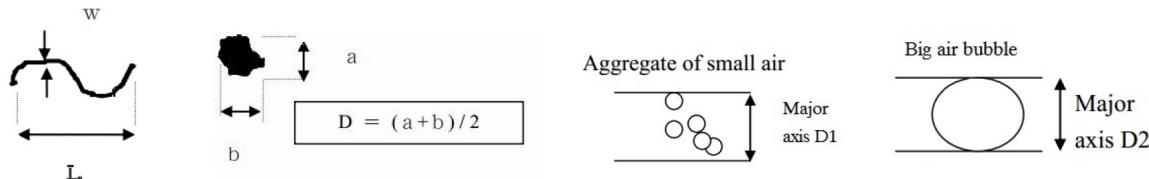
Any defect which is visible under gray pattern or transition process but invisible under black and white is disregarded.

Here is definition of the “Spot” and “Scratch or line defect”.

Spot: $W > 1/4L$ Scratch or line defect: $W \leq 1/4L$

Definition for L/W and D (major axis)

FPC bonding area pad doesn't allowed visual inspection.



Note: AQL = 0.4

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14. Packaging

CUSTOMER'S APPROVED:

DATE: 2020.11.11

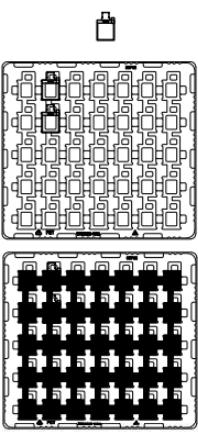
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PRODUCT PART NO.:YMS152152-0150&YMS152152-0154

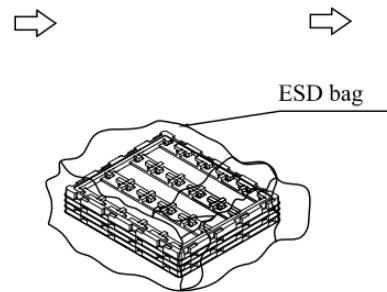
PACKING TYPE: BY PET TRAY(TPET152152-0154A)

PACKLING ORDER:

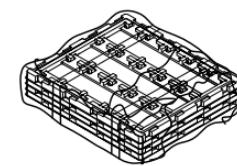
1) Putting 35 pcs Modules on each PET tray. And cover a dedicated EPE film.



2) Putting 12 pcs PET trays together with 1 empty tray on the top of PET tray. Insert in the ESD bag, add desiccant in the ESD bag.

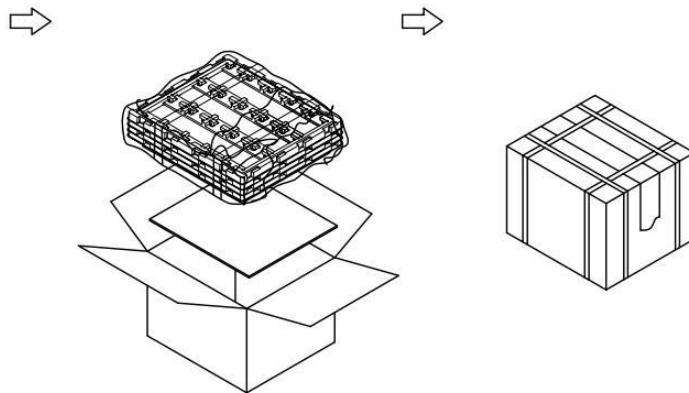


3) the tray together with adhesive tape



4) Putting into one outcarton

5) Packing finished



Note: 35 pcs in a tray, 12 trays in a inner carton, 1 inner cartons in a out carton, so $35 \times 12 \times 1 = 420$ pcs/Outcarton

Dimension (Out carton): 394*344*255mm

	Drw:	Chk:	Apv:

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